# Ampere® Mt. Mitchell Motherboard Overview

In Partnership with Inspur®

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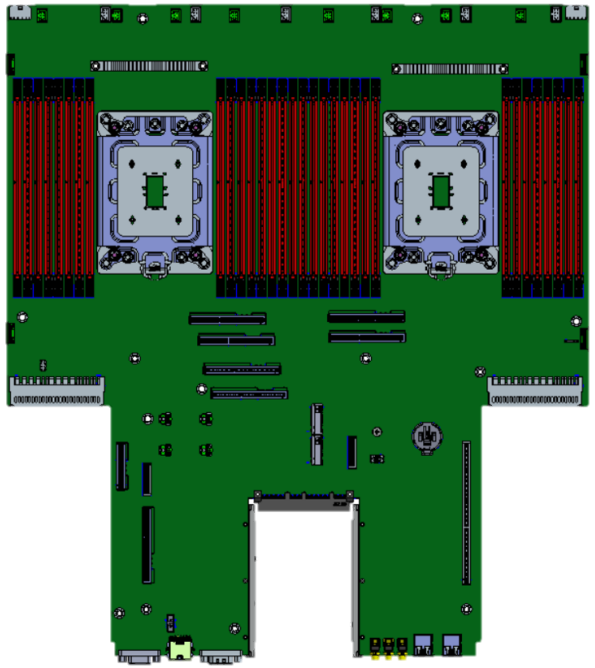
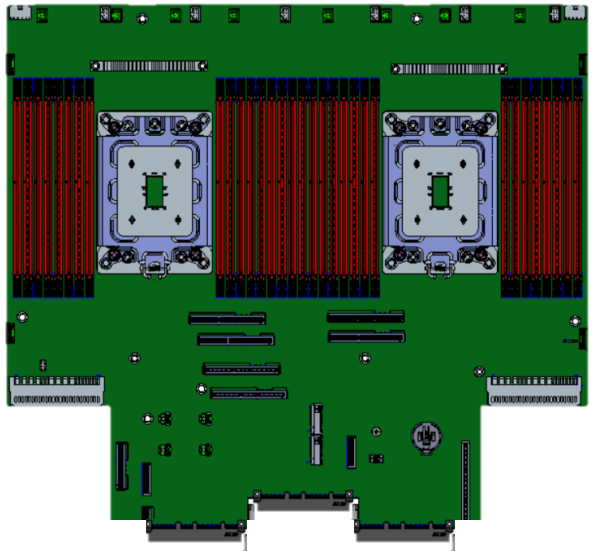
# Ampere® Mt. Mitchell Motherboard Background

- Mt. Jade specification has evolved into DC-MHS

Ampere® Mt. Jade Motherboard Specification



OCP DC-MHS

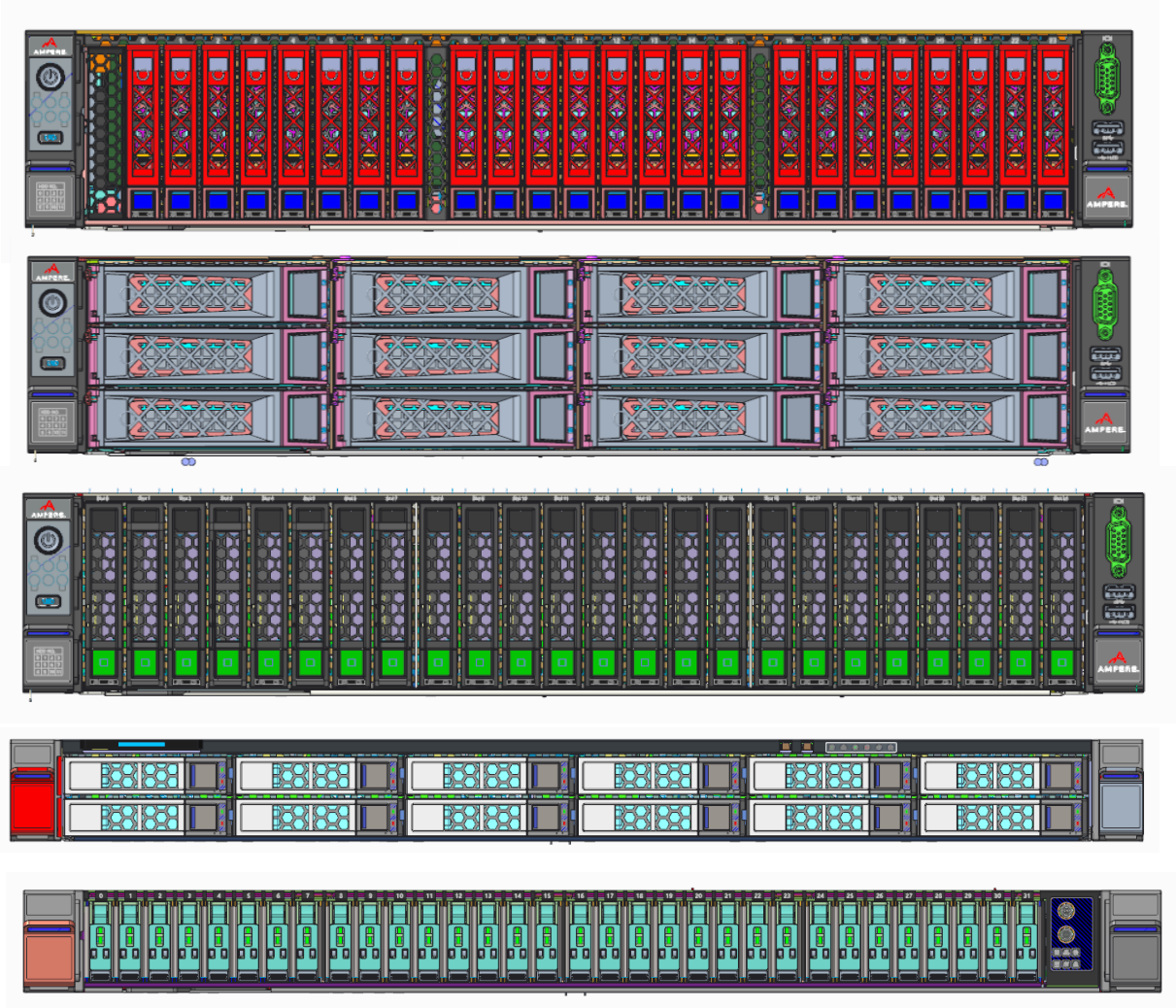


- There is a need for L-shaped implementation for Tier2/Tier3 datacenter that don’t use bus bars. Ampere® proposal is Mt. Mitchell motherboard specification to fill that need

# Ampere® Mt. Mitchell Motherboard Overview

## Proposal for OCP Specification, Hardware Design and Firmware Submission

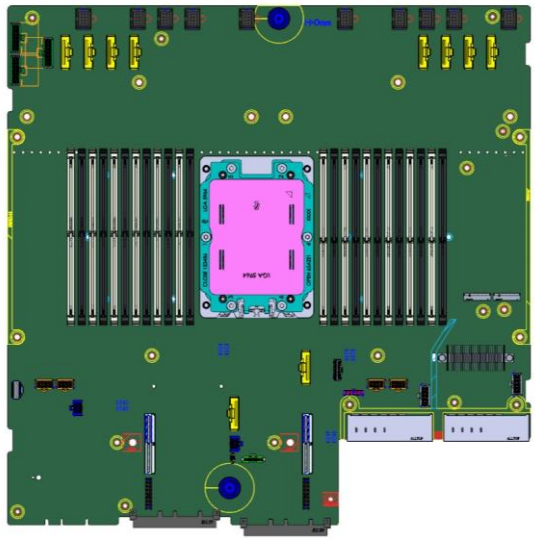
- Ampere® 1-socket and 2-socket spread-core platform design for cloud general compute
- Supports 19” EIA Rack Systems for 1U and 2U chassis
- DDR5 1DPC or 2DPC DIMM support
- PCIe Gen5 with flexibility for front or rear PCIe cabling
- OCP DC-SCM 1.0 upport
- OCP 3.0 NIC support
- Standard CRPS PSU support
- Platform specification to be uploaded to wiki for review



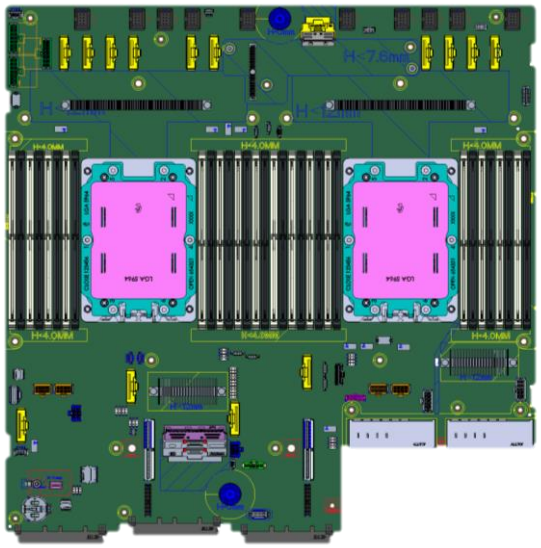
# Mt. Mitchell OCP Motherboard Specification

Dimensions: 424.9 mm / 16.7”W x 422.9mm 16”D?

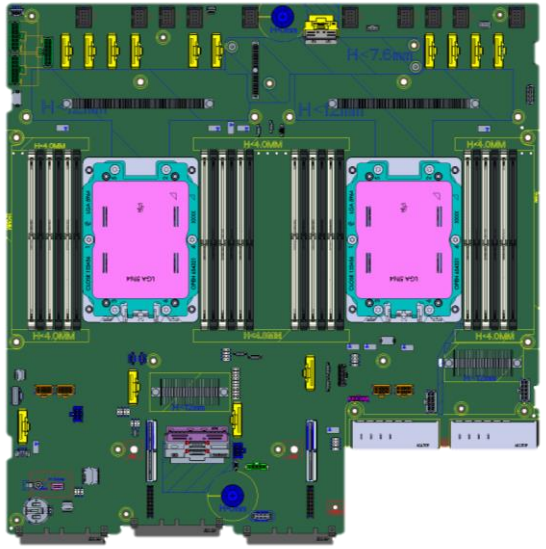
Variation 1: 1S 2DPC (12-DDR channels)



Variation 2: 2S 2DPC (8-DDR channels)



Variation 3: 2S 1DPC (12-DDR channels)

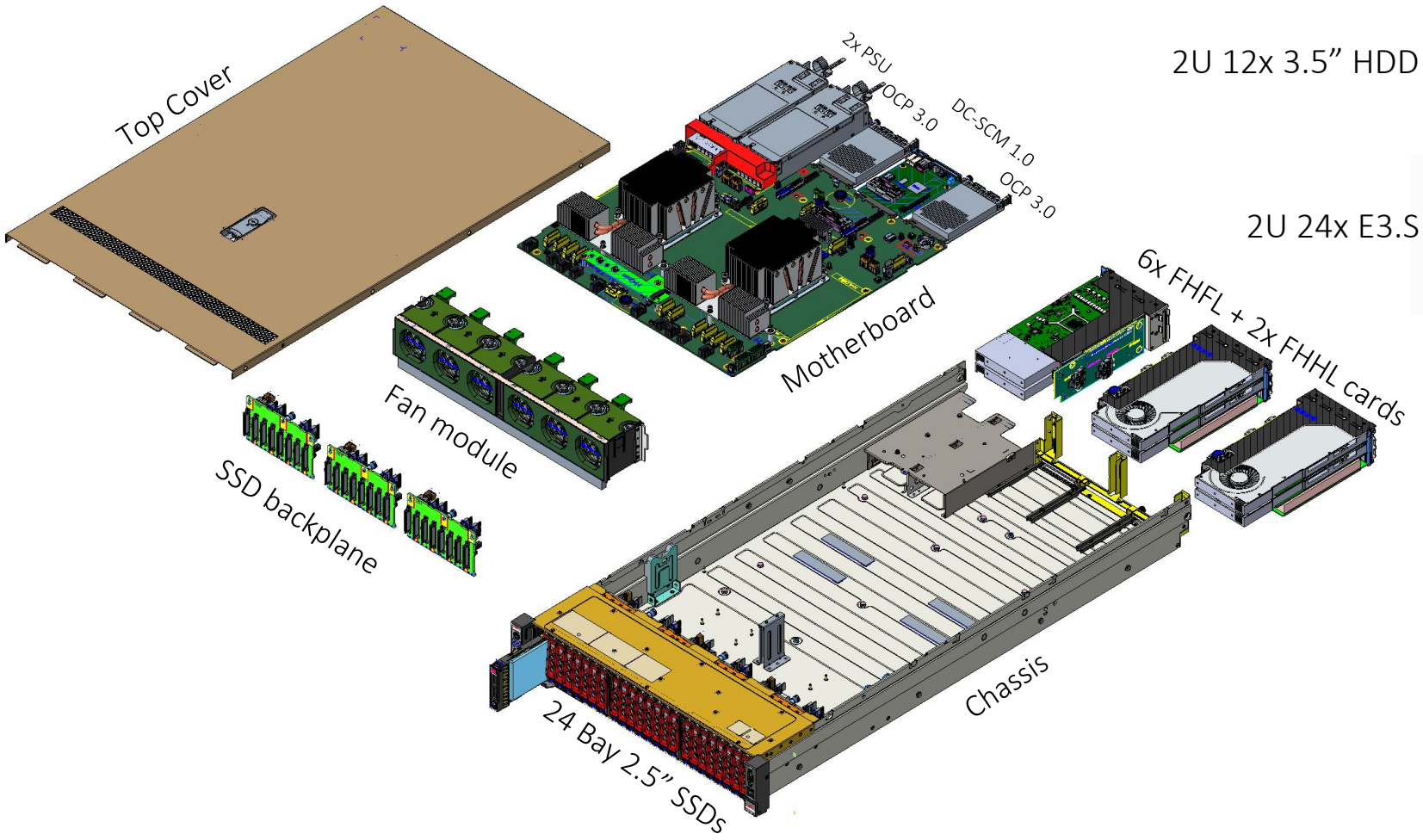


- Support for upto dual redundant CRPS PSUs
- Support for up to two OCP 3.0 NICs
- Support for OCP DC-SCM 1.0 (can also work with DC-SCM 2.0)

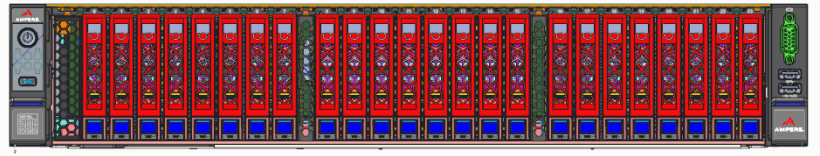
FHHL = Full height half-length PCIE add-in card
FHFL = Full height Full Length PCIE add-in card

# Mt. Mitchell OCP Motherboard in 2U Chassis

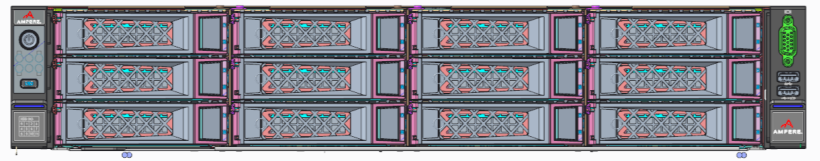
## Variation 1 & 3 Shown



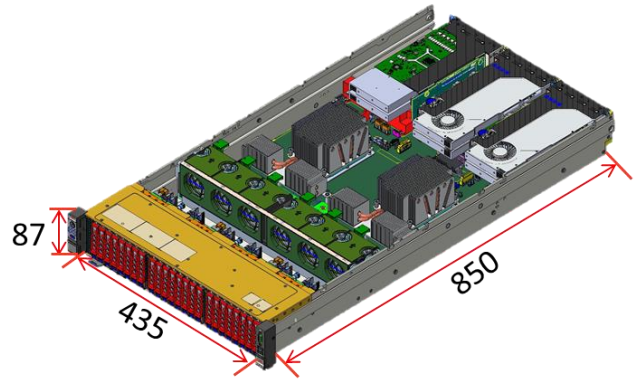

2U 24x NVMe



2U 12x 3.5" HDD



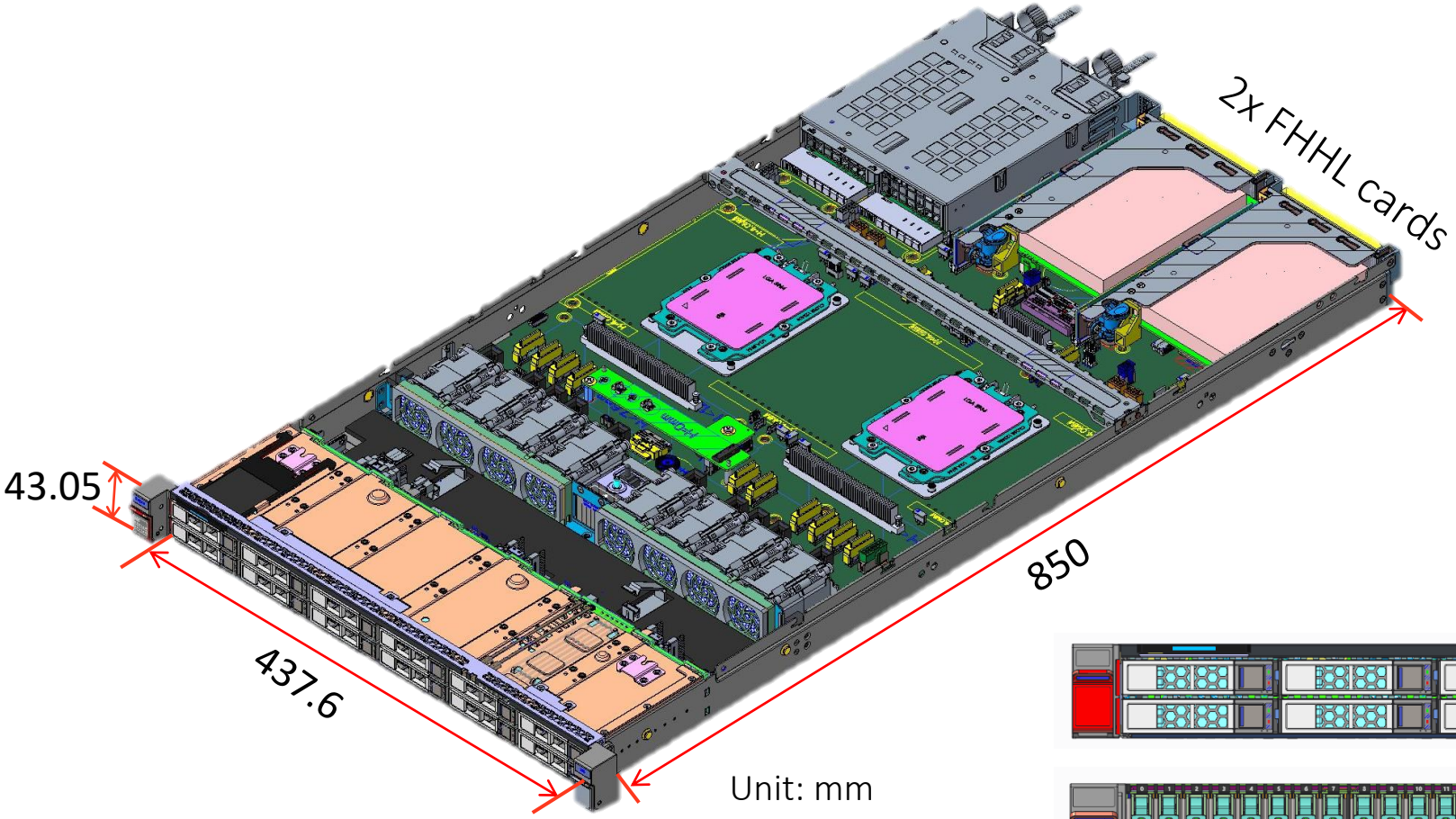
2U 24x E3.S



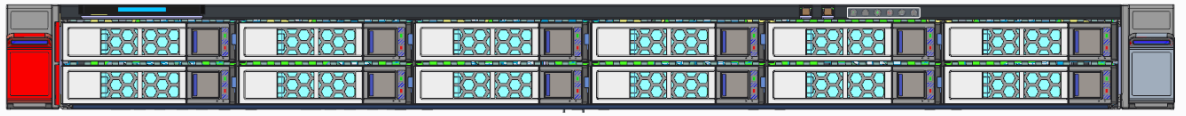

Unit: mm

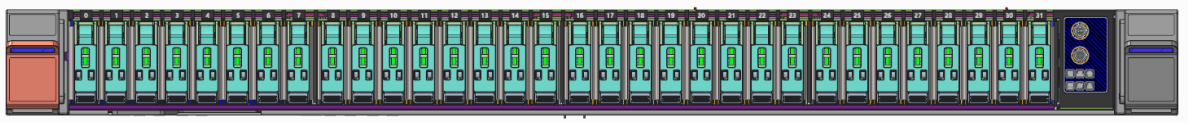
# Mt. Mitchell OCP Motherboard in 1U Chassis

Variation 1 & 3 Shown




1U 12x U.2 NVMe



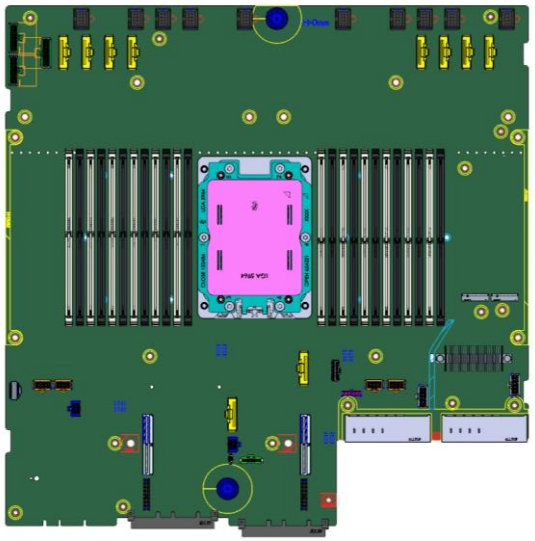


1U 32x E1.S (9.5mm)

# Security and OSF / Arm SystemReady

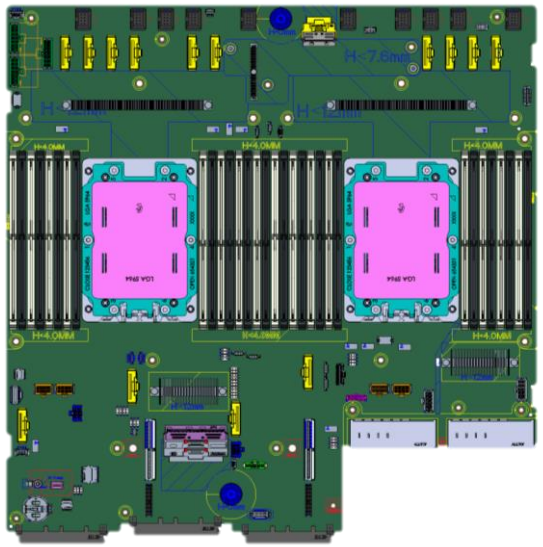
- Mt. Mitchell specification will leverage DC-SCM 1.0
- DC-SCM 1.0 implementation will be supplier specific with regards to Root of Trust (RoT)
- Mt. Mitchell product instance will go through Arm SystemReady compliance

Variation 1: 1S 2DPC (12-DDR channels)



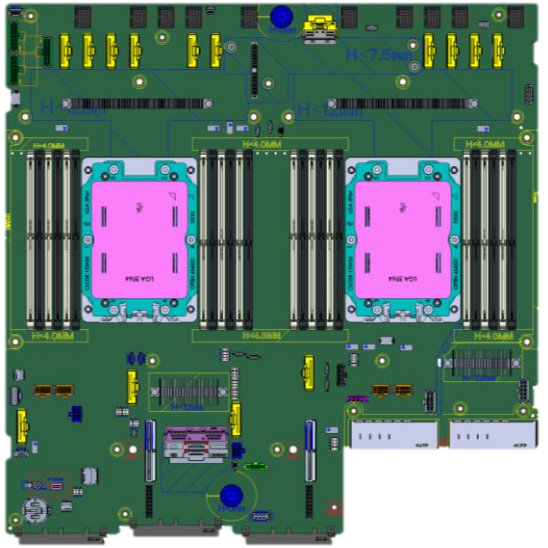
DC-SCM 1.0

Variation 2: 2S 2DPC (8-DDR channels)



DC-SCM 1.0

Variation 3: 2S 1DPC (12-DDR channels)



DC-SCM 1.0

# Ampere® Mt. Mitchell Motherboard Open-source Contribution

**OpenBMC**

Ampere Computing Helpful links and info

- Github: https://github.com/ampere-openbmc
- Mt Jade implementation: https://github.com/ampere-openbmc/openbmc
- Linux kernel changes https://github.com/ampere-openbmc/linux
- SSIF bridge https://github.com/openbmc/ssifbridge
- Ampere's support for various IPMI commands, standard and OEM.https://github.com/ampere-openbmc/ampere-ipmi-oem
- Code for platform hardware interface and control https://github.com/ampere-openbmc/ampere-platform-mgmt
- Other source code that do not fit any permanent category or expect further changes https://github.com/ampere-openbmc/ampere-misc

Effort will be around Redfish and not IPMI

**Tianocore (Github) Project / EDK2 Implementation**

- Helpful links and info
  - Ampere Computing github releases
    - https://github.com/AmpereComputing/edk2
    - https://github.com/AmpereComputing/edk2-platforms
  - Ampere Computing source
    - https://github.com/AmpereComputing/edk2-platforms/tree/ampere/Platform/Ampere
    - https://github.com/AmpereComputing/edk2-platforms/tree/ampere/Silicon/Ampere
  - The above were forked from:
    - https://github.com/tianocore/edk2
    - https://github.com/tianocore/edk2-platforms
- Currently under review by upstream community and this skeleton directory has been set up
  - https://github.com/tianocore/edk2-platforms/tree/master/Platform/Ampere

Ampere® Will Submit Mt. Mitchell Spec, Design, OpenBMC FW and Tianocore/EDK-II to OCP

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