Mt. Olympus

C2020

COVER PAGE

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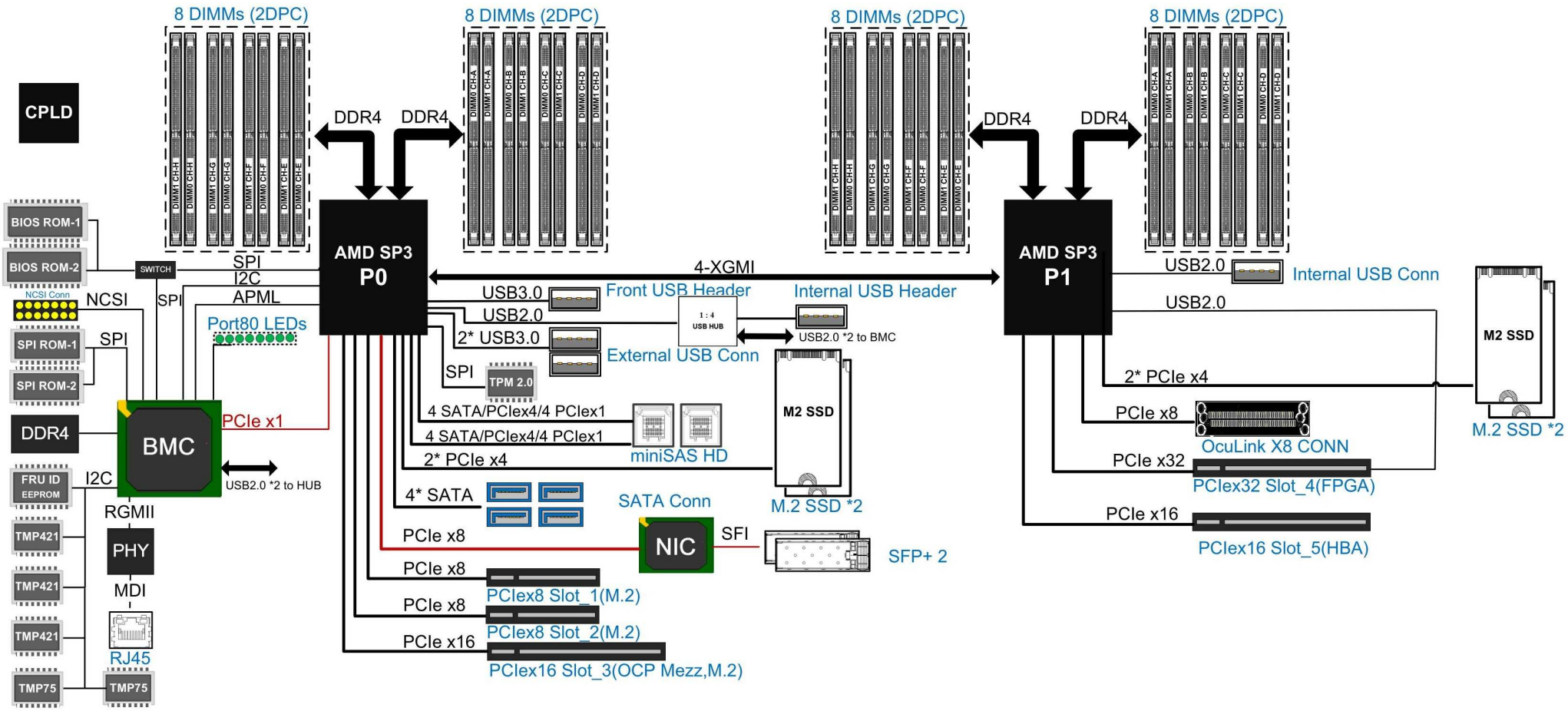

SYSTEM BLOCK DIAGRAM

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SERDES MAPPING

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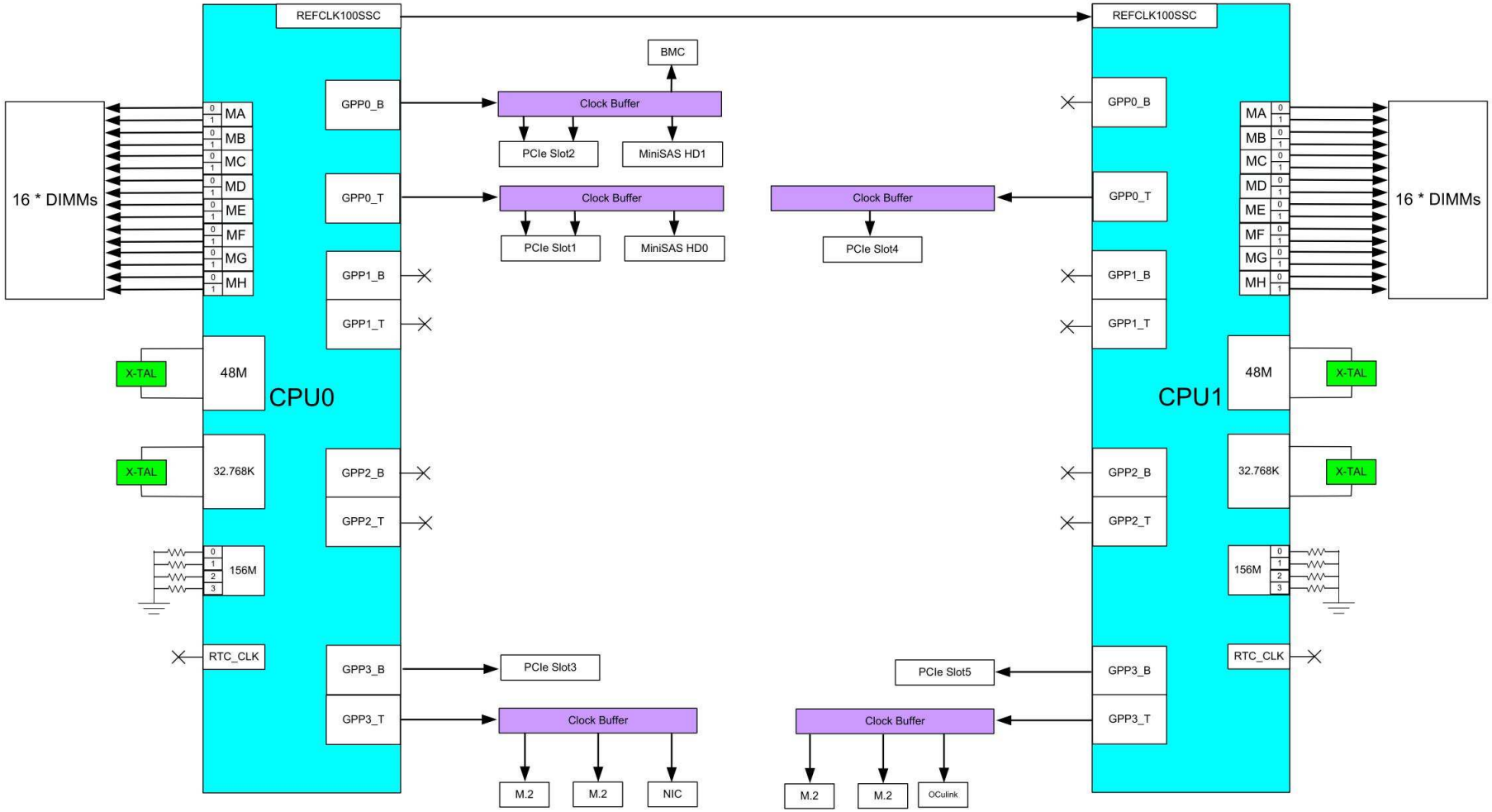

CLK BLOCK DIAGRAM

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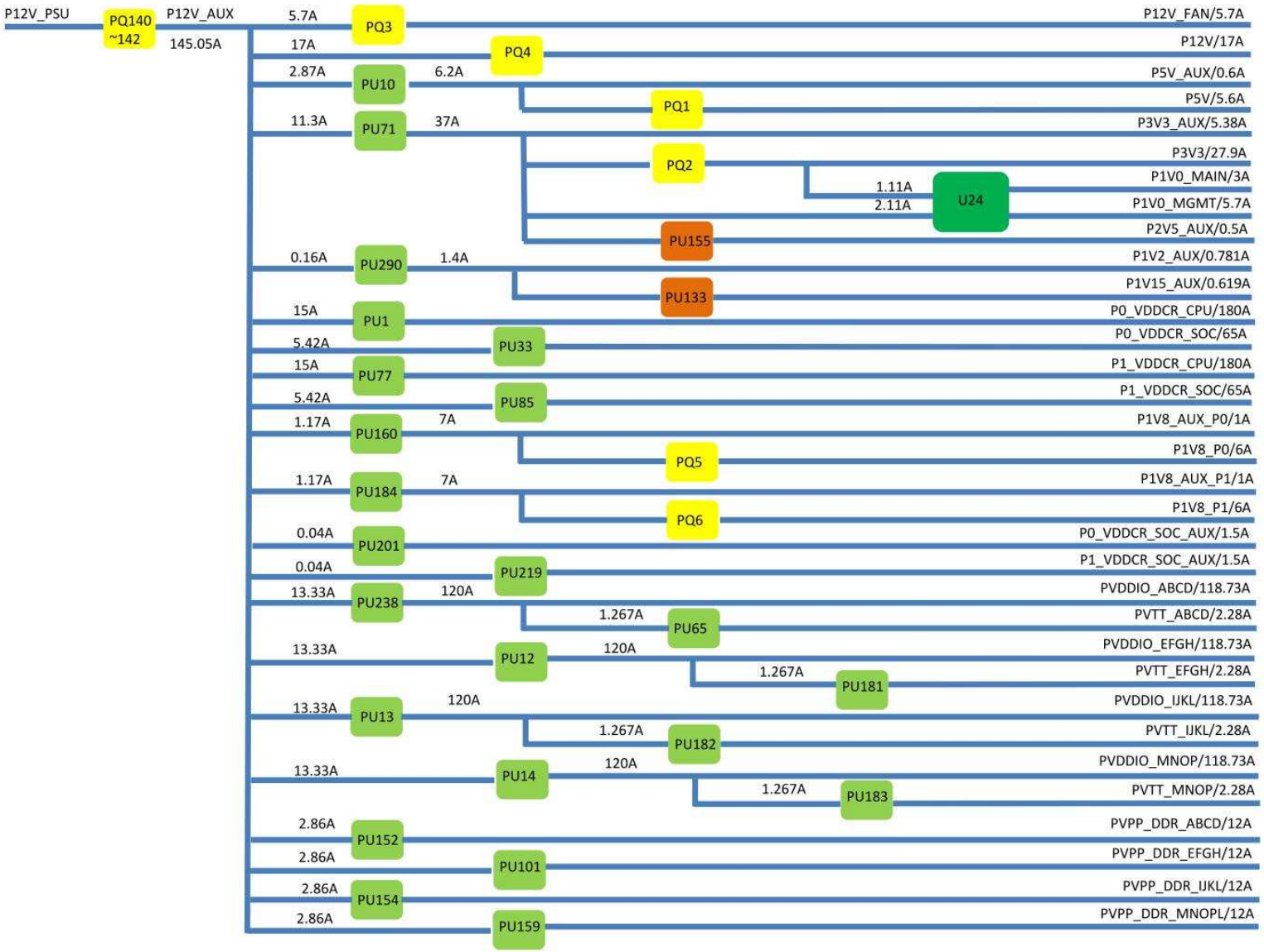

VR BLOCK DIAGRAM

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POWER-ON SEQUENCE

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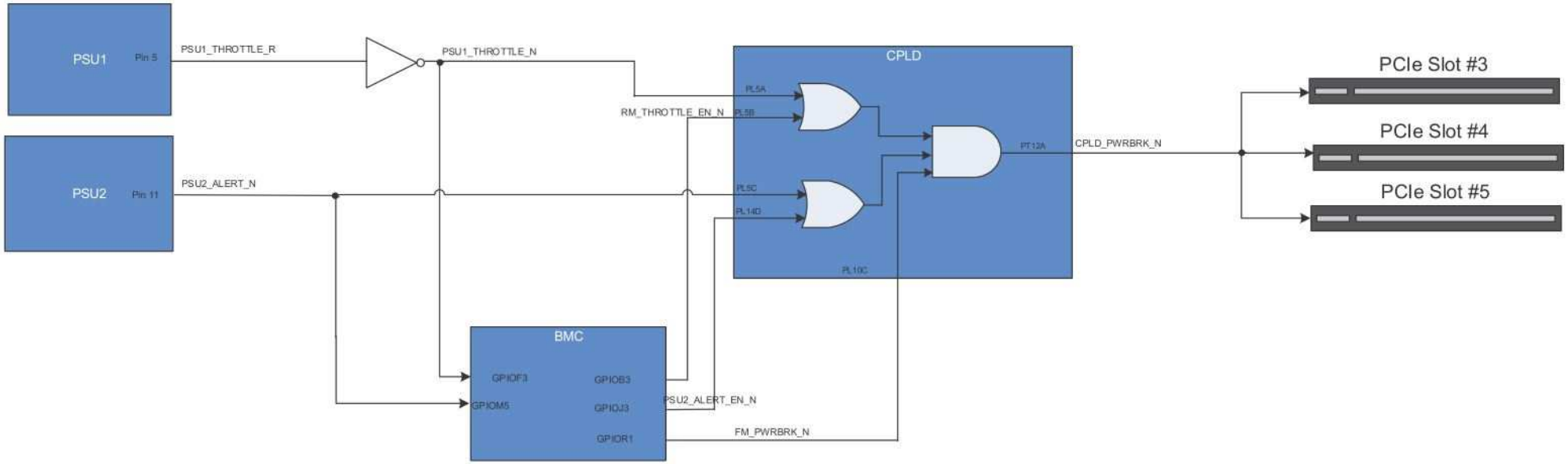
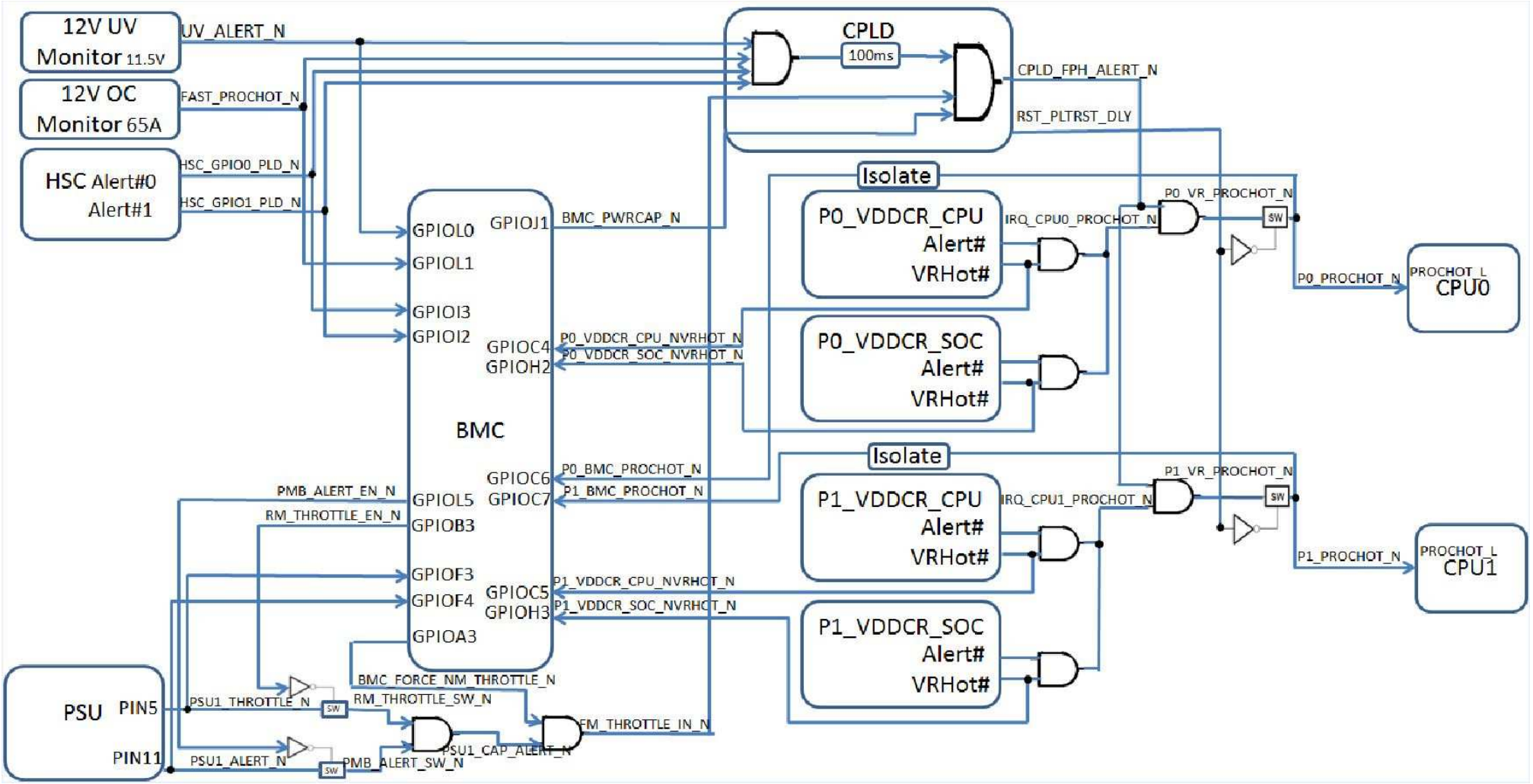
PWRBRK# BLOCK DIAGRAM





PROCHOT BLOCK DIAGRAM

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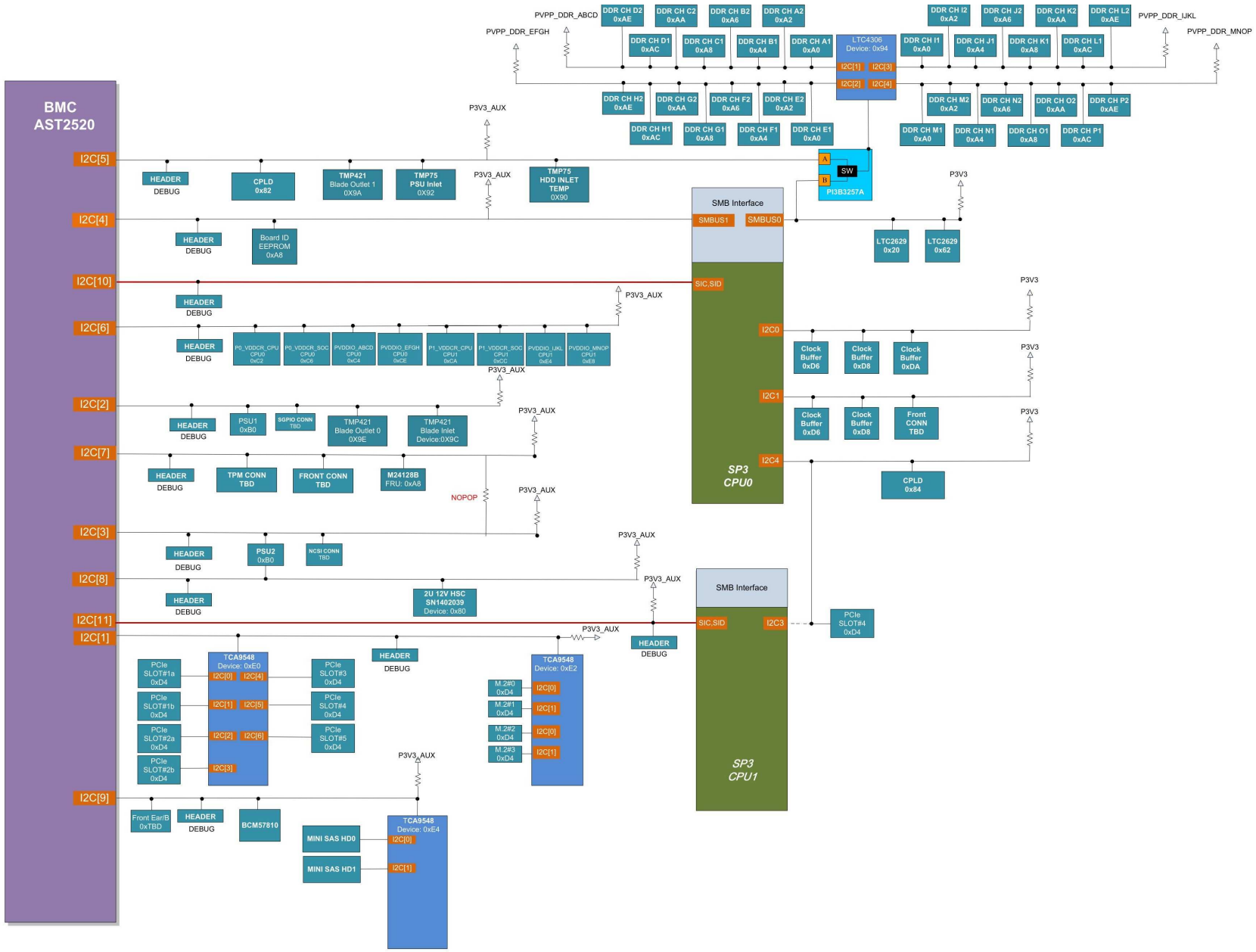

SMBUS DIAGRAM

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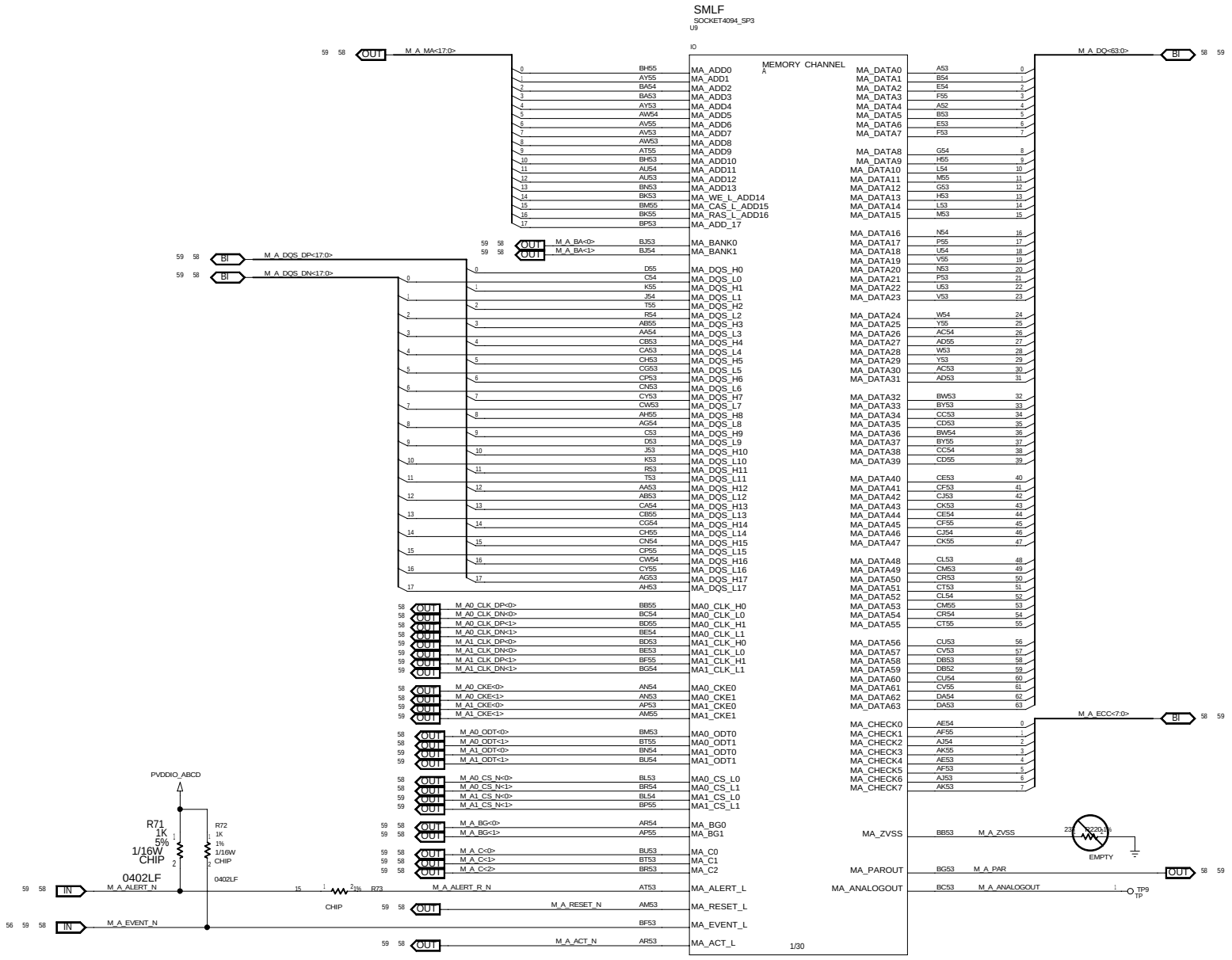

DESIGN NOTE:

DGA^0000050

P0 MEMORY CHA (1 OF 19)

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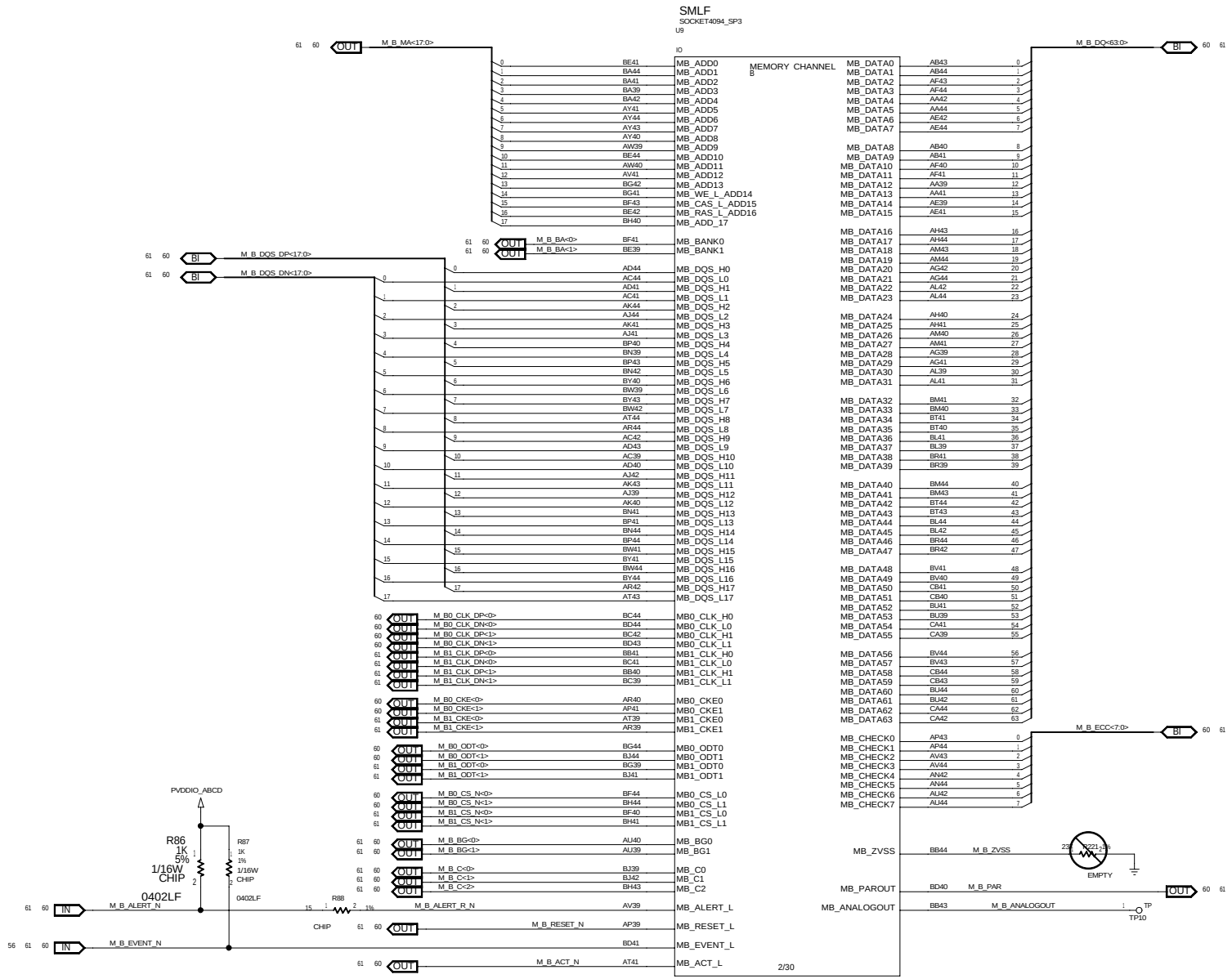

P0 MEMORY CHB (2 OF 19)

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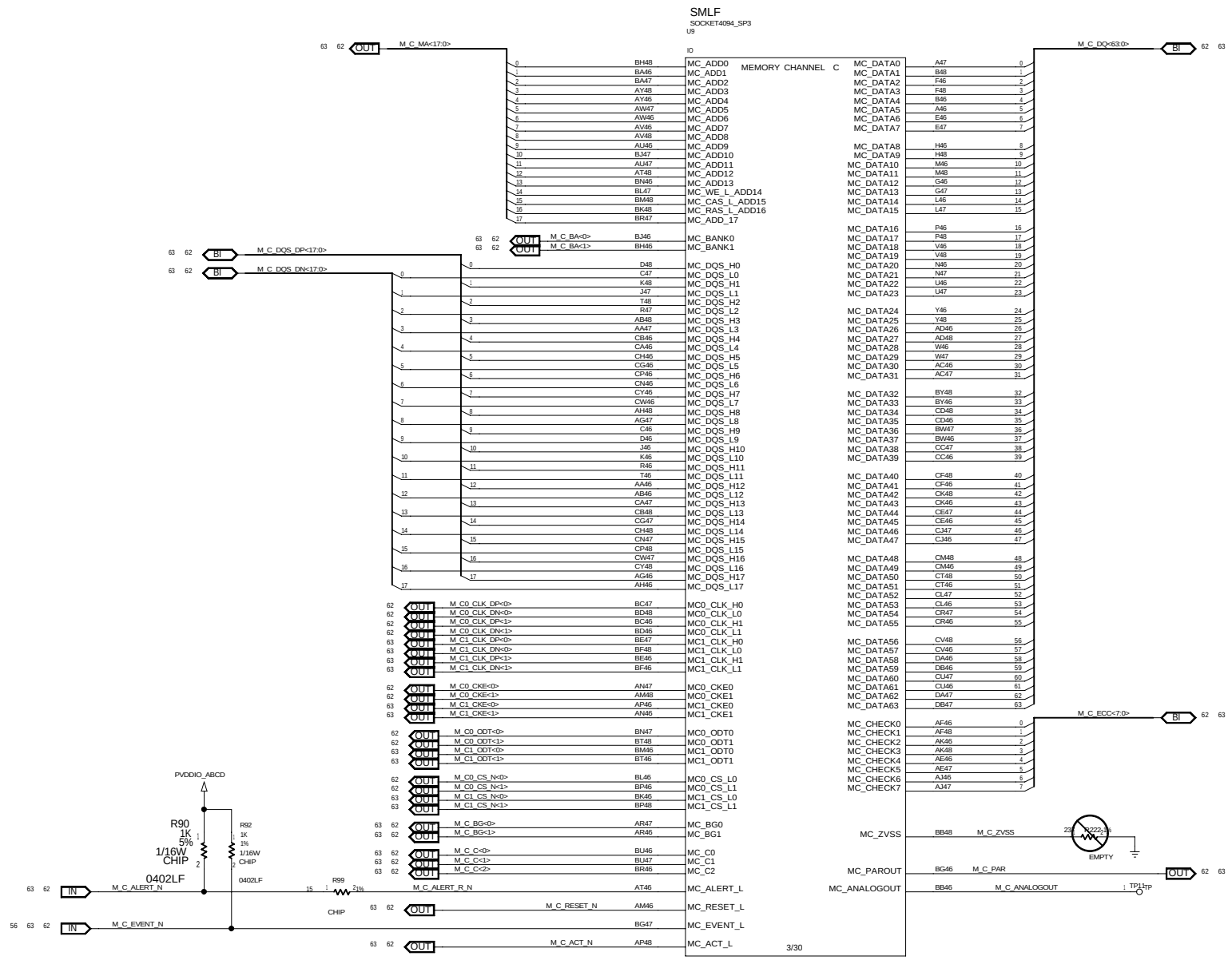

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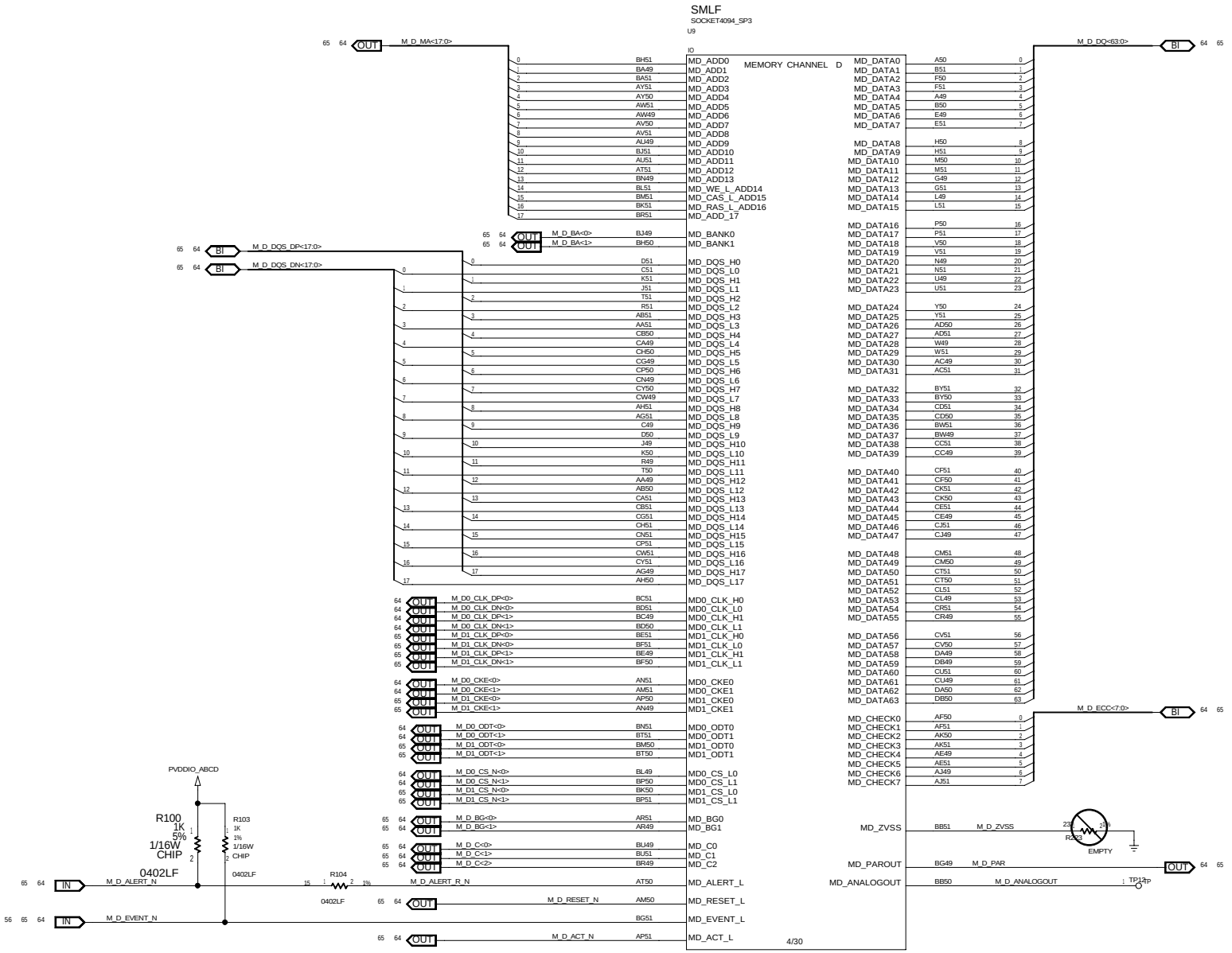

P0 MEMORY CHD (4 OF 19)

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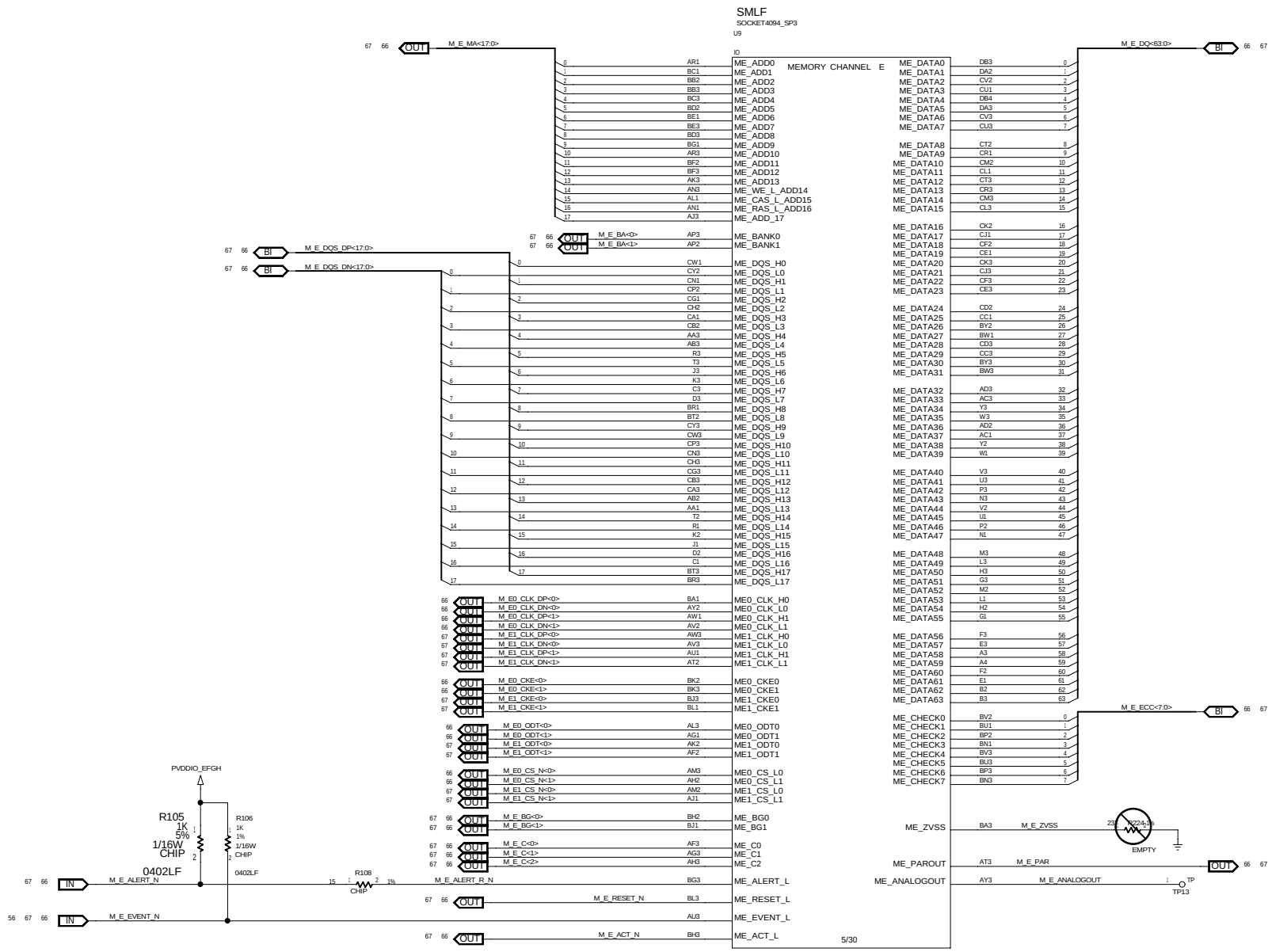

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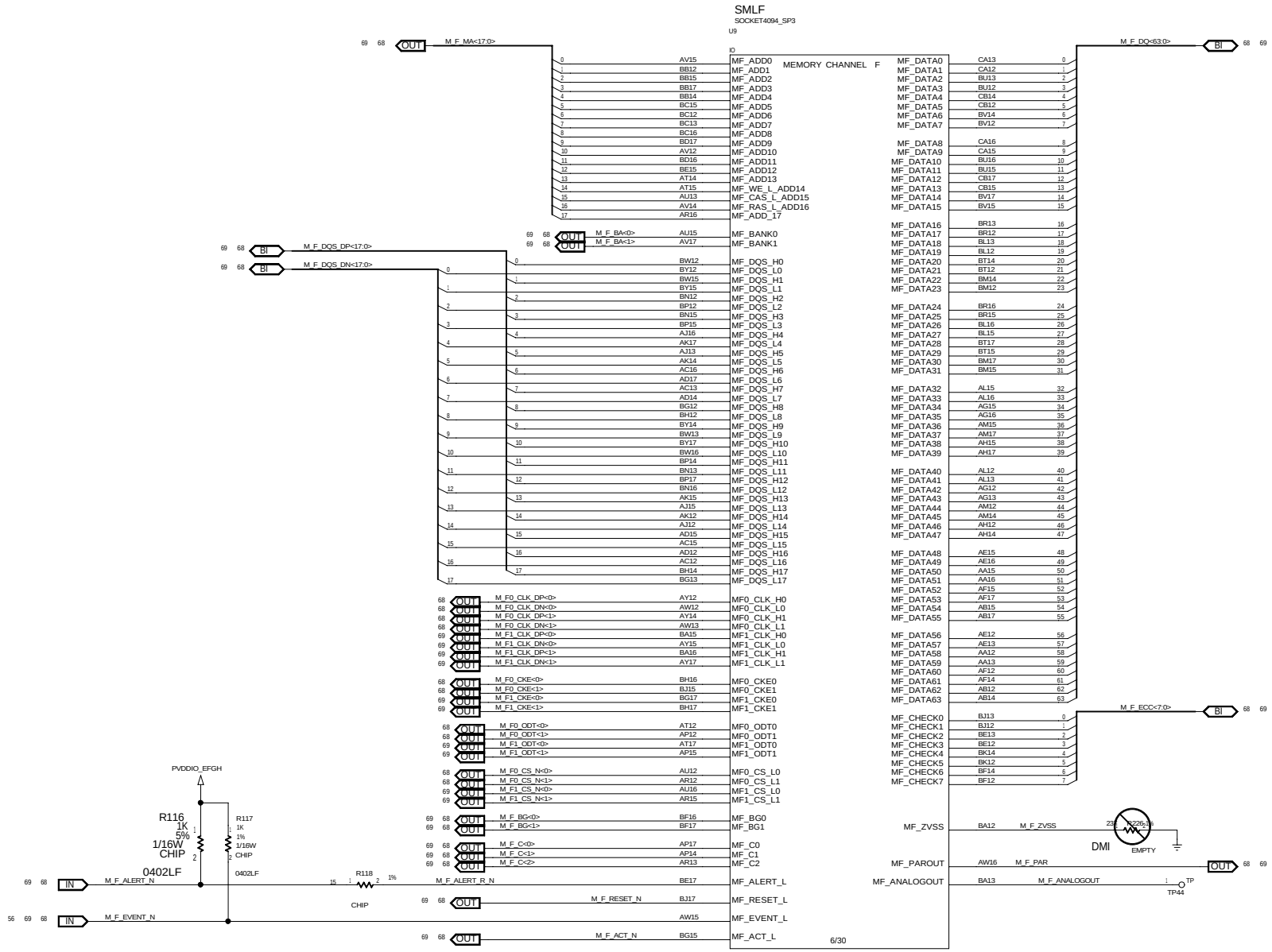

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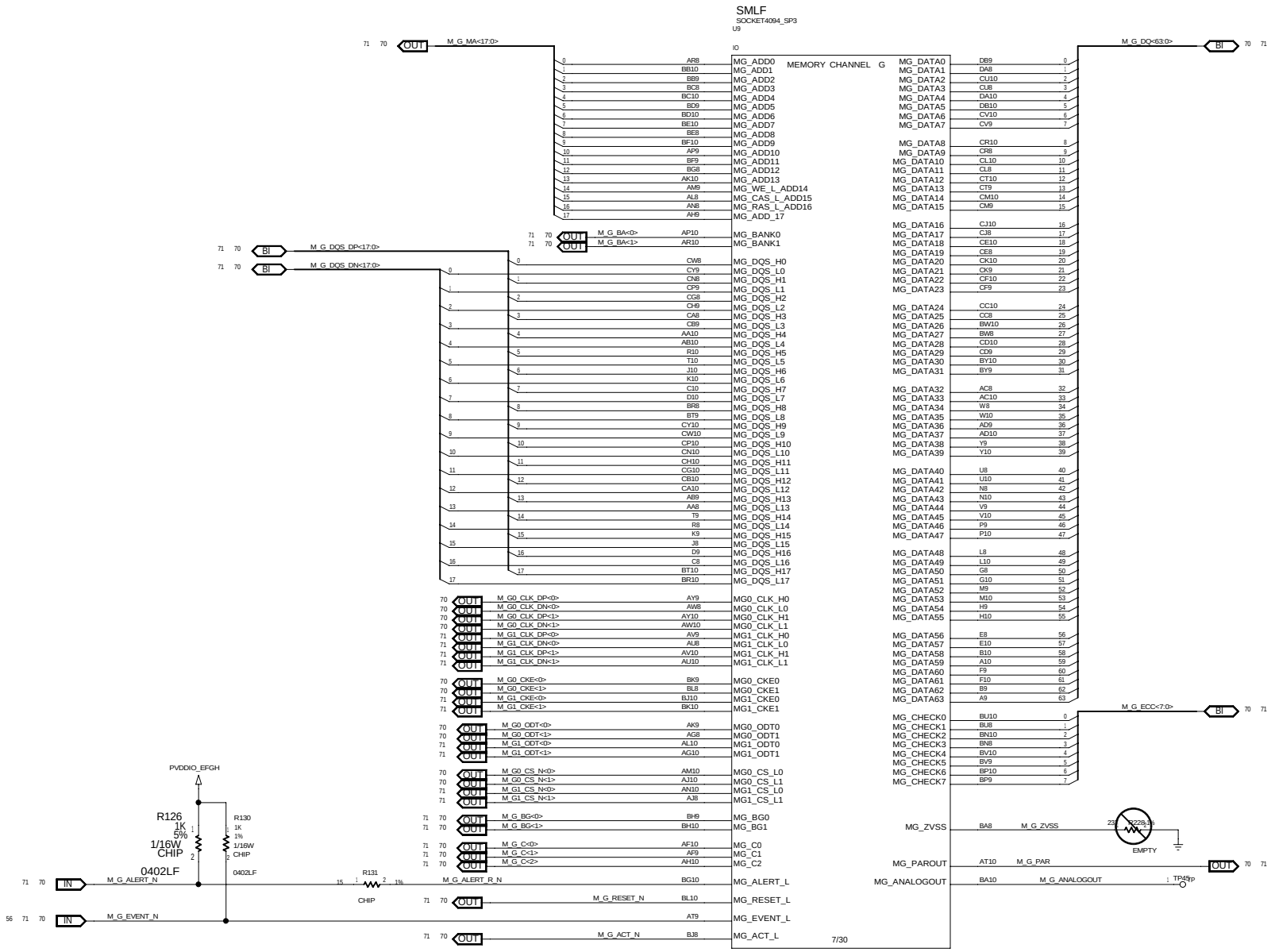

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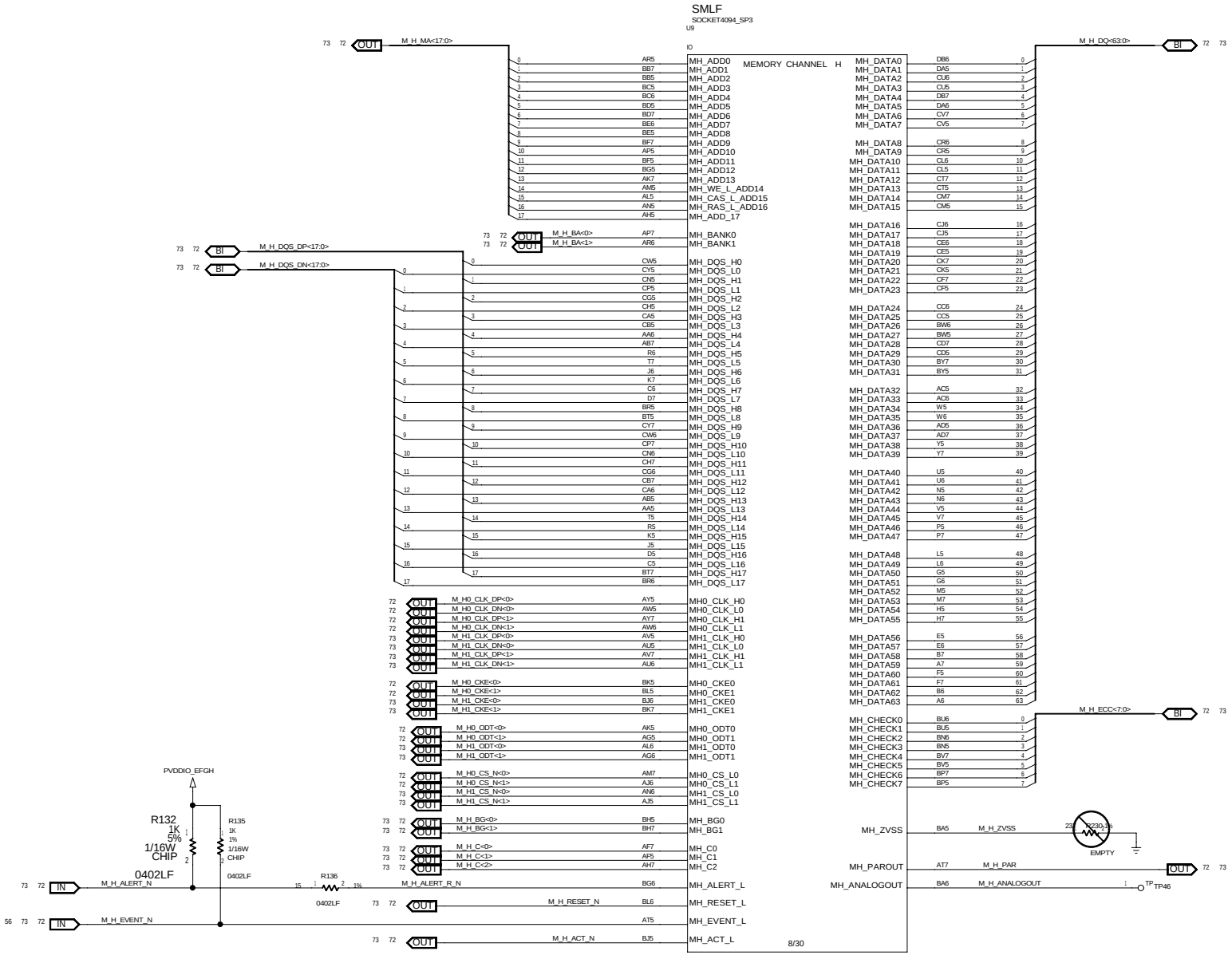

P0 MEMORY CHH (8 OF 19)

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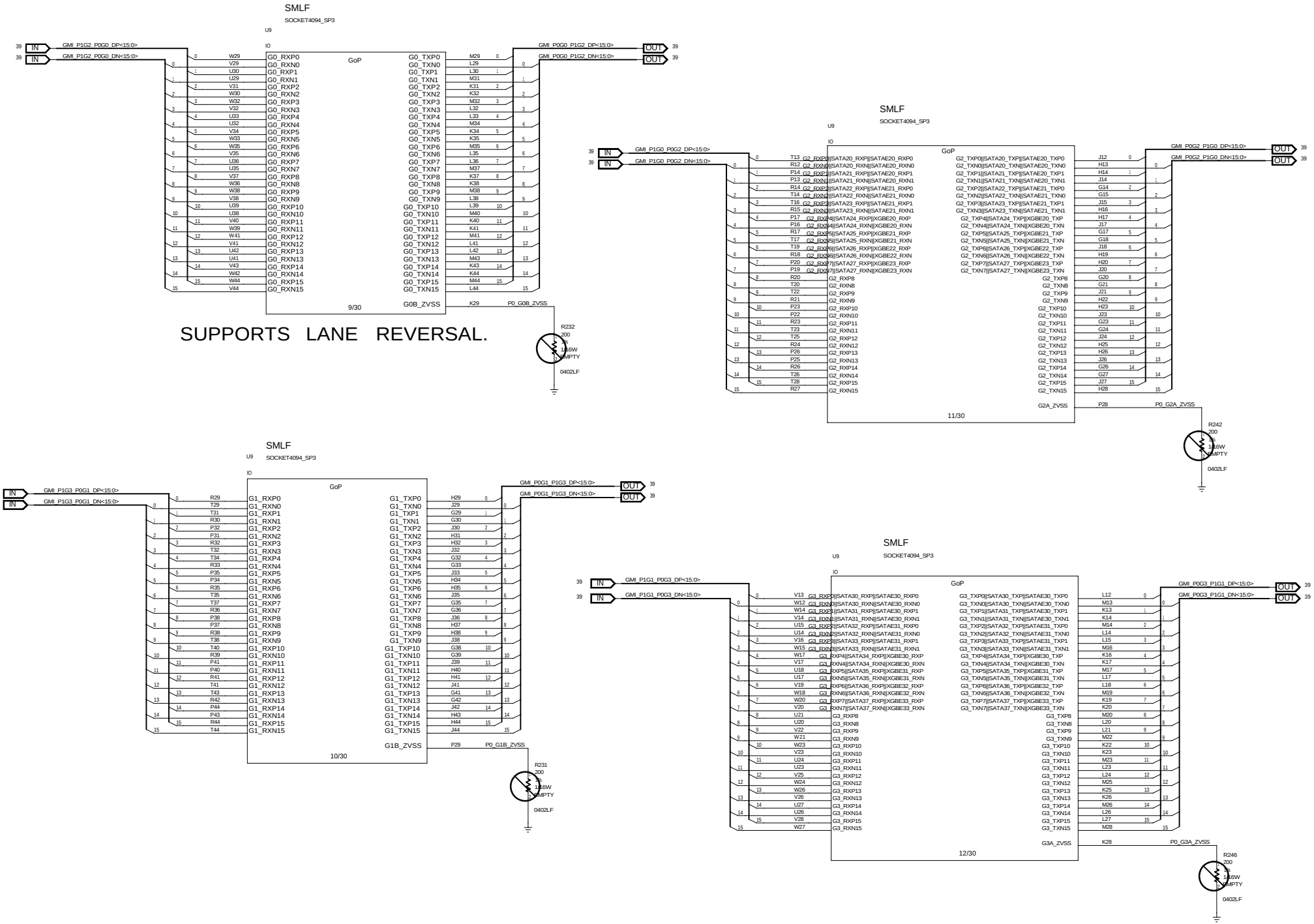

P0 xGMI (9 OF 19)

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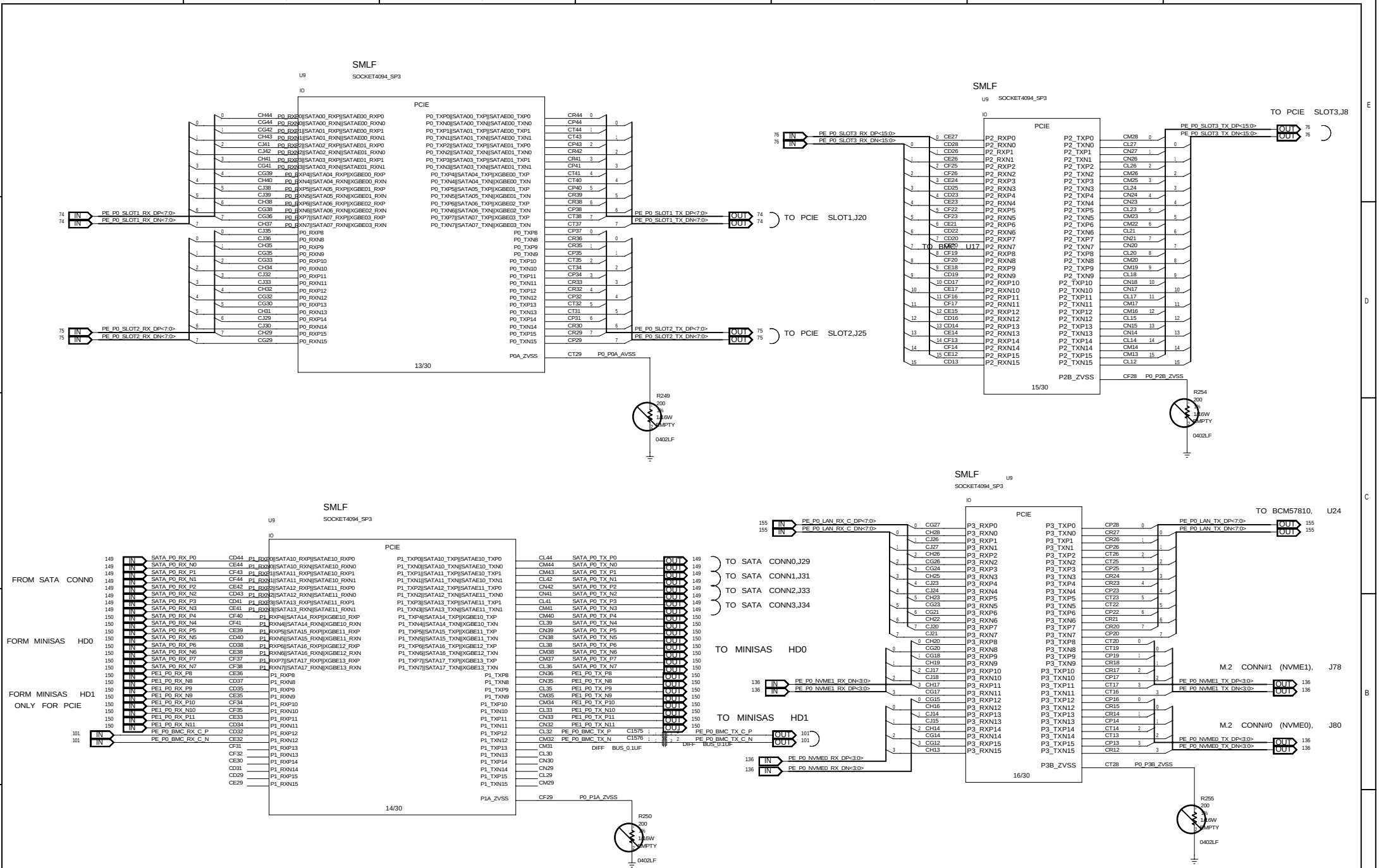

P0 PCIE & SATA (10 OF 19)

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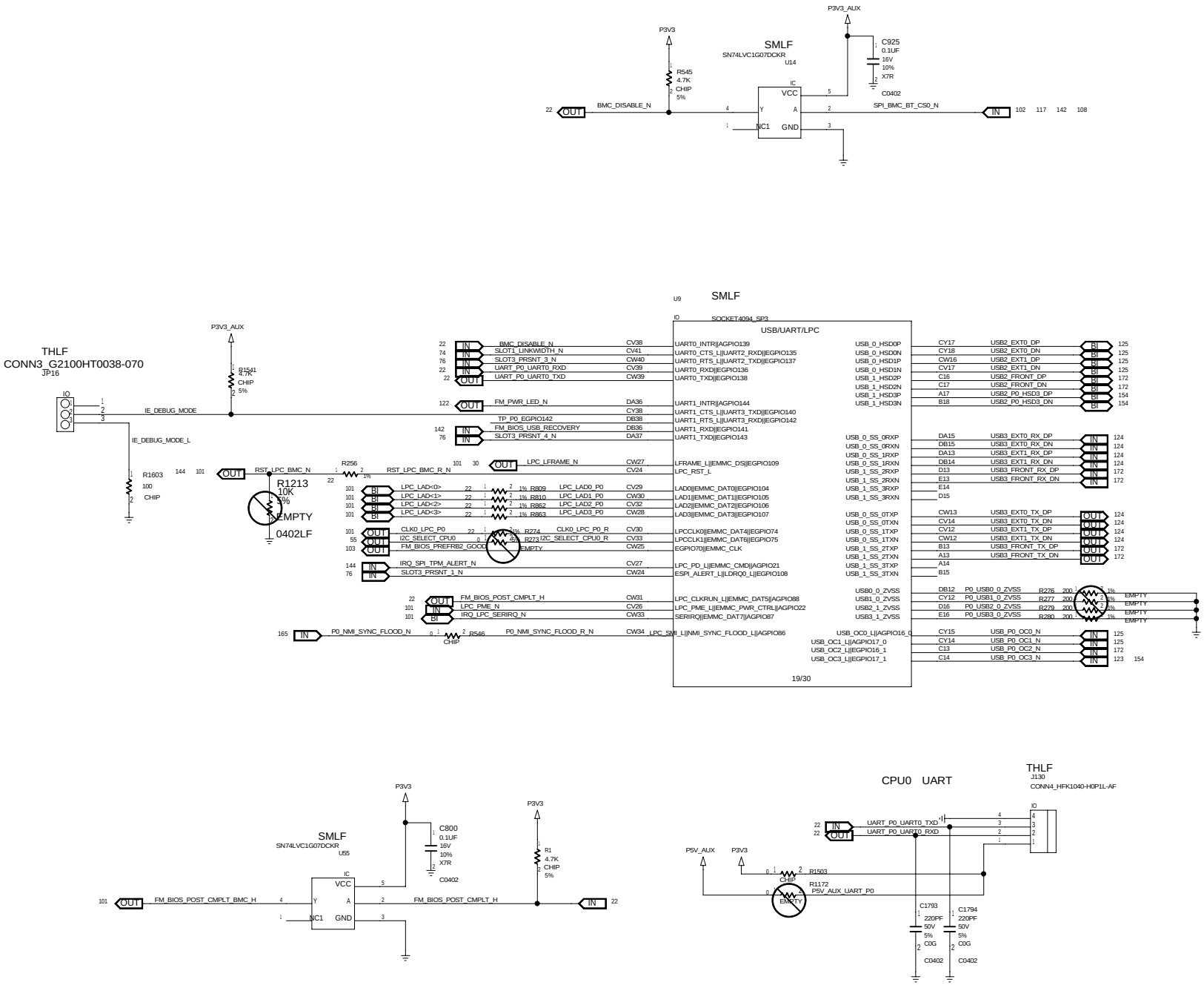

P0 USB, LPC & UART (11 OF 19)

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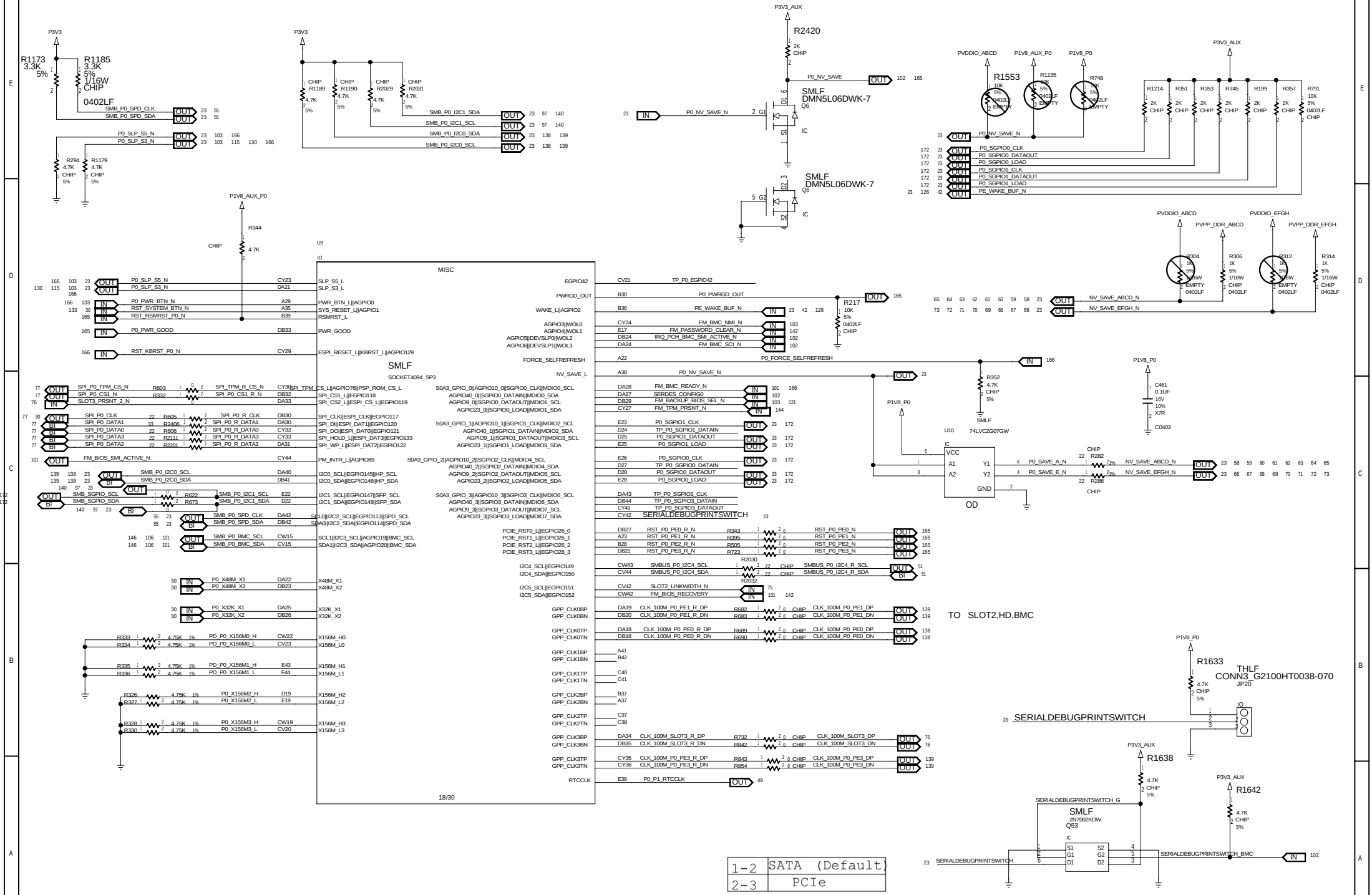

P0 MISC 1 (12 OF 19)

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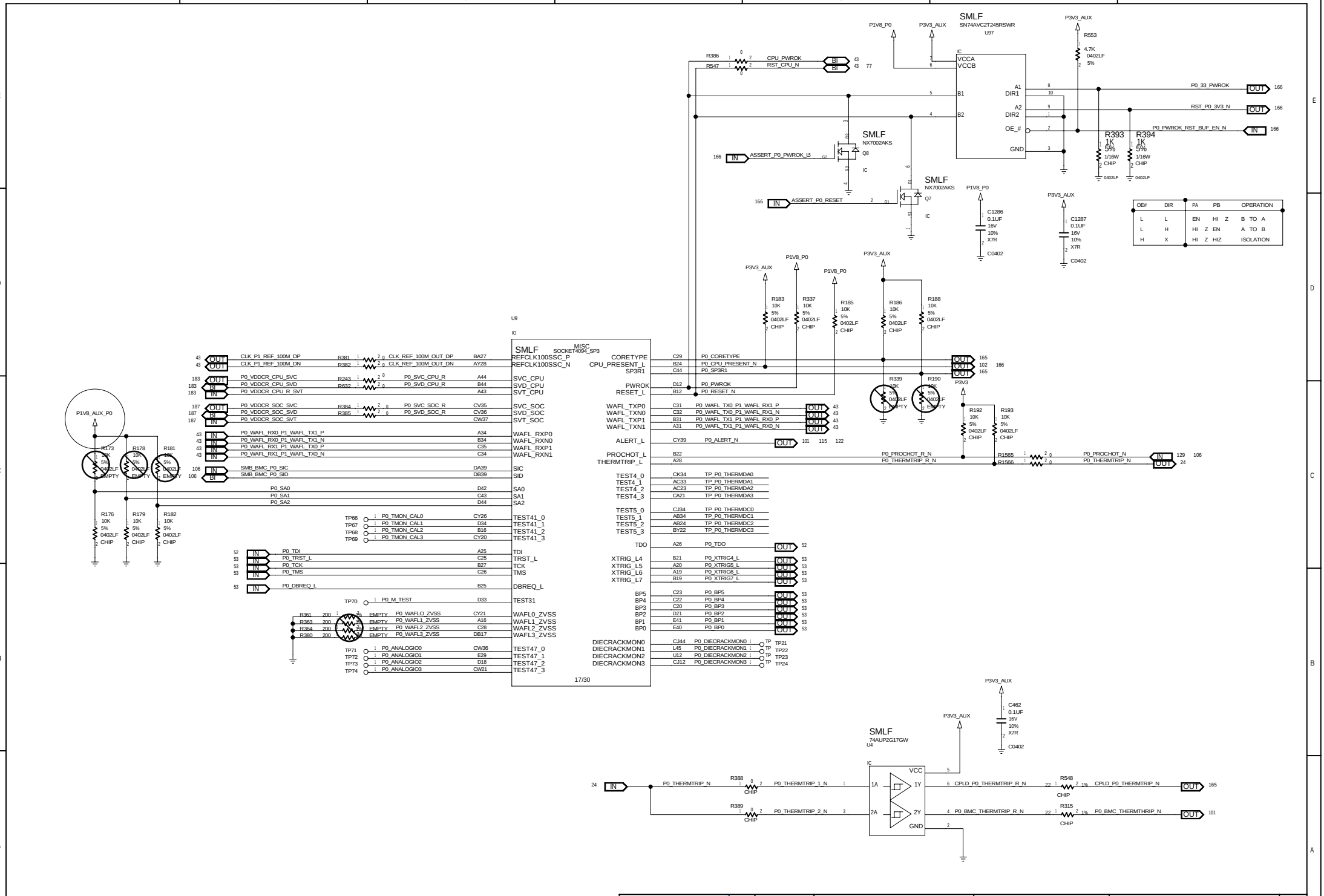

P0 MISC 2 (13 OF 19)

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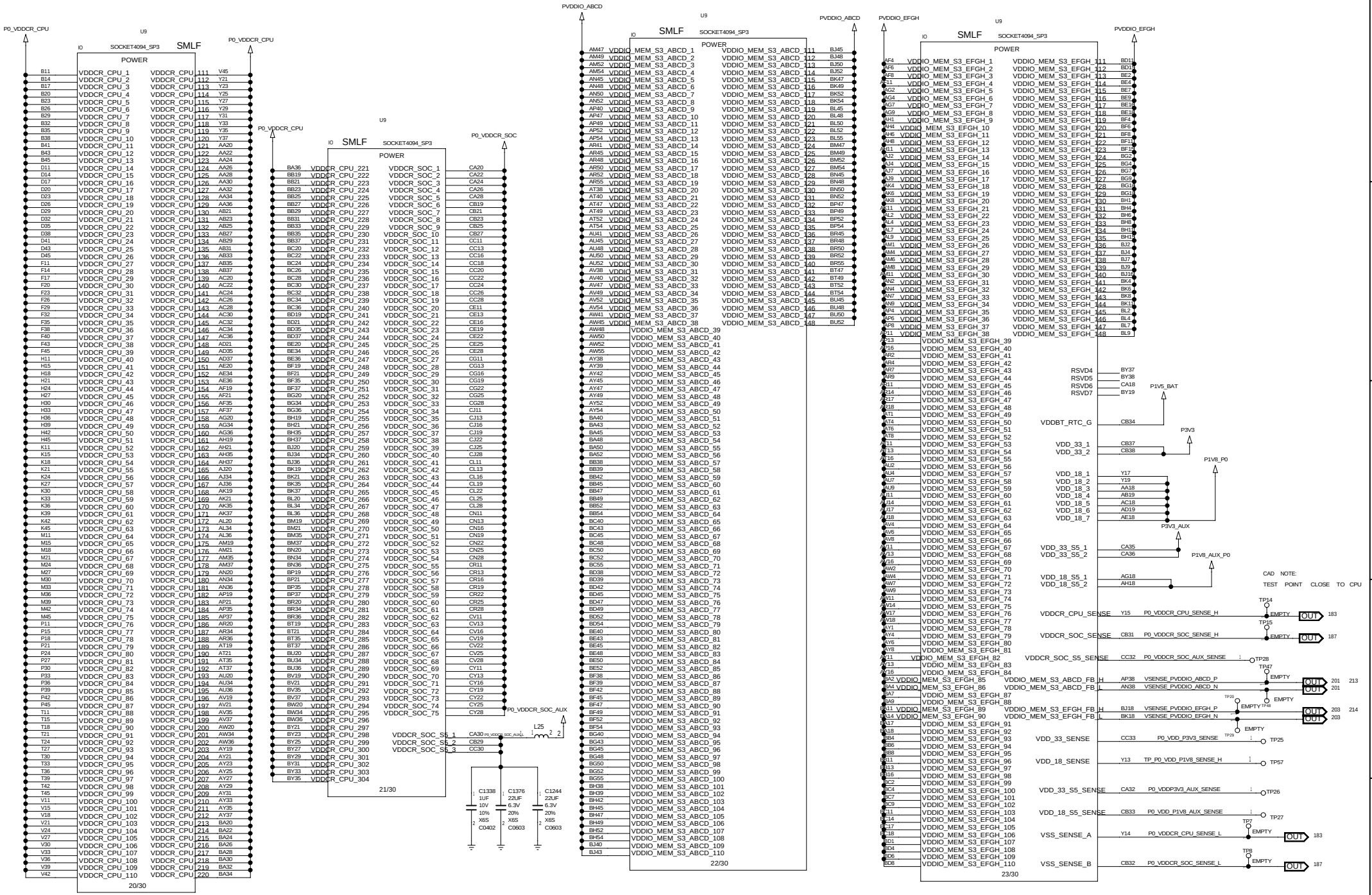

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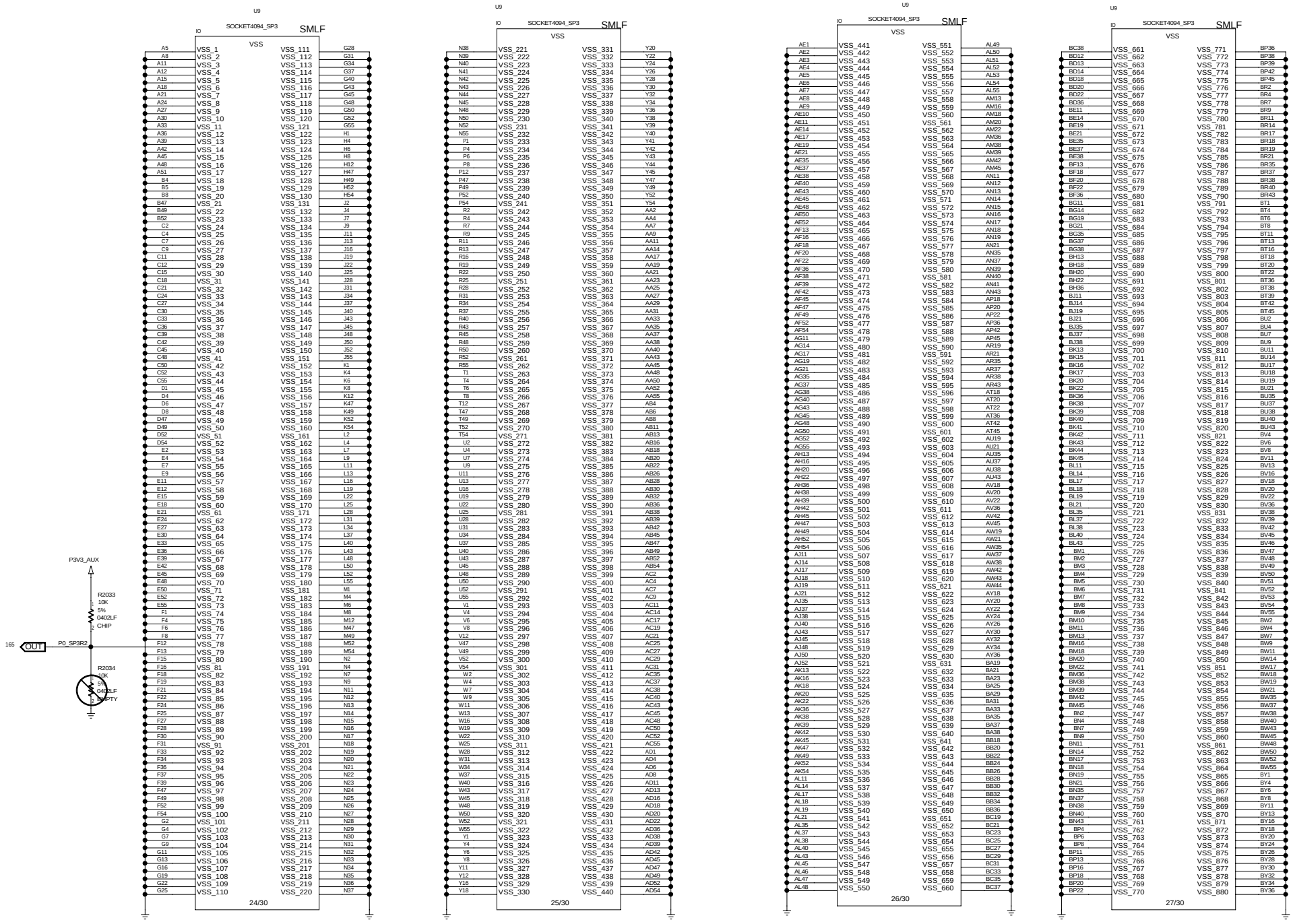
P0 POWER (14 OF 19)



P0 GROUND 1 (15 OF 19)

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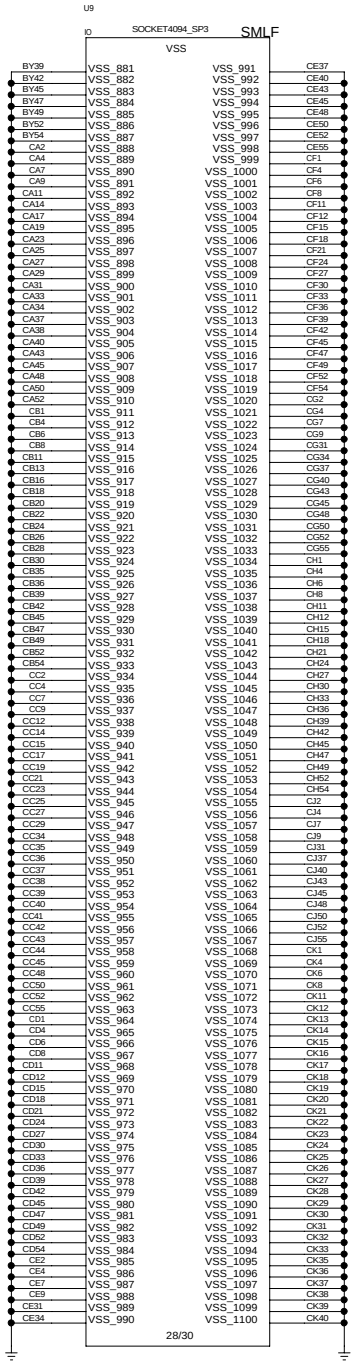

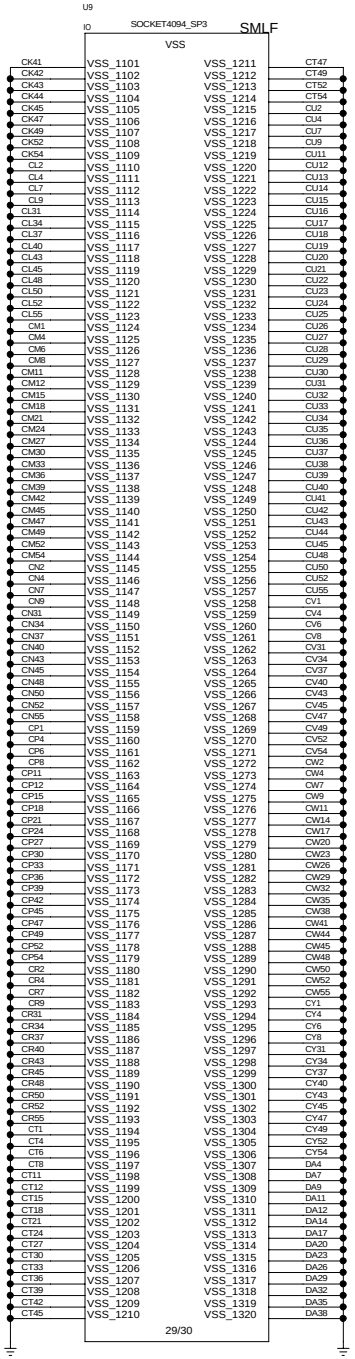

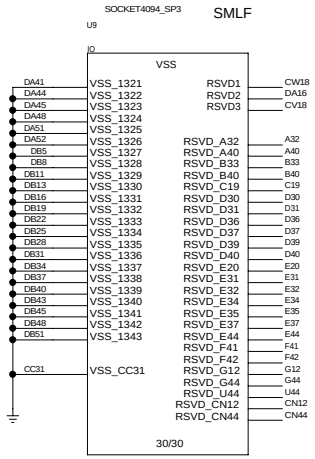

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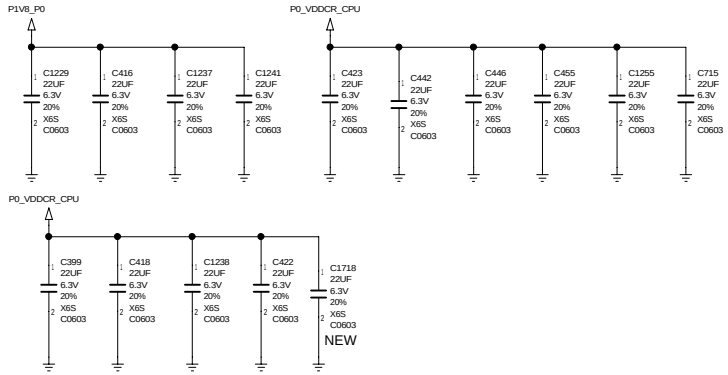
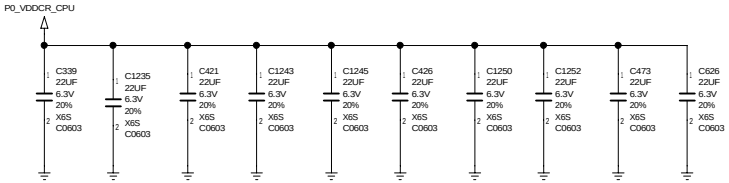
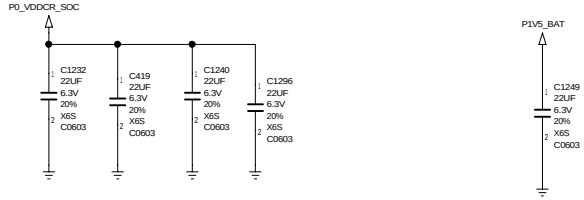
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:30 2017	SHEET 27 OF 226

BOTTOM SIDE- MIRRORED WITH TOP CAVITY- NORTH

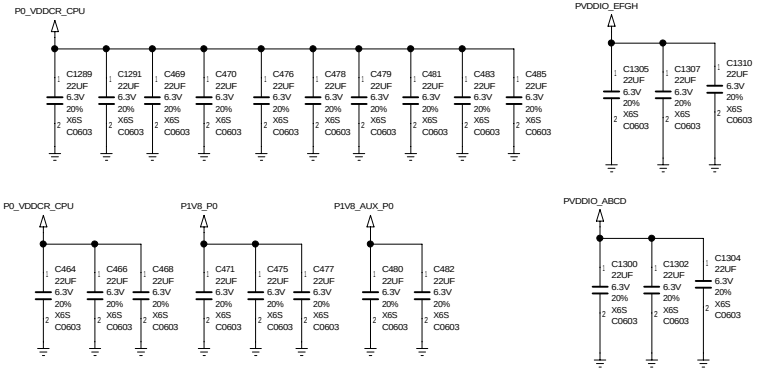


BOTTOM SIDE- MIRRORED WITH TOP CAVITY- SOUTH

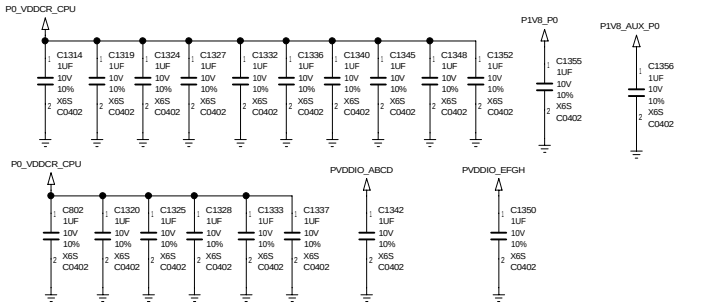




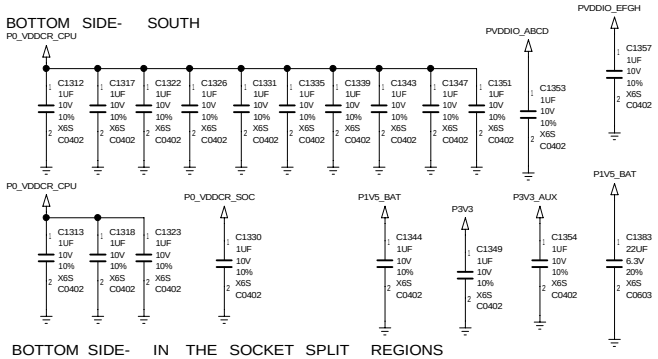
BOTTOM SIDE- NORTH



BOTTOM SIDE- NORTH

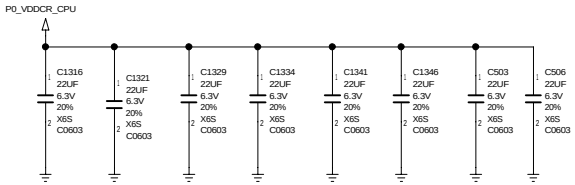


BOTTOM SIDE- SOUTH

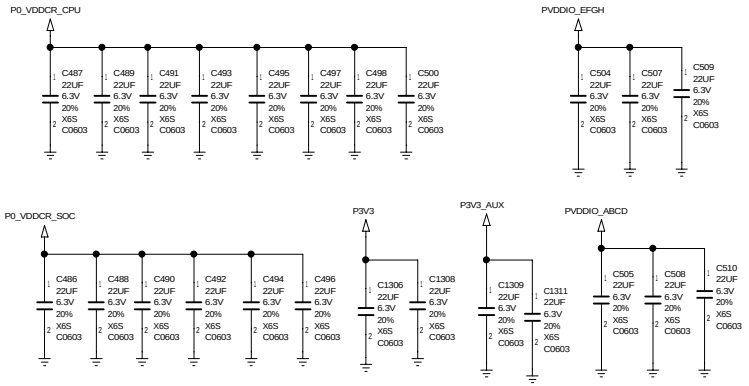


BOTTOM SIDE- IN THE SOCKET SPLIT REGIONS

OEM SKT ONLY: NOT AVAILABLE IN SLT;CAN BE USED FOR RESISTORS

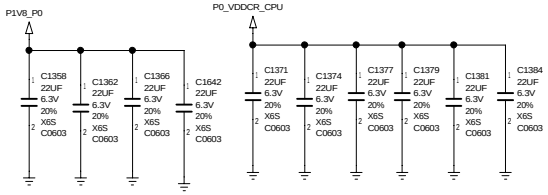


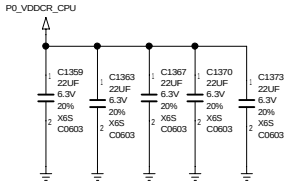
BOTTOM SIDE- SOUTH



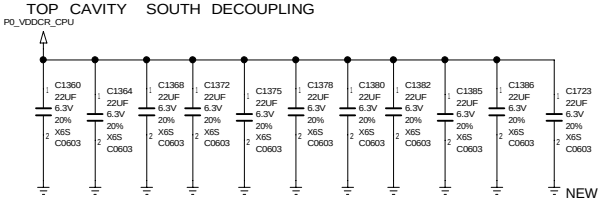
TOP SIDE DECOUPLING

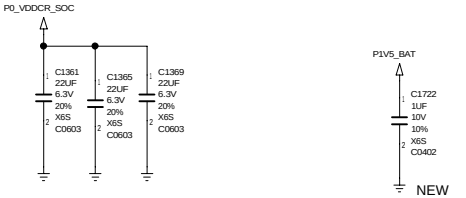
TOP CAVITY-NORTH DECOUPLING





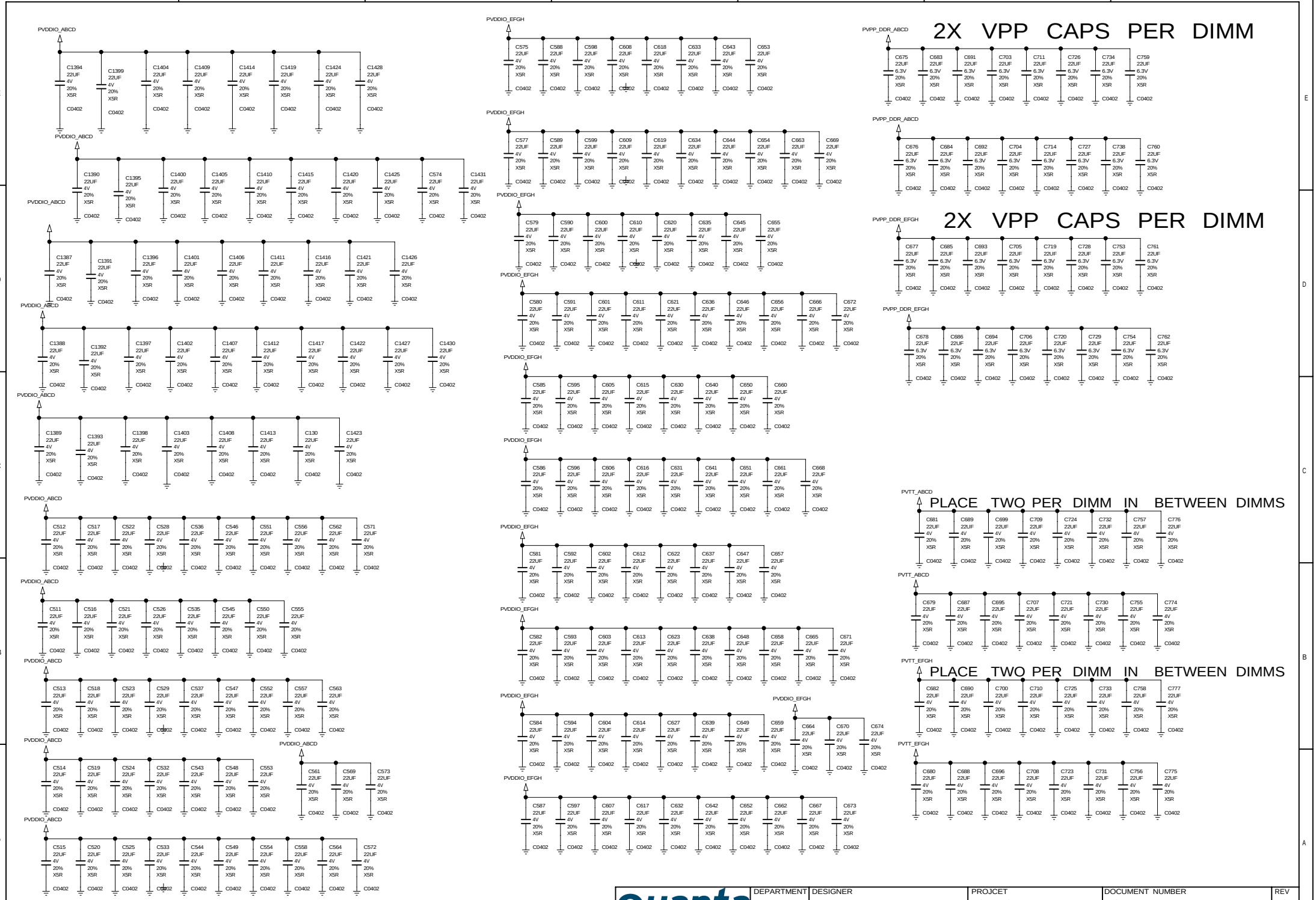
TOP CAVITY SOUTH DECOUPLING





P0 DECOUPLING (17 OF 19)

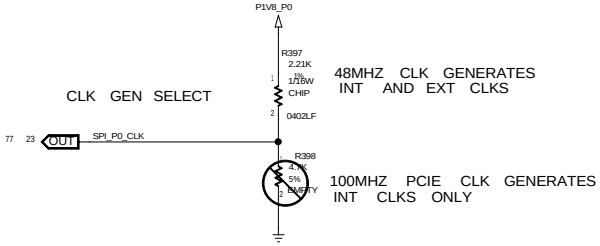
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:31 2017	SHEET 28 OF 226

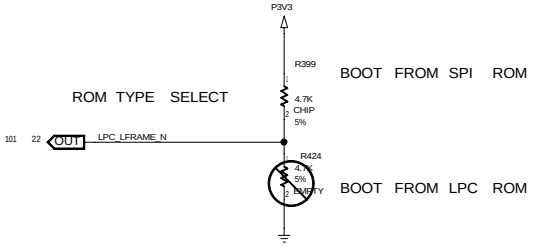


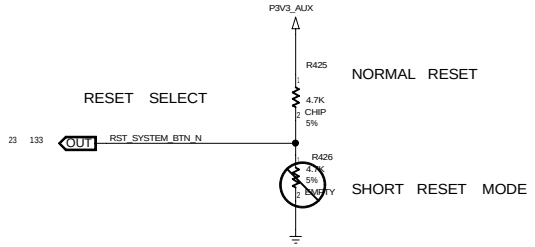
P0 DIMM DECOUPLING (18 OF 19)

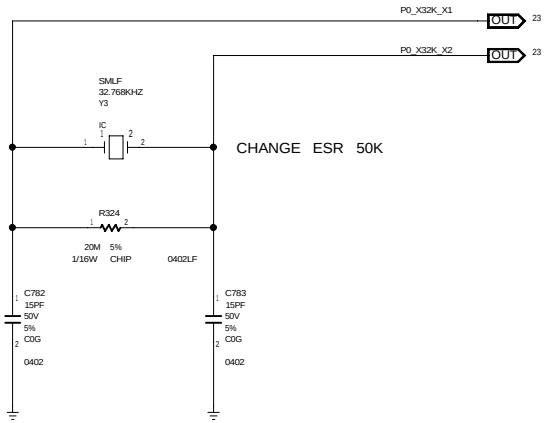
Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:31 2017	SHEET 29 OF 226

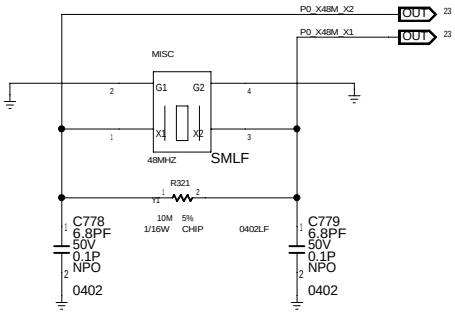
PROCESSOR STRAPS





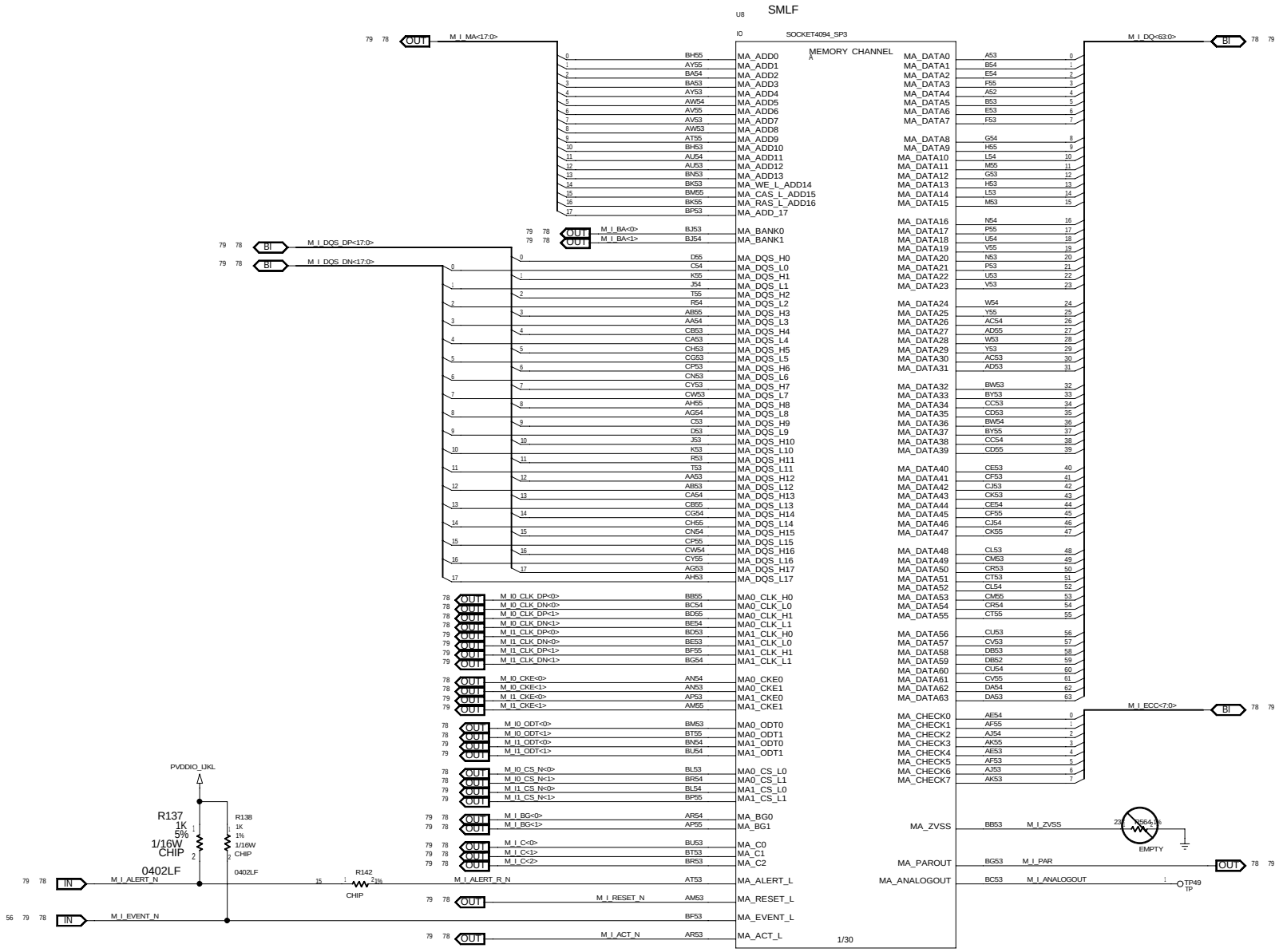






P0 CLOCK & STRAPS(19 OF 19)

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:32 2017	SHEET 30 OF 226



P1 MEMORY CHI (1 OF 19)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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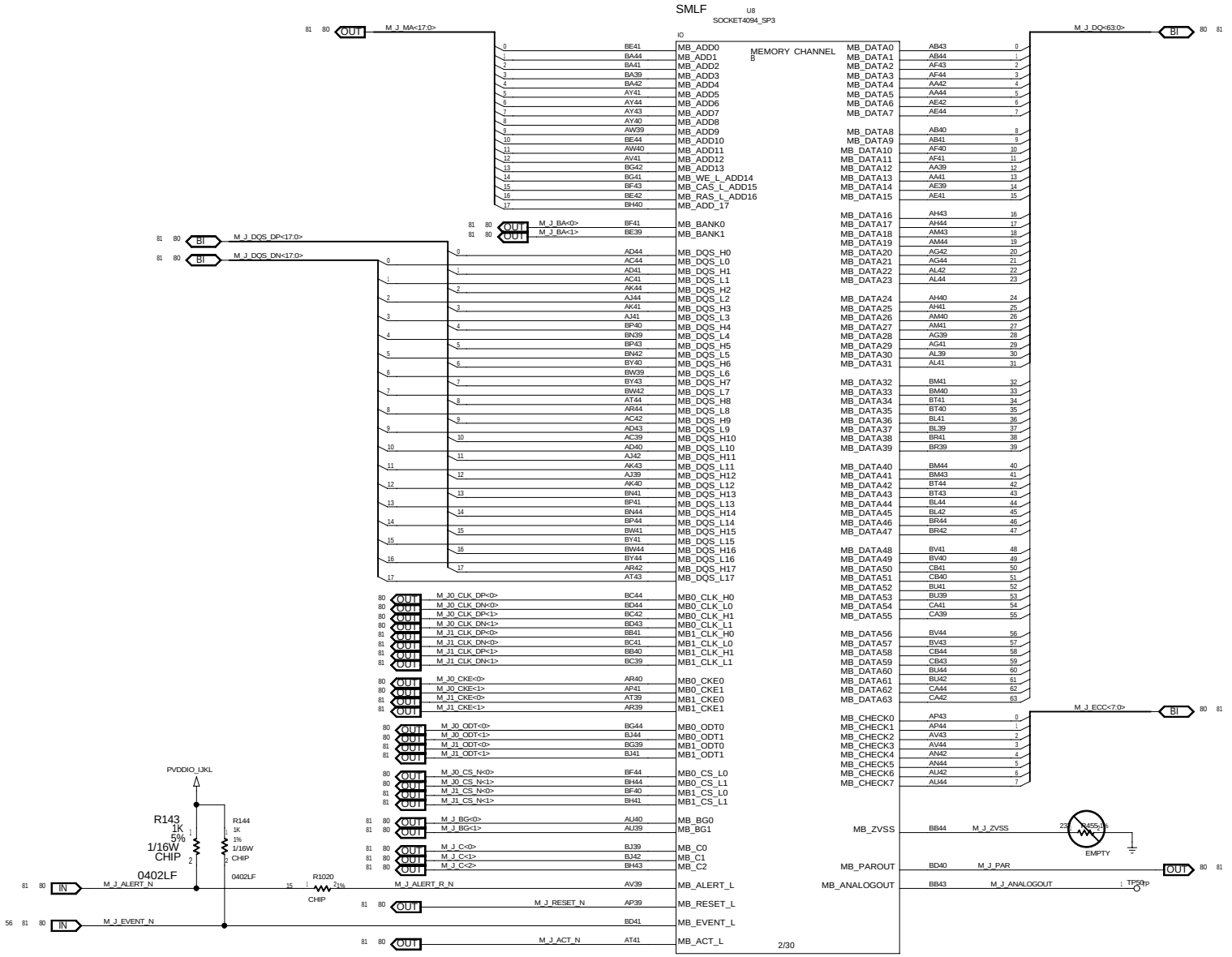
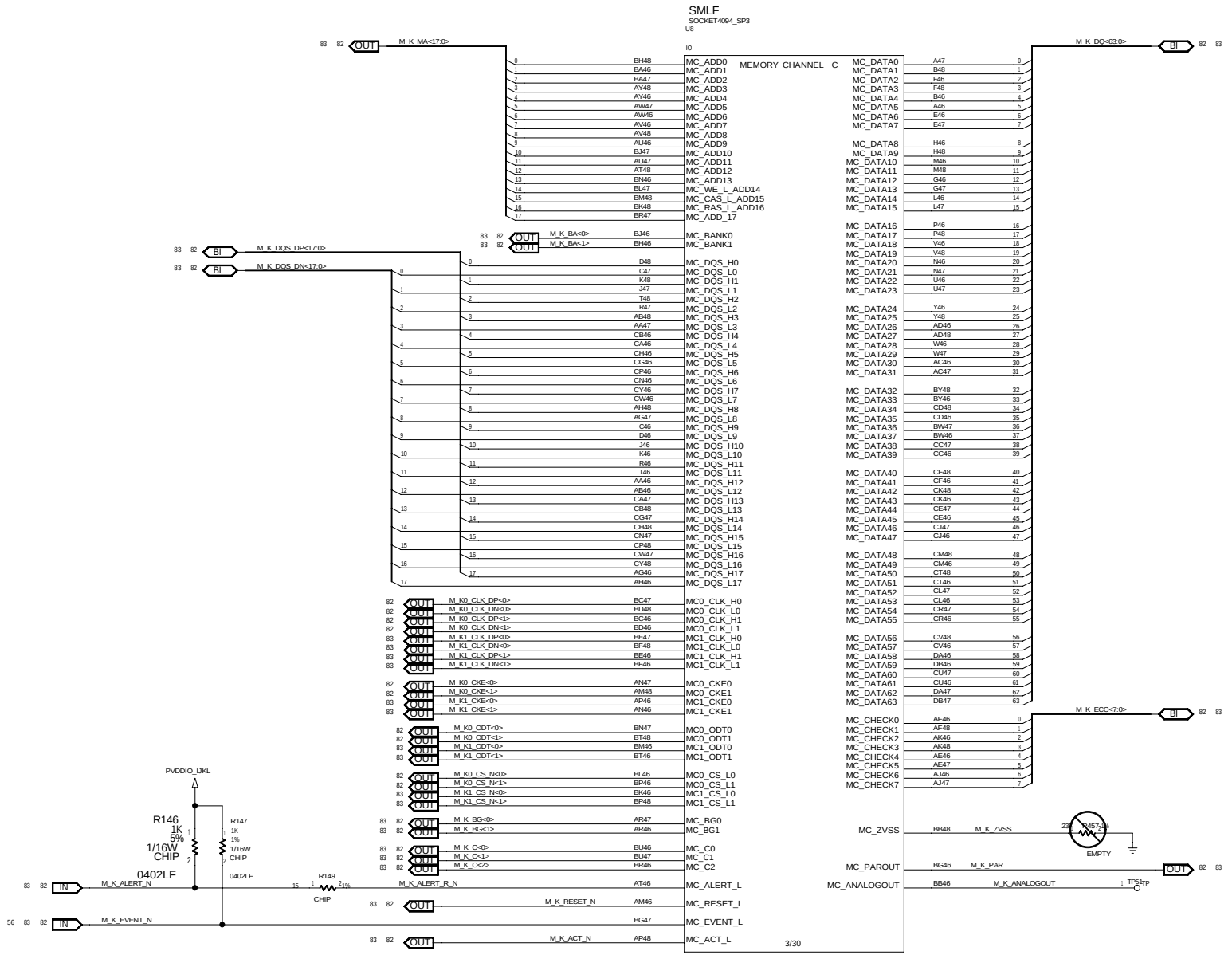


P1 MEMORY CHJ (2 OF 19)

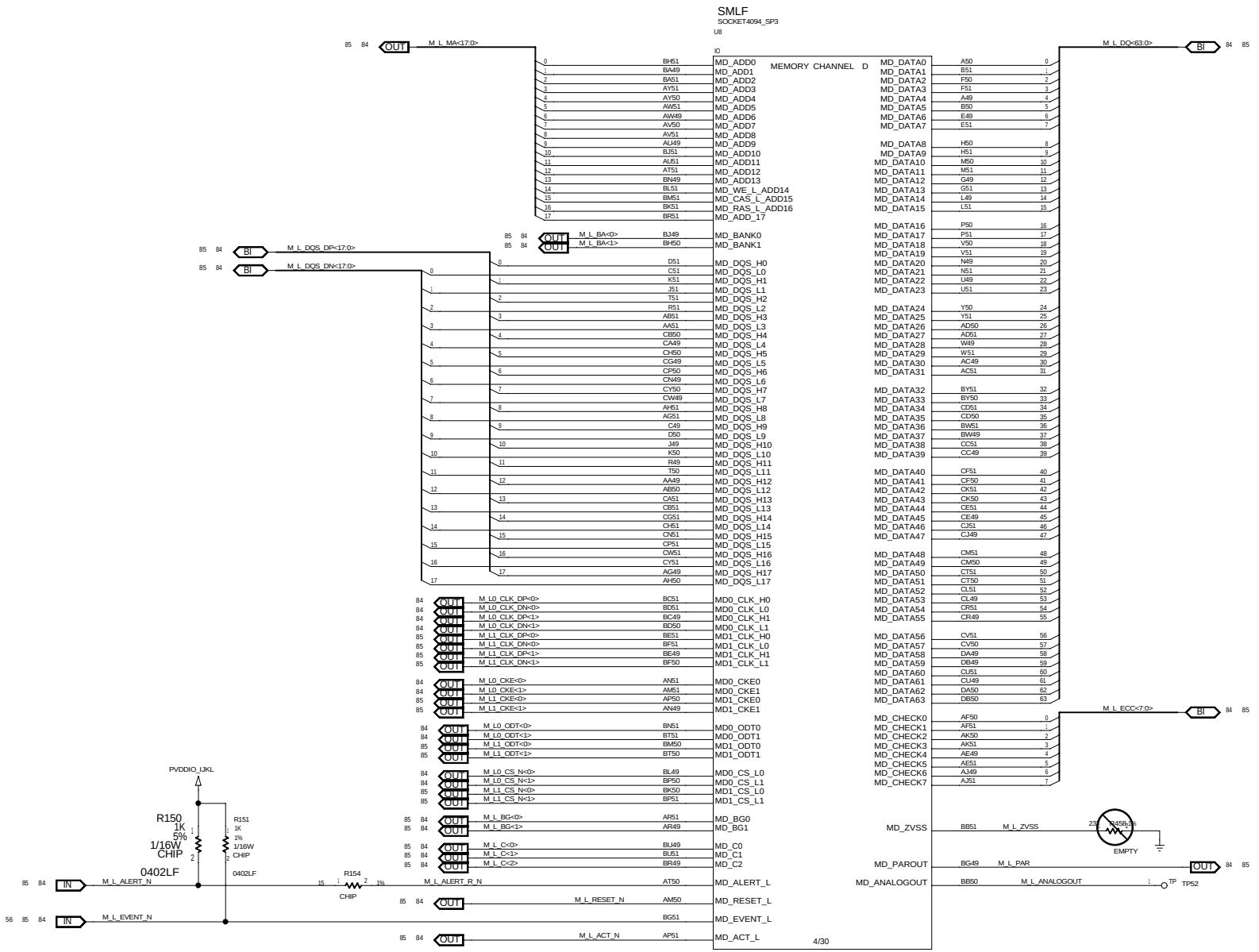
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:32 2017	SHEET 32 OF 226



P1 MEMORY CHK (3 OF 19)

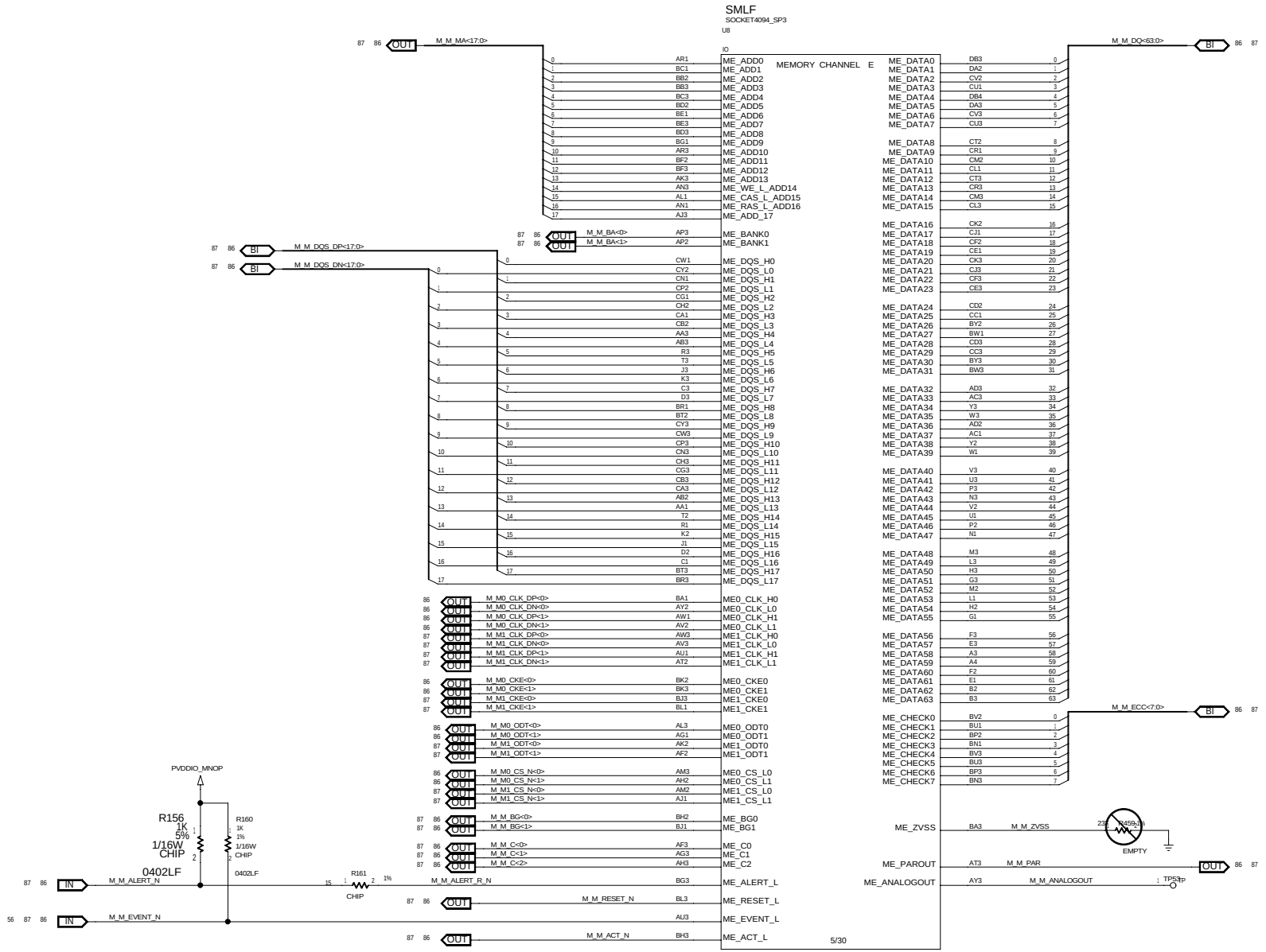
Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:33 2017 SHEET 33 OF 226



P1 MEMORY CHL (4 OF 19)

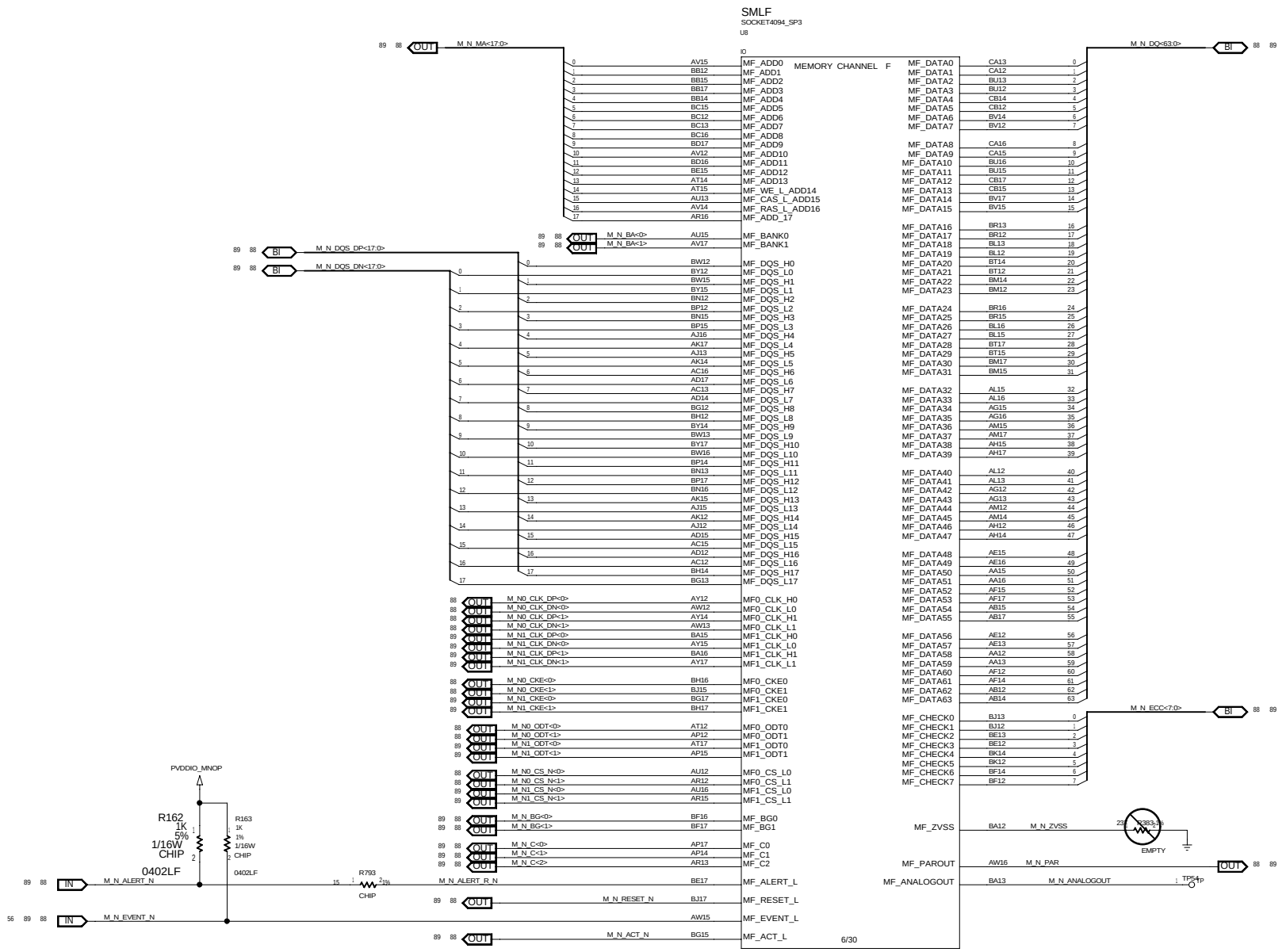
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> / REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:33 2017
			SHEET 34 OF 226	



P1 MEMORY CHM (5 OF 19)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

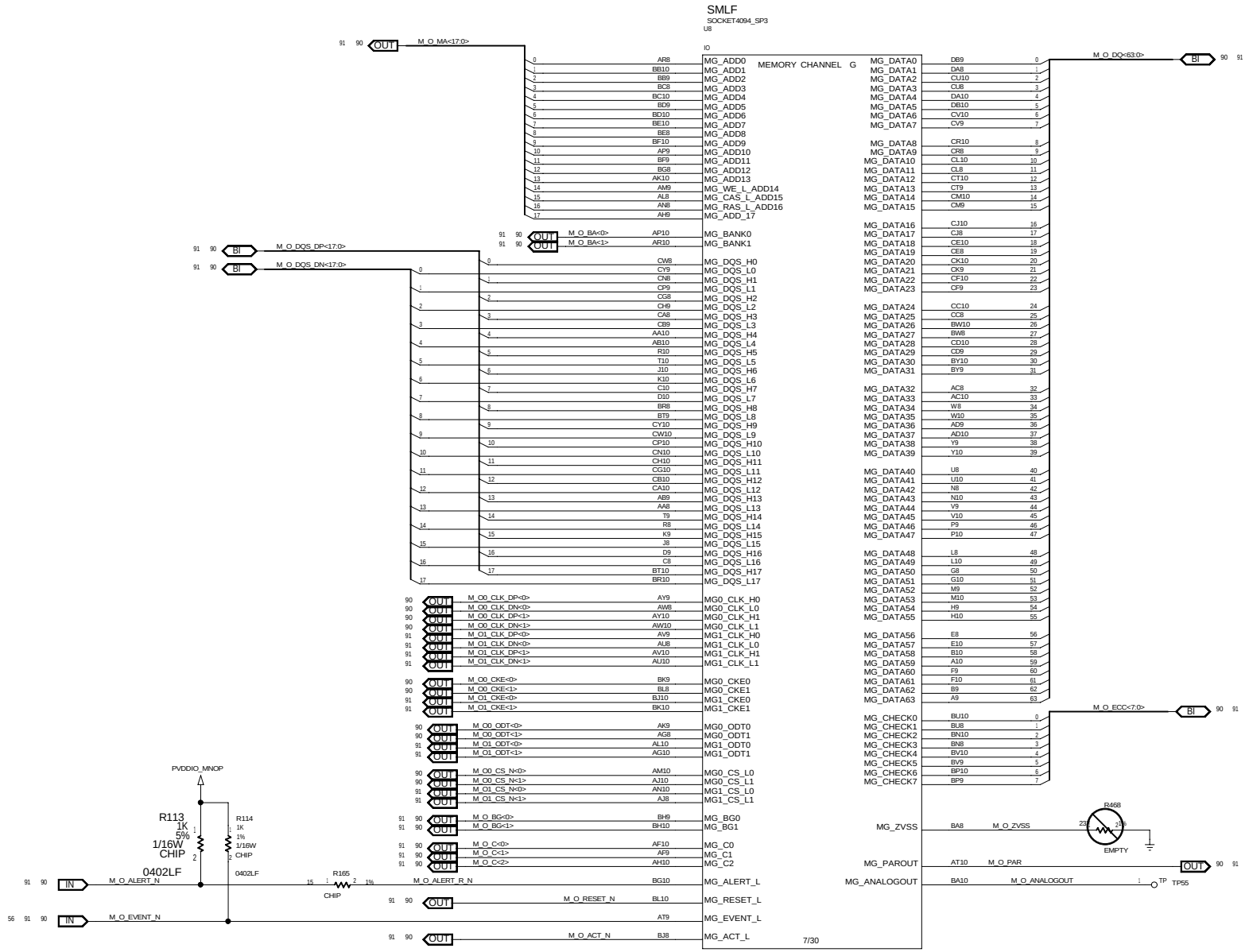
SIZE C DATE Fri Dec 15 20:21:33 2017 SHEET 35 OF 226



P1 MEMORY CHN (6 OF 19)

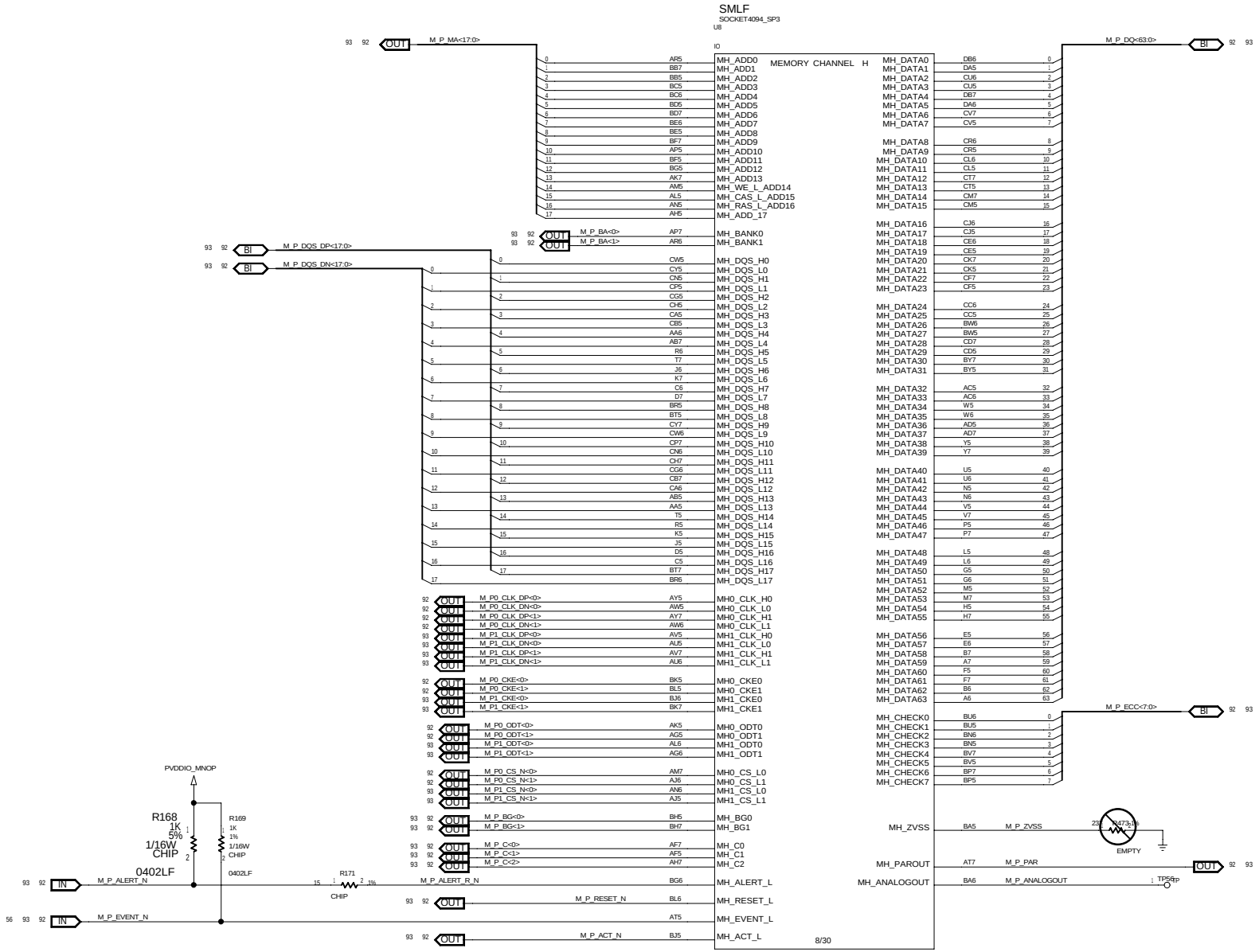
Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:34 2017 SHEET 36 OF 226



DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:34 2017 SHEET 37 OF 226



P1 MEMORY CHP (8 OF 19)

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
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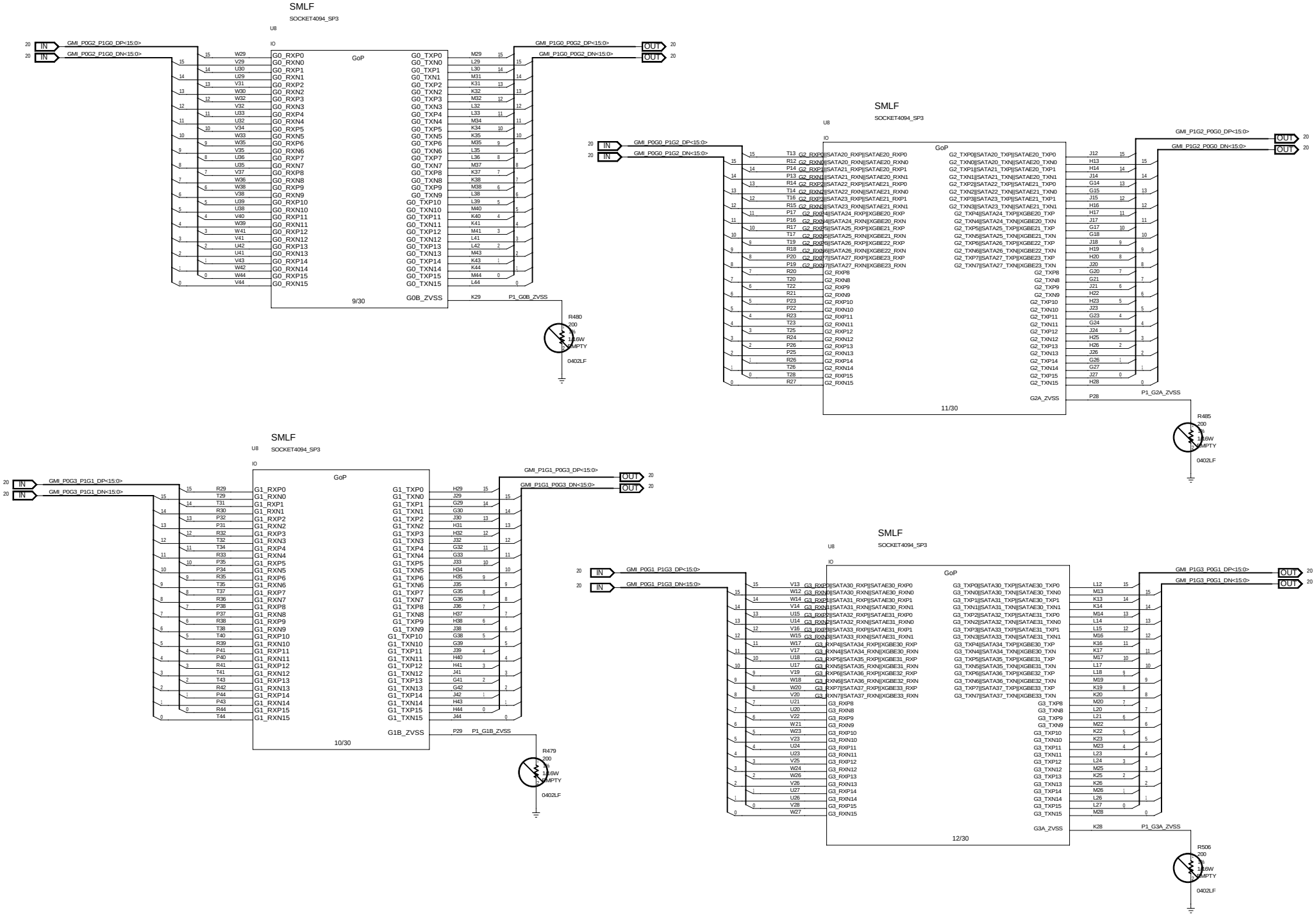
SIZE C DATE Fri Dec 15 20:21:34 2017 SHEET 38 OF 226



P1 xGMI (9 OF 19)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C	DATE Fri Dec 15 20:21:35 2017
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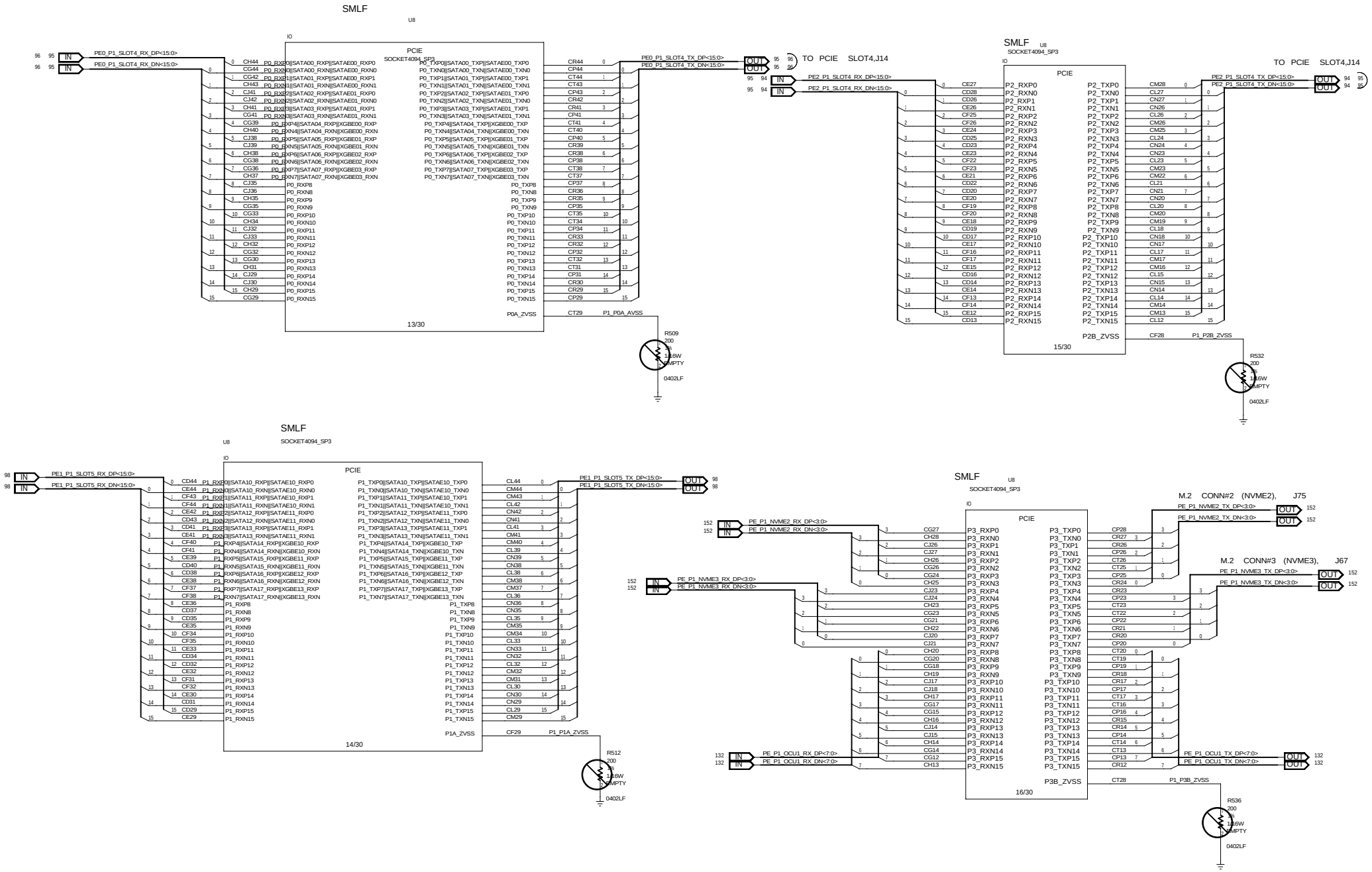
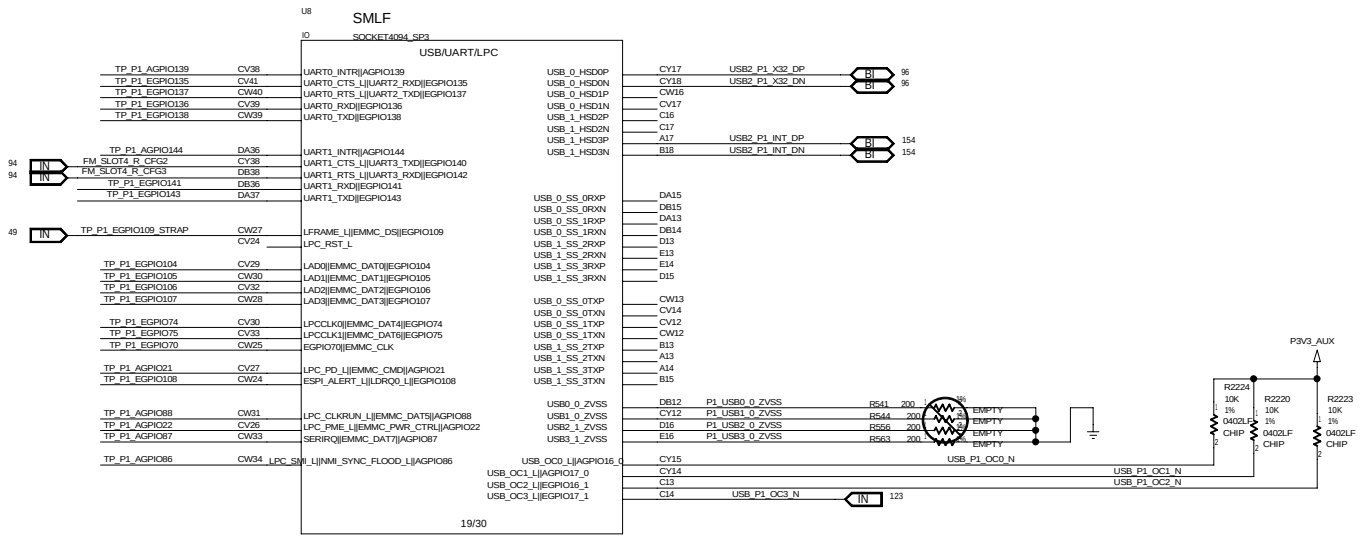


P1 PCIE & SATA (10 OF 19)

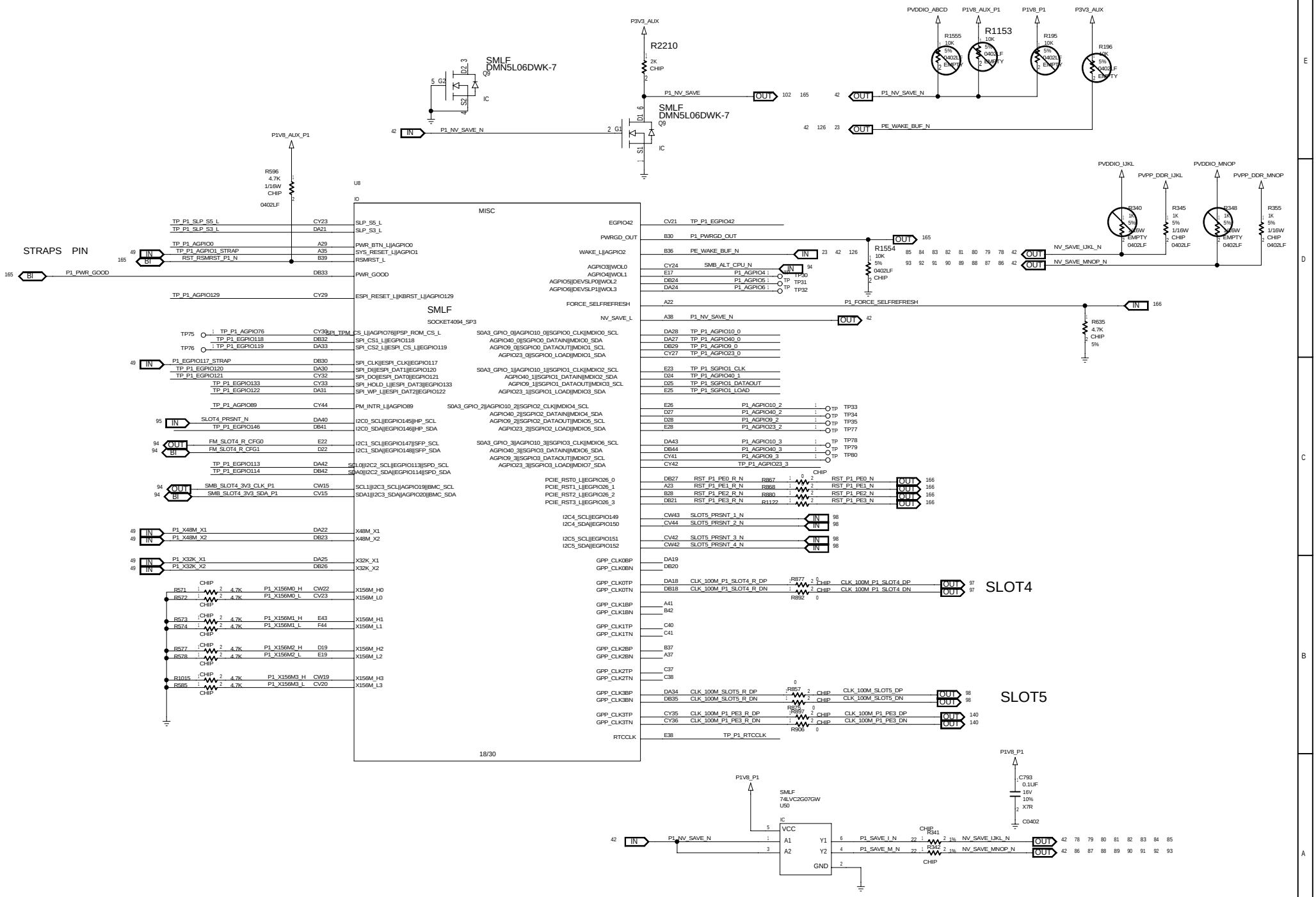
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:35 2017 SHEET 40 OF 226



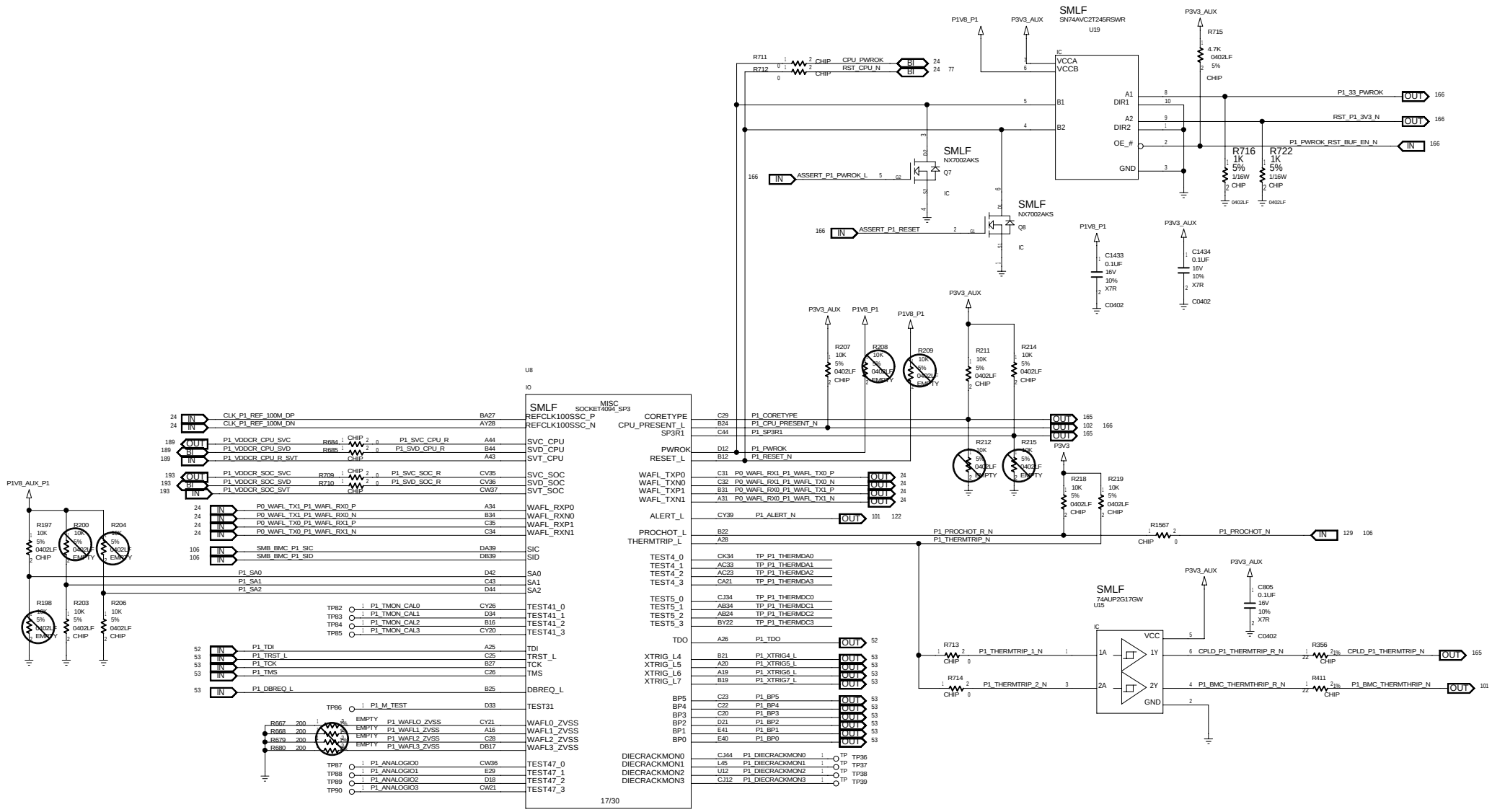
P1 USB, LPC & UART (11 OF 19)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:35 2017	SHEET 41 OF 226	



DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:36 2017 SHEET 42 OF 226



P1 MISC 2 (13 OF 19)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
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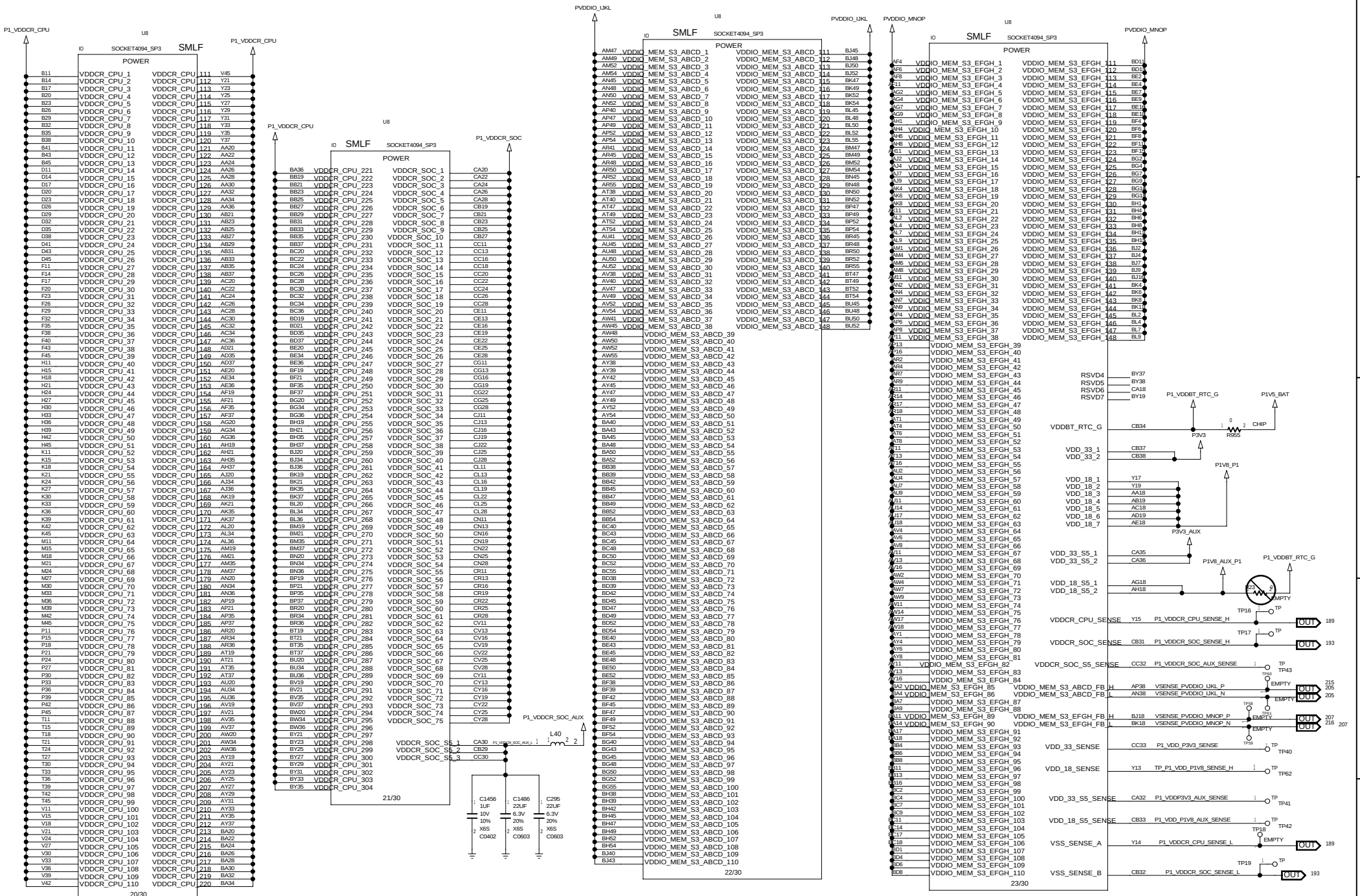
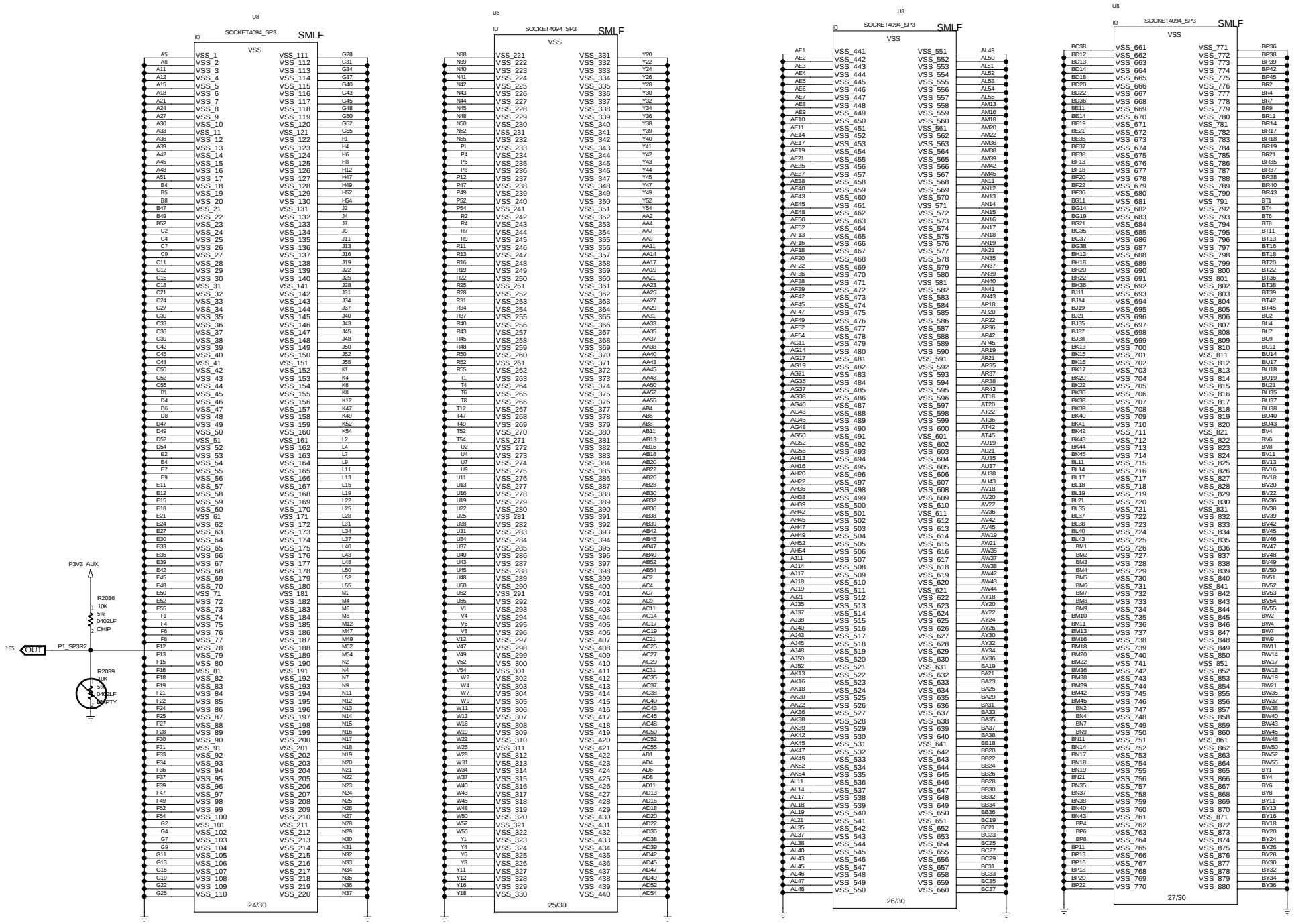
	REVIEWER	SIZE C DATE Fri Dec 15 20:21:36 2017	SHEET 43 OF 226	



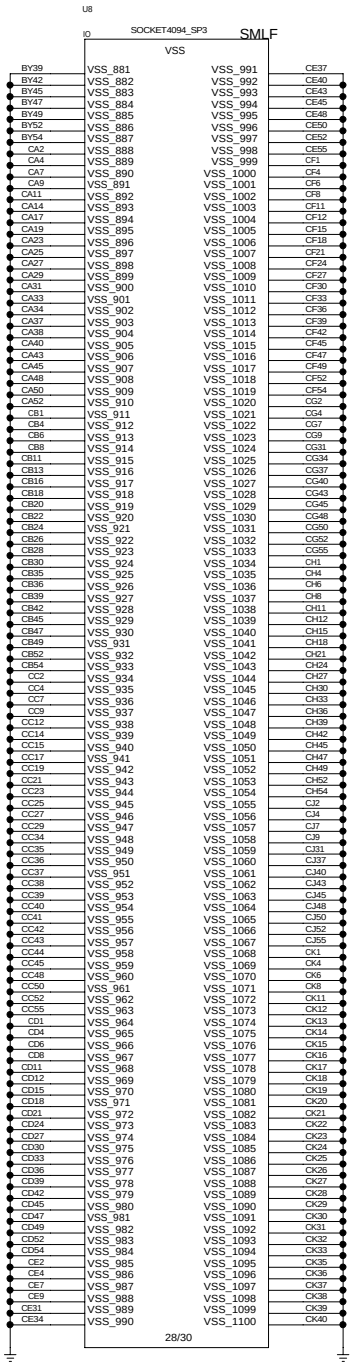
P1 POWER (14 OF 19)

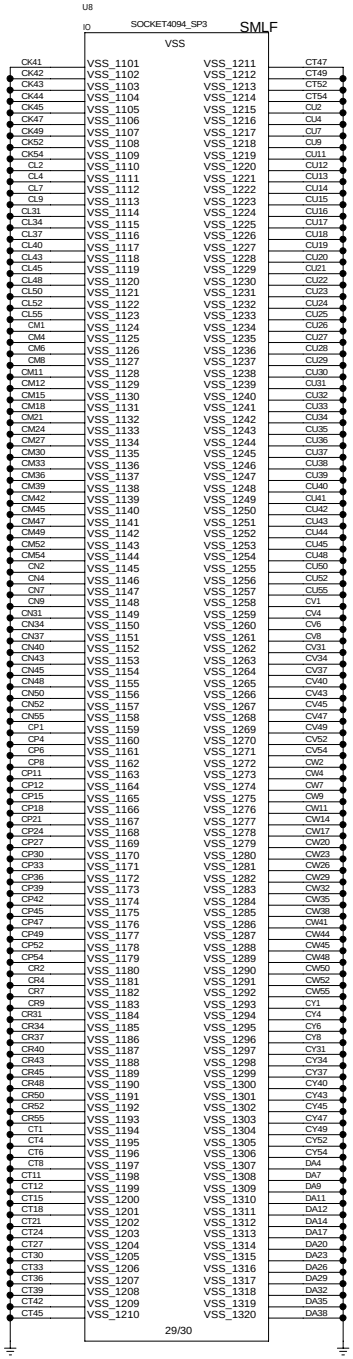
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU		<Q_PROJ>	<Q_NUMBER>	<Q_REV>
	REVIEWER	SIZE C	DATE Fri Dec 15 20:21:36 2017	SHEET 44 OF 226

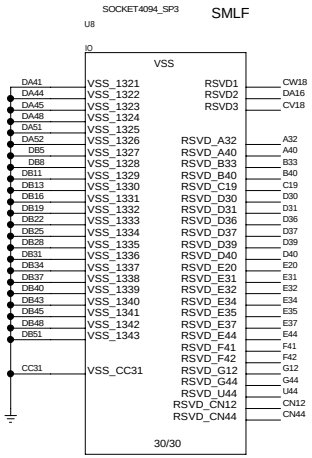


P1 GROUND 1 (15 OF 19)

Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>
		REVIEWER	DOCUMENT NUMBER <Q_NUMBER>
			REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:37 2017 SHEET 45 OF 226







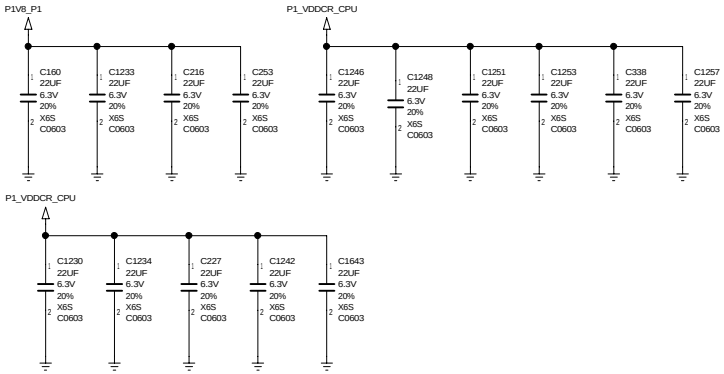
P1 GROUND 2 (16 OF 19)

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

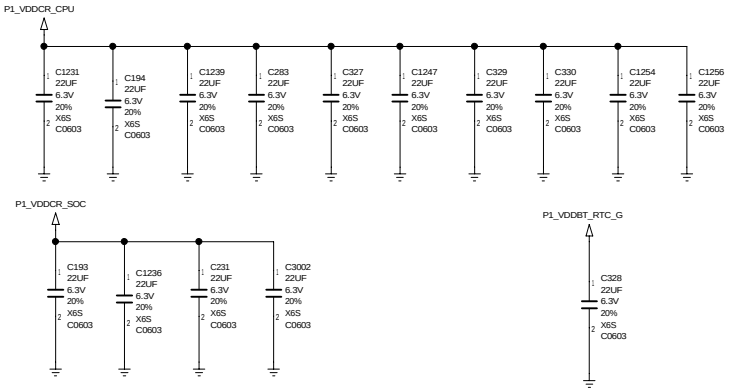
SIZE C DATE Fri Dec 15 20:21:37 2017 SHEET 46 OF 226

VDDCR_CPU BOTTOM SIDE DECOUPLING

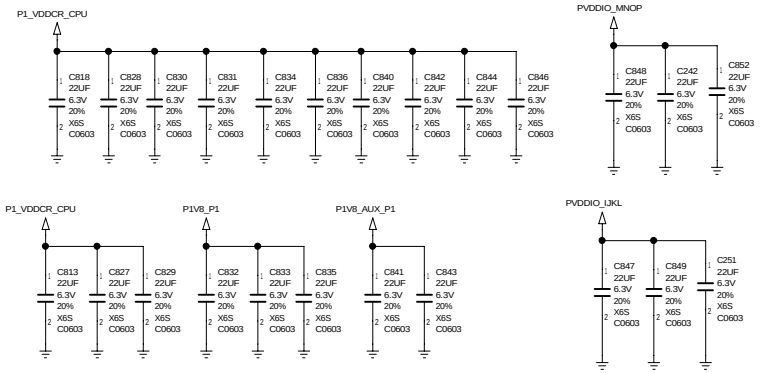
BOTTOM SIDE- MIRRORED WITH TOP CAVITY- NORTH



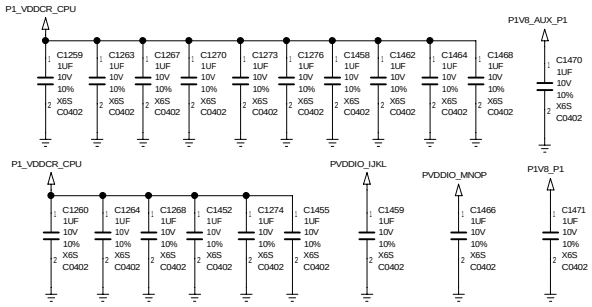
BOTTOM SIDE- MIRRORED WITH TOP CAVITY- SOUTH



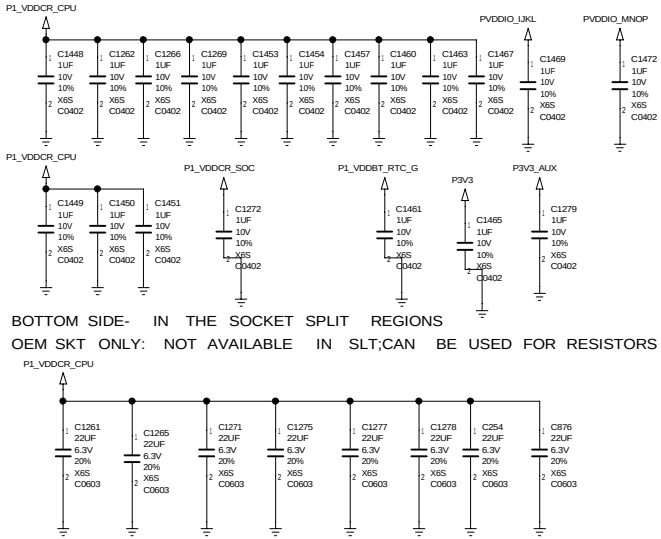
BOTTOM SIDE- NORTH



BOTTOM SIDE- NORTH



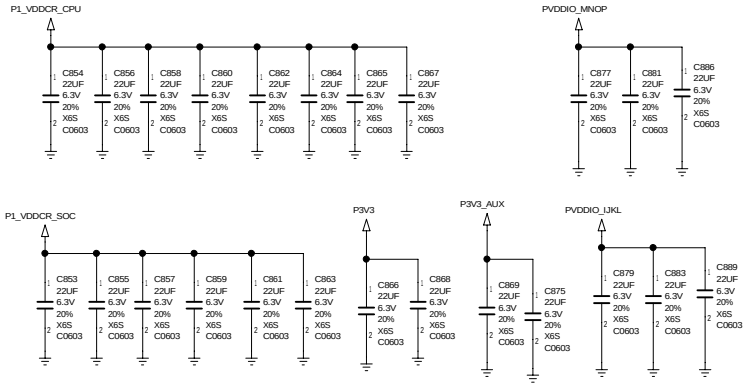
BOTTOM SIDE- SOUTH



BOTTOM SIDE- IN THE SOCKET SPLIT REGIONS

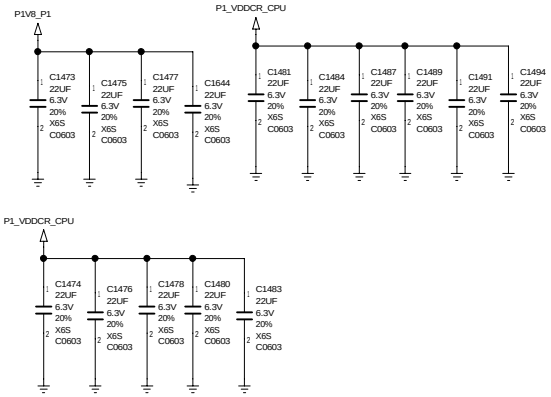
OEM SKT ONLY: NOT AVAILABLE IN SLT;CAN BE USED FOR RESISTORS

BOTTOM SIDE- SOUTH

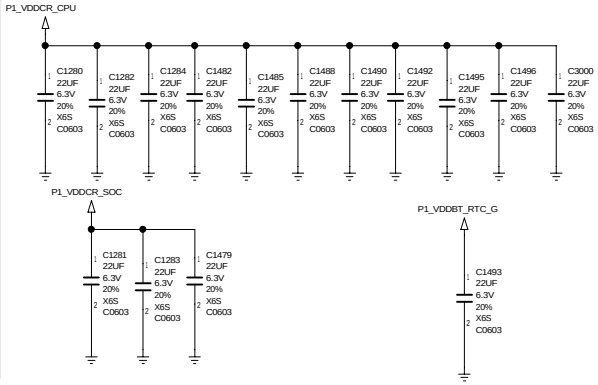


TOP SIDE DECOUPLING

TOP CAVITY-NORTH DECOUPLING

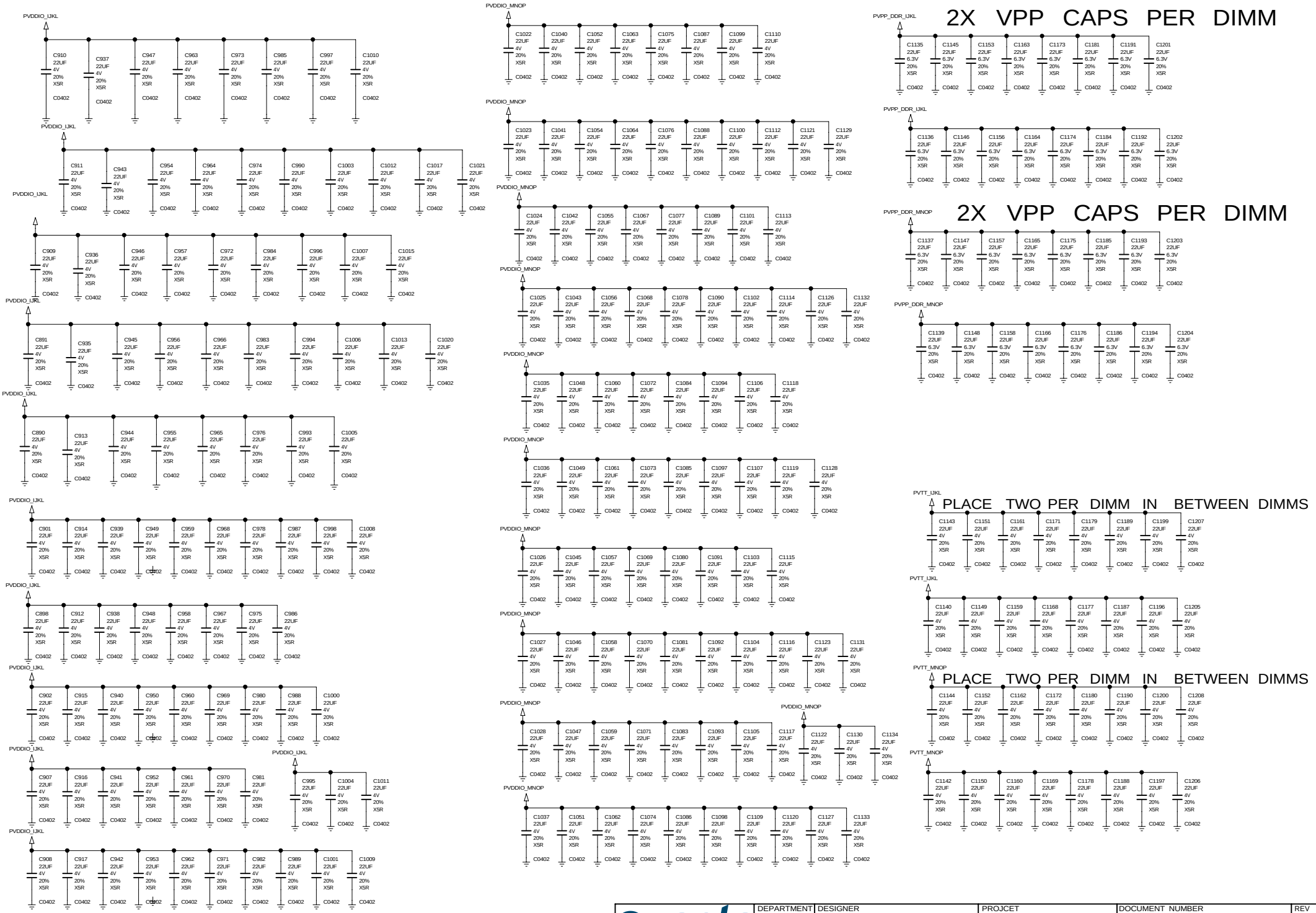


TOP CAVITY SOUTH DECOUPLING



P1 DECOUPLING (17 OF 19)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:38 2017	SHEET 47 OF 226

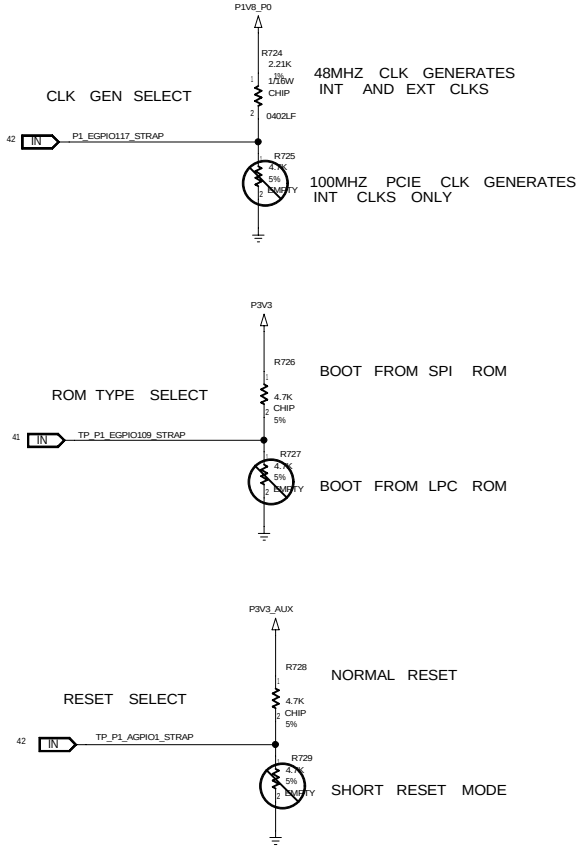


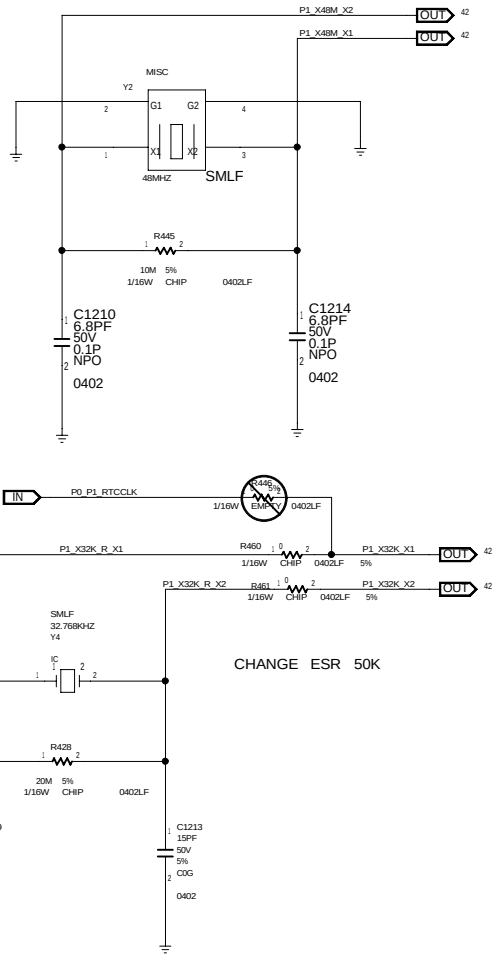
P1 DIMM DECOUPLING (12 OF 19)

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:38 2017 SHEET 48 OF 226

PROCESSOR STRAPS





P1 CLOCKS & STRAPS (12 OF 19)

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
			SIZE C DATE Fri Dec 15 20:21:39 2017	SHEET 49 OF 226	

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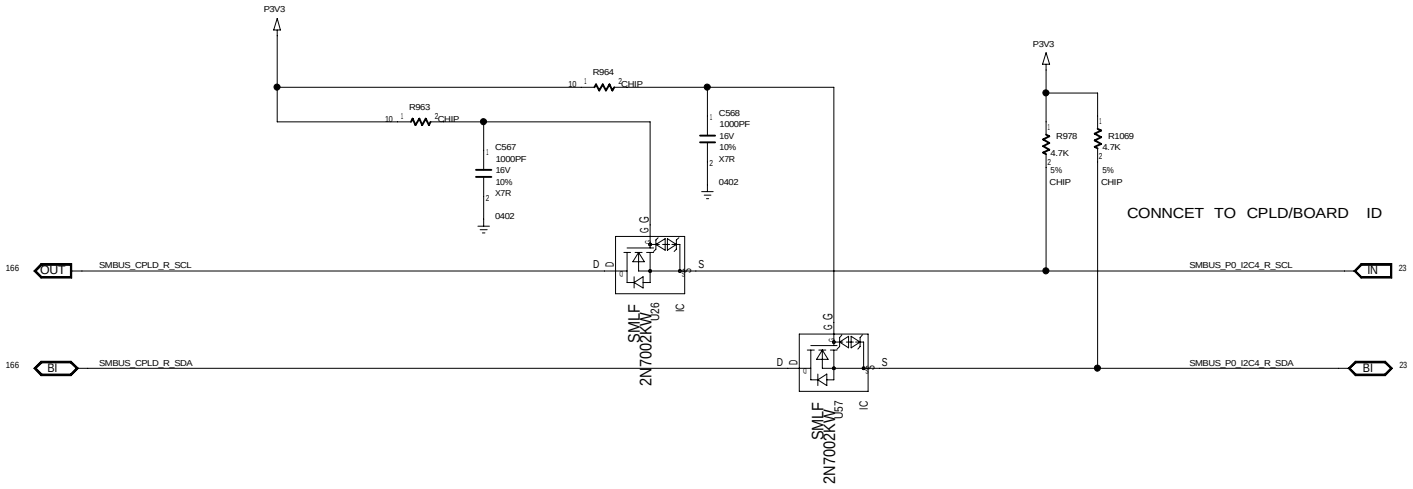
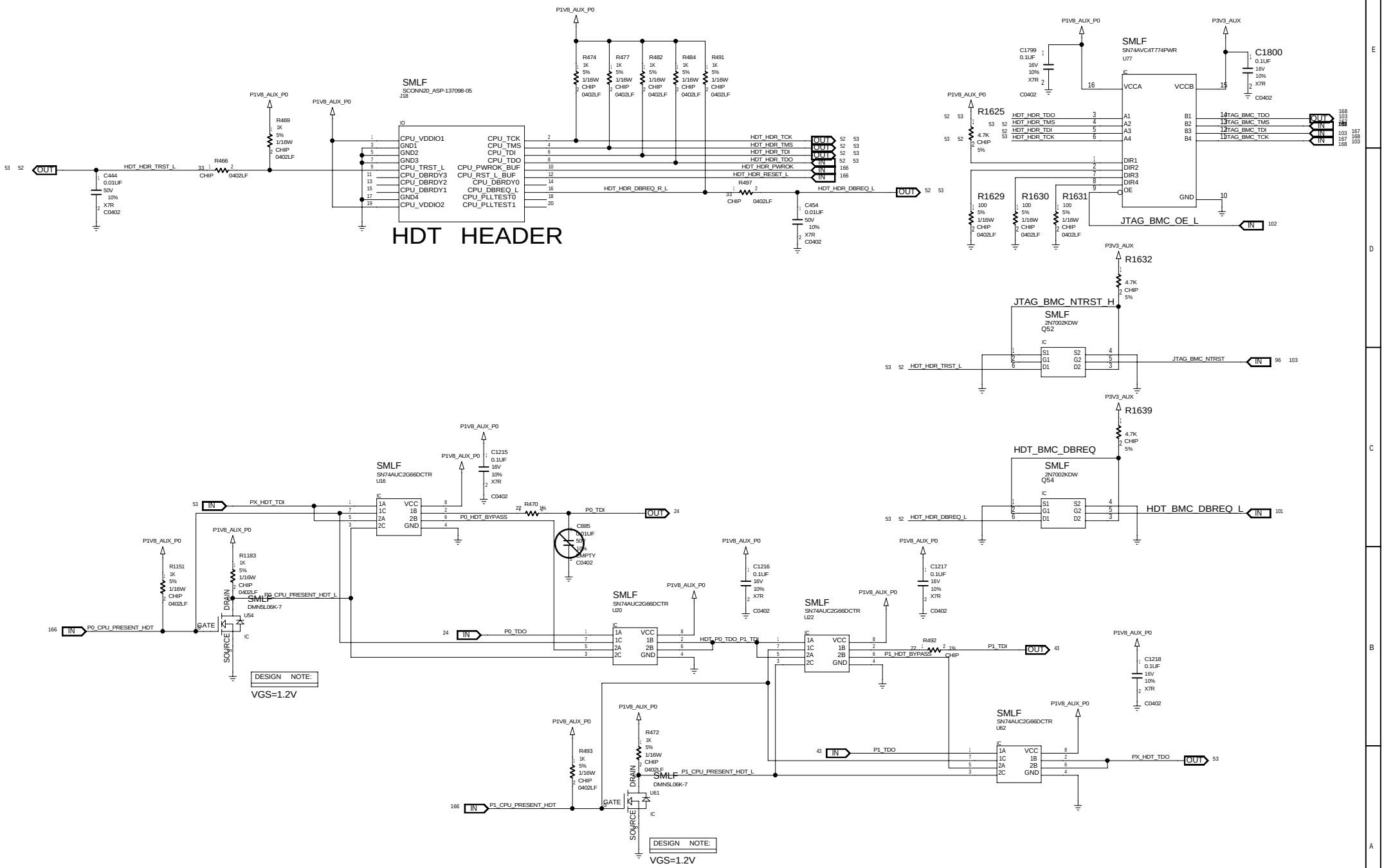
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:31:19 2017	SHEET 50 OF 226



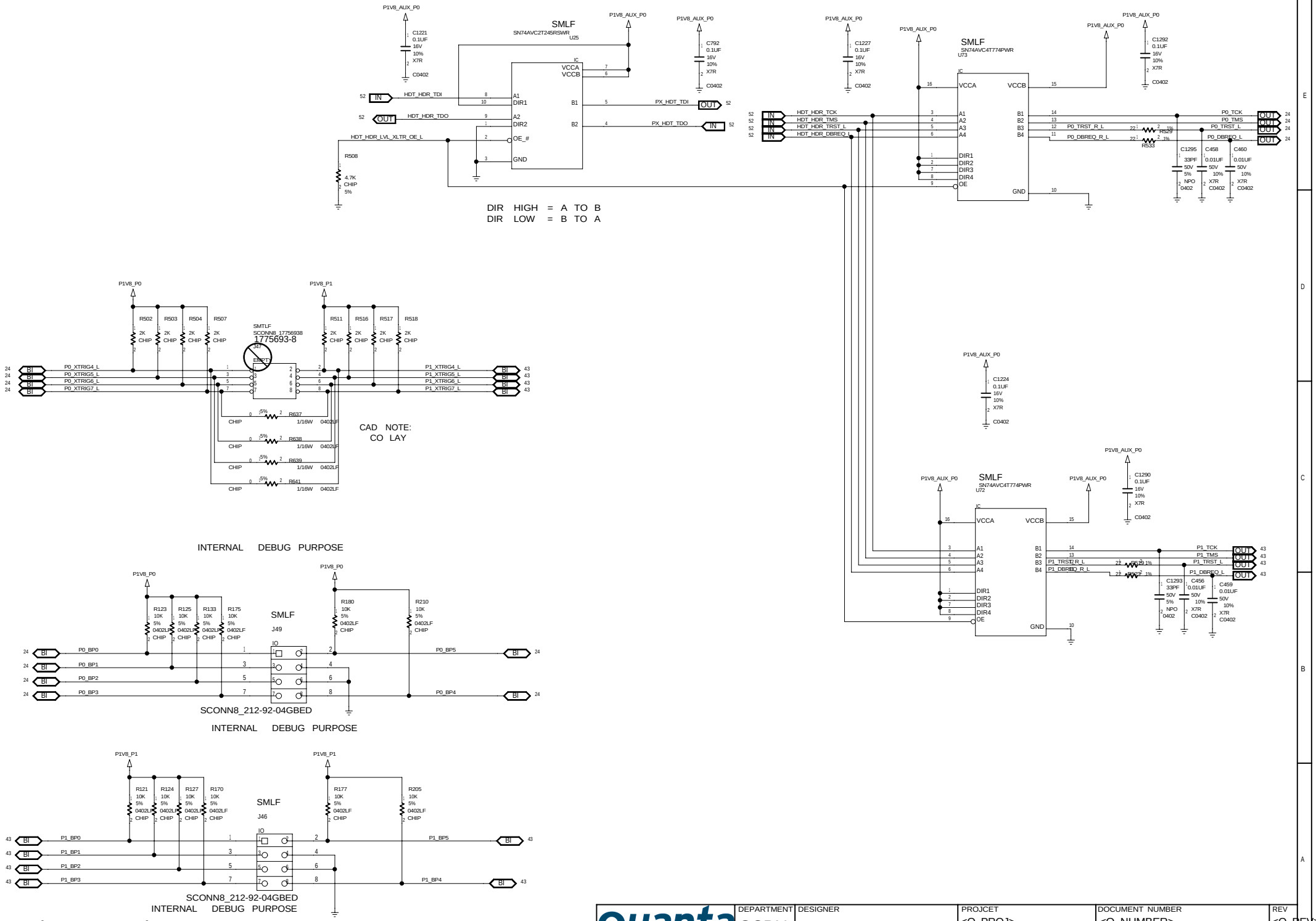
SMBUS ISOLATE for CPU0

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:20 2017	SHEET 51 OF 226



HDT (1 OF 2)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:15 2017	SHEET 52 OF 226



HDT (2 OF 2)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU		<Q_PROJ>	<Q_NUMBER>	<Q_REV>
	REVIEWER			

SIZE C DATE Fri Dec 15 20:21:39 2017 SHEET 53 OF 226

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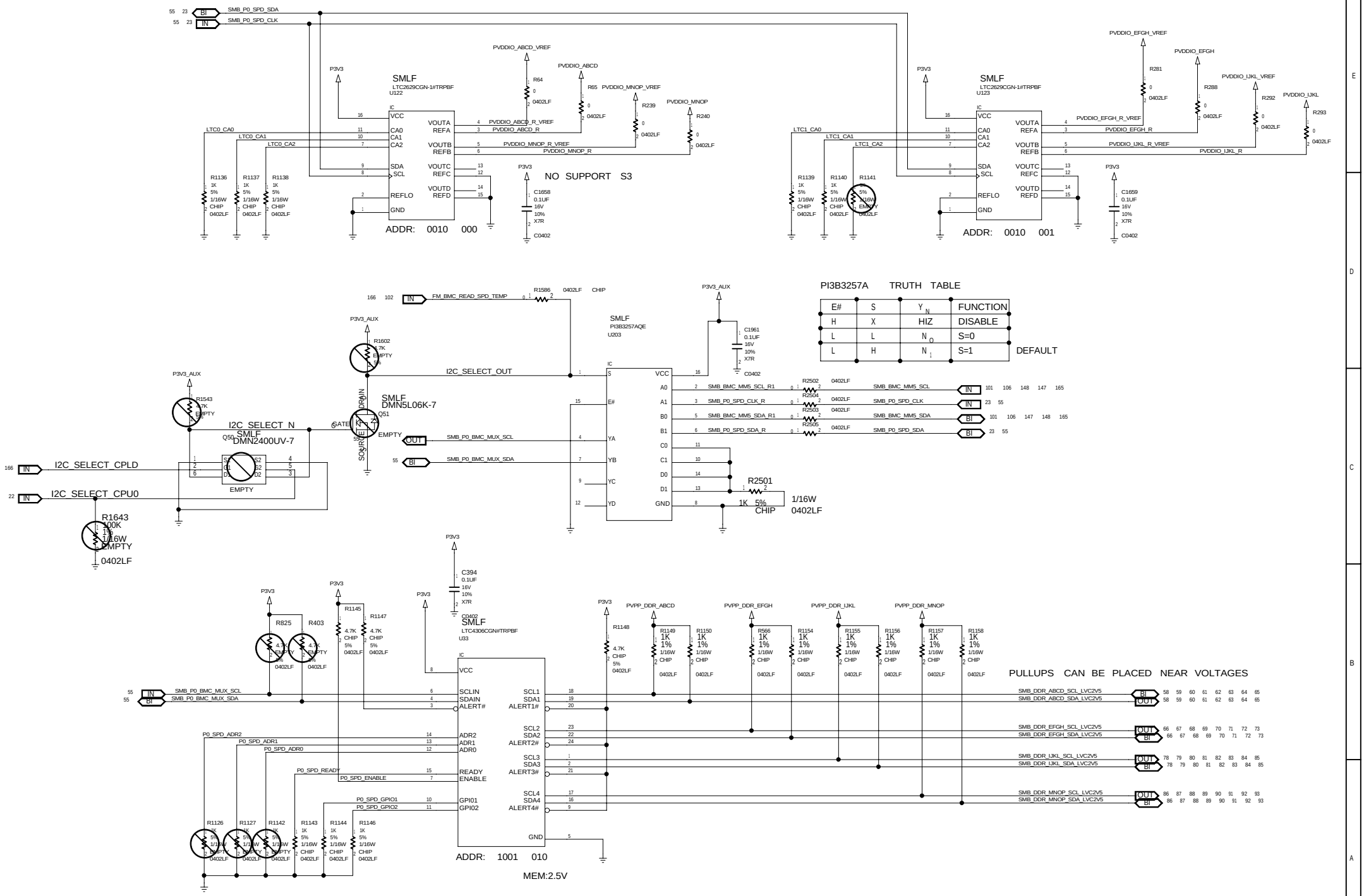
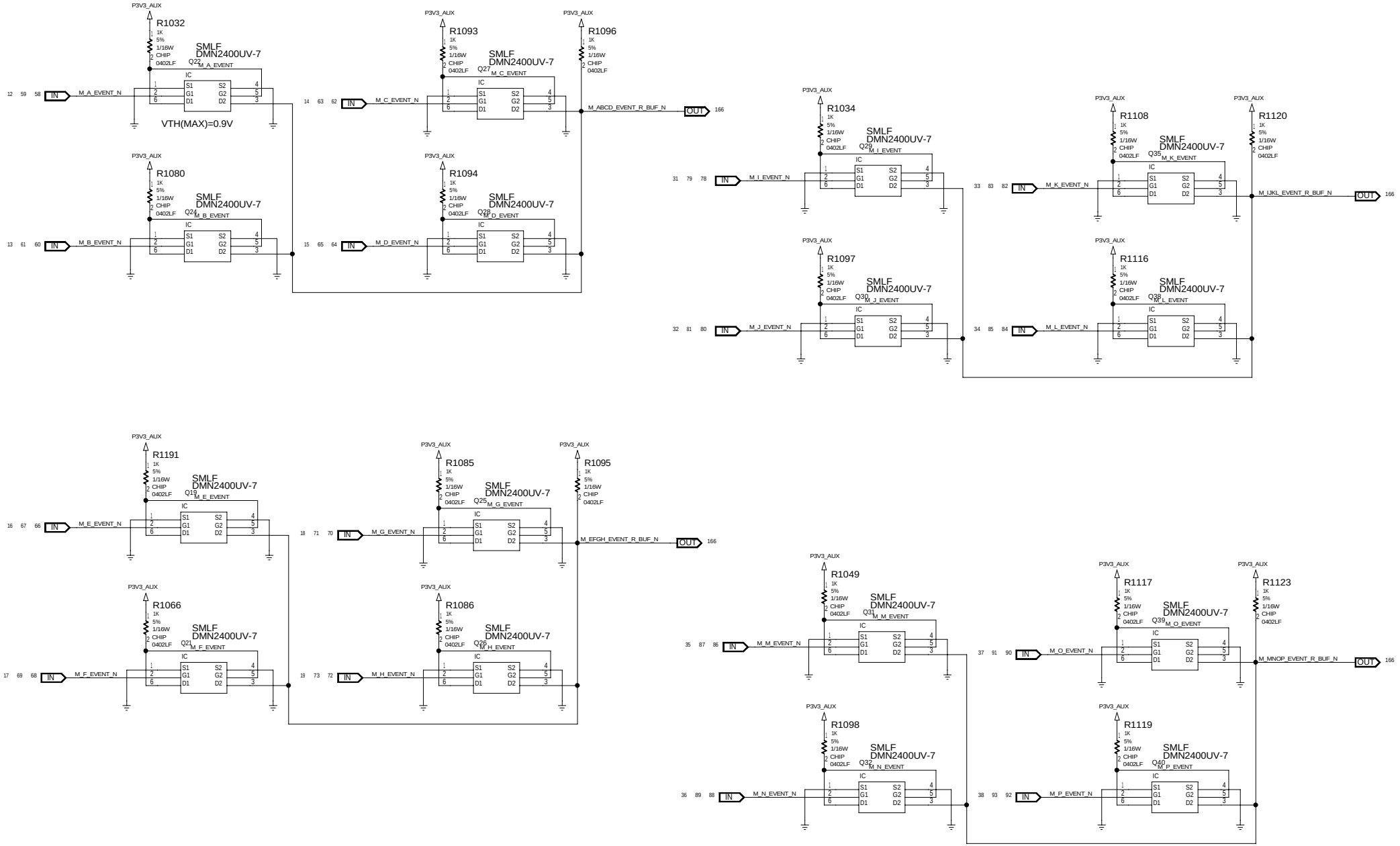
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:31:24 2017	SHEET 54 OF 226



DIMM SMBUS

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:16 2017 SHEET 55 OF 226



MEM_EVENT

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:22:10 2017 SHEET 56 OF 226

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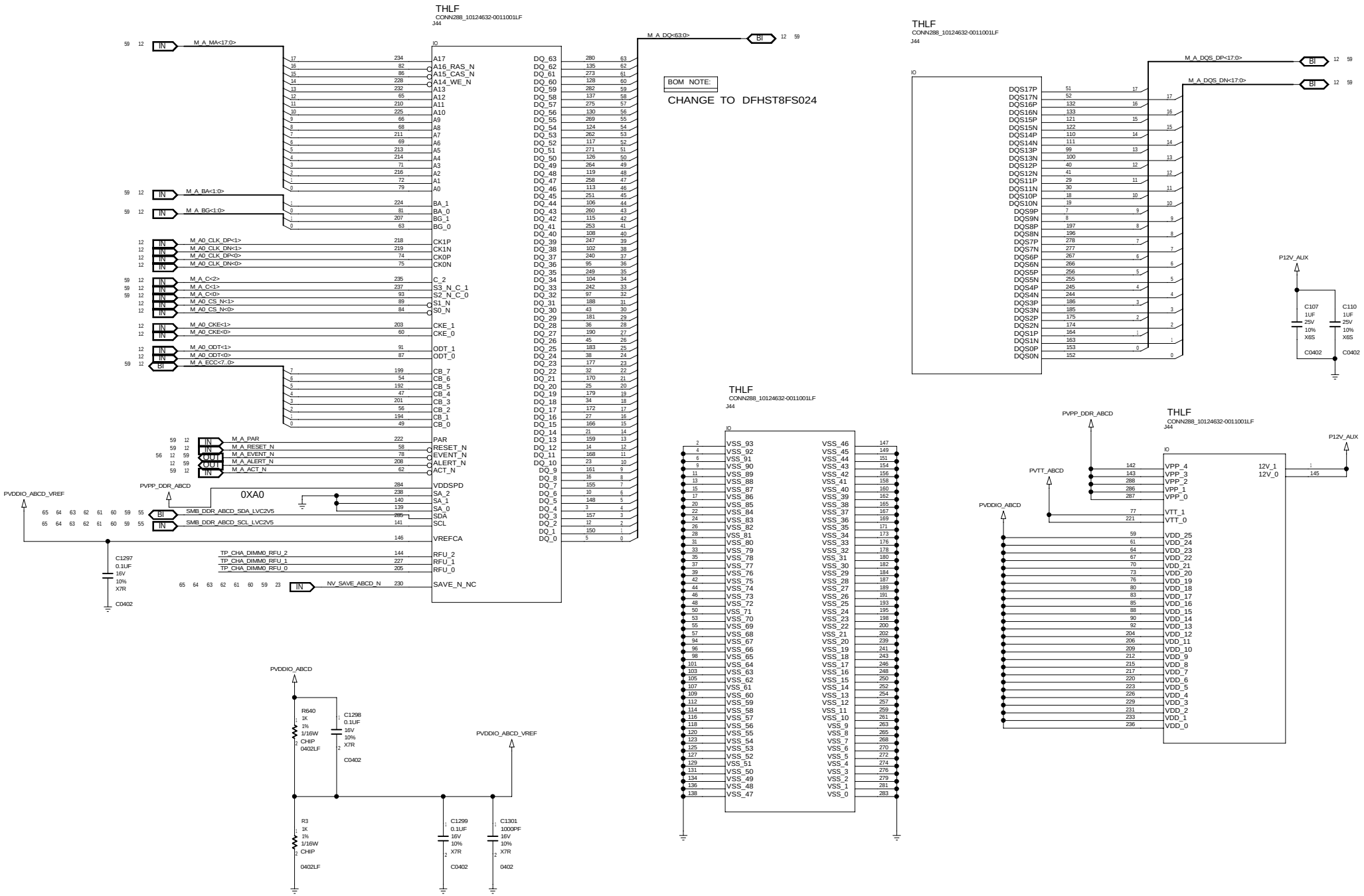
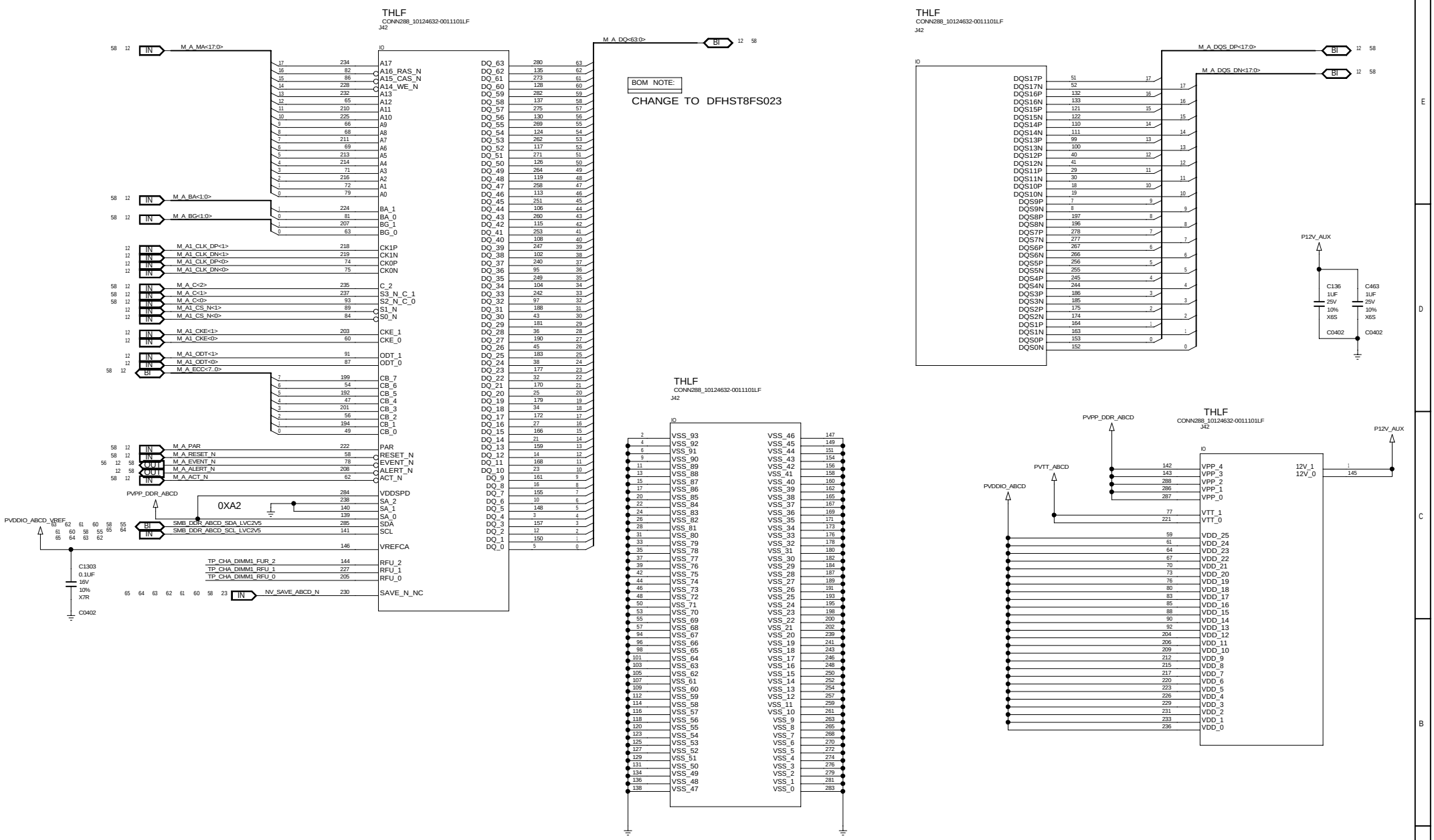
Quanta	DEPARTMENT CCBU	DESIGNER REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 19:31:26 2017	SHEET 57 OF 226



CPU0 DDR4 CH_A1(YELLOW)

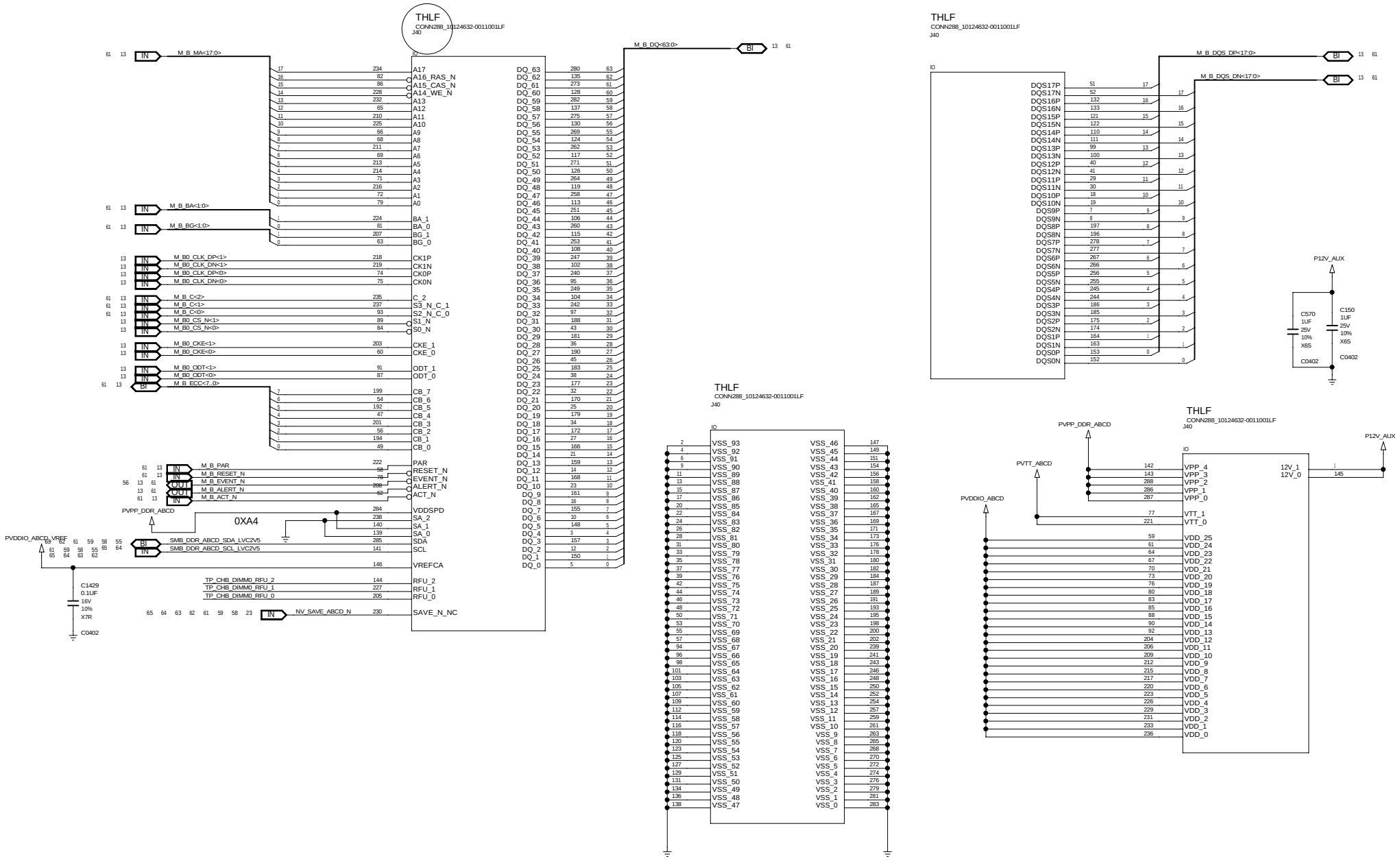
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:39 2017 SHEET 58 OF 226



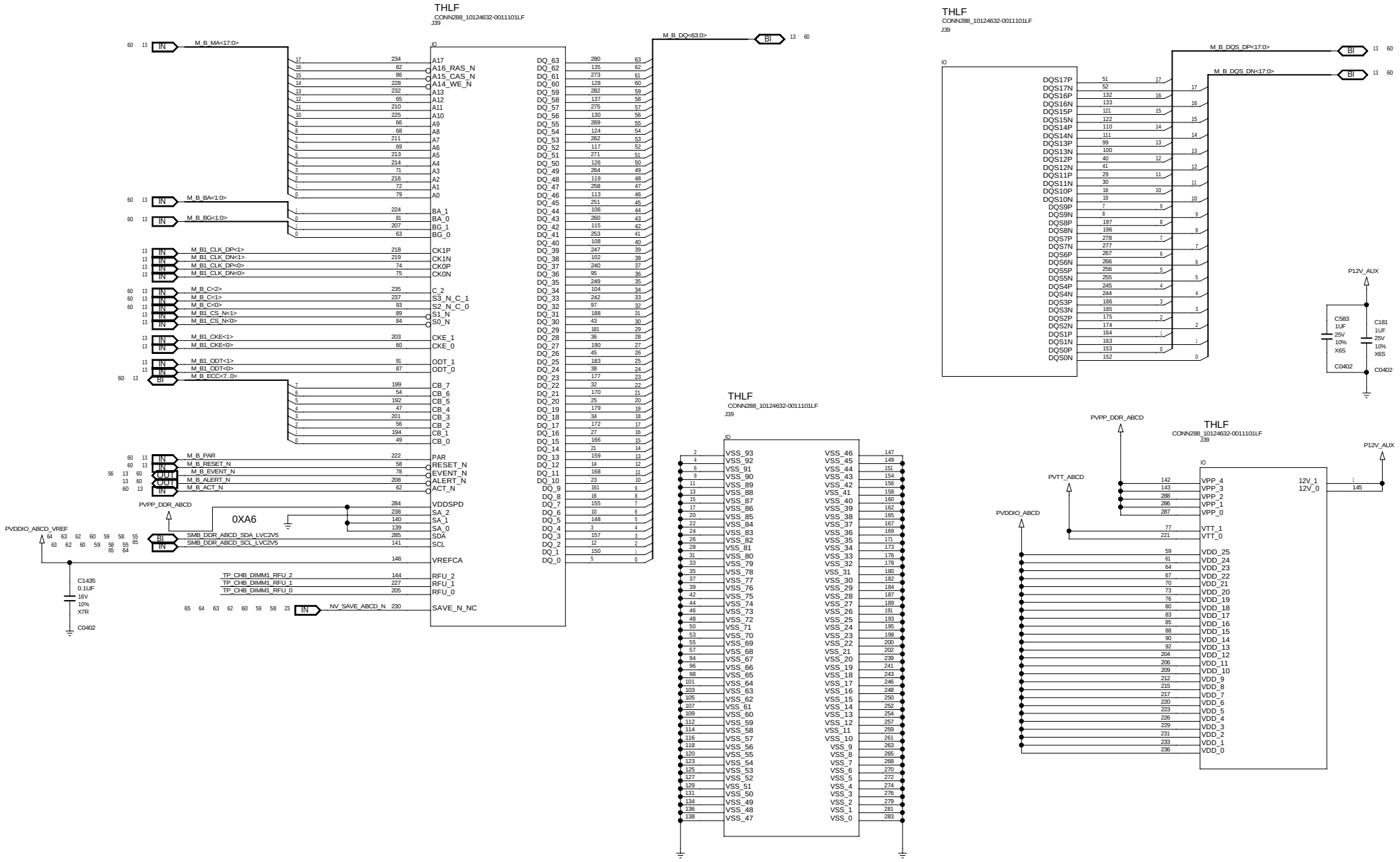
CPU0 DDR4 CH_A2(BLACK)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:40 2017	SHEET 59 OF 226



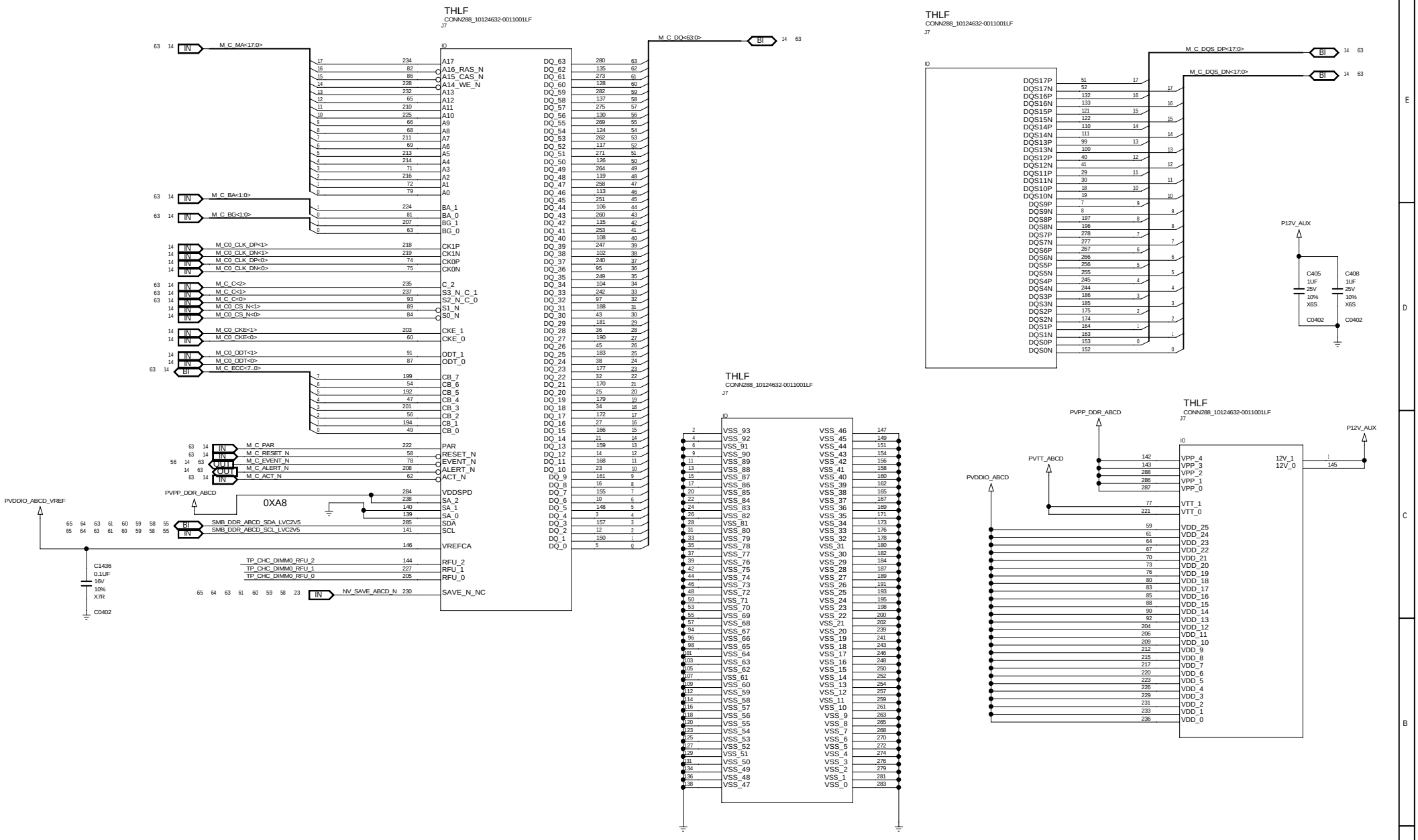
CPU0 DDR4 CH_B1(YELLOW)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:40 2017	SHEET 60 OF 226



CPU0 DDR4 CH_B2(BLACK)

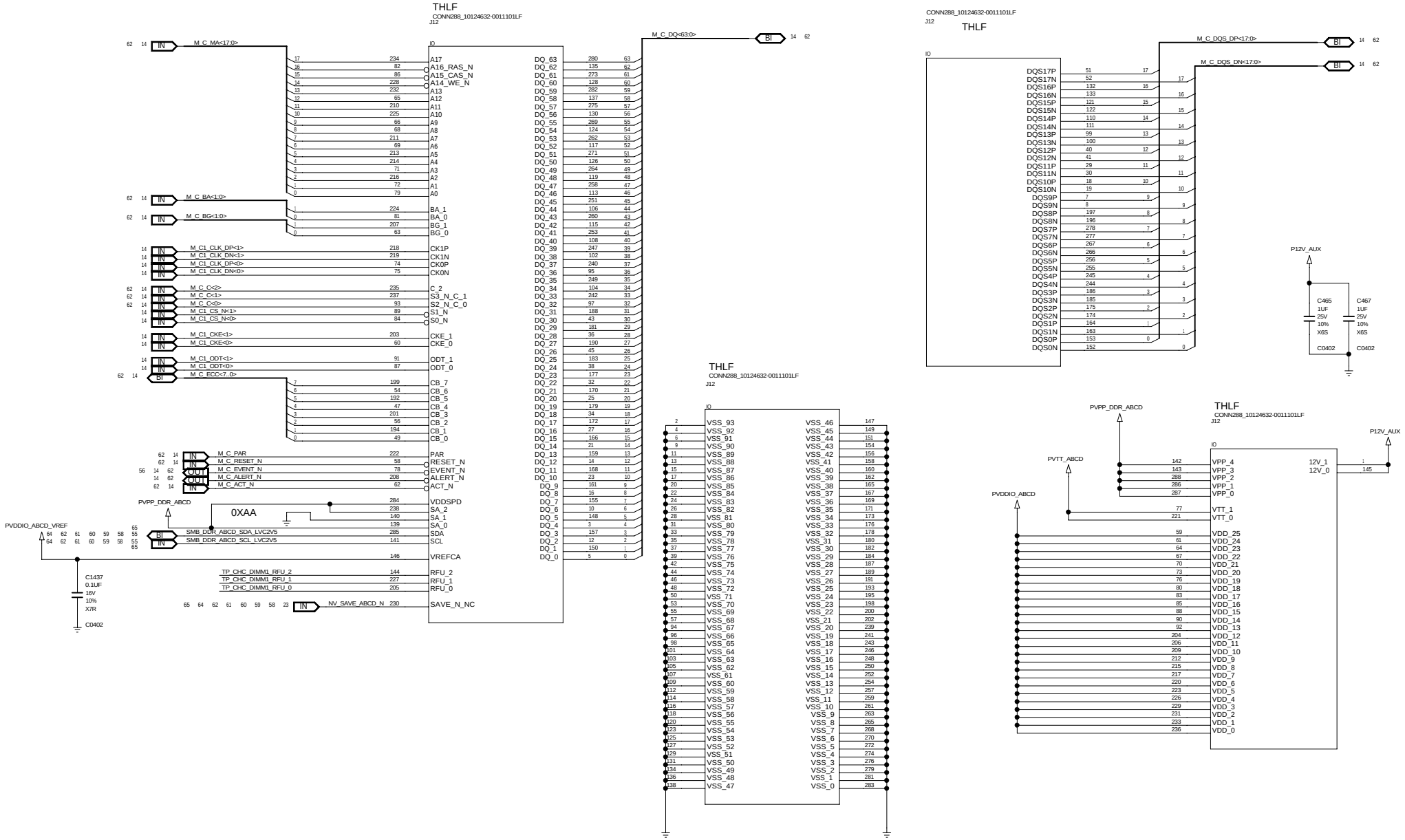
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:40 2017	SHEET 61 OF 226



CPU0 DDR4 CH_C1(YELLOW)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

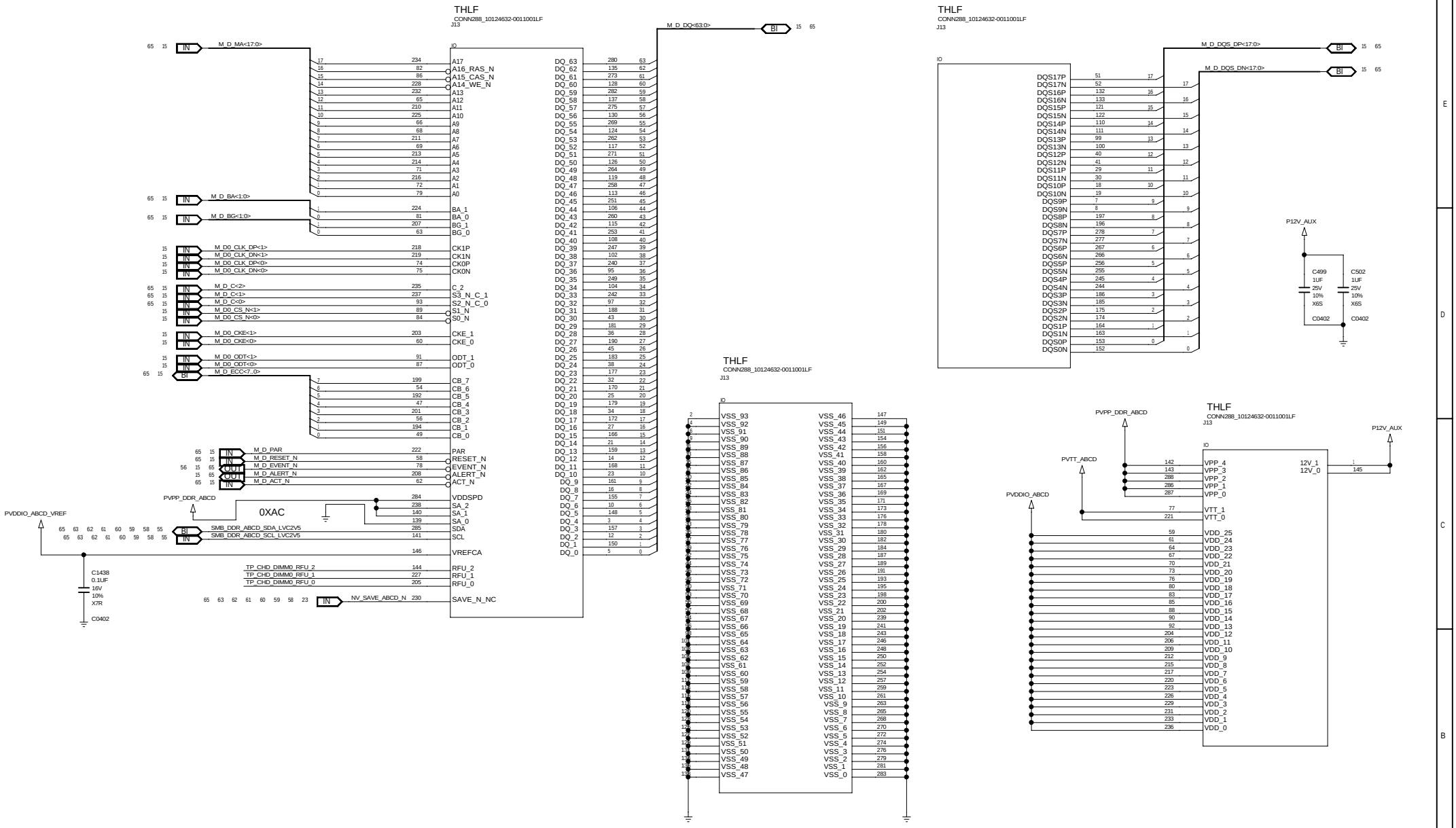
SIZE C DATE Fri Dec 15 20:21:41 2017 SHEET 62 OF 226



CPU0 DDR4 CH_C2(BLACK)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

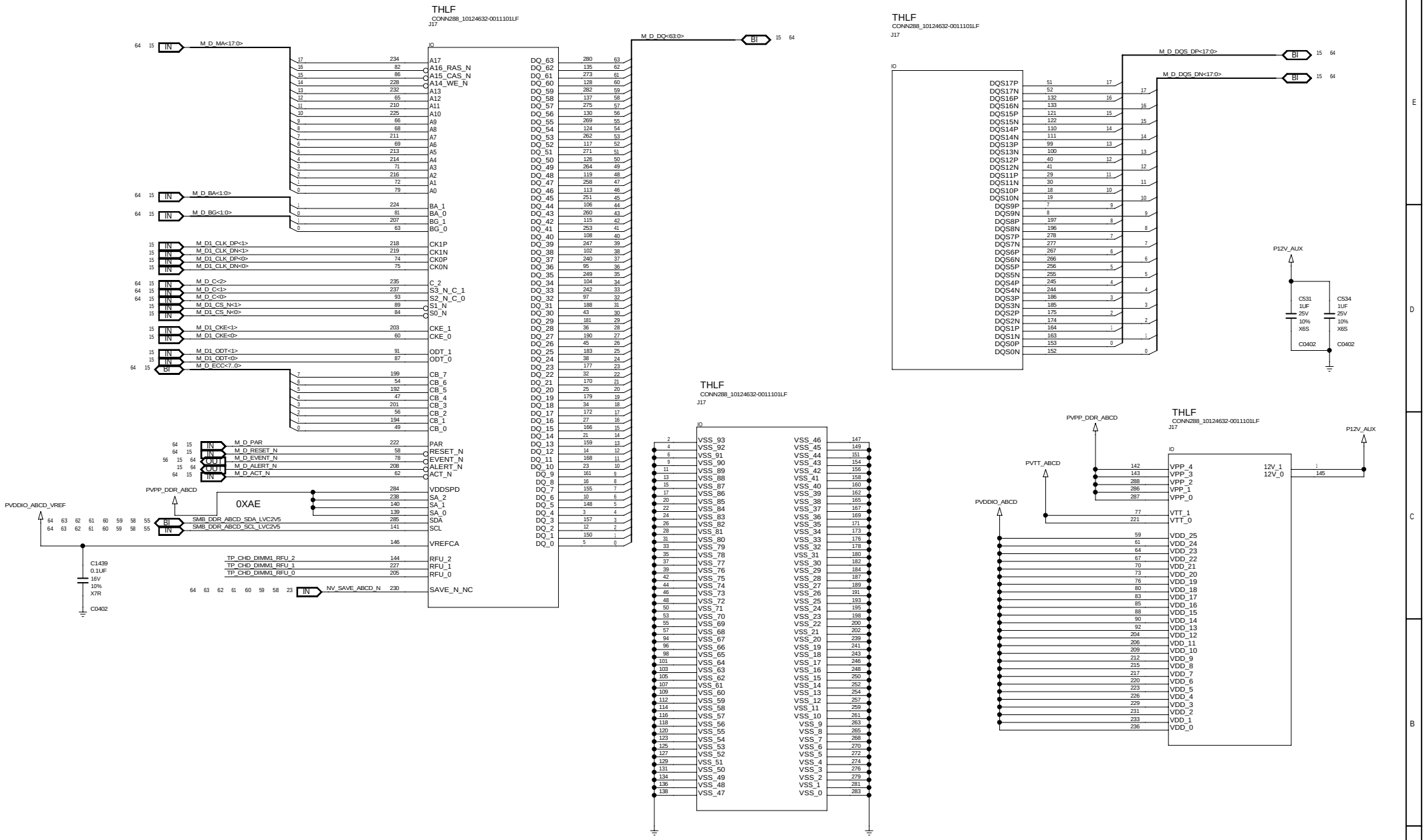
SIZE C DATE Fri Dec 15 20:21:41 2017 SHEET 63 OF 226



CPU0 DDR4 CH_D1(YELLOW)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

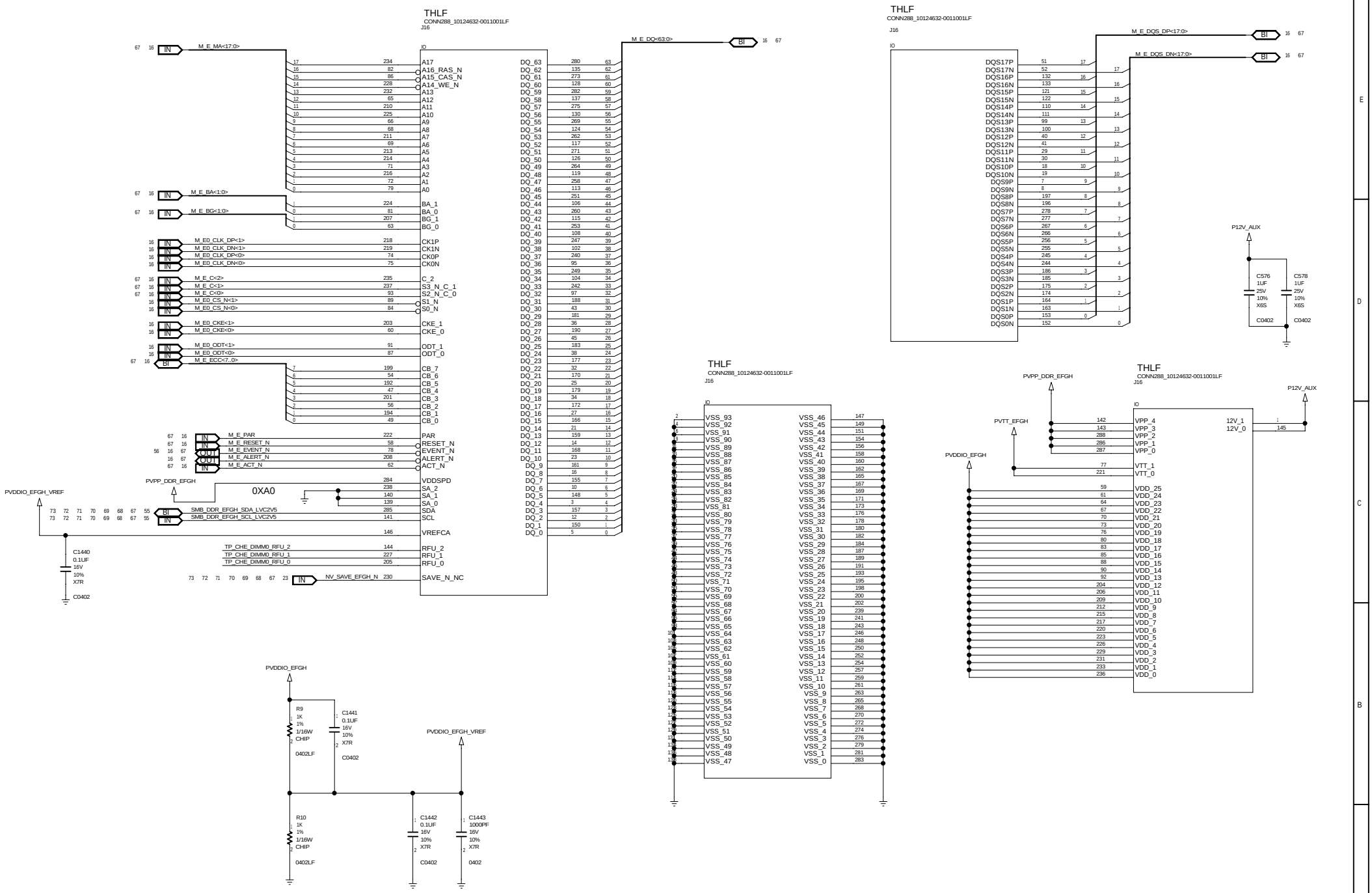
SIZE C DATE Fri Dec 15 20:21:42 2017 SHEET 64 OF 226



CPU0 DDR4 CH D2(BLACK)

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:42 2017 SHEET 65 OF 226

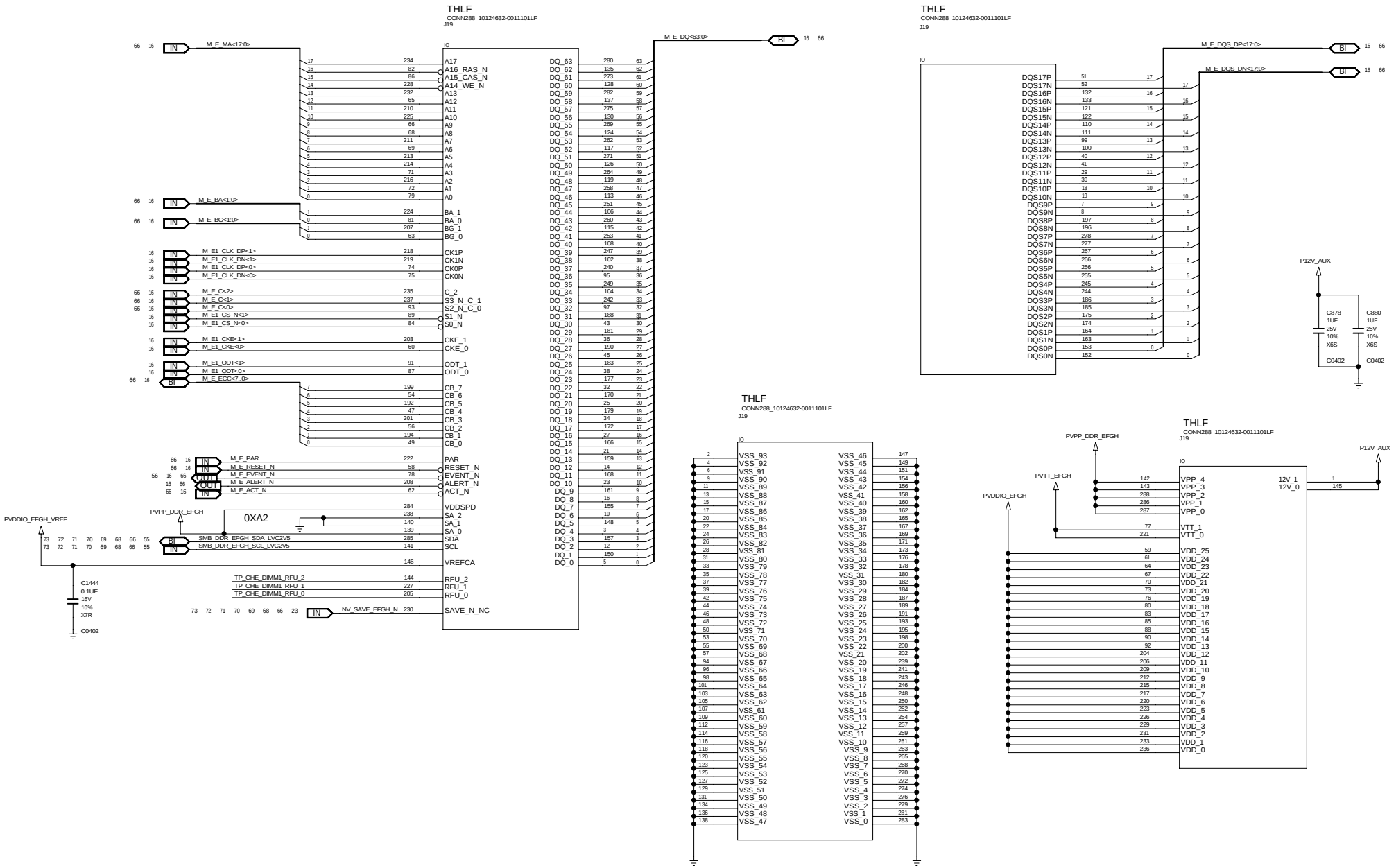


LAYOOUT: PLEASE NEAR DIMMS

CPU0 DDR4 CH_E1(YELLOW)

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

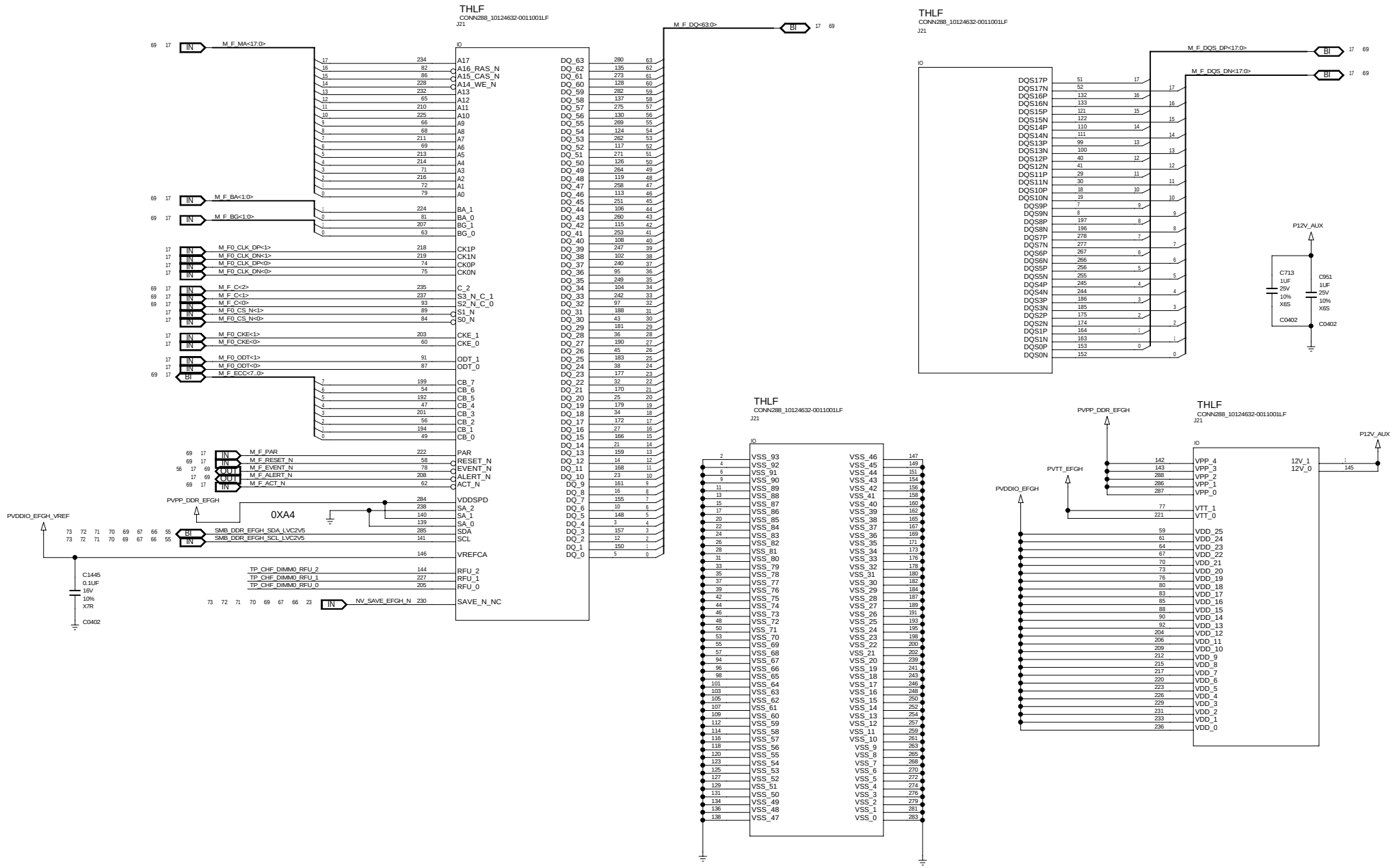
SIZE C DATE Fri Dec 15 20:21:42 2017 SHEET 66 OF 226



CPU0 DDR4 CH E2(BLACK)

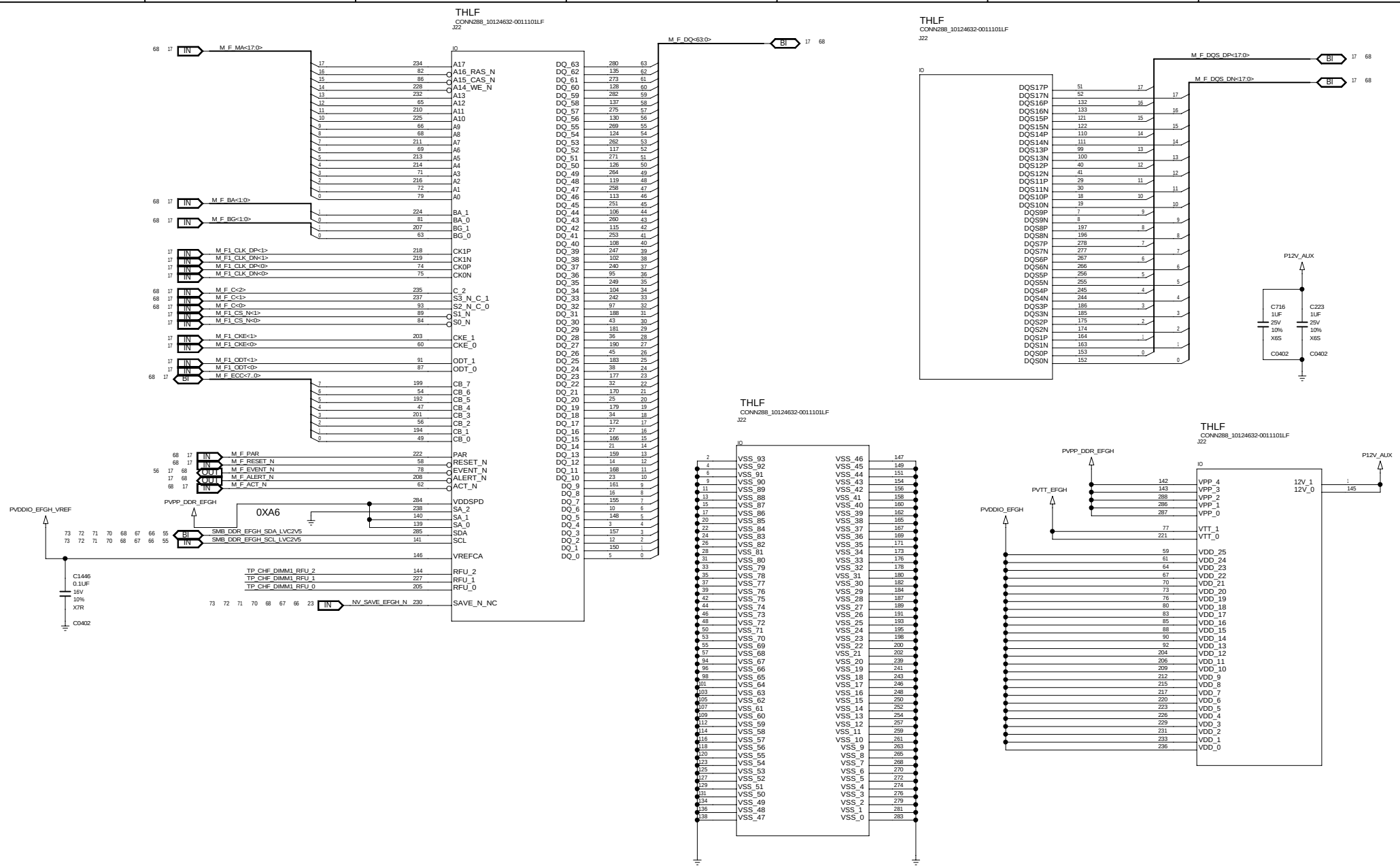
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:43 2017 SHEET 67 OF 226



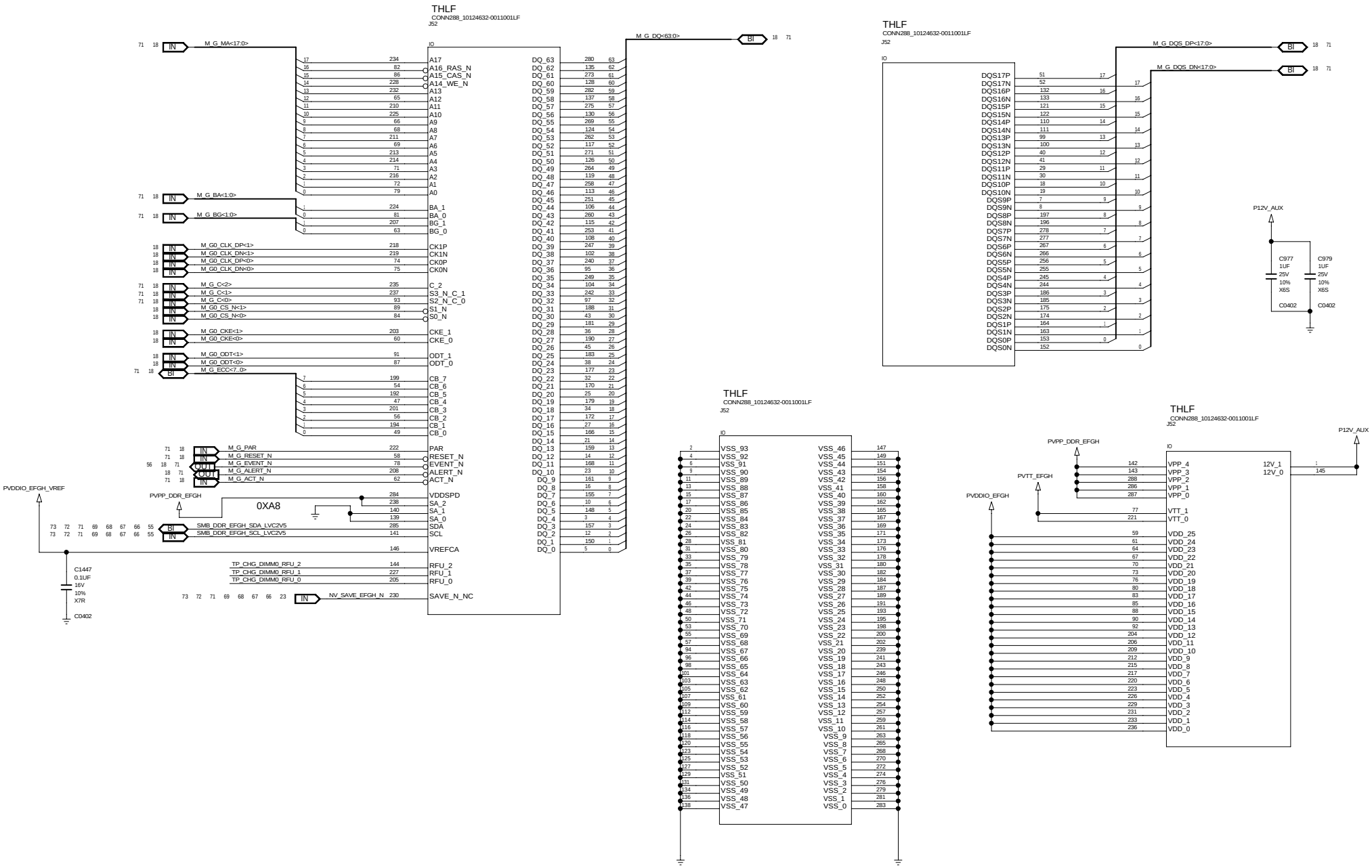
CPU0 DDR4 CH_F1(YELLOW)

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:43 2017	SHEET 68 OF 226



CPU0 DDR4 CH F2(BLACK)

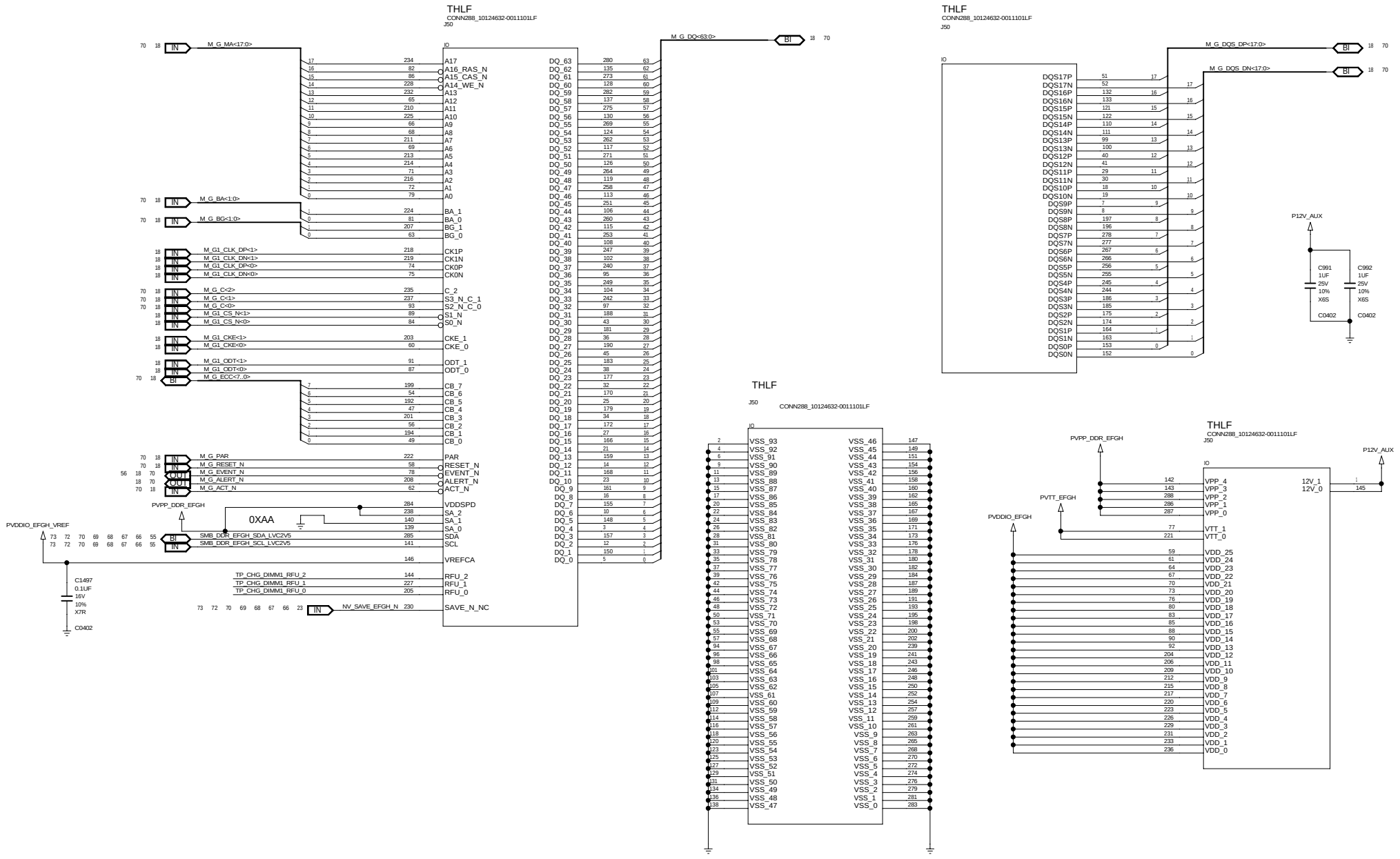
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:43 2017	SHEET 69 OF 226



CPU0 DDR4 CH_G1(YELLOW)

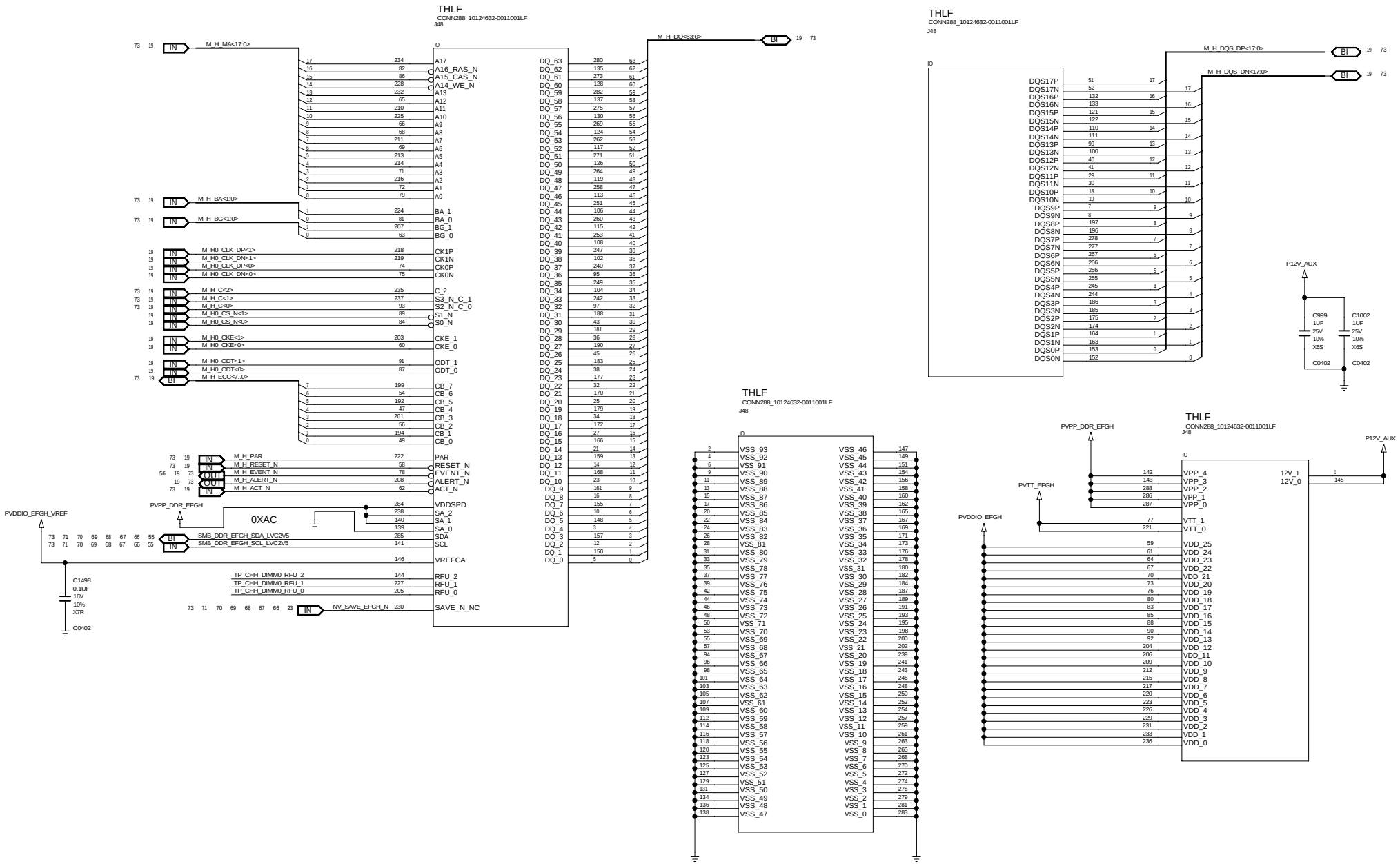
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:44 2017 SHEET 70 OF 226



CPU0 DDR4 CH G2(BLACK)

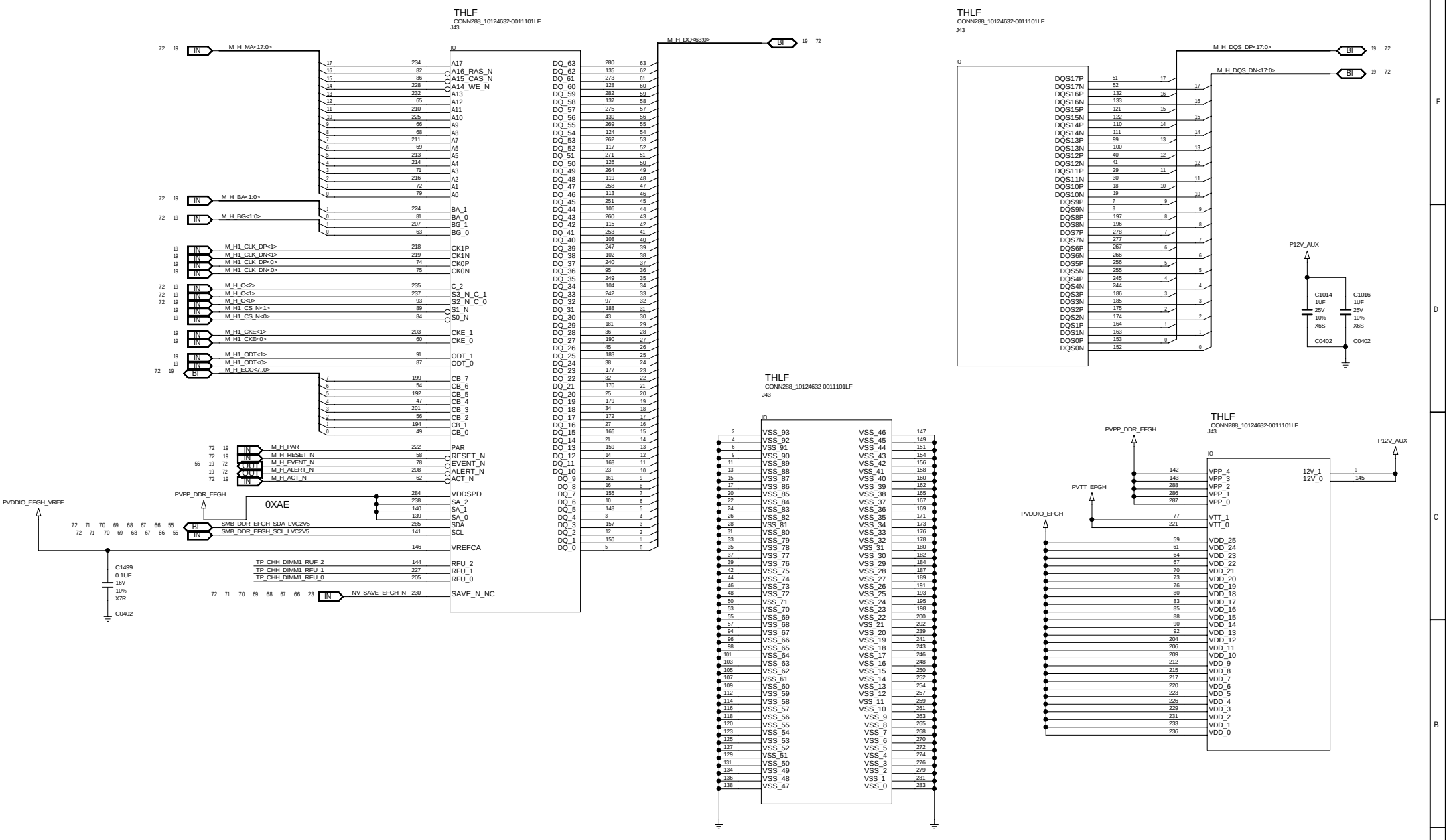
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:44 2017	SHEET 71 OF 226	



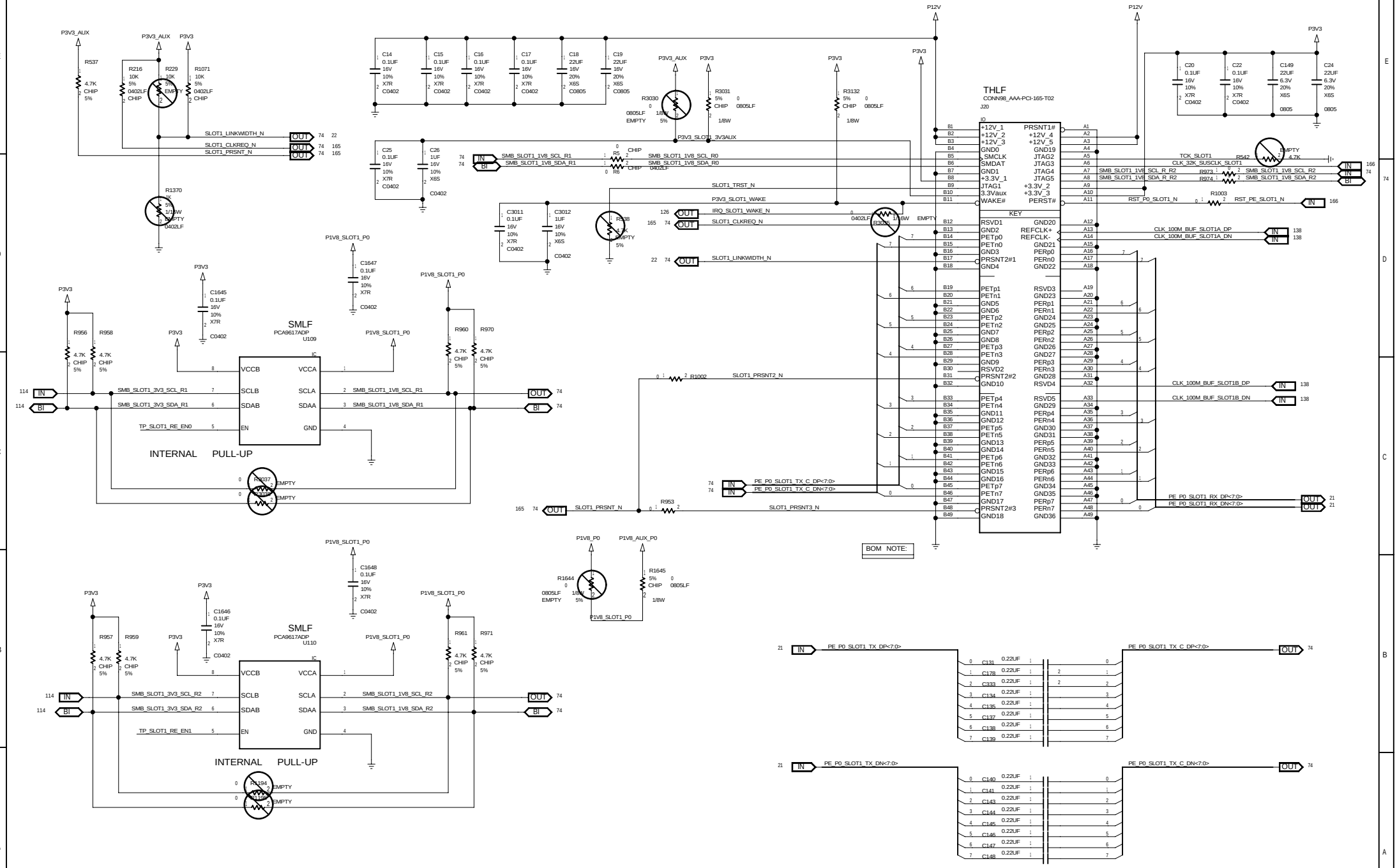
CPU0 DDR4 CH_H1(YELLOW)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:45 2017 SHEET 72 OF 226



CPU0 DDR4 CH H2(BLACK)	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>
	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C DATE Fri Dec 15 20:21:45 2017 SHEET 73 OF 226



PCIE SLOT1

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C	DATE Fri Dec 15 20:21:45 2017
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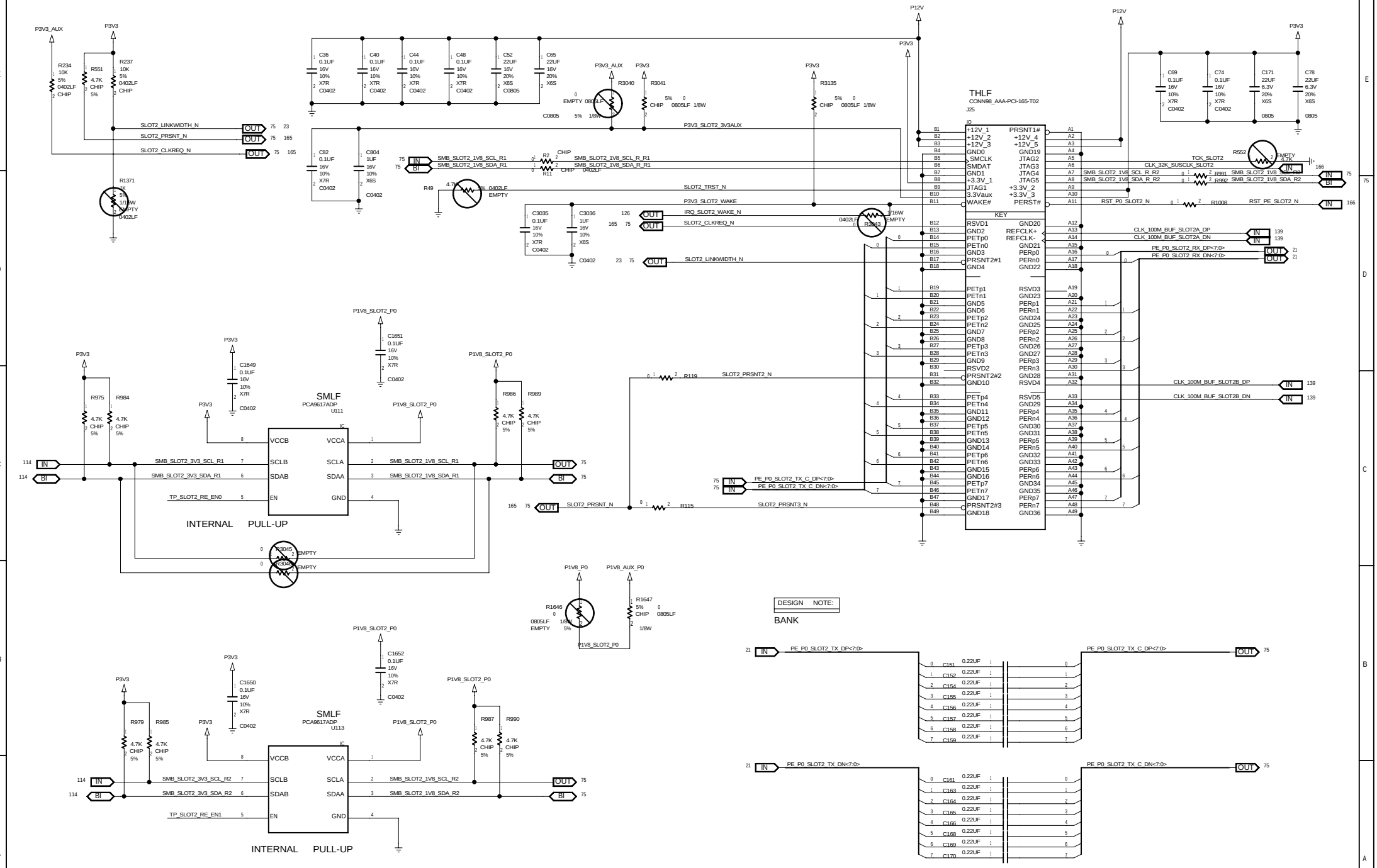
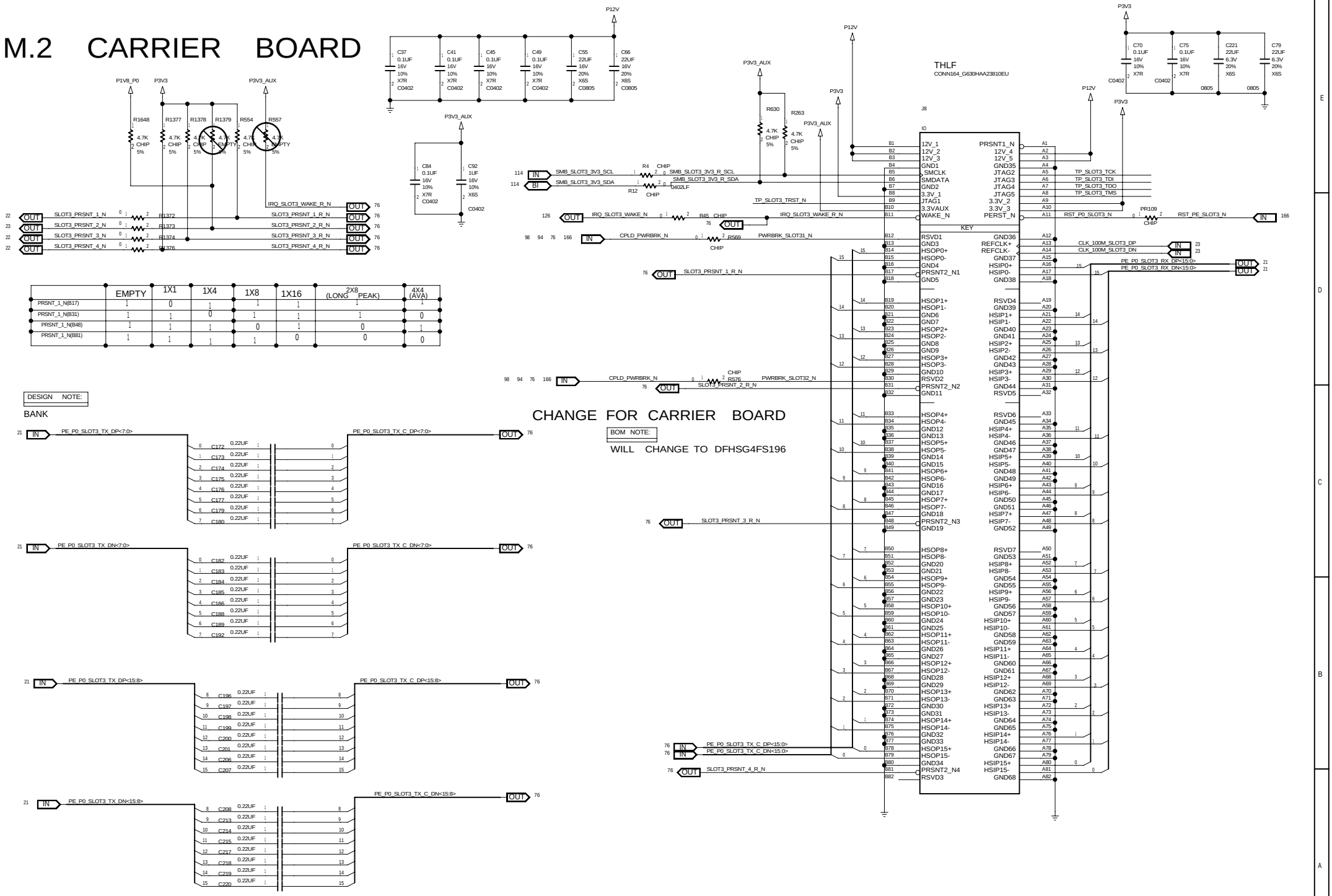


PCIE SLOT2

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>
		REVIEWER	DOCUMENT NUMBER: <Q_NUMBER>
			REV: <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:46 2017 SHEET 75 OF 226

M.2 CARRIER BOARD



	EMPTY	1X1	1X4	1X8	1X16	2X8 (LONG PEAK)	4X4 (AVA)
PRSNT_1_N(B17)	1	0	1	1	1	1	1
PRSNT_1_N(B31)	1	1	0	1	1	1	0
PRSNT_1_N(B48)	1	1	1	0	1	0	1
PRSNT_1_N(B81)	1	1	1	1	0	0	0

DESIGN NOTE:

BANK

CHANGE FOR CARRIER BOARD

BOM NOTE:

WILL CHANGE TO DFHSG4FS196

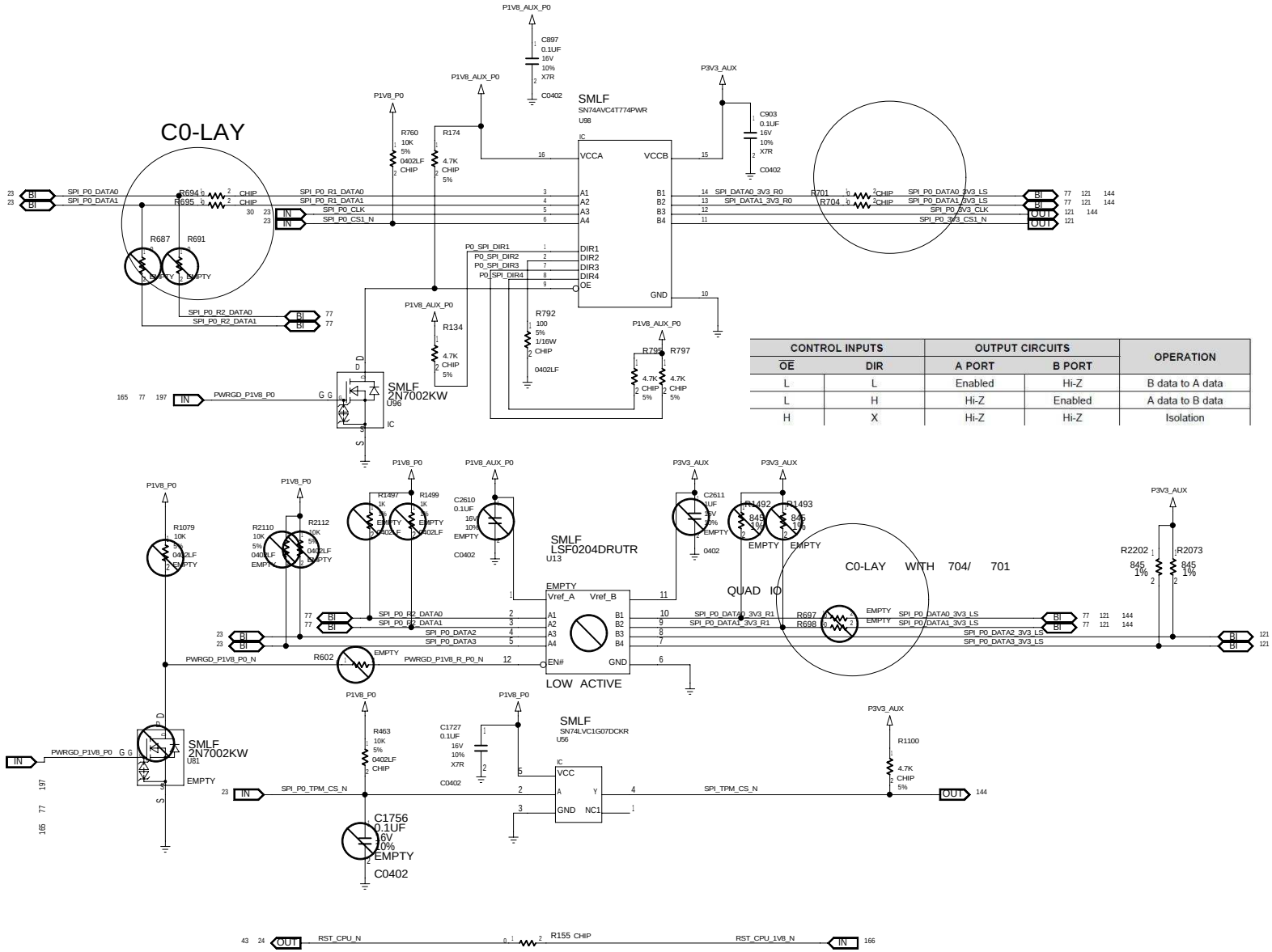
PCIE SLOT3

SYMBOL AND NET NAME ARE NOT READY

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:46 2017 SHEET 76 OF 226

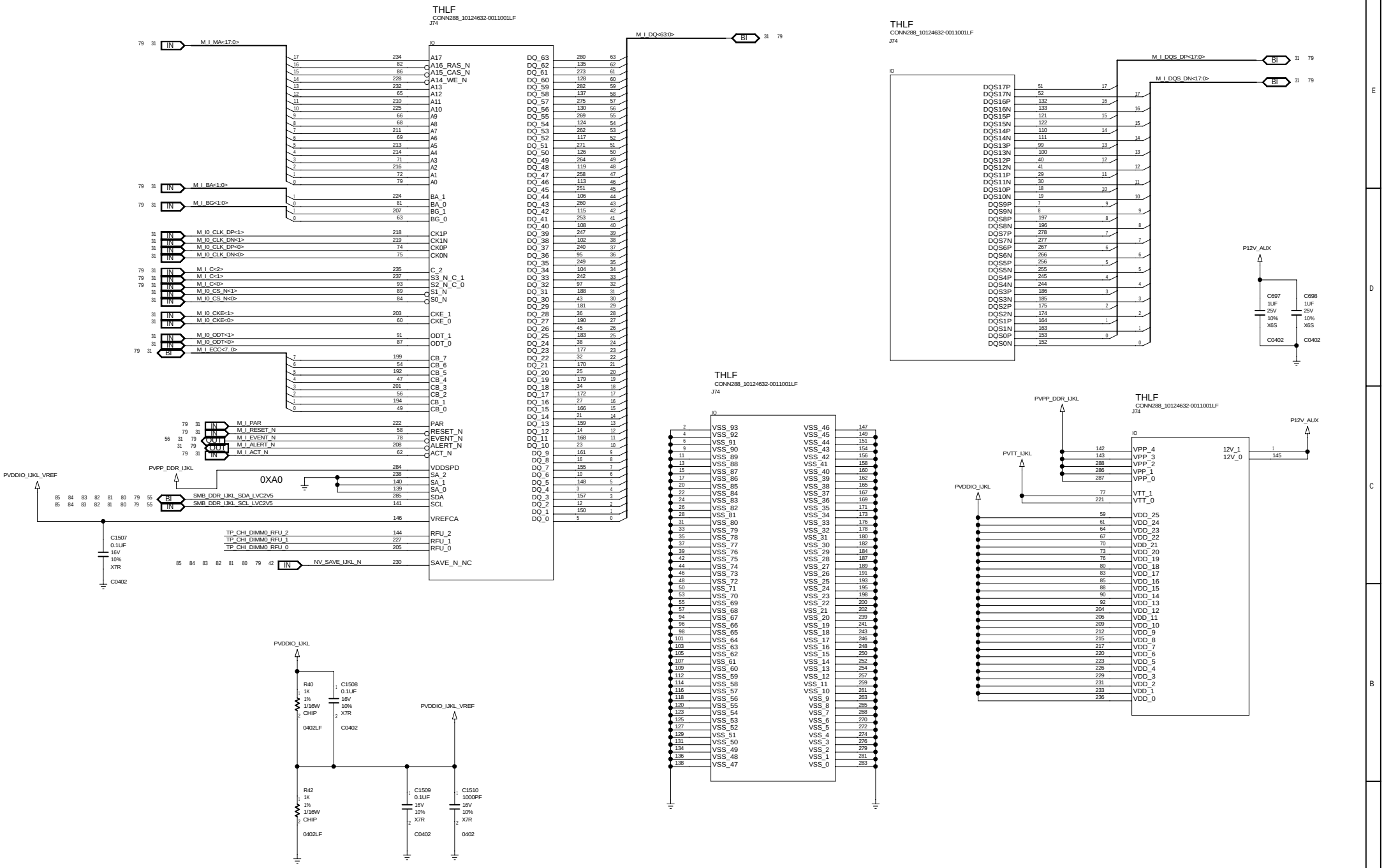
1.8V/3.3V VOLTAGE TRANSLATION



CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

SPI TRANSLATION

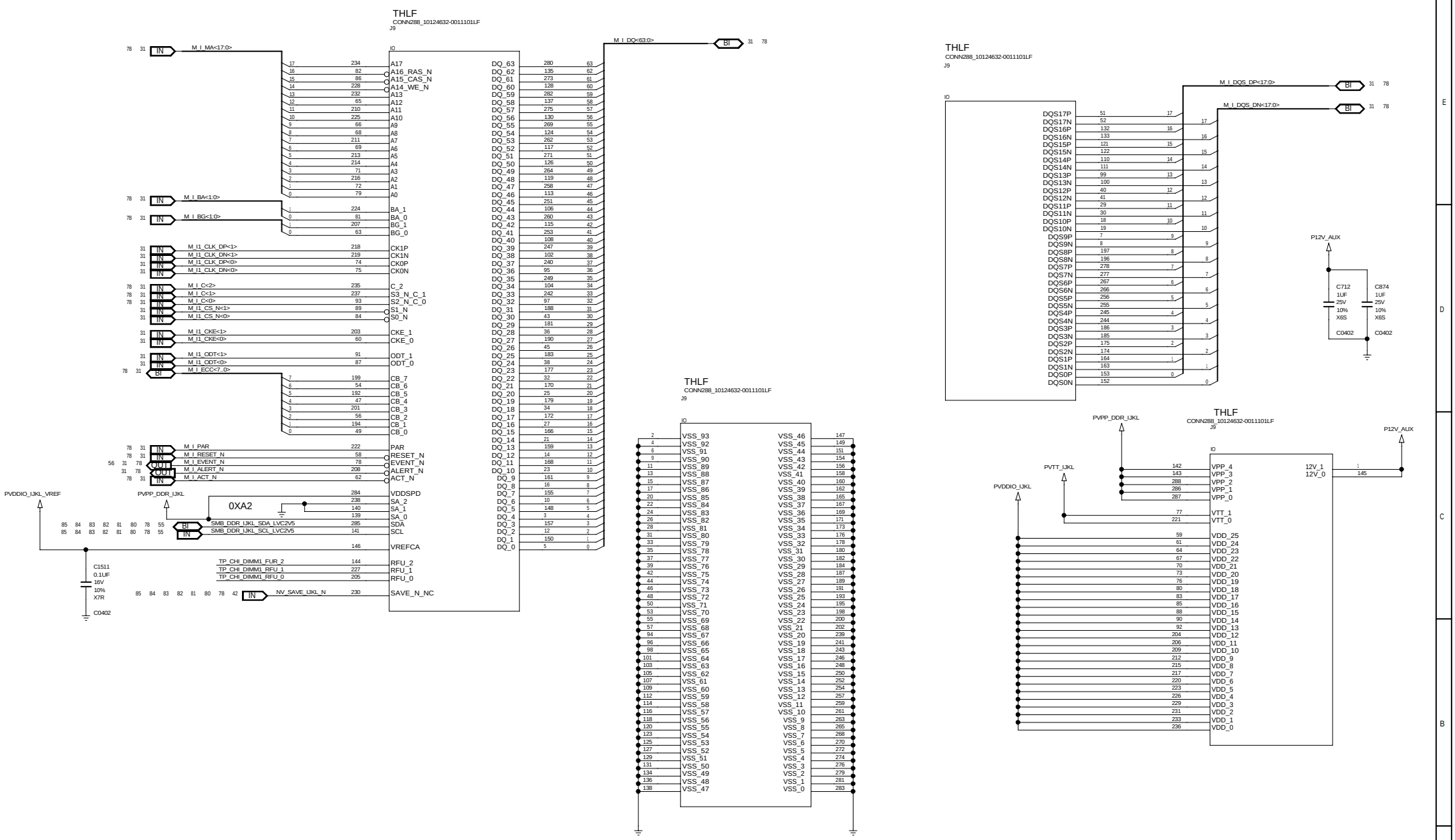
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C	DATE Fri Dec 15 20:21:20 2017
SHEET 77 OF 226			



CPU1 DDR4 CH_I1(YELLOW)

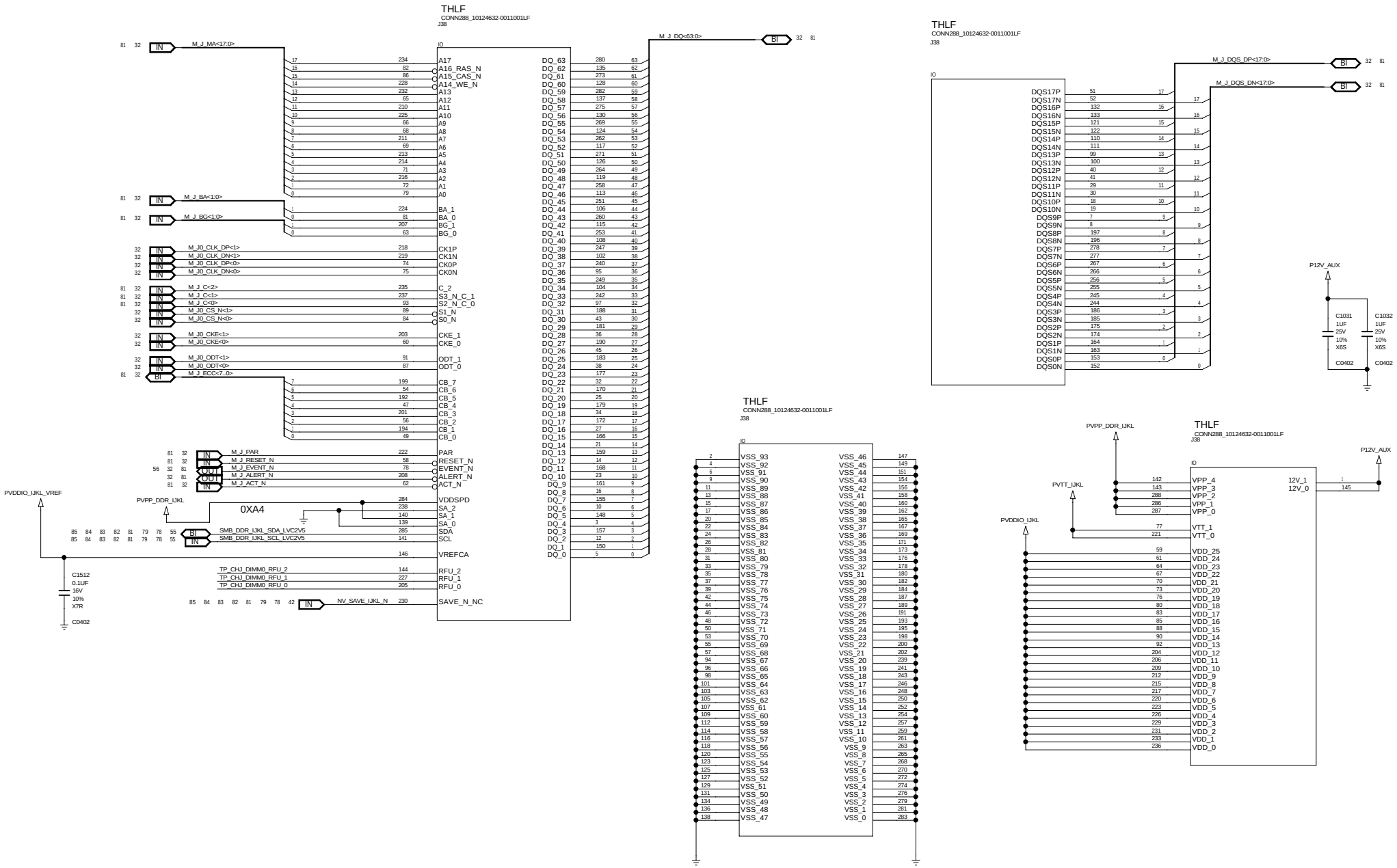
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:46 2017 SHEET 78 OF 226



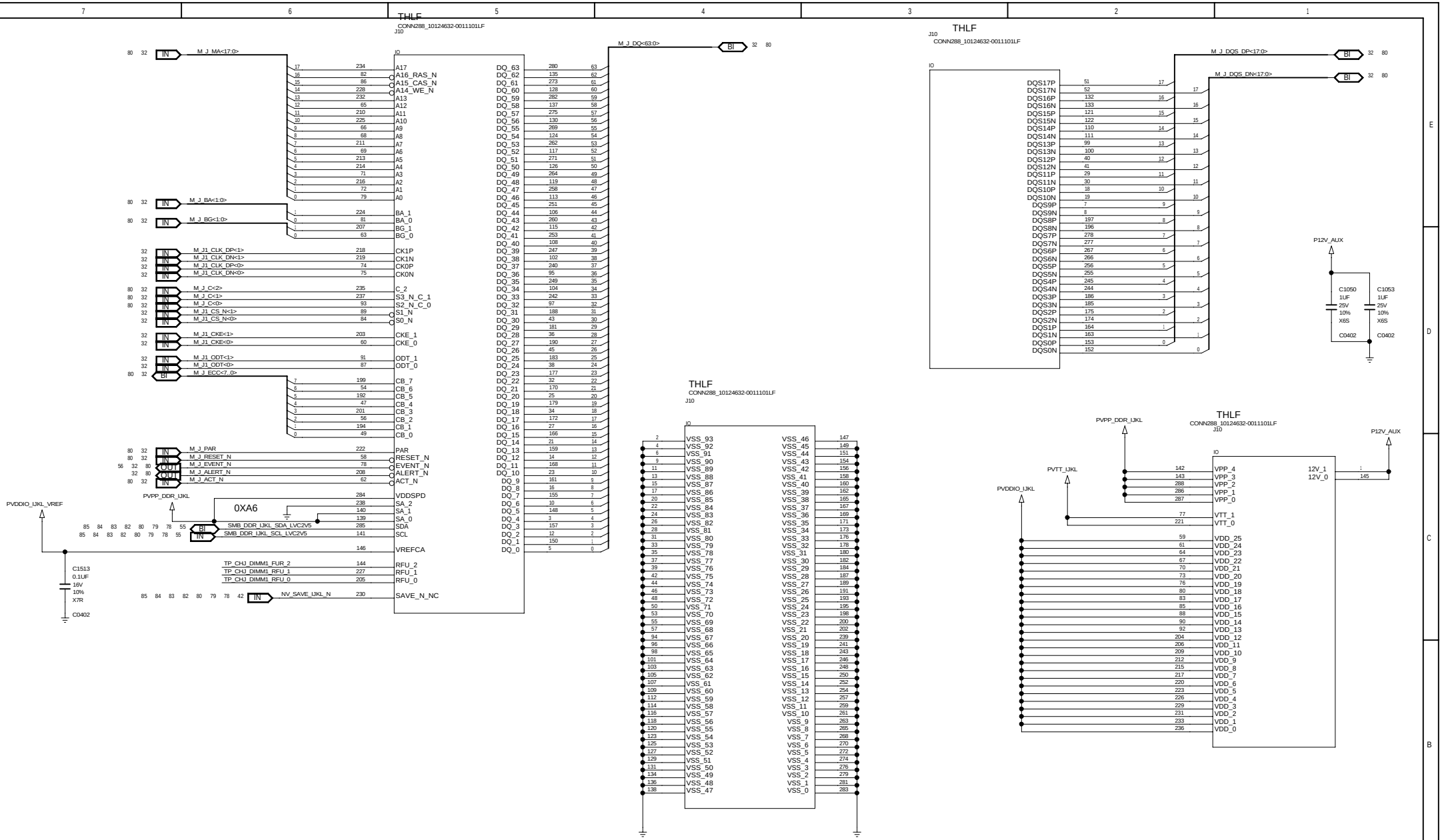
CPU1 DDR4 CH_I2(BLACK)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:47 2017	SHEET 79 OF 226



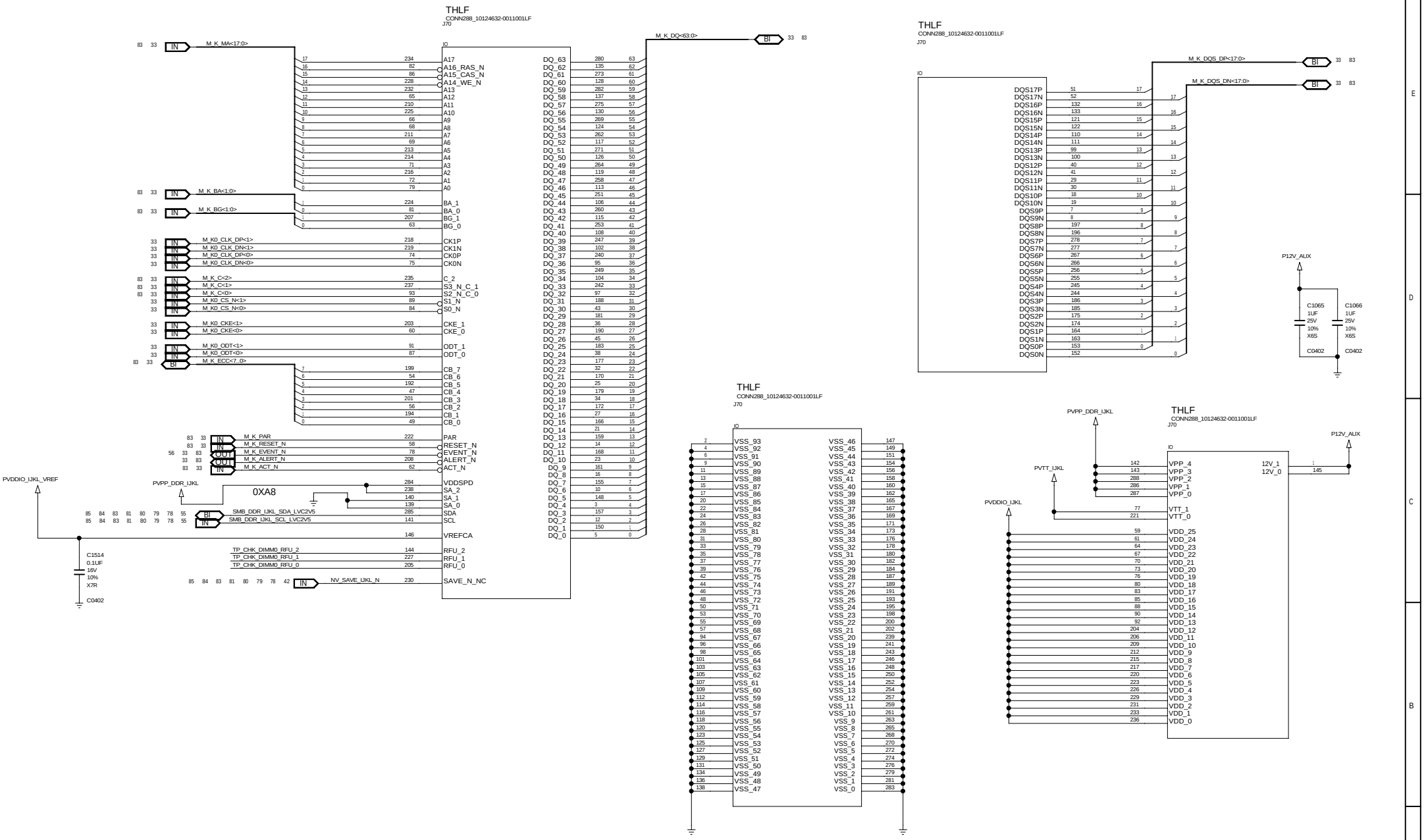
CPU1 DDR4 CH J1(YELLOW)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:47 2017	SHEET 80 OF 226



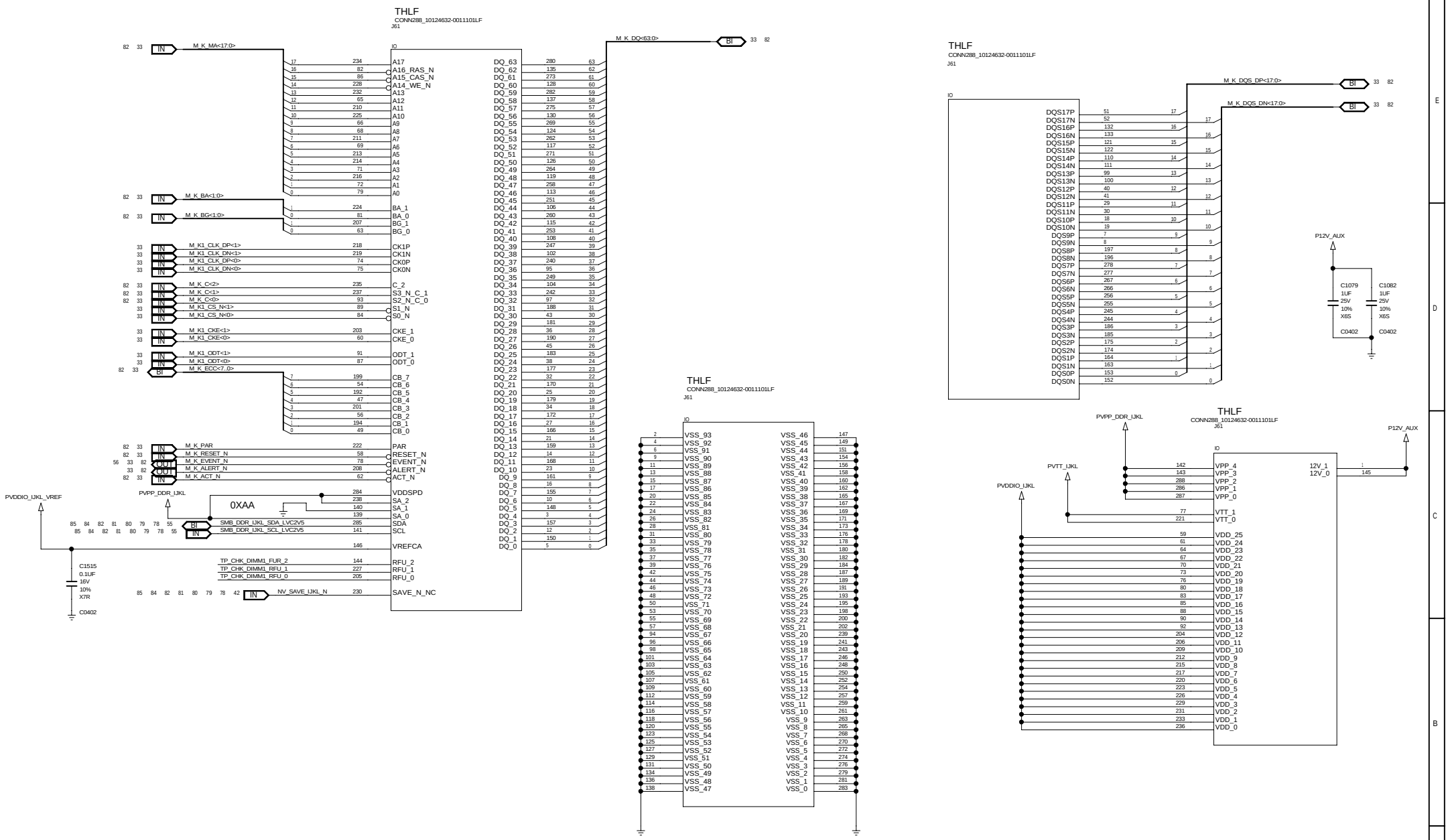
CPU1 DDR4 CH_J2(BLACK)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:47 2017	SHEET 81 OF 226	



CPU1 DDR4 CH K1(YELLOW)

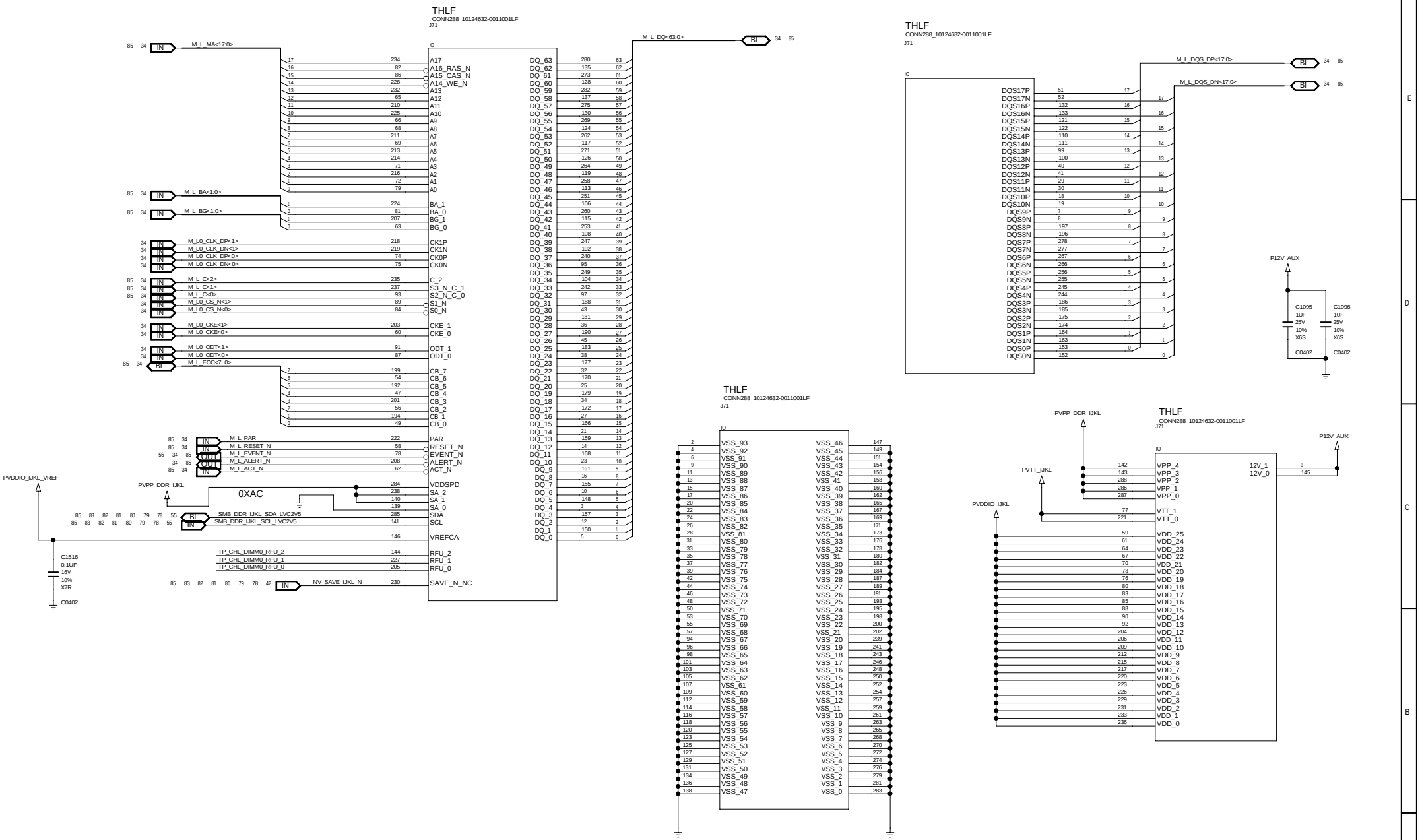
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:48 2017	SHEET 82 OF 226	



CPU1 DDR4 CH_K2(BLACK)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:48 2017 SHEET 83 OF 226



CPU1 DDR4 CH L1(YELLOW)

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
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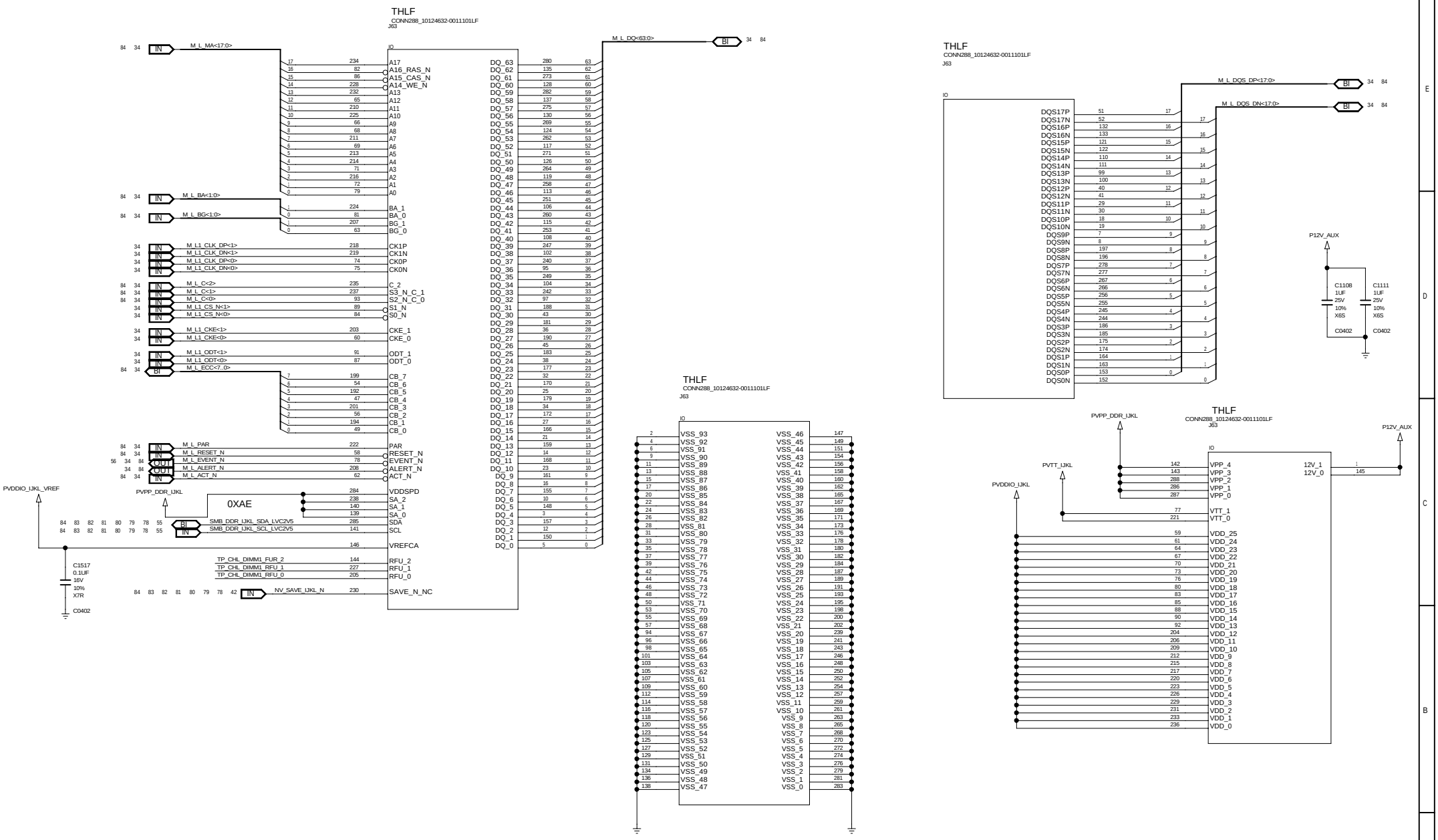
SIZE C DATE Fri Dec 15 20:21:49 2017 SHEET 84 OF 226



CPU1 DDR4 CH_L2(BLACK)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
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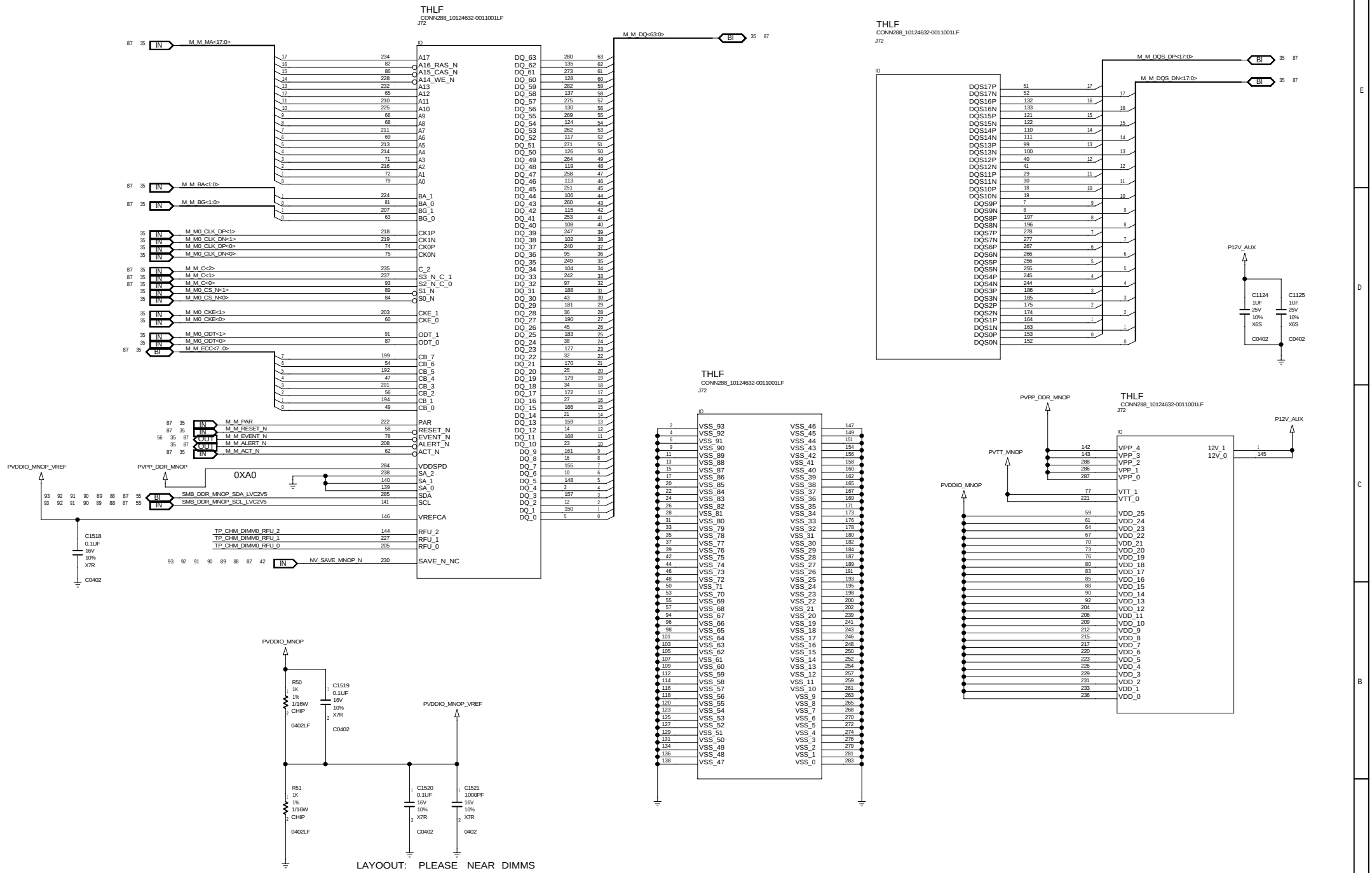
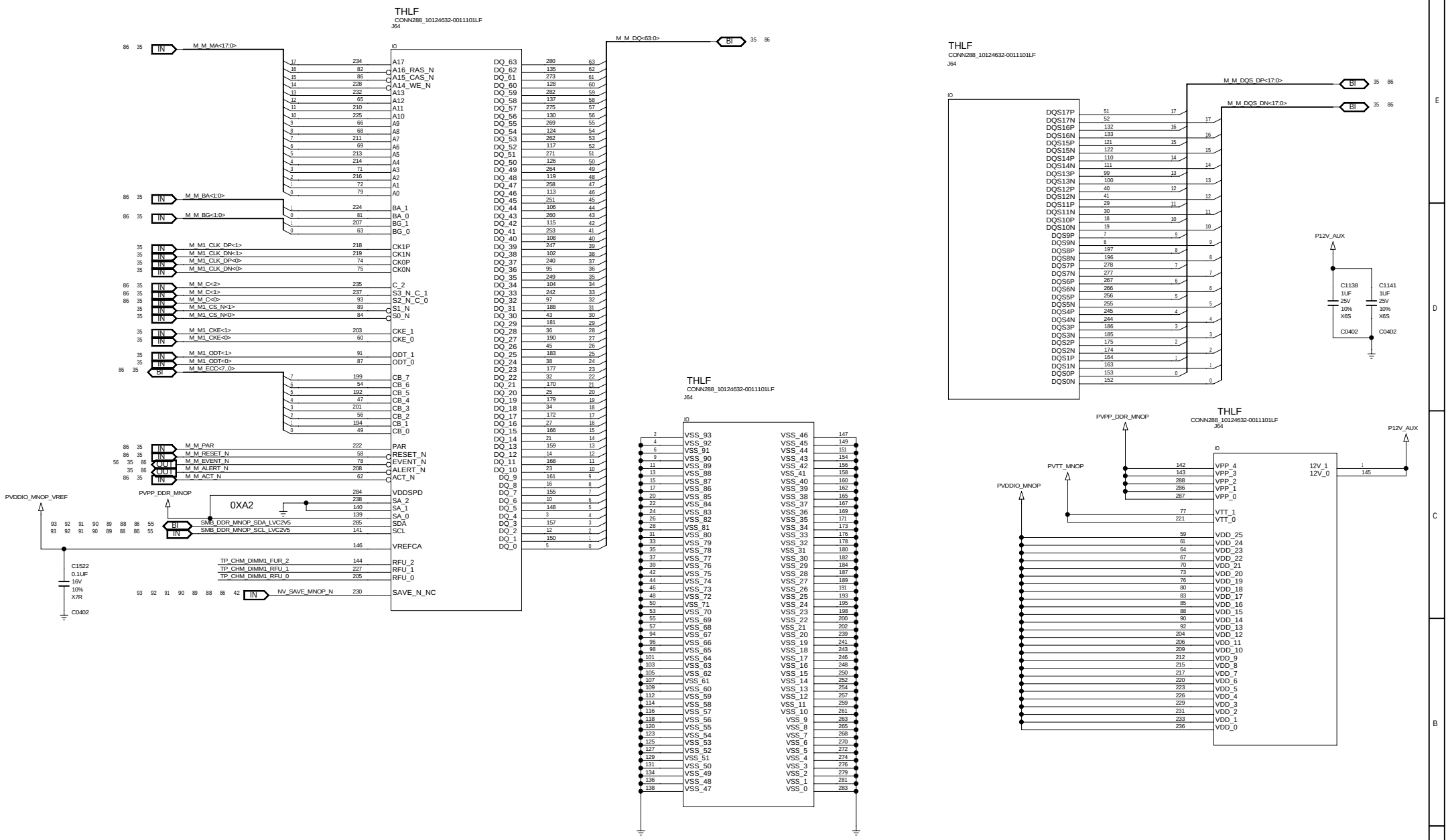
	REVIEWER	SIZE C	DATE Fri Dec 15 20:21:49 2017	SHEET 85 OF 226



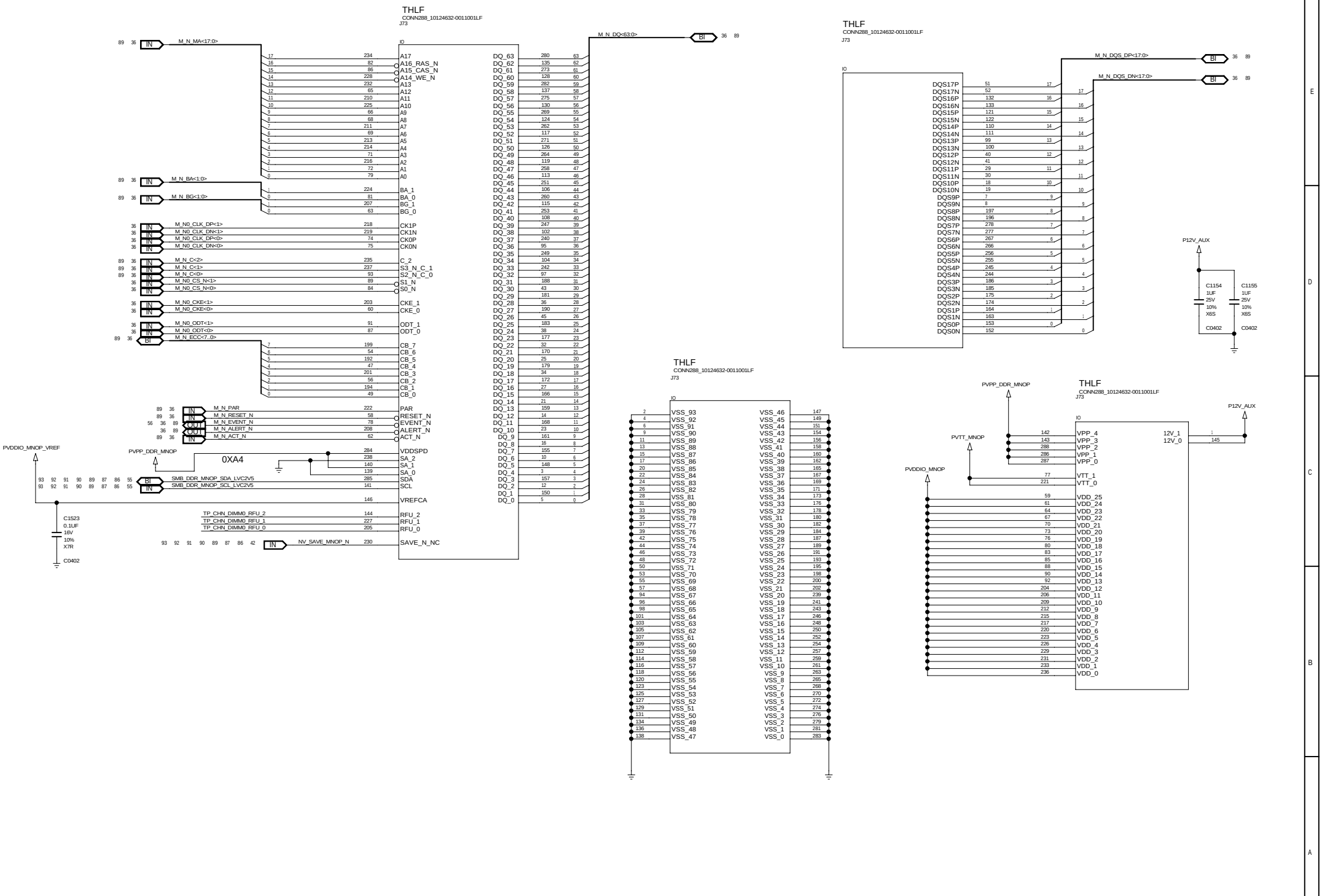
CPU1 DDR4 CH M1(YELLOW)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C	DATE Fri Dec 15 20:21:49 2017
SHEET 86 OF 226			



CPU1 DDR4 CH M2(BLACK)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:50 2017	SHEET 87 OF 226



CPU1 DDR4 CH N1(YELLOW)

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
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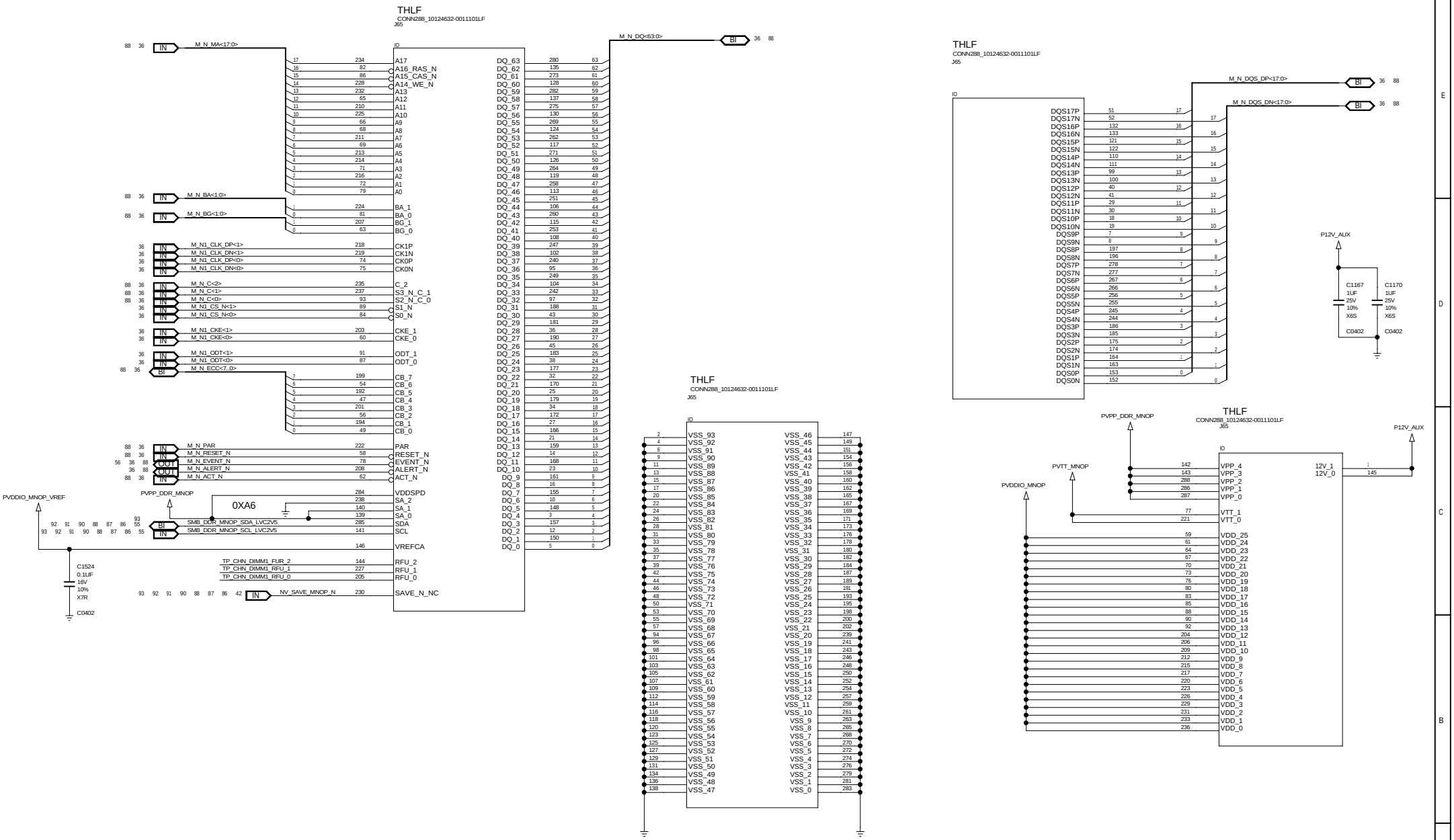
SIZE C DATE Fri Dec 15 20:21:50 2017 SHEET 88 OF 226



CPU1 DDR4 CH_N2(BLACK)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
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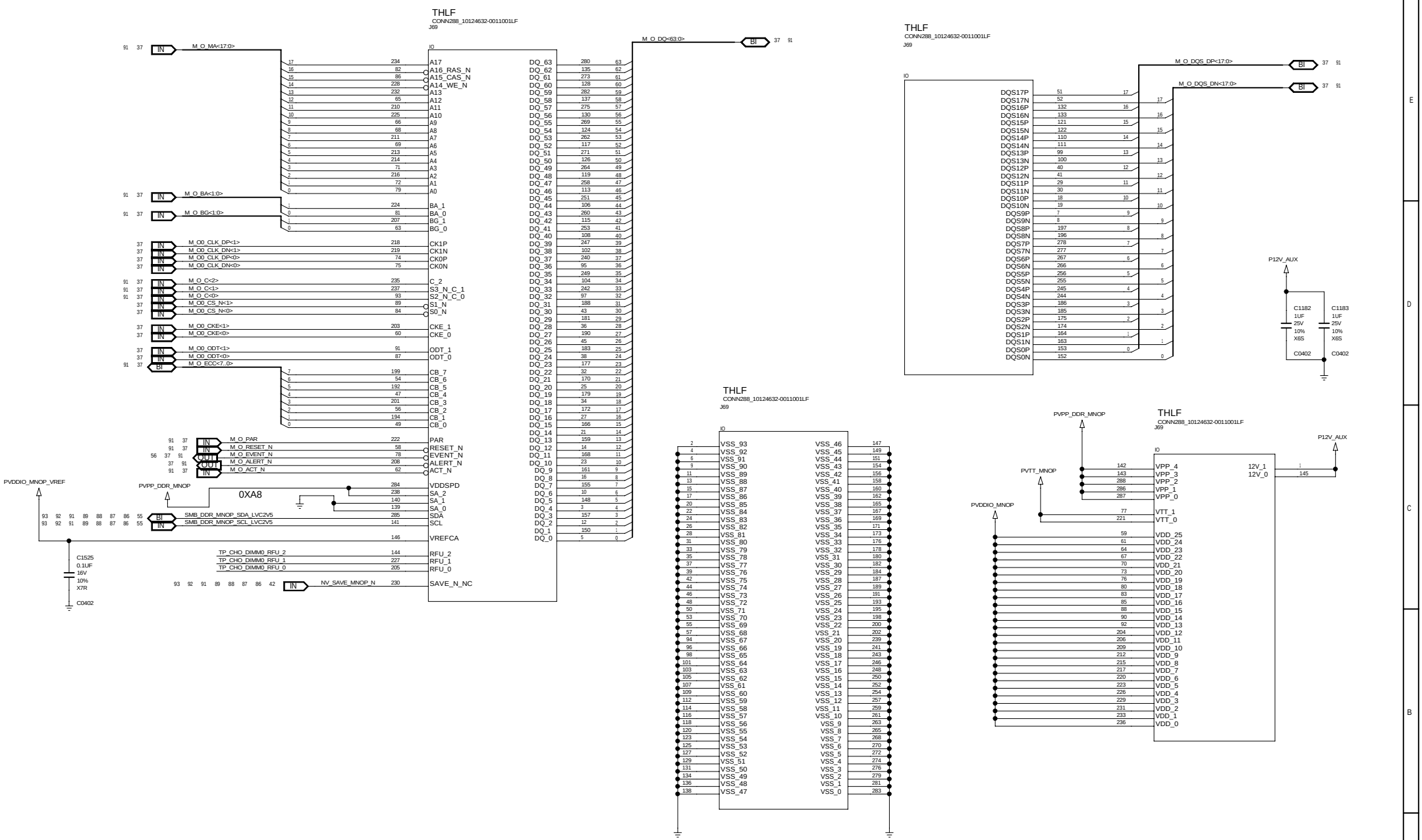
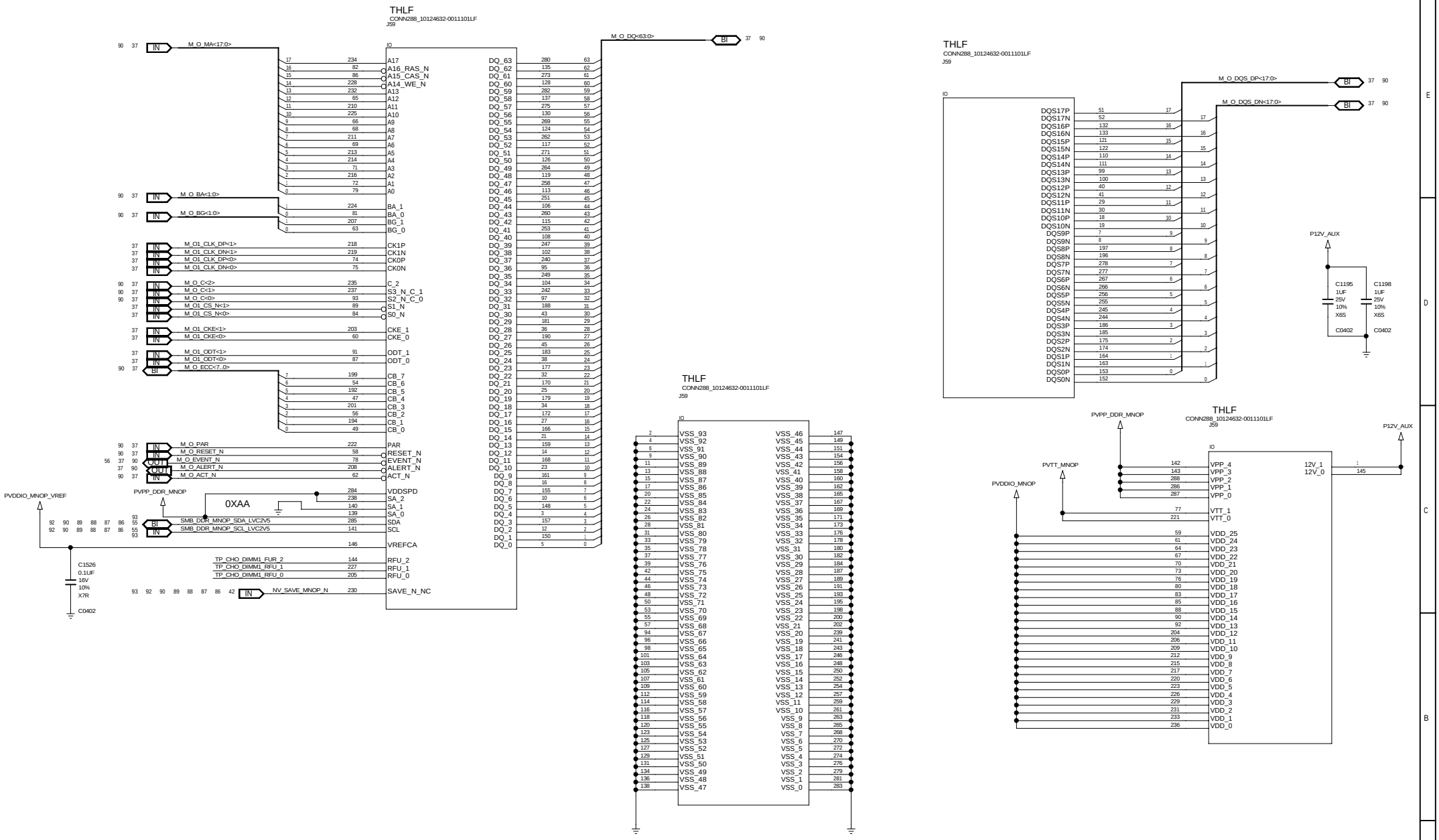
SIZE C DATE Fri Dec 15 20:21:51 2017 SHEET 89 OF 226



CPU1 DDR4 CH_O1(YELLOW)

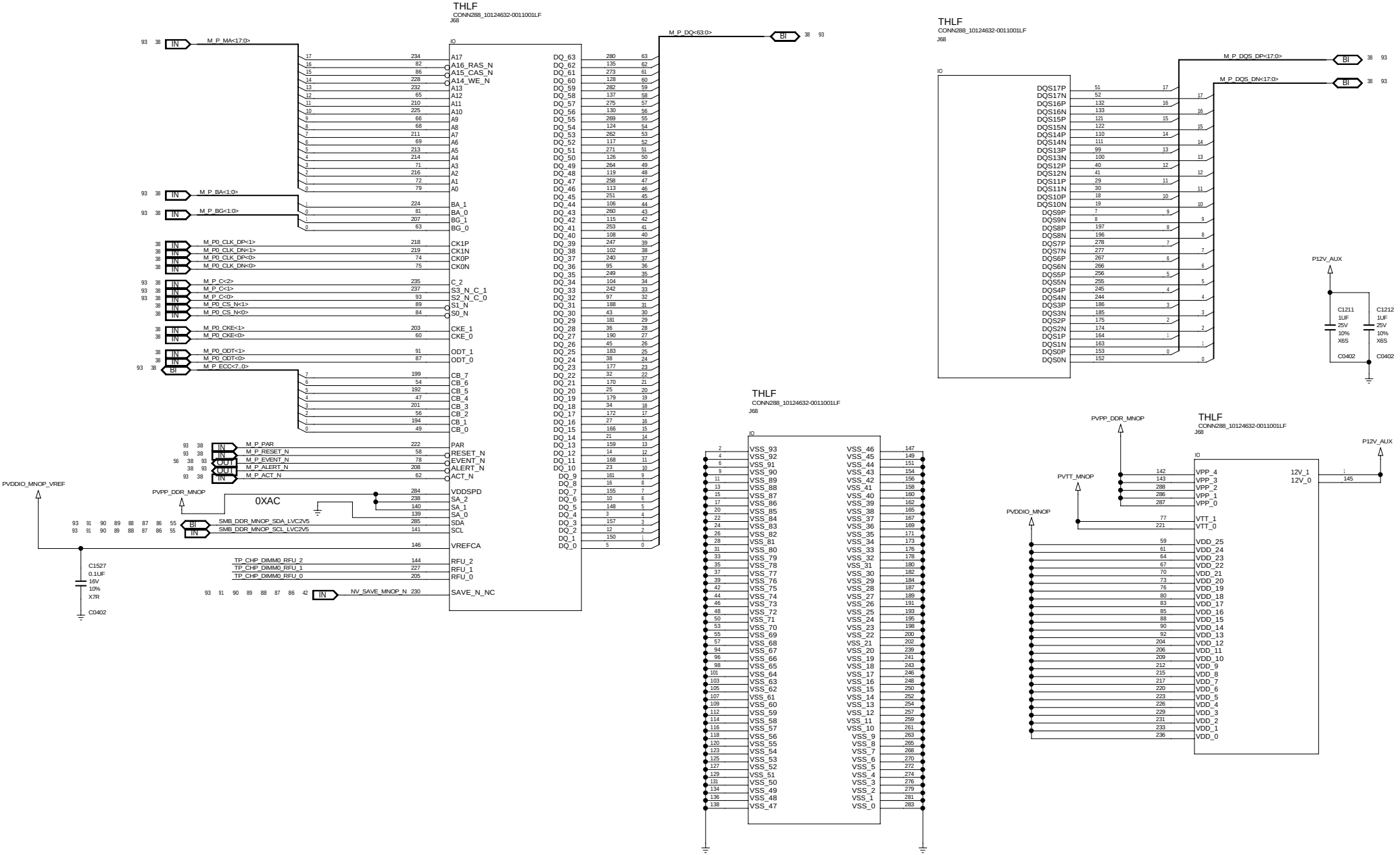
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:51 2017 SHEET 90 OF 226



CPU1 DDR4 CH_O2(BLACK)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:51 2017	SHEET 91 OF 226



CPU1 DDR4 CH P1(YELLOW)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
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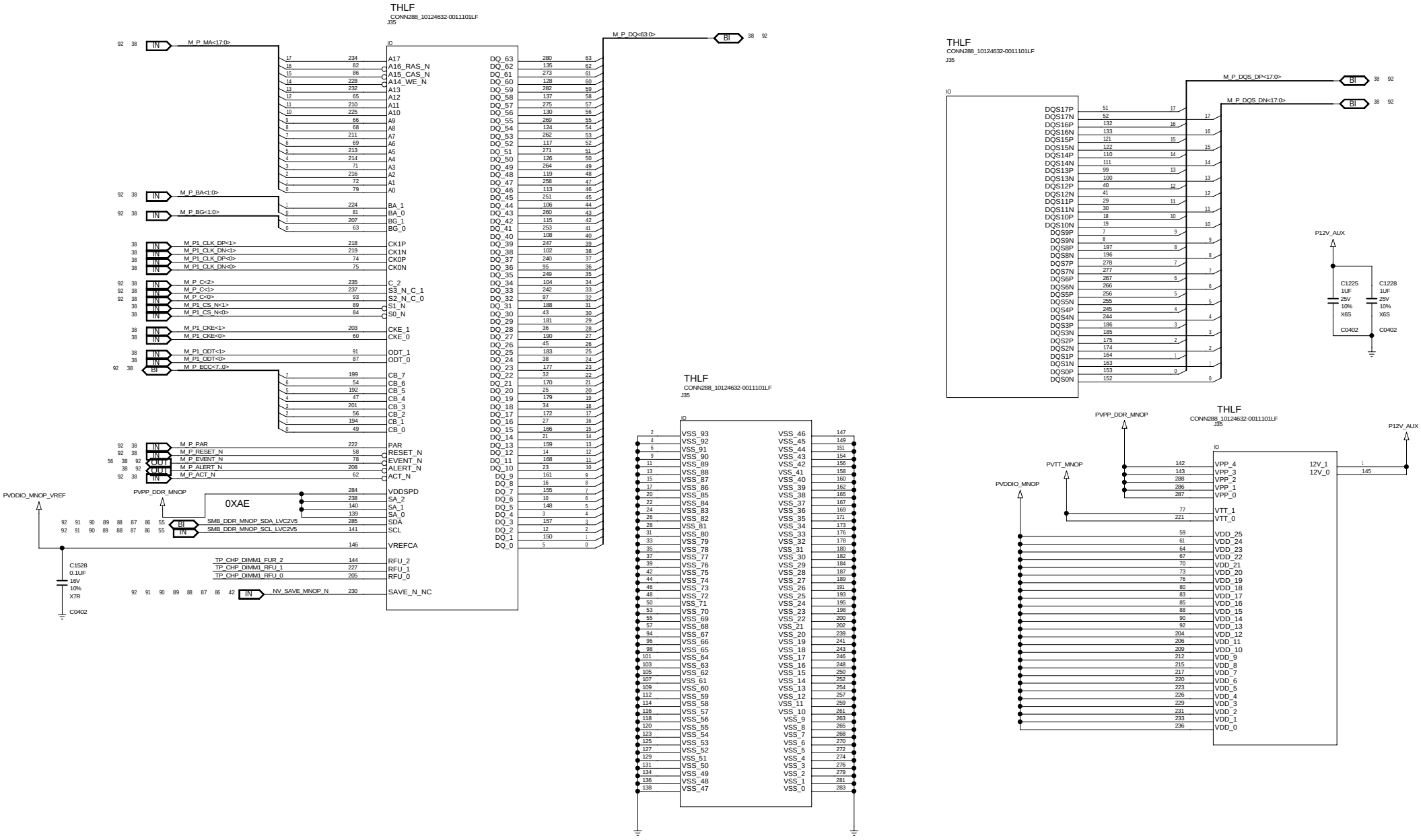
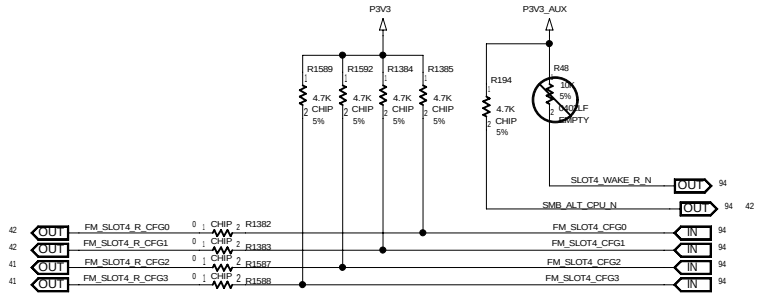
	REVIEWER	SIZE C DATE Fri Dec 15 20:21:52 2017	SHEET 92 OF 226	



CPU1 DDR4 CH_P2(BLACK)

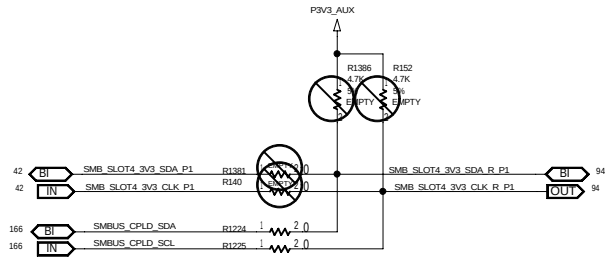
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

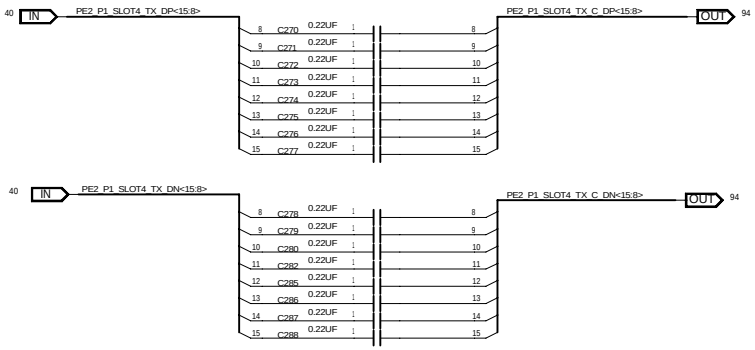
SIZE C DATE Fri Dec 15 20:21:52 2017 SHEET 93 OF 226

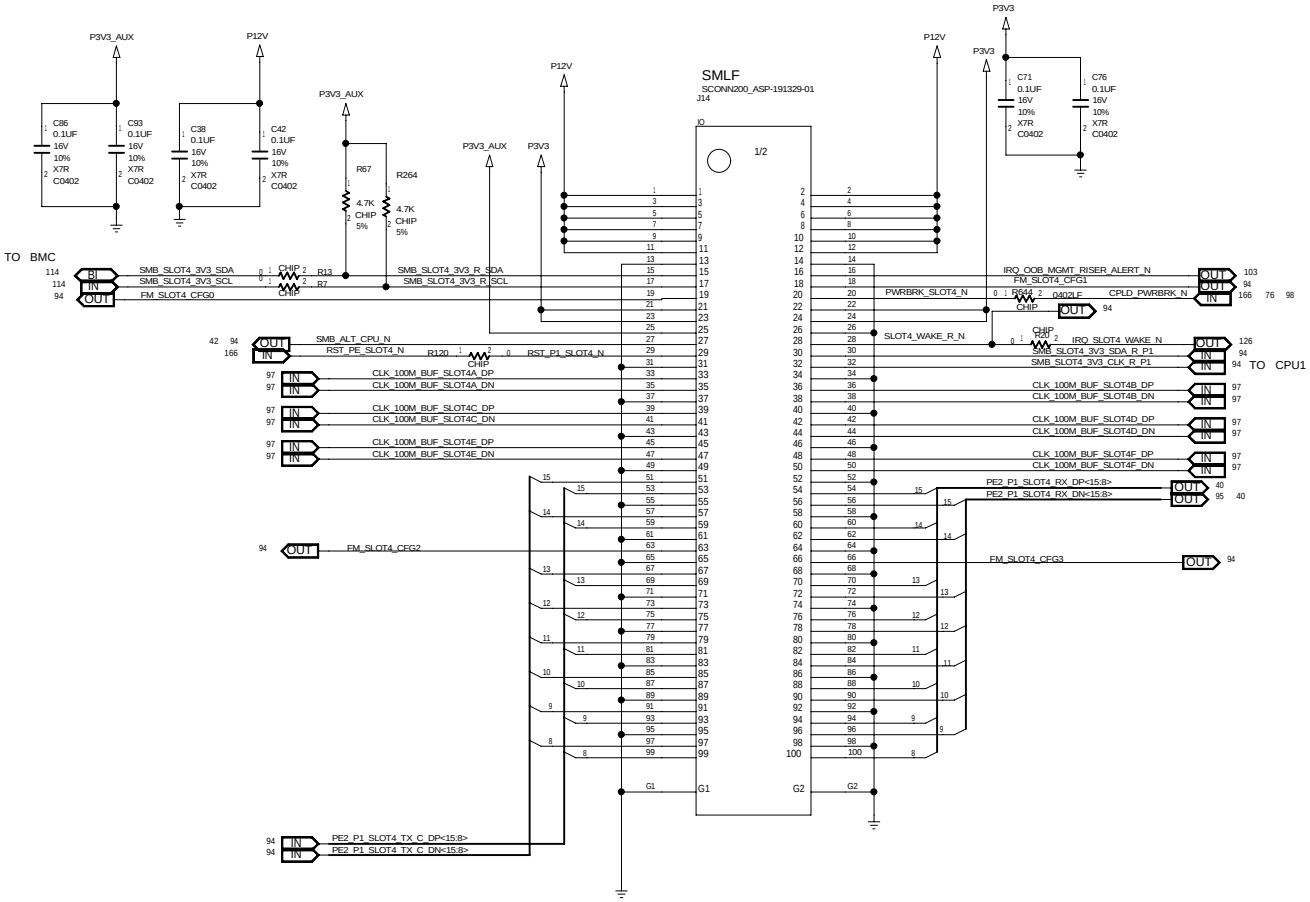


PCIE CONFIG SETTING

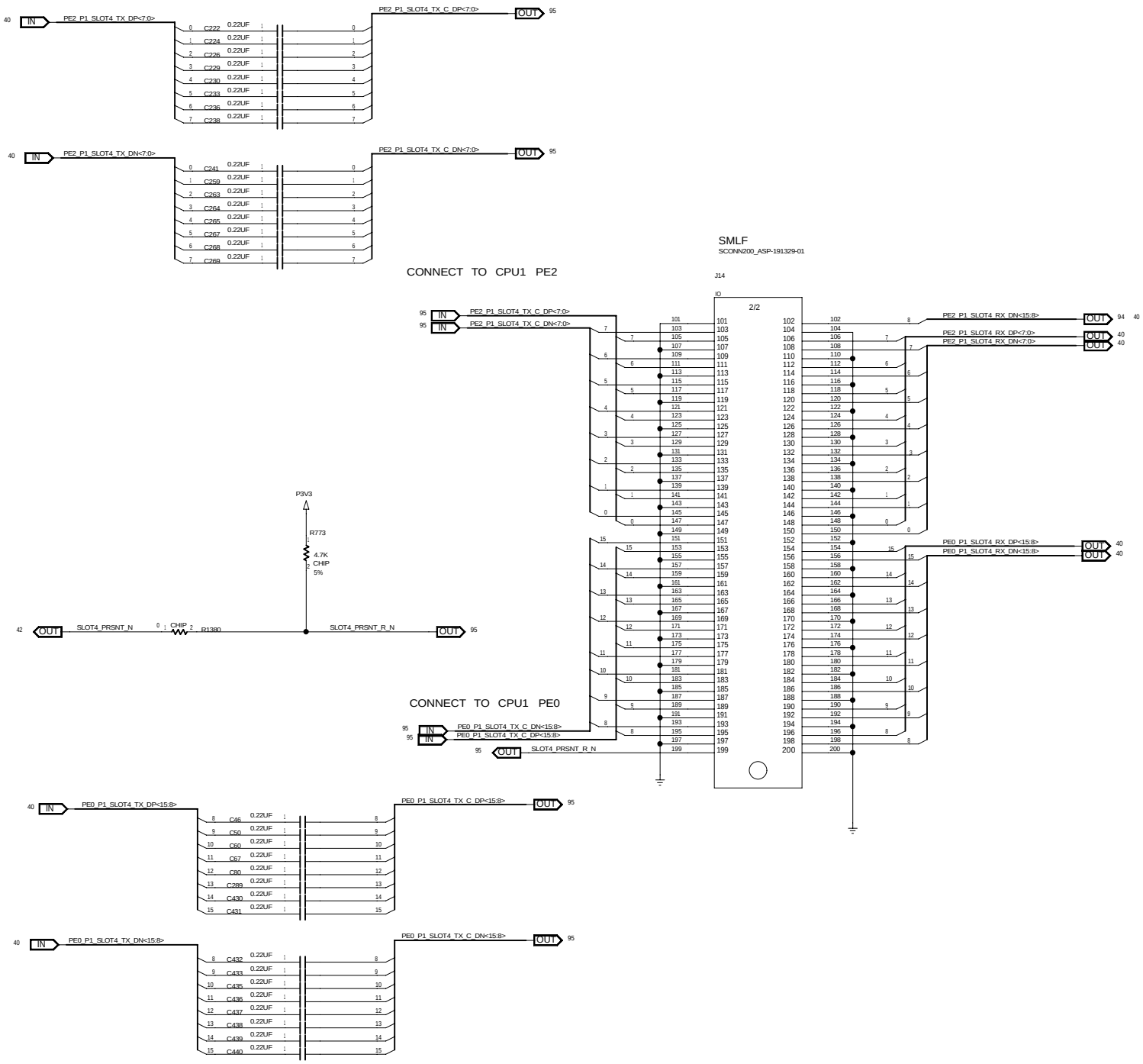
SLOT4_CFG0	SLOT4_CFG1	MB MAPPING TO RISER SLOTS
0	0	SS-2-SLOT PCIE RISER
0	1	SS-2-SLOT PCIE RISER
1	0	DS-2-SLOT PCIE RISER
1	1	RSVD





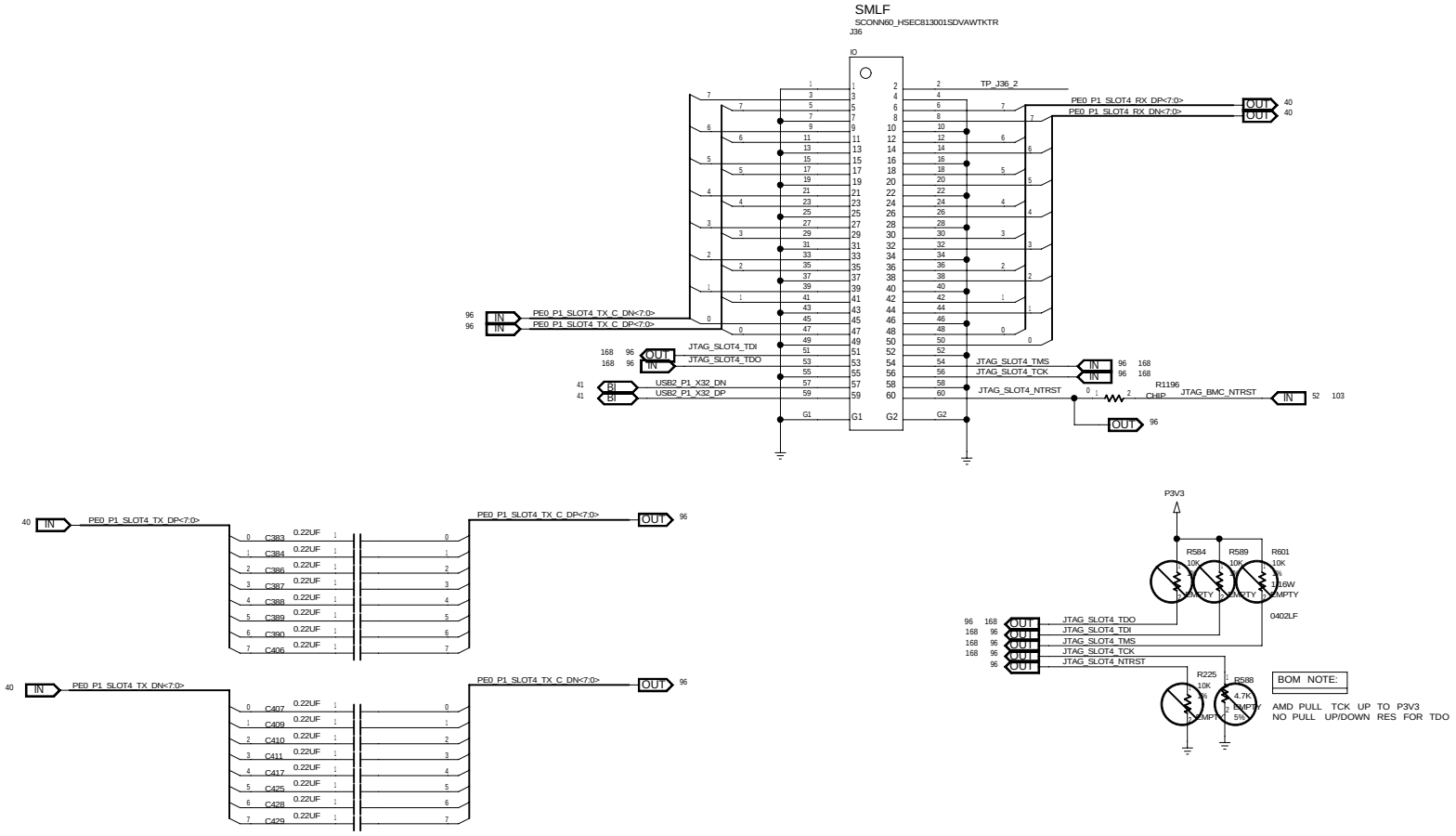


BOM NOTE:
N/A



SLOT4 X32(2 OF 3)

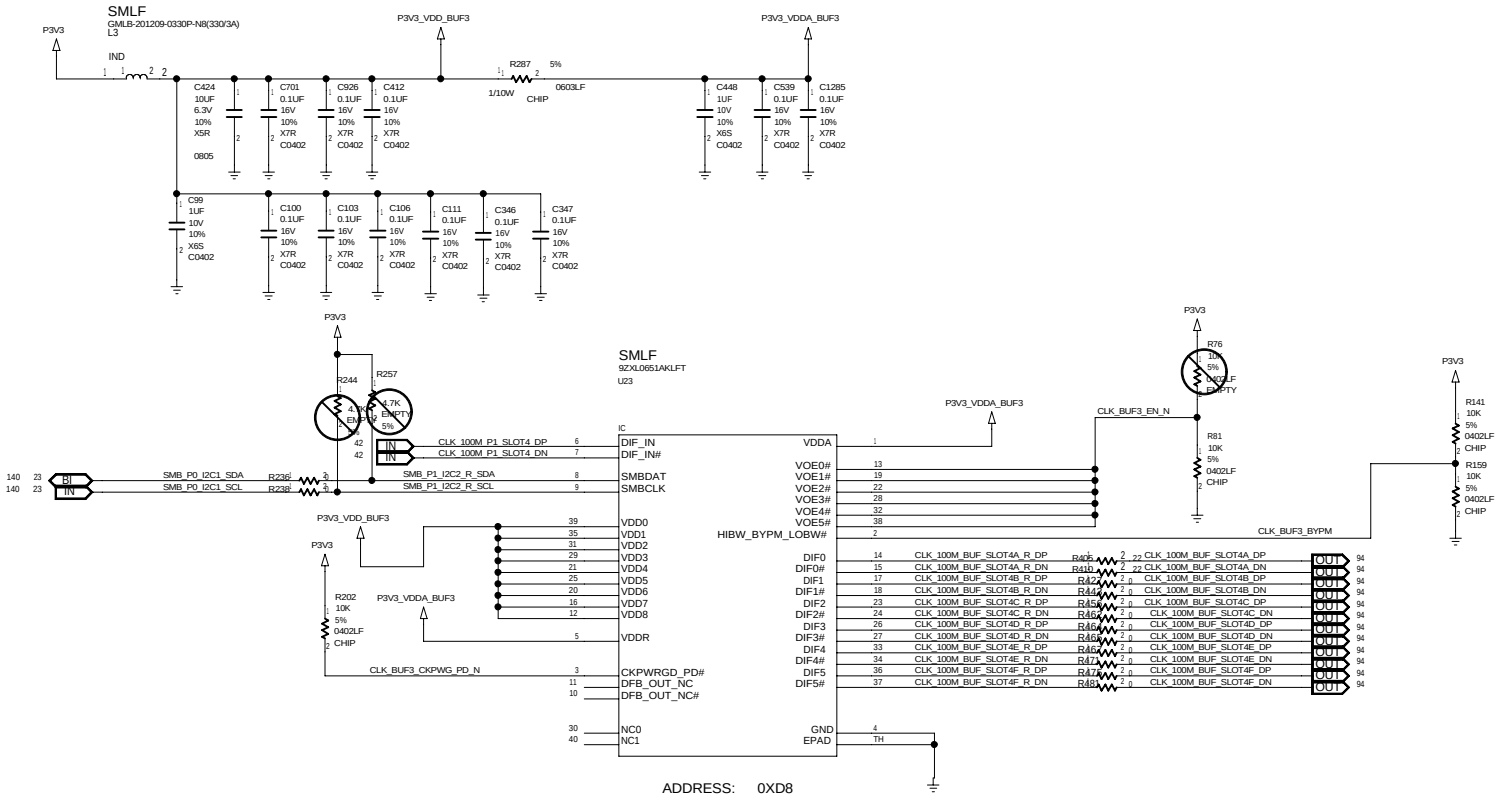
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C DATE Fri Dec 15 20:21:53 2017	SHEET 95 OF 226	



SLOT4 X32(3 OF 3)

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

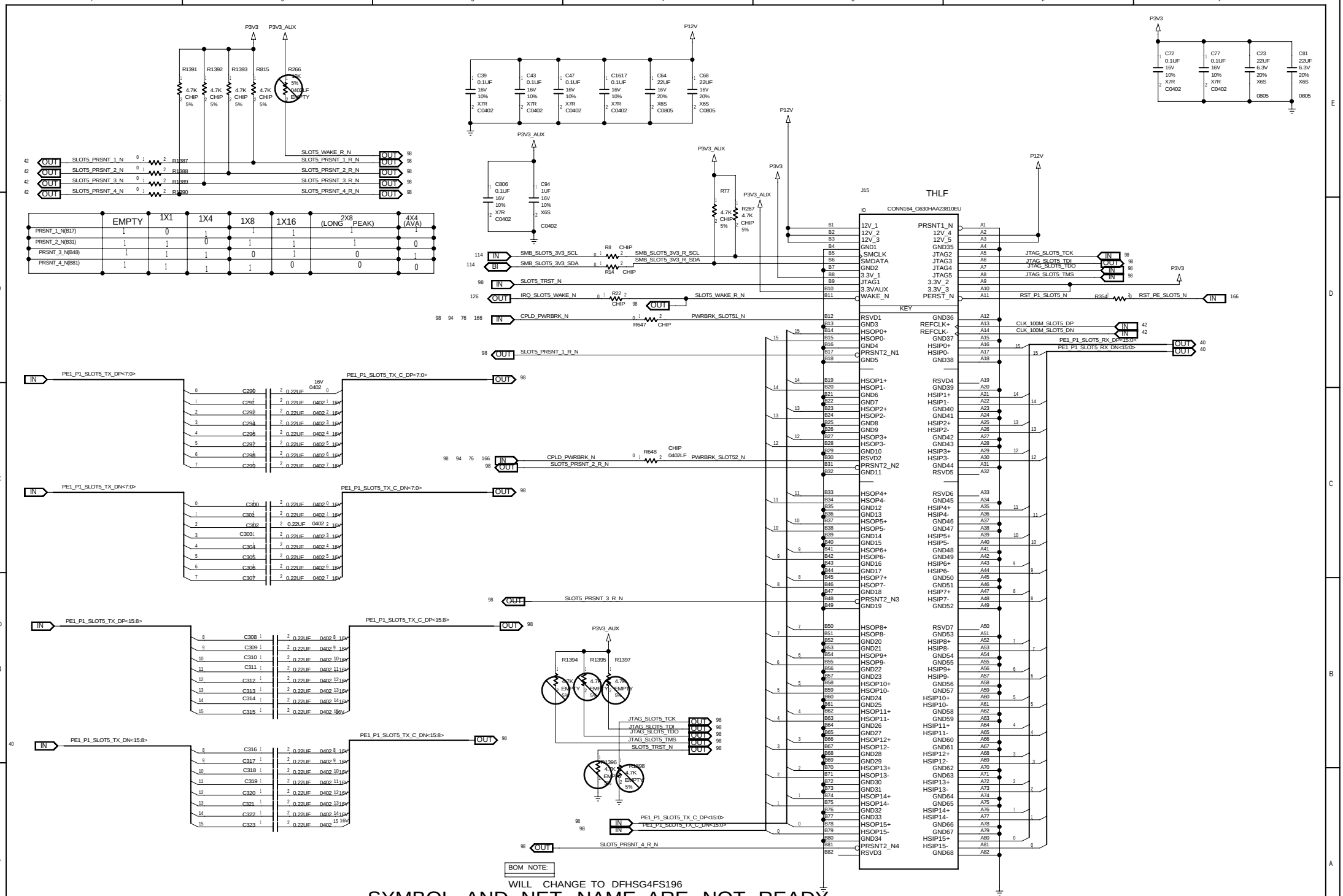
SIZE C DATE Fri Dec 15 20:21:53 2017 SHEET 96 OF 226



ADDRESS: 0XD8

Clock BUFFER For Slot4

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:53 2017	SHEET 97 OF 226



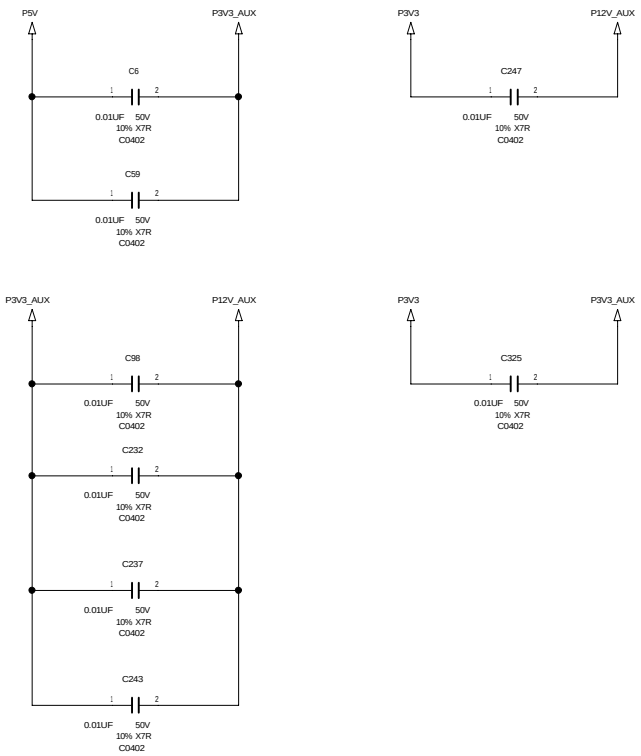
	EMPTY	1X1	1X4	1X8	1X16	2X8 (LONG PEAK)	4X4 (AVA)
PRSNT_1_N(B17)	1	0	1	1	1	1	1
PRSNT_2_N(B31)	1	1	0	1	1	1	0
PRSNT_3_N(B48)	1	1	1	0	1	0	1
PRSNT_4_N(B81)	1	1	1	1	0	0	0

PCIE SLOT 5

Quanta

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:54 2017 SHEET 98 OF 226

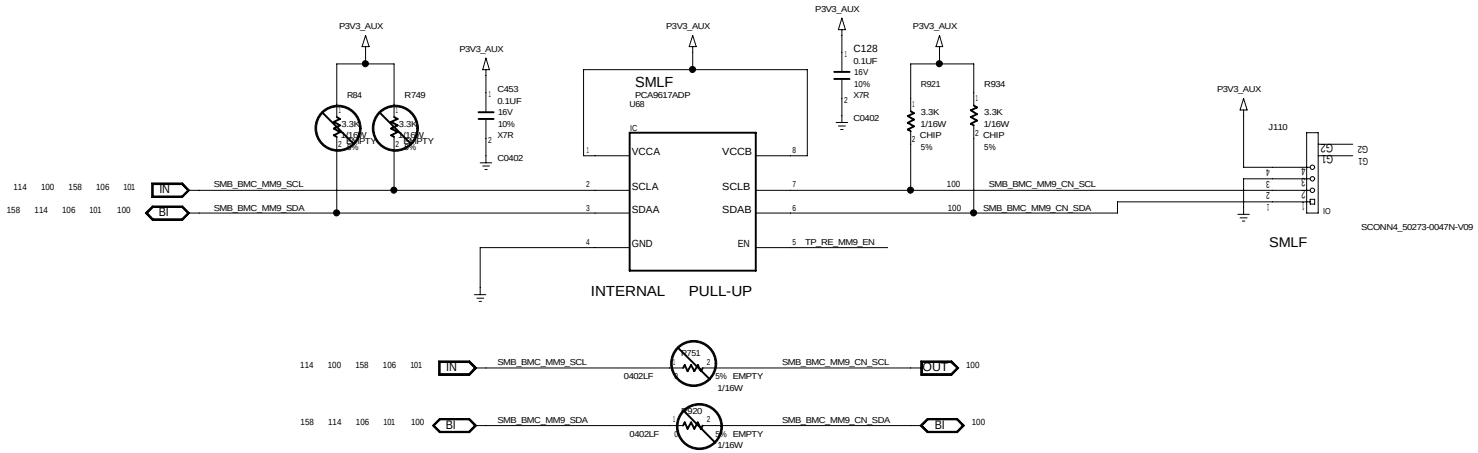


STITCHING CAP

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

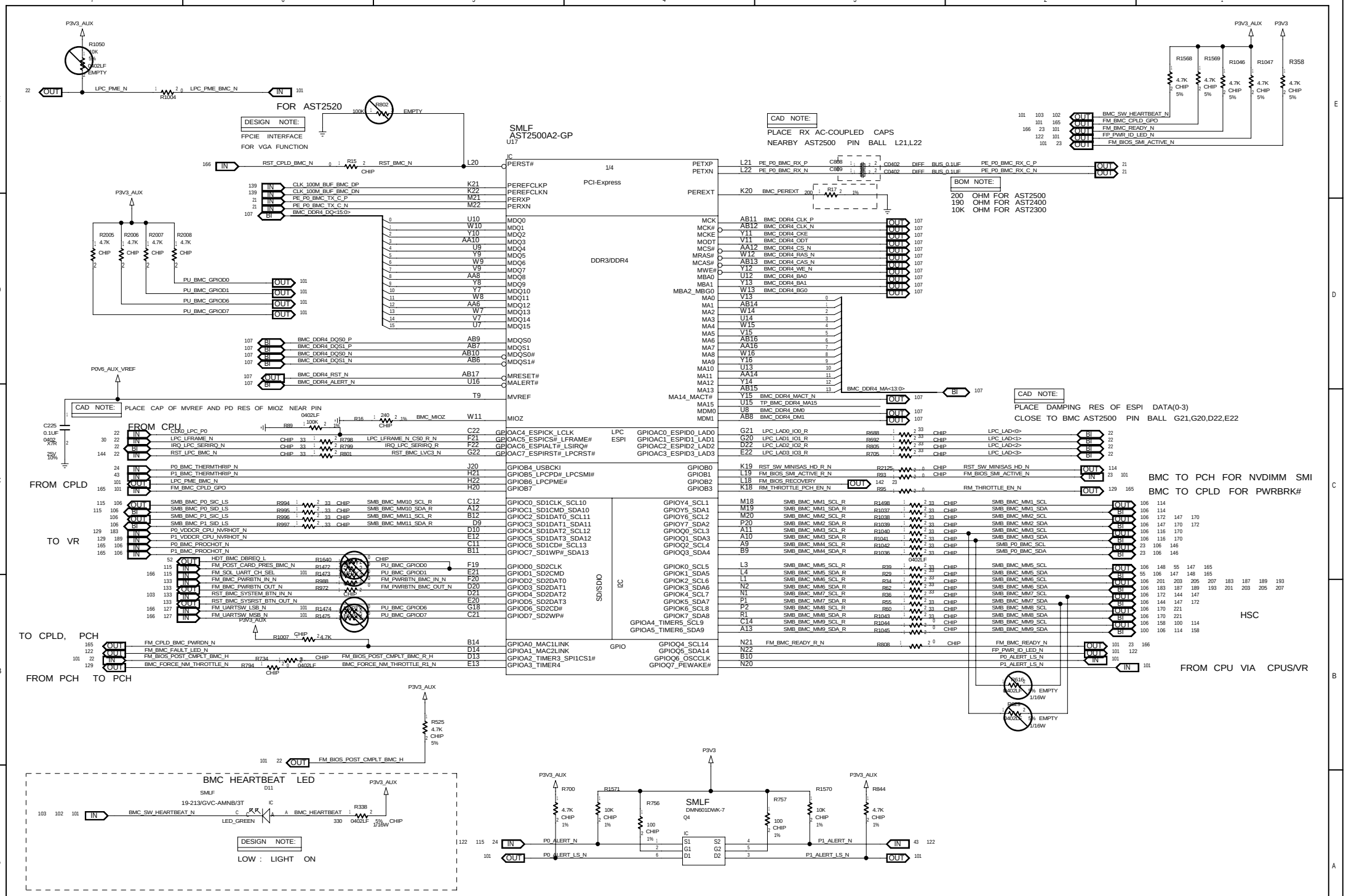
SIZE C DATE Fri Dec 15 20:21:54 2017 SHEET 99 OF 226

I2C REPEATER(FOR ESD)



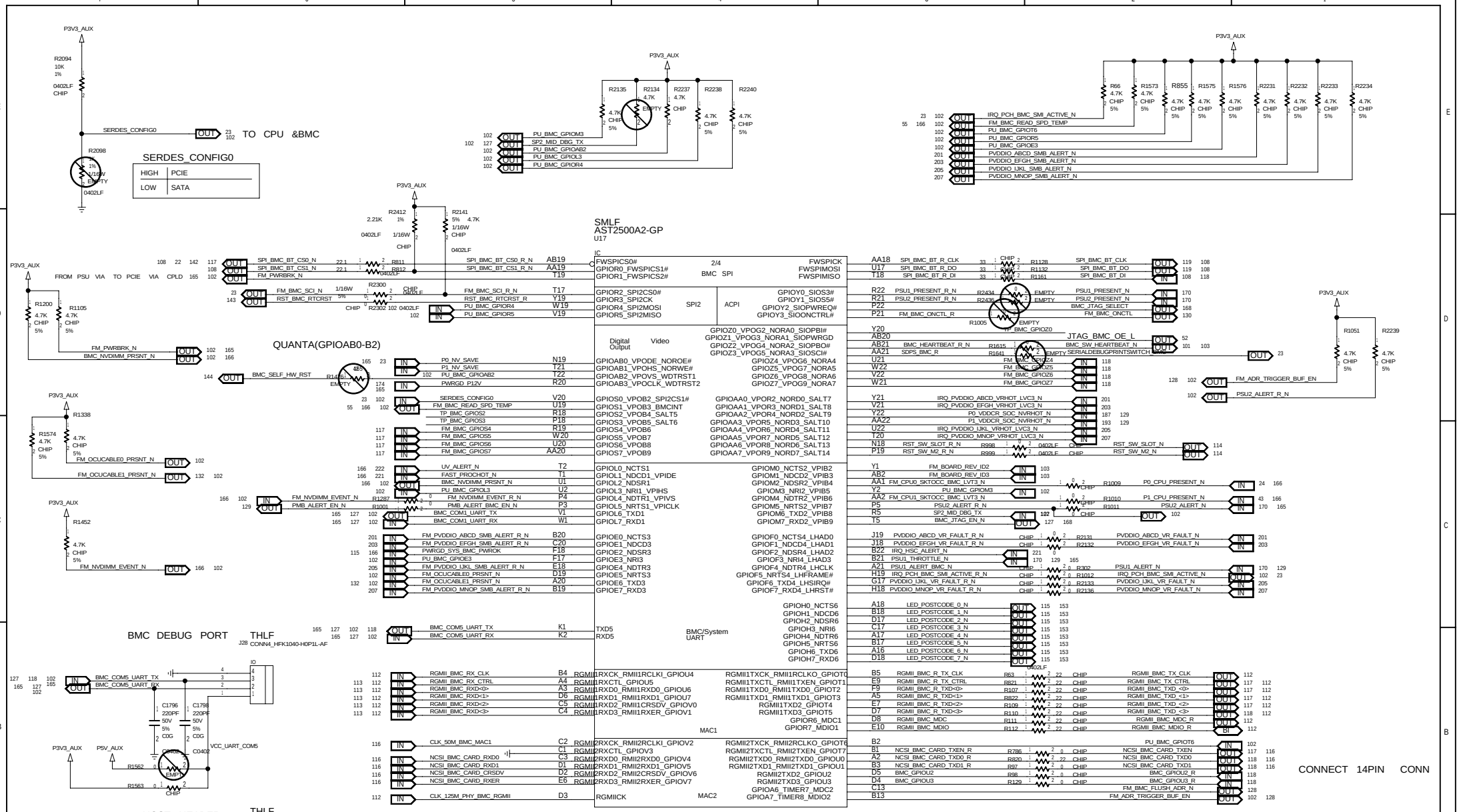
2U I2C EXPANDER

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:54 2017	SHEET 100 OF 226



BMC DDR/I2C/ESP/SD (1 OF 4)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU		<Q_PROJ>	<Q_NUMBER>	<Q_REV>
	REVIEWER	SIZE C DATE Fri Dec 15 20:21:16 2017	SHEET 101 OF 226	



BMC (SPI/UART/MAC) (2 OF 4)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
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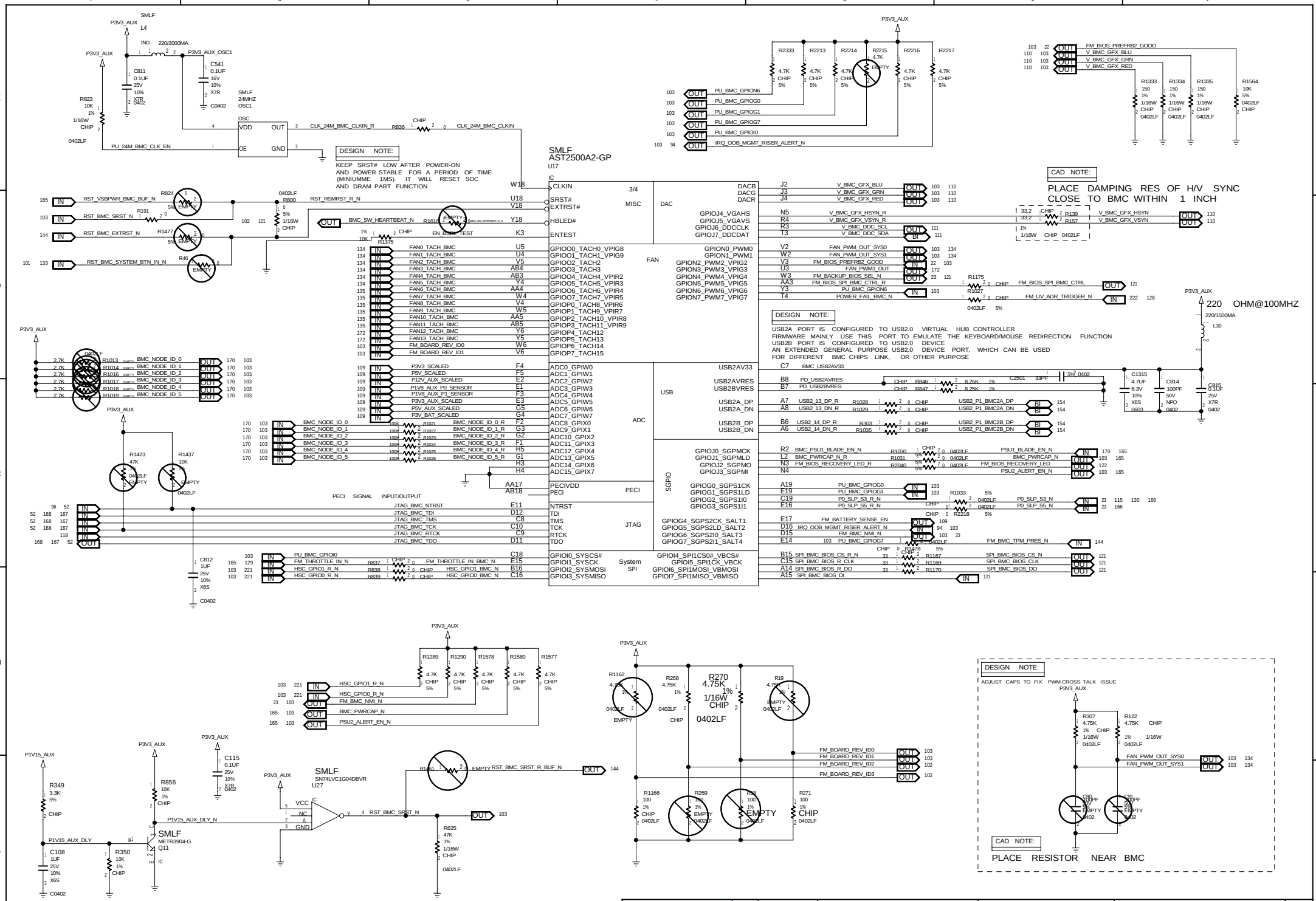
	REVIEWER	SIZE C DATE Fri Dec 15 20:21:54 2017	SHEET 102 OF 226	



BMC (VGA/FAN/ADC/SGPIO/JTAG)(3 OF 4)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
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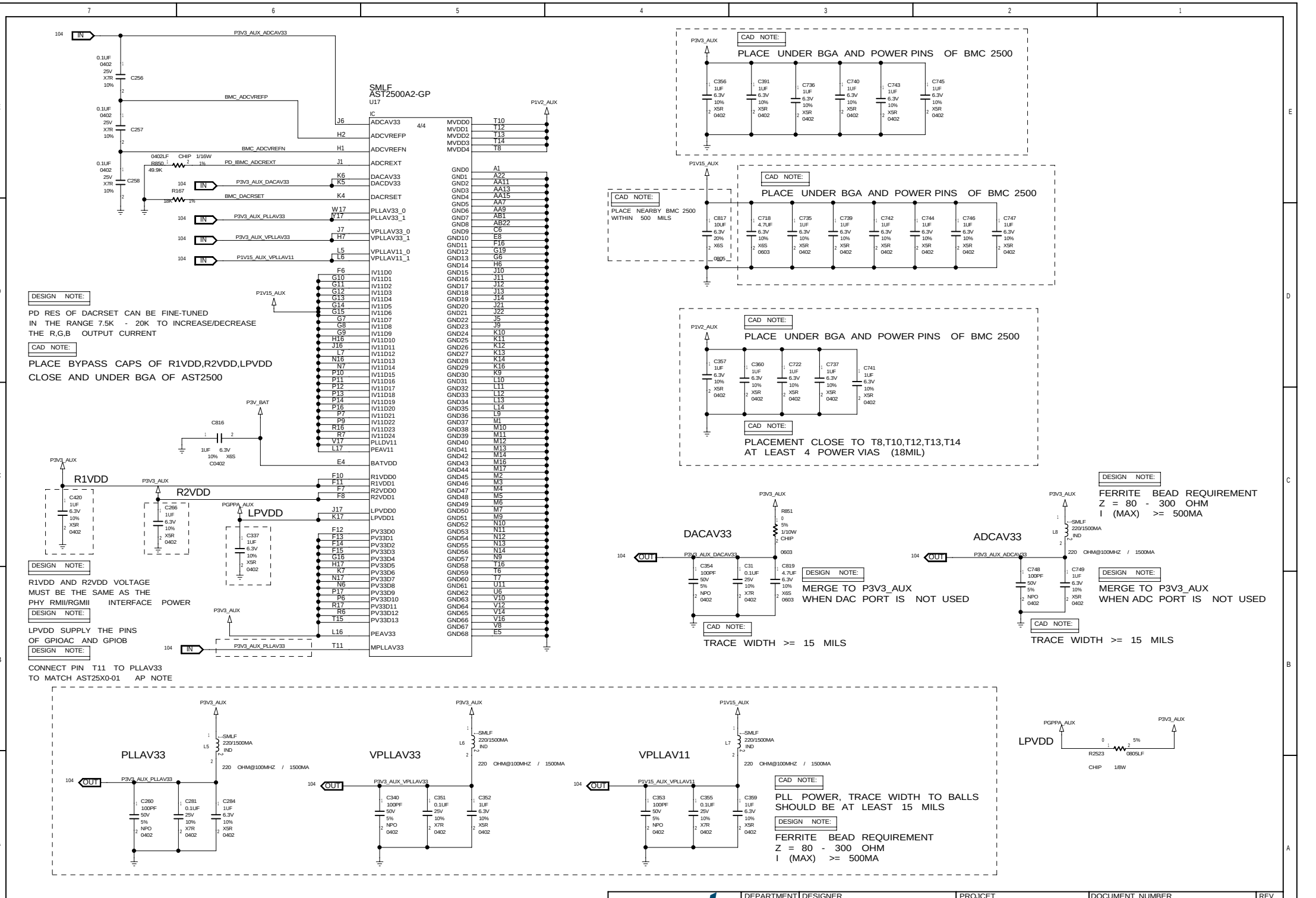
	REVIEWER	SIZE C DATE Fri Dec 15 20:21:19 2017	SHEET 103 OF 226	



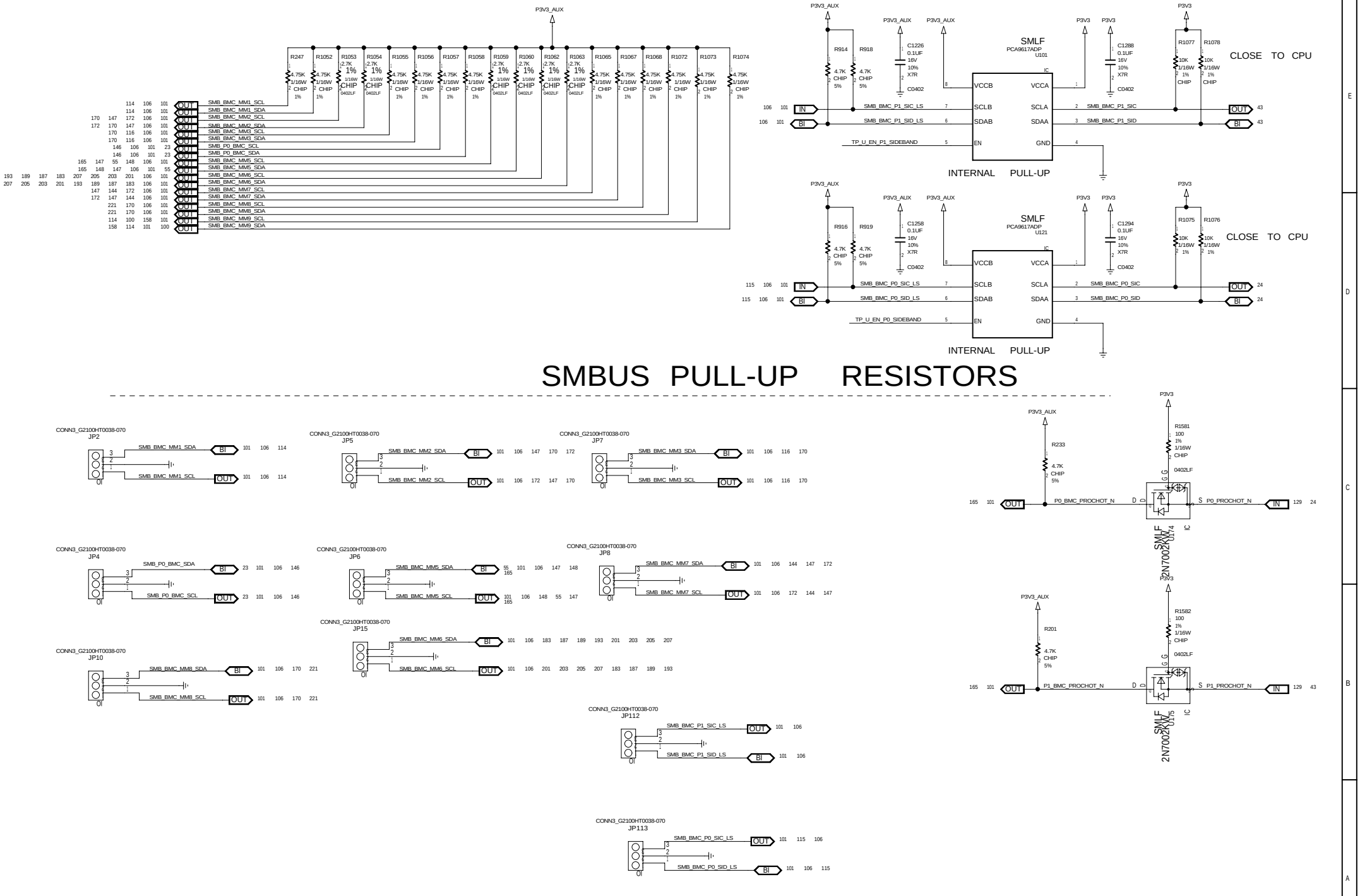
BMC POWER (4 OF 4)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:55 2017 SHEET 104 OF 226

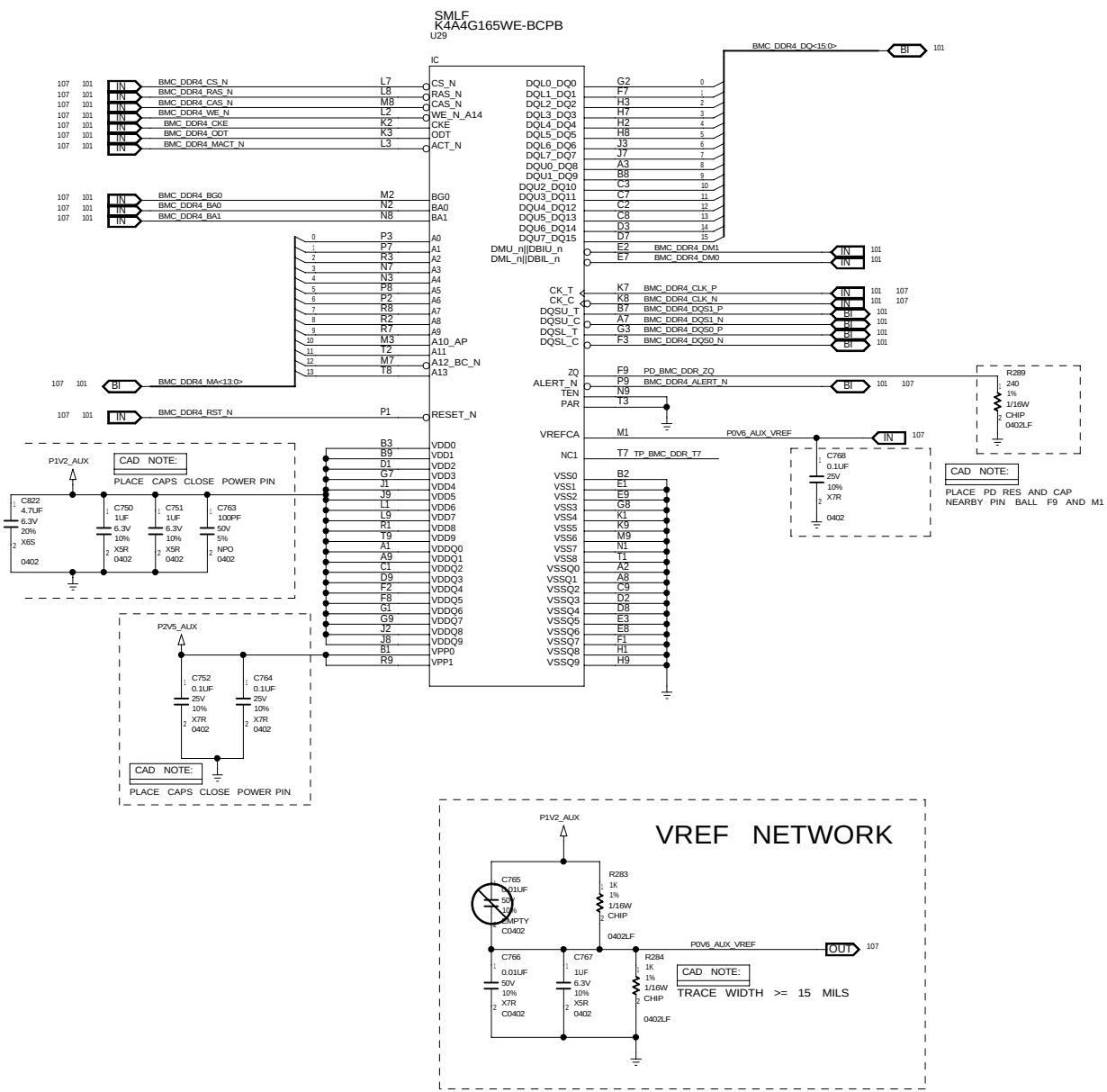
BLANK

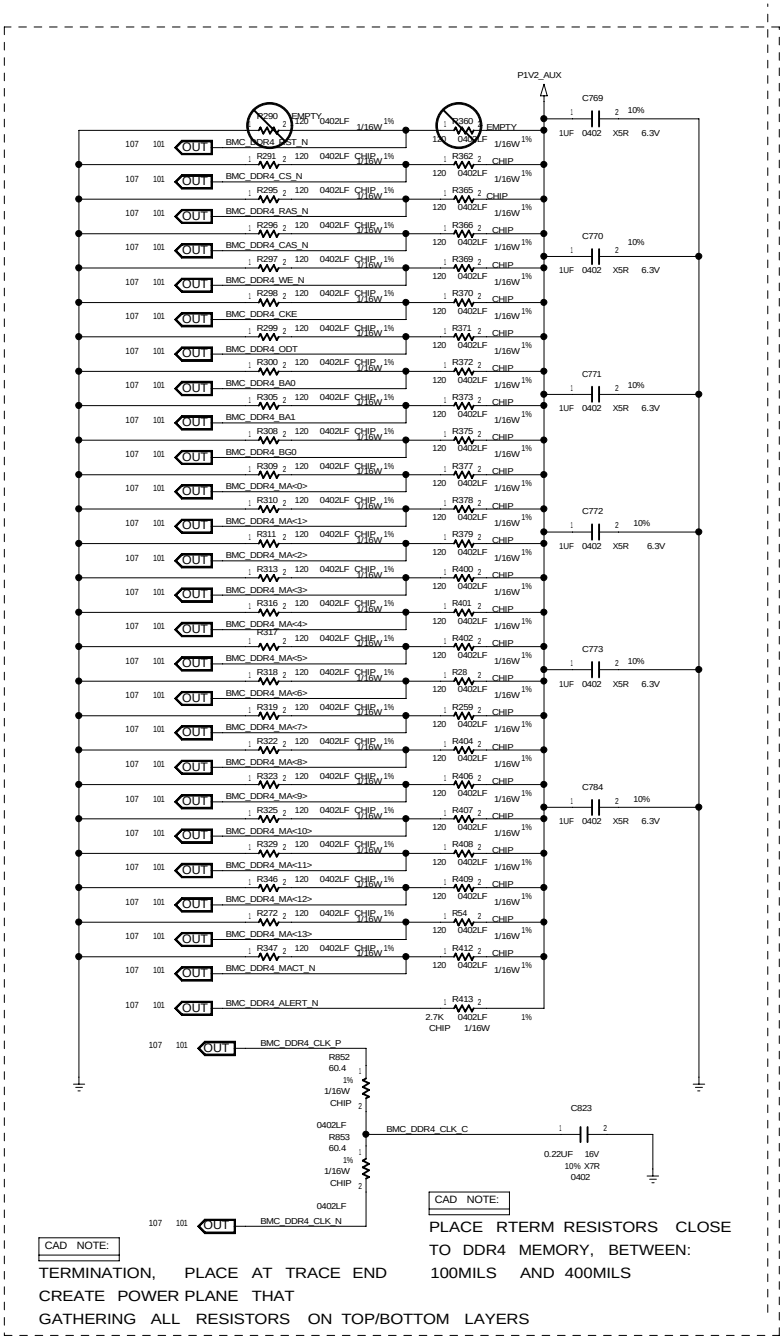
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:34:03 2017	SHEET 105 OF 226



SMBus PULL UP/DOWN RES & Debug CONN

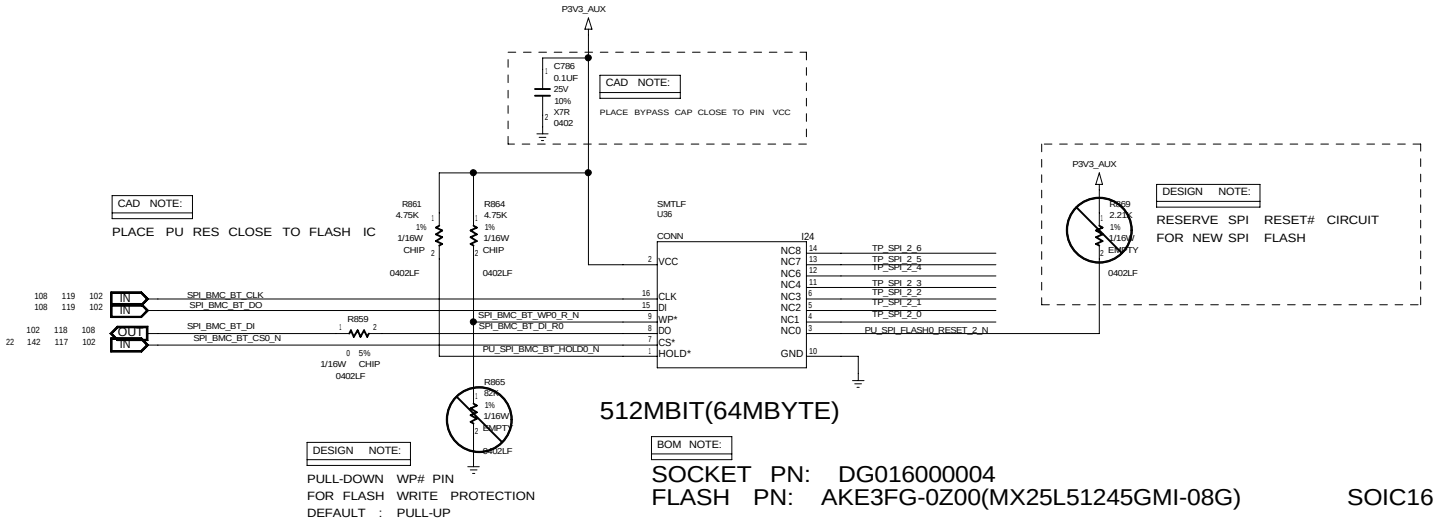
Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:21 2017	SHEET 106 OF 226

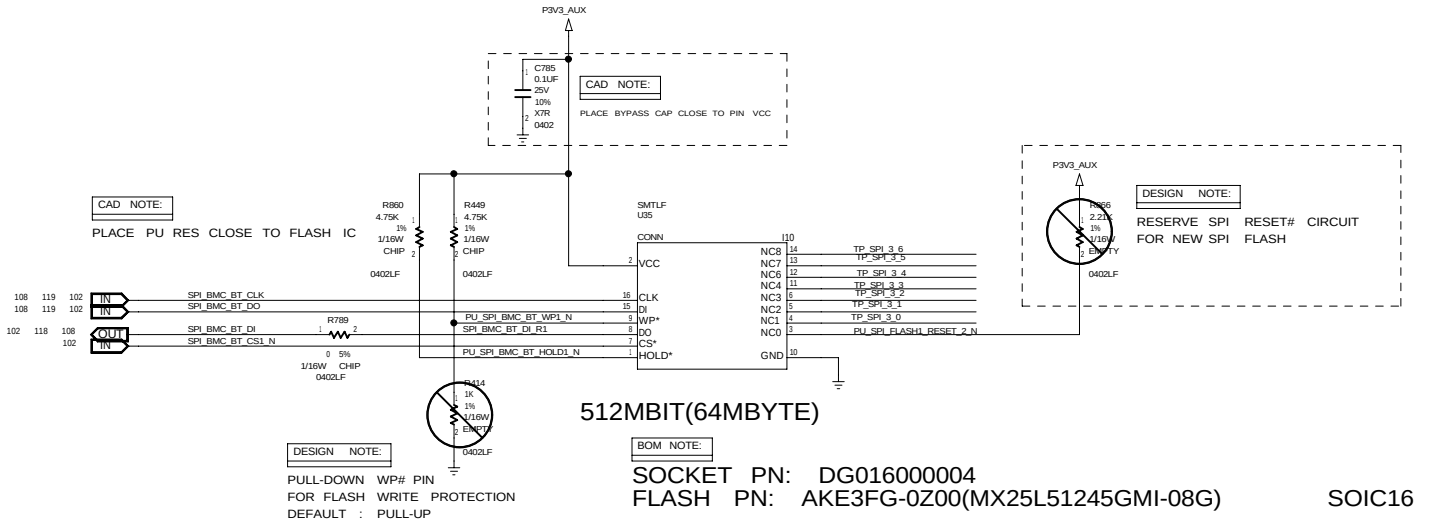




BMC DDR4 SDRAM

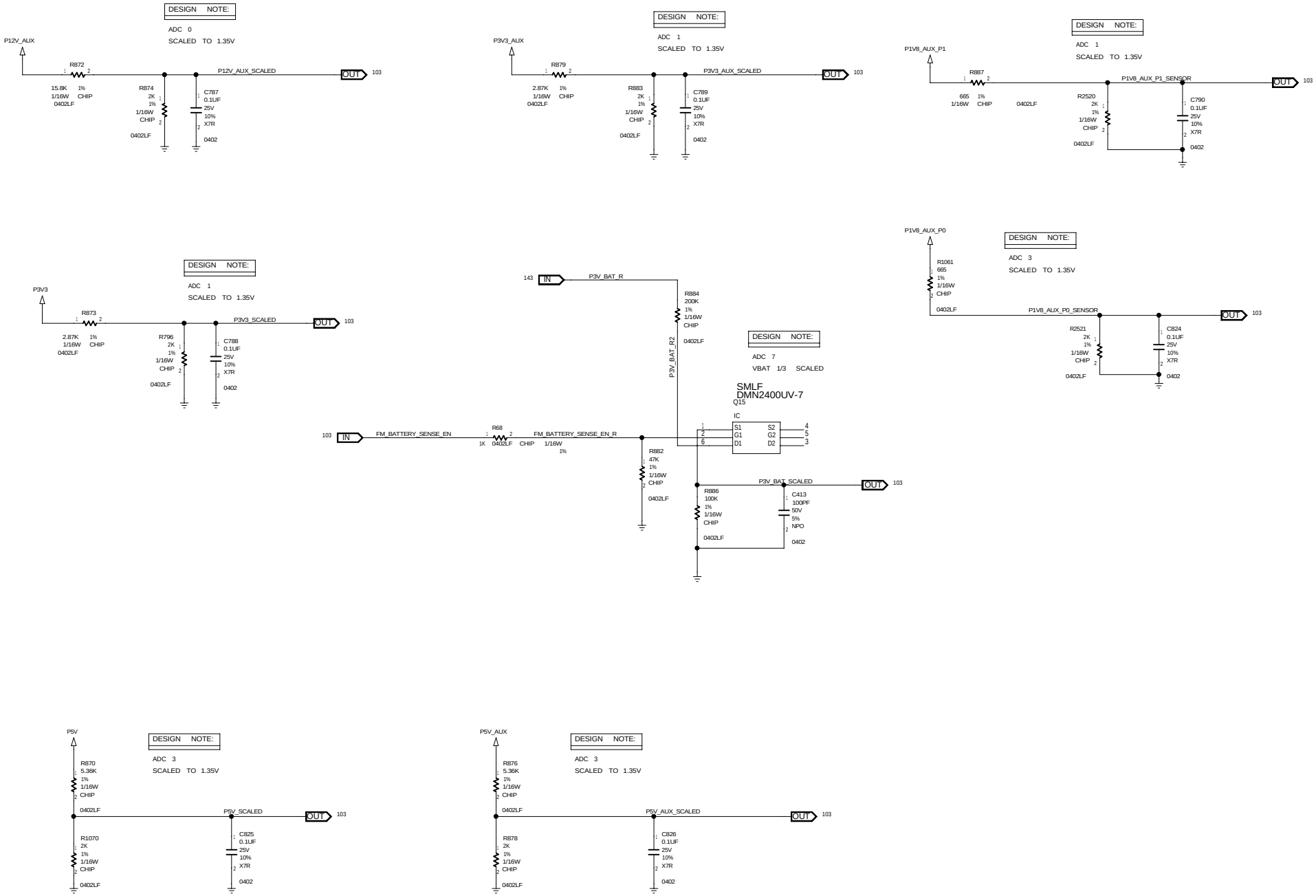
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>
		REVIEWER	
DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C	DATE Fri Dec 15 20:21:55 2017
SHEET 107 OF 226			





BMC BOOT FLASH(DUAL)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:55 2017	SHEET 108 OF 226



CAD NOTE:

ROUTE ALL ADC NETS AT 6 MILS WIDE

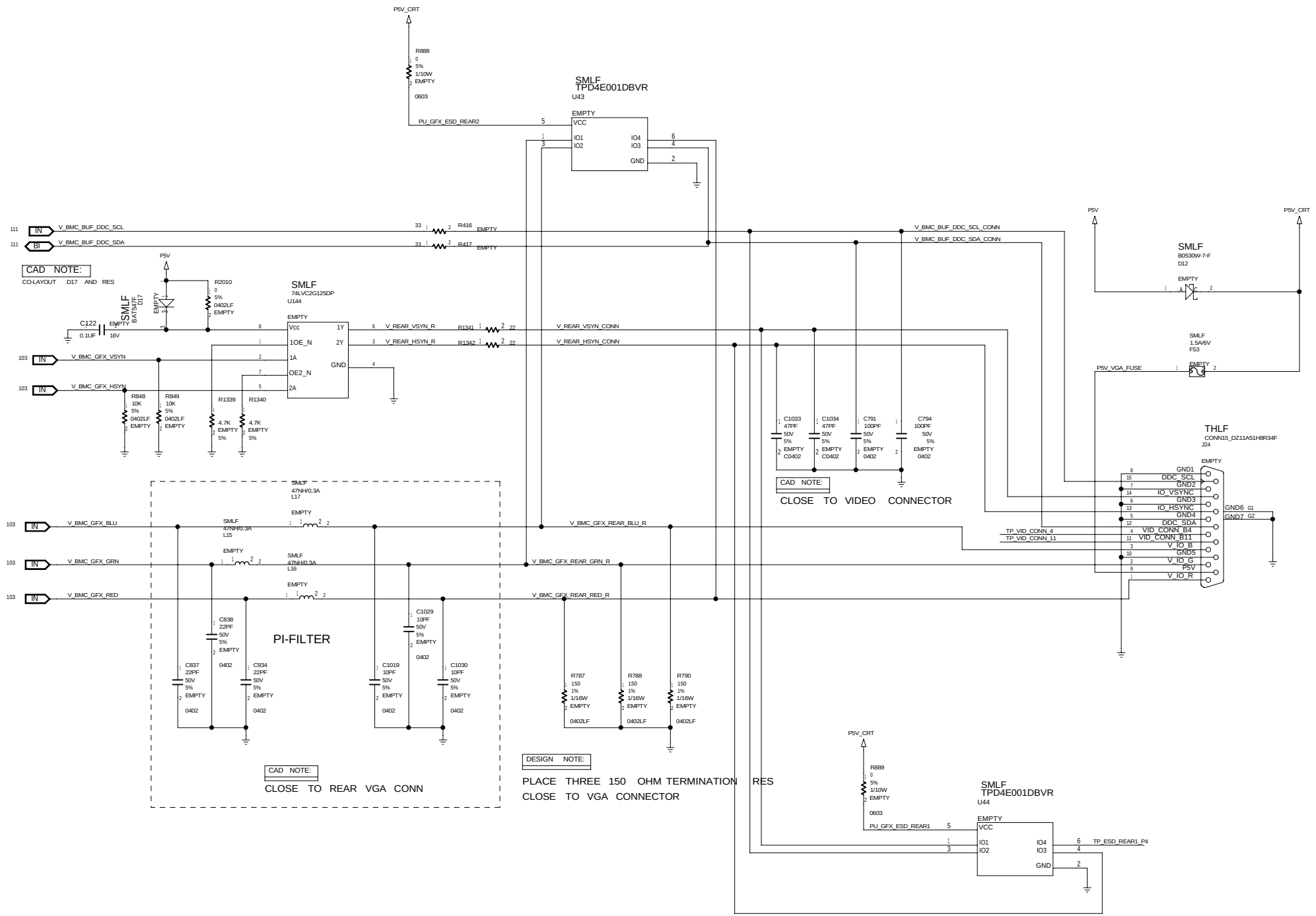
DESIGN NOTE:

ADC INPUT VOLTAGE RANGE : 0-1.8V

A GOOD NOMINAL INPUT VOLTAGE OF 3/4 VIN_MAX = 1.35V

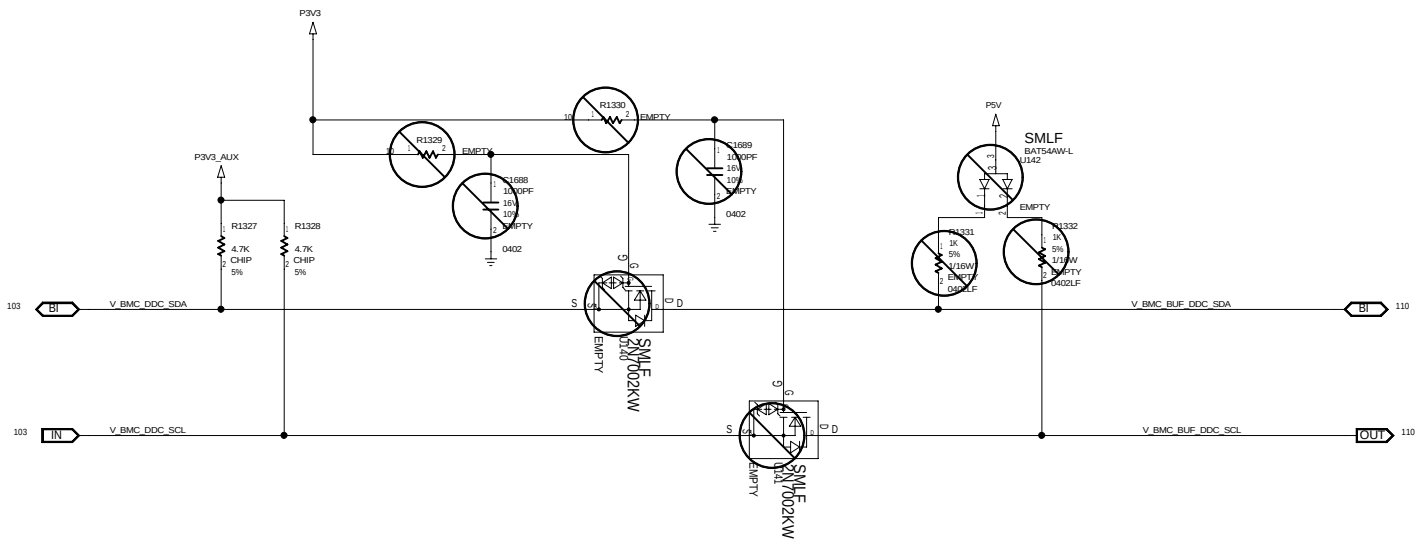
BMC VOTAGE SENSOR

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:55 2017	SHEET 109 OF 226



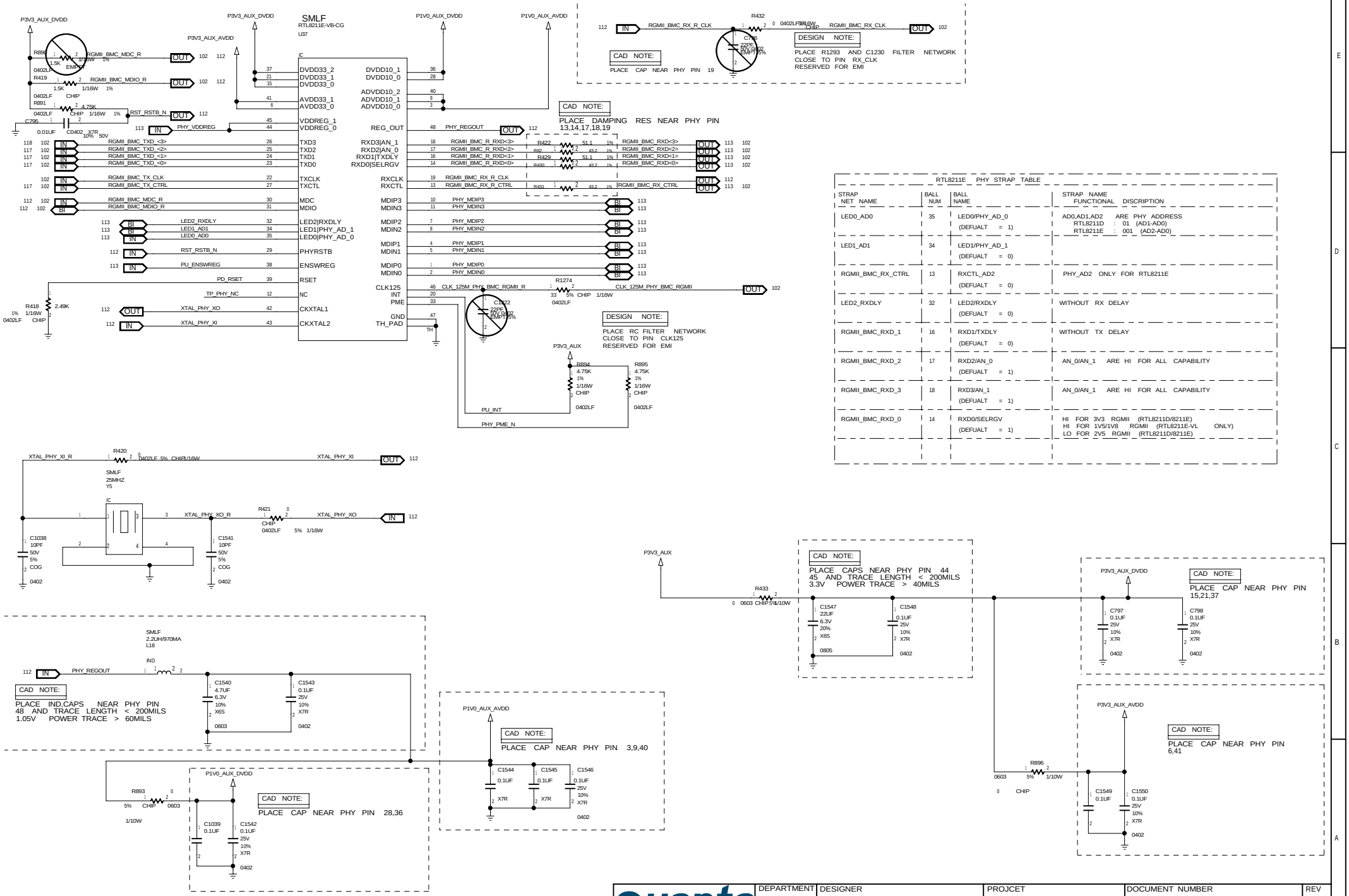
BMC VGA CONN

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:16 2017	SHEET 110 OF 226



BMC DDC SMBUS ISOLATORS

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER		REV: <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:16 2017
			SHEET 111 OF 226	



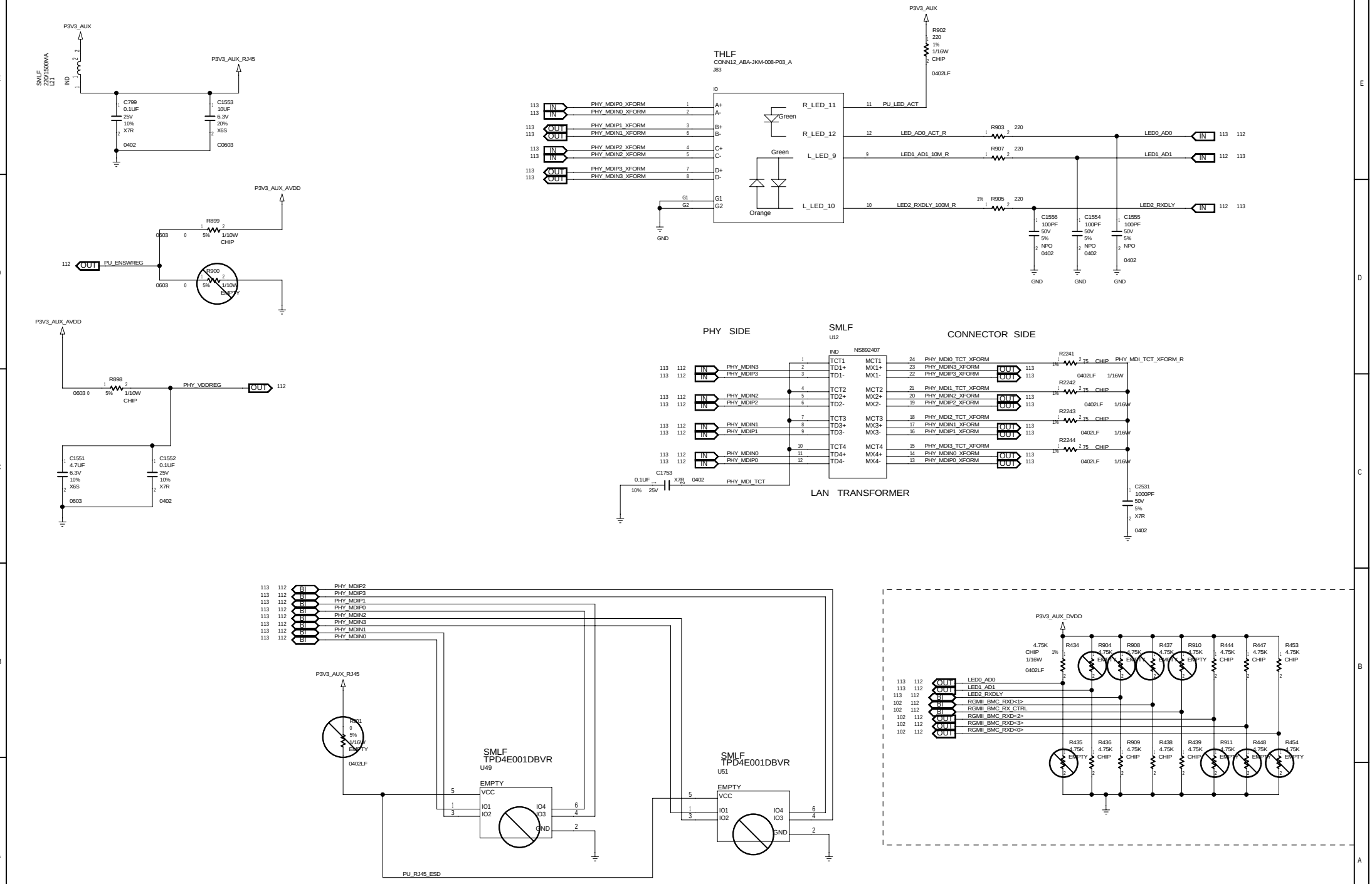
RTL8211E PHY STRAP TABLE

STRAP NET NAME	BALL NUM	BALL NAME	STRAP NAME FUNCTIONAL DISCRIPTION
LED0_AD0	35	LED0/PHY_AD_0 (DEFUALT = 1)	AD0,AD1,AD2 ARE PHY ADDRESS RTL8211D : 01 (AD1-AD0) RTL8211E : 001 (AD2-AD0)
LED1_AD1	34	LED1/PHY_AD_1 (DEFUALT = 0)	
RGMII_BMC_RX_CTRL	13	RXCTL_AD2 (DEFUALT = 0)	PHY_AD2 ONLY FOR RTL8211E
LED2_RXDLY	32	LED2/RXDLY (DEFUALT = 0)	WITHOUT RX DELAY
RGMII_BMC_RXD_1	16	RXD1/TXDLY (DEFUALT = 0)	WITHOUT TX DELAY
RGMII_BMC_RXD_2	17	RXD2/AN_0 (DEFUALT = 1)	AN_0/AN_1 ARE HI FOR ALL CAPABILITY
RGMII_BMC_RXD_3	18	RXD3/AN_1 (DEFUALT = 1)	AN_0/AN_1 ARE HI FOR ALL CAPABILITY
RGMII_BMC_RXD_0	14	RXD0/SELRGV (DEFUALT = 1)	HI FOR 3V3 RGMII (RTL8211D/8211E) HI FOR 1V5/1V8 RGMII (RTL8211E-VL ONLY) LO FOR 2V5 RGMII (RTL8211D/8211E)

BMC 1GB PHY (1 OF 2)

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:56 2017 SHEET 112 OF 226



BMC 1GB PHY (2 OF 2)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
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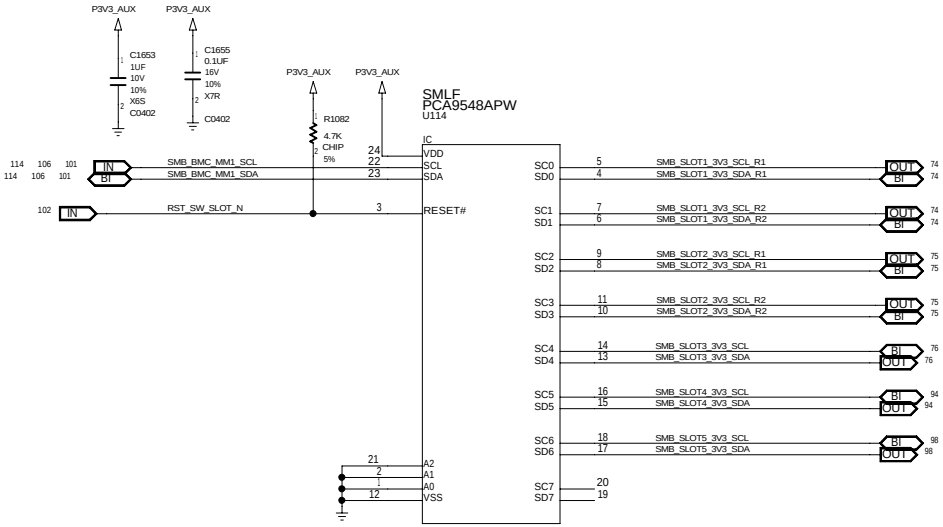

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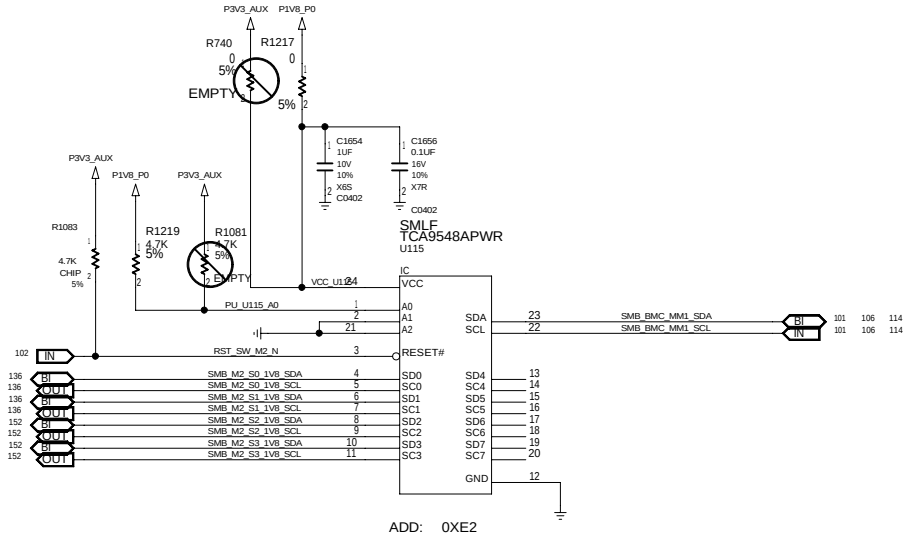

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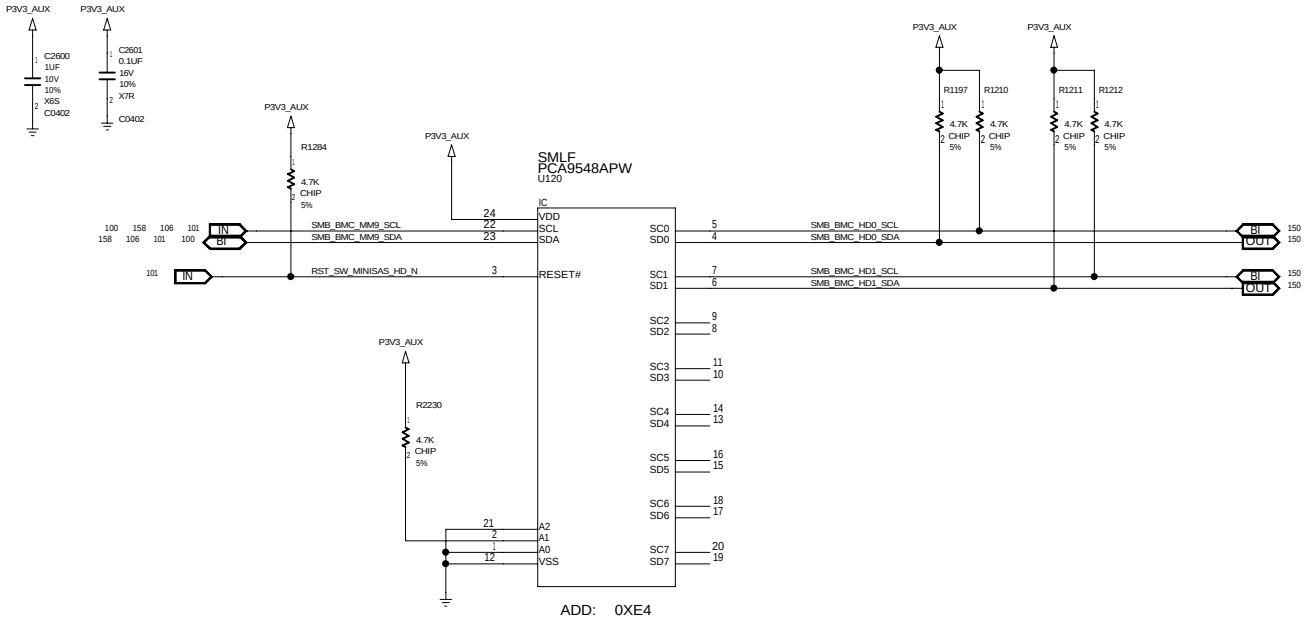

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SMBUS SWITCH FOR PCIe slots

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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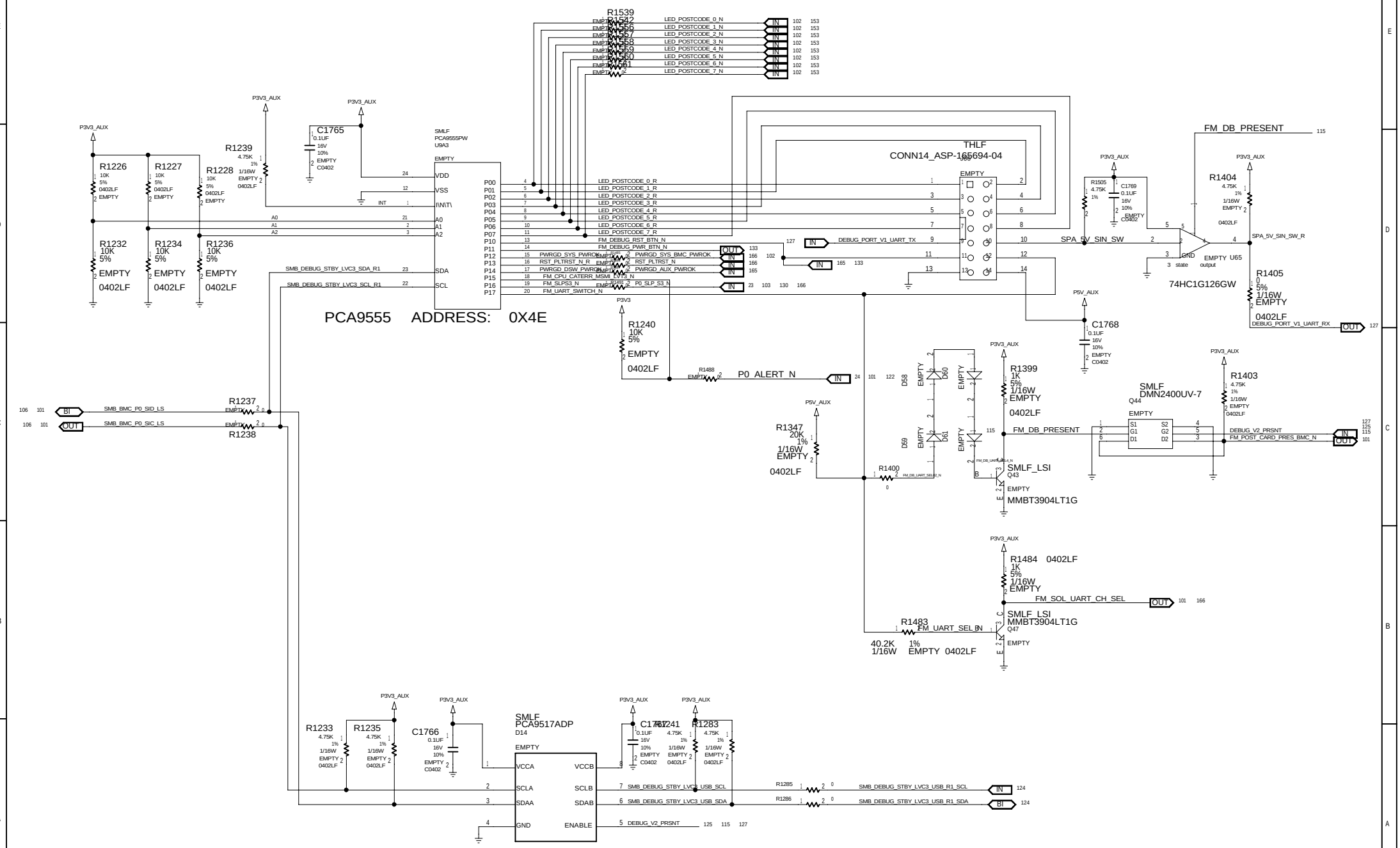

DEBUG_SMBUS

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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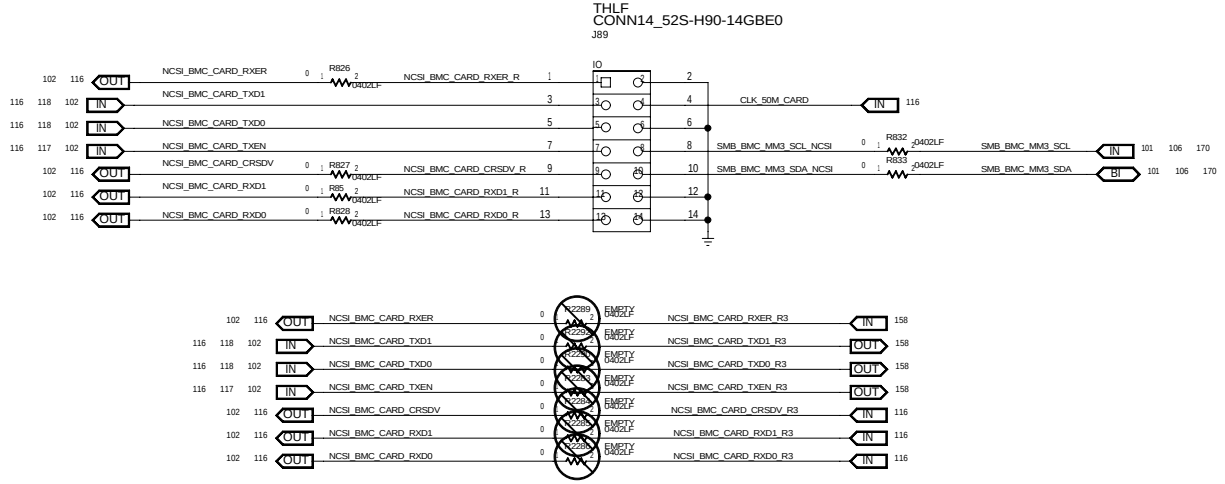
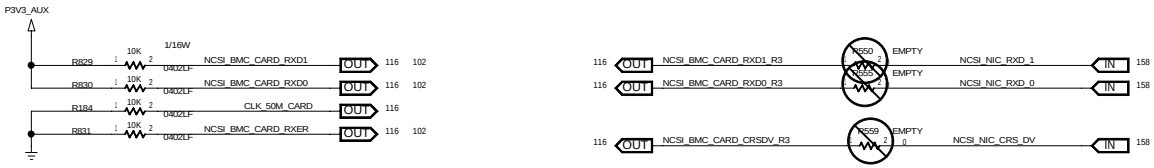
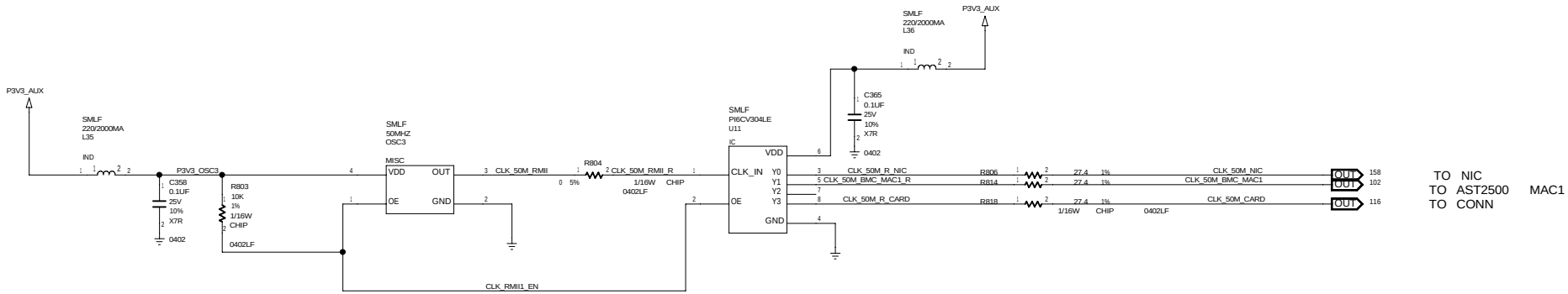
NCSI Connector				
Pin	Signal	I/O	Voltage	Description
1	RXER	O	3.3V	Enable signal from Rack Manager to HSC on the Blade
2	GND	I	0V	Ground
3	TXD1	I	3.3V	Transmit Data from BMC to NIC
4	CLK_50M	I	0V	50Mhz Clock
5	TXD0	I	3.3V	Transmit Data from BMC to NIC
6	GND	I	0V	Ground
7	TXEN	I	3.3V	Transmit Enable from BMC to NIC
8	GND	I	0V	Ground
9	CRSDV	O	3.3V	Receive carrier sense and data valid from NIC to BMC
10	GND	I	0V	Ground
11	RXD1	O	3.3V	Receive Data from NIC to BMC
12	GND	I	0V	Ground
13	RXD0	O	3.3V	Receive Data from NIC to BMC
14	GND	I	0V	Ground



CAD NOTE:
PLACE SEVEN RESISTORS CLOSE CONNECTOR WITHIN 0.5"





TO NIC
TO AST2500 MAC1
TO CONN

NCSI CONN

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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DESIGN NOTE: BIT 0 (DEDICATED STRAP PIN)
BALL NAME: FWSPICS0#

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
DISABLE CPU BOOT	AB19	SPI_BMC_FW_CS0_N	PU

STRAP VALUE = INVERSE OF INPUT	DESCRIPTION	INPUT LEVEL
STRAP VALUE= 0(DEFAULT)	ENABLE BMC	PU
STRAP VALUE= 1	DISABLE BMC	PD

P3V3_AUX
0402LF
R922
2.21K
1%
1/16W
CHIP
SPI_BMC_BT_CS0_N — OUT — 102 142 22 108

DESIGN NOTE:
TO PCH GPIO AND BIOS CONTROL,
IF BMC DISABLE,
BIOS IS HIGH ACTIVITY

DESIGN NOTE: BIT 1 (NOT IN HW STRAP)
RESERVED

DESIGN NOTE:
-STRAP VALUE=0,PULL HIGH THE PIN TO 3V3 STANDBY POWER
BY A RESISTOR OF VALUE 2.2K OHM
-STRAP VALUE=1,PULL DOWN THE PIN TO GROUND
BY A RESISTOR OF VALUE 1K TO 4.7K OHM

DESIGN NOTE: BIT 2 (OPTIONAL STRAP PIN) FOR VGA MEMORY SIZE SELECTION
BIT 2 IS CONTROLLED BY BMC FIRMWARE. BMC FIRMWARE DEFAULT IS 1
BIT 3 IS CONTROLLED BY HW PU/PD RES. DEFAULT IS 0

P3V3_AUX
CAD NOTE: PLACE THE PU RES CLOSE BMC PIN R19,
AND ON THE TRACE TO REDUCE STUB
R520 — EMPTY — 3.3K 0402LF 5% 1/16W — FM_BMC_GPIOS4 — OUT — 102

DESIGN NOTE: BIT 3 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOS4

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
VGA MEMORY SIZE SELECTION	R19	FM_BMC_GPIOS4	PD

00	SELECT 8MB VGA MEMORY	
01(DEFAULT)	SELECT 16MB VGA MEMORY	
10	SELECT 32MB VGA MEMORY	
11	SELECT 64MB VGA MEMORY	

DEFINED THE VGA MEMORY SIZE THAT WILL SHARE WITH SOC MEMORY
ASTPPED COMMENT:
FOR AST2500,IT ONLY REQUIRES 16MB TO SUPPORT ALL RESOLUTIONS.
THIS STRAPIS RESERVED FOR AST2510
WHICH IS VGA ONLY SKEW TO CHOOSE 64MB SIZE

DESIGN NOTE:
-STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER
BY A RESISTOR OF VALUE 1K TO 4.7K OHM

DESIGN NOTE: BIT 4 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOS5

P3V3_AUX
CAD NOTE:
AND ON THE TRACE TO REDUCE STUB
R543 — EMPTY — 3.3K 0402LF 5% 1/16W — FM_BMC_GPIOS5 — OUT — 102

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
RESERVED (1)	W20	FM_BMC_GPIOS5	PD

DESIGN NOTE:
-STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER
BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX
CAD NOTE: PLACE THE PU RES CLOSE BMC PIN U20,
AND ON THE TRACE TO REDUCE STUB
R521 — EMPTY — 3.3K 0402LF 5% 1/16W — FM_BMC_GPIOS6 — OUT — 102
R858 — 3.3K 5% 1/16W — EMPTY — 0402LF

DESIGN NOTE: BIT 5 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOS6

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
ENABLE DEDICATED VGA BIOS ROM	U20	FM_BMC_GPIOS6	PD

0(DEFAULT)	NO VGA BIOS ROM,VGA BIOS IS MERGED IN THE SYSTEM BIOS
1	ENABLE DEDICATED VGA BIOS ROM

DESIGN NOTE:
-STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER
BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX
CAD NOTE: PLACE THE PU RES CLOSE BMC PIN E9,
AND ON THE TRACE TO REDUCE STUB
R580 — CHIP — 3.3K 0402LF 5% 1/16W — RGMII_BMC_TX_CTRL — OUT — 102 112

DESIGN NOTE: BIT 6 (DEDICATEDL STRAP PIN)
BALL NAME: RGMII1TXCTL

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
DEFINE MAC#1 INTERFACE	E9	RGMII_BMC_TX_CTRL	PD

0(DEFAULT)	RMII/NCSI
1	RGMII

DESIGN NOTE:
-STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER
BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX
CAD NOTE: PLACE THE PU RES CLOSE BMC PIN B1,
AND ON THE TRACE TO REDUCE STUB
R555 — EMPTY — 3.3K 0402LF 1/16W 5% — NCSI_BMC_CARD_TXEN — OUT — 102 116
R912 — 4.7K CHIP 5%

DESIGN NOTE: BIT 7 (DEDICATEDL STRAP PIN)
BALL NAME: RGMII2TXCTL

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
DEFINE MAC#2 INTERFACE	B1	NCSI_BMC_CARD_TXEN	PD

0	RMII/NCSI
1(DEFAULT)	RGMII

DESIGN NOTE:
-STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER
BY A RESISTOR OF VALUE 1K TO 4.7K OHM

DESIGN NOTE: BIT 8 (NOT IN HW STRAP)
ENABLE SOFTWARE SECURE-BOOT TEST MODE

0(DEFAULT)	NORMAL MODE (DEFAULT)
1	ENABLE SECURE BOOT TEST

DESIGN NOTE: BIT 11:9 (NOT IN HW STRAP)
AXI/AHB CLOCK FREQUENCY RATIO SELECTION

11:9	DESCRIPTION
000	UNDEFINED
001(DEFAULT)	SELECT AXI:AHB= 2:1
010	SELECT AXI:AHB= 3:1
011	SELECT AXI:AHB= 4:1
100	SELECT AXI:AHB= 5:1
101	SELECT AXI:AHB= 6:1
110	SELECT AXI:AHB= 7:1
111	SELECT AXI:AHB= 8:1

HCLK FREQ=H-PLL/(RATIO_OF_CPU-AXI)/(RATIO_OF_AXI-AHB)

DESIGN NOTE: BIT 12 (DEDICATEDL STRAP PIN)
BALL NAME: RGMII1TXD0
INTERNAL PD

DESIGN NOTE: BIT 13 (DEDICATEDL STRAP PIN)
BALL NAME: RGMII1TXD1
INTERNAL PD

RGMII_BMC_TXD_<0> — OUT — 102 112
RGMII_BMC_TXD_<1> — OUT — 102 112
R265 — 4.7K CHIP 5%
R275 — 4.7K CHIP 5%

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
SPI MODE SELECTION	F9,A5	RMII_BMC_LOM_MEZZ_TXD<0> RMII_BMC_LOM_MEZZ_TXD<1>	PD PD

13:12	DESCRIPTION
00(DEFAULT)	DISABLE SPI INTERFACE
01	ENABLE SPI MASTER
10	ENABLE SPI MASTER AND SPI SLAVE TO AHB BRIDGE
11	ENABLE SPI PASS-THROUGH

DESIGN NOTE:
-STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER
BY A RESISTOR OF VALUE 1K TO 4.7K OHM

DESIGN NOTE: BIT 14 (NOT IN HW STRAP)
SELECT DEDICATED LPC RESET INPUT

0	LPC RESET IS SHARED WITH PCIE RESET PIN
1(DEFAULT)	LPC RESET IS LOCATED AT PIN NUMBER G22,SHARED WITH GPIOAC7

P3V3_AUX
CAD NOTE: PLACE THE PU RES CLOSE BMC PIN AA20,
AND ON THE TRACE TO REDUCE STUB
R750 — CHIP 1/16W — 3.3K 5% 0402LF — FM_BMC_GPIOS7 — OUT — 102

DESIGN NOTE: BIT 15 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOS7

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
VGA CLASS CODE SELECTION	AA20	FM_BMC_GPIOS7	PD

0	SELECT THE CLASS CODE FOR VIDEO DEVICE
1(DEFAULT)	SELECT THE CLASS CODE FOR VGA DEVICE

DESIGN NOTE:
-STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER
BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX
CAD NOTE: PLACE THE PU RES CLOSE BMC PIN E7,
AND ON THE TRACE TO REDUCE STUB
R760 — EMPTY — 3.3K 0402LF 5% 1/16W — RGMII_BMC_TXD_<2> — OUT — 102 112
R1552 — 3.3K 5%

DESIGN NOTE: BIT 16 (DEDICATED STRAP PIN)
BALL NAME: RGMII1TXD2

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
SUPERIO CONFIGURATION ADDRESS SELECTION	E7	RGMII_BMC_TXD_<2>	PD

0(DEFAULT)	DECODE 0X2E
1	DECODE 0X4E

DESIGN NOTE:
-STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER
BY A RESISTOR OF VALUE 1K TO 4.7K OHM

BMC HW STRAPS (BIT 0-16)

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P3V3_AUX — R164 (CHIP, 3.3K, 1/16W, 0402LF, 5%) — FM_BMC_GPIOZ4 — OUT 102

CAD NOTE: PLACE THE PU RES CLOSE BMC PIN U21, AND ON THE TRACE TO REDUCE STUB

DESIGN NOTE: BIT 17 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOZ4

STRAP NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
ENABLE BMC 2ND BOOT WATCHDOG TIMER	U21	FM_BMC_GPIOZ4	PD

0	DISABLE
1(DEFAULT)	ENABLE BMC 2ND BOOT WATCHDOG TIMER START COUNTING AT POWER UP.

THE WATCHDOG TIMER WAS LOCATED AT WDT2.AFTER WATCHDOG TIMEOUT, IT WILL RESET BMC AND RESTART BOOTING FROM THE 2ND BOOT FLASH AT CS1#. CS1# MUST BE THE SAME FLASH TYPE AS CS0# AND COULD BE THE SAME FIRMWARE AS CS0#.

BMC COMMENT:
FOLLOW GRANTLEY PROJECT DESIGN. USE DEFAULT FW SETTING.
THIS IS RESERVED ONLY.

ASPEED COMMENT:
IT IS NOT REQUIRED TO DISABLE THIS FEATURE BY HARDWARE, FIRMWARE CAN DO IT.

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — R172 (EMPTY, 3.3K, 0402LF, 5%, 1/16W) — FM_BMC_GPIOZ5 — OUT 102

CAD NOTE: PLACE THE PU RES CLOSE BMC PIN W22, AND ON THE TRACE TO REDUCE STUB

DESIGN NOTE: BIT 18 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOZ5

STRAP NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
SELECT USBCKI INPUT FRRQ.	W22	FM_BMC_GPIOZ5	PD

0(DEFAULT)	24 MHZ
1	48 MHZ

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — R1408 (EMPTY, 4.75K, 1%, 1/16W, 0402LF) — RGMII_BMC_TXD_<3> — R1604 (3.3K, 5%) — OUT 102 112

CAD NOTE: PLACE THE PU RES CLOSE BMC PIN D7, AND ON THE TRACE TO REDUCE STUB

DESIGN NOTE: BIT 19 (DEDICATED STRAP PIN)
BALL NAME: RGMII1TXD3

STRAP NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
ENABLE ACPI FUNCTION	D7	RMII_BMC_TXD<3>	PD

0(DEFAULT)	DISABLE ACPI
1	ENABLE ACPI

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — R764 (EMPTY, 3.3K, 5%, 1/16W, 0402LF) — FM_BMC_GPIOZ6 — OUT 102

CAD NOTE: PLACE THE PU RES CLOSE BMC PIN V22, AND ON THE TRACE TO REDUCE STUB

DESIGN NOTE: BIT 20 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOZ6

STRAP NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
DISABLE LPC TO DECODE SUPERIO 0X2E/0X4E ADDRESS	V22	FM_BMC_GPIOZ6	PD

0(DEFAULT)	ENABLE ADDRESS DECODING
1	DISABLE ADDRESS DECODING

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — R765 (CHIP, 3.3K, 1/16W, 0402LF, 5%) — NCSI_BMC_CARD_TXD0 — OUT 102 116
R924 (EMPTY, 4.75K, 1/16W, 0402LF, 1%)

CAD NOTE: PLACE THE PU RES CLOSE BMC PIN A2, AND ON THE TRACE TO REDUCE STUB

DESIGN NOTE: BIT 21 (DEDICATED STRAP PIN)
BALL NAME: RGMII2TXD0

STRAP NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
ENABLE GPIOD PASS-THROUGH MODE	A2	NCSI_BMC_CARD_TXD0	PD

0	DISABLE PASS THROUGH CAN BE ENABLED BY SCU8C[11:8]
1(DEFAULT)	ENABLE PASS-THROUGH AT POWER ON.

PASS-THROUGH PINS SET:
GPIOD0 -> GPIOD1
GPIOD2 -> GPIOD3
GPIOD4 -> GPIOD5
GPIOD6 -> GPIOD7

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — R766 (EMPTY, 3.3K, 1/16W, 5%, 0402LF) — NCSI_BMC_CARD_TXD1 — OUT 102 116
R2404 (CHIP, 4.75K, 1%, 1/16W, 0402LF)

CAD NOTE: PLACE THE PU RES CLOSE BMC PIN B3, AND ON THE TRACE TO REDUCE STUB

DESIGN NOTE: BIT 22 (DEDICATED STRAP PIN)
BALL NAME: RGMII2TXD1

STRAP NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
ENABLE GPIOE PASS-THROUGH MODE	B3	NCSI_BMC_CARD_TXD1	PD

0(DEFAULT)	DISABLE PASS THROUGH CAN BE ENABLED BY SCU8C[15:12]
1	ENABLE PASS-THROUGH AT POWER ON.

PASS-THROUGH PINS SET:
GPIOE0 -> GPIOE1
GPIOE2 -> GPIOE3
GPIOE4 -> GPIOE5
GPIOE6 -> GPIOE7

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — R767 (EMPTY, 3.3K, 0402LF, 5%, 1/16W) — BMC_GPIOU2_R — OUT 102
R923 (4.75K, 1/16W, CHIP, 0402LF, 1%)

CAD NOTE: PLACE THE PU RES CLOSE BMC PIN D5, AND ON THE TRACE TO REDUCE STUB

DESIGN NOTE: BIT 23 (DEDICATED STRAP PIN)
BALL NAME: RGMII2TXD2

STRAP NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
SELECT 25 MHZ REFERENCE CLOCK INPUT MODE	D5	BMC_GPIOU2_R	PD

0(DEFAULT)	CLKIN IS 24 MHZ AND USBCKI NOT USED
1	CLKIN IS 25 MHZ AND USBCKI= 24/48 MHZ (DETERMINED BY BIT[18]

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — R768 (CHIP, 3.3K, 0402LF, 5%, 1/16W) — BMC_GPIOU3_R — OUT 102

CAD NOTE: PLACE THE PU RES CLOSE BMC PIN D4, AND ON THE TRACE TO REDUCE STUB

DESIGN NOTE: BIT 24 (DEDICATED STRAP PIN)
BALL NAME: RGMII2TXD3

STRAP NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
SELECT DDR4 SDRAM	D4	BMC_GPIOU3_R	PD

0	DDR3 SDRAM
1(DEFAULT)	DDR4 SDRAM

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — R772 (EMPTY, 3.3K, 5%, 0402LF, 1/16W) — SPI_BMC_BT_DI — OUT 108 102

CAD NOTE: PLACE THE PU RES CLOSE BMC PIN T18, AND ON THE TRACE TO REDUCE STUB

DESIGN NOTE: BIT 25 (DEDICATED STRAP PIN)
BALL NAME: FWSPIMISO

STRAP NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
ENABLE ESPI MODE	T18	SPI_BMC_BT_DI	PD

0(DEFAULT)	LPC MODE (ONLY FOR PSPO STAGE)
1	ESPI MODE (NORMAL STAGE)

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — R770 (EMPTY, 4.75K, 0402LF, 1%, 1/16W) — JTAG_BMC_RTCK — OUT 103

CAD NOTE: PLACE THE PU RES CLOSE BMC PIN C9, AND ON THE TRACE TO REDUCE STUB

DESIGN NOTE: BIT 26 (DEDICATED STRAP PIN)
BALL NAME: RTCK

STRAP NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
ENABLE ESPI FLASH MODE	C9	JTAG_BMC_RTCK	PD

0(DEFAULT)	ESPI RESPOND WITH NO FLASH ATTACHED
1	ESPI RESPOND WITH FLASH ATTACHED

THIS BIT IS VALID ONLY WHEN ESPI IS ENABLED

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

P3V3_AUX — R769 (CHIP, 3.3K, 0402LF, 1/16W, 5%) — FM_BMC_GPIOZ7 — OUT 102

CAD NOTE: PLACE THE PU RES CLOSE BMC PIN W21, AND ON THE TRACE TO REDUCE STUB

DESIGN NOTE: BIT 27 (OPTIONAL STRAP PIN)
IT ONLY BE USED FOR GPIO FUNCTION DUE TO BIT30 IS DISABLED
BALL NAME: GPIOZ7

STRAP NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
ENALBE FAST RESET MODE FOR ARM ICE DEBUGGER	W21	FM_BMC_GPIOZ7	PD

0	LONG RESET MODE, NORMAL OPERATION
1(DEFAULT)	FAST RESET MODE, FOR ICE DEBUGGER CONNECTION

ENABLE FAST RESET MODE TO ENABLE ICE DEBUGGER CAN STOP ARM AT STARTING ADDRESS 0

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

DESIGN NOTE: BIT 28 (NOT IN HW STRAP)
RESERVED

R926 (4.75K, 1/16W, EMPTY, 0402LF) — BMC_COM5_UART_TX — OUT 102 127 165

CAD NOTE: PLACE THE PD RES CLOSE BMC PIN K1, AND ON THE TRACE TO REDUCE STUB

DESIGN NOTE: BIT 29 (DEDICATED STRAP PIN)
BALL NAME: TXD5

STRAP NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
SELECT UART DEBUG PORT	K1	BMC_COM5_UART_TX	PU

0	SELECT UART1 AS BMC CONSOLE PORT
1(DEFAULT)	SELECT UART5 AS BMC CONSOLE PORT

THIS BIT IS USED TO SELECT THE UART PORT FOR USER DEBUGGING. IT IS NOT THE BMC CONSOLE FUNCTION. THE FUNCTION IS SIMILAR TO THE PCIE-TO-AHB BRIDEG, WHICH IS WORKING AS A HARDWARE U-BOOT INTERFACE, AND NO FIRMWARE REQUIRED TO OPERATE. THIS INTERFACE CAN SUPPORT FIRMWARE UPDATE CAPABILITY WIHTOUT FIRMWARE WORKING REQUIRED.

ASPEED COMMENT:
FOR THE UARTS PORT LEVEL SHIFTER,PLEASE USE THE ONE THAT CAN SUPPORT BAUD RATE UP TO 1MBPS. AST2500 HAS A NEW FEATURE THAT CAN UPDATE THE BMC SPI FLASH THROUGH THE DEBUG UART INTERFACE.

DESIGN NOTE: -STRAP VALUE=0,PULL DOWN THE PIN TO GROUND BY A RESISTOR OF VALUE 1K TO 4.7K OHM
-STRAP VALUE=1,JUST LEAVE THE PIN FLOATING OR PULL UP

BMC HW STRAPS(BIT 17-29)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C	DATE Fri Dec 15 20:21:56 2017
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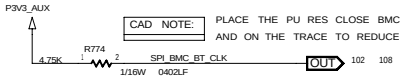


CAD NOTE: PLACE THE PU RES CLOSE BMC PIN AA18, AND ON THE TRACE TO REDUCE STUB

DESIGN NOTE: BIT 30 (DEDICATED STRAP PIN)
BALL NAME: FWSPICK

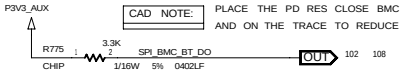
STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
ENABLE GPIO STRAP MODE(STEP2)	AA18	SPI_BMC_BT_CLK	PD

0	DISABLE
1(DEFAULT)	ENABLE

BMC COMMENT:
GPIO STRAP PINS(GPIOS[4-7]/GPIOZ[4-7]) CAN BE SETTING BY BMC FIRMWARE

ASPEED COMMENT:
RESERVED PU/PD RES FOR HW STRAP IF BMC FIRMWARE CRASH
BMC FIRMWARE NEED TO CHECK HW STRAP DEFAULT VALUE IF MATCH BMC'S REQUESTMENT

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM



CAD NOTE: PLACE THE PD RES CLOSE BMC PIN U17, AND ON THE TRACE TO REDUCE STUB

DESIGN NOTE: BIT 31 (DEDICATED STRAP PIN)
BALL NAME: FWSPIMOSI

STRAP NET NAME	BALL NUMBER	SIGNAL NAME	INTERNAL PU/PD
ENABLE SPI FLASH STRAP AUTO FETCH MODE(STEP3)	U17	SPI_BMC_BT_DO	PD

0(DEFAULT)	DISABLE
1	ENABLE

BMC COMMENT:
RESERVE PIN HEADER FOR DEBUGGING

ASPEED COMMENT:
PLEASE CHECK THIS FEATURE WITH FIRMWARE, IF THEY WANT TO DEFAULT ASSIGN SOME REGISTERS AT POWER UP. SINCE THIS FUNCTION WILL REQUIRE A SPECIAL FIRMWARE TO EMBEDDED THE STRAP CODE. OF COURSE IT HAS NO PROBLEM IF THE STRAP FIRMWARE CODE NOT EXISTED.

DESIGN NOTE: -STRAP VALUE=0,JUST LEAVE THE PIN FLOATING
-STRAP VALUE=1,PULL HIGH THE PIN TO 3V3 STANDBY POWER BY A RESISTOR OF VALUE 1K TO 4.7K OHM

DESIGN NOTE:

WHEN GPIO IS USED AS HARDWARE STRAP,
IT WILL CONSTRAIN THE ACTIVE LEVEL SELECTION OF THE GPIO APPLICATION.
EX.WHEN STRAP SETTING IS PULLED HIGH, THEN IT CAN BE USED AS A GPIO OF ACTIVE LOW THAT HAVE A POWER UP STATE OF HIGH.

NOTE: IF GPIO PINS THAT ALSO WANT TO USED AS HARDWARE STRAP, HAD BETTER TO USE THEM AS GPO ONLY.

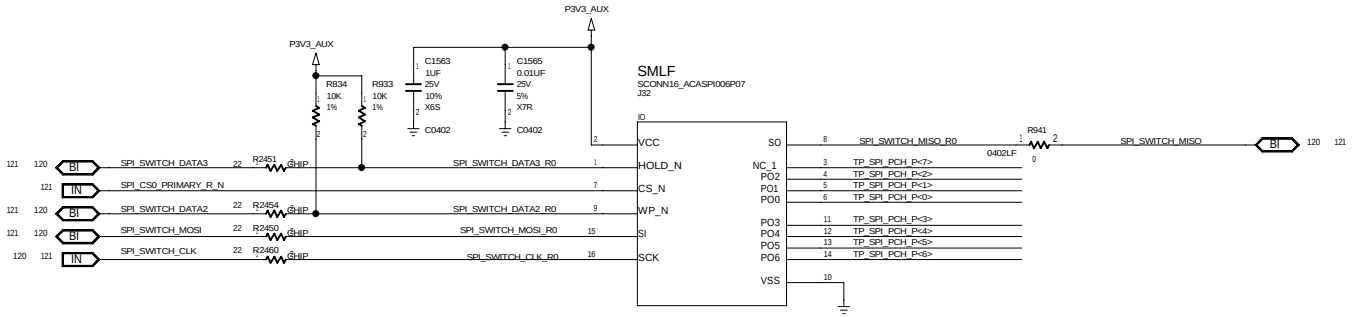
DESIGN NOTE:

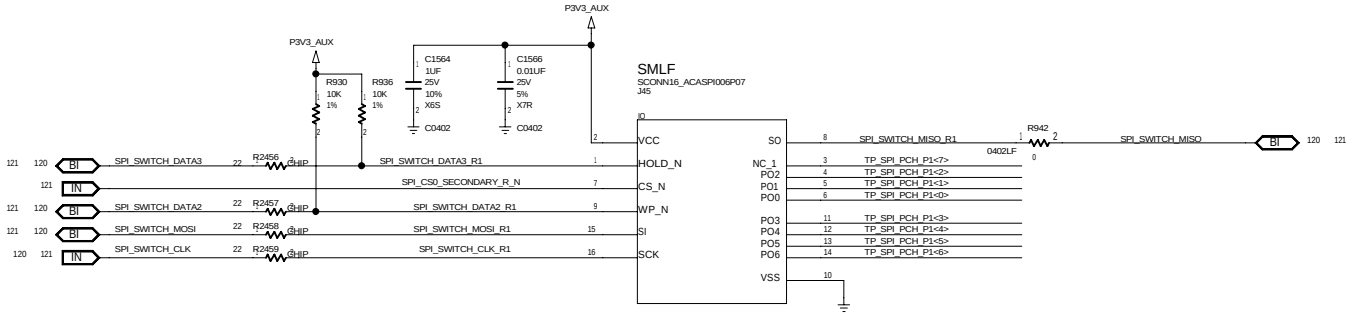
AST2500 DEFINES A 3 STEPS PROCEDURE FOR FUNCTIONAL STRAP SETTING INPUT.

1. STEP1:LOAD FROM DEDICATED STRAP PINS.
   - BASED ON THE SETTING AT STEP 1 TO LOAD STEP 2 OR STEP 3 STRAP INPUTS.
2. STEP2:HARDWARE STRAP: LOAD FROM THE OPTIONAL STRAP PINS WHEN SRST#(RST_RSMRST_N) ACTIVE.
3. STEP3:SOFTWARE STRAP: LOAD FROM THE FIRMWARE SPI FLASH WHEN SRST#(RST_RSMRST_N) INACTIVE.
   - THE STEP 2 AND STEP 3 STRAP INPUT MODES CAN BE ENABLED SIMUTANEOUSLY.
     BUT SOFTWARE STRAP EXECUTES LATER AND HAS HIGHER PRIORITY TO OVERWRITE HARDWARE STRAP.

THE HARDWARE STRAP REGISTERS LOAD THE EXTERNAL PIN VOLTAGE STATE
WHEN SRST#(RST_RSMRST_N) RESET INPUT IS LOW.
AND KEEP THE VALUE UNCHANGED AFTER SRST#(RST_RSMRST_N) GOEST HIGH.
THE STRAP REGISTER IS DEFINED AT ADDRESS 0X1E6E2070 IN THE SYSTEM CONTROL UNIT (SCU) MODULE.

BMC HW STRAPS (BIT 30-31)





CPU BIOS ROM

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
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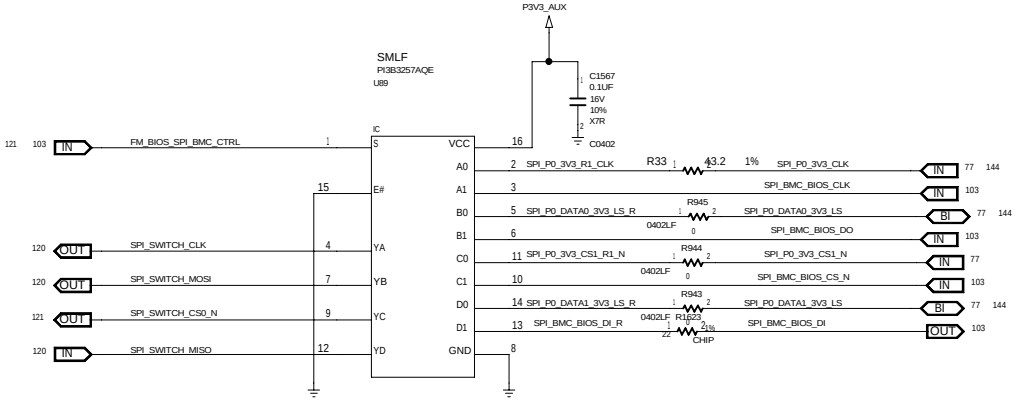
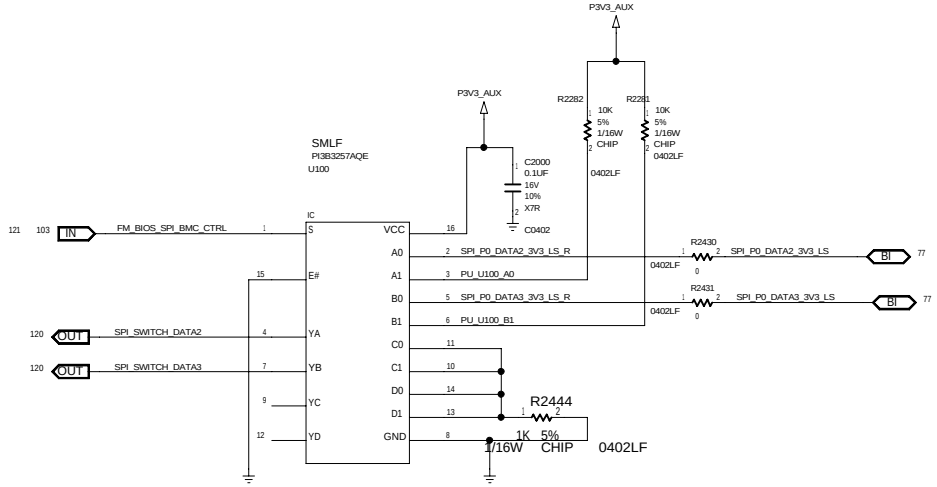
PI3B3257A TRUTH TABLE

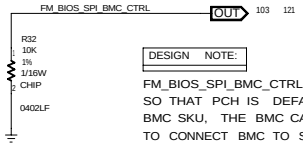
E#	S	Y_N	FUNCTION
H	X	HIZ	DISABLE
L	L	N_0	S=0
L	H	N_1	S=1





CAD NOTE:

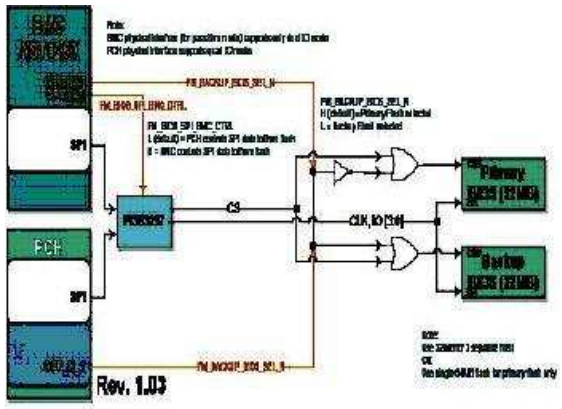
PLACE R8E18 CLOSE TO U8E6

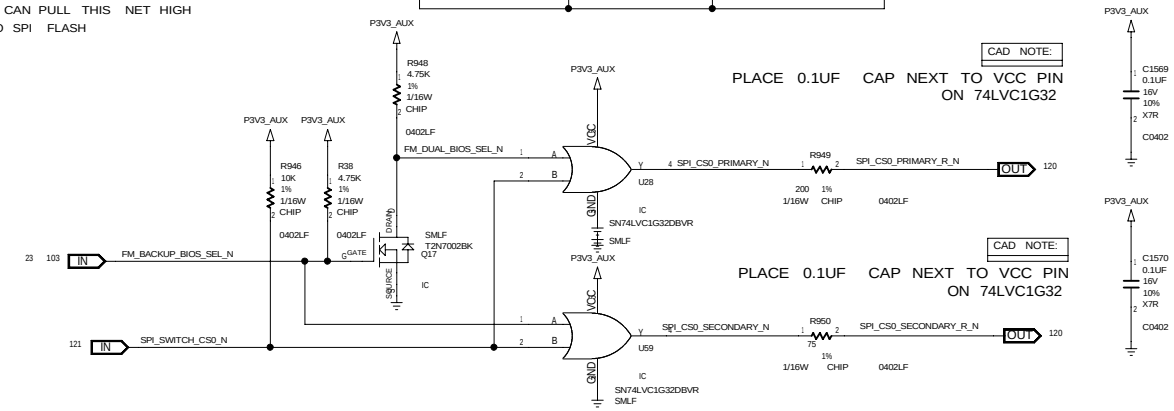


DESIGN NOTE:

FM_BIOS_SPI_BMC_CTRL NET SHOULD BE PULLED DOWN SO THAT PCH IS DEFAULT BUS AND FOR BMC SKU, THE BMC CAN PULL THIS NET HIGH TO CONNECT BMC TO SPI FLASH

FM_BACKUP_BIOS_SEL_N	SPI_SWITCH_CS0_N	BIOS	
H (DEFAULT)	L	PRIMARY (DEFAULT)	A1
L	L	SECONDARY	A0
X	H	X	





CAD NOTE:

PLACE 0.1UF CAP NEXT TO VCC PIN ON 74LVC1G32

CAD NOTE:

PLACE 0.1UF CAP NEXT TO VCC PIN ON 74LVC1G32

BMC SHARED SPI FLASH MUX

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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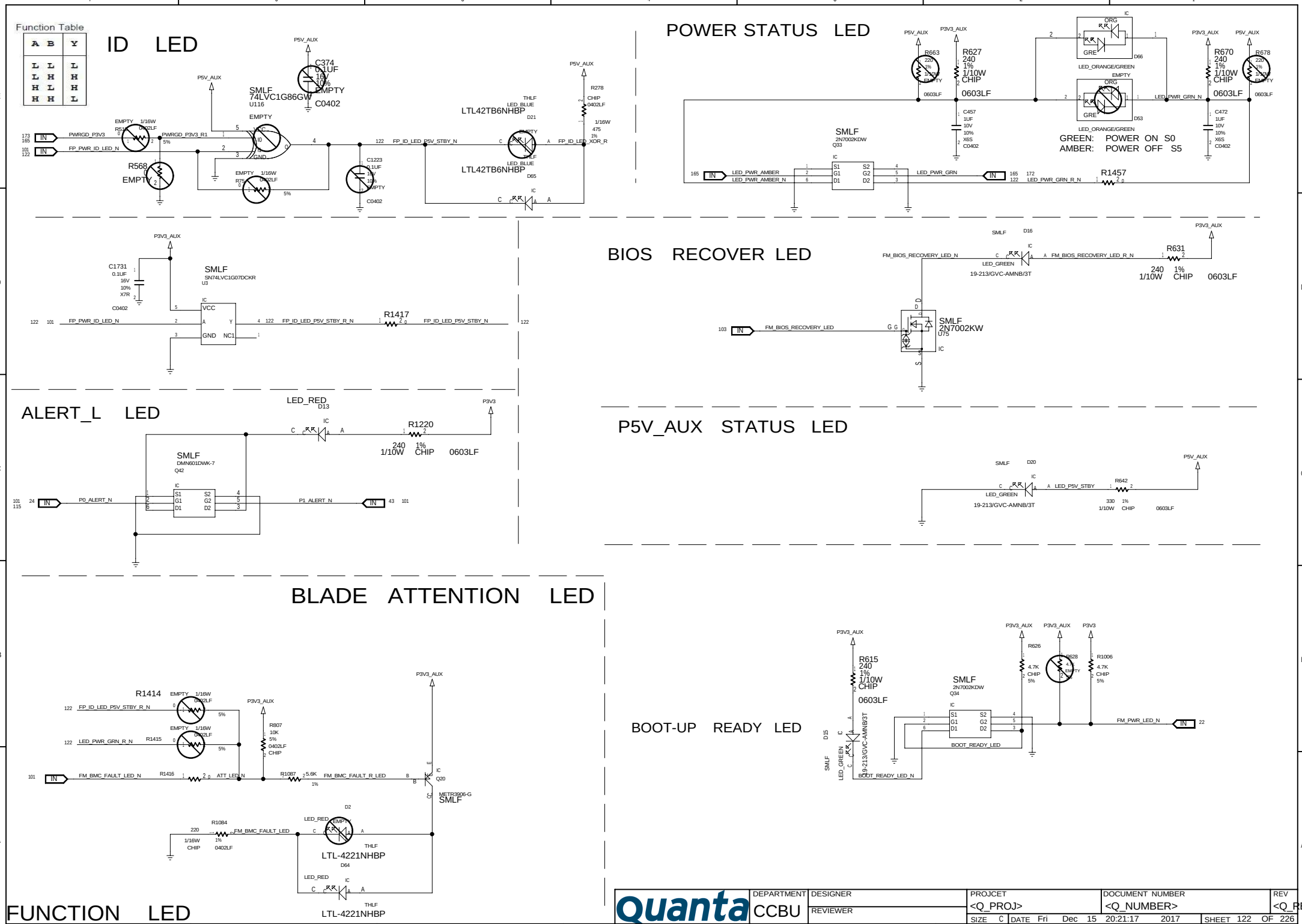
Function Table
A B Y
L L L
L H H
H L H
H H L
ID LED
SMLF 74LVC1G86GW U116
C374 0.1UF 16V 10% EMPTY C0402
LTL42TB6NHBP
POWER STATUS LED
LED_ORANGE/GREEN
GREEN: POWER ON S0
AMBER: POWER OFF S5
SMLF 2N7002KDW Q33
SN74LVC1G07DCKR U3
BIOS RECOVER LED
19-213/GVC-AMNB/3T
SMLF 2N7002KW U75
ALERT_L LED
SMLF DMN601DWK-7 Q42
P5V_AUX STATUS LED
BLADE ATTENTION LED
METR3906-G
LTL-4221NHBP
BOOT-UP READY LED
FUNCTION LED
Quanta
DEPARTMENT CCBU
DESIGNER
REVIEWER
PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>
REV <Q_REV>
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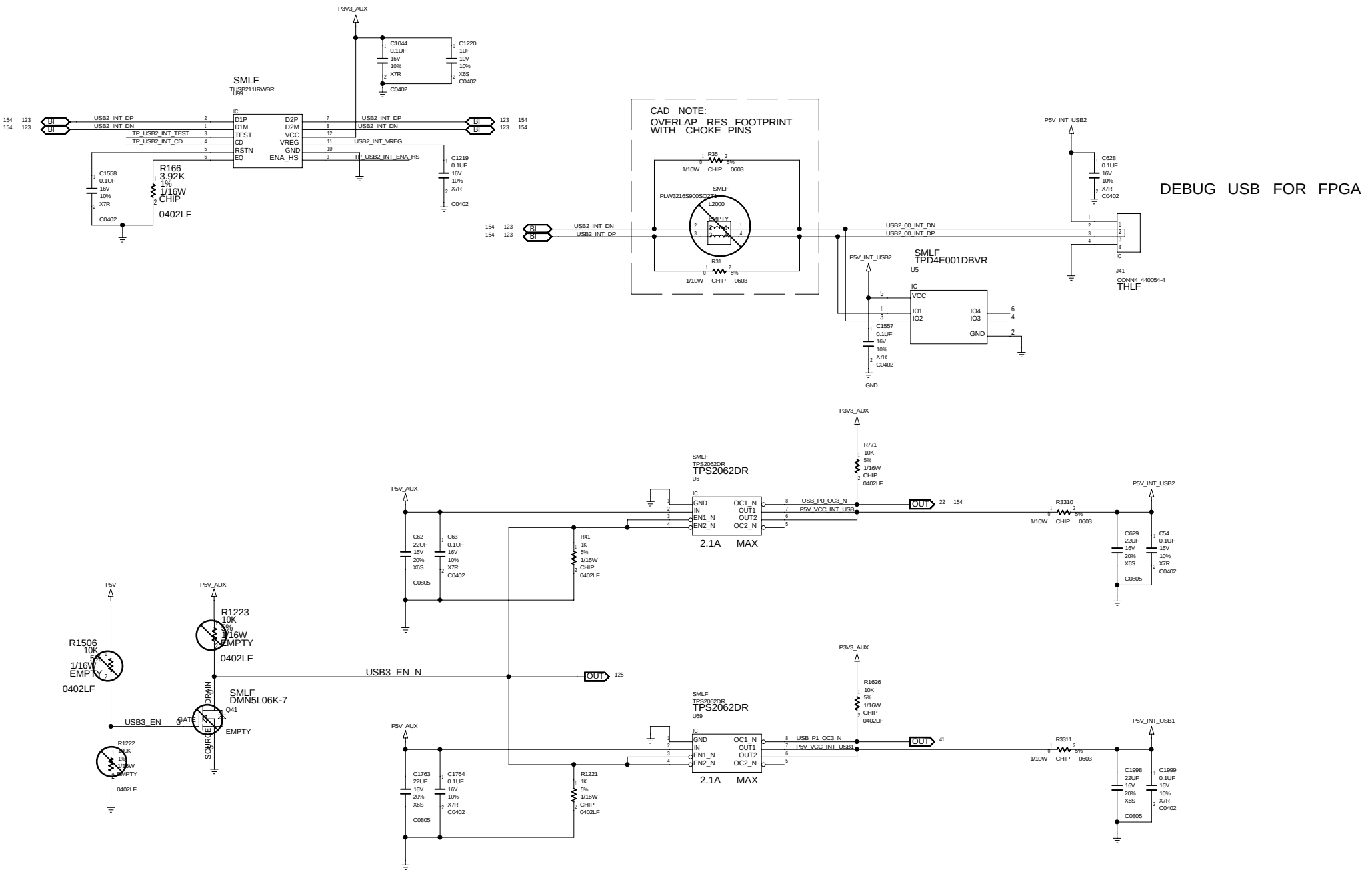
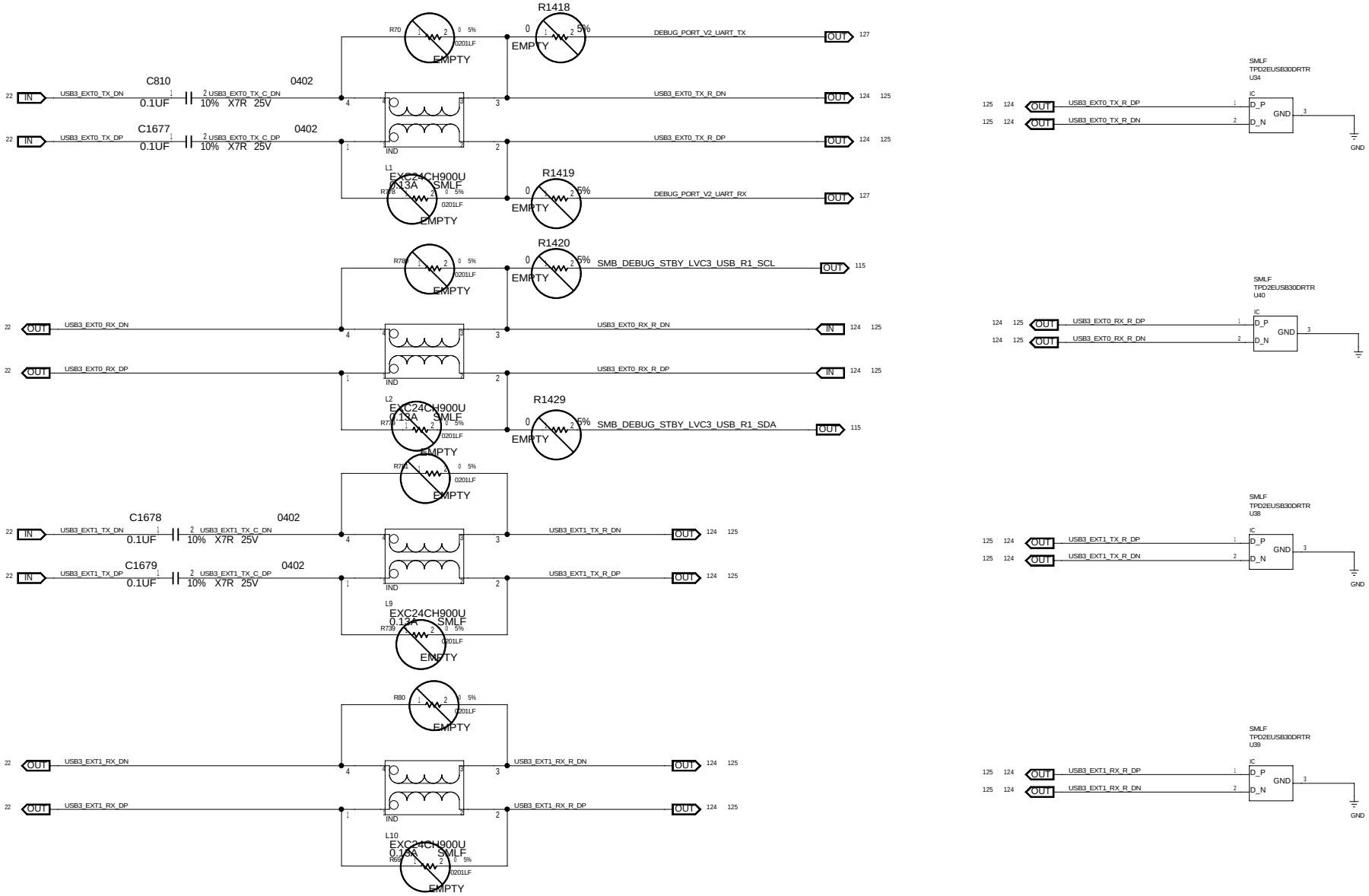


USB2 Internal for debug

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:17 2017	SHEET 123 OF 226



USB3 External (1 OF 2)

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
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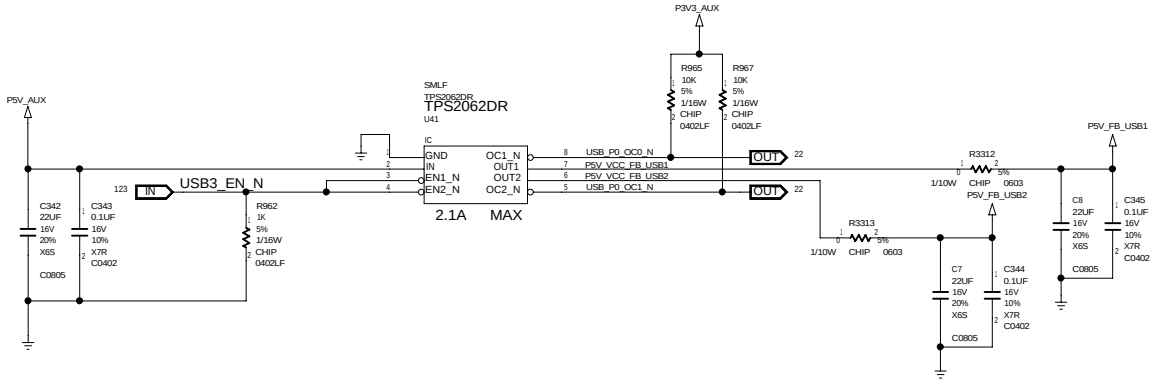
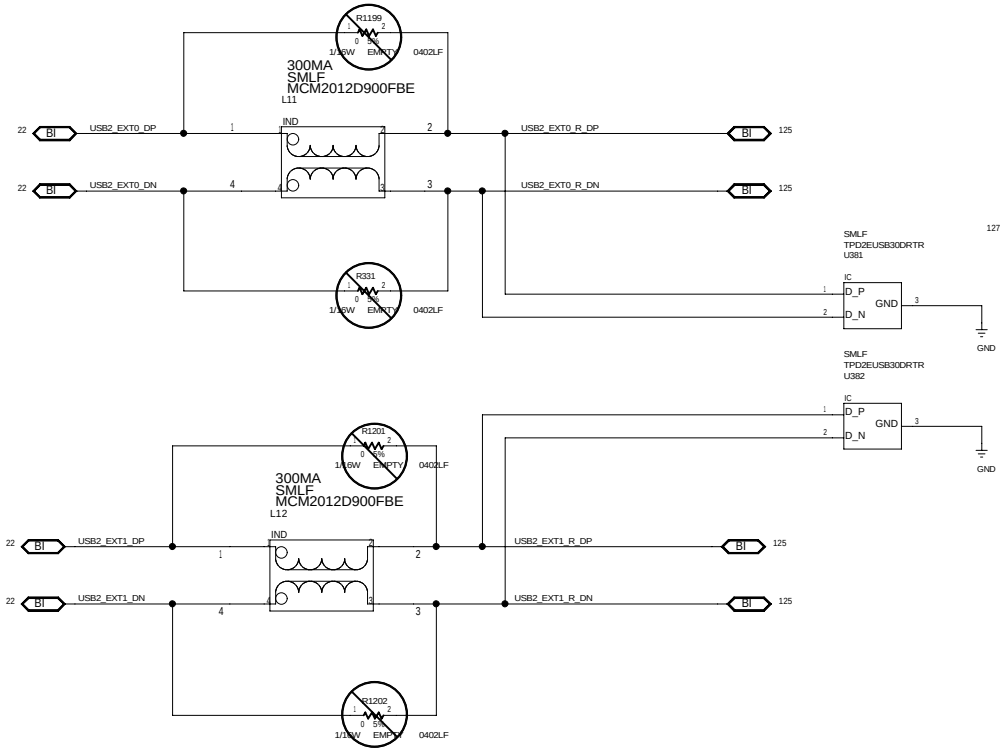
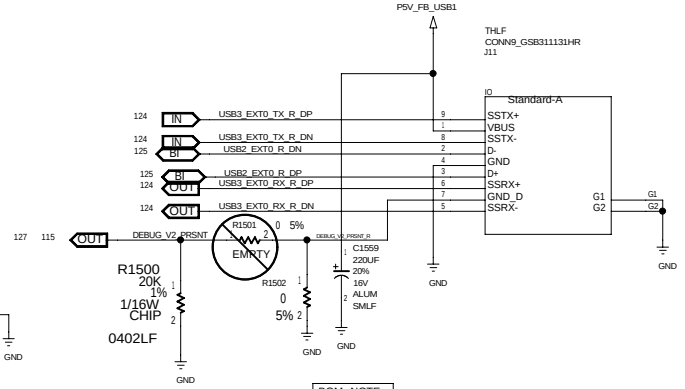
			SIZE C	DATE Fri Dec 15 20:21:57 2017	SHEET 124 OF 226





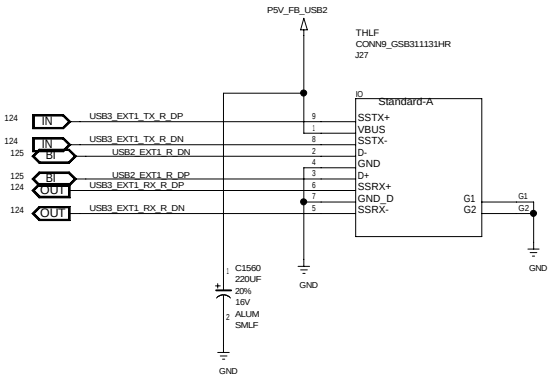
BOM NOTE:

CONTACT FINISH 30U GOLD/ SINGLE/ RIGHT TYPE



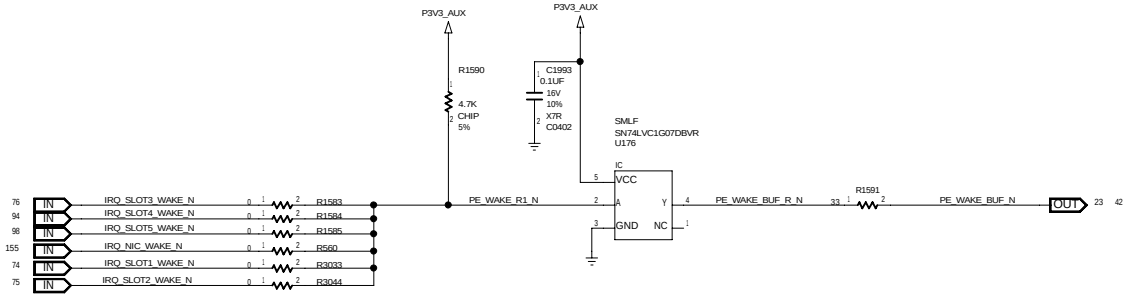
BOM NOTE:

CONTACT FINISH 30U GOLD/ SINGLE/ RIGHT TYPE



USB3 External (2 OF 2)

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:57 2017	SHEET 125 OF 226	



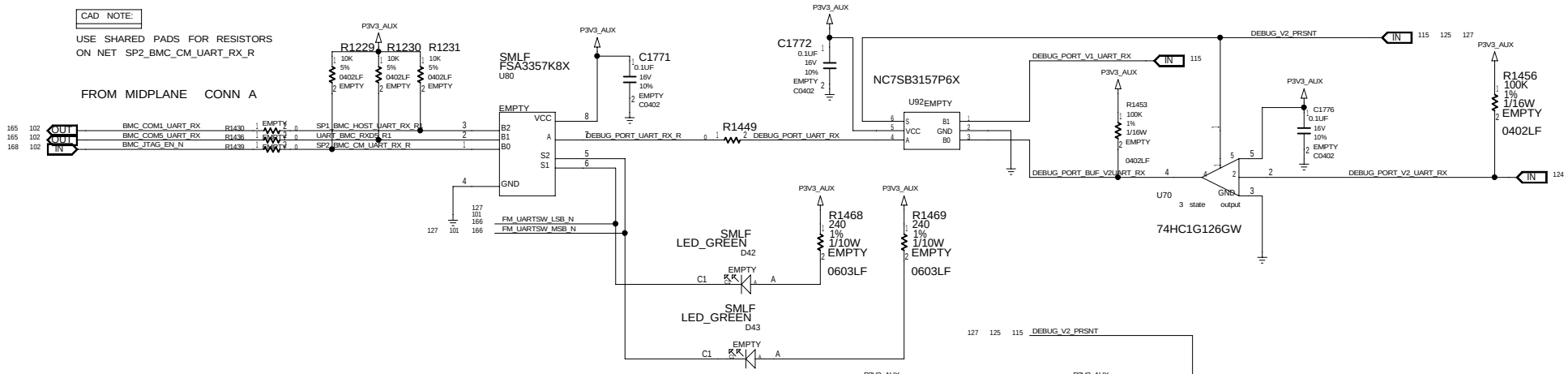
PCIE RESET & WAKEUP

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:57 2017	SHEET 126 OF 226

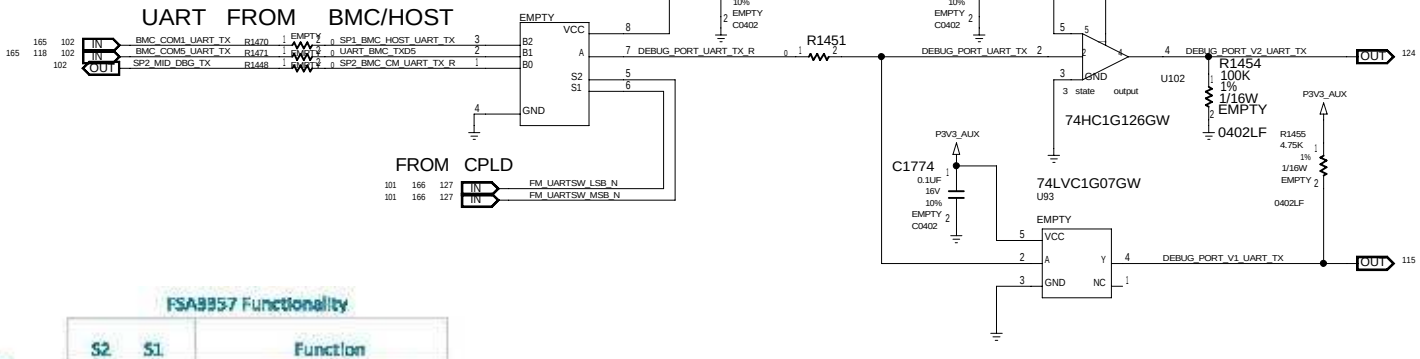
CAD NOTE:

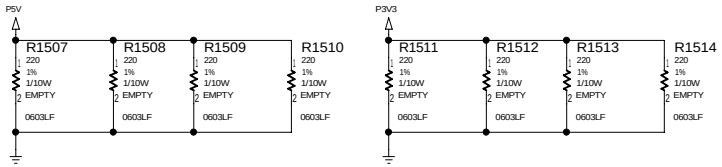
USE SHARED PADS FOR RESISTORS ON NET SP2_BMC_CM_UART_RX_R

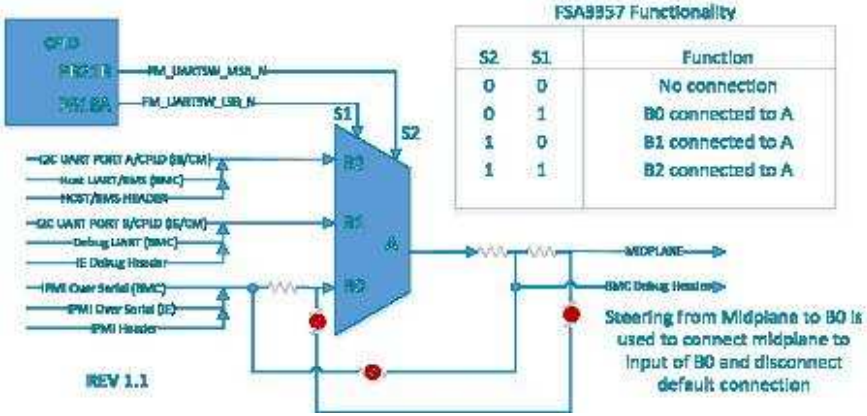
FROM MIDPLANE CONN A



UART FROM BMC/HOST







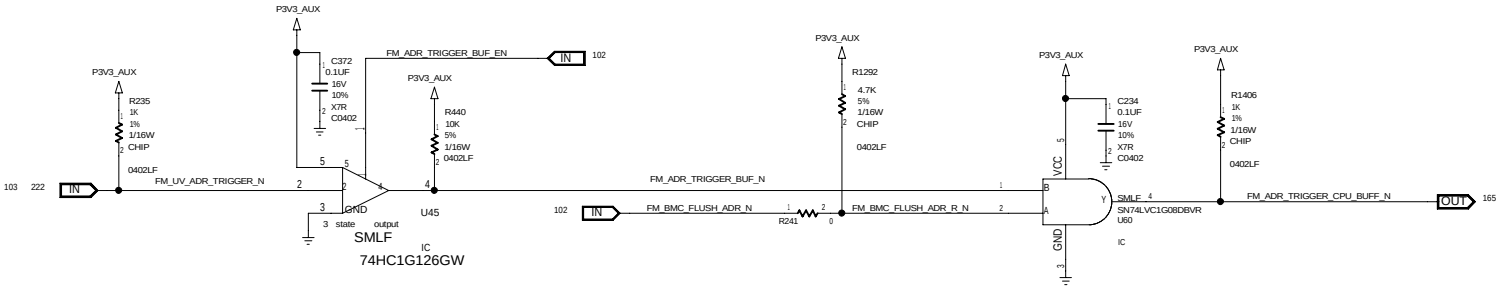
FSA3357 Functionality

S2	S1	Function
0	0	No connection
0	1	B0 connected to A
1	0	B1 connected to A
1	1	B2 connected to A

DEBUG_UART

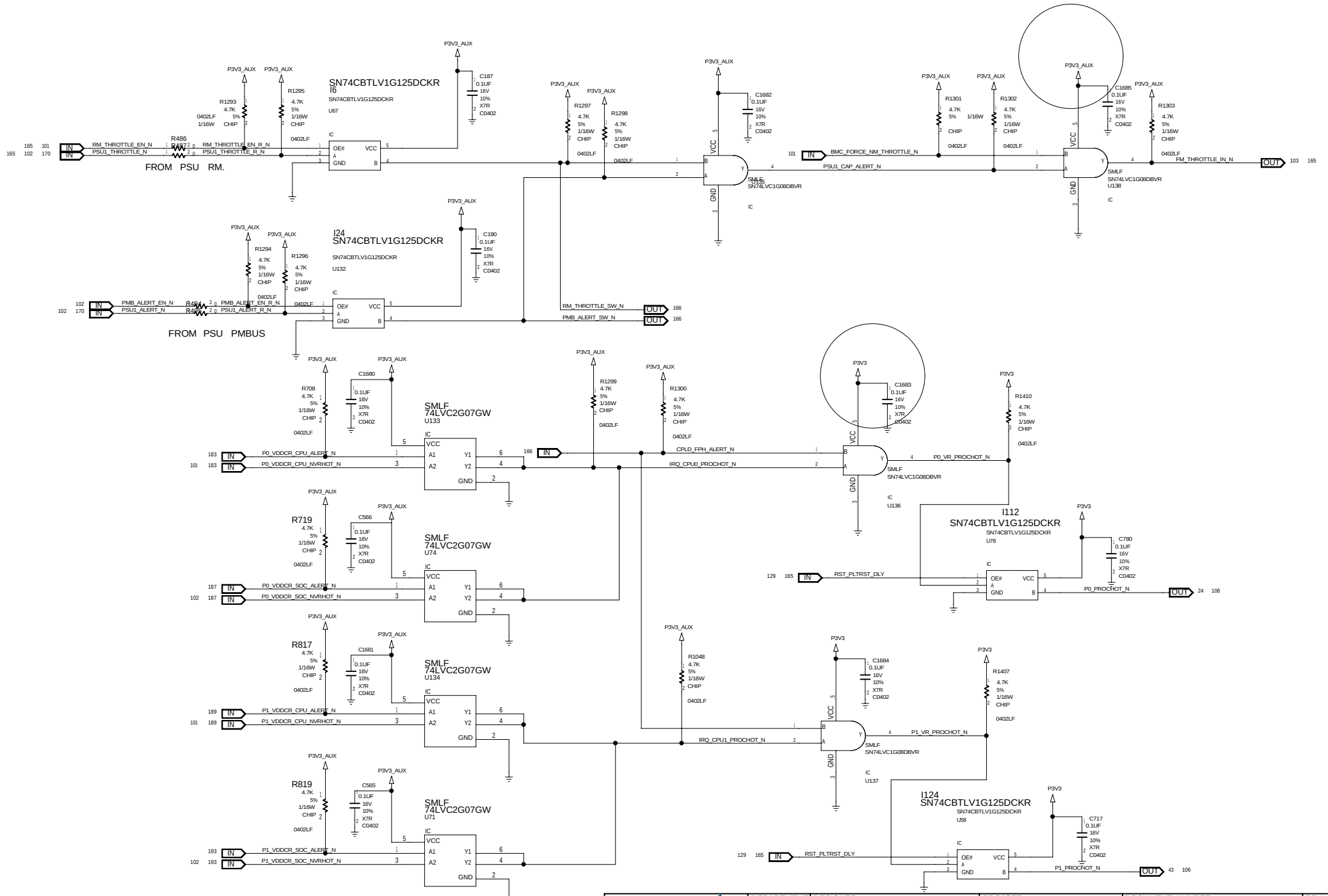
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:20 2017	SHEET 127 OF 226

NVDIMM SUPPORT



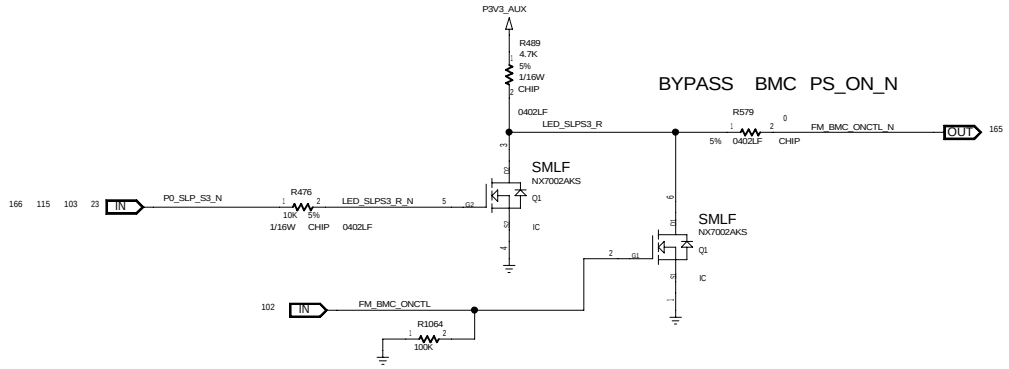
ADR SAVE & TRIGGER

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:57 2017	SHEET 128 OF 226



PSU & VR ALERT

Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>
		REVIEWER	DOCUMENT NUMBER <Q_NUMBER>
			REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:57 2017 SHEET 129 OF 226



S3 CONTROL

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:58 2017	SHEET 130 OF 226

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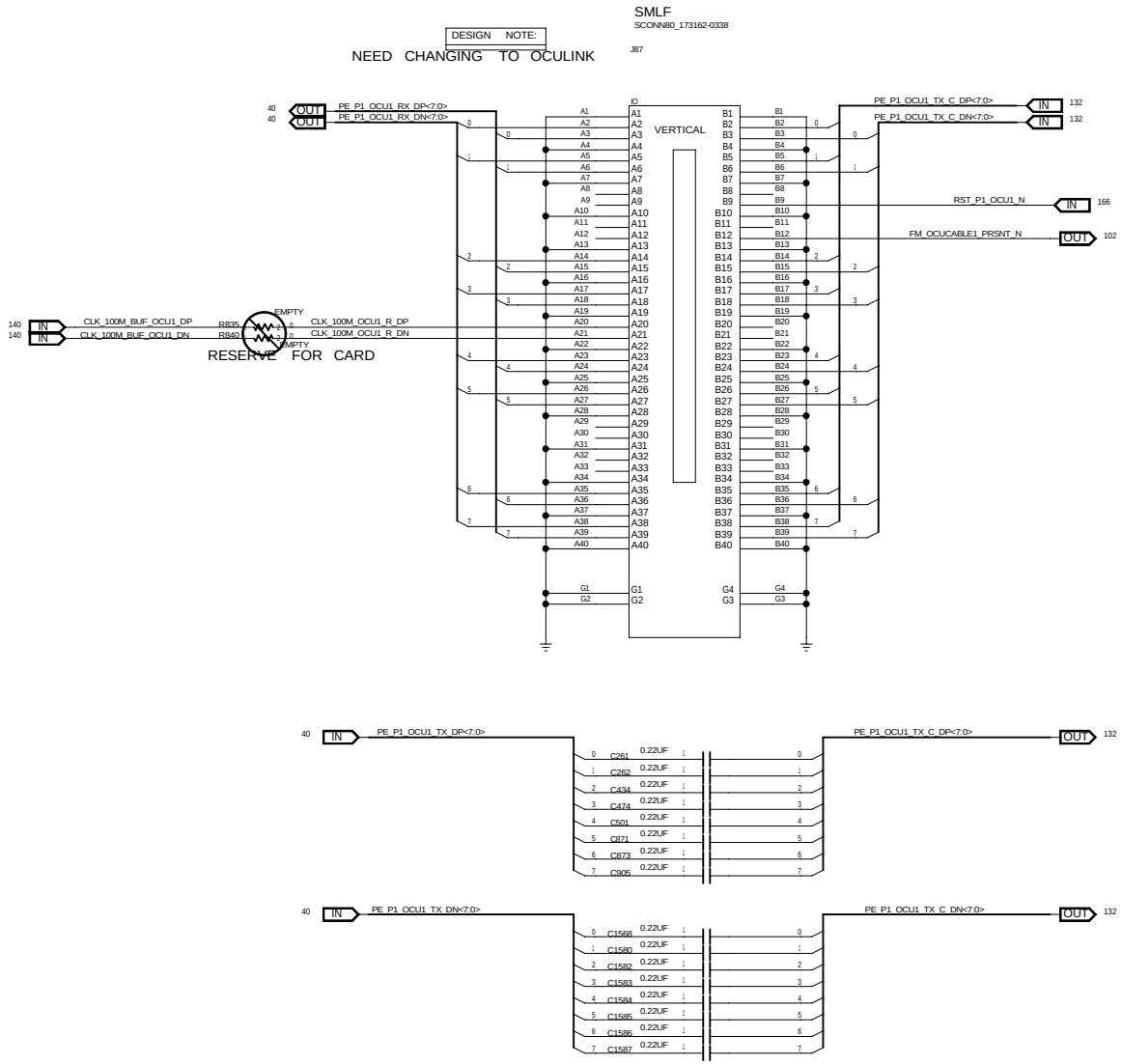
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:34:33 2017	SHEET 131 OF 226



OCulink CONN1

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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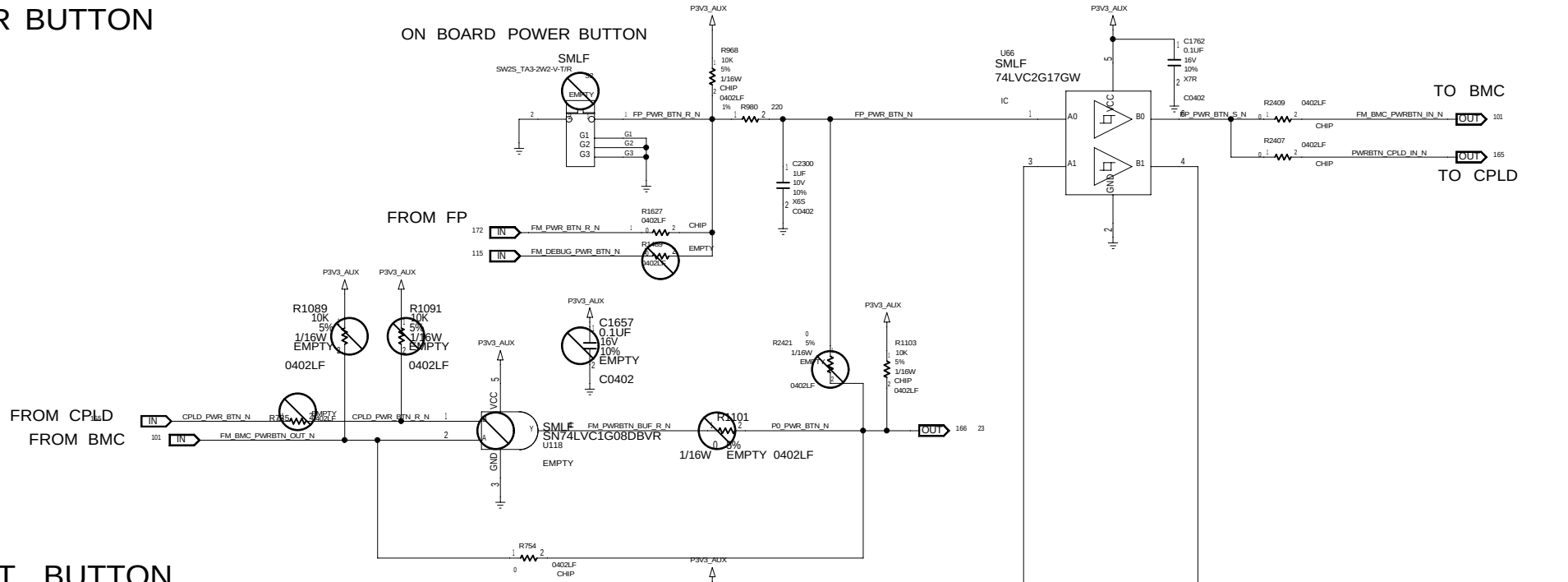
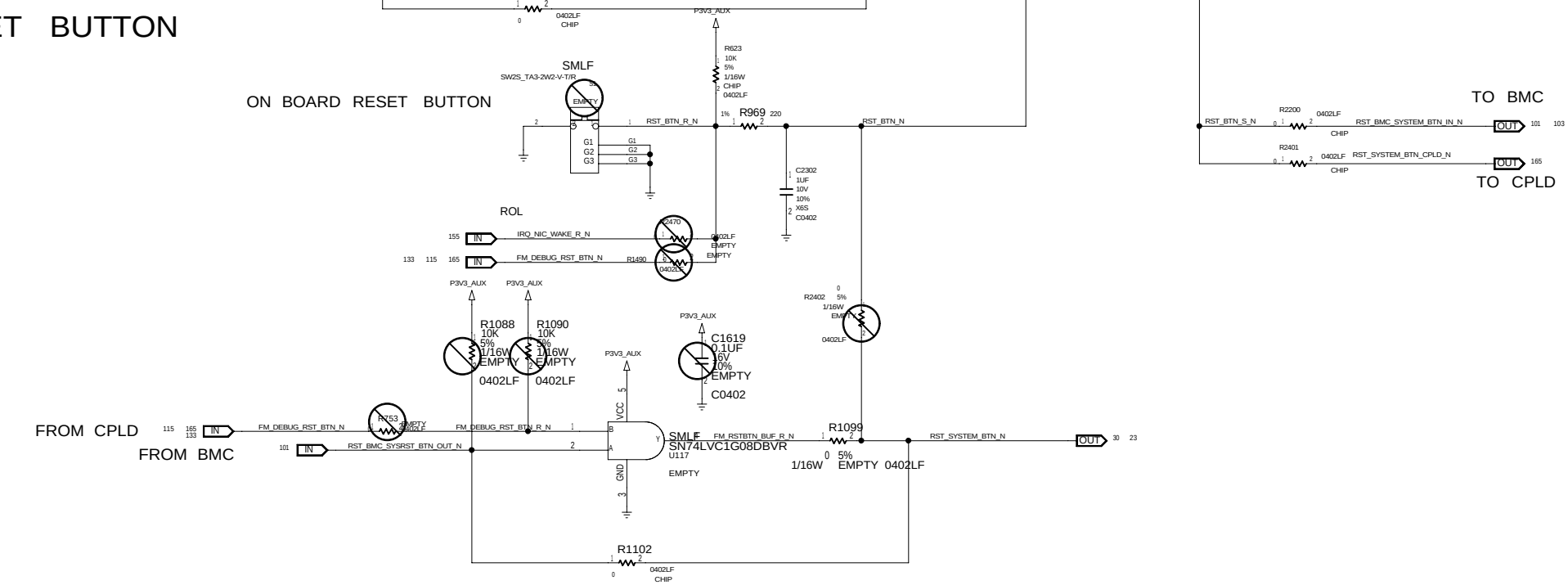
POWER BUTTON

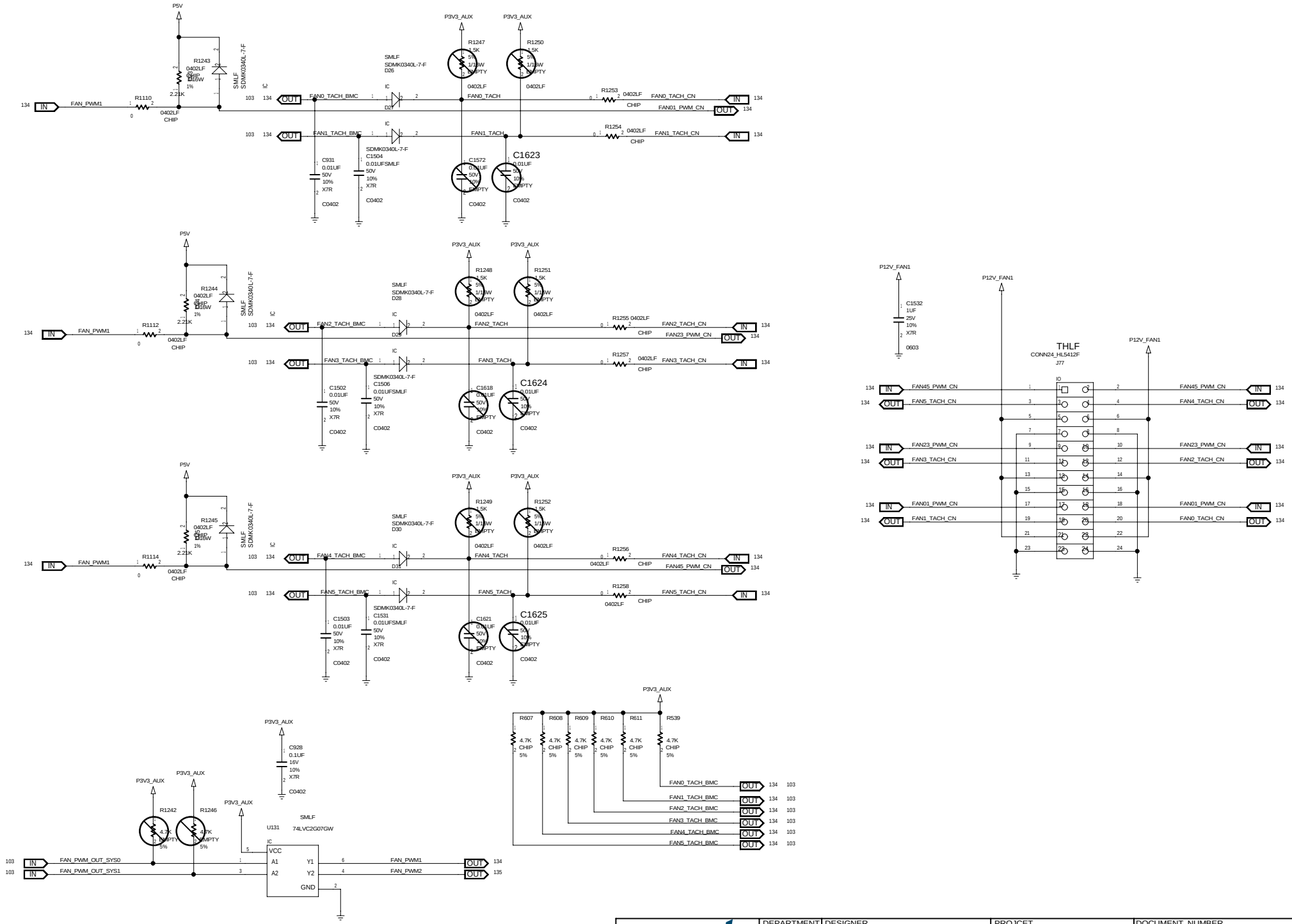


RESET BUTTON



POWER & RESET BUTTON

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:58 2017	SHEET 133 OF 226	



FAN HEADER 1U

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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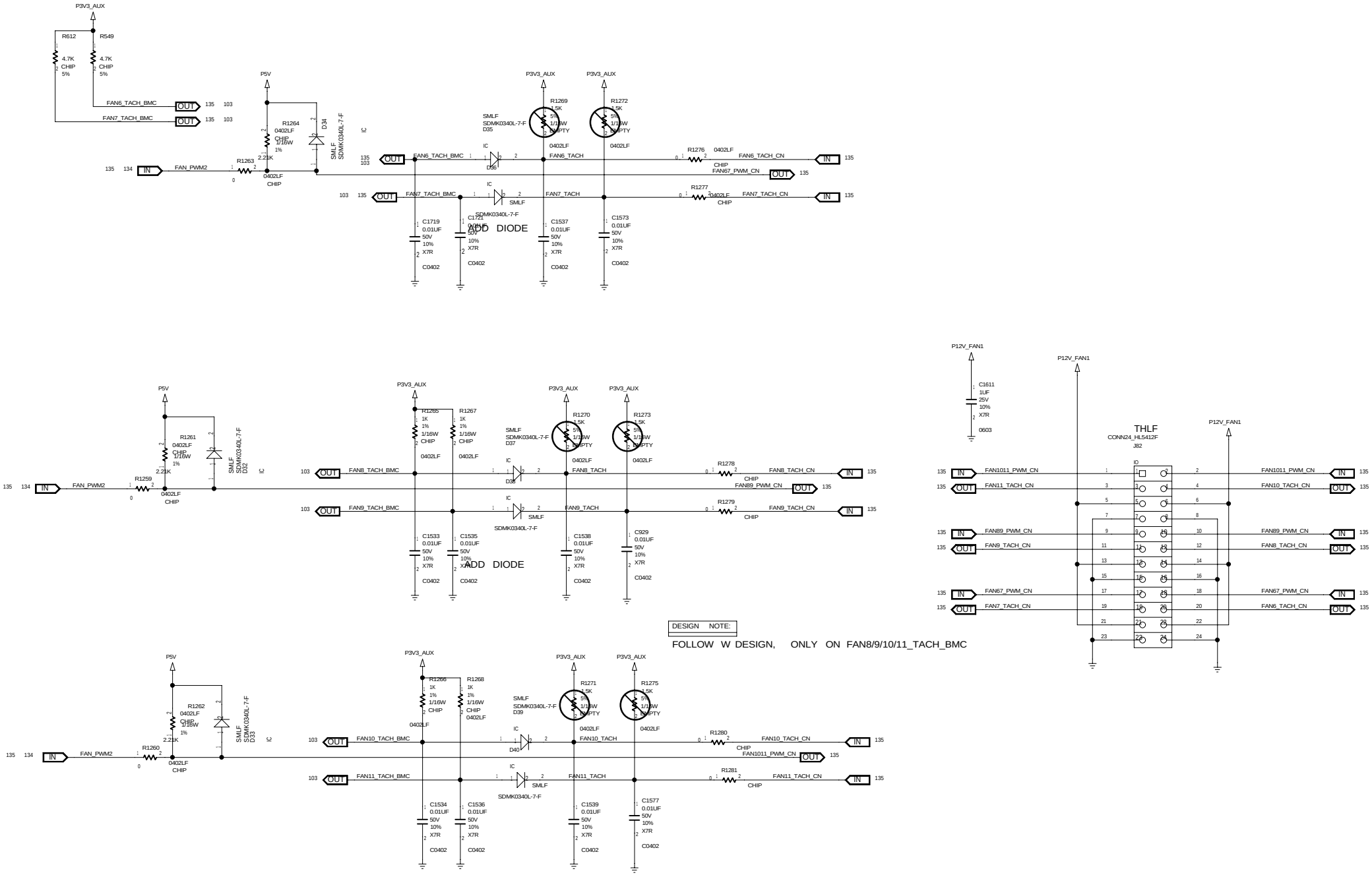
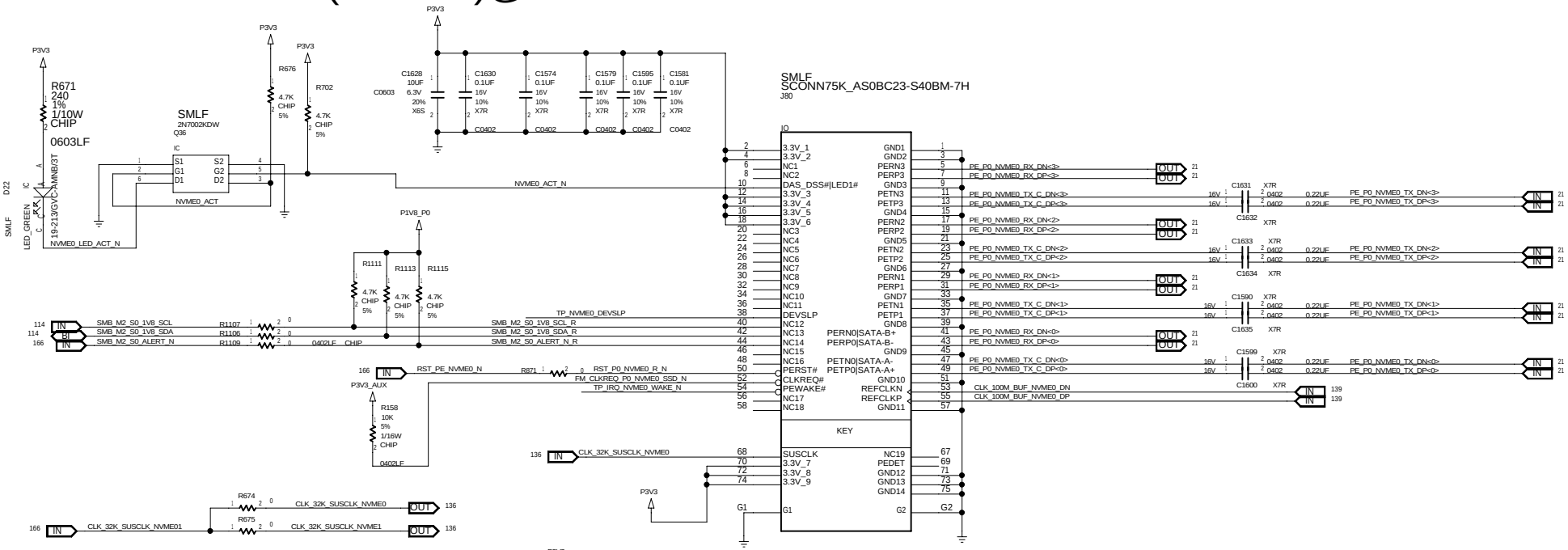


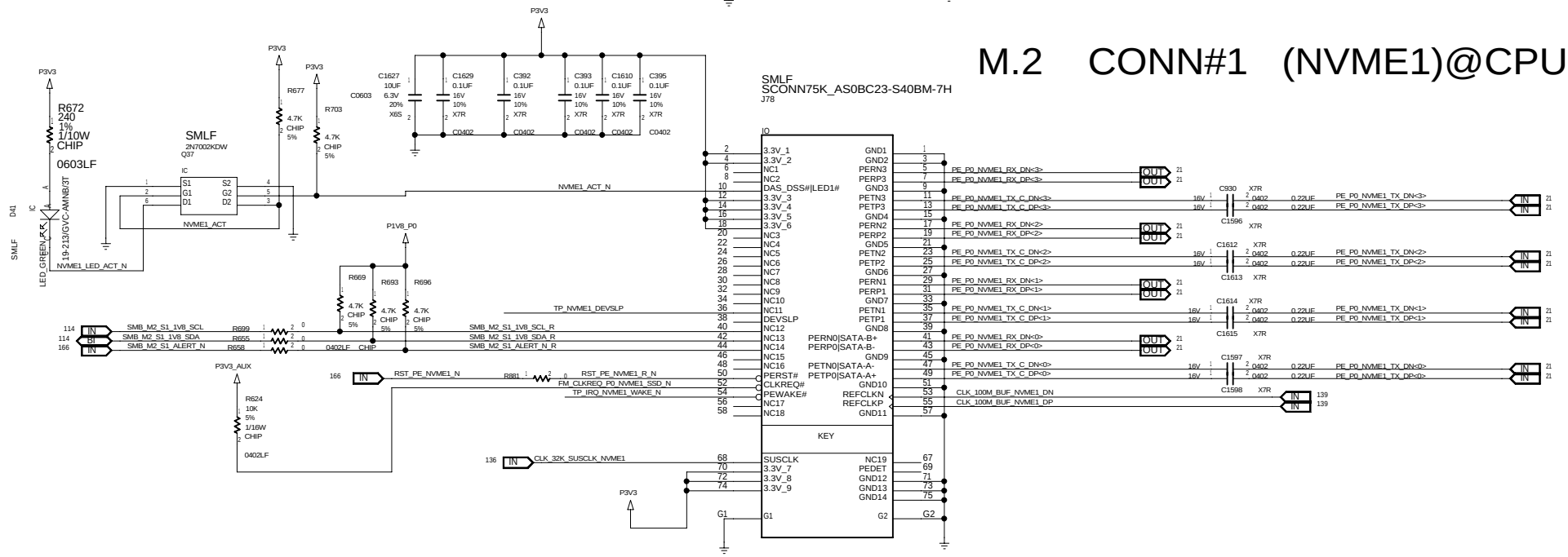
FAN HEADER 2U

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU		<Q_PROJ>	<Q_NUMBER>	<Q_REV>
	REVIEWER	SIZE C DATE Fri Dec 15 20:21:58 2017	SHEET 135 OF 226	

M.2 CONN#0 (NVME0)@CPU0



M.2 CONN#1 (NVME1)@CPU0



M.2 CPU0 CONN

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:17 2017	SHEET 136 OF 226

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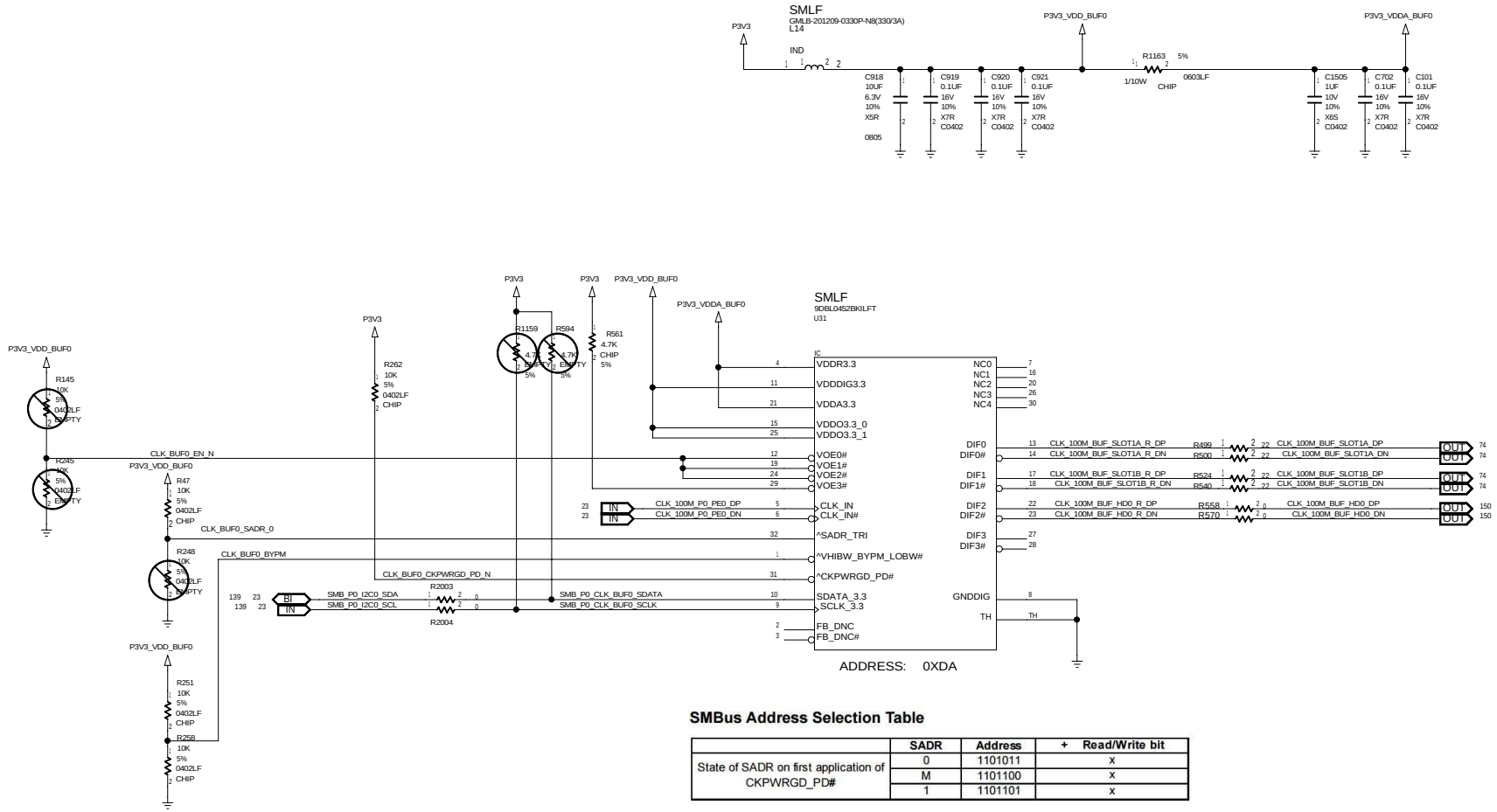
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:42:30 2017	SHEET 137 OF 226

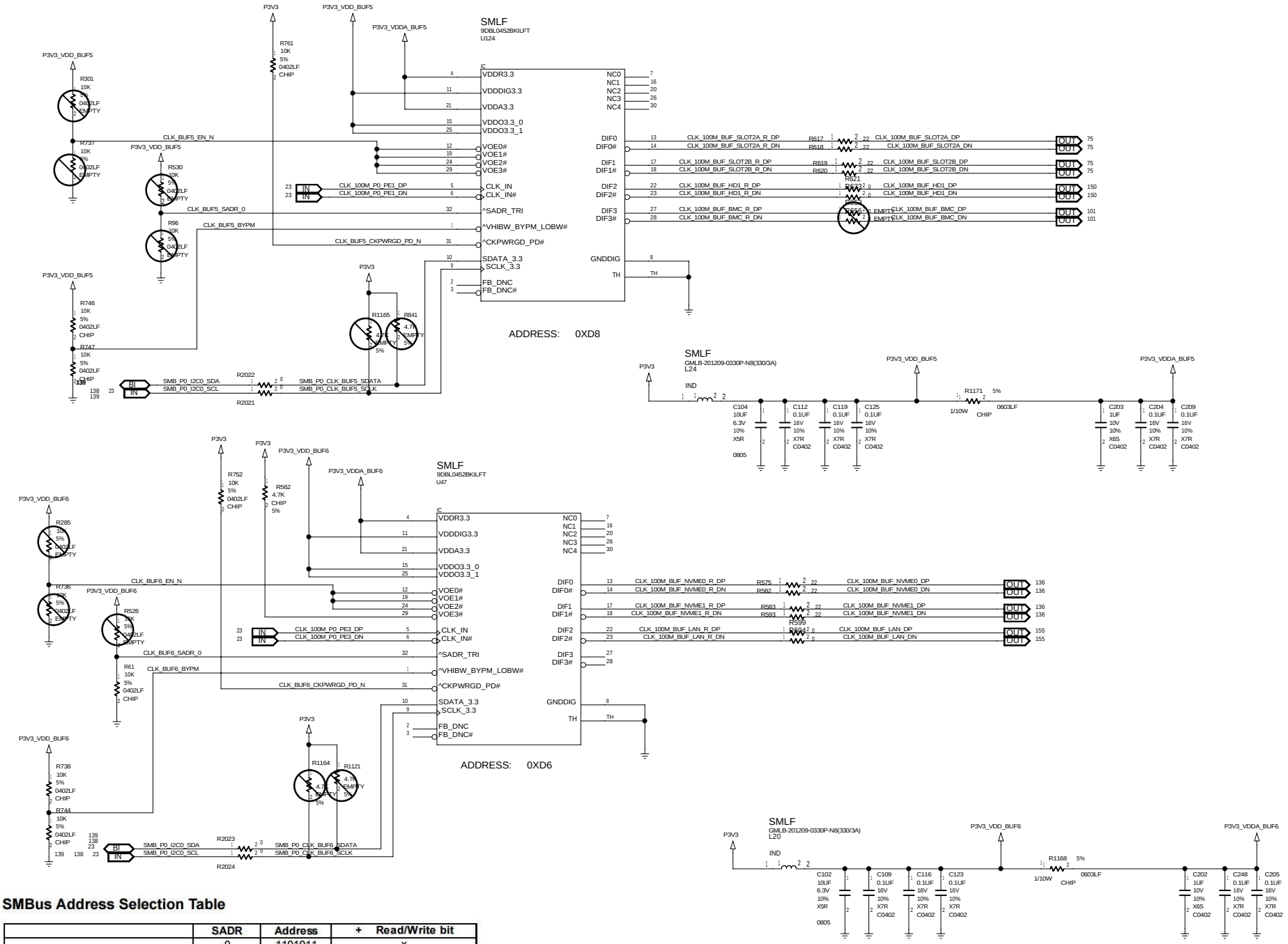


SMBus Address Selection Table

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	x
	M	1101100	x
	1	1101101	x

CLOCK BUF FOR P0 1/2

Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER	SIZE C	DATE Fri Dec 15 20:21:18 2017
			REV <Q_REV>	SHEET 138 OF 226



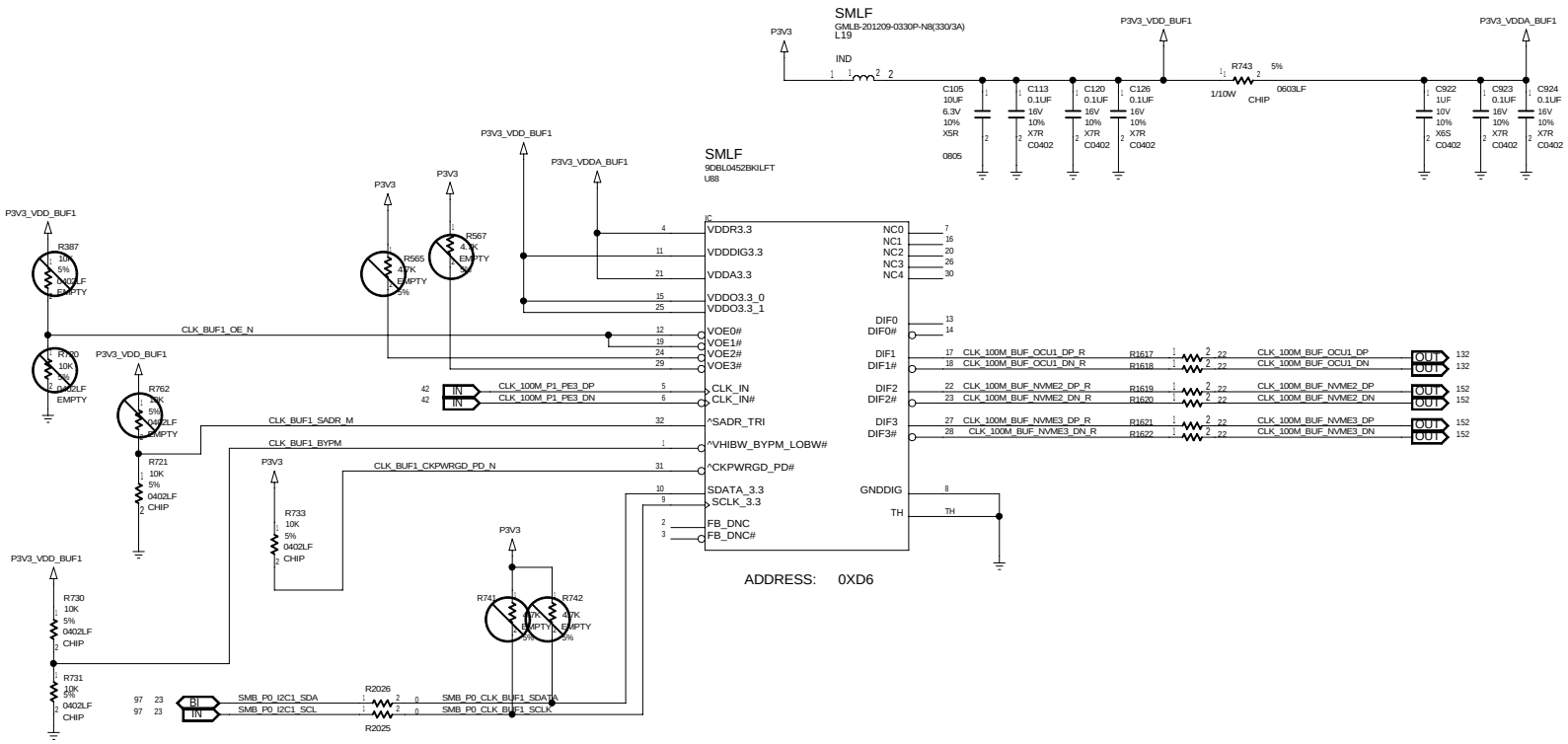
SMBus Address Selection Table

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	x
	M	1101100	x
	1	1101101	x

CLOCK BUF FOR P0 2/2

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:18 2017 SHEET 139 OF 226



CLOCK BUFF FOR P1

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

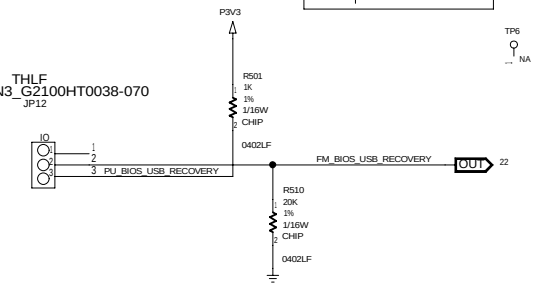
SIZE C DATE Fri Dec 15 20:21:18 2017 SHEET 140 OF 226

BLANK

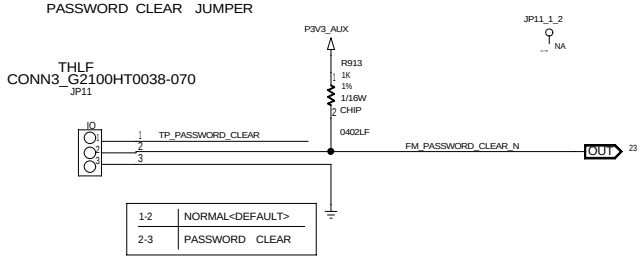
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:34:43 2017	SHEET 141 OF 226

BIOS USB RECOVERY JUMPER

1-2	NORMAL<DEFAULT>
2-3	BIOS USB RECOVERY MODE



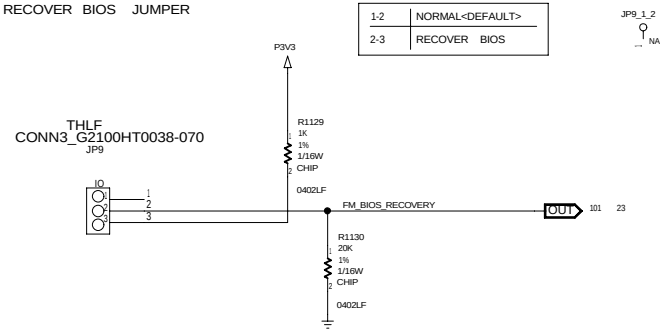
PASSWORD CLEAR JUMPER



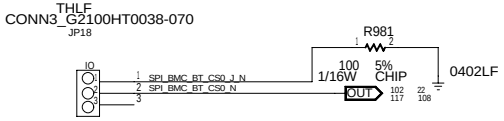
1-2	NORMAL<DEFAULT>
2-3	PASSWORD CLEAR

RECOVER BIOS JUMPER

1-2	NORMAL<DEFAULT>
2-3	RECOVER BIOS



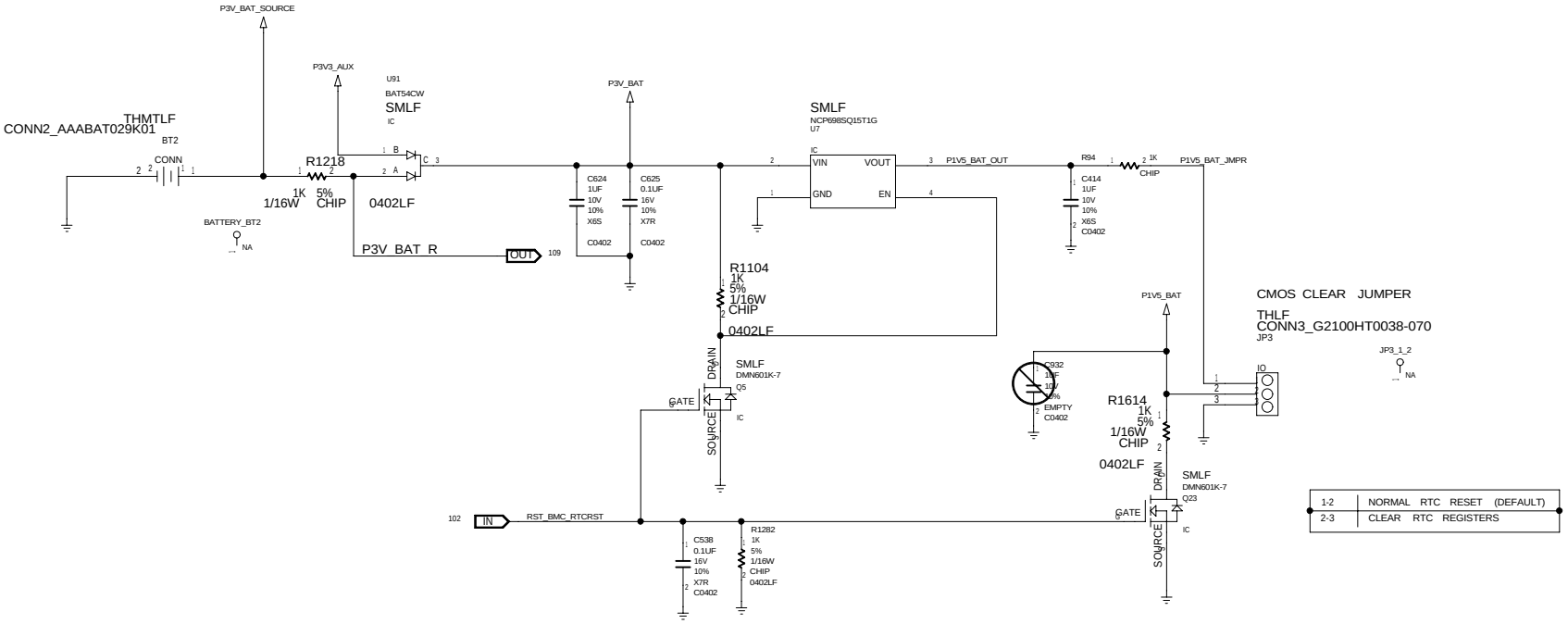
BMC DISABLE JUMPER



FWSPICS0# = 0, DISABLED

JUMPER SETTING

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:24 2017	SHEET 142 OF 226	

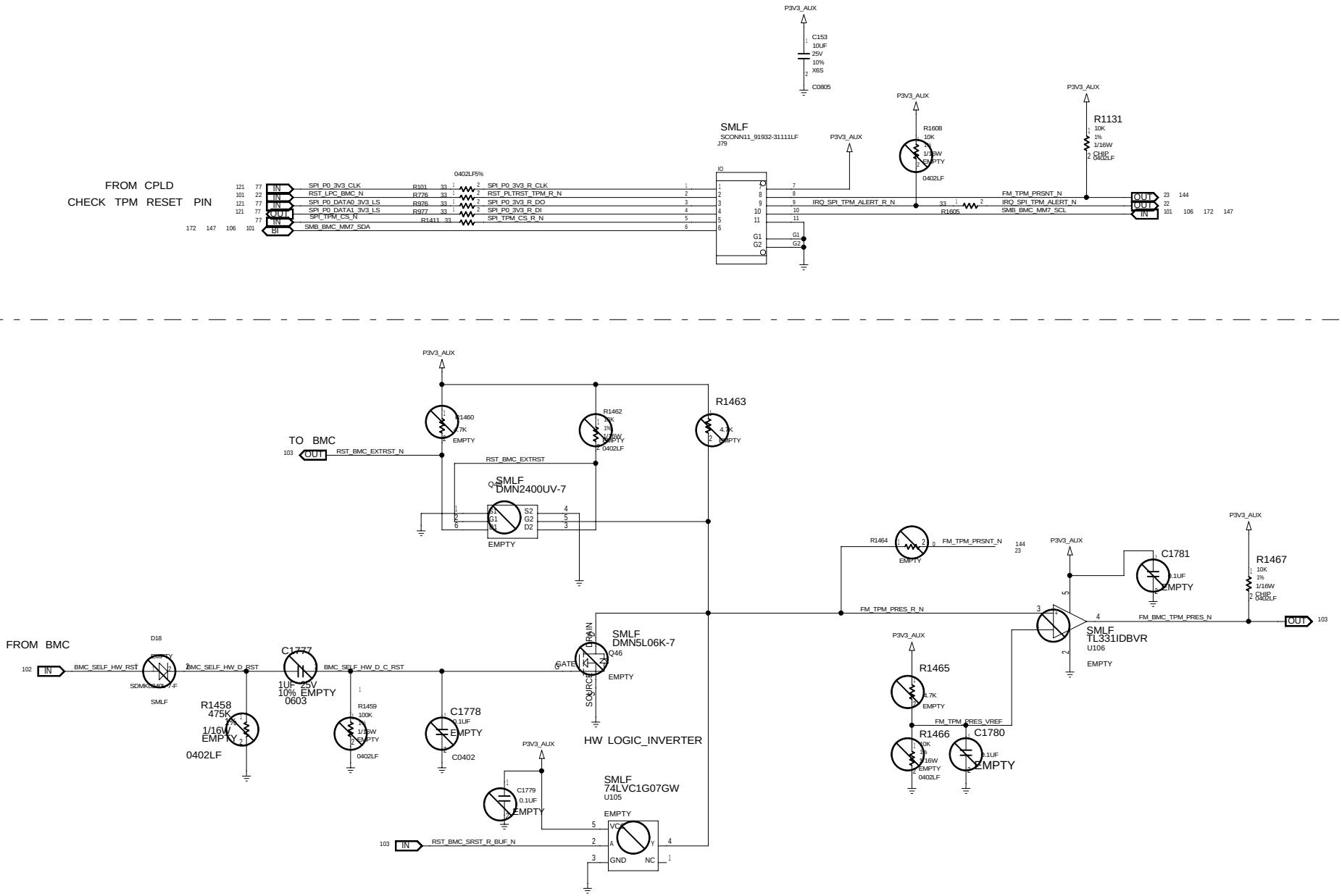


1-2	NORMAL RTC RESET (DEFAULT)
2-3	CLEAR RTC REGISTERS

BATTERY & P1V5_BAT

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:18 2017 SHEET 143 OF 226



TPM CONN

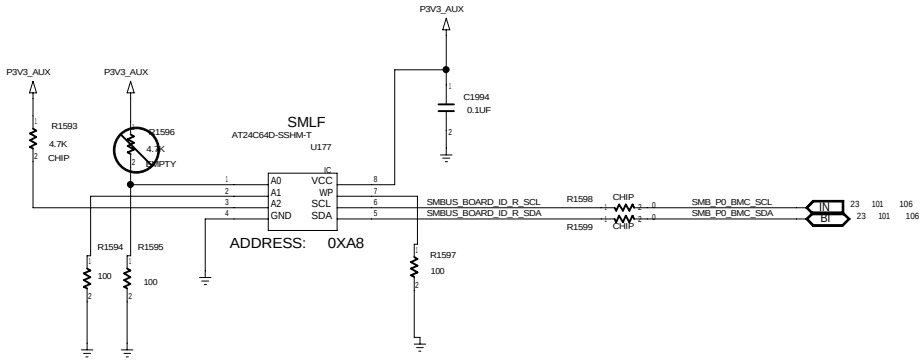
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:21:59 2017 SHEET 144 OF 226

BLANK

Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:34:46 2017	SHEET 145 OF 226

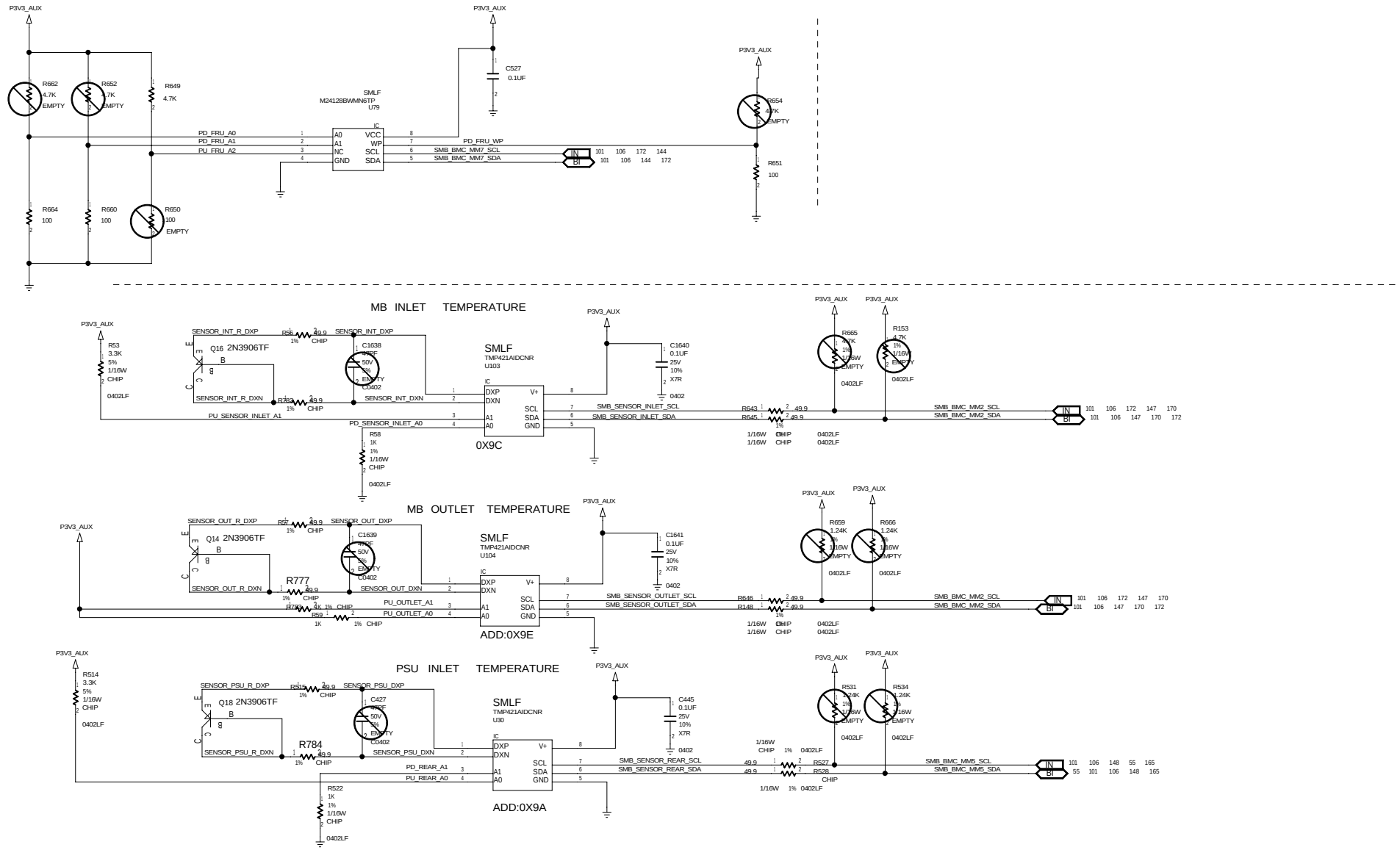
BOARD ID FOR BIOS



BOARD ID for BIOS

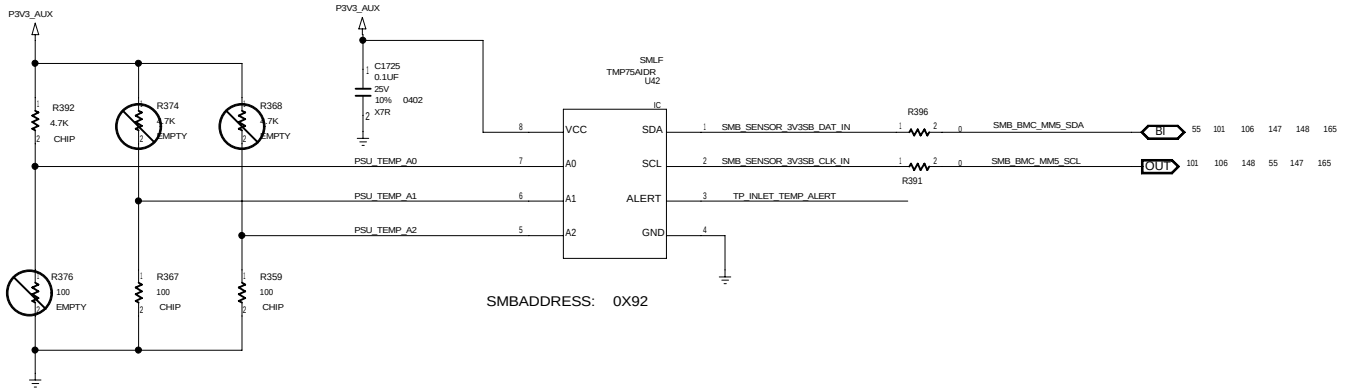
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:18 2017	SHEET 146 OF 226

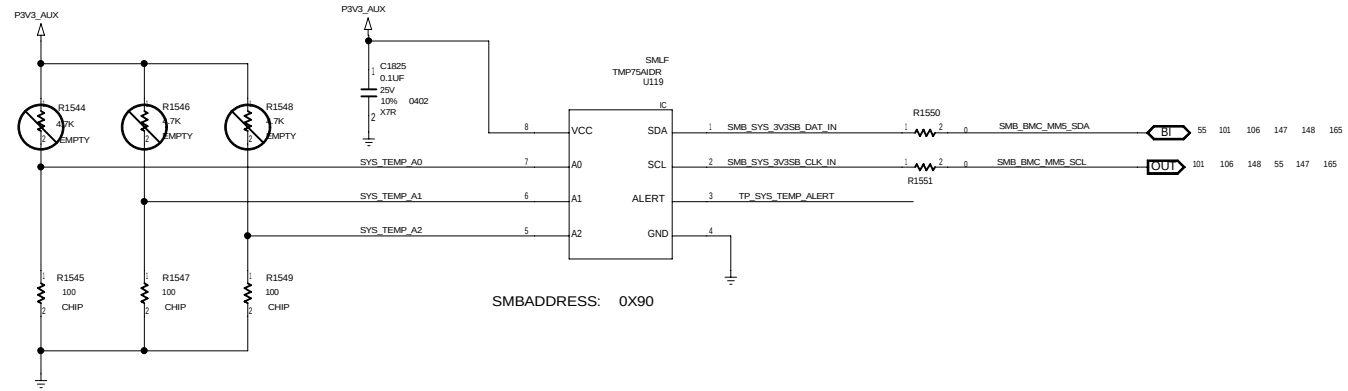
BOARD ID FRU EEPROM
SMBUS ADDRESS: 0XA8



FRU & TEMP SENSOR

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:59 2017	SHEET 147 OF 226





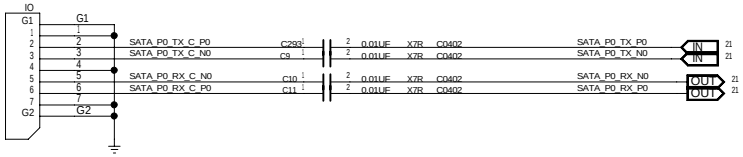
PSU TEMP SENSOR

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:59 2017	SHEET 148 OF 226

SATA0 CONN

BOM NOTE:
WILL CHANGE TO DFHD07MS231

CONN7_ABA-SAT-054-KA4 THLF
J29

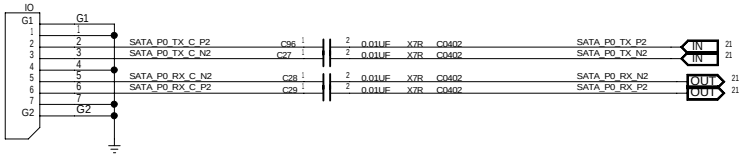


SATA1 CONN

CONN7_ABA-SAT-054-KA4 THLF
J31

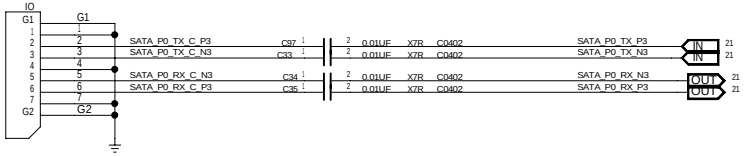
SATA2 CONN

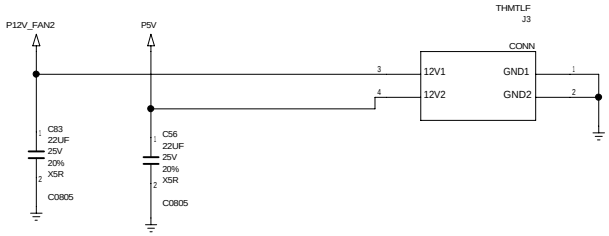
CONN7_ABA-SAT-054-KA4 THLF
J33

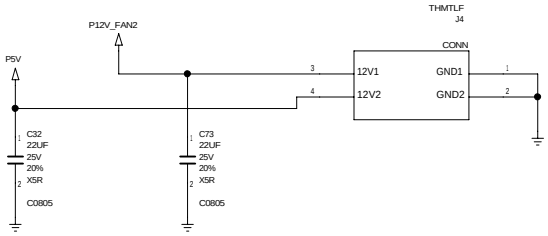


SATA3 CONN

CONN7_ABA-SAT-054-KA4 THLF
J34



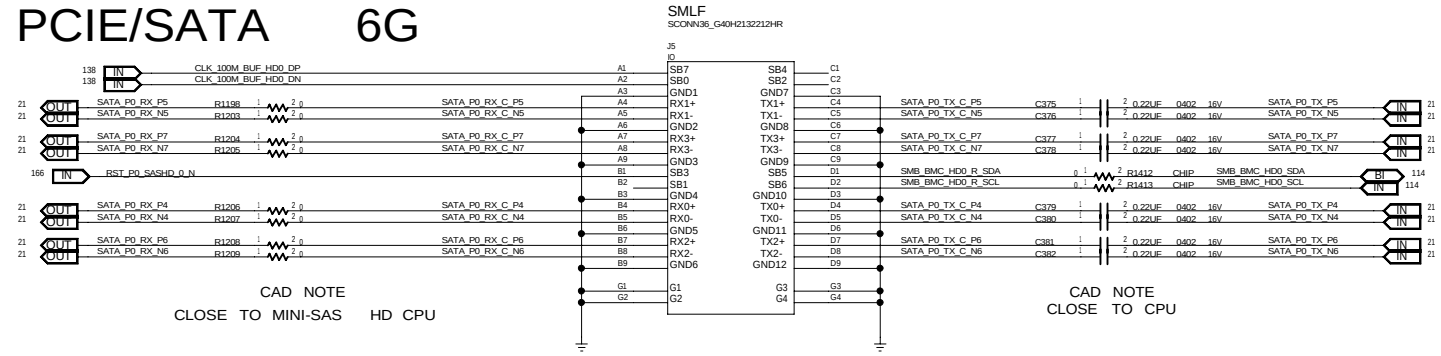




SATA CONN

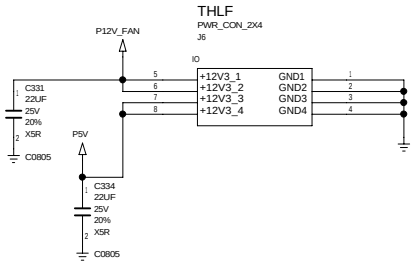
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:59 2017	SHEET 149 OF 226	

PCIE/SATA 6G

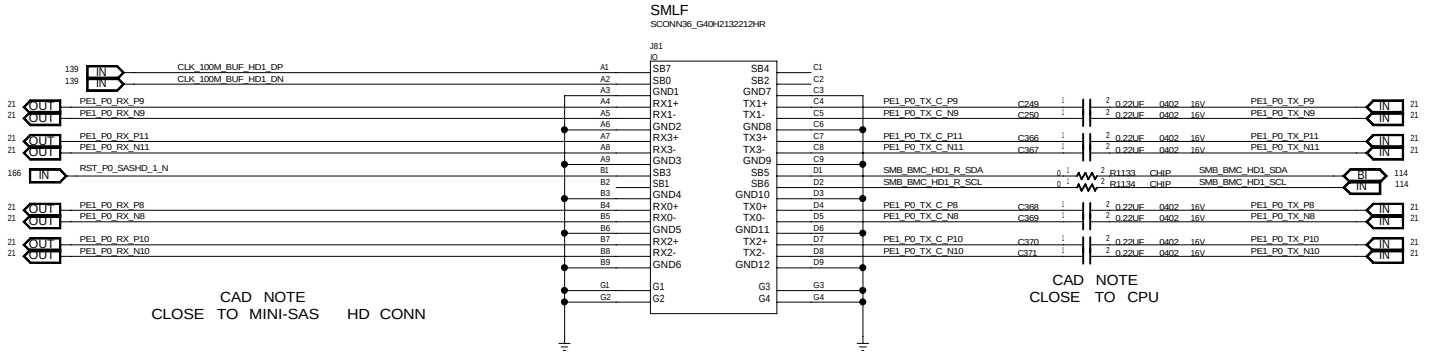


MINI-SAS HD 0

BOM NOTE:
WILL CHANGE TO DFHS36FS109

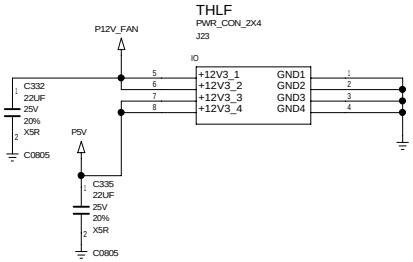


PCIE ONLY



MINI-SAS HD 1

BOM NOTE:
WILL CHANGE TO DFHS36FS109



MINISAS HD FOR CPU0

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:59 2017	SHEET 150 OF 226	

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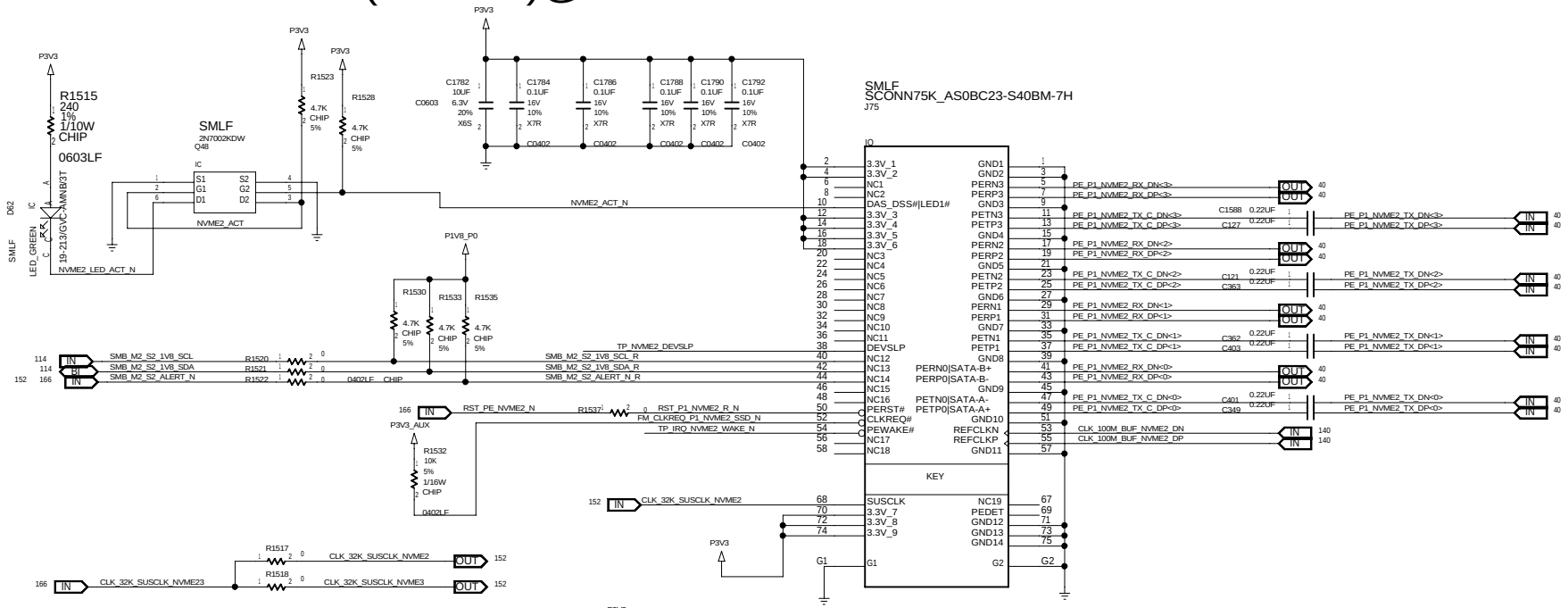
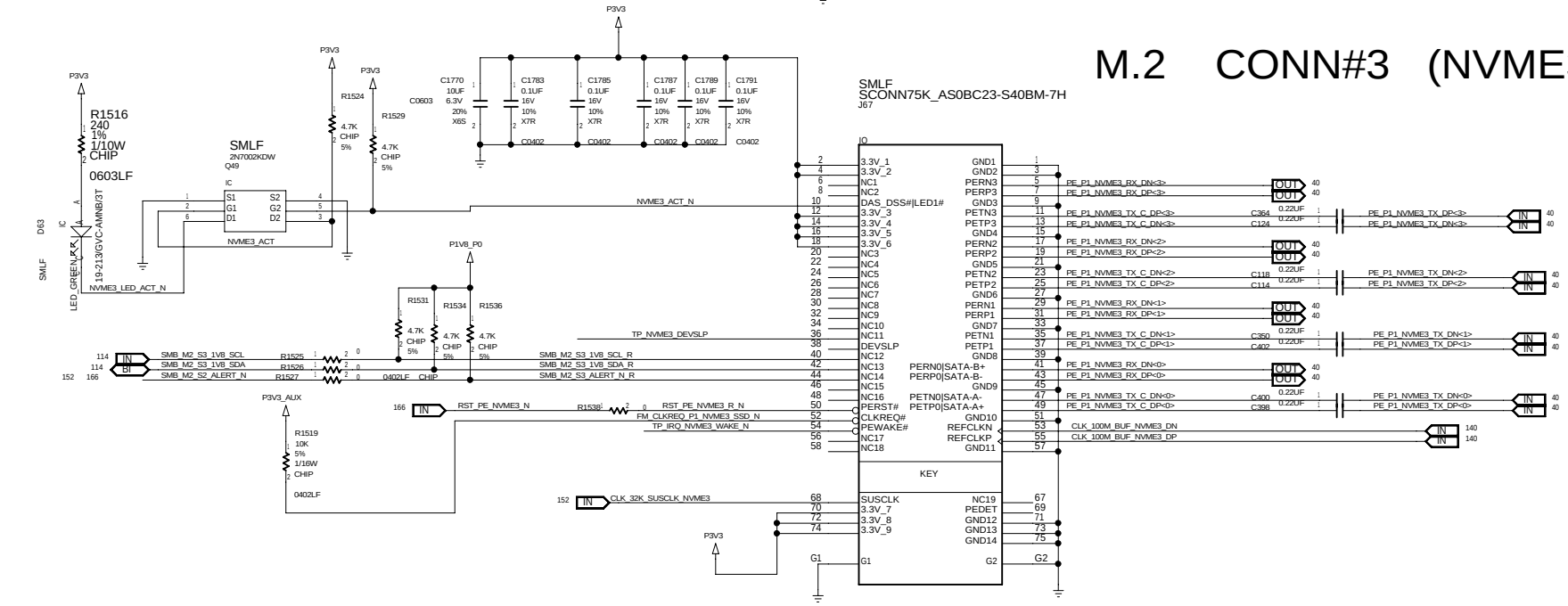
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:34:53 2017	SHEET 151 OF 226

M.2 CONN#2 (NVME2)@CPU1



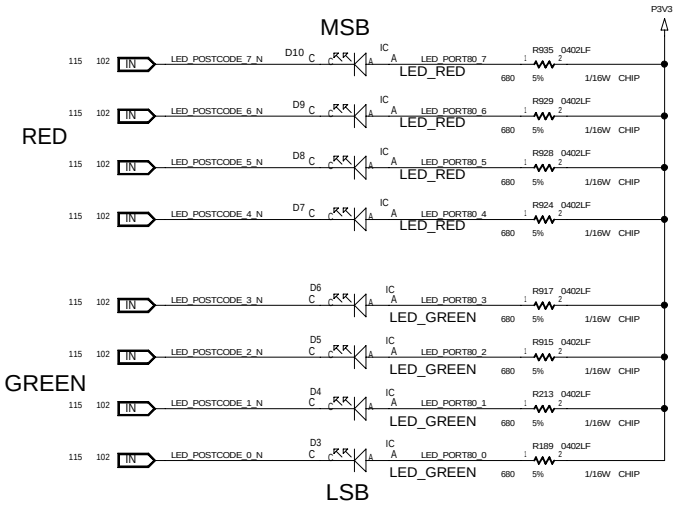
M.2 CONN#3 (NVME3)@CPU1



M.2 CONN 2/3

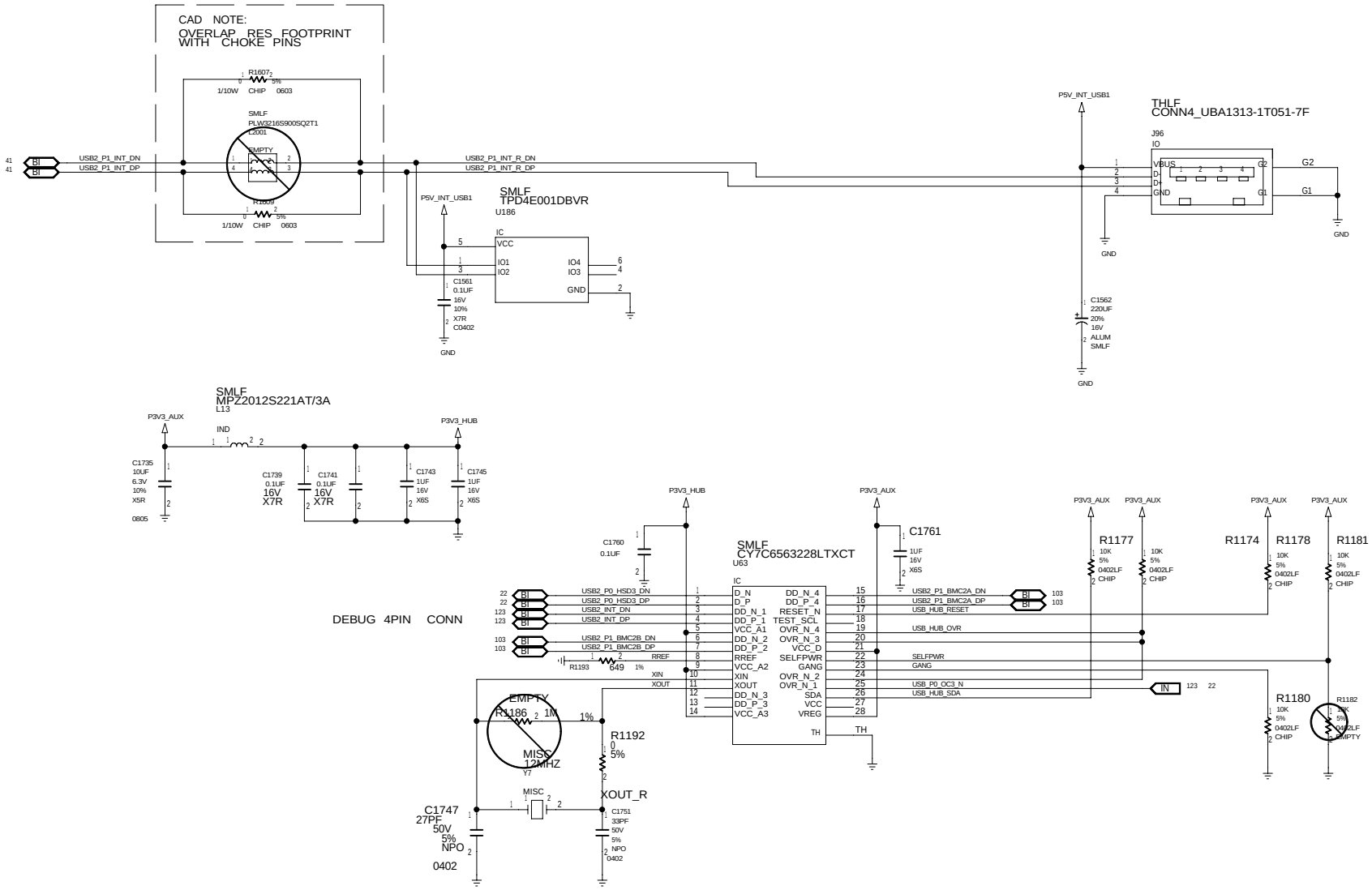
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:21 2017	SHEET 152 OF 226

DEBUG PORT 80 LED



PORT80 LED

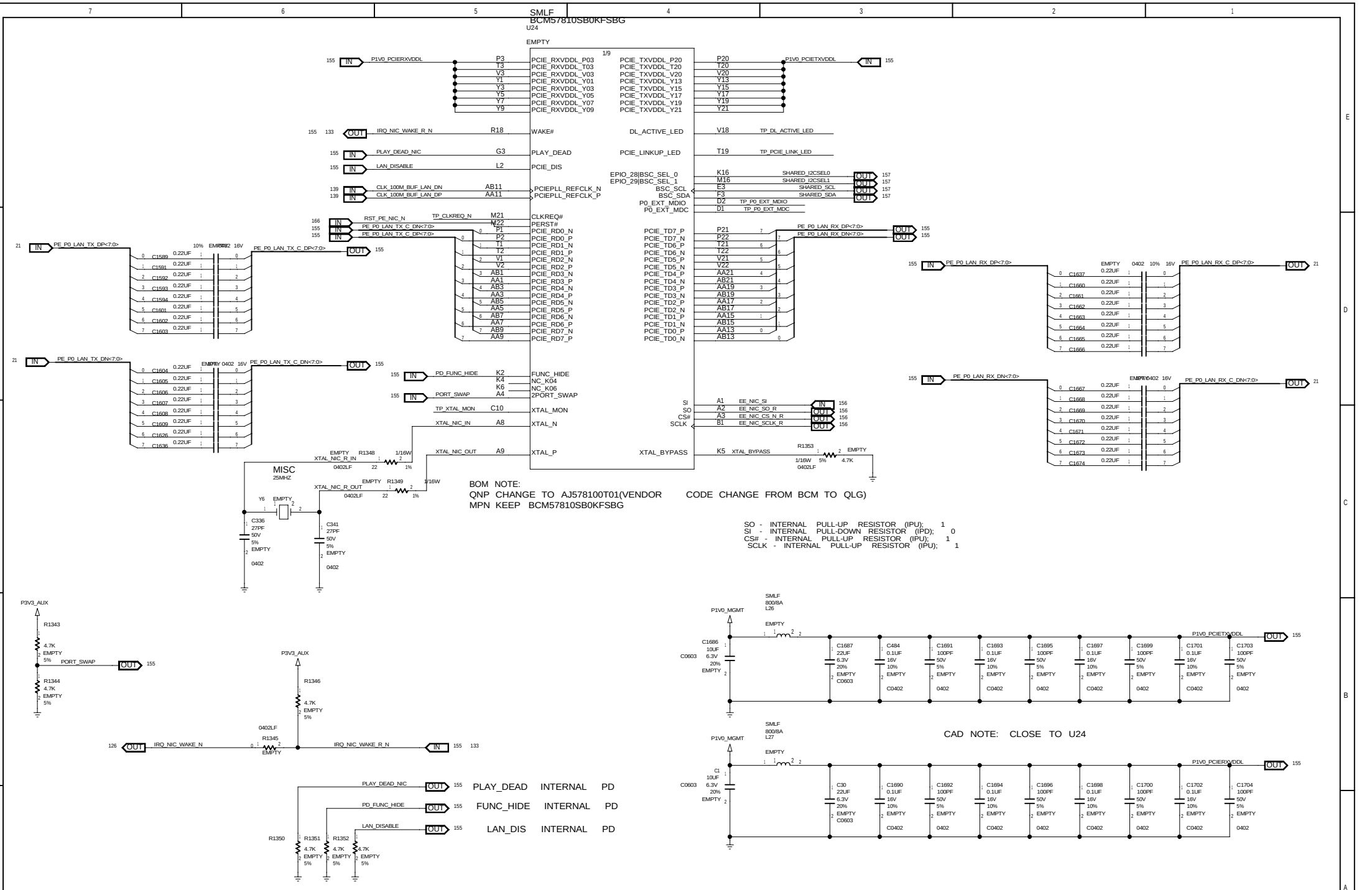
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 20:22:00 2017	SHEET 153 OF 226



USB2.0 INTERNAL

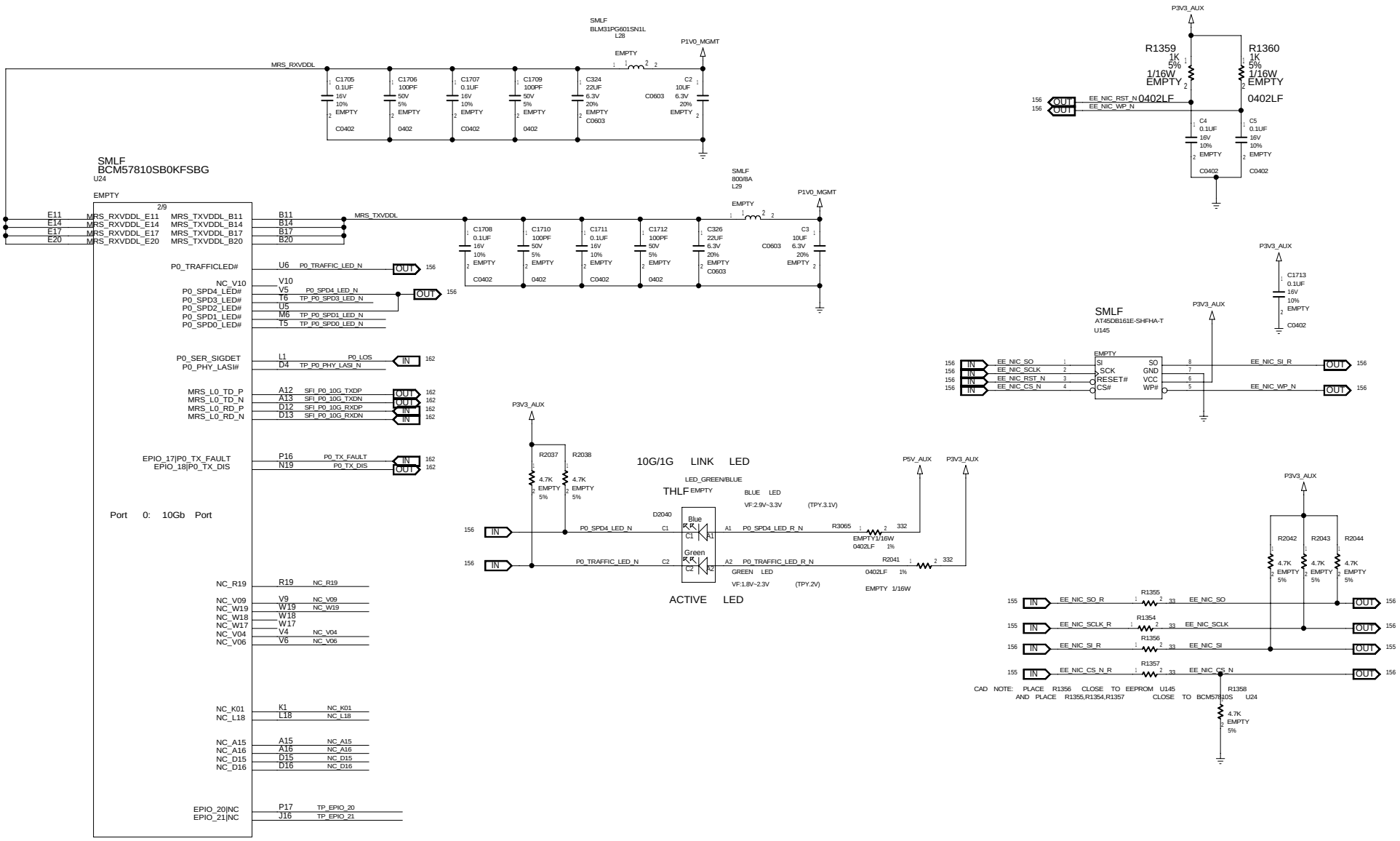
Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:22:00 2017 SHEET 154 OF 226



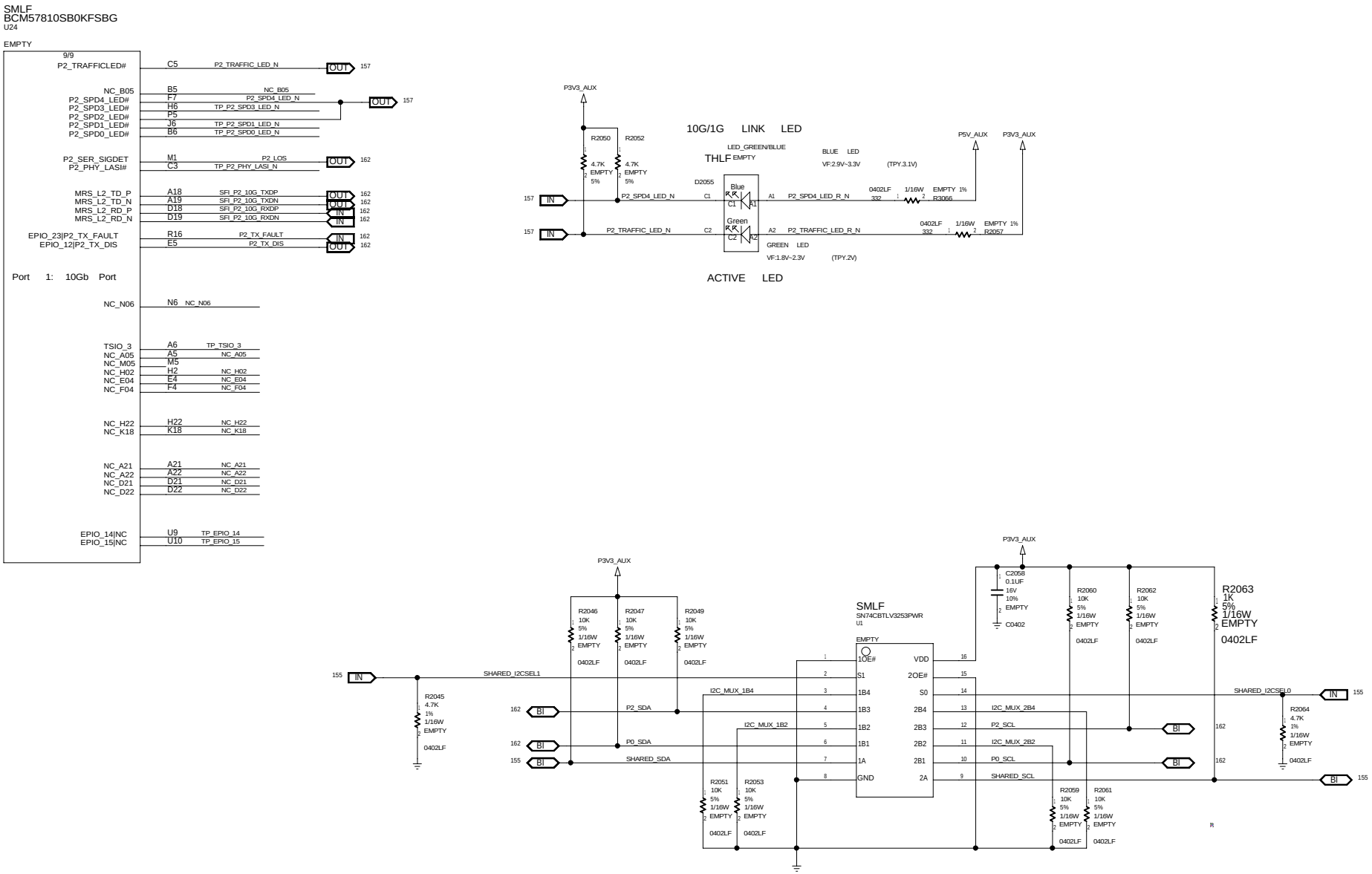
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:22:00 2017 SHEET 155 OF 226



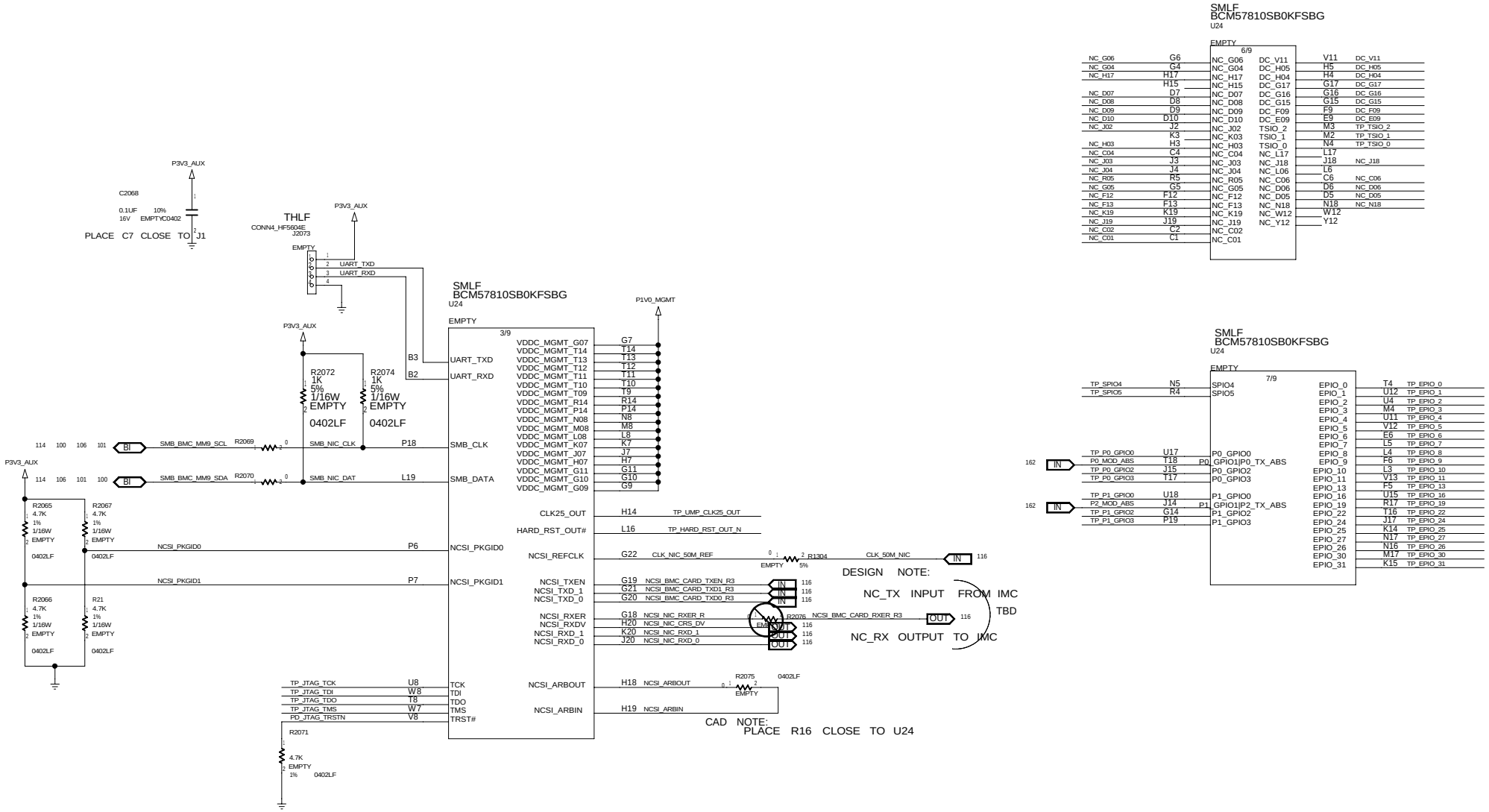
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:22:00 2017 SHEET 156 OF 226



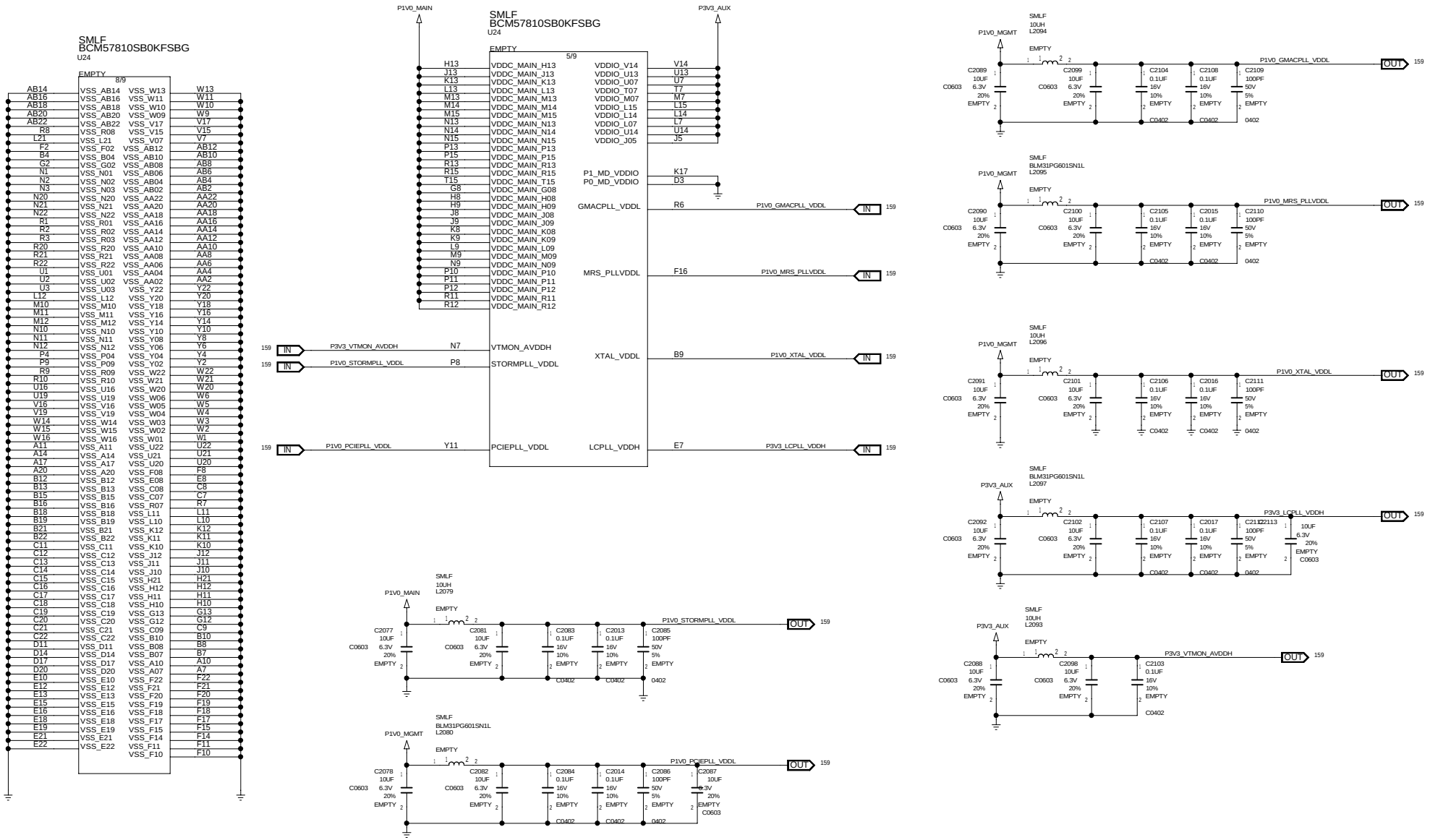
BCM57810 3 of 10

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
			SIZE C	DATE Fri Dec 15 20:22:01 2017	SHEET 157 OF 226



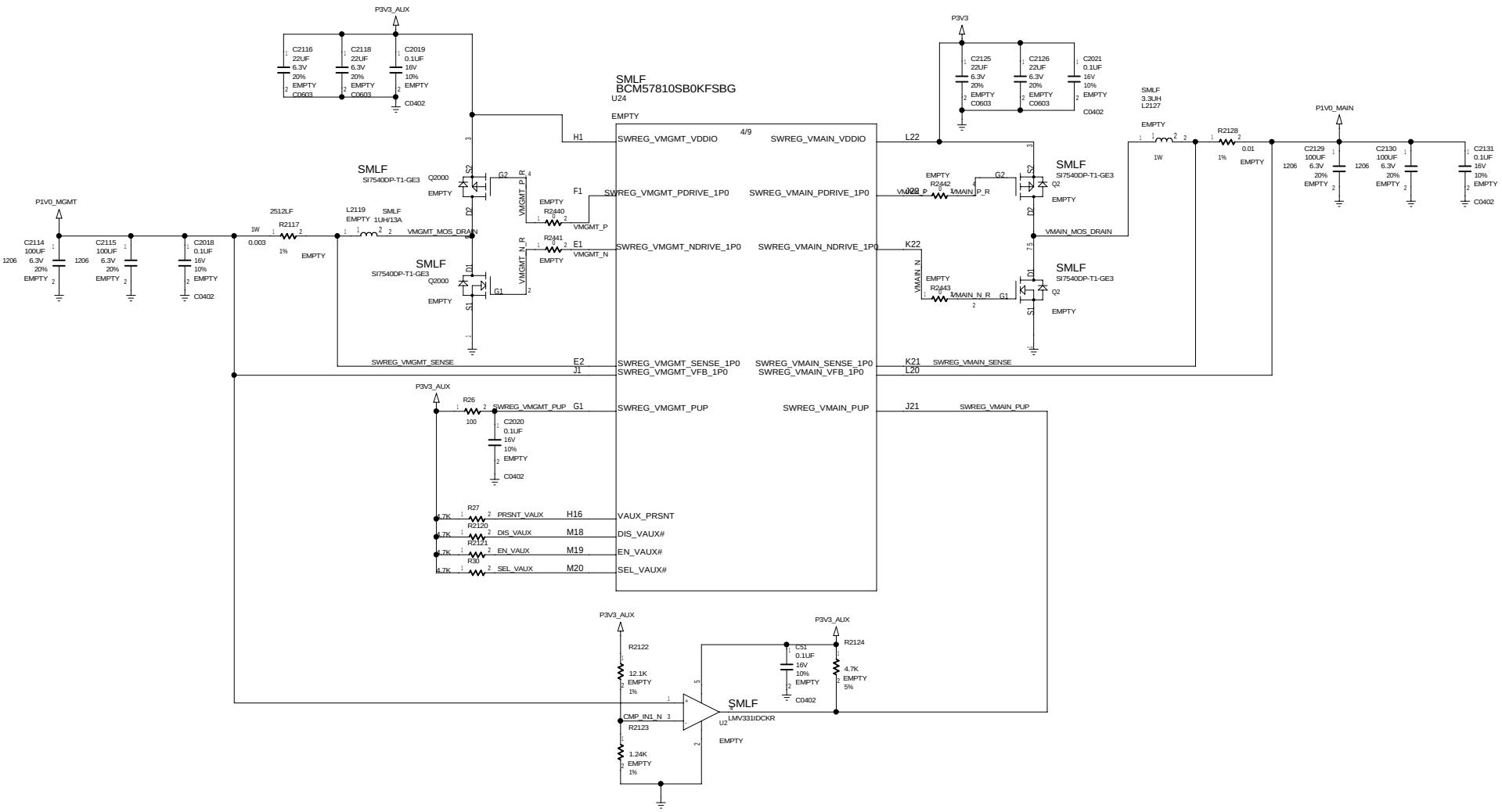
DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

SIZE C DATE Fri Dec 15 20:22:01 2017 SHEET 158 OF 226



DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

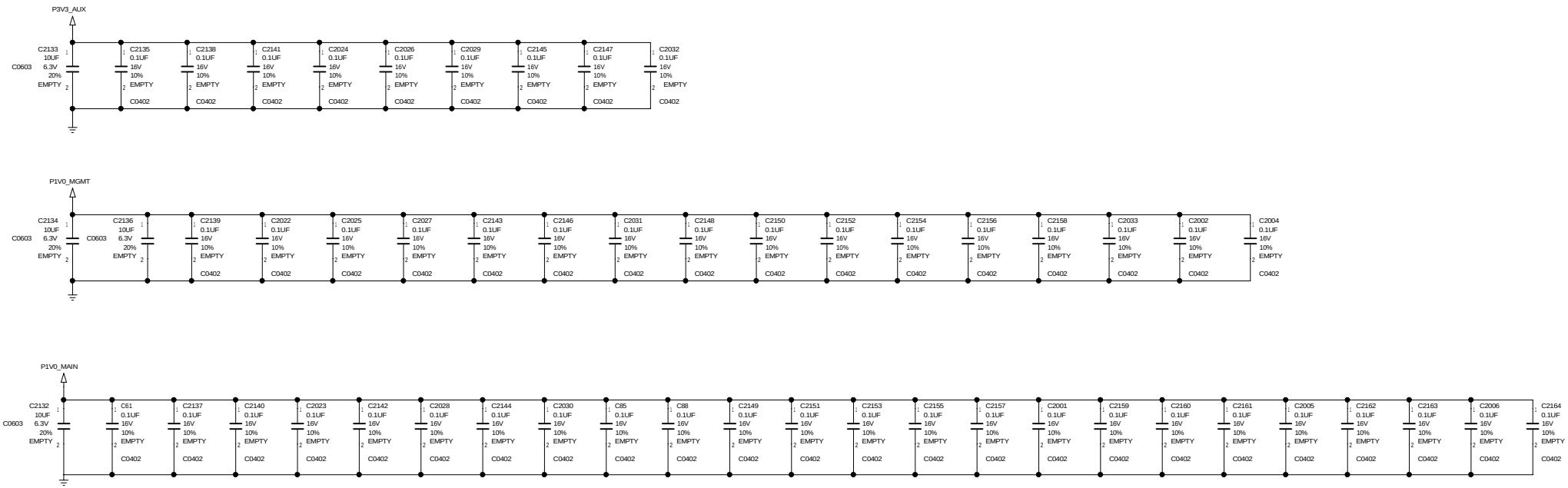
SIZE C DATE Fri Dec 15 20:22:01 2017 SHEET 159 OF 226



DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

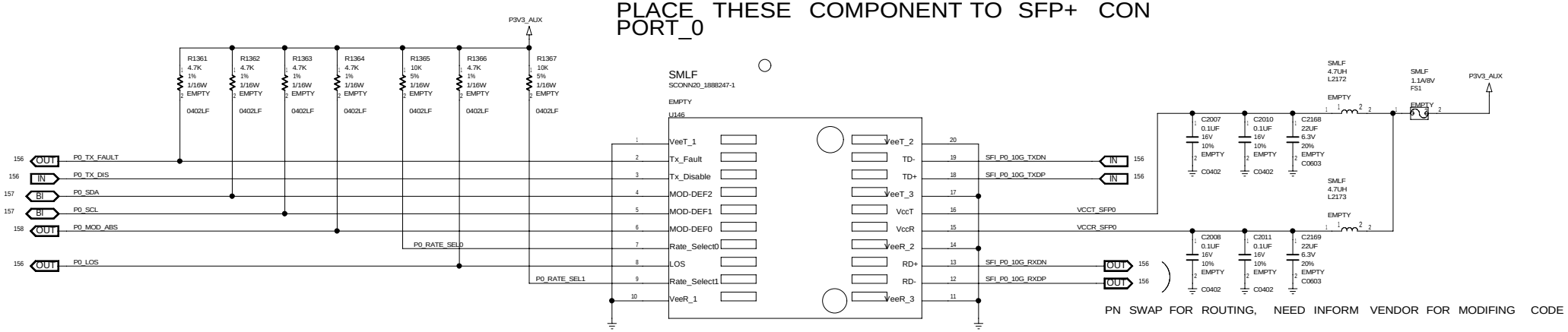
SIZE C DATE Fri Dec 15 20:22:01 2017 SHEET 160 OF 226

CAD NOTE: PLACE THESE CAPACITORS IN THIS PAGE CLOSE TO U24



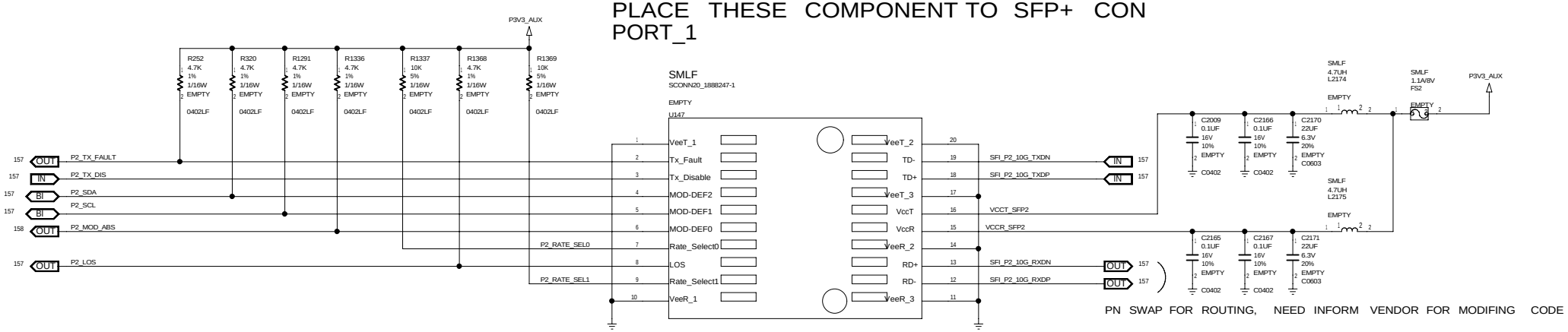
Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
			SIZE C	DATE Fri Dec 15 20:22:02 2017	SHEET 161 OF 226

PLACE THESE COMPONENT TO SFP+ CON PORT_0



PN SWAP FOR ROUTING, NEED INFORM VENDOR FOR MODIFING CODE

PLACE THESE COMPONENT TO SFP+ CON PORT_1



PN SWAP FOR ROUTING, NEED INFORM VENDOR FOR MODIFING CODE

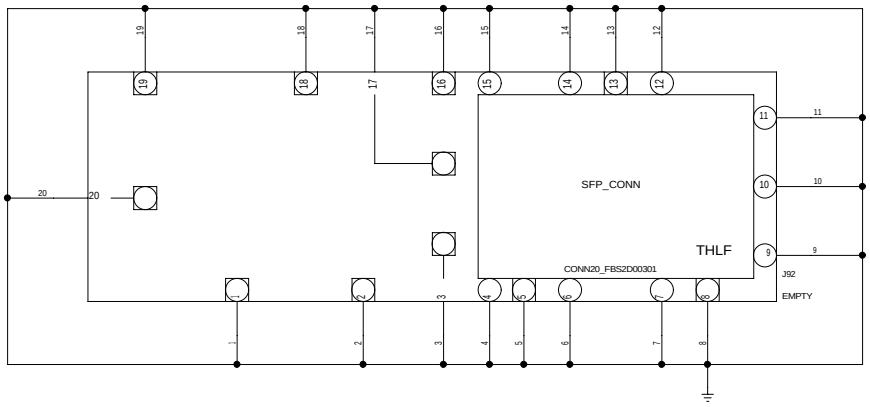
HEATSINK FOR BCM57810

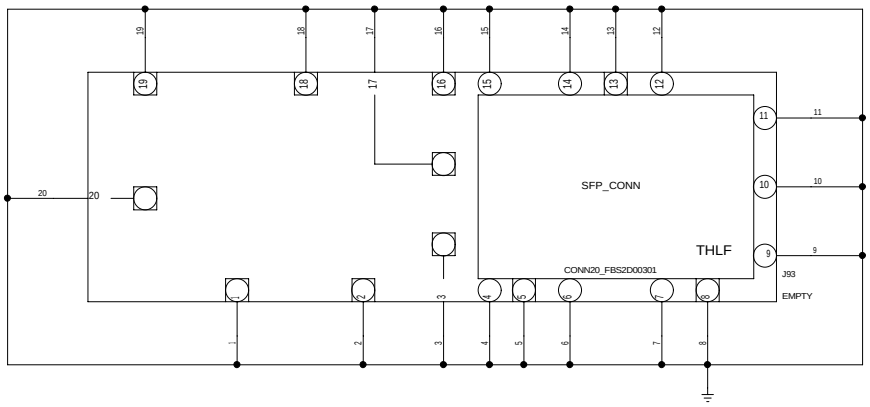
TP93
EMPTY

HEATSINK SCREW

TH
H2176
EMPTY

TH
H2179
EMPTY





Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:22:02 2017	SHEET 163 OF 226	

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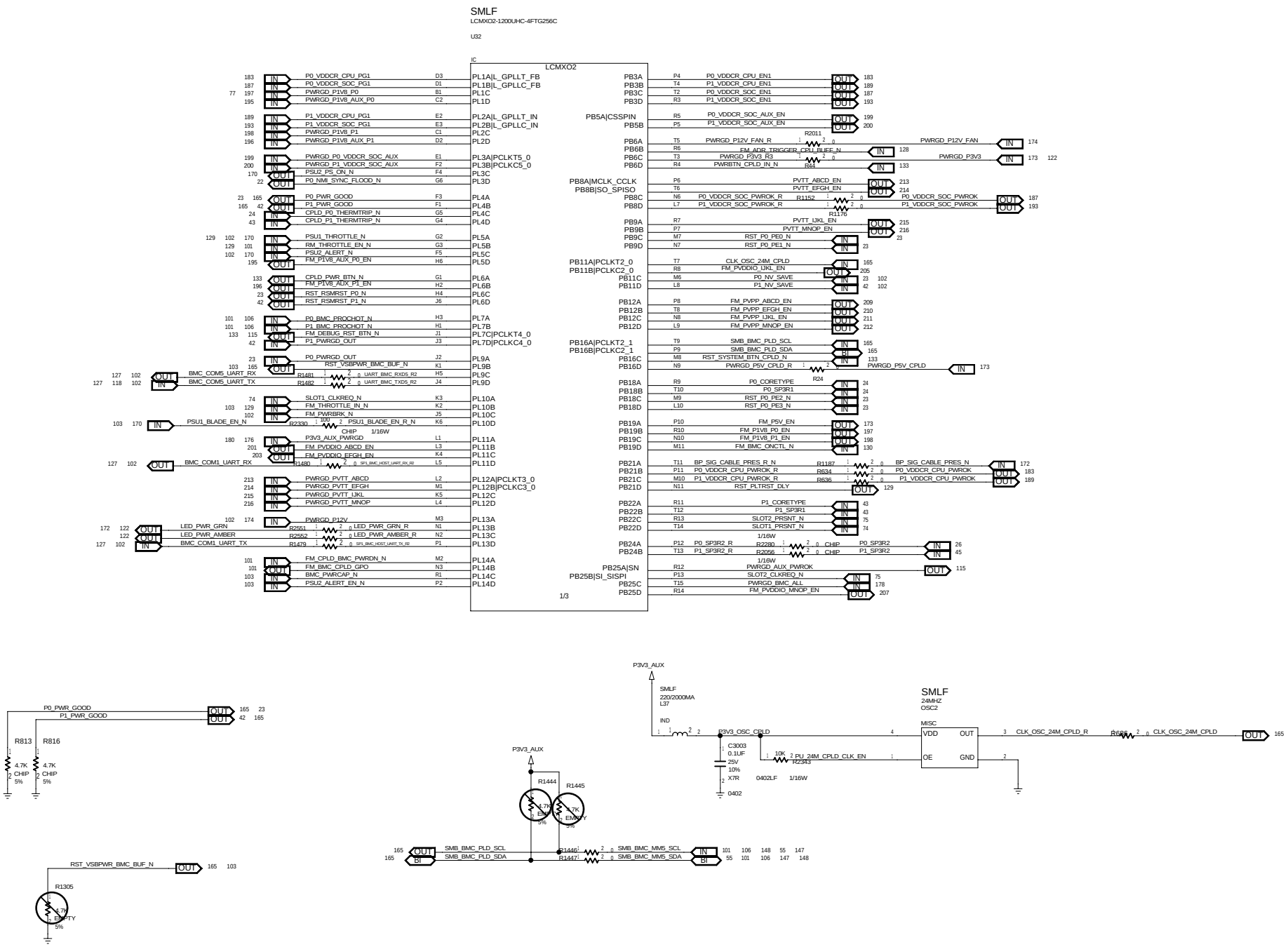
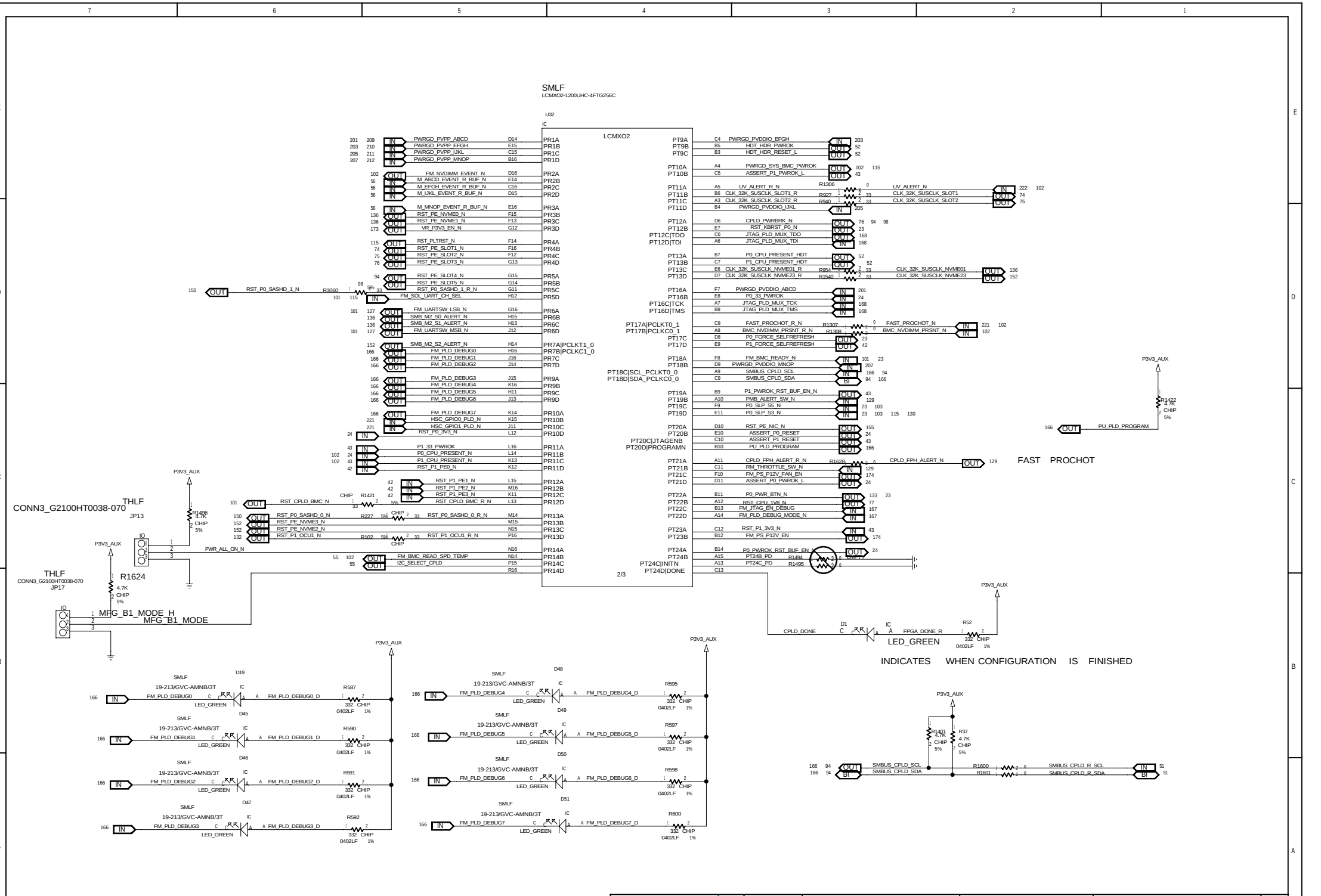
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:42:48 2017	SHEET 164 OF 226



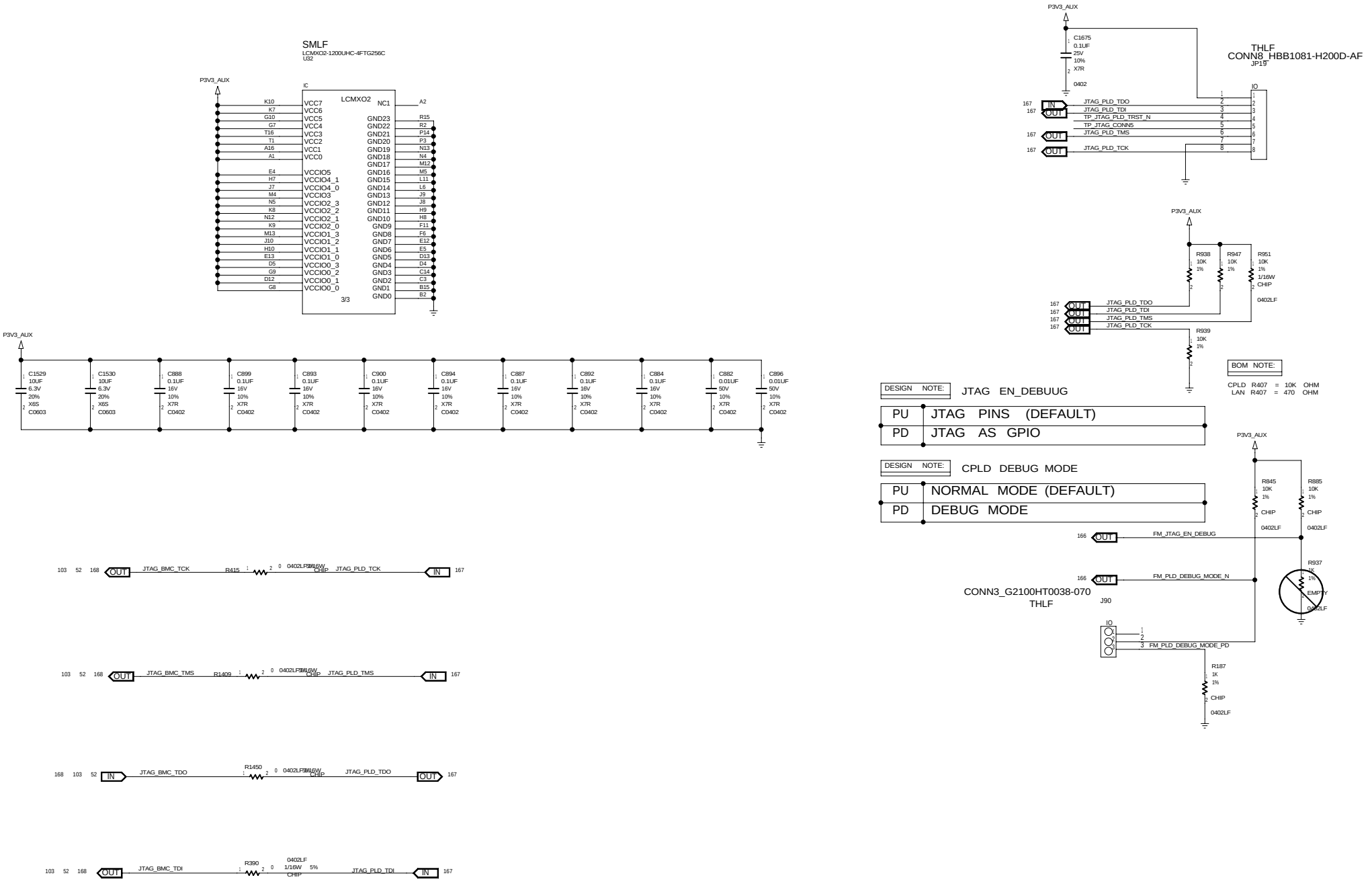
CPLD 1/3

Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 20:22:02 2017	SHEET 165 OF 226



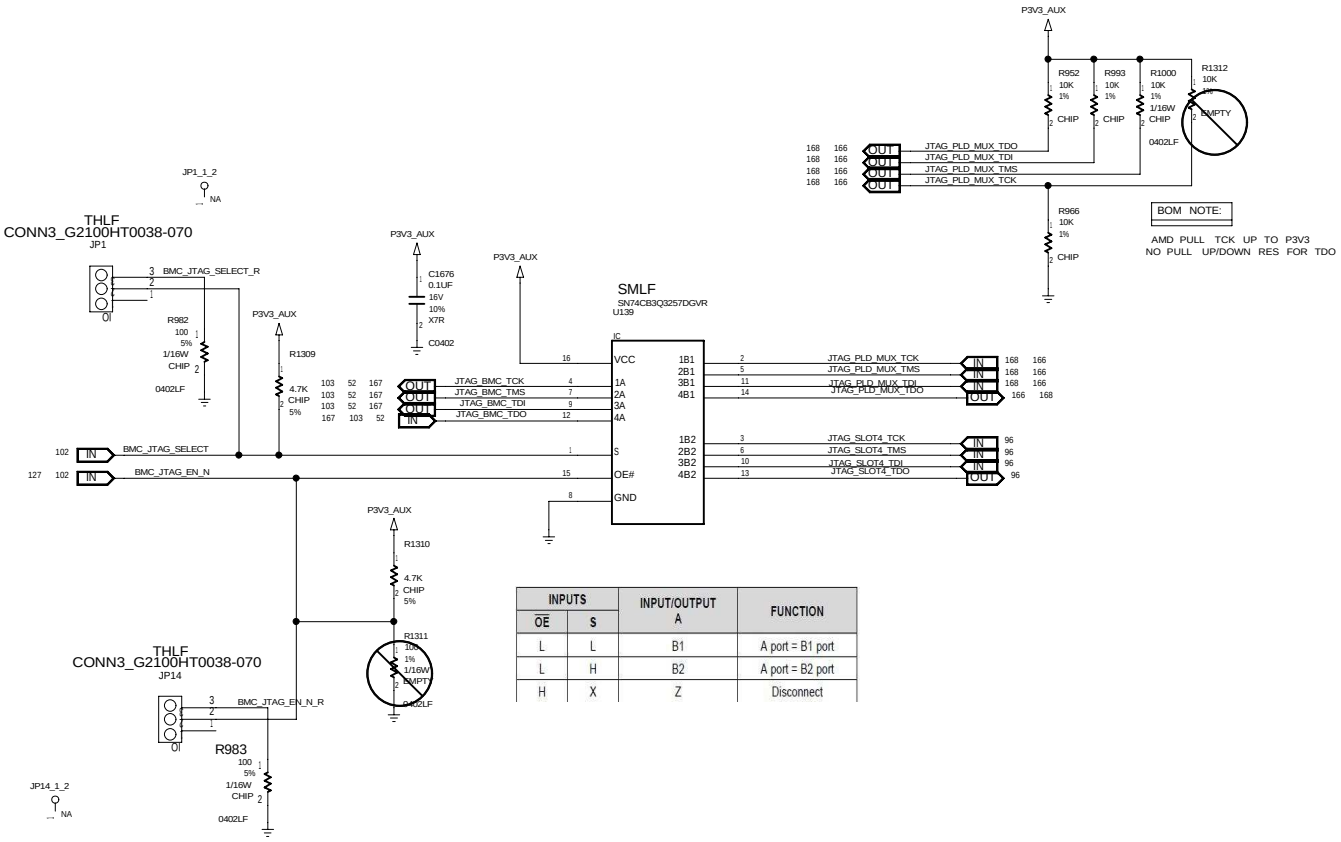
CPLD 2/3

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:21:24 2017	SHEET 166 OF 226



CPLD 3/3

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:22:02 2017	SHEET 167 OF 226



INPUTS		INPUT/OUTPUT A	FUNCTION
$\overline{OE}$	S		
L	L	B1	A port = B1 port
L	H	B2	A port = B2 port
H	X	Z	Disconnect

BMC JTAG

Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 20:22:02 2017	SHEET 168 OF 226

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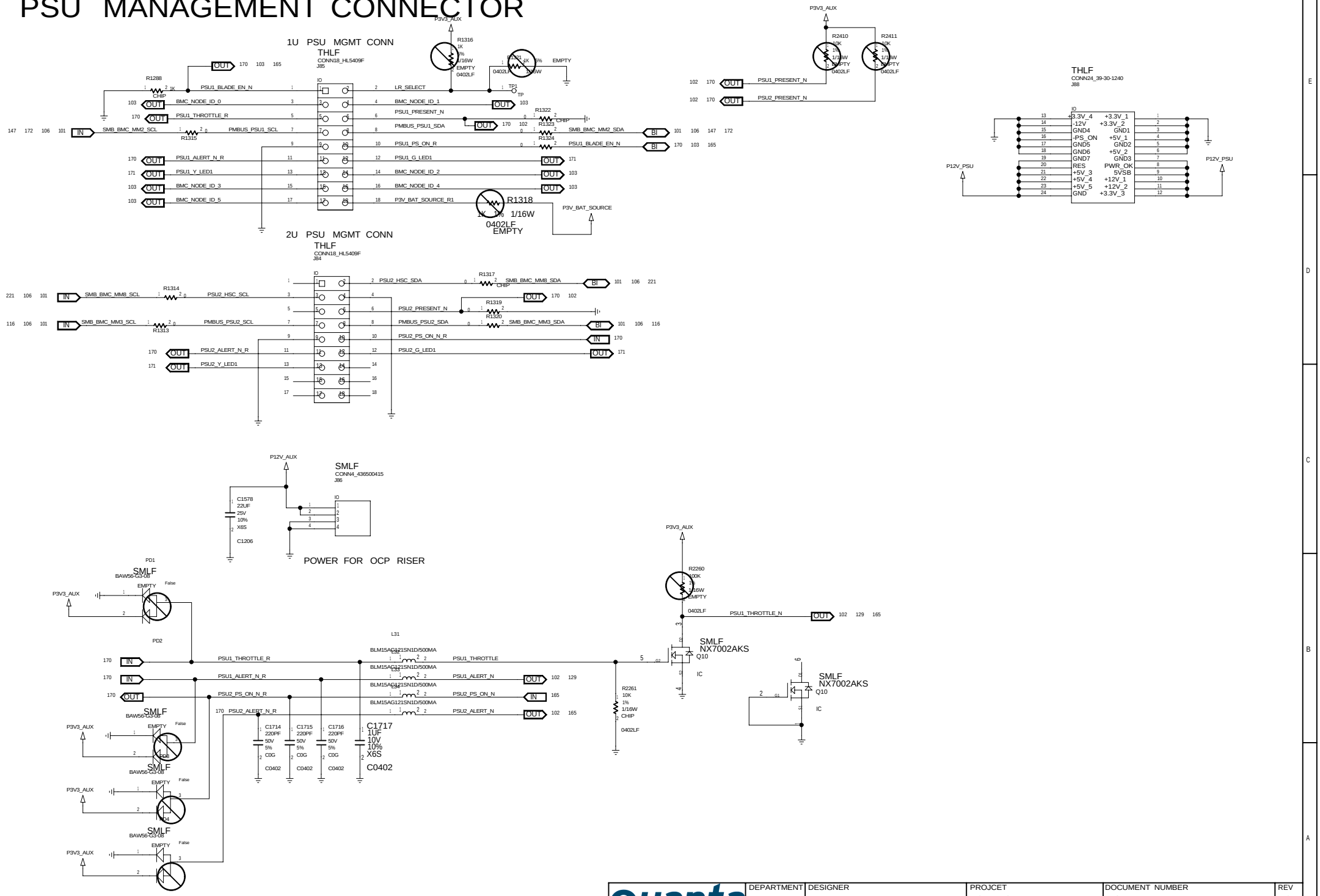
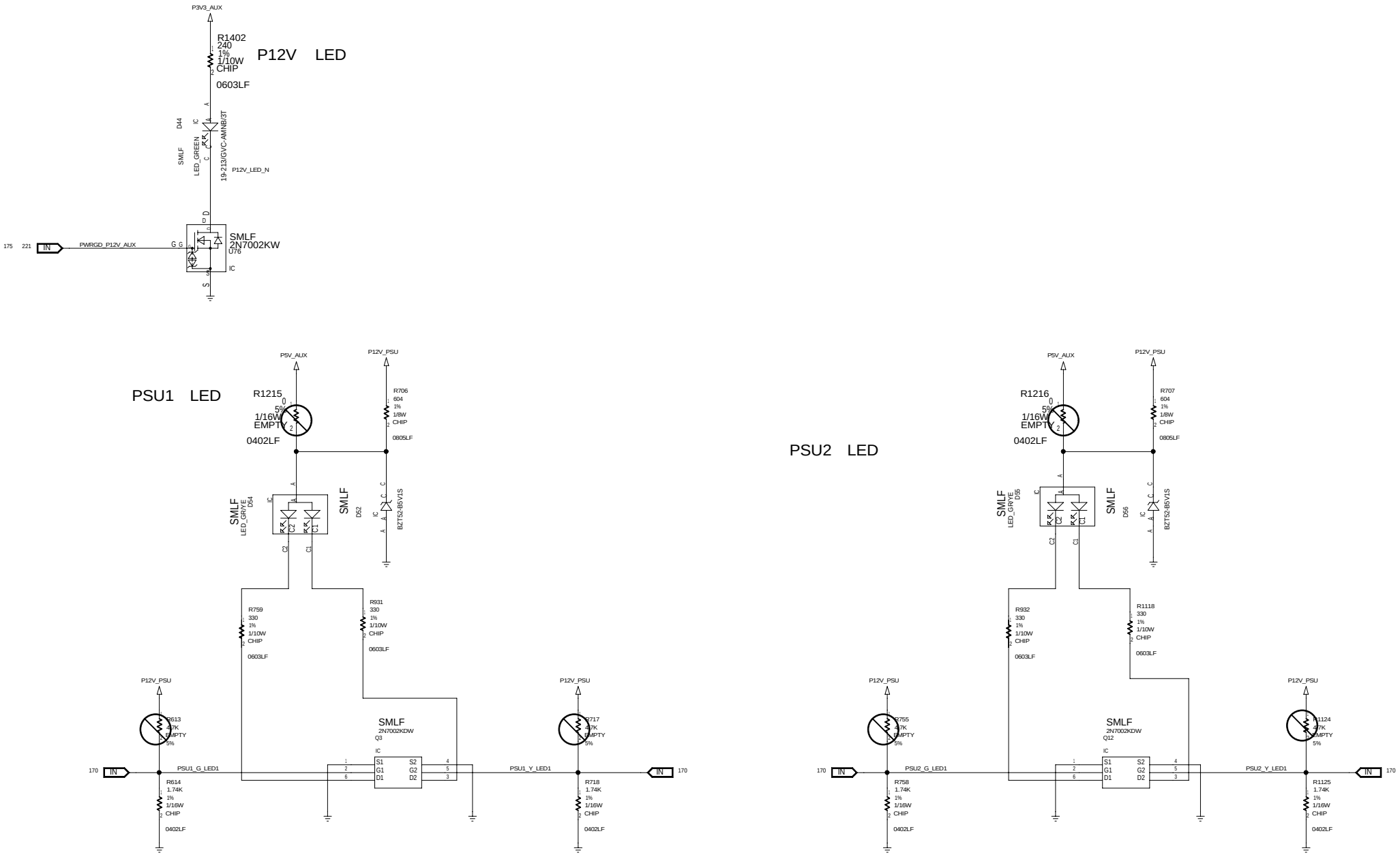
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:36:55 2017	SHEET 169 OF 226

PSU MANAGEMENT CONNECTOR



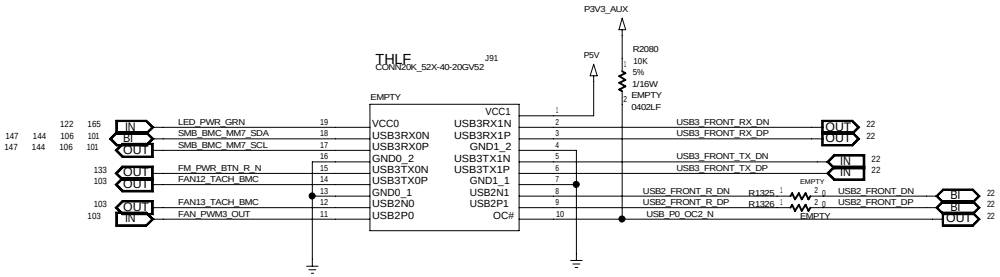
POWER CONNECTORS

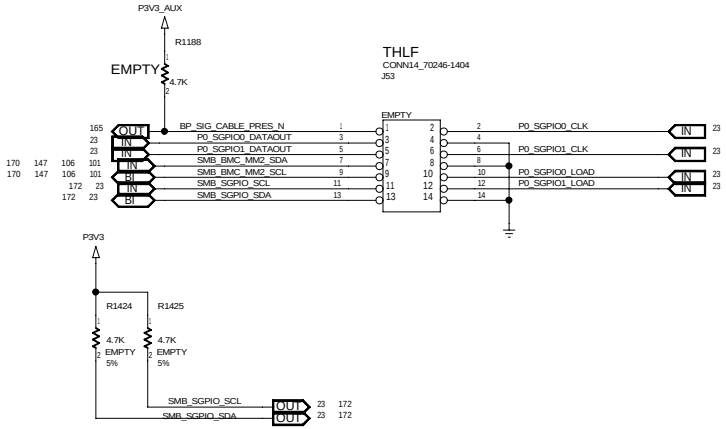
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:22:03 2017	SHEET 170 OF 226	



PSU & P12V LED

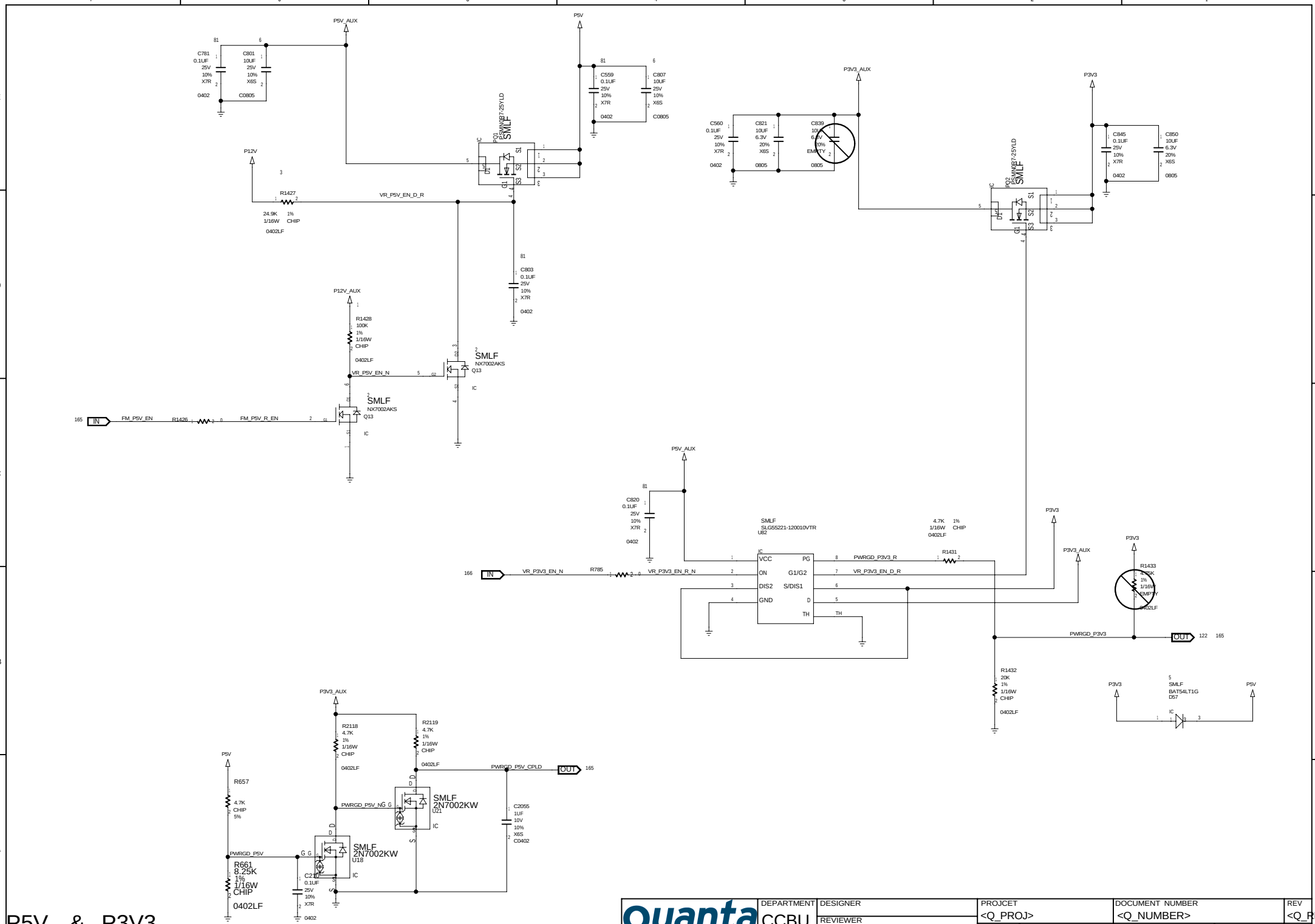
Quanta	DEPARTMENT: CCBU	DESIGNER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>
		REVIEWER		REV: <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:19 2017
			SHEET 171 OF 226	





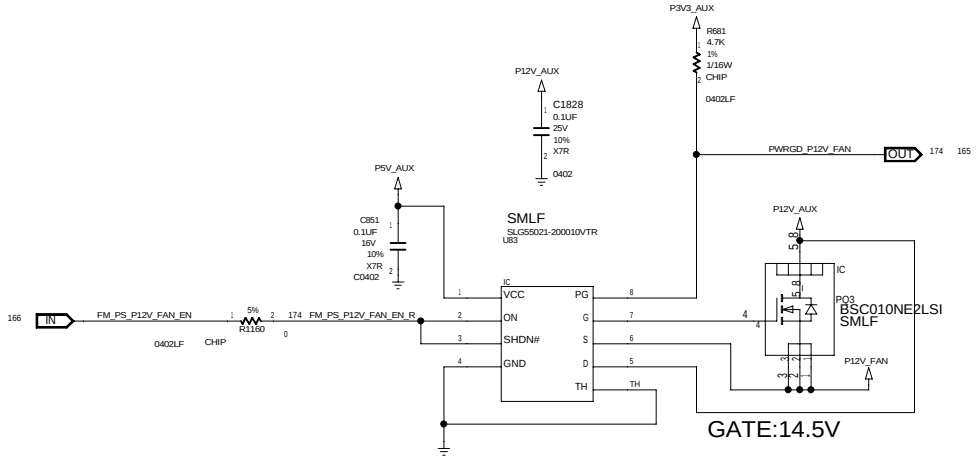
FRONT CONN

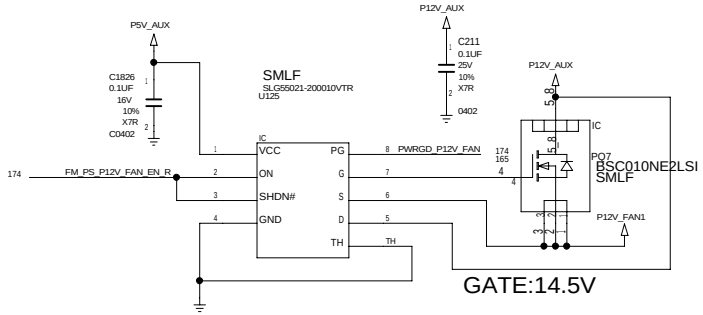
Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
			SIZE C	DATE Fri Dec 15 20:22:03 2017	SHEET 172 OF 226

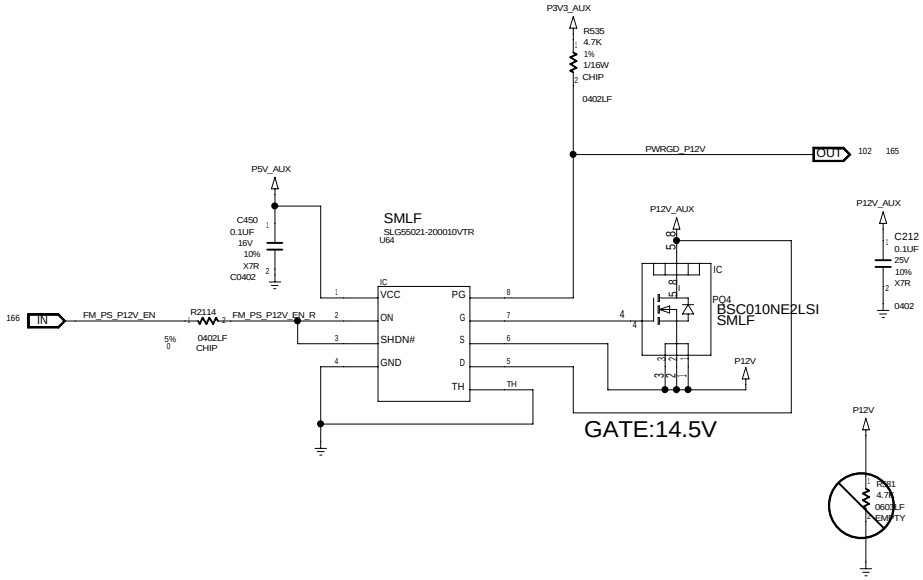


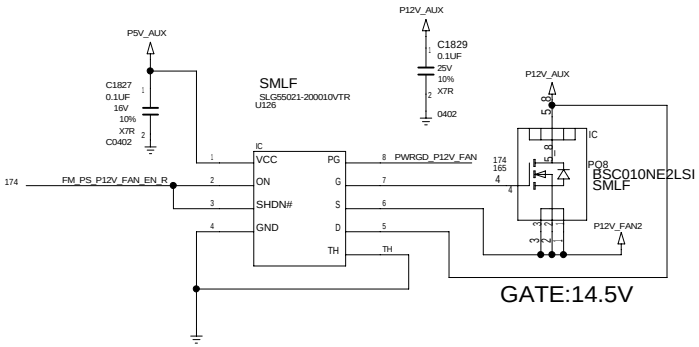
P5V & P3V3

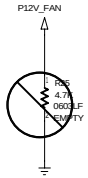
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C	DATE Fri Dec 15 20:22:03 2017
SHEET 173 OF 226			









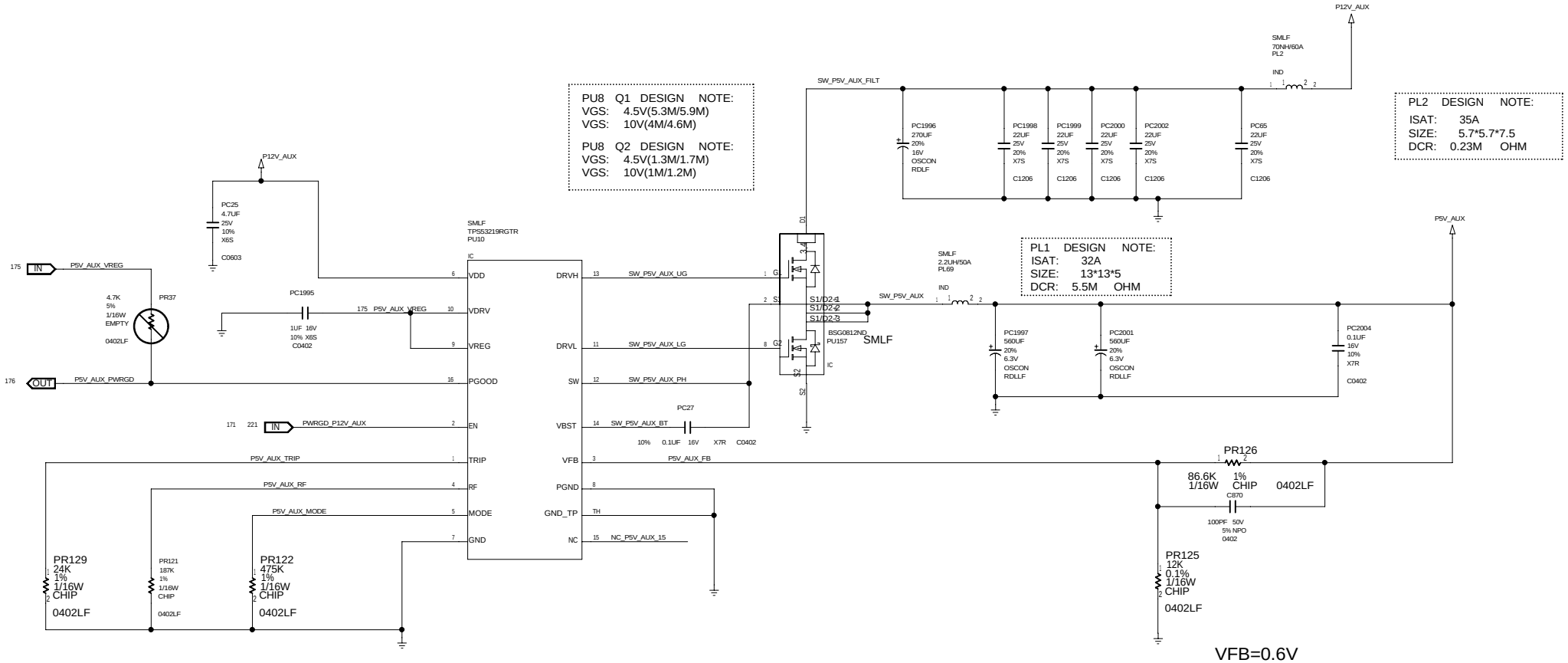


P12V & P12V_FAN

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:25 2017	SHEET 174 OF 226

DESIGN NOTE:
OUTPUT VOLTAGE = 5V+/-5%
OUTPUT RIPPLE&NOISE<50MV
TRANSIENT TOLERANCE=500MV
TDC = 19.2A
MAX CURRENT = 24A
OVER-CURRENT PROTECTION (MAX RATING*1.3)=31.2A
CURRENT STEP = 9A
SLEW RATE = 2.5A/US
WORK FREQUENCY = 300KHZ
EFFICIENCY > 85% @ TDC

P5V_AUX VR

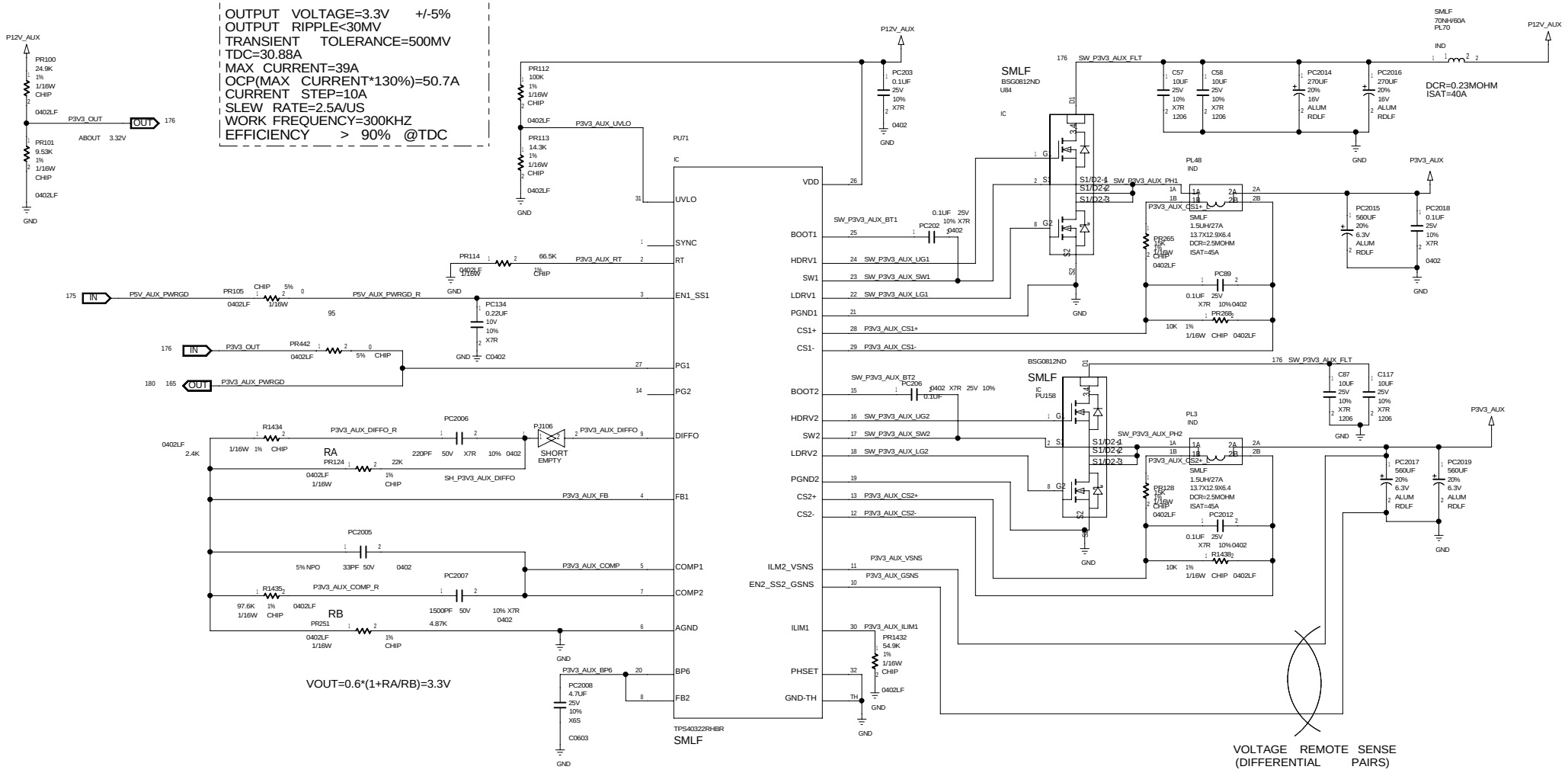


P5V_AUX	Quanta	DEPARTMENT: CCBU	DESIGNER / REVIEWER	PROJCET: <Q_PROJ>	DOCUMENT NUMBER: <Q_NUMBER>	REV: <Q_REV>
				SIZE C	DATE Fri Dec 15 20:22:03 2017	SHEET 175 OF 226

P3V3_AUX VR

DESIGN SPECIFICATION

OUTPUT VOLTAGE=3.3V +/-5%
OUTPUT RIPPLE<30MV
TRANSIENT TOLERANCE=500MV
TDC=30.88A
MAX CURRENT=39A
OCP(MAX CURRENT*130%)=50.7A
CURRENT STEP=10A
SLEW RATE=2.5A/US
WORK FREQUENCY=300KHZ
EFFICIENCY > 90% @TDC



P3V3_AUX	Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>
				DOCUMENT NUMBER <Q_NUMBER>
				REV <Q_REV>
				SIZE C DATE Fri Dec 15 20:22:03 2017 SHEET 176 OF 226

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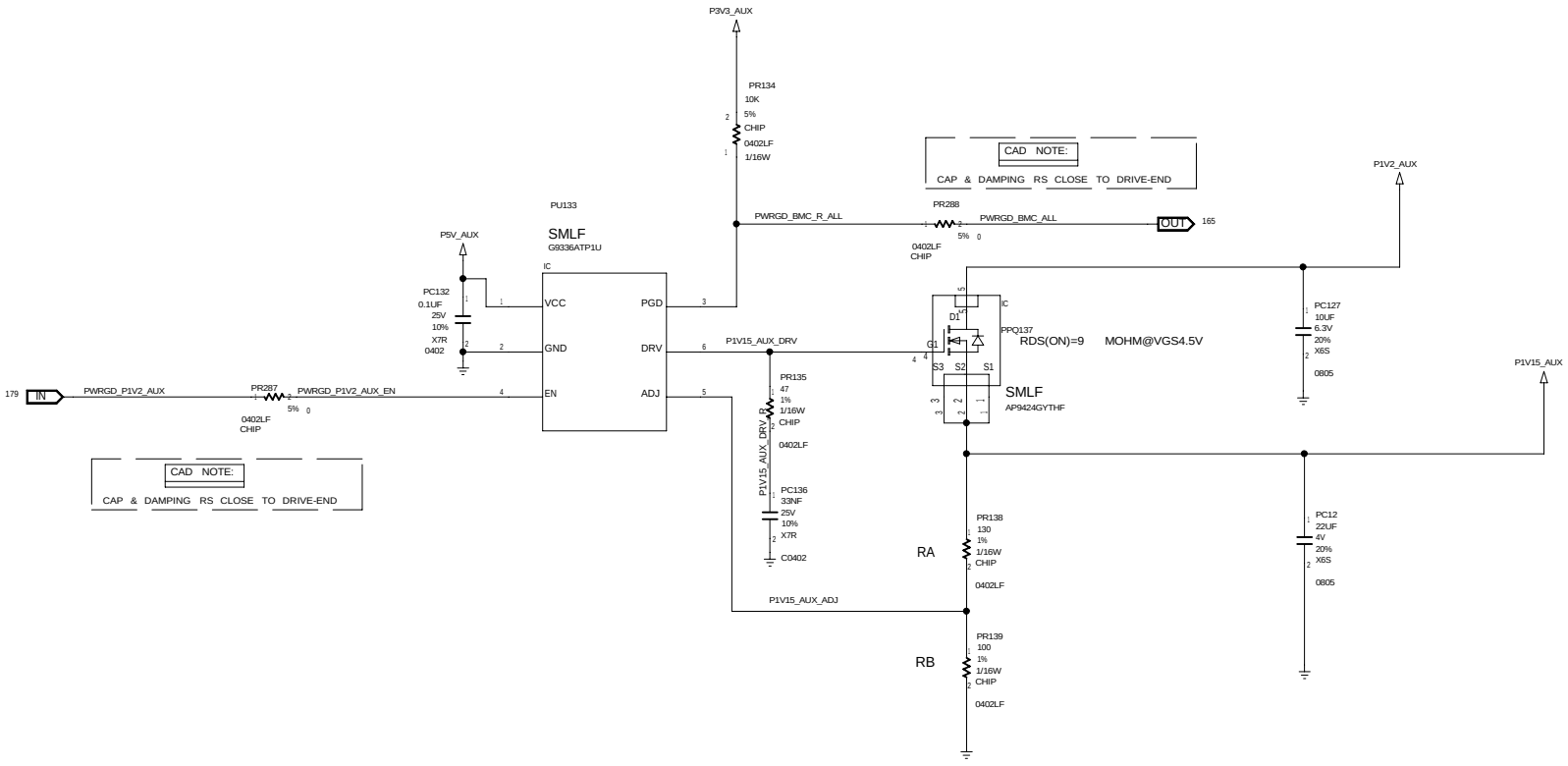
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:48:55 2017	SHEET 177 OF 226

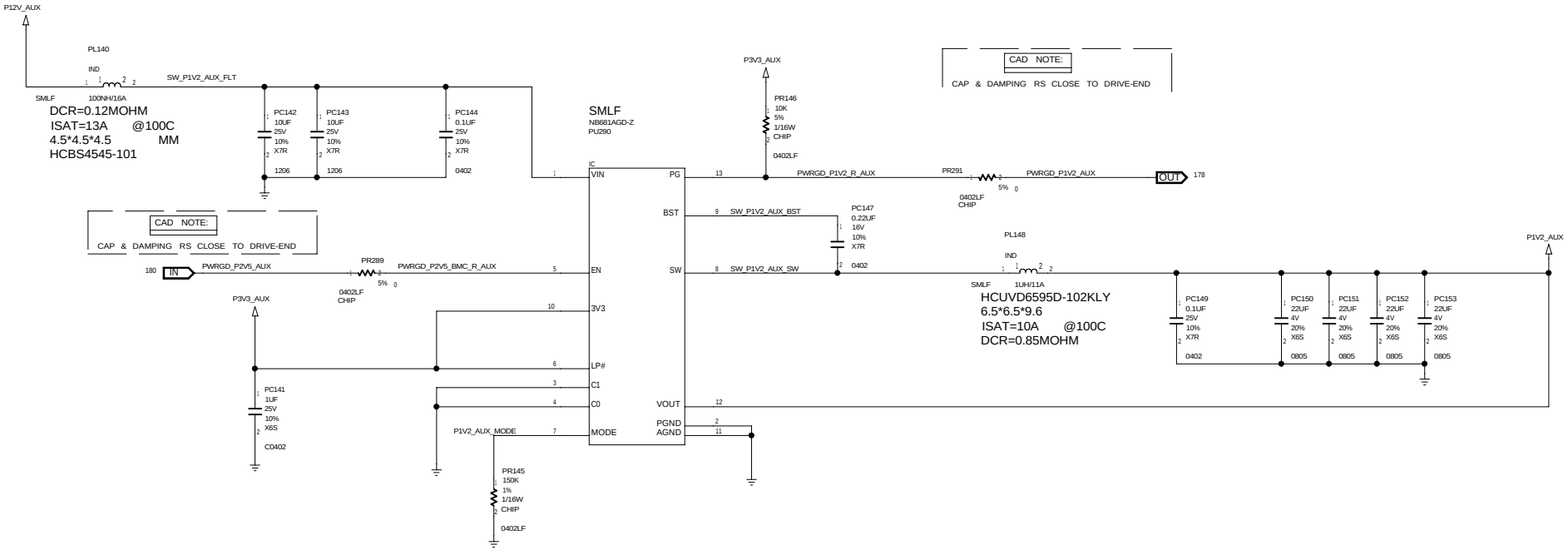
P1V15_AUX

DESIGN SPECIFICATION
OUTPUT VOLTAGE=1.15V
OUTPUT RIPPLE<+/-11.5MV
TRANSIENT TOLERANCE=+/-51.75MV
TDC=0.75A
MAX CURRENT=0.75A



VOUT=0.5(1+RA/RB)=1.15V

DESIGN SPECIFICATION
OUTPUT VOLTAGE=1.2V
OUTPUT RIPPLE<+/-12MV
TRANSIENT TOLERANCE=+/-54MV
TDC=1.2A
MAX CURRENT=2A
OVER CURRENT PROTECTION(IC RATING)=7A
CURRENT STEP=2A
SLEW RATE=2A/US
WORK FREQUENCY=750KHZ
EFFICIENCY>90%@TDC



Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
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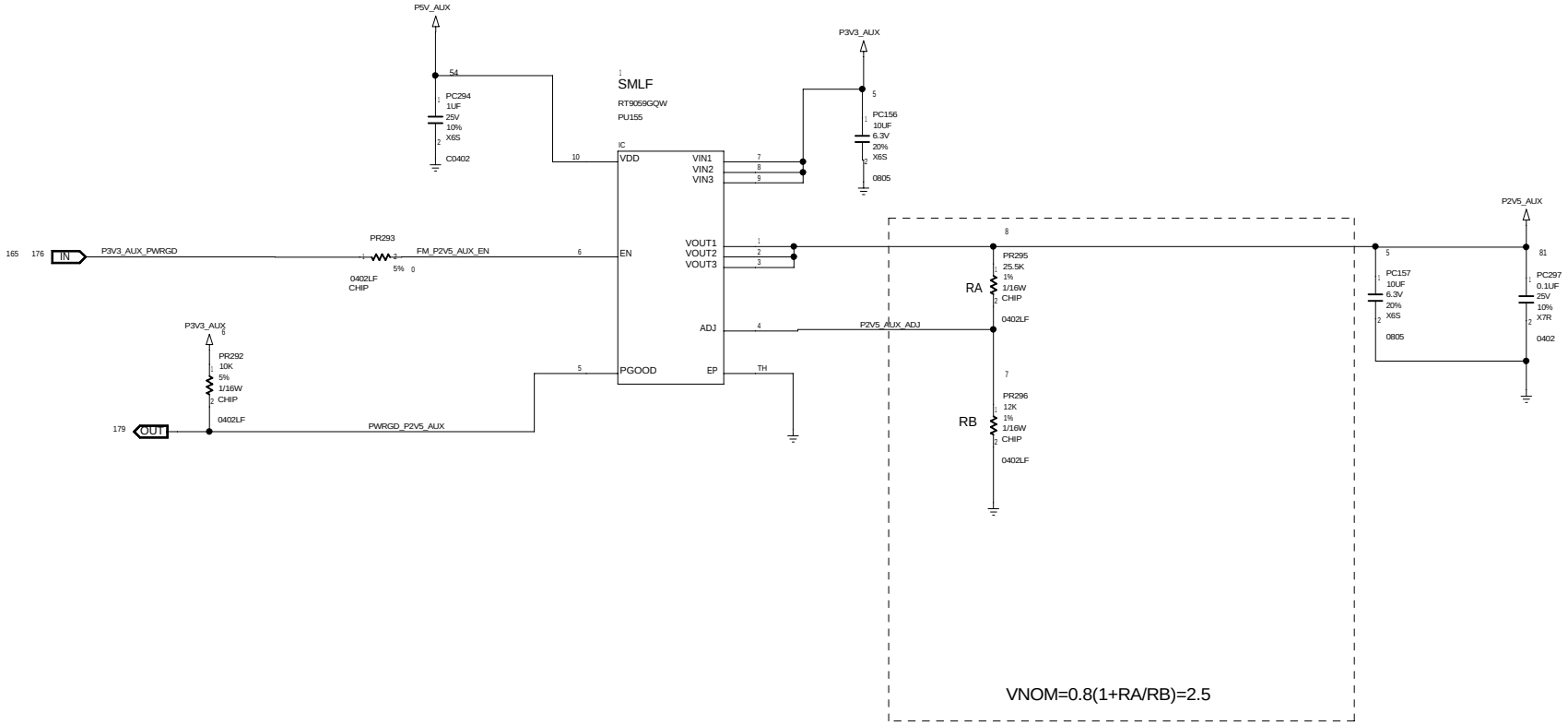
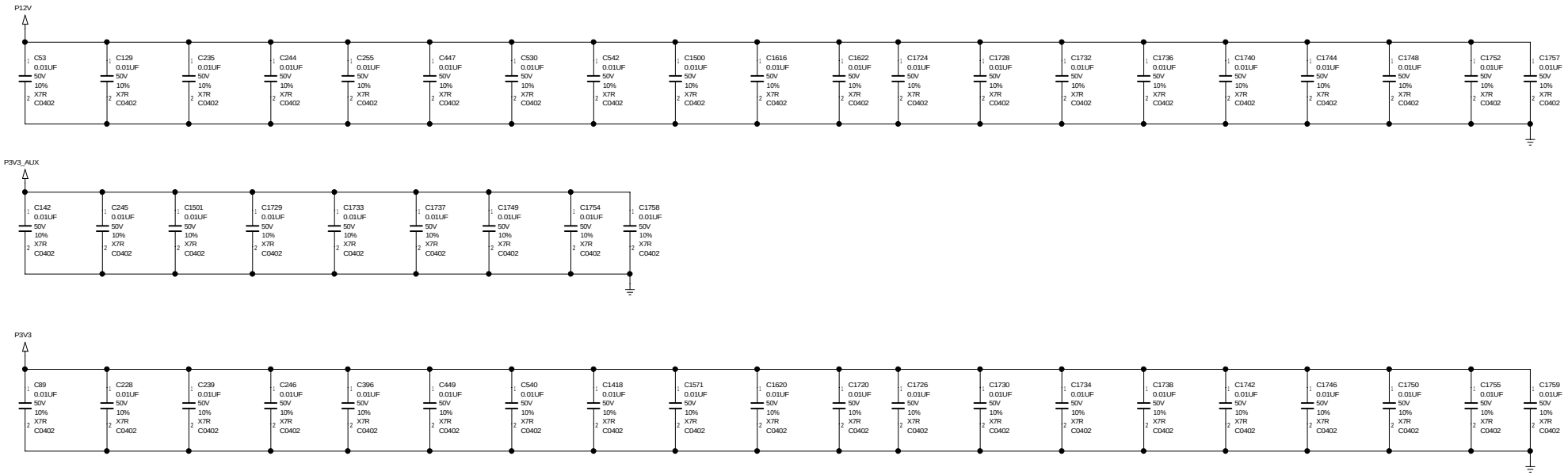
P1V2_AUX

OUTPUT VOLTAGE = 2.5V+/-5%
OUTPUT RIPPLE & NOISE < 50MV
TRANSIENT TOLERANCE = +/-137.5MV
TDC CURRENT = 0.3A
CURRENT STEP = 0.1A
SLEW RATE = 0.1A/US
MAX CURRENT = 0.5A
PD = (3.3V - 2.5V) * 0.5A =0.4W



P2V5_AUX

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:22:04 2017	SHEET 180 OF 226



STITCHING CAP

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
			SIZE C	DATE Fri Dec 15 20:22:04 2017	SHEET 181 OF 226

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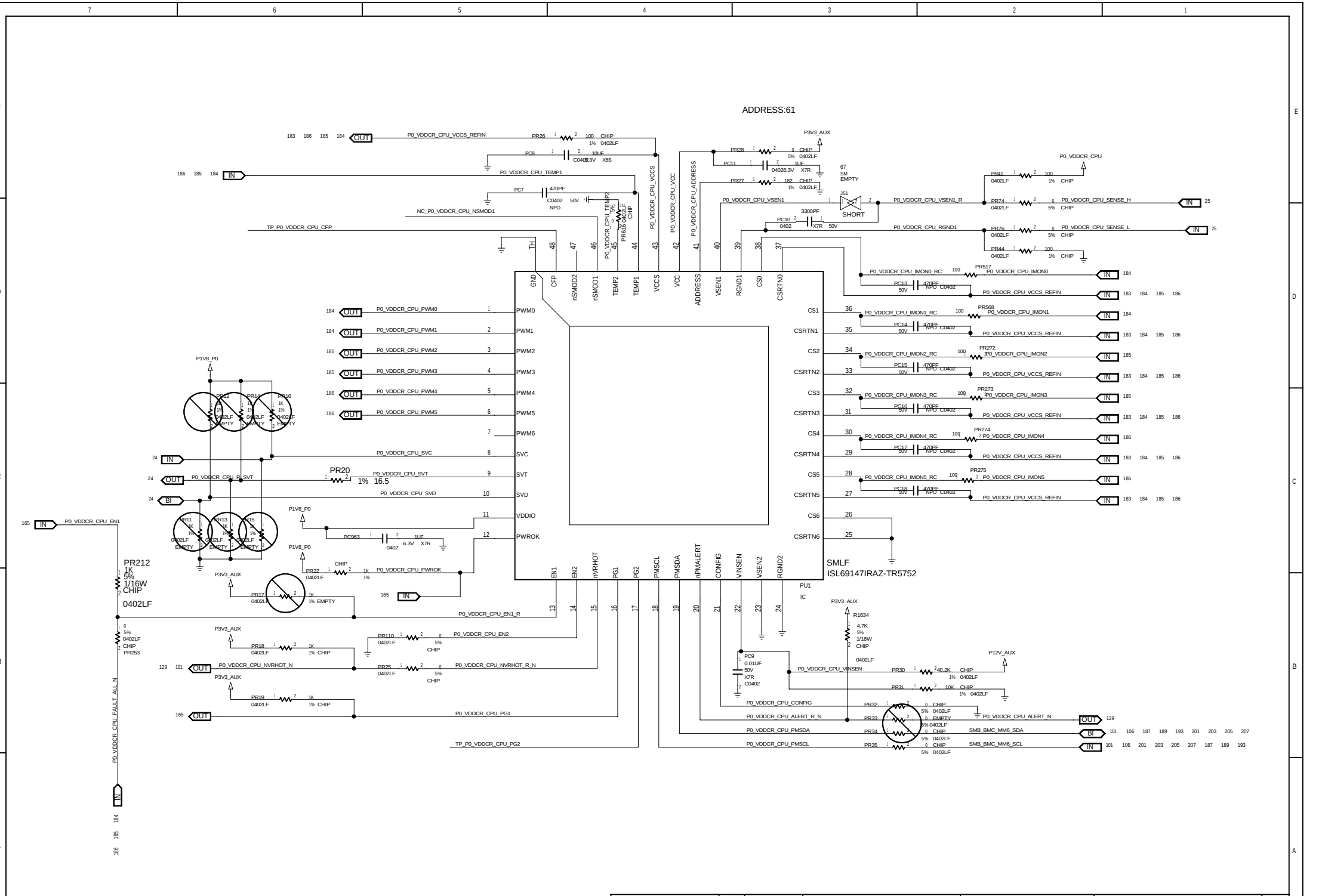
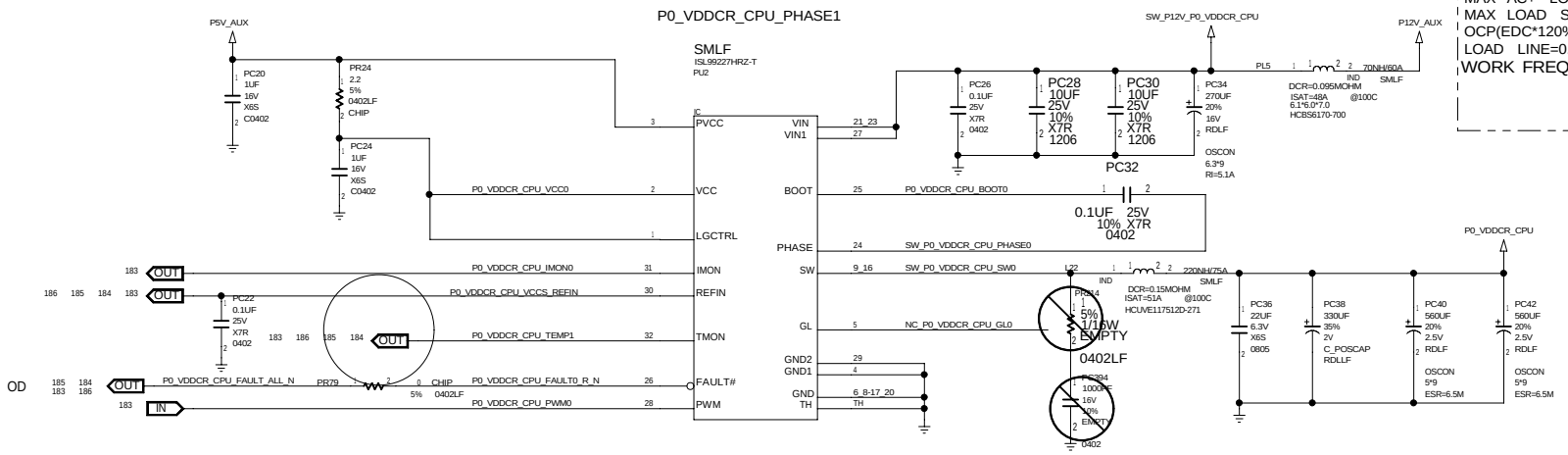
Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
			SIZE C	DATE Fri Dec 15 19:37:01 2017	SHEET 182 OF 226

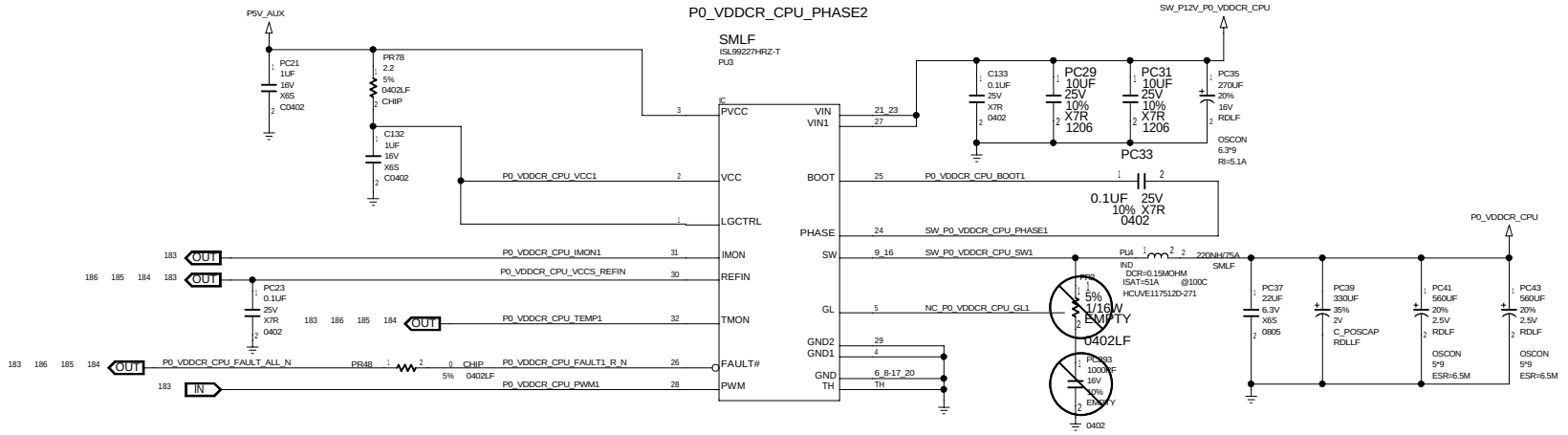


P0_VDDCR_CPU CONTROLLER

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU		<Q_PROJ>	<Q_NUMBER>	<Q_REV>
	REVIEWER	SIZE C	DATE Fri Dec 15 20:22:04 2017	SHEET 183 OF 226

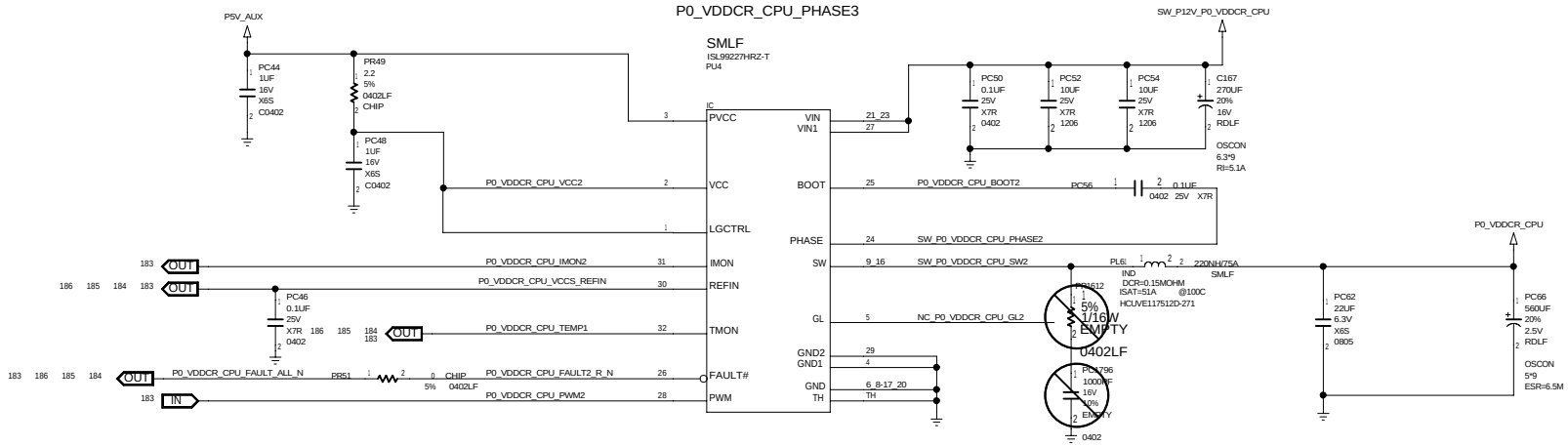
P0_VDDCR_CPU SPECIFICATION
VID=0.7V~1.15V, VBOOT=0.8V
TDC=180A
EDC=240A
MAX AC+ LOAD STEP=160A
MAX LOAD STEP=200A
OCP(EDC*120%)=288A
LOAD LINE=0.3MOHM
WORK FREQUENCY=300KHZ

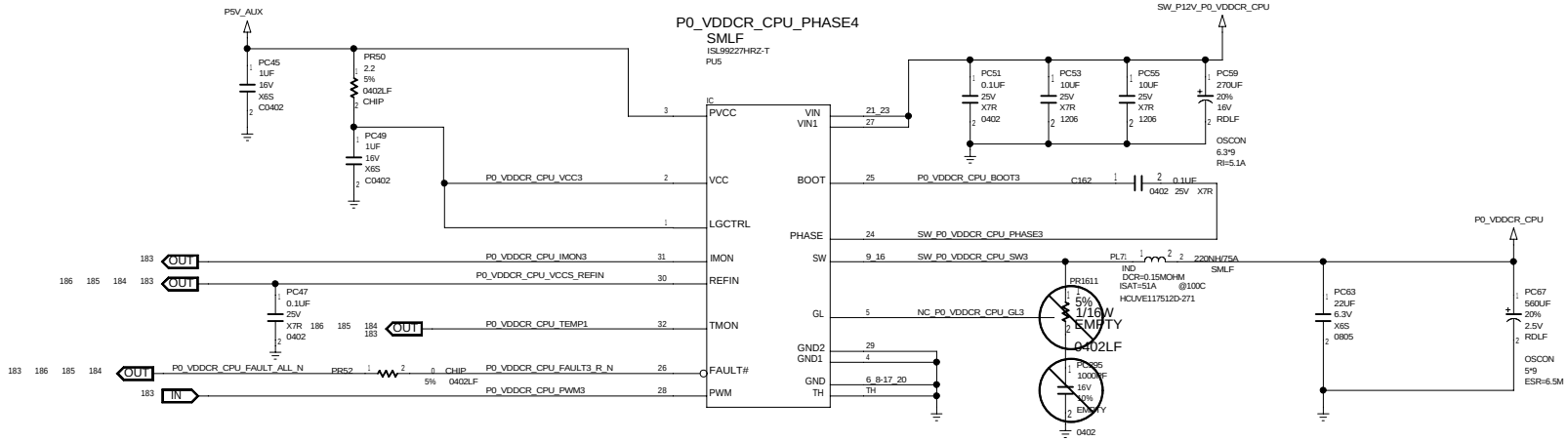




P0_VDDCR_CPU POWER STAGE_1

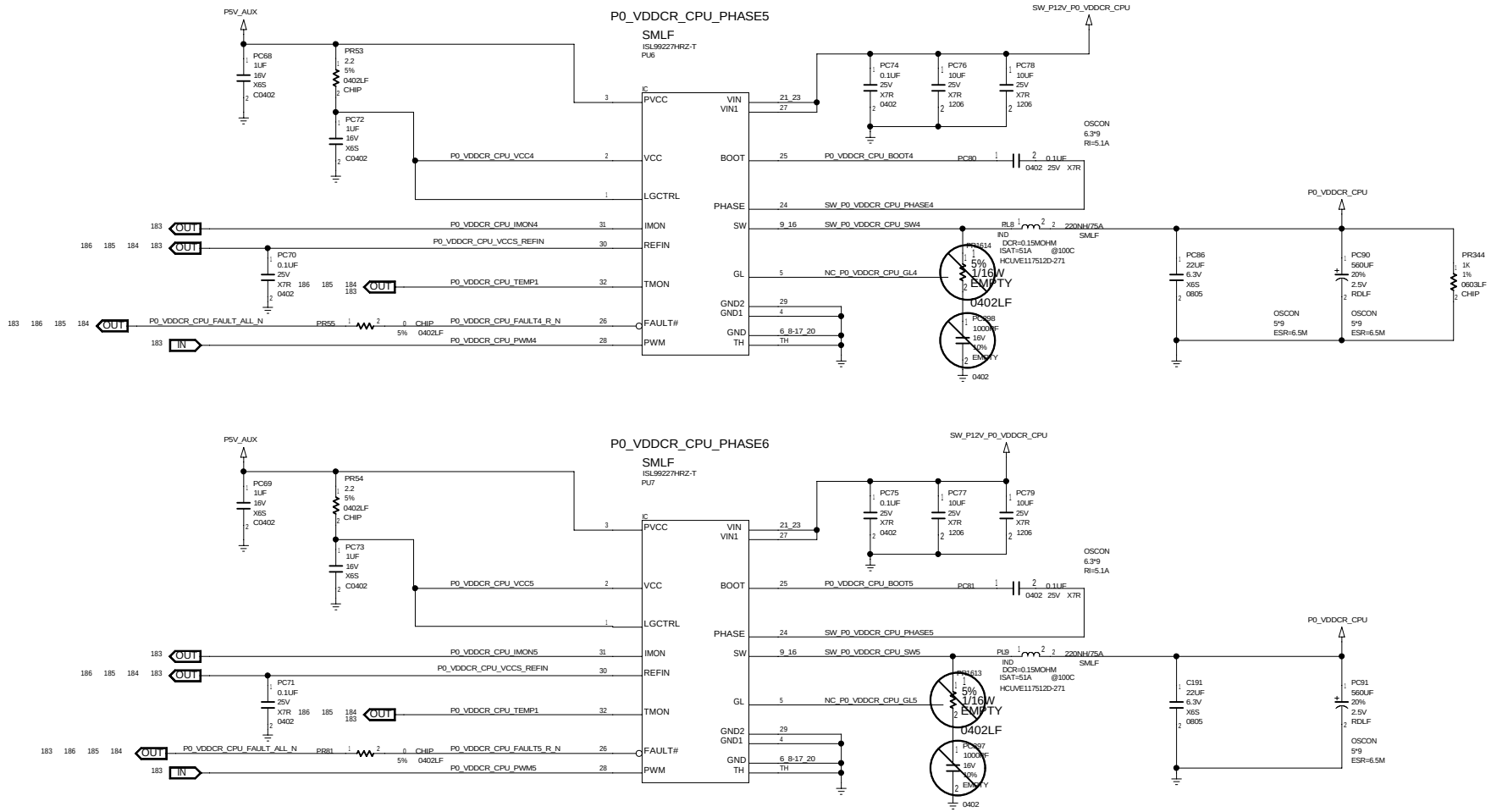
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:21 2017	SHEET 184 OF 226





P0_VDDCR_CPU POWER STAGE 2

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:21 2017	SHEET 185 OF 226



P0_VDDCR_CPU POWER STAGE_3

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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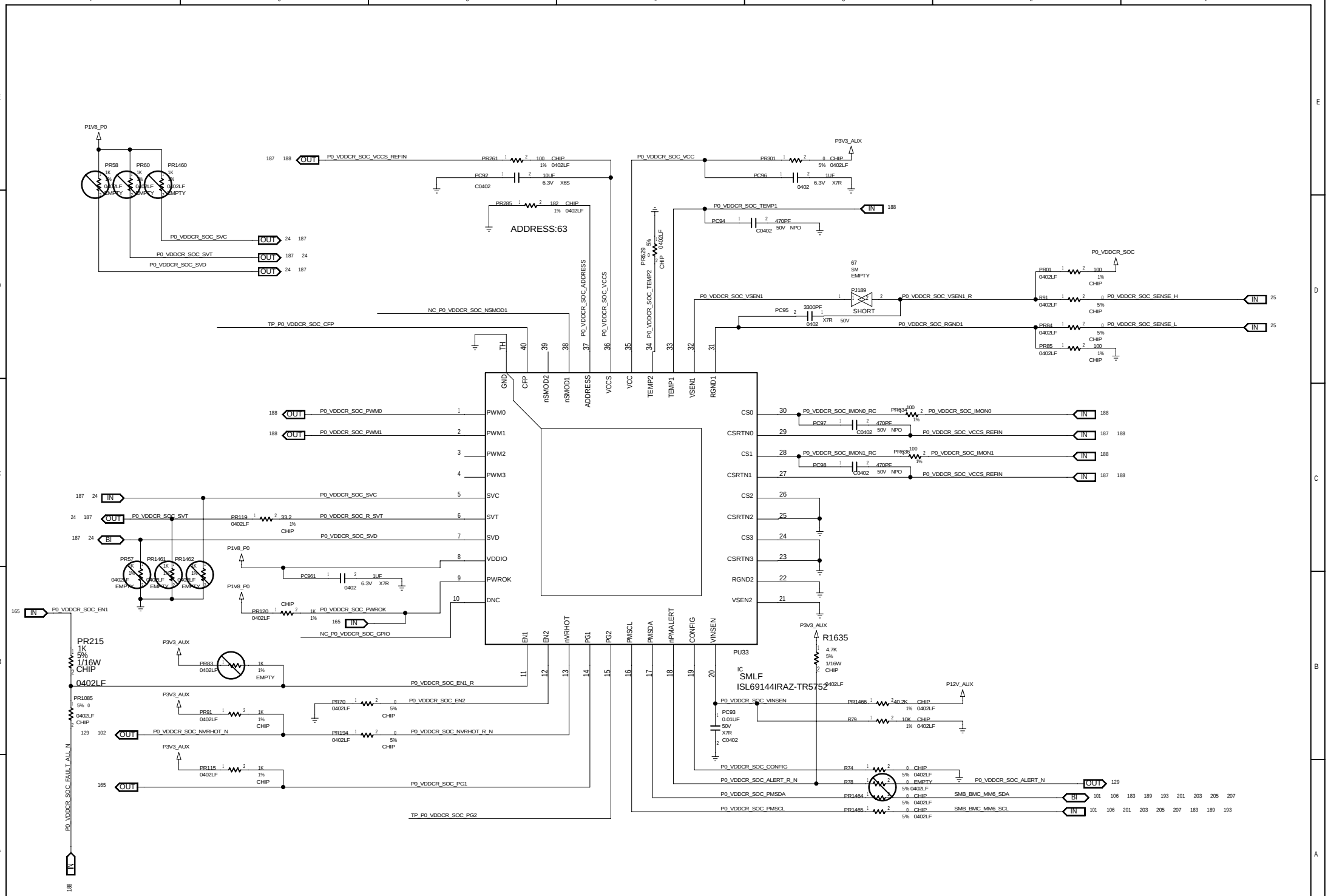
P0_VDDCR_SOC CONTROLLER
ADDRESS:63
PU33
IC
SMLF
ISL69144IRAZ-TR5752
P0_VDDCR_SOC_VCCS_REFIN
P0_VDDCR_SOC_VCC
P0_VDDCR_SOC_TEMP1
P0_VDDCR_SOC_VSEN1
P0_VDDCR_SOC_VSEN1_R
P0_VDDCR_SOC_RGND1
P0_VDDCR_SOC_SENSE_H
P0_VDDCR_SOC_SENSE_L
NC_P0_VDDCR_SOC_NSMOD1
TP_P0_VDDCR_SOC_CFP
P0_VDDCR_SOC_ADDRESS
P0_VDDCR_SOC_VCCS
P0_VDDCR_SOC_TEMP2
P0_VDDCR_SOC_PWM0
P0_VDDCR_SOC_PWM1
P0_VDDCR_SOC_IMON0_RC
P0_VDDCR_SOC_IMON0
P0_VDDCR_SOC_IMON1_RC
P0_VDDCR_SOC_IMON1
P0_VDDCR_SOC_SVC
P0_VDDCR_SOC_SVT
P0_VDDCR_SOC_R_SVT
P0_VDDCR_SOC_SVD
P0_VDDCR_SOC_PWROK
NC_P0_VDDCR_SOC_GPIO
P0_VDDCR_SOC_EN1
P0_VDDCR_SOC_EN1_R
P0_VDDCR_SOC_EN2
P0_VDDCR_SOC_NVRHOT_N
P0_VDDCR_SOC_NVRHOT_R_N
P0_VDDCR_SOC_PG1
TP_P0_VDDCR_SOC_PG2
P0_VDDCR_SOC_VINSEN
P0_VDDCR_SOC_CONFIG
P0_VDDCR_SOC_ALERT_R_N
P0_VDDCR_SOC_ALERT_N
P0_VDDCR_SOC_PMSDA
P0_VDDCR_SOC_PMSCL
SMB_BMC_MM6_SDA
SMB_BMC_MM6_SCL
P0_VDDCR_SOC_FAULT_ALL_N
P0_VDDCR_SOC_EN1
P1V8_P0
P3V3_AUX
P12V_AUX
PR215
1K
5%
1/16W
CHIP
0402LF
R1635
4.7K
5%
1/16W
CHIP
0402LF
Quanta
DEPARTMENT
CCBU
DESIGNER
REVIEWER
PROJCET
<Q_PROJ>
DOCUMENT NUMBER
<Q_NUMBER>
REV
<Q_REV>
SIZE C
DATE Fri Dec 15 20:22:05 2017
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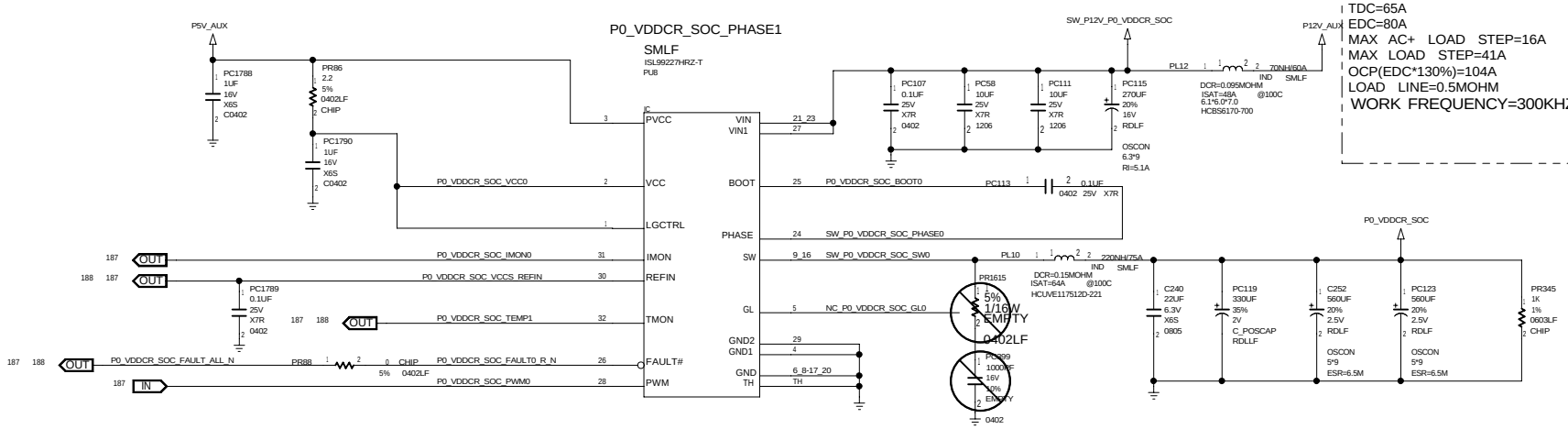
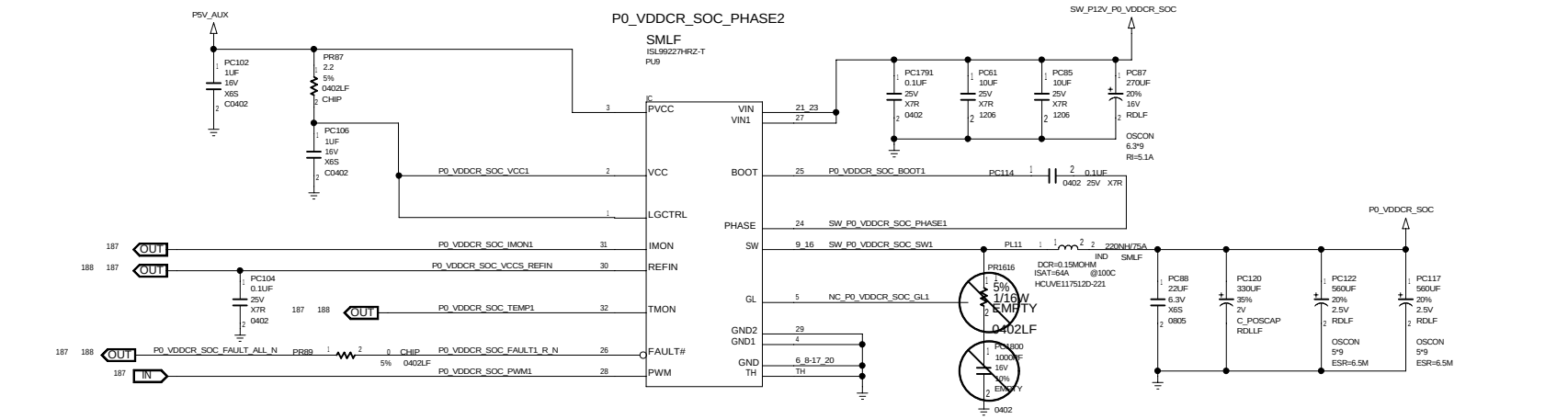
P0_VDDCR_SOC SPECIFICATION
VID=0.8V~0.9V, VBOOT=0.8V
TDC=65A
EDC=80A
MAX AC+ LOAD STEP=16A
MAX LOAD STEP=41A
OCP(EDC*130%)=104A
LOAD LINE=0.5MOHM
WORK FREQUENCY=300KHZ





P0_VDDCR_SOC_POWER_STAGE_1

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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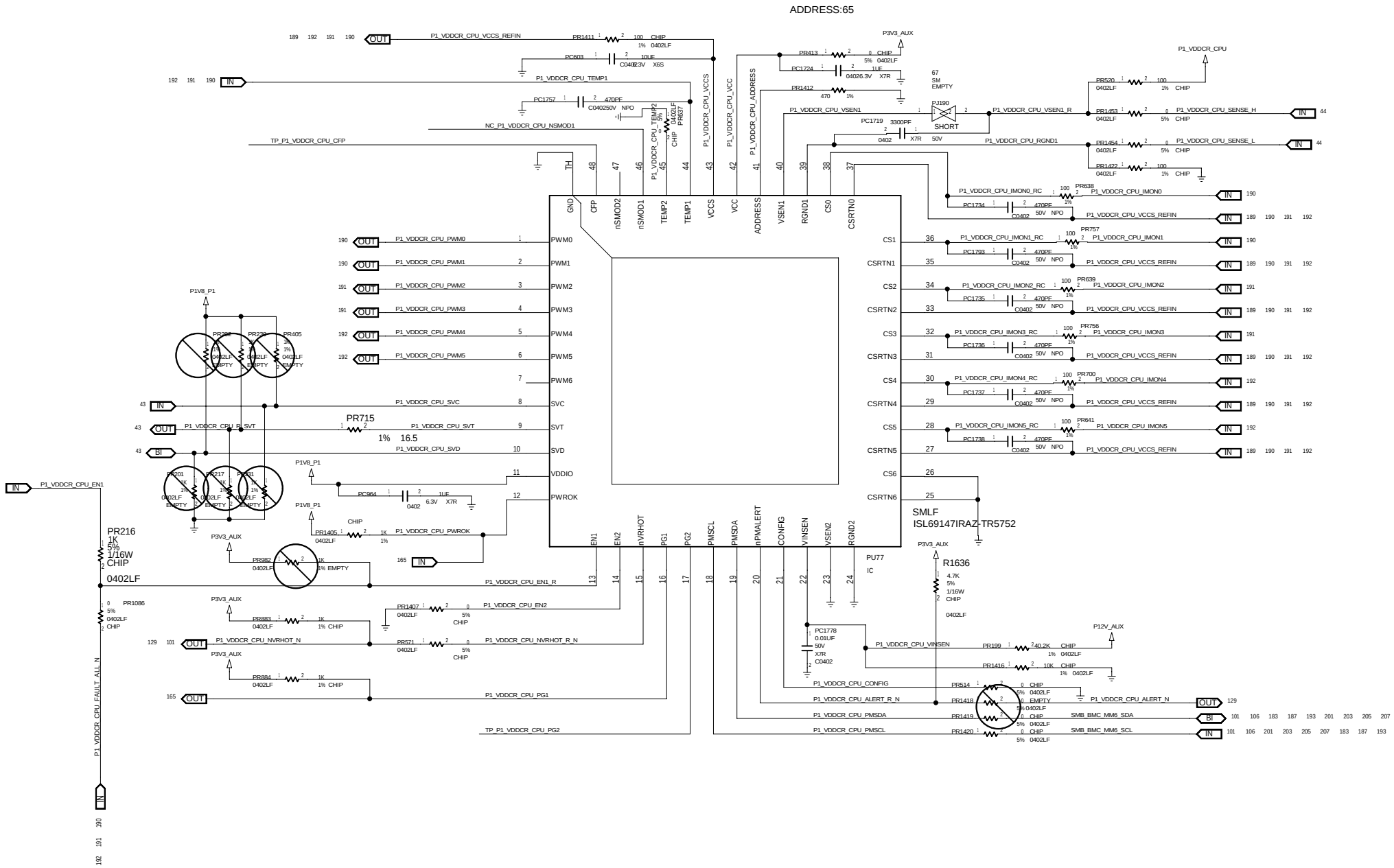
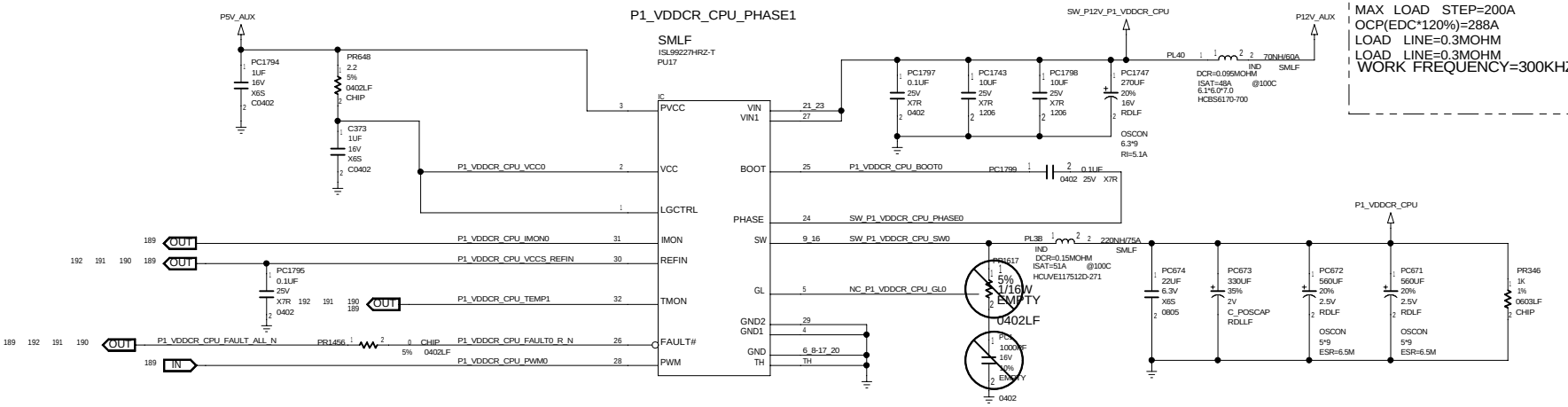
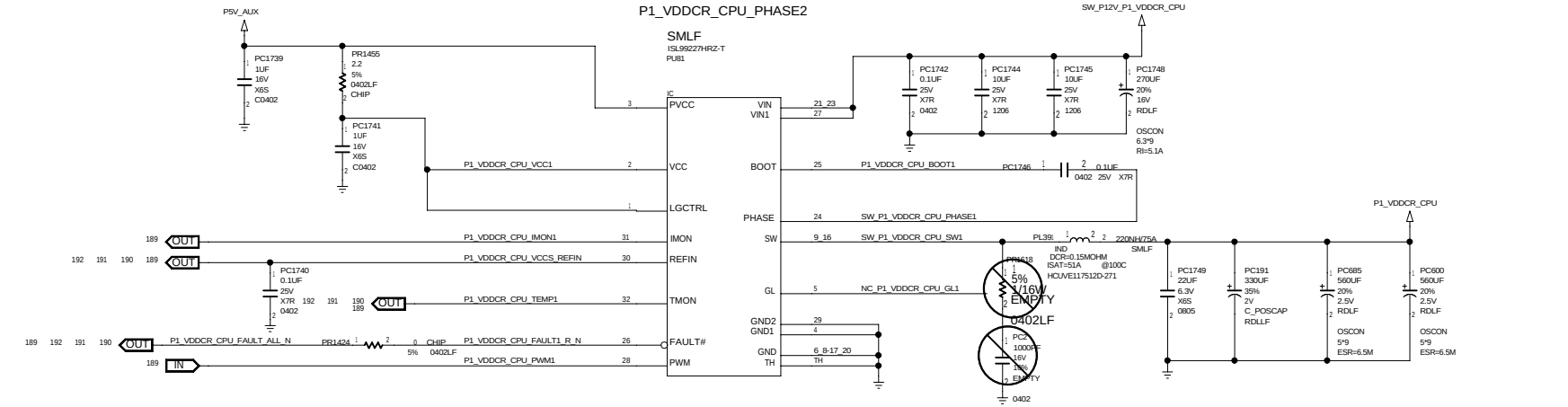


Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>
		REVIEWER	DOCUMENT NUMBER <Q_NUMBER>
			REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:22:05 2017 SHEET 189 OF 226

P1_VDDCR_CPU SPECIFICATION
VID=0.7V~1.15V, VBOOT=0.8V
TDC=180A
EDC=240A
MAX AC+ LOAD STEP=160A
MAX LOAD STEP=200A
OCP(EDC*120%)=288A
LOAD LINE=0.3MOHM
LOAD LINE=0.3MOHM
WORK FREQUENCY=300KHZ





P1_VDDCR_CPU POWER STAGE_1

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C	DATE Fri Dec 15 20:21:22 2017
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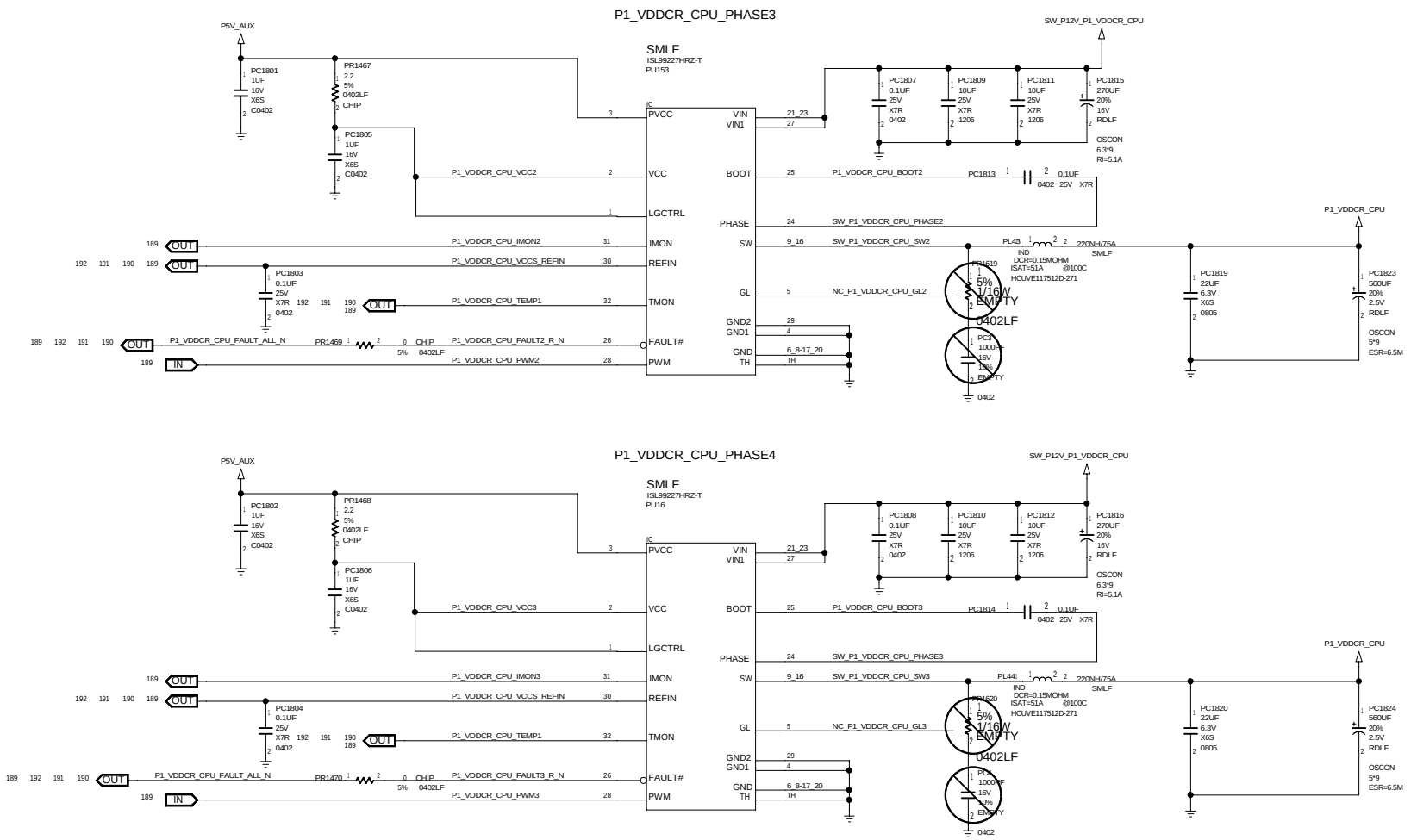

P1_VDDCR_CPU POWER STAGE 2

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU		<Q_PROJ>	<Q_NUMBER>	<Q_REV>
	REVIEWER			

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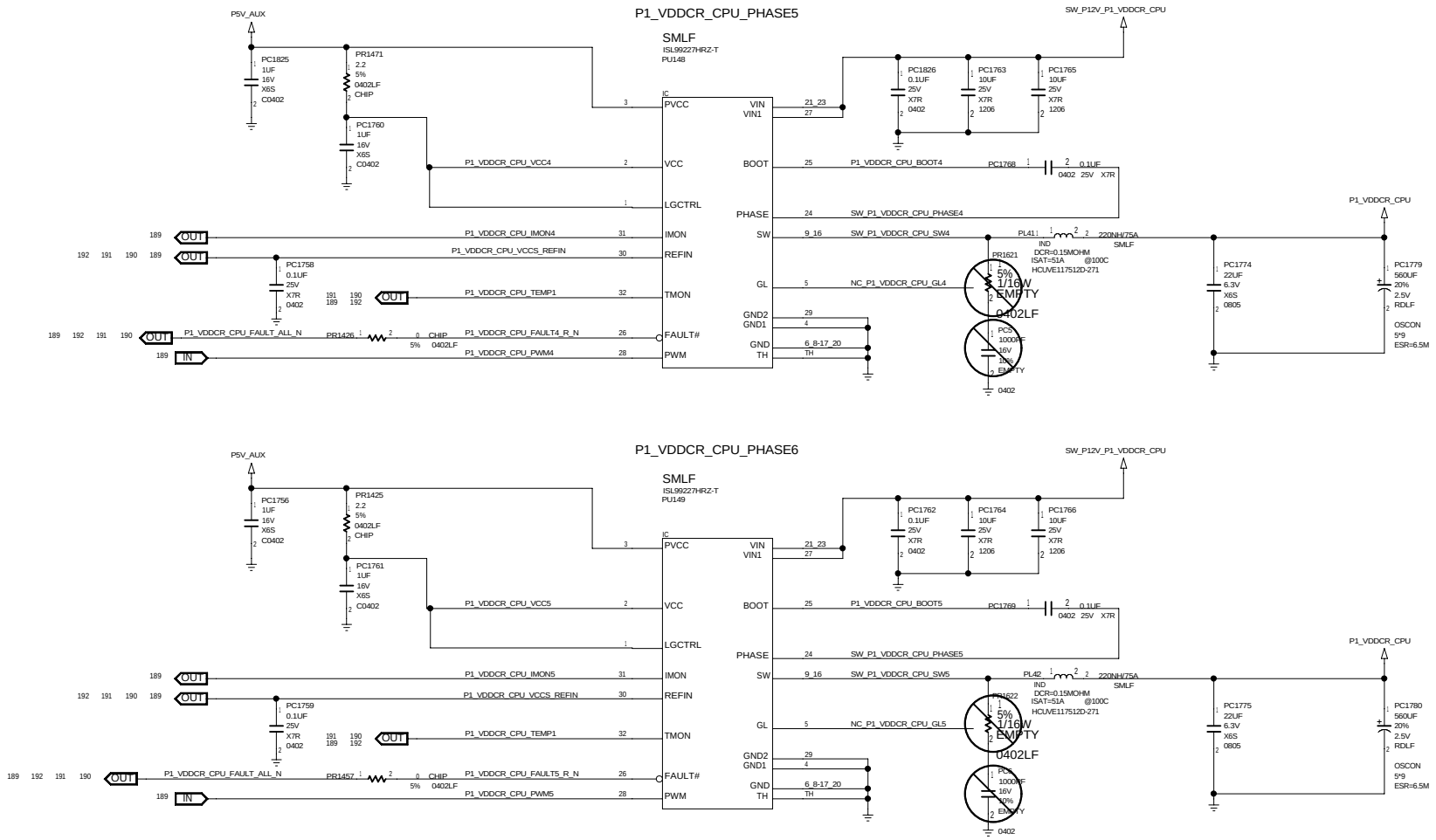

P1_VDDCR_CPU POWER STAGE_3

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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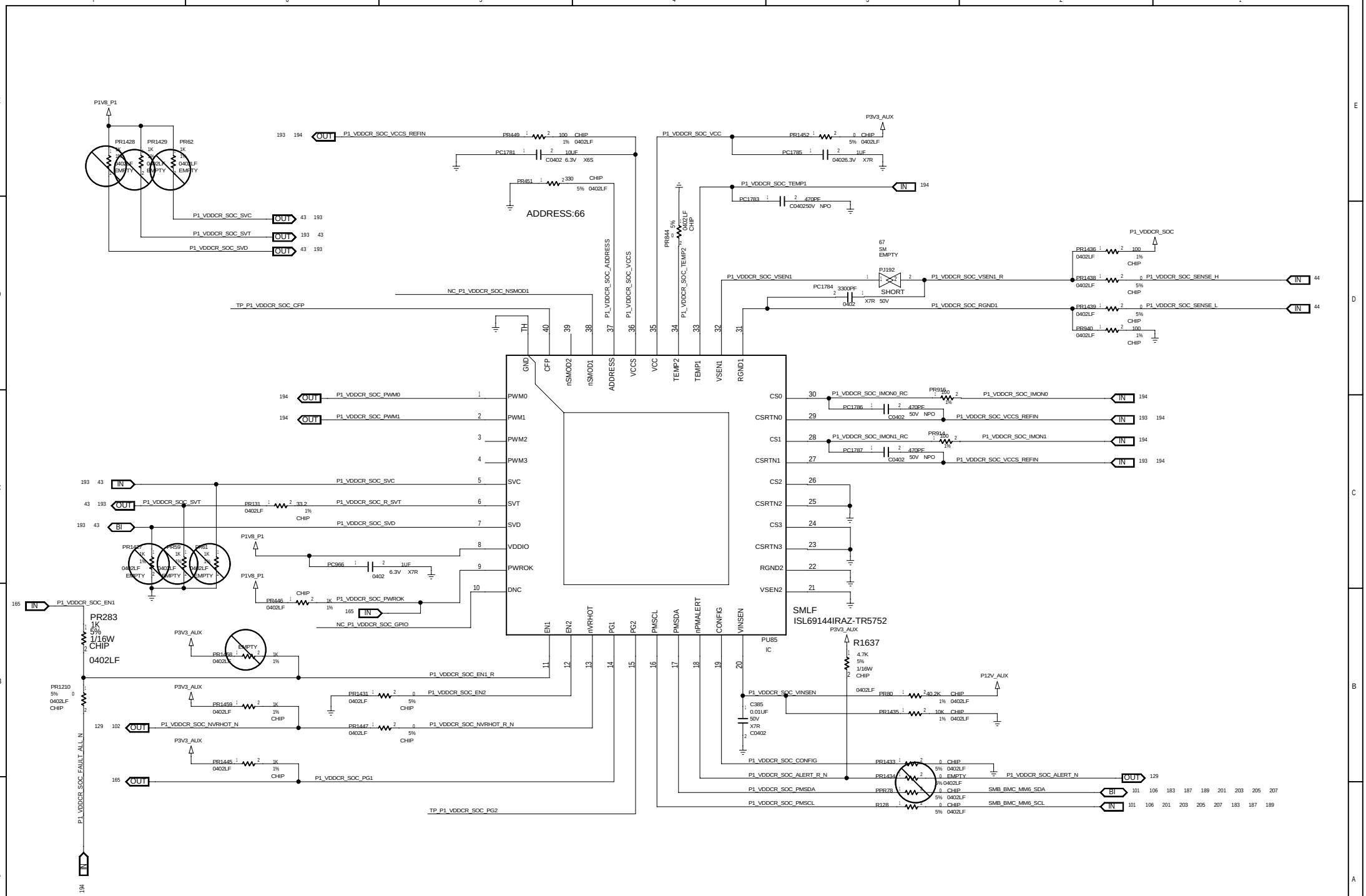
P1_VDDCR_SOC CONTROLLER
SMLF
ISL69144IRAZ-TR5752
PU85
IC
ADDRESS:66
P1_VDDCR_SOC_VCCS_REFIN
P1_VDDCR_SOC_VCC
P1_VDDCR_SOC_TEMP1
P1_VDDCR_SOC_VSEN1
P1_VDDCR_SOC_VSEN1_R
P1_VDDCR_SOC_RGND1
P1_VDDCR_SOC_SENSE_H
P1_VDDCR_SOC_SENSE_L
P1_VDDCR_SOC_PWM0
P1_VDDCR_SOC_PWM1
P1_VDDCR_SOC_IMON0_RC
P1_VDDCR_SOC_IMON0
P1_VDDCR_SOC_IMON1_RC
P1_VDDCR_SOC_IMON1
P1_VDDCR_SOC_SVC
P1_VDDCR_SOC_SVT
P1_VDDCR_SOC_R_SVT
P1_VDDCR_SOC_SVD
P1_VDDCR_SOC_PWROK
P1_VDDCR_SOC_EN1
P1_VDDCR_SOC_EN1_R
P1_VDDCR_SOC_EN2
P1_VDDCR_SOC_NVRHOT_N
P1_VDDCR_SOC_NVRHOT_R_N
P1_VDDCR_SOC_PG1
P1_VDDCR_SOC_VINSEN
P1_VDDCR_SOC_CONFIG
P1_VDDCR_SOC_ALERT_R_N
P1_VDDCR_SOC_ALERT_N
P1_VDDCR_SOC_PMSDA
P1_VDDCR_SOC_PMSCL
SMB_BMC_MM6_SDA
SMB_BMC_MM6_SCL
P1_VDDCR_SOC_FAULT_ALL_N
NC_P1_VDDCR_SOC_NSMOD1
TP_P1_VDDCR_SOC_CFP
NC_P1_VDDCR_SOC_GPIO
TP_P1_VDDCR_SOC_PG2
P1_VDDCR_SOC_ADDRESS
P1_VDDCR_SOC_VCCS
P1_VDDCR_SOC_TEMP2
P1V8_P1
P3V3_AUX
P12V_AUX
PR283
1K
5%
1/16W
CHIP
0402LF
R1637
4.7K
5%
1/16W
CHIP
PJ192
SHORT
67
SM
EMPTY
GND
CFP
nSMOD2
nSMOD1
ADDRESS
VCCS
VCC
TEMP2
TEMP1
VSEN1
RGND1
PWM0
PWM1
PWM2
PWM3
SVC
SVT
SVD
VDDIO
PWROK
DNC
CS0
CSRTN0
CS1
CSRTN1
CS2
CSRTN2
CS3
CSRTN3
RGND2
VSEN2
EN1
EN2
nVRHOT
PG1
PG2
PMSCL
PMSDA
nPMALERT
CONFIG
VINSEN
TH
Quanta
DEPARTMENT
CCBU
DESIGNER
REVIEWER
PROJCET
<Q_PROJ>
DOCUMENT NUMBER
<Q_NUMBER>
REV
<Q_REV>
SIZE C
DATE Fri Dec 15 20:22:05 2017
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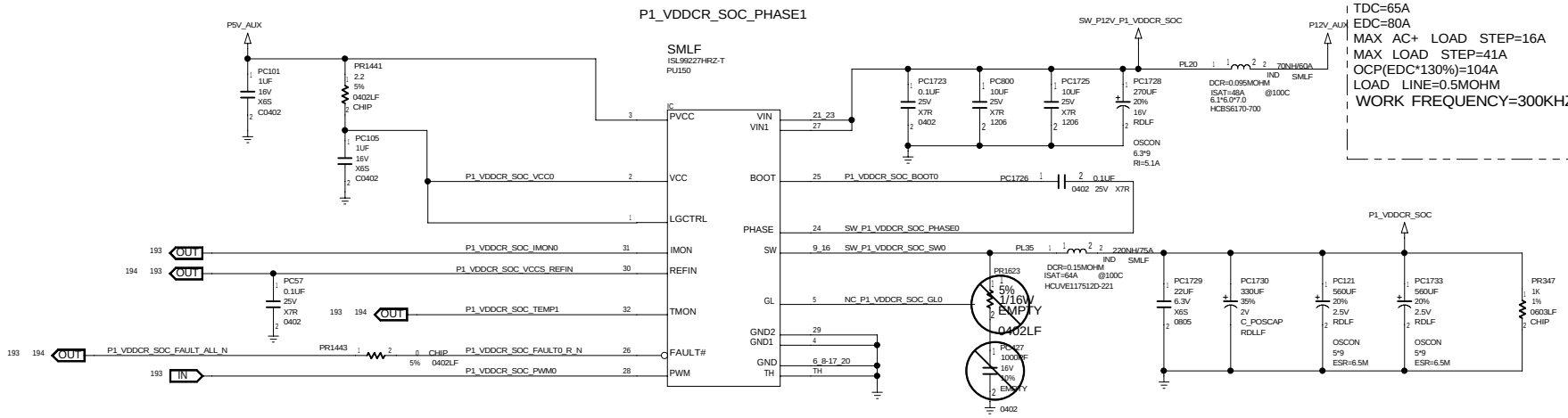
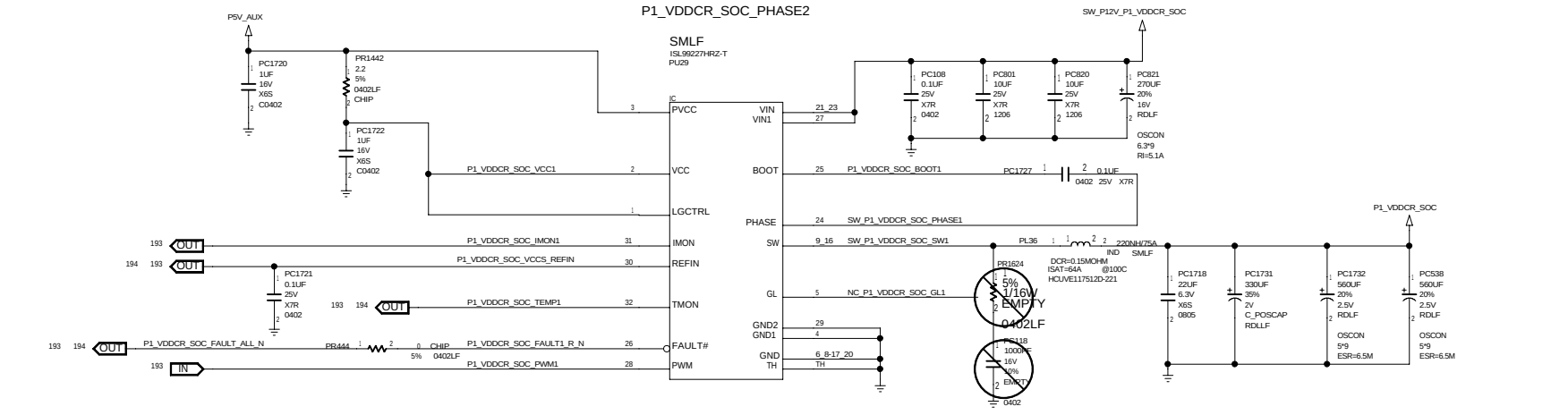
P1_VDDCR_SOC SPECIFICATION
VID=0.8V~0.9V, VBOOT=0.8V
TDC=65A
EDC=80A
MAX AC+ LOAD STEP=16A
MAX LOAD STEP=41A
OCP(EDC*130%)=104A
LOAD LINE=0.5MOHM
WORK FREQUENCY=300KHZ





P1_VDDCR_SOC_POWER_STAGE_1

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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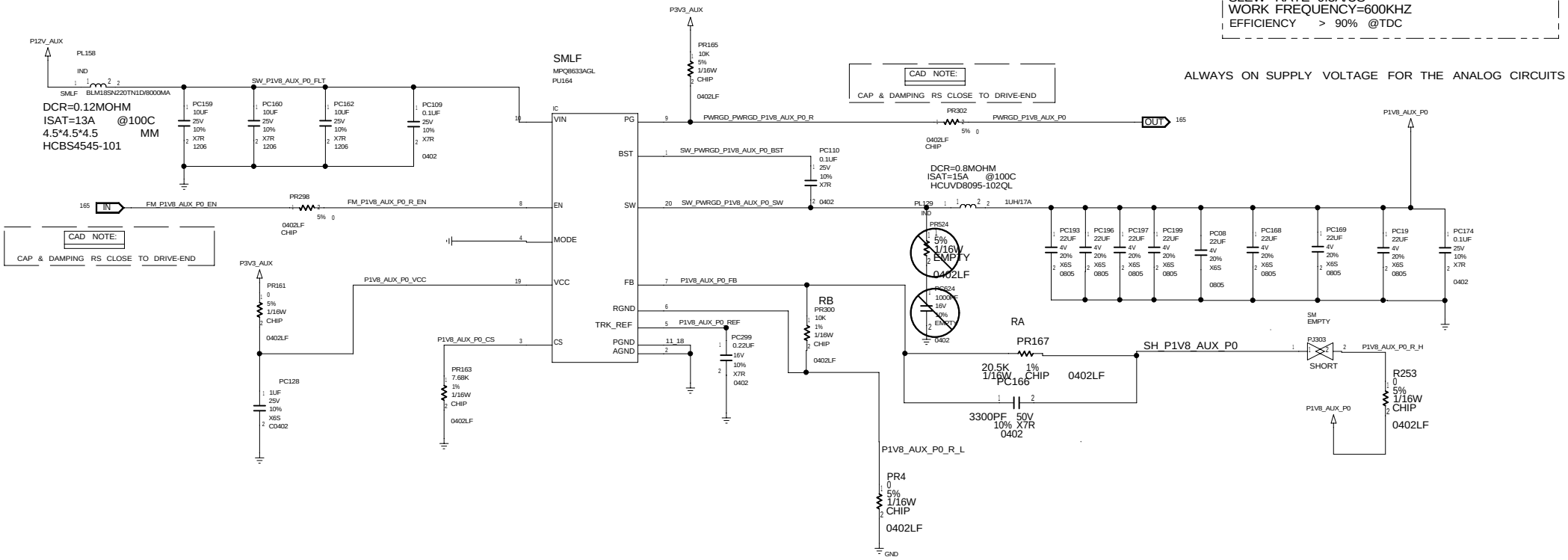
P1V8_AUX_P0

DESIGN SPECIFICATION
OUTPUT VOLTAGE=1.8V +/-5%
OUTPUT RIPPLE<+/-30MV
DC TOLERANCE = 180MV
TRANSIENT TOLERANCE=+175MV/-165MV
TDC=5.6A
MAX CURRENT=7A
OCP(IMAX*130%)=9.1A
CURRENT STEP=0.5A
SLEW RATE=0.5A/US
WORK FREQUENCY=600KHZ
EFFICIENCY > 90% @TDC

ALWAYS ON SUPPLY VOLTAGE FOR THE ANALOG CIRCUITS

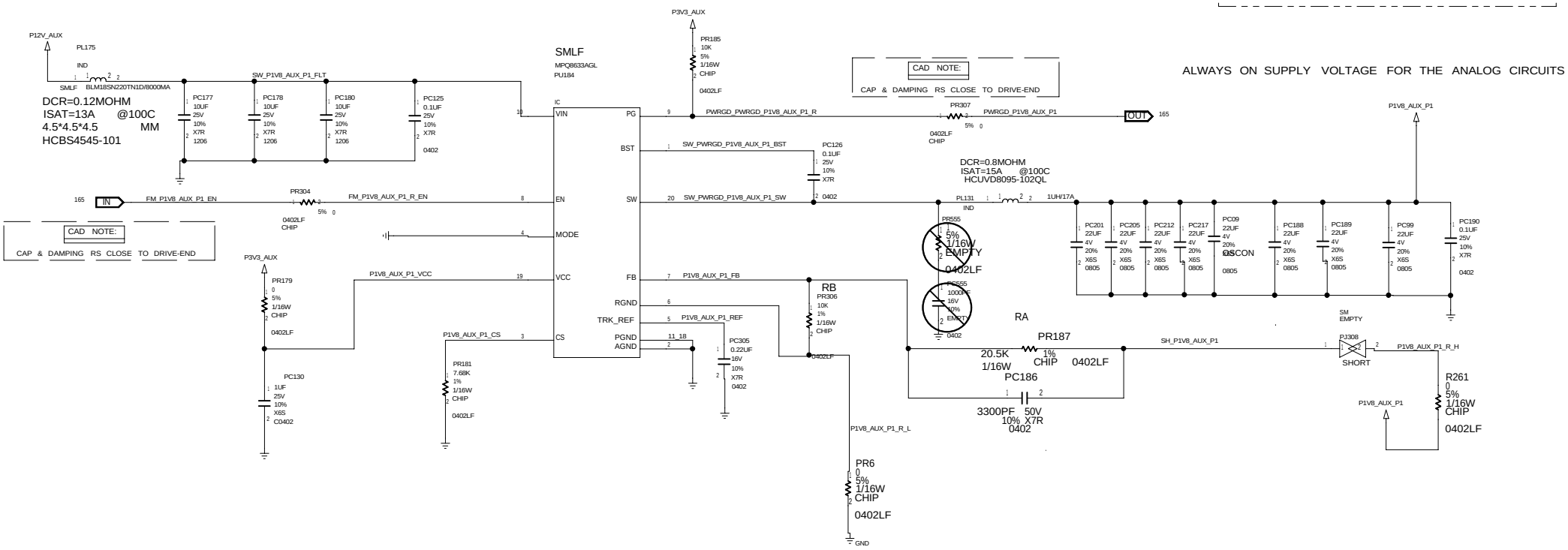


VOUT=0.6(1+RA/RB)=1.8V

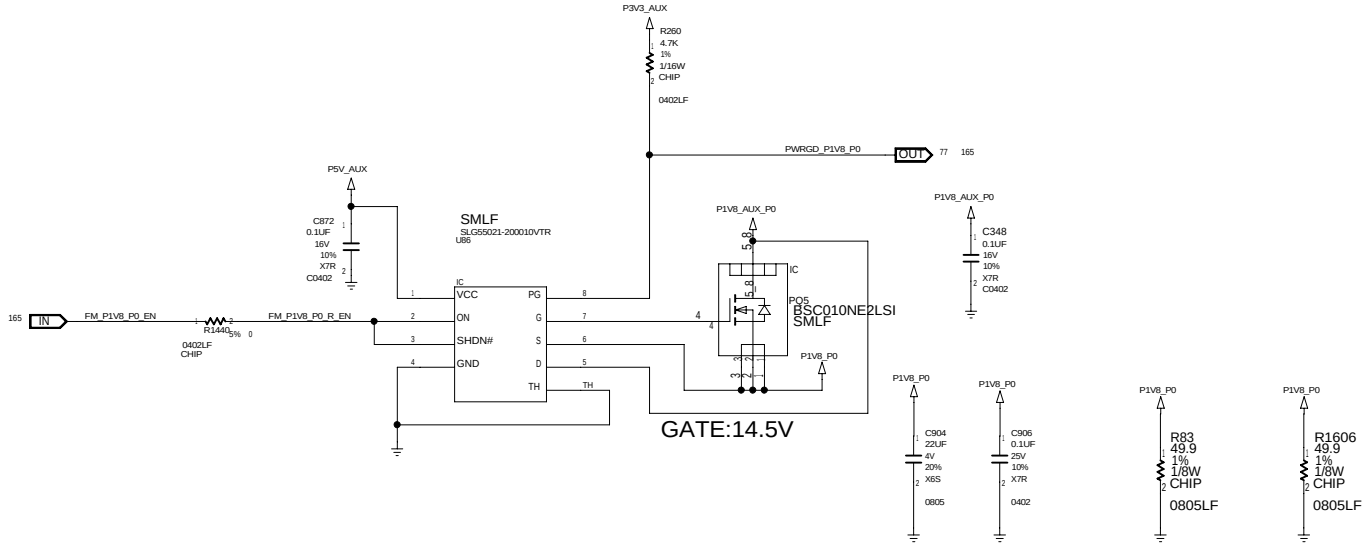
Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:21:24 2017	SHEET 195 OF 226

P1V8_AUX_P1

DESIGN SPECIFICATION
OUTPUT VOLTAGE=1.8V +/-5%
OUTPUT RIPPLE<+/-30MV
DC TOLERANCE = 180MV
TRANSIENT TOLERANCE=+175MV/-165MV
TDC=5.6A
MAX CURRENT=7A
OCP(IMAX*130%)=9.1A
CURRENT STEP=0.5A
SLEW RATE=0.5A/US
WORK FREQUENCY=600KHZ
EFFICIENCY > 90% @TDC

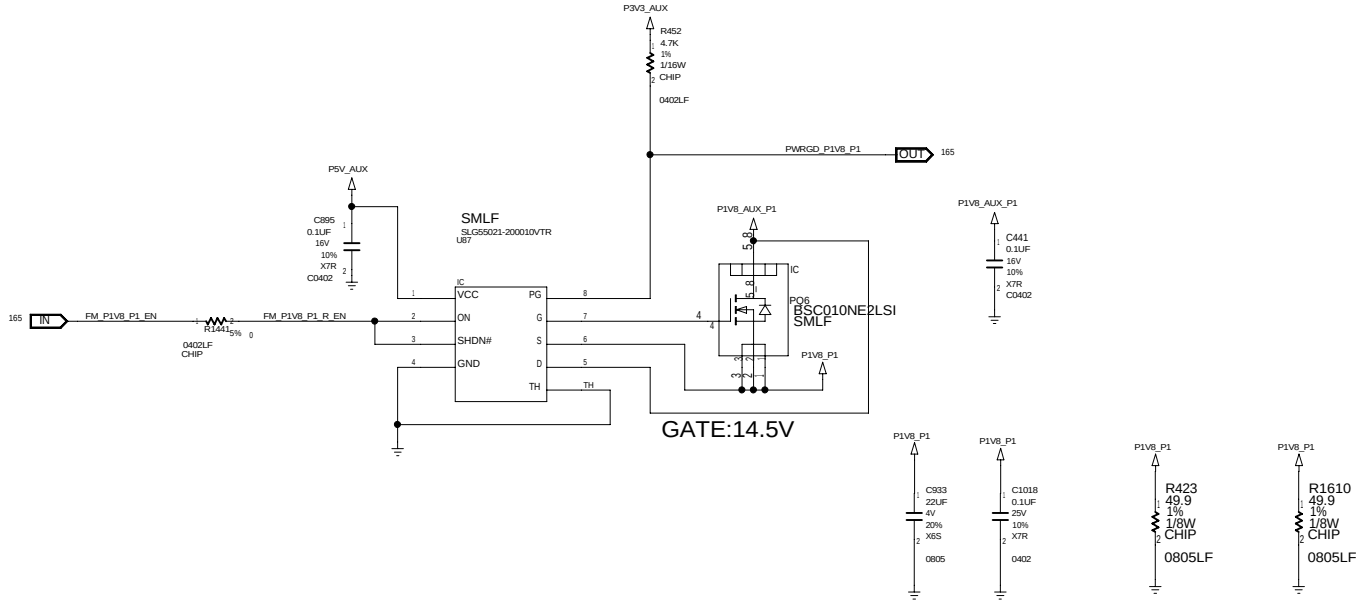


VOUT=0.6(1+RA/RB)=1.8V



P1V8_P0

Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 20:21:25 2017	SHEET 197 OF 226



P1V8_P1

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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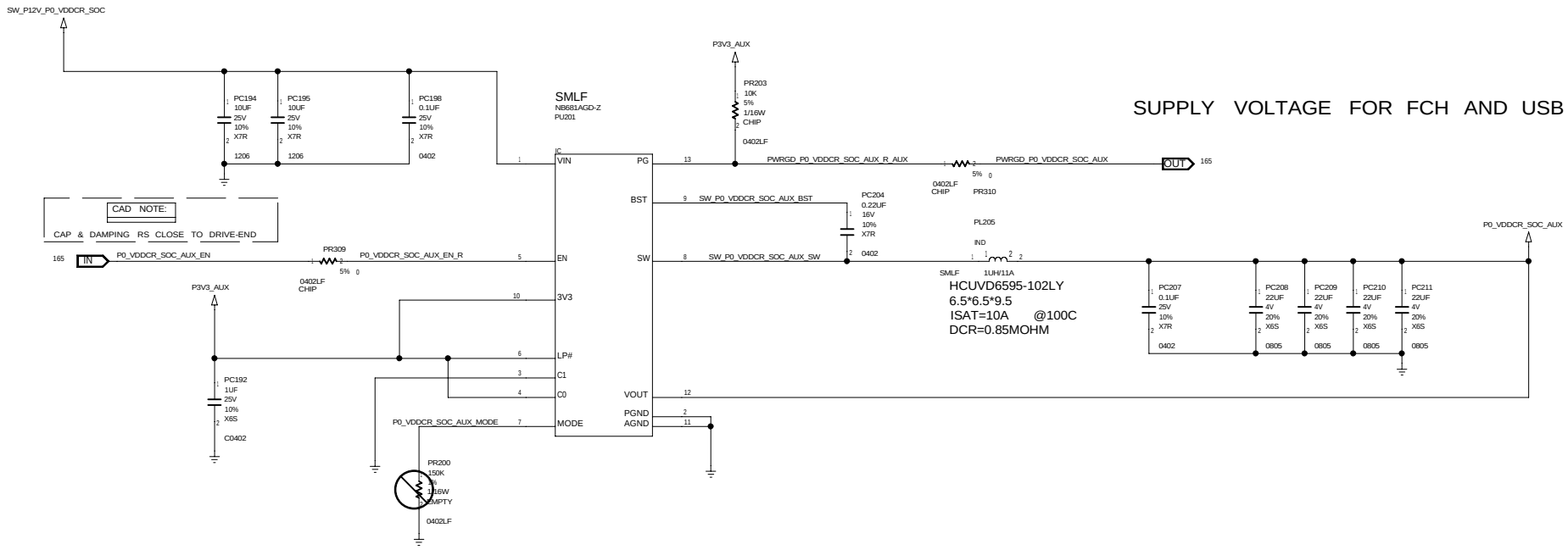
P0_VDDCR_SOC_AUX

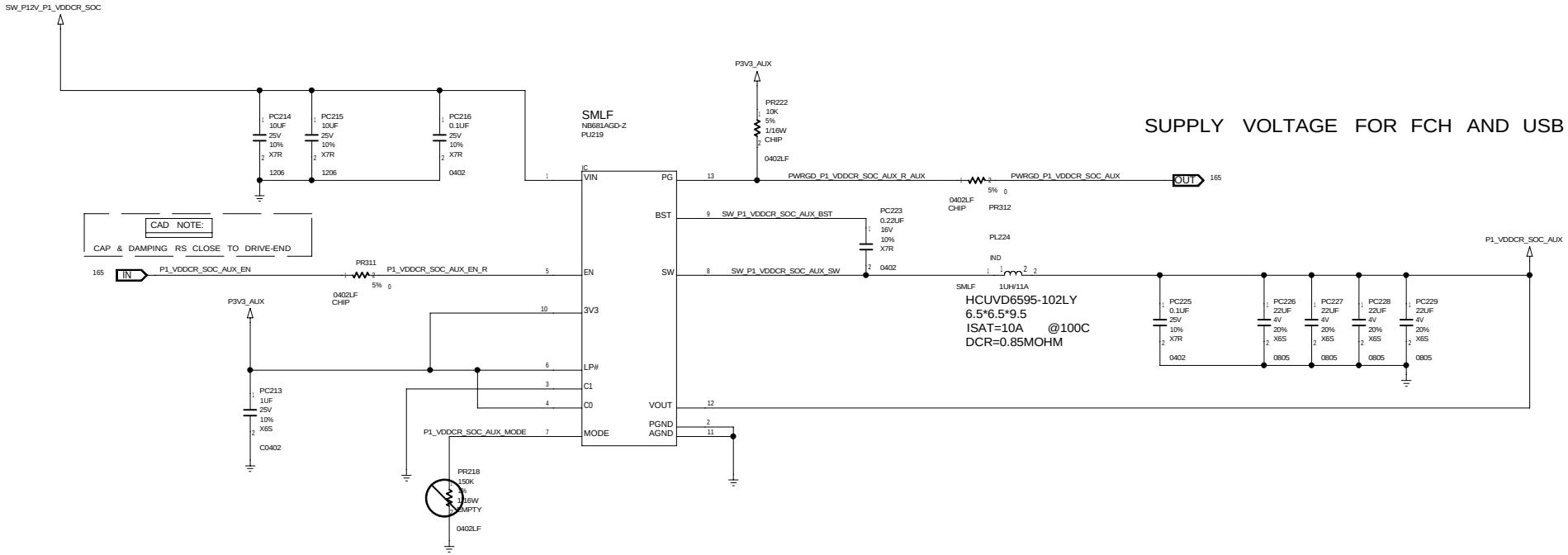
DESIGN SPECIFICATION
OUTPUT VOLTAGE=0.9V+/-5%
OUTPUT RIPPLE<+/-30MV
TRANSIENT TOLERANCE=+/-90MV
TDC=0.7A
MAX CURRENT=1.5A
OVER CURRENT PROTECTION(IC RATING)=7A
CURRENT STEP=0.25A
SLEW RATE=0.25A/US
WORK FREQUENCY=750KHZ
EFFICIENCY>85%@TDC

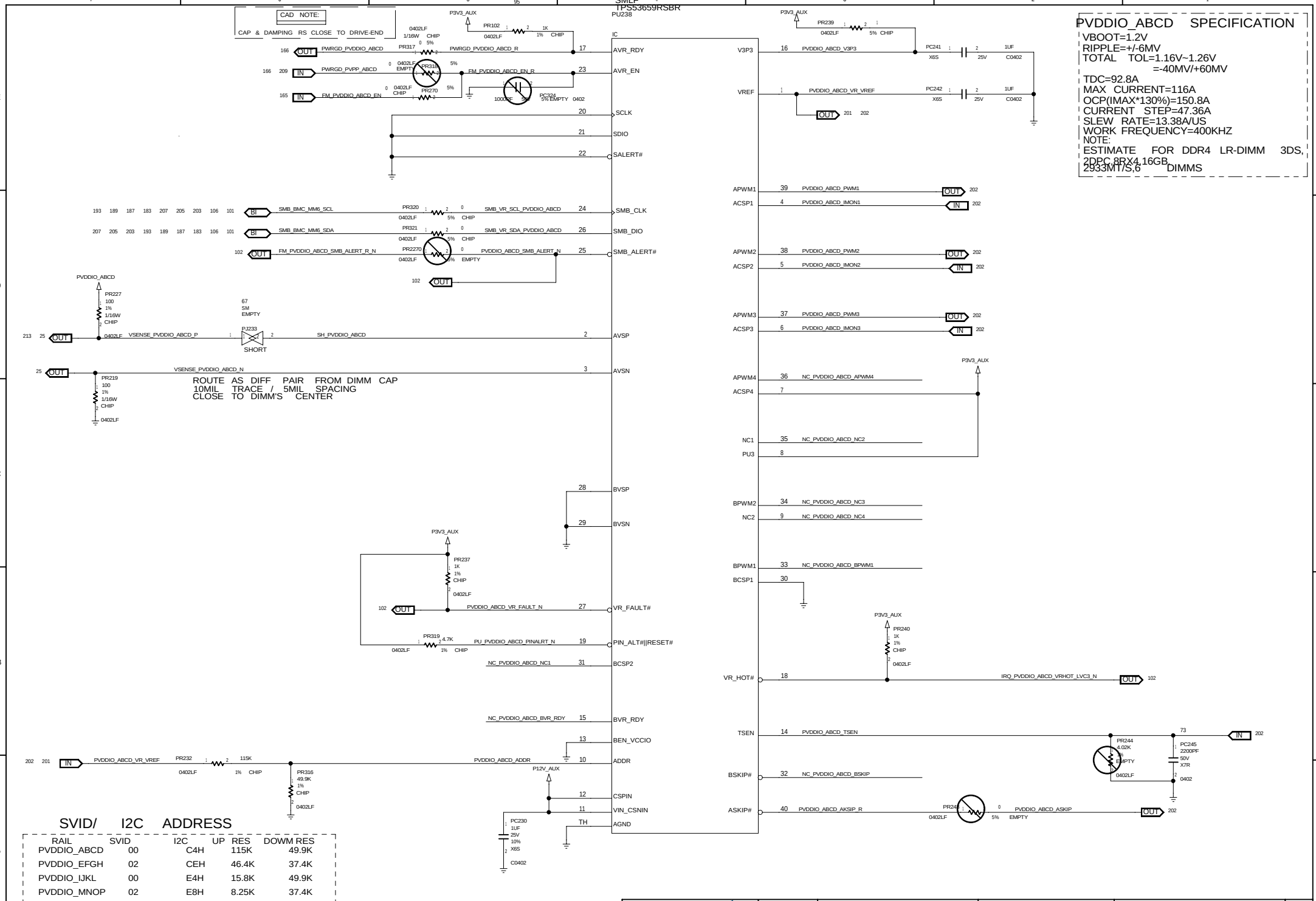
SUPPLY VOLTAGE FOR FCH AND USB



DESIGN SPECIFICATION
OUTPUT VOLTAGE=0.9V+/-5%
OUTPUT RIPPLE<+/-30MV
TRANSIENT TOLERANCE=+/-90MV
TDC=0.7A
MAX CURRENT=1.5A
OVER CURRENT PROTECTION(IC RATING)=7A
CURRENT STEP=0.25A
SLEW RATE=0.25A/US
WORK FREQUENCY=750KHZ
EFFICIENCY>85%@TDC

P1_VDDCR_SOC_AUX





PVDDIO_ABCD SPECIFICATION

VBOOT=1.2V
RIPPLE=+/-6MV
TOTAL TOL=1.16V~1.26V
=-40MV/+60MV
TDC=92.8A
MAX CURRENT=116A
OCP(IMAX*130%)=150.8A
CURRENT STEP=47.36A
SLEW RATE=13.38A/US
WORK FREQUENCY=400KHZ
NOTE:
ESTIMATE FOR DDR4 LR-DIMM 3DS, 2DPC 8RX4 16GB 2933MT/S,6 DIMMS

SVID/ I2C ADDRESS

RAIL	SVID	I2C	UP RES	DOWM RES
PVDDIO_ABCD	00	C4H	115K	49.9K
PVDDIO_EFGH	02	CEH	46.4K	37.4K
PVDDIO_IJKL	00	E4H	15.8K	49.9K
PVDDIO_MNOP	02	E8H	8.25K	37.4K

PVDDIO_ABCD 1/2

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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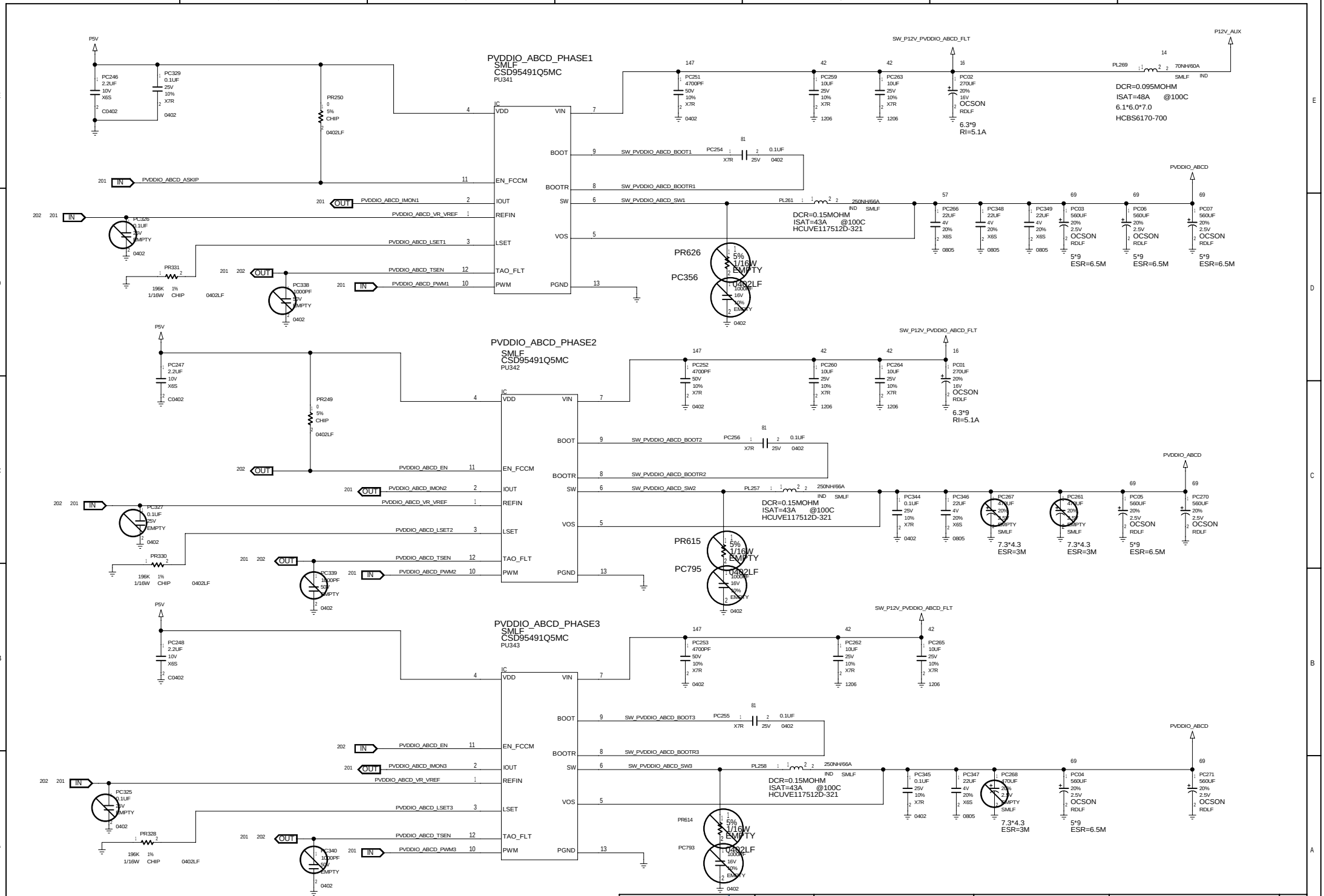

PVDDIO_ABCD 2/2

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C	DATE Fri Dec 15 20:21:23 2017
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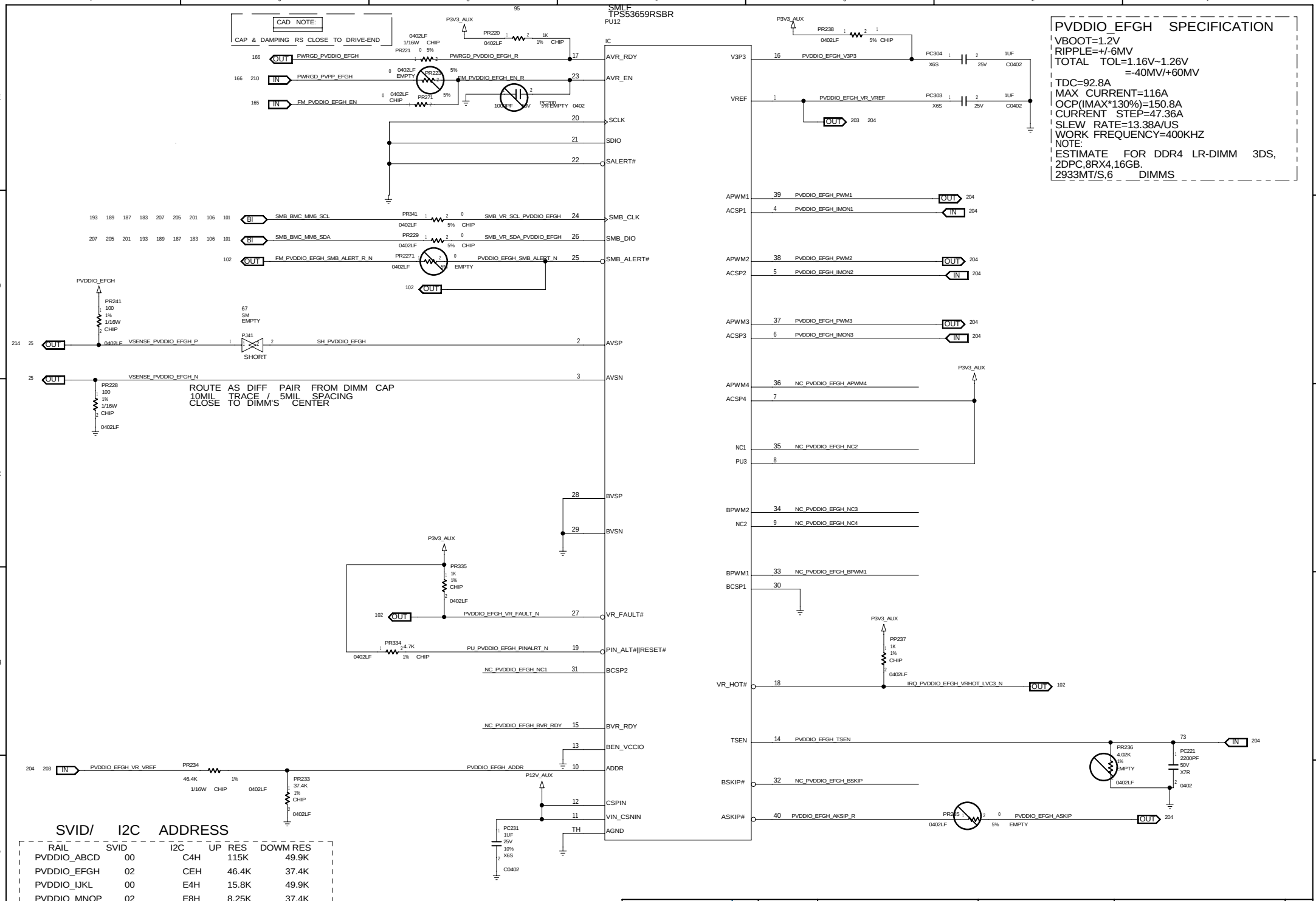
CAD NOTE:
CAP & DAMPING RS CLOSE TO DRIVE-END
SMLF
TPS53659RSBR
PU12
IC
PVDDIO_EFGH SPECIFICATION
VBOOT=1.2V
RIPPLE=+/-6MV
TOTAL TOL=1.16V~1.26V
=-40MV/+60MV
TDC=92.8A
MAX CURRENT=116A
OCP(IMAX*130%)=150.8A
CURRENT STEP=47.36A
SLEW RATE=13.38A/US
WORK FREQUENCY=400KHZ
NOTE:
ESTIMATE FOR DDR4 LR-DIMM 3DS, 2DPC,8RX4,16GB.
2933MT/S,6 DIMMS
ROUTE AS DIFF PAIR FROM DIMM CAP
10MIL TRACE / 5MIL SPACING
CLOSE TO DIMM'S CENTER
SVID/ I2C ADDRESS
RAIL SVID I2C UP RES DOWM RES
PVDDIO_ABCD 00 C4H 115K 49.9K
PVDDIO_EFGH 02 CEH 46.4K 37.4K
PVDDIO_IJKL 00 E4H 15.8K 49.9K
PVDDIO_MNOP 02 E8H 8.25K 37.4K
PVDDIO_EFGH 1/2
Quanta
DEPARTMENT CCBU
DESIGNER
REVIEWER
PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>
REV <Q_REV>
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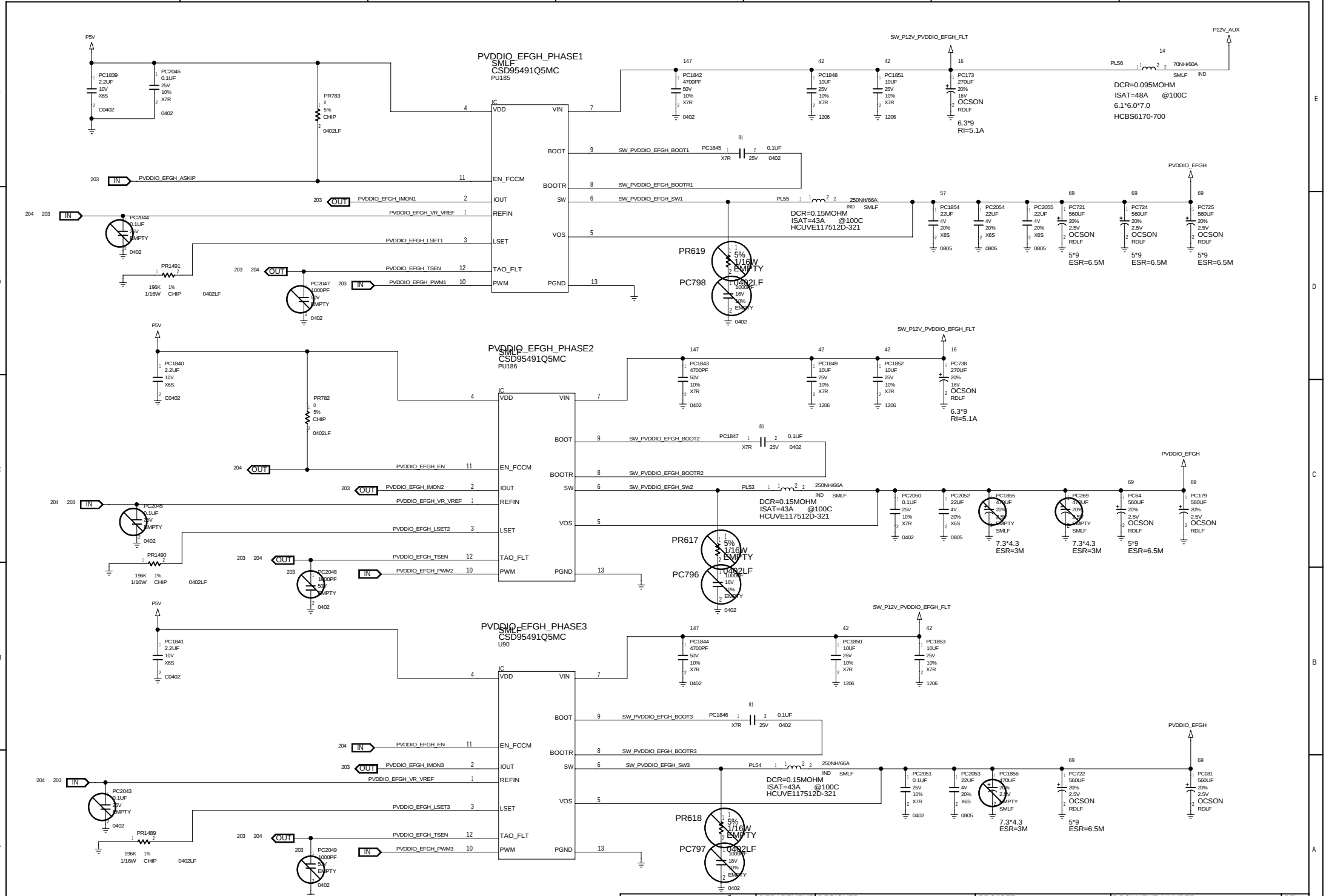

PVDDIO_EFGH 2/2

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C	DATE Fri Dec 15 20:21:23 2017
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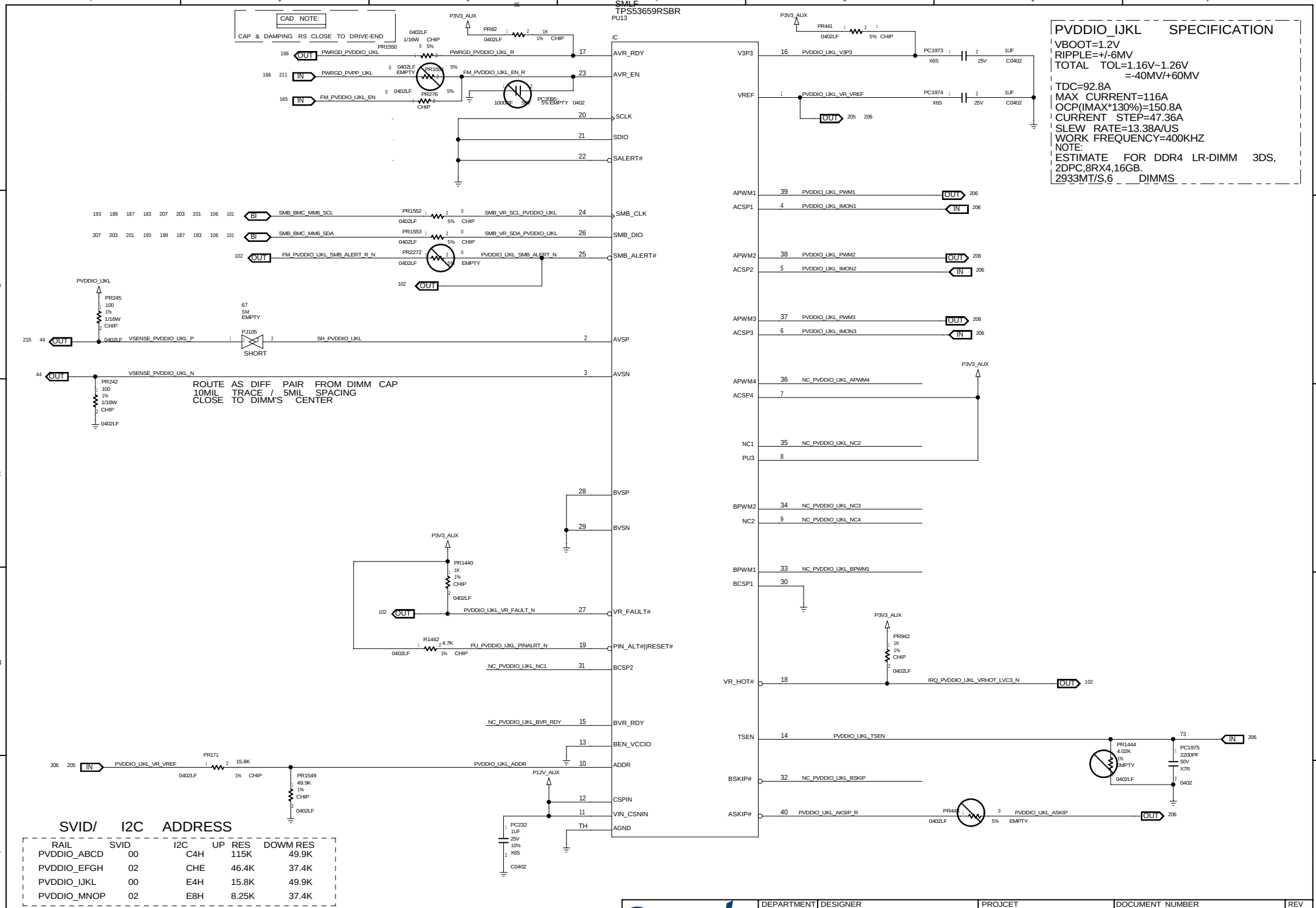
SMLF
TPS53659RSBR
PU13
CAD NOTE:
CAP & DAMPING RS CLOSE TO DRIVE-END
PVDDIO_IJKL SPECIFICATION
VBOOT=1.2V
RIPPLE=+/-6MV
TOTAL TOL=1.16V~1.26V
=-40MV/+60MV
TDC=92.8A
MAX CURRENT=116A
OCP(IMAX*130%)=150.8A
CURRENT STEP=47.36A
SLEW RATE=13.38A/US
WORK FREQUENCY=400KHZ
NOTE:
ESTIMATE FOR DDR4 LR-DIMM 3DS, 2DPC,8RX4,16GB.
2933MT/S,6 DIMMS
ROUTE AS DIFF PAIR FROM DIMM CAP
10MIL TRACE / 5MIL SPACING
CLOSE TO DIMM'S CENTER
SVID/ I2C ADDRESS
RAIL SVID I2C UP RES DOWM RES
PVDDIO_ABCD 00 C4H 115K 49.9K
PVDDIO_EFGH 02 CHE 46.4K 37.4K
PVDDIO_IJKL 00 E4H 15.8K 49.9K
PVDDIO_MNOP 02 E8H 8.25K 37.4K
PVDDIO_IJKL 1/2
Quanta
DEPARTMENT CCBU
DESIGNER
REVIEWER
PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>
REV <Q_REV>
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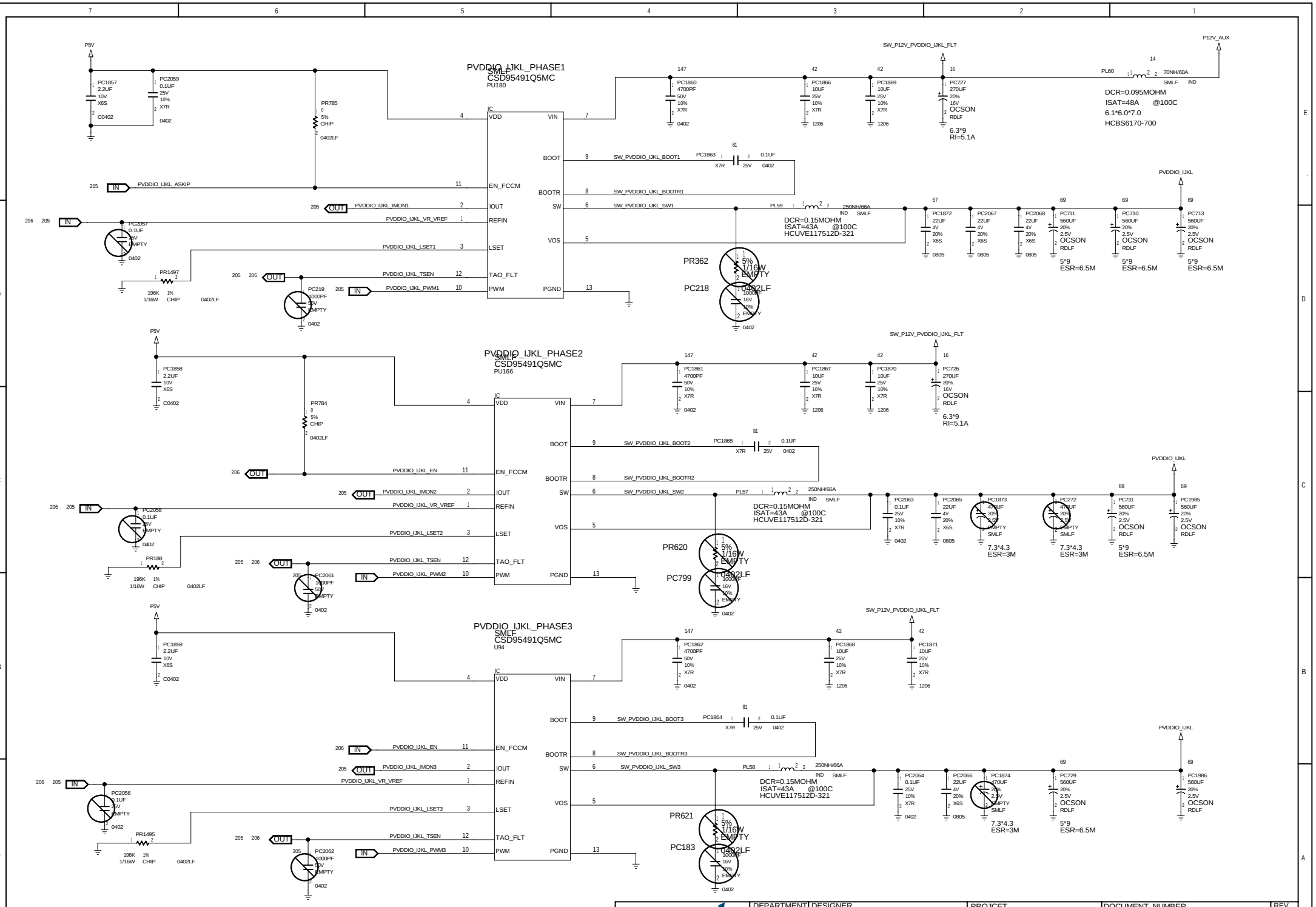

PVDDIO_IJKL 2/2

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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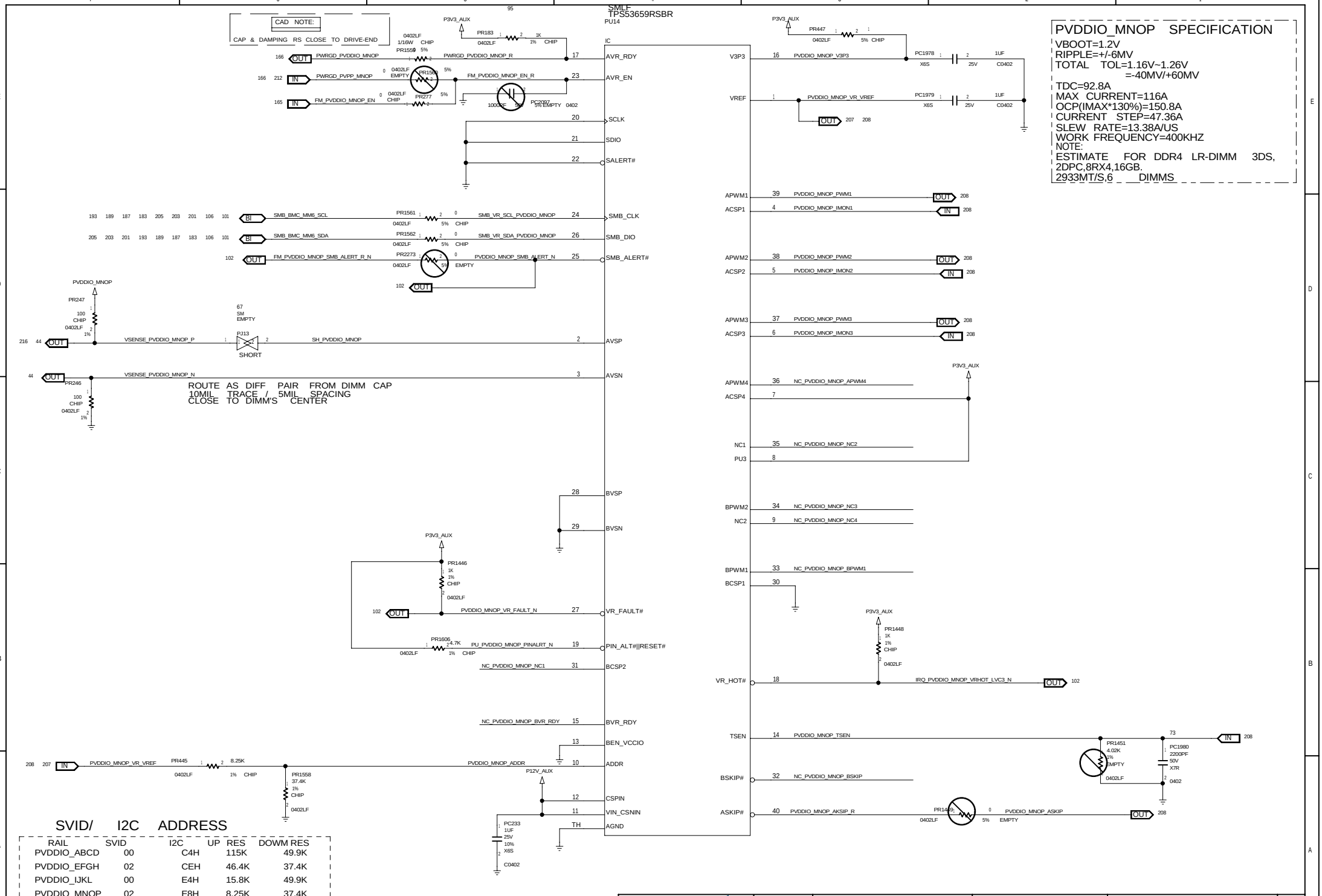
CAD NOTE:
CAP & DAMPING RS CLOSE TO DRIVE-END
SMLF
TPS53659RSBR
PU14
IC
PVDDIO_MNOP SPECIFICATION
VBOOT=1.2V
RIPPLE=+/-6MV
TOTAL TOL=1.16V~1.26V
=-40MV/+60MV
TDC=92.8A
MAX CURRENT=116A
OCP(IMAX*130%)=150.8A
CURRENT STEP=47.36A
SLEW RATE=13.38A/US
WORK FREQUENCY=400KHZ
NOTE:
ESTIMATE FOR DDR4 LR-DIMM 3DS, 2DPC,8RX4,16GB.
2933MT/S,6 DIMMS
ROUTE AS DIFF PAIR FROM DIMM CAP
10MIL TRACE / 5MIL SPACING
CLOSE TO DIMM'S CENTER
SVID/ I2C ADDRESS
RAIL SVID I2C UP RES DOWM RES
PVDDIO_ABCD 00 C4H 115K 49.9K
PVDDIO_EFGH 02 CEH 46.4K 37.4K
PVDDIO_IJKL 00 E4H 15.8K 49.9K
PVDDIO_MNOP 02 E8H 8.25K 37.4K
PVDDIO_MNOP 1/2
Quanta
DEPARTMENT CCBU
DESIGNER
REVIEWER
PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>
REV <Q_REV>
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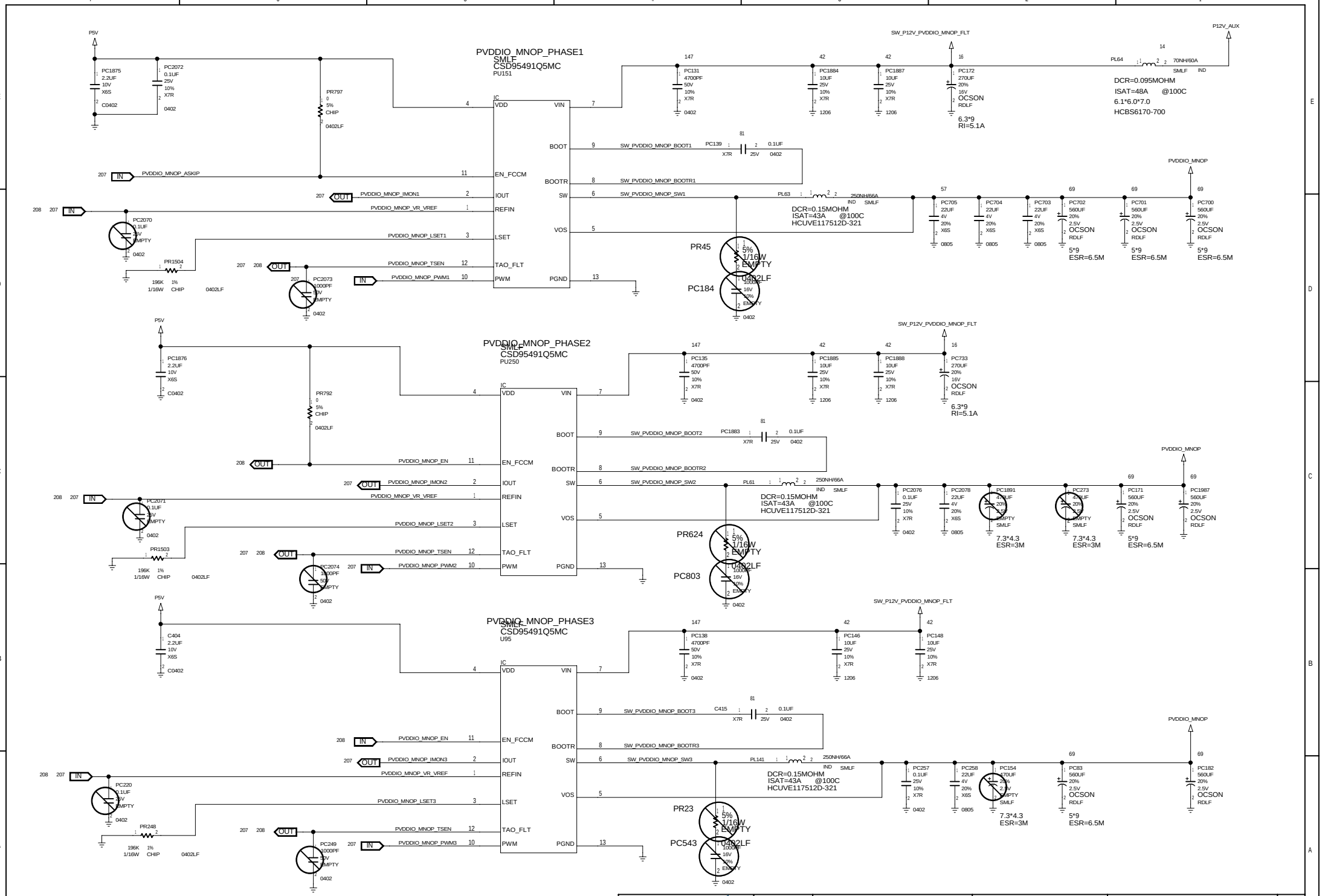

PVDDIO_MNOP 2/2

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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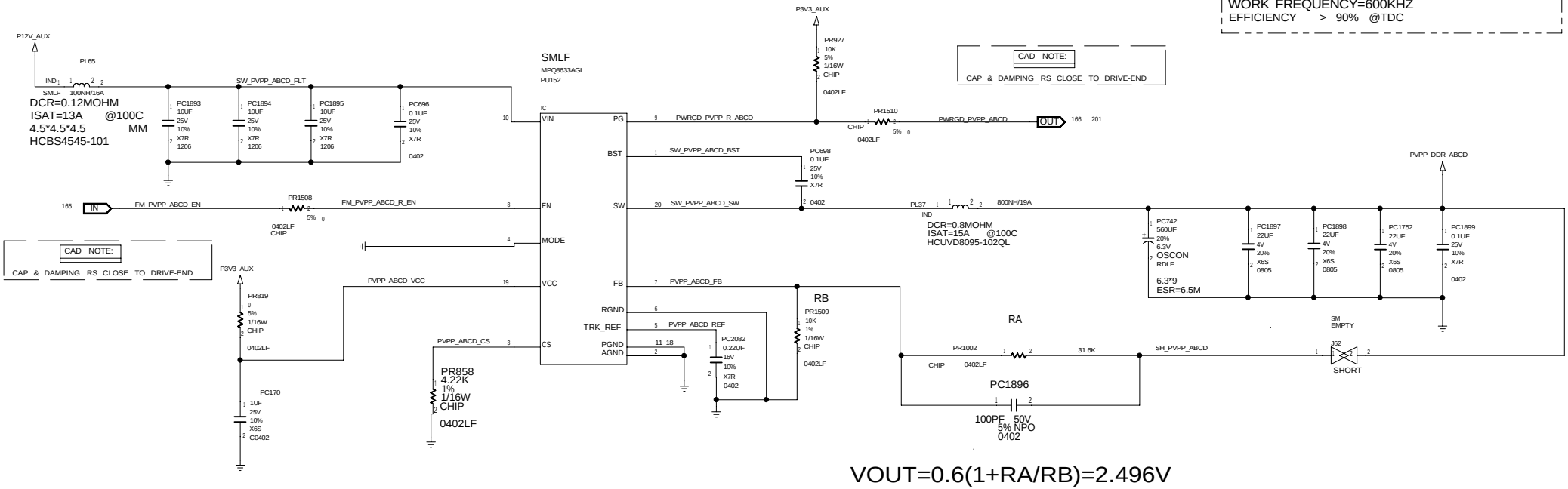
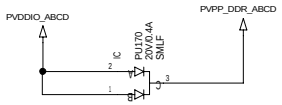
PVPP_DDR_ABCD

PVPP_DDR_ABCD SPECIFICATION
OUTPUT VOLTAGE=2.575V +/-3%
OUTPUT RIPPLE<+/-25MV
DC TOLERANCE = +/- 37.5MV
TRANSIENT TOLERANCE=+175MV/-165MV
TDC=9.6A
MAX CURRENT=12A
OCP(IMAX*130%)=15.6A
CURRENT STEP=5.3A
SLEW RATE=21.5A/US
WORK FREQUENCY=600KHZ
EFFICIENCY > 90% @TDC



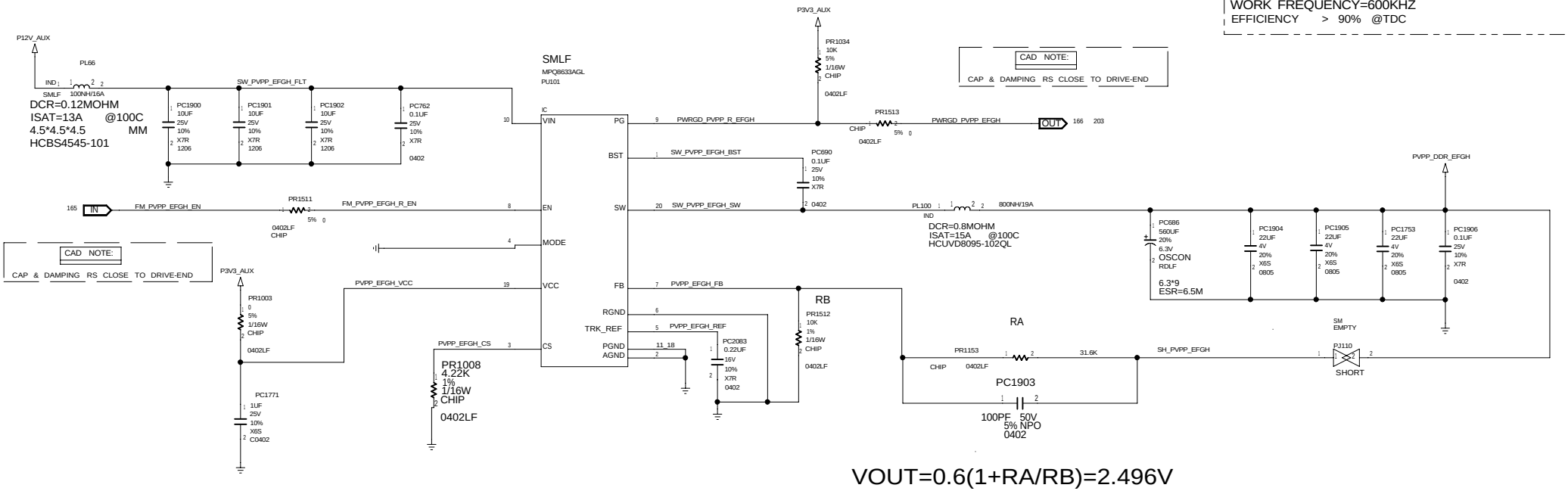
VOUT=0.6(1+RA/RB)=2.496V



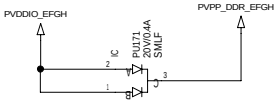
PVPP_DDR_ABCD	Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C	DATE Fri Dec 15 20:22:06 2017	SHEET 209 OF 226

PVPP_DDR_EFGH

PVPP_DDR_EFGH SPECIFICATION
OUTPUT VOLTAGE=2.575V +/-3%
OUTPUT RIPPLE<+/-25MV
DC TOLERANCE = +/- 37.5MV
TRANSIENT TOLERANCE=+175MV/-165MV
TDC=9.2A
MAX CURRENT=12A
OCP(IMAX*130%)=15.6A
CURRENT STEP=5.3A
SLEW RATE=21.5A/US
WORK FREQUENCY=600KHZ
EFFICIENCY > 90% @TDC



VOUT=0.6(1+RA/RB)=2.496V

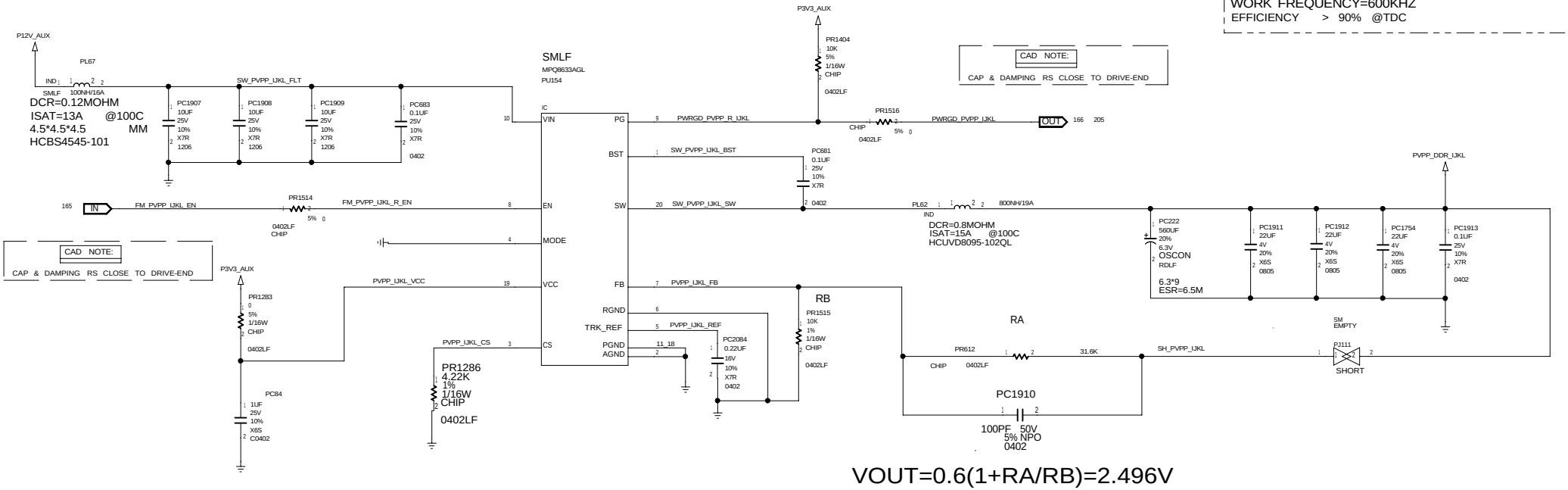


Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> REV <Q_REV>
			SIZE C DATE Fri Dec 15 20:22:06 2017	SHEET 210 OF 226

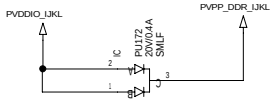
PVPP_DDR_EFGH

PVPP_DDR_IJKL

PVPP_DDR_IJKL SPECIFICATION
OUTPUT VOLTAGE=2.575V +/-3%
OUTPUT RIPPLE<+/-25MV
DC TOLERANCE = +/- 37.5MV
TRANSIENT TOLERANCE=+175MV/-165MV
TDC=9.6A
MAX CURRENT=12A
OCP(IMAX*130%)=15.6A
CURRENT STEP=5.3A
SLEW RATE=21.5A/US
WORK FREQUENCY=600KHZ
EFFICIENCY > 90% @TDC



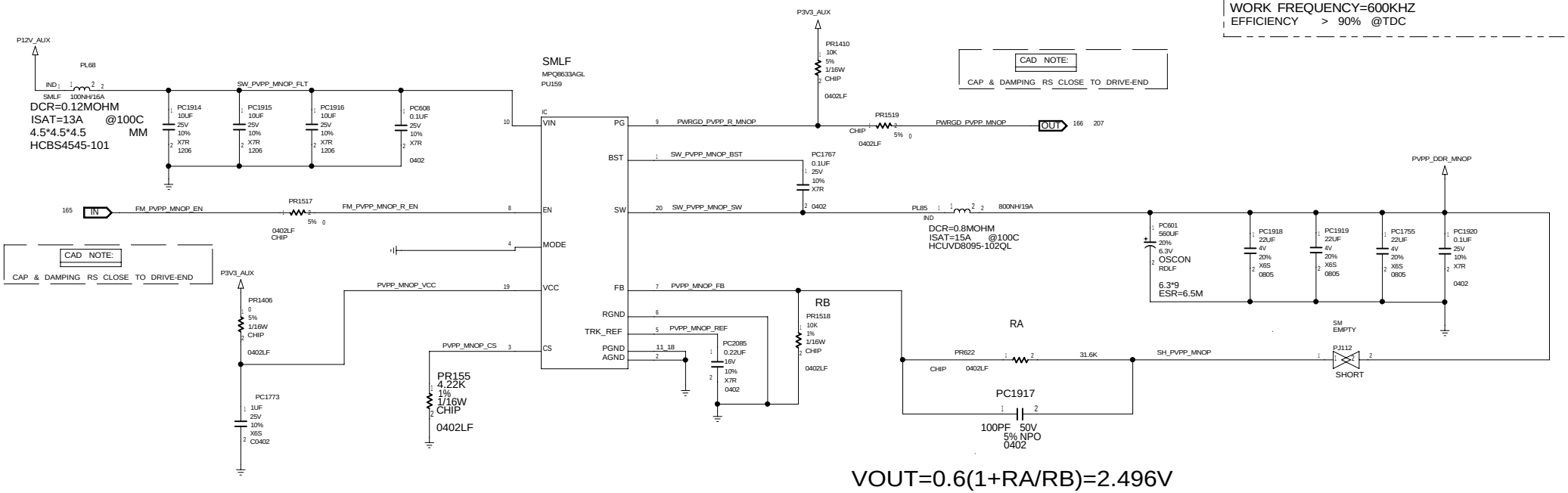
VOUT=0.6(1+RA/RB)=2.496V



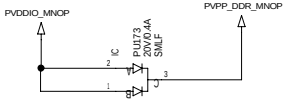
PVPP_DDR_IJKL	Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER> / REV <Q_REV>
				SIZE C	DATE Fri Dec 15 20:22:07 2017 / SHEET 211 OF 226

PVPP_DDR_MNOP

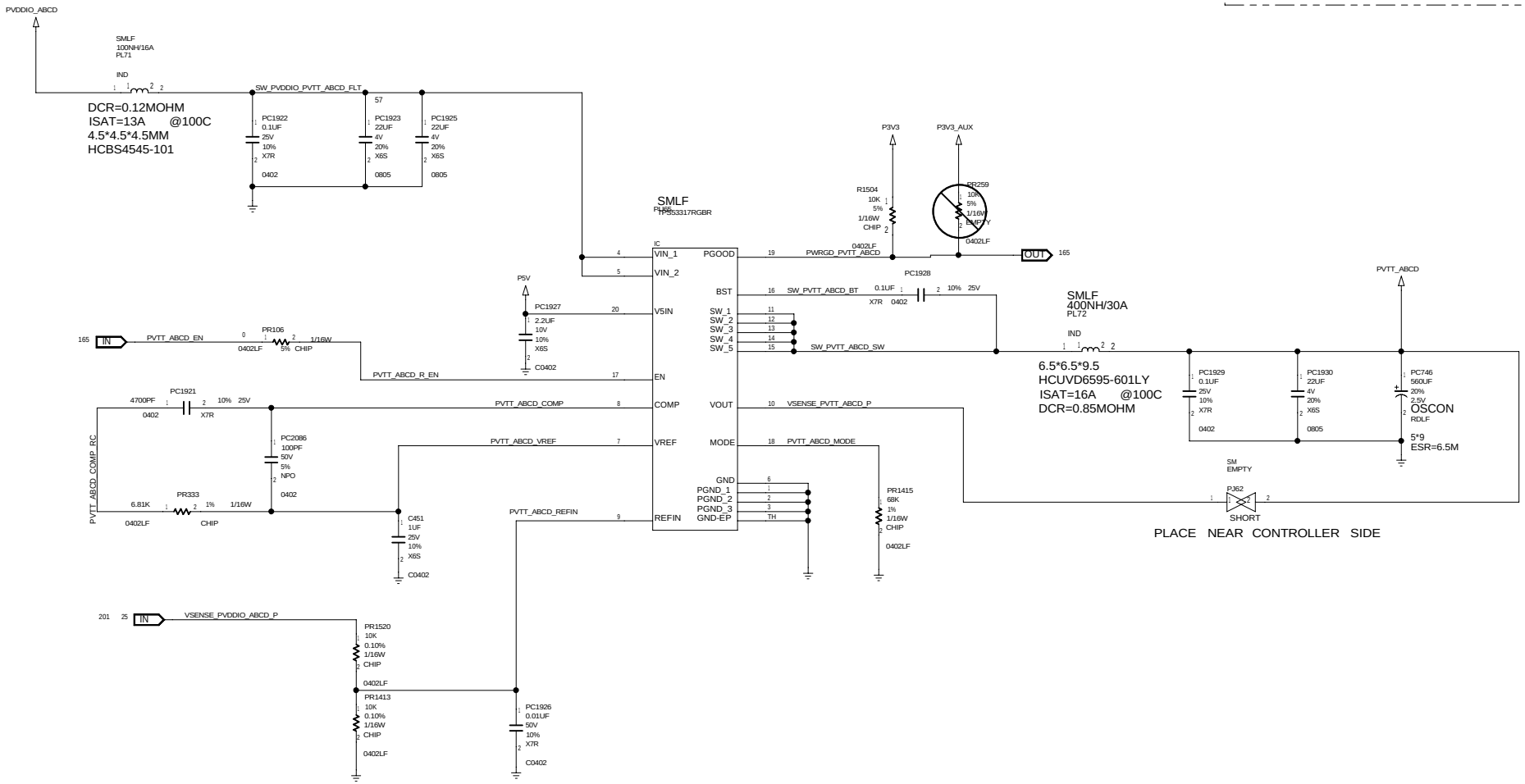
PVPP_DDR_MNOP SPECIFICATION
OUTPUT VOLTAGE=2.575V +/-3%
OUTPUT RIPPLE<+/-25MV
DC TOLERANCE = +/- 37.5MV
TRANSIENT TOLERANCE=+175MV/-165MV
TDC=9.6A
MAX CURRENT=12A
OCP(IMAX*130%)=15.6A
CURRENT STEP=5.3A
SLEW RATE=21.5A/US
WORK FREQUENCY=600KHZ
EFFICIENCY > 90% @TDC



VOUT=0.6(1+RA/RB)=2.496V

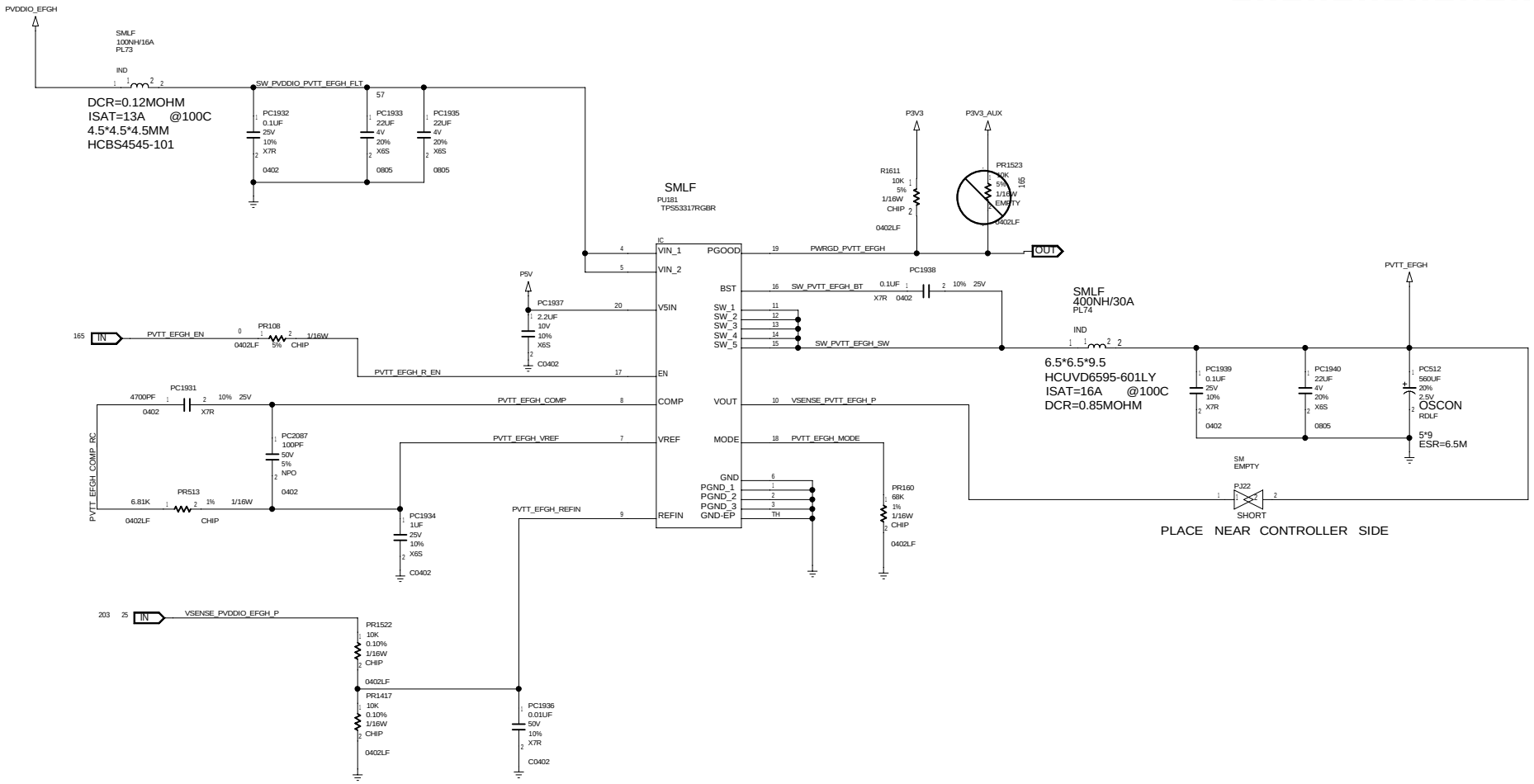


PVTT_ABCD SPECIFICATION
VOUT = 0.5*VDDQ = 0.607V
DC TOLERANCE = +/- 6MV
RIPPLE=+/-9MV
TOTAL TOL=0.555V~0.651V@DIMM
=0.542V~0.662V@RTT
TDC=SINKING=1.824A,SOURCING=1.37A
MAX CURRENT=2.28A
OCP(IMAX*130%)=5.4A
CURRENT STEP=2.77A,-1.4A~+1.37A
SLEW RATE=6A/US
WORK FREQUENCY=600KHZ



PVTT_ABCD	Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C	DATE Fri Dec 15 20:22:07 2017	SHEET 213 OF 226

PVTT_EFGH SPECIFICATION
VOUT = 0.5*VDDQ = 0.607V
DC TOLERANCE = +/- 6MV
RIPPLE=+/-9MV
TOTAL TOL=0.555V~0.651V@DIMM
=0.542V~0.662V@RTT
TDC=SINKING=1.824A,SOURCING=1.37A
MAX CURRENT=2.28A
OCP(IMAX*130%)=5.4A
CURRENT STEP=2.77A,-1.4A~+1.37A
SLEW RATE=6A/US
WORK FREQUENCY=600KHZ



PVTT_EFGH

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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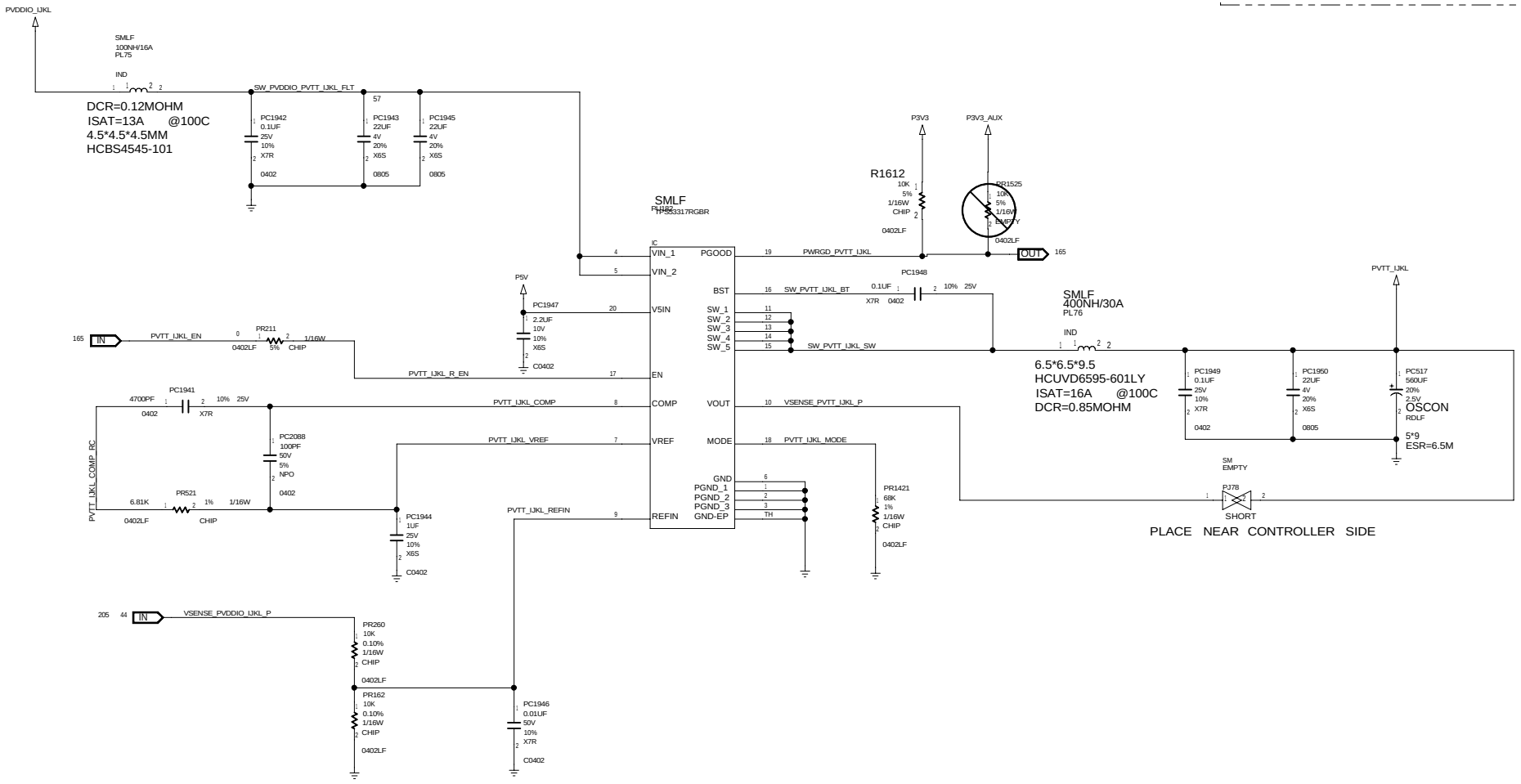
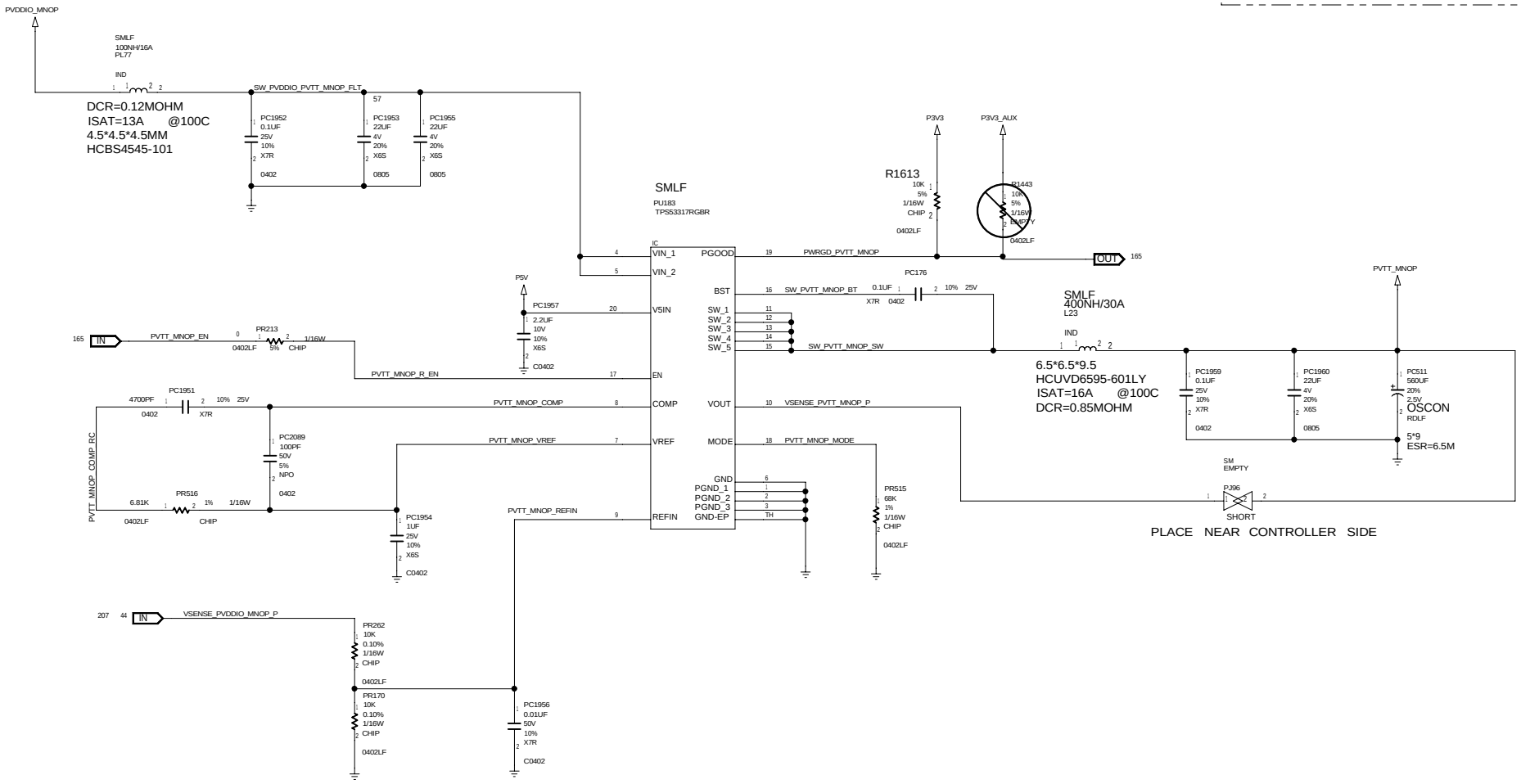
PVTT_IJKL SPECIFICATION
VOUT = 0.5*VDDQ = 0.607V
DC TOLERANCE = +/- 6MV
RIPPLE=+/-9MV
TOTAL TOL=0.555V~0.651V@DIMM
=0.542V~0.662V@RTT
TDC=SINKING=1.824A,SOURCING=1.37A
MAX CURRENT=2.28A
OCP(IMAX*130%)=5.4A
CURRENT STEP=2.77A,-1.4A~+1.37A
SLEW RATE=6A/US
WORK FREQUENCY=600KHZ



PVTT_IJKL	Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>
DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>	SIZE C	DATE Fri Dec 15 20:22:07 2017	SHEET 215 OF 226

PVTT_MNOP SPECIFICATION
VOUT = 0.5*VDDQ = 0.607V
DC TOLERANCE = +/- 6MV
RIPPLE=+/-9MV
TOTAL TOL=0.555V~0.651V@DIMM
=0.542V~0.662V@RTT
TDC=SINKING=1.824A,SOURCING=1.37A
MAX CURRENT=2.28A
OCP(IMAX*130%)=5.4A
CURRENT STEP=2.77A,-1.4A~+1.37A
SLEW RATE=6A/US
WORK FREQUENCY=600KHZ



PVTT_MNOP

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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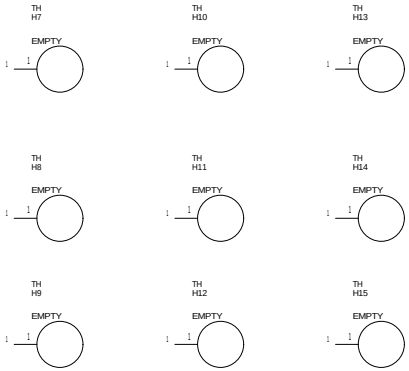
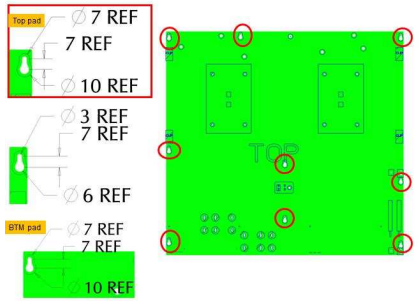
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:43:00 2017	SHEET 217 OF 226

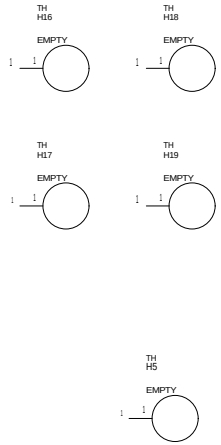
MLB SCREW HOLE
HOLE_C7D3_6B7_OB7XC5N_NPM
QTY: 9

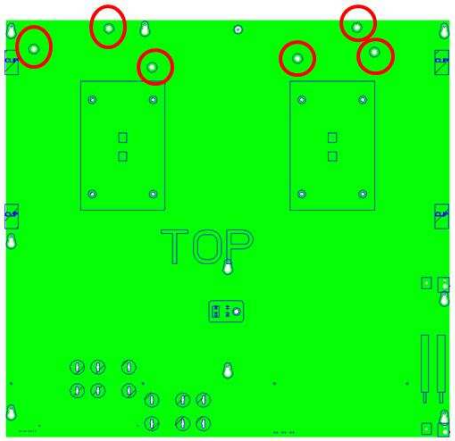
ITEM1

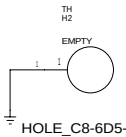




AIR DEFLECTOR AND HS HOLE
HOLE_C7D5B9_NPM
QTY: 6







TP_BOM_ME_1
NA

THUMB SCREW

QTY: 1

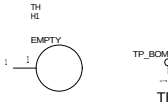
HOLE_C8-6D5-6B9_OB7XC4-5B_NPB
FOR THUMB SCREW
QTY: 1

ITEM 2

HOLE_C8D5-13B9_NPB
SMD NUT HOLE
NEED POP SMD NUT
QTY: 1

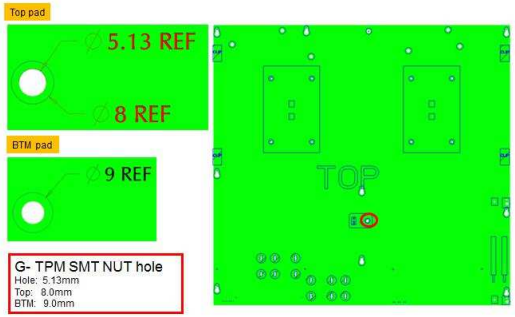
ITEM 5

CLIP X4

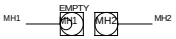


TPM SMT NUT

QTY: 1

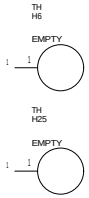


MECH
HOLE2_R11X14-5D2-3_4-3B9N_P0-5W5-5_NPM
H3

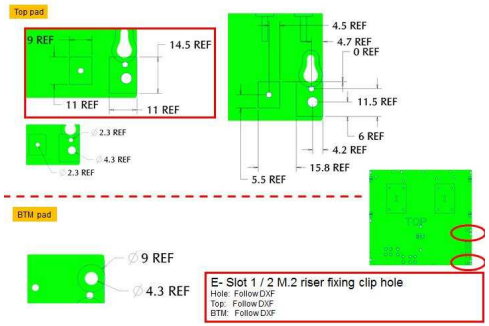


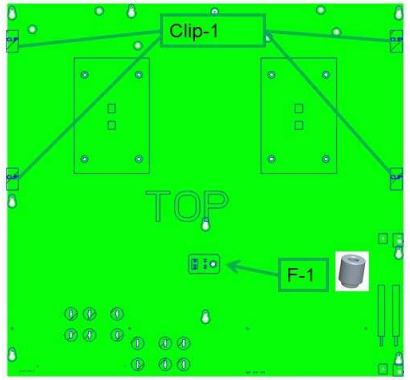
MECH
HOLE2_R11X14-5D2-3_4-3B9N_P0-5W5-5_NPM
H4

HOLE2_R11X14-5D2-3_4-3B9N_P0-5W5-5_NPM
HOLE FOR SLOT 1 / 2 M.2 RISER FIXING CLIP HOLE
QTY: 4



HOLE_R9X11D2-3TN_NPM
FOR M.2 RISER OF SLOT2
QTY: 2





G-1 : MBT6M020010 (1pcs / per MB)
Clip 1 : JXS2V013010 (4pcs / per MB)

SCREW HOLES

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:37:13 2017	SHEET 219 OF 226

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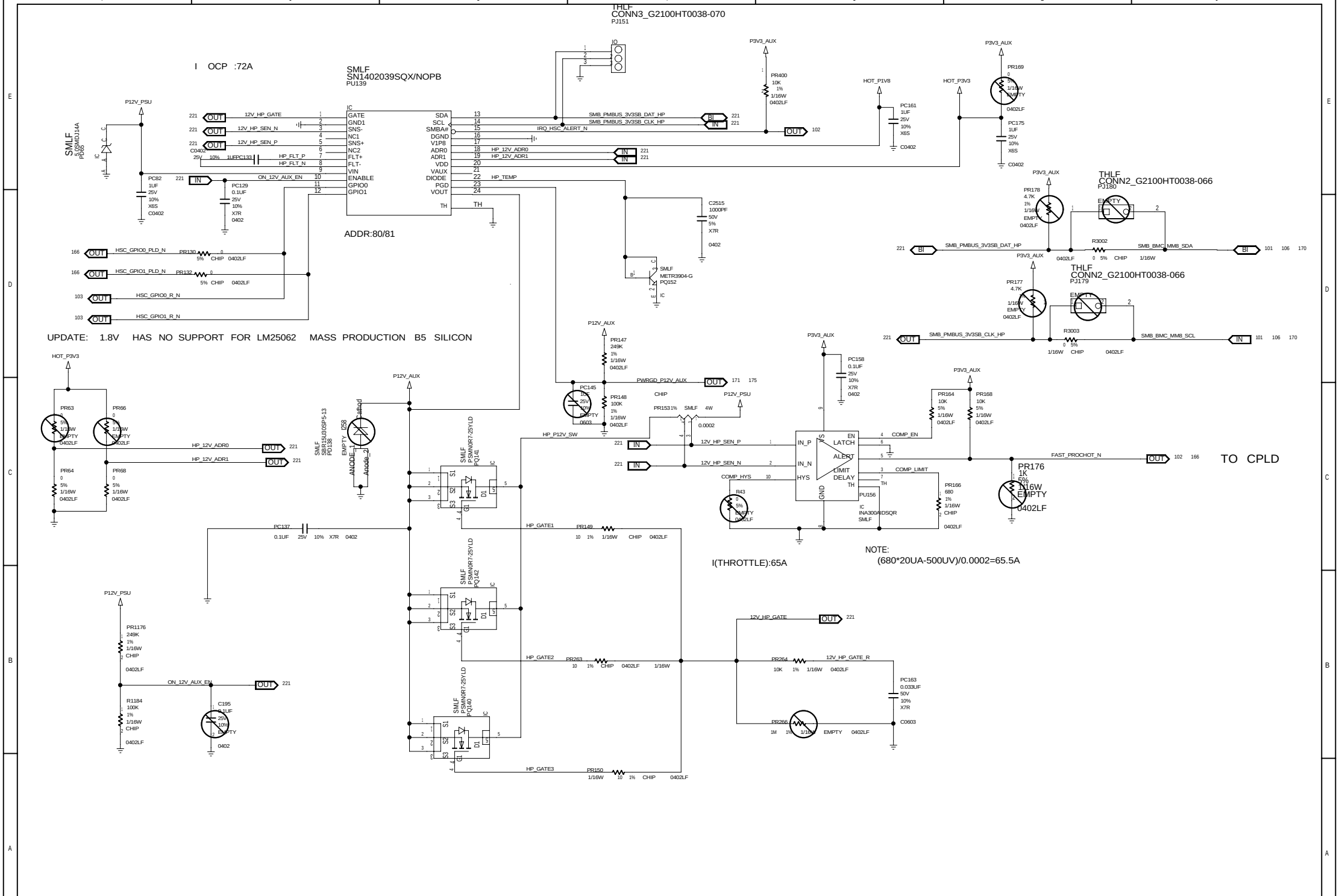
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:37:14 2017	SHEET 220 OF 226



HOT SWAP

Quanta	DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
	CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>
			SIZE C	DATE Fri Dec 15 20:22:08 2017	SHEET 221 OF 226

UV CIRCUIT

	MIN	NORMAL	MAX
R2	17.82	18	18.18
R1	4.94	4.99	5.04
2.5_DIODE	2.48	2.5	2.52

P12V TRIP POINT IS 11.52V

11.52*(R1/R1+R2)=2.5

11VMAX

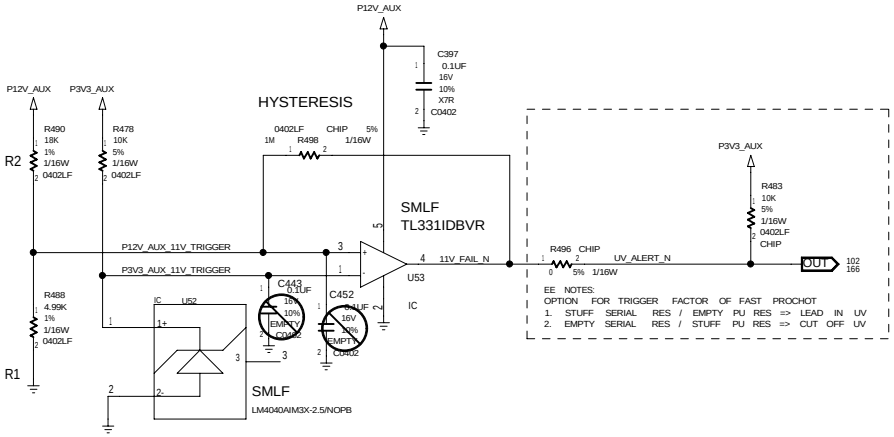
$$V = \frac{(R1_{MIN} + R2_{MAX})*2.5_DIODE}{R1_{MIN}}_{MAX}$$

=11.79V

11VMIN

$$V = \frac{(R1_{MAX} + R2_{MIN})*2.5_DIODE}{R1_{MAX}}_{MIN}$$

=11.25V



UV FOR ADR

	MIN	NORMAL	MAX
R2	16.73	16.9	17.07
R1	4.9401	4.99	5.04
2.5_DIODE	2.48	2.5	2.52

P12V TRIP POINT IS 10.967V

10.967*(R1/R1+R2)=2.5

10.5VMAX

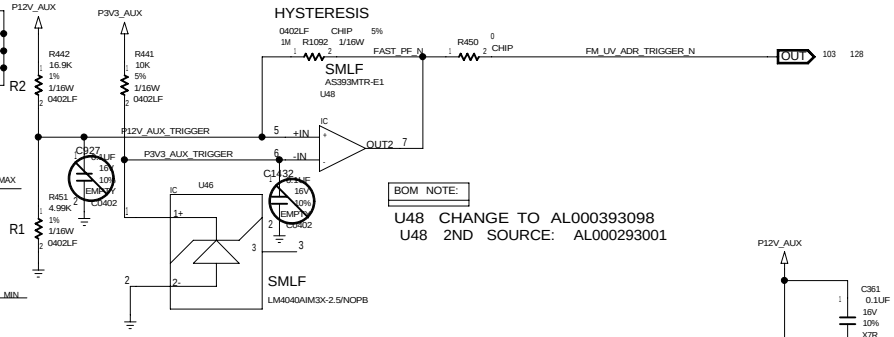
$$V = \frac{(R1_{MIN} + R2_{MAX})*2.5_DIODE}{R1_{MIN}}_{MAX}$$

=11.23V

10.5VMIN

$$V = \frac{(R1_{MAX} + R2_{MIN})*2.5_DIODE}{R1_{MAX}}_{MIN}$$

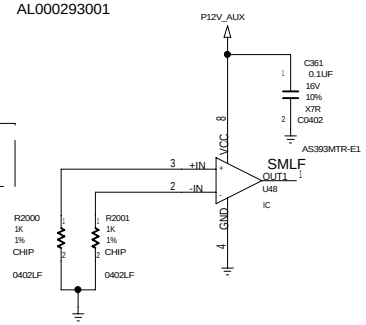
=10.71V



BOM NOTE:

U48 CHANGE TO AL000393098
U48 2ND SOURCE: AL000293001

BOM NOTE:U46,U52 CHANGE TO AL404025013
TO IMPROVE DERATING TEMPERATURE



VOLTAGE MONITOR

DEPARTMENT	DESIGNER	PROJCET	DOCUMENT NUMBER	REV
CCBU	REVIEWER	<Q_PROJ>	<Q_NUMBER>	<Q_REV>

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MECH
WEEE
DM2

EMPTY
DUMMY_SYMBOL

MECH
PB-E1_SMALL
DM3

EMPTY
DUMMY_SYMBOL

MECH
PCB_VENDOR_LOGO_15X8
DM4

EMPTY
DUMMY_SYMBOL

BACKPLATE X2

TP2
NA

TP3
NA

SAM BRACKET X2

TP4
NA

TP5
NA

CARRIER FRAME X2

-> NO NEED, AMD WILL WHIP CPU WITH CARRIER FRAME

DUMMY SYMBOL

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
			SIZE C	DATE Fri Dec 15 20:22:09 2017	SHEET 223 OF 226

PCB PN

PCB
NA

MAC LABEL

MAC_LABEL
NA

PN LABEL

HCS09004010
MECH
PCBA_LABEL_15X5
PN_LABEL

MECH
DUMMY_SYMBOL

BIOS LABEL

BMC LABEL

SN LABEL

HCS67003010
MECH
BARCODE
SN_LABEL

MECH
DUMMY_SYMBOL

AIRDUCT_RIGHT

AIRDUCT_LEFT

LASER MARK

COMPONENT SIDE(TOP)
MECH
LASER_MARK_LABELS_10X10B
DM5

EMPTY
DUMMY_SYMBOL

SOLDER SIDE(BOT)
MECH
LASER_MARK_LABELS_10X10B
DM6

EMPTY
DUMMY_SYMBOL

SCREW FOR M.2

SCREW FOR M.2

SCREW HLOE

TH
H23
EMPTY

TH
H24
EMPTY

TH
H28
EMPTY

TH
H30
EMPTY

NUT FOR LAN MEZZ

DUMMY SYMBOL

Quanta	DEPARTMENT CCBU	DESIGNER / REVIEWER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
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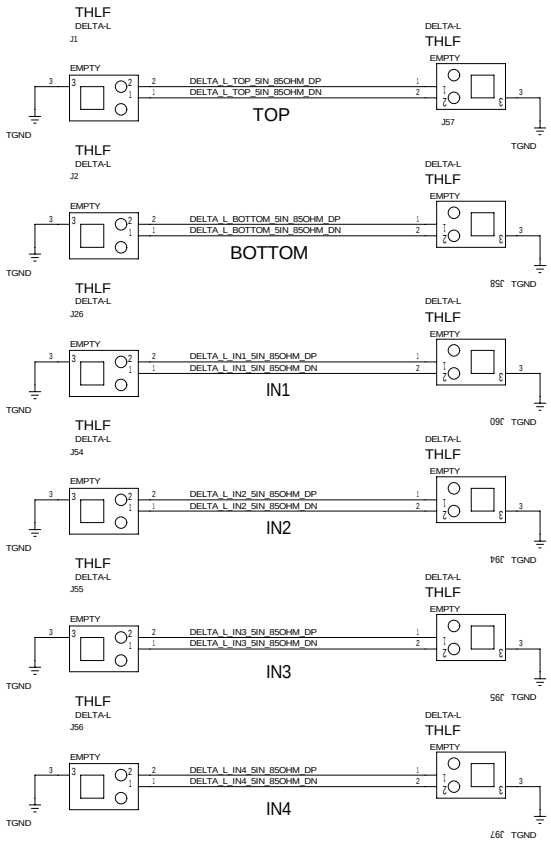
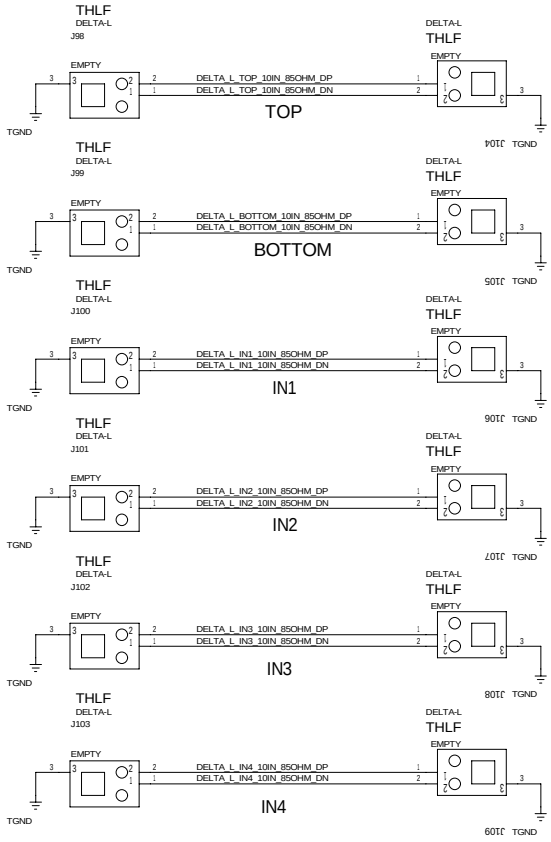
Quanta	DEPARTMENT CCBU	DESIGNER	PROJCET <Q_PROJ>	DOCUMENT NUMBER <Q_NUMBER>	REV <Q_REV>
		REVIEWER	SIZE C	DATE Fri Dec 15 19:37:18 2017	SHEET 225 OF 226

DELTA-L: CONTROL PCB LOSS

85 OHM, 5INCH



85 OHM, 10INCH