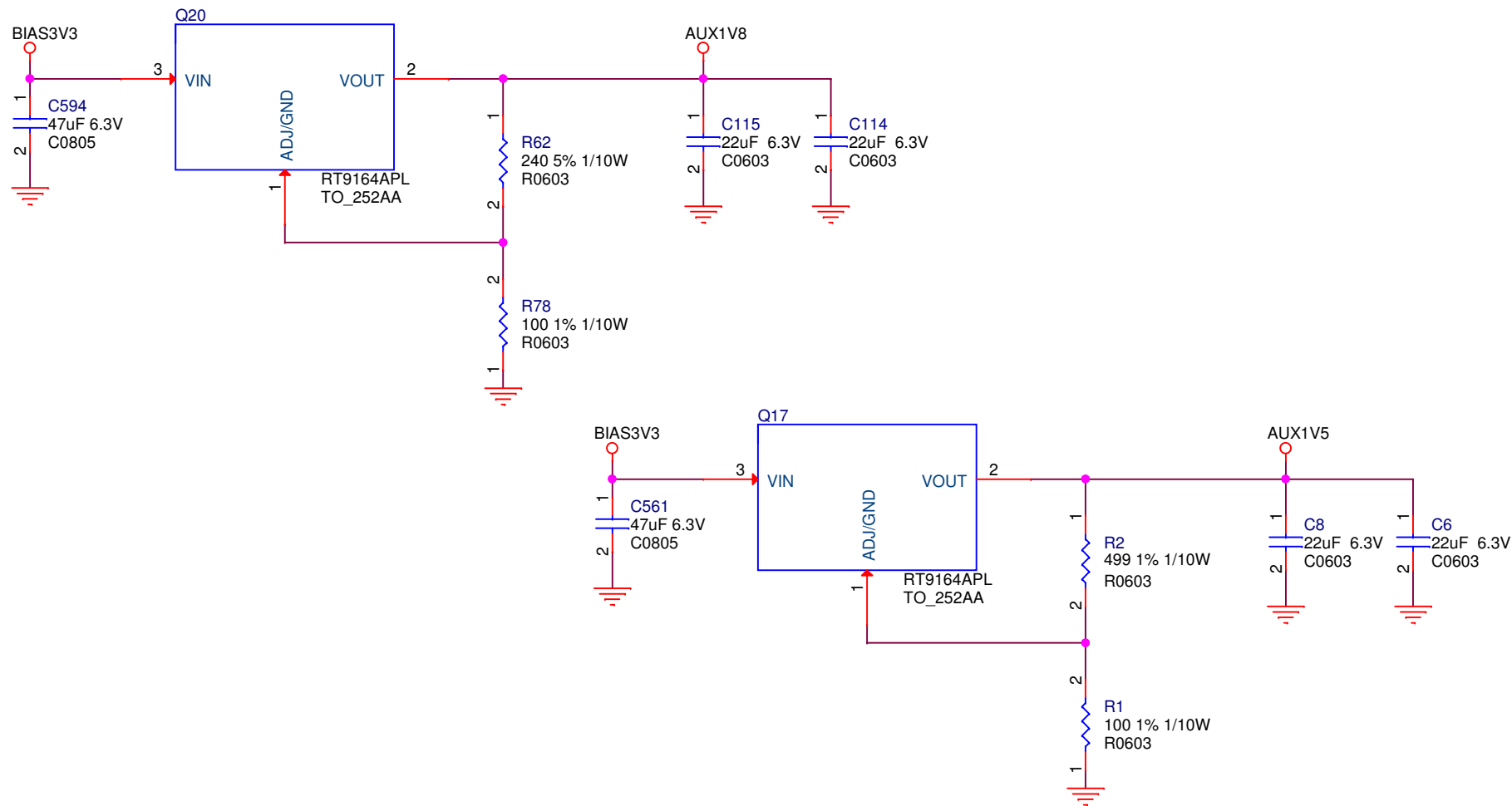
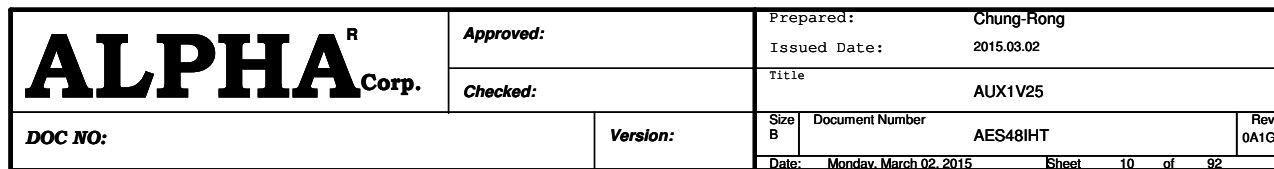


<b>ALPHA<sup>R</sup> Corp.</b>		Prepared: Chung-Rong	
		Issued Date: 2015.03.02	
DOC NO:		Title: BIAS3V3	
Version:		Size B	Document Number: AES48IHT
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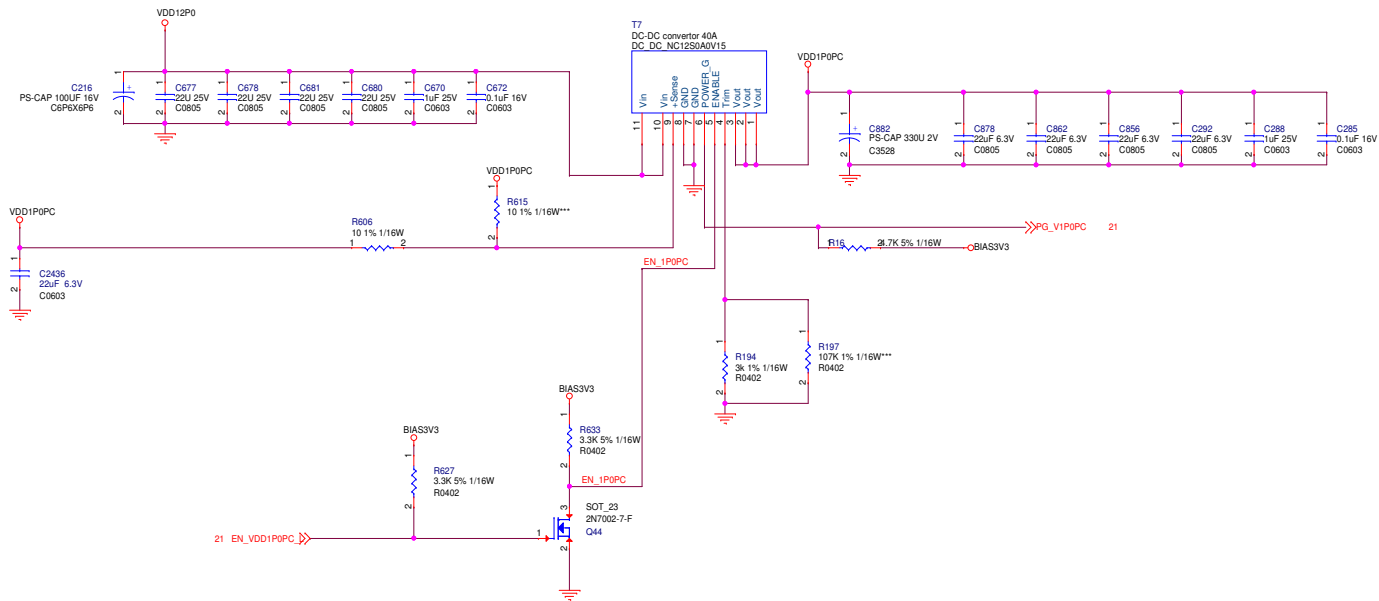
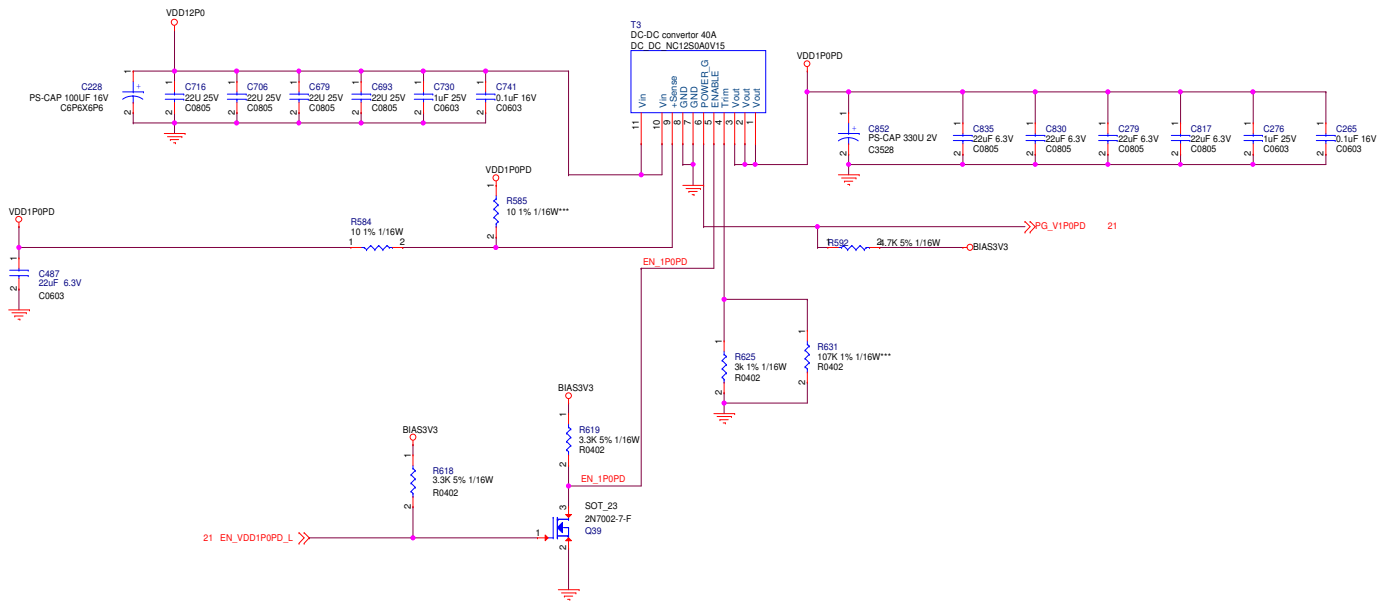
<b>ALPHA<sup>R</sup> Corp.</b>	<b>Approved:</b>		Prepared: Chung-Rong	
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				Rev: 0A1G
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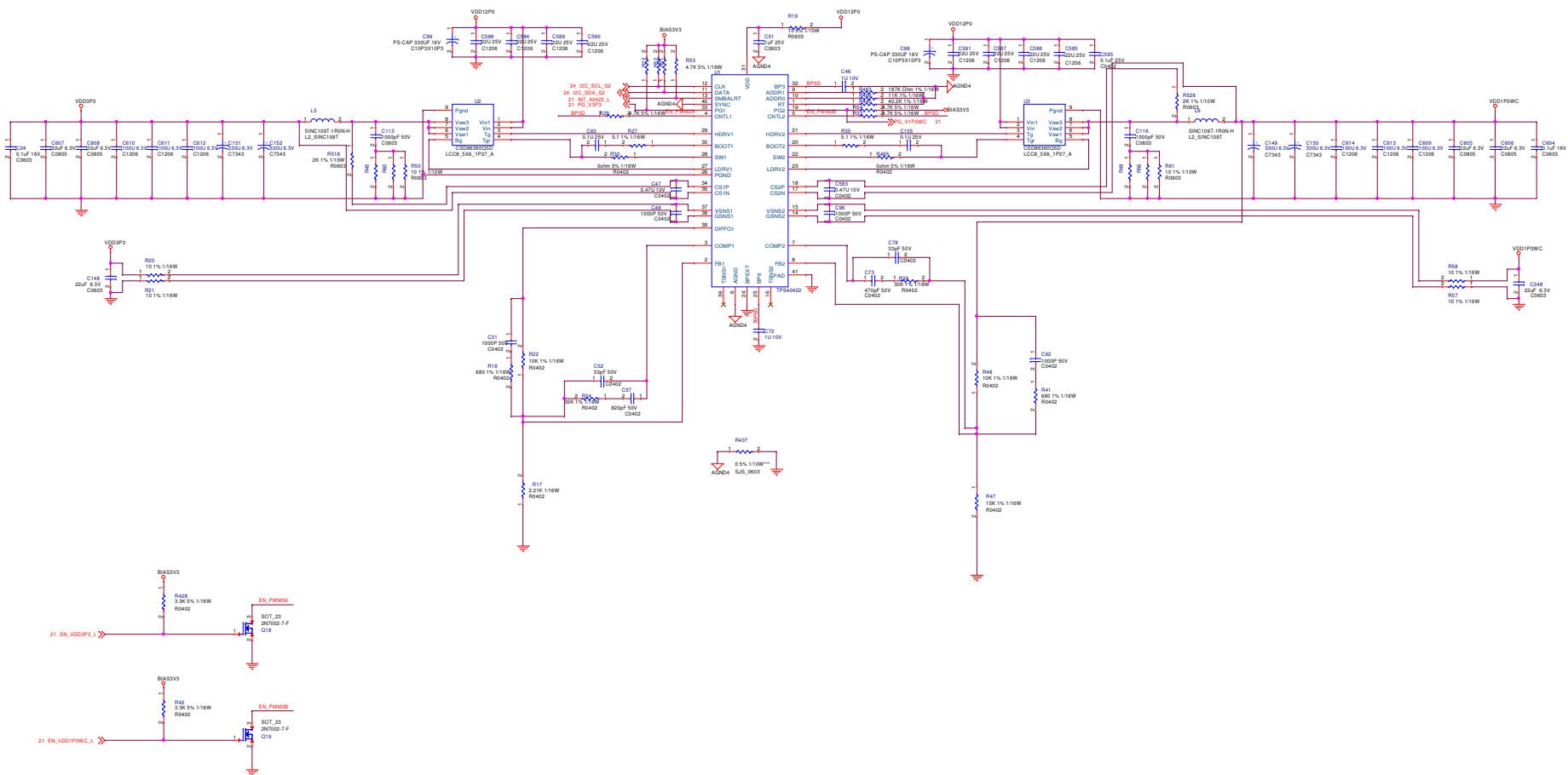


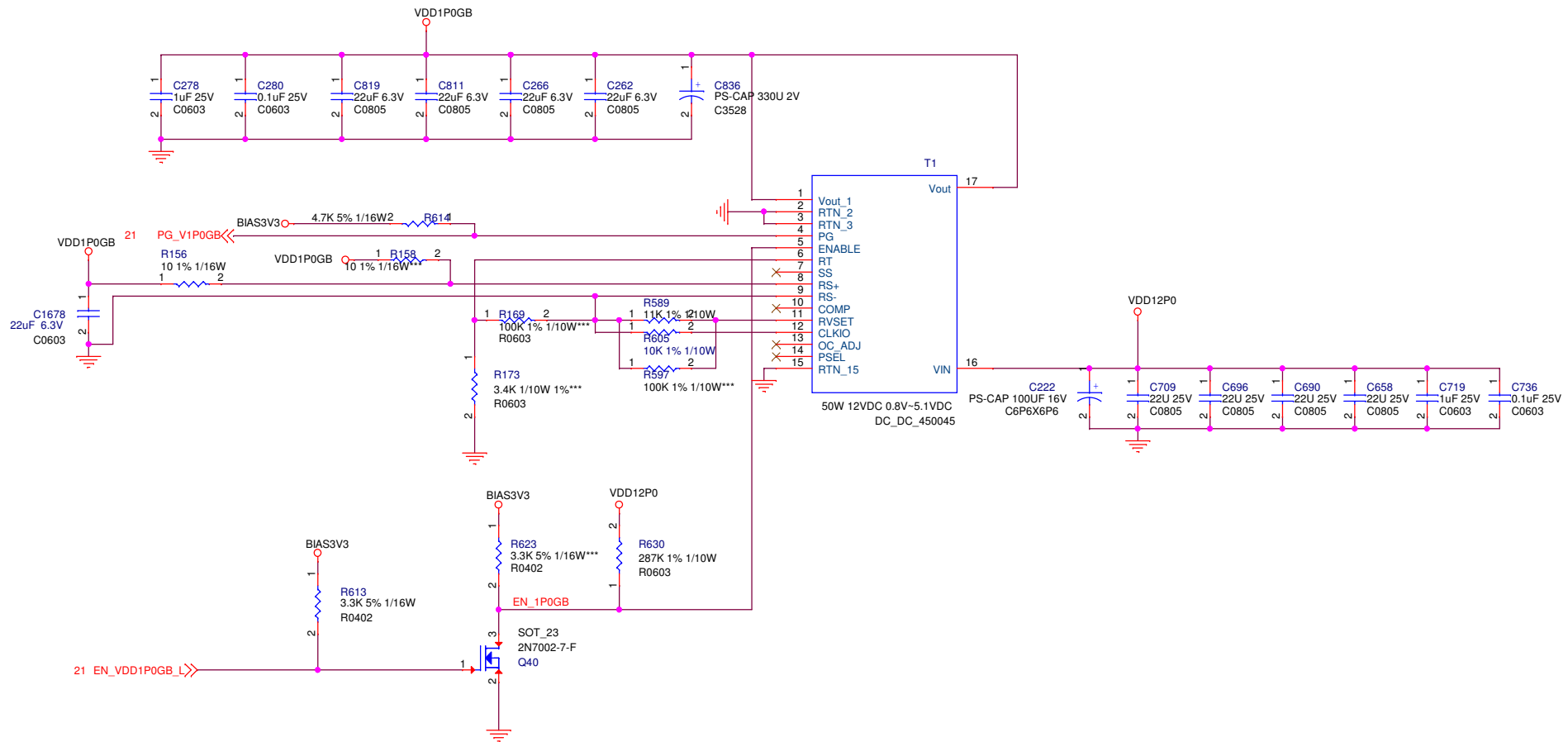




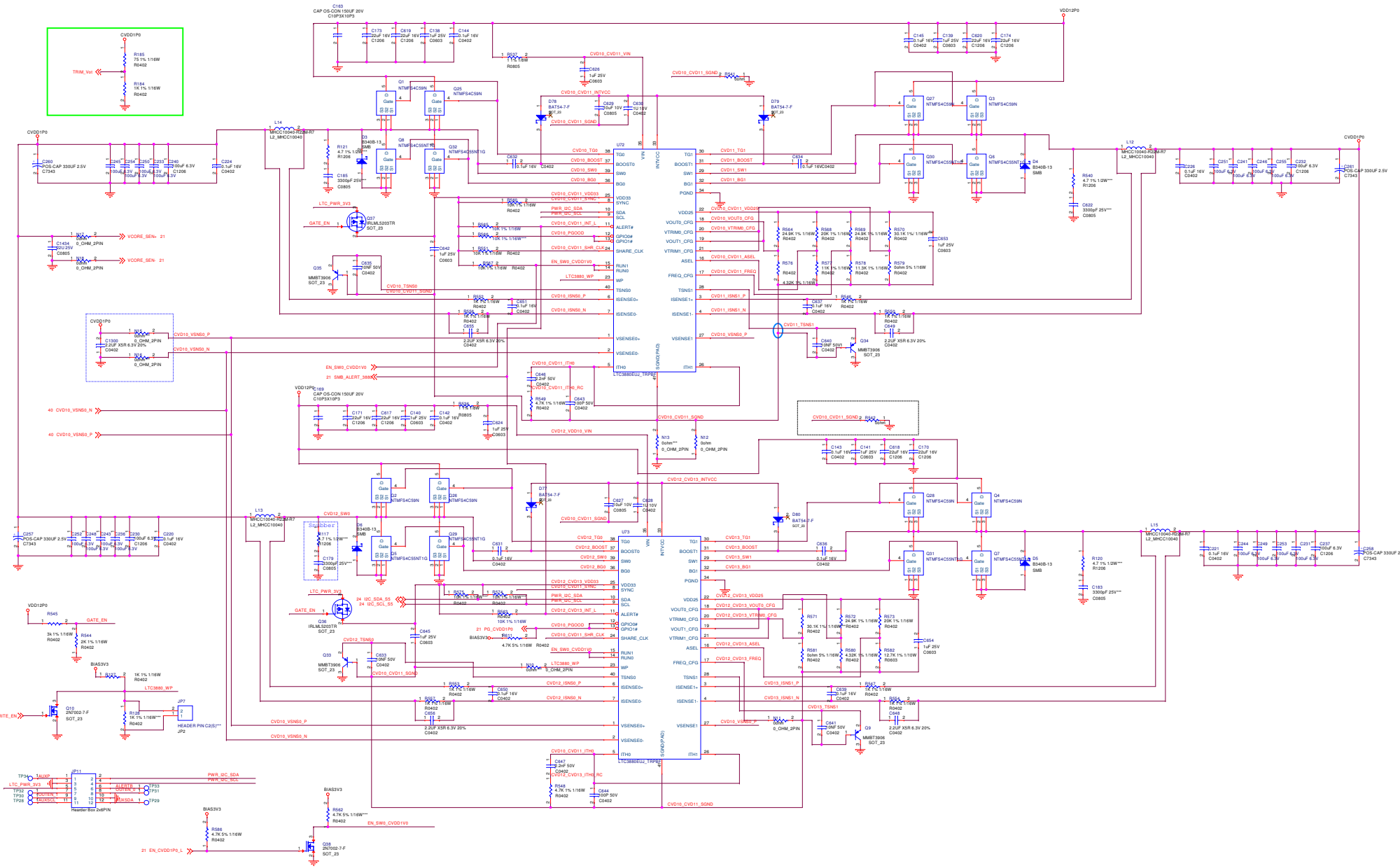


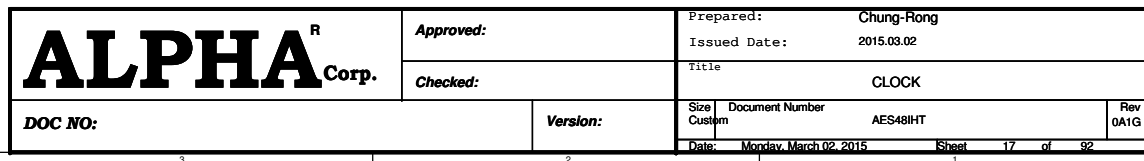
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Version:		Size C	Document Number	AES48IHT	Rev 0A1G
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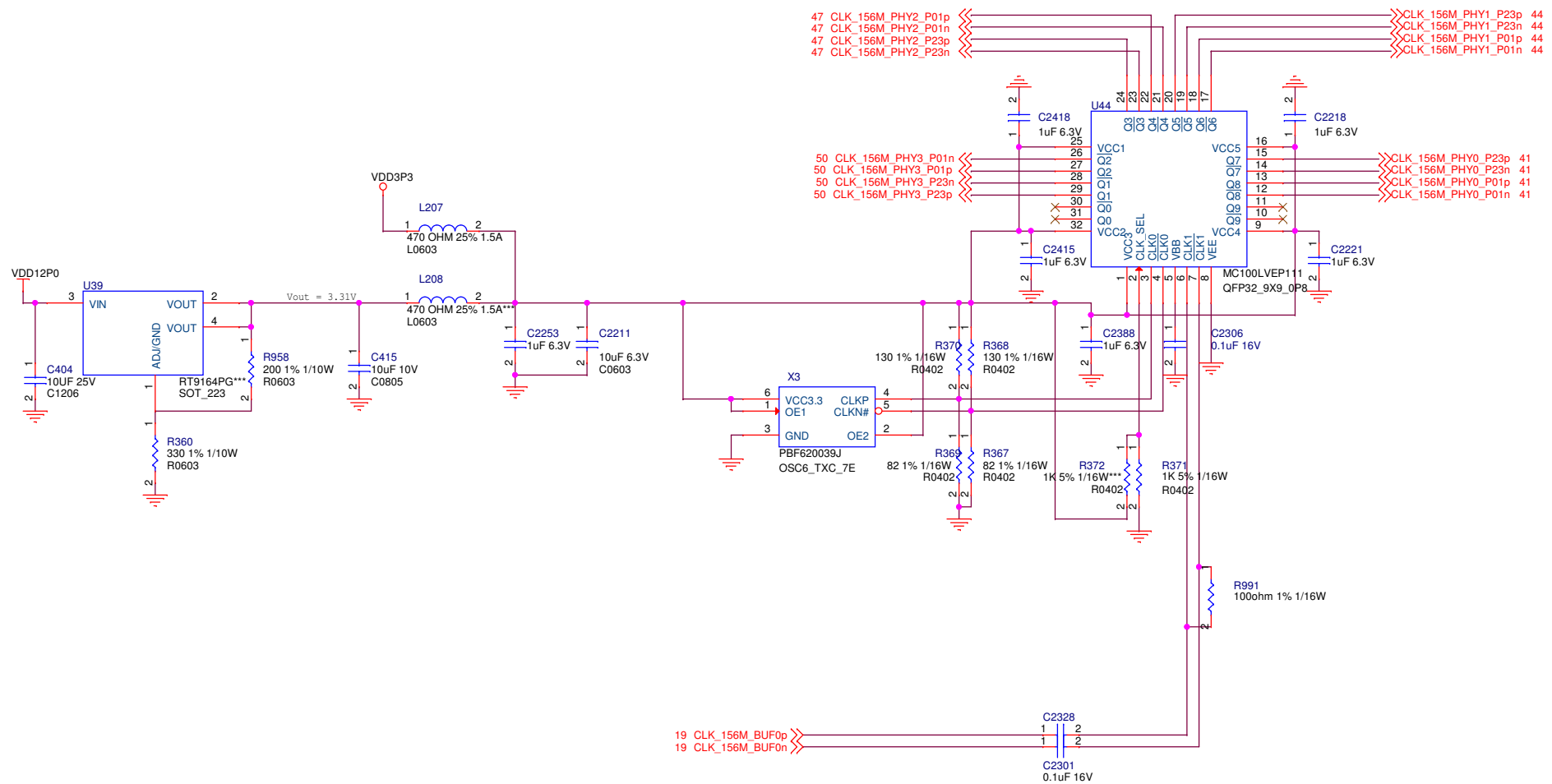




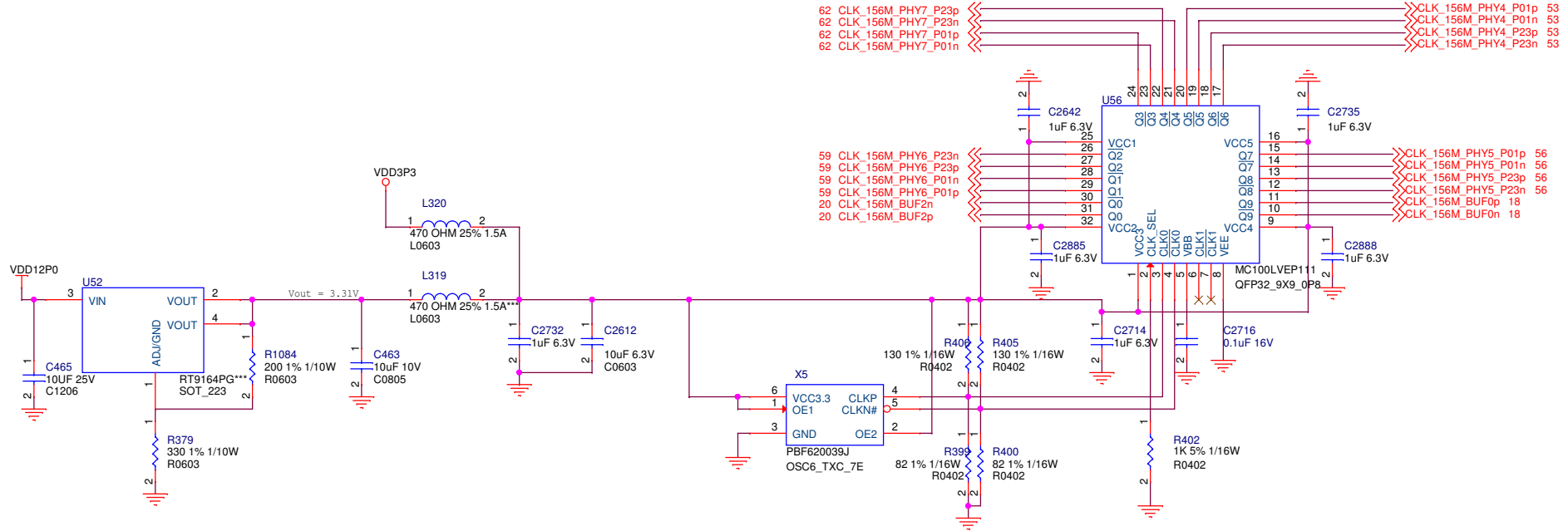
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				Size B	Document Number: AES48IHT
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	<b>Checked:</b>		Issued Date: 2015.03.02		
			Title GB CLK 1		
<b>DOC NO:</b>		<b>Version:</b>	Size B	Document Number AES48IHT	Rev 0A1G
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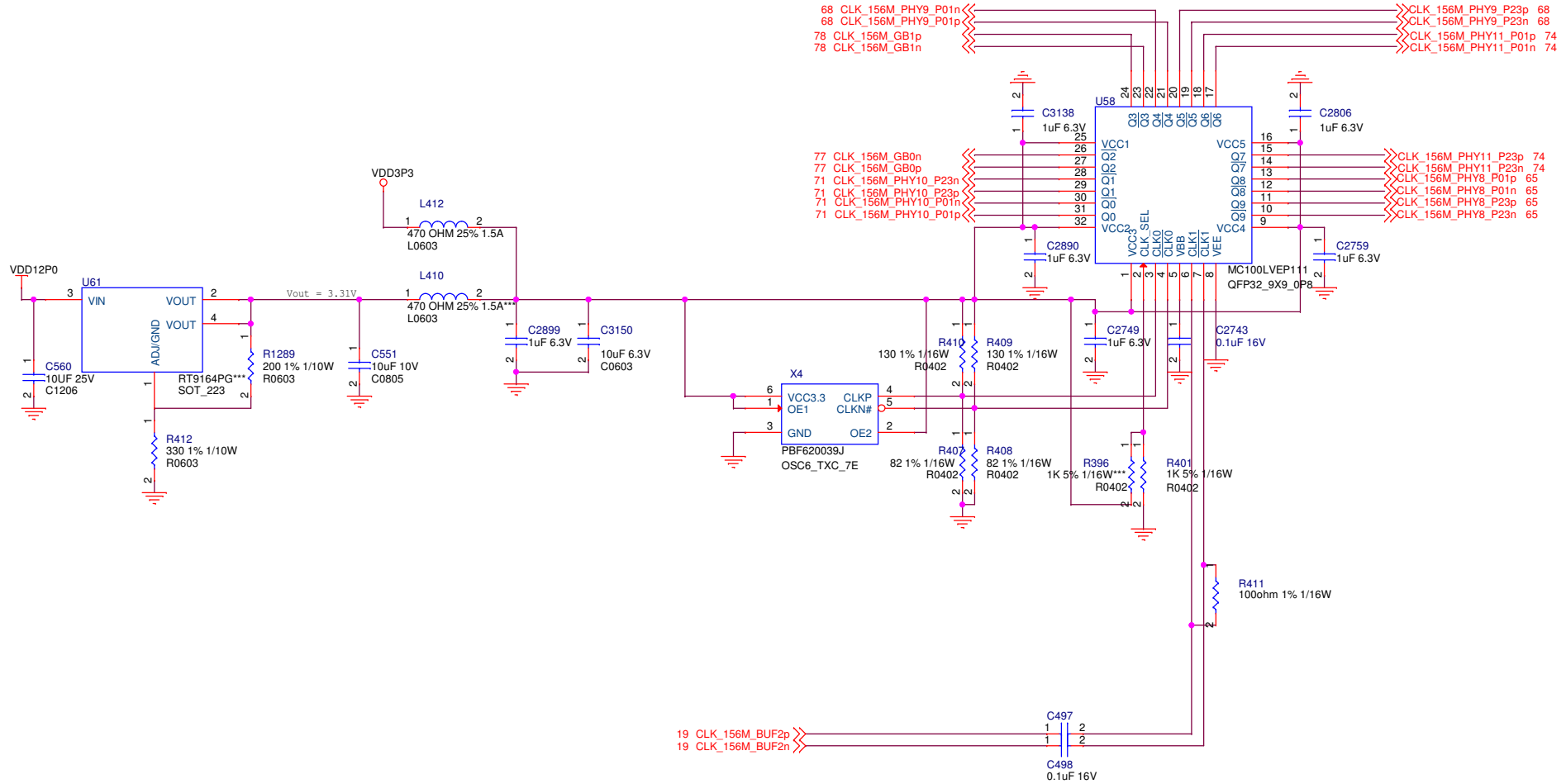
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Size: Document Number: AES48IHT

Date: Monday, March 02, 2015

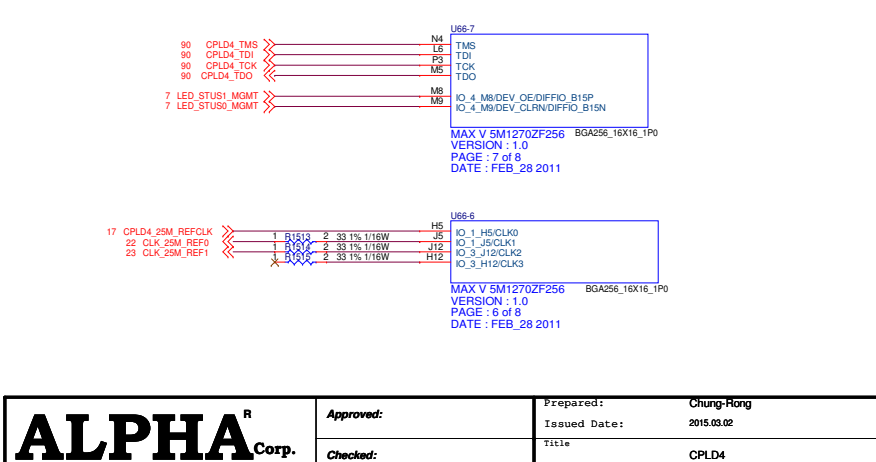
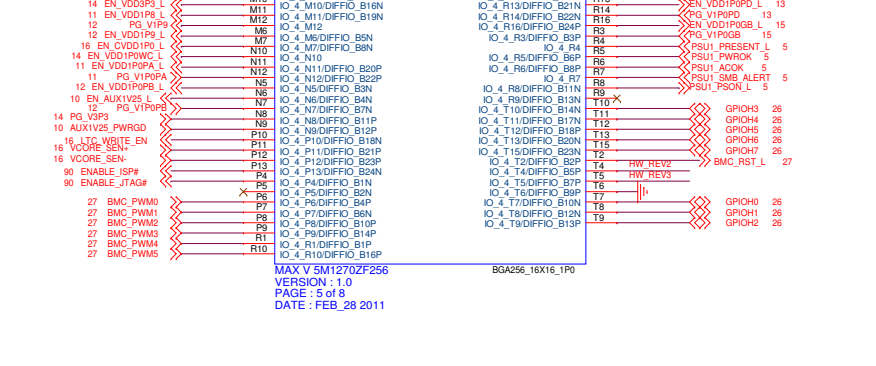
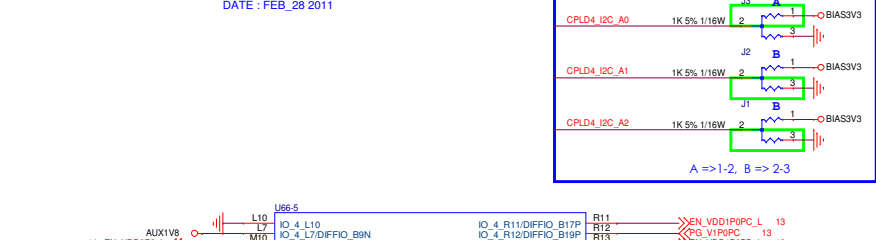
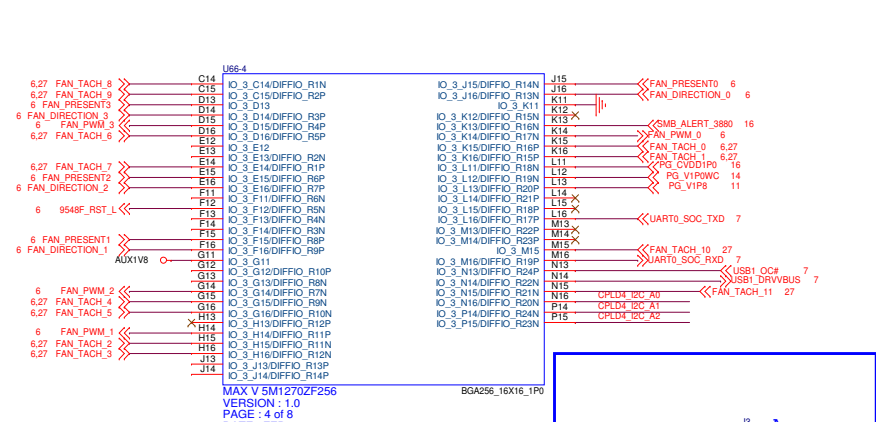
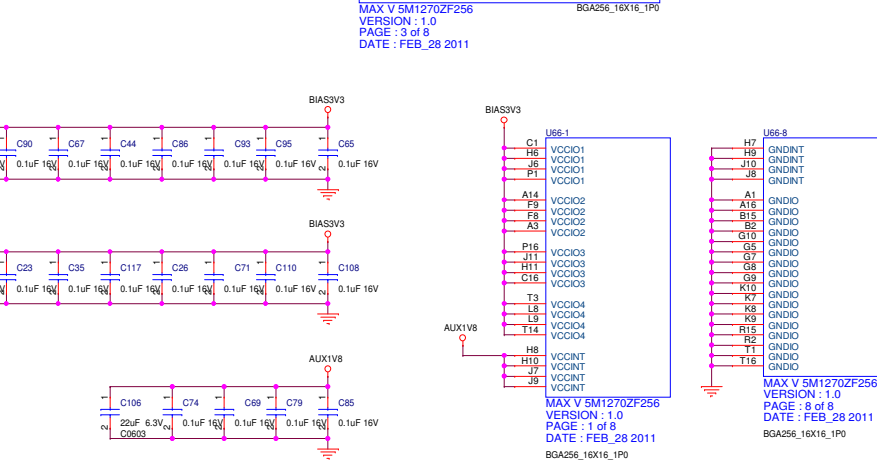
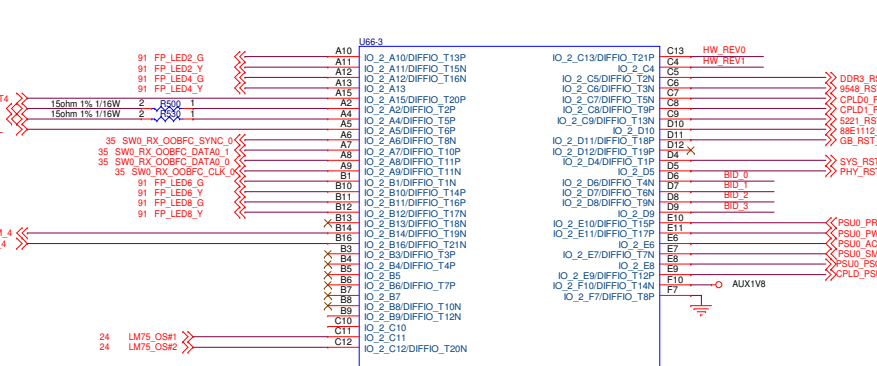
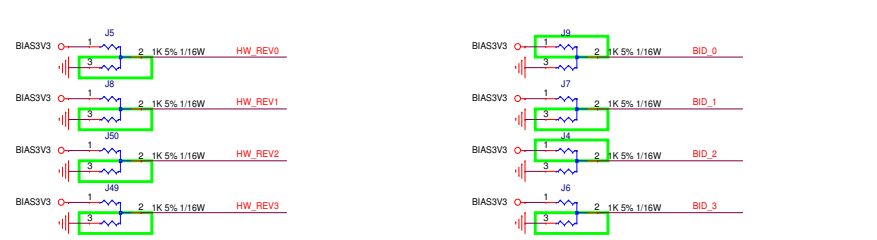
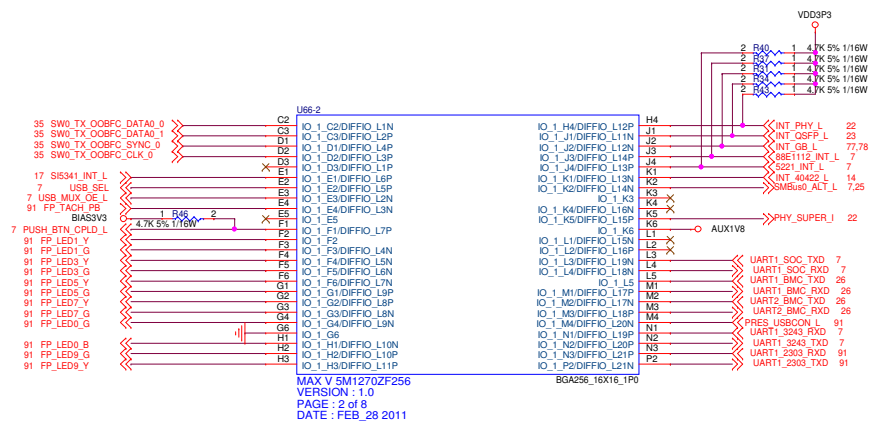
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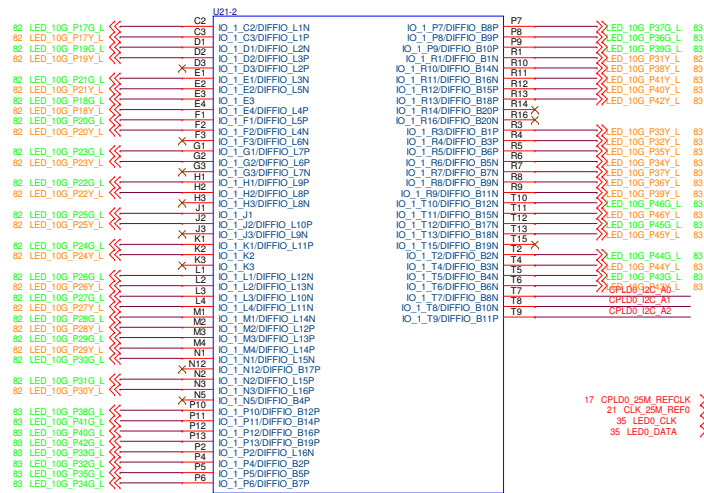
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		Issued Date: 2015.03.02	
<b>DOC NO:</b>		Title: GB CLK 3	
<b>Version:</b>		Size: B	Document Number: AES48IHT
		Date: Monday, March 02, 2015	Rev: 0A1G
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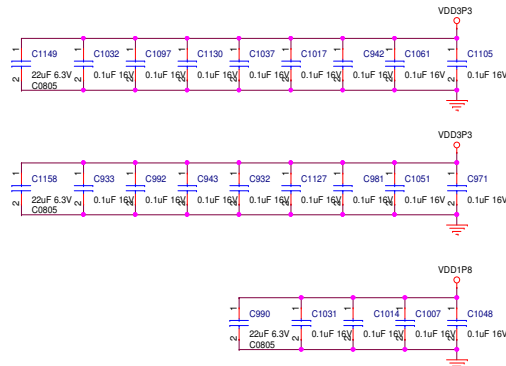
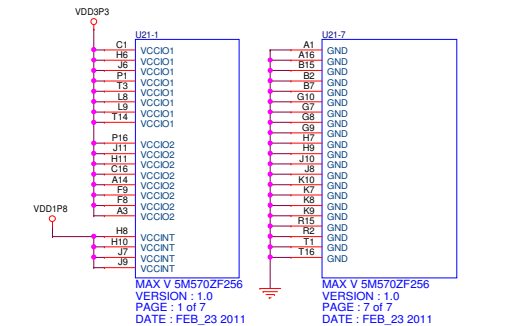
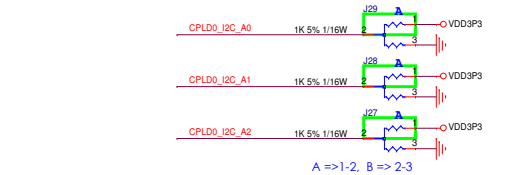
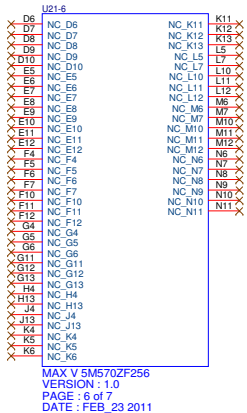
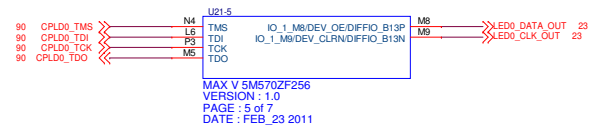
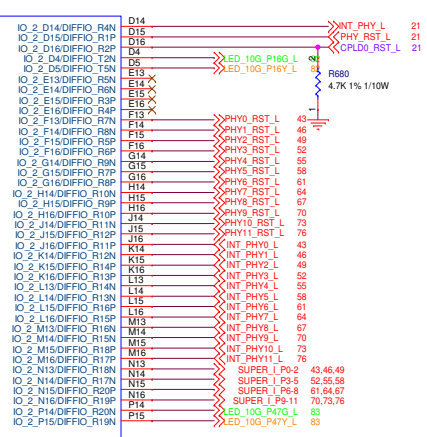
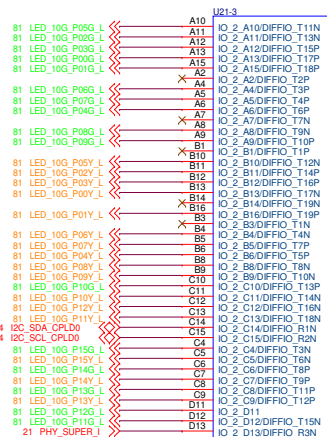




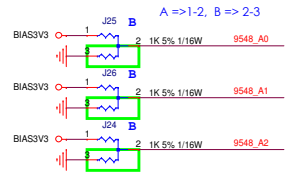


17 CPLD0\_25M\_REFCLK  
21 CLK\_25M\_REF0  
35 LED0\_CLK  
35 LED0\_DATA

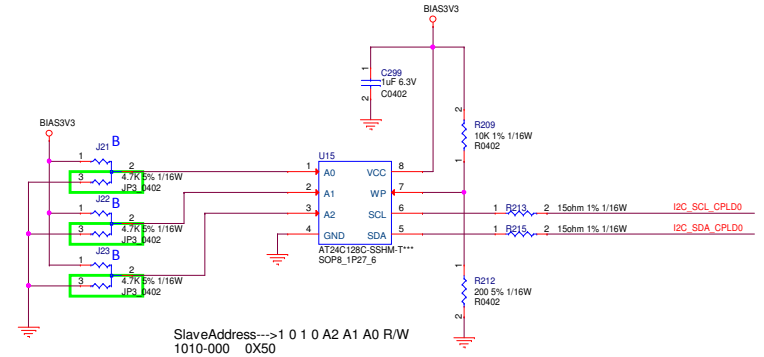
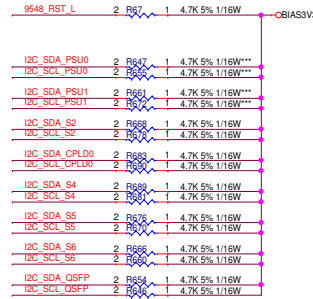
U21-4  
IO\_1\_H5/CLK0  
IO\_1\_J5/CLK1  
IO\_2\_J12/CLK2  
IO\_2\_H12/CLK3  
MAX V 5M570ZF256  
VERSION : 1.0  
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DATE : FEB\_23 2011



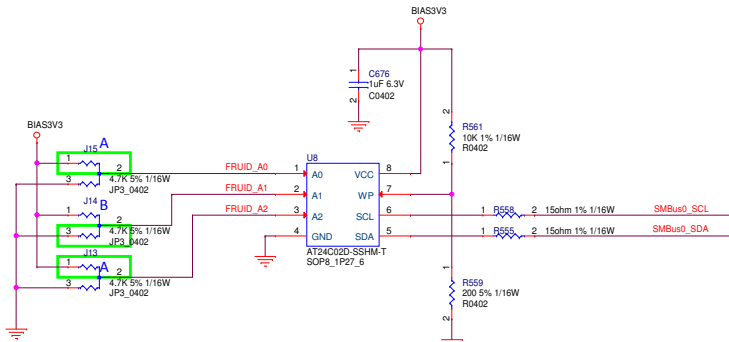




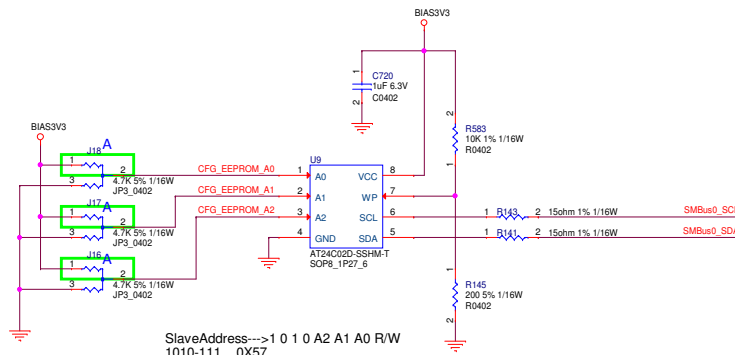
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1110-000 0X70



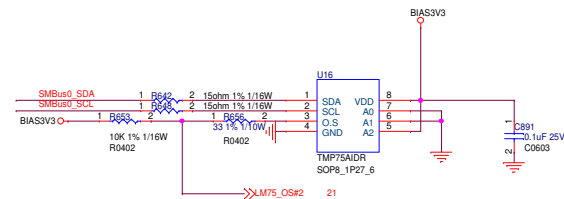
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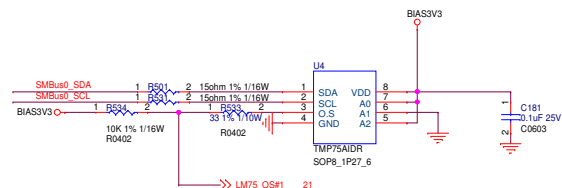
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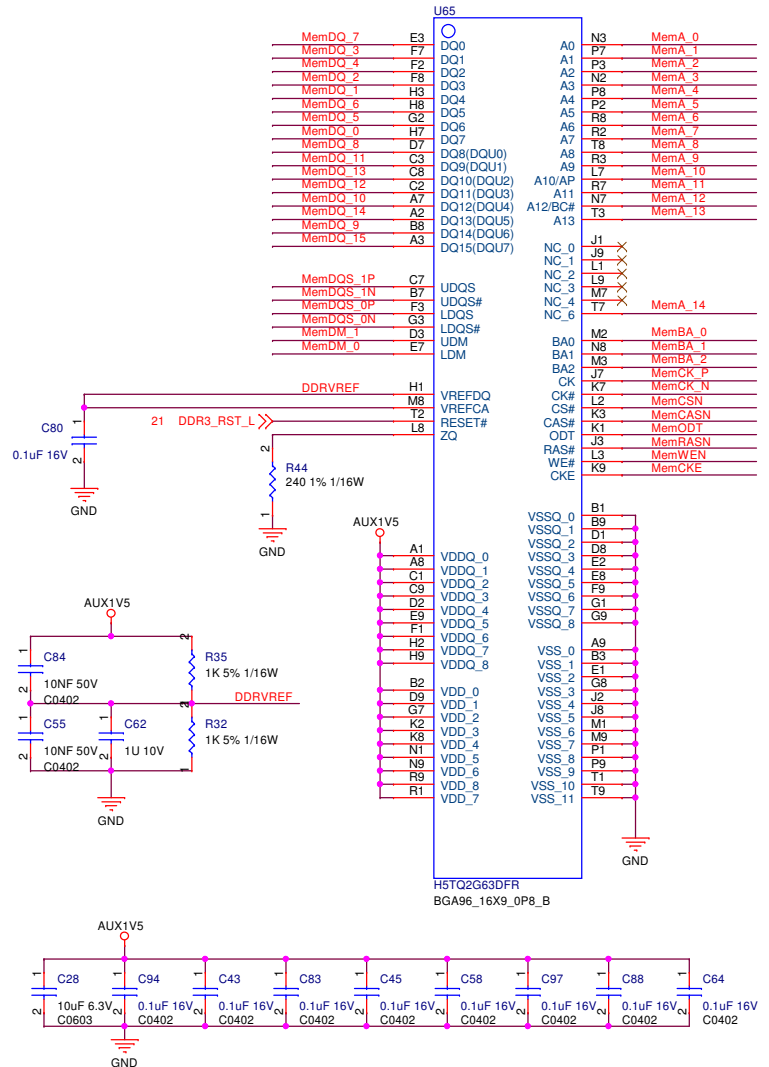
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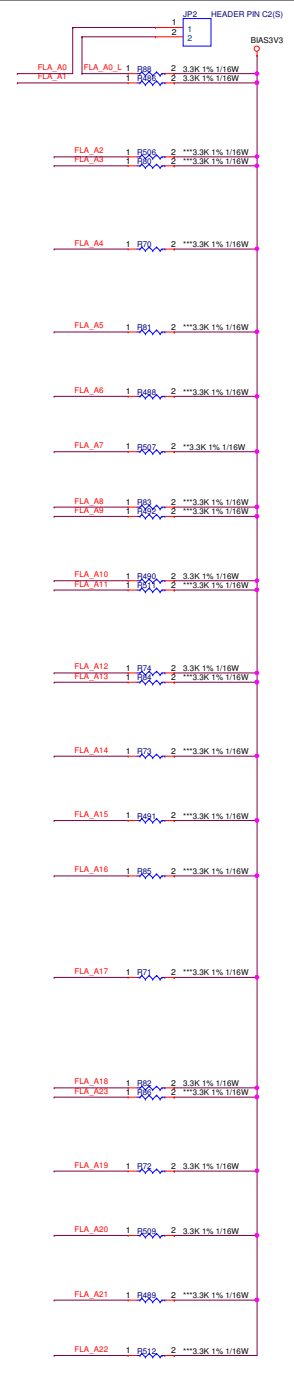
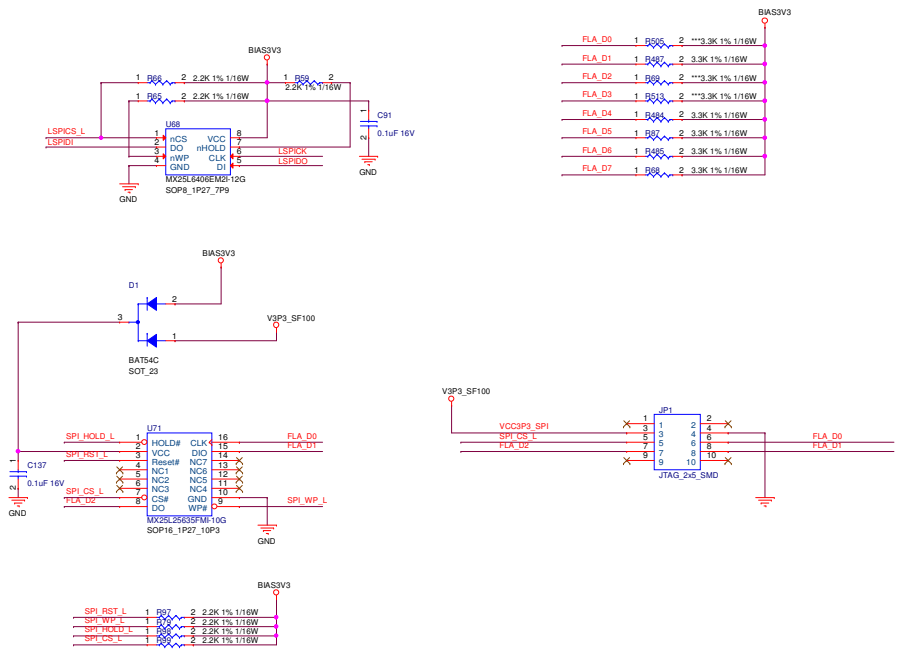


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1001-100 0X4C



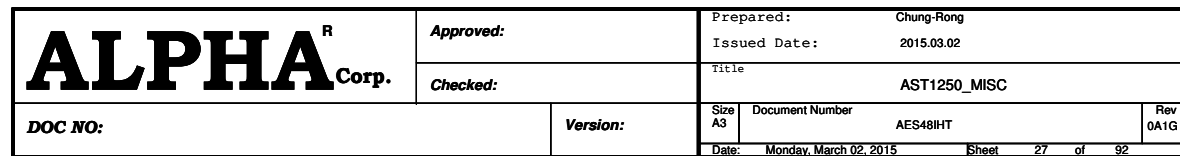
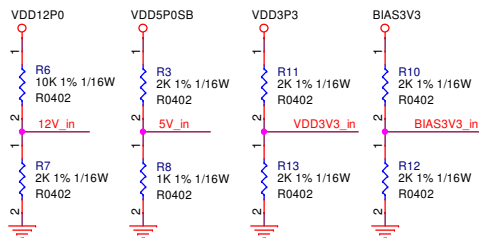
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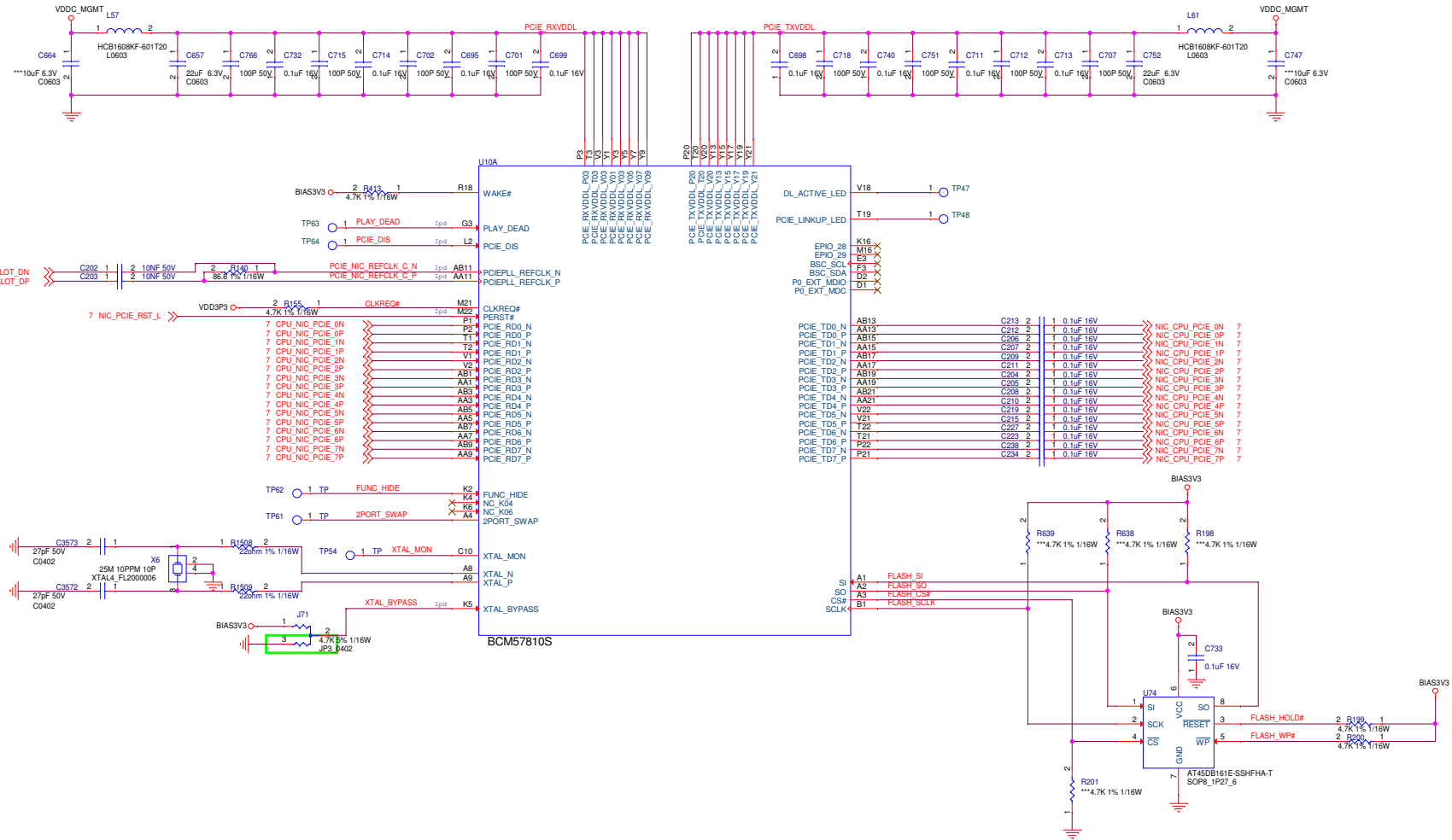
ROMA[0] : ARM CPU boot code selection 00 : Boot from NOR flash memory 01 : Boot from NAND flash memory 10 : Boot from SPI flash memory (Select) 11 : Disable ARM CPU operation	10
ROMA[32] : VGA memory size selection 00 : Select 8 MB VGA memory 01 : Select 16 MB VGA memory 10 : Select 32 MB VGA memory 11 : Select 64 MB VGA memory	AST1250 : 00
ROMA[4] : Boot flash memory extended option NOR type flash: data bus width selection 0 : Select 8 bits interface 1 : Select 16 bits interface SPI type flash: boot address mode selection 0 : Boot with 24 bits address mode (Select) 1 : Boot with 32 bits address mode	0
ROMA[5] : Enable VGA BIOS ROM 0 : No VGA BIOS ROM (for on-board application) 1 : Enable VGA BIOS ROM (for add-on application)	AST1250 : 0
ROMA[6] : Define MAC#1 interface 0 : RMII/NCSS (Select) 1 : RMII	0
ROMA[7] : Define MAC#2 interface 0 : RMII/NCSS (Select) 1 : RMII	0
ROMA[9:8] : R-PLL default clock frequency selection 00: Select 384 Mhz 01: Select 360 Mhz 10: Select 336 Mhz 11: Select 204 Mhz	AST1250 : 00
ROMA[11:10] : CPU/AHB clock frequency ratio selection 00 : Select CPU:AHB = 1:1 01 : Select CPU:AHB = 2:1 10 : Select CPU:AHB = 4:1 11 : Select CPU:AHB = 3:1	AST1250 : 01
ROMA[13:12] : SPI mode selection 00 : Disable SPI interface 01 : Enable SPI Master (Select) 10 : Enable SPI Master and SPI Slave to AHB Bridge 11 : Enable SPI Bypass	01
ROMA[14] : Enable LPC dedicated reset pin function 0 : LPC reset is shared with PCI reset pin (Select) 1 : LPC reset is shared with GPIOB.	0
ROMA[15] : VGA Class Code selection 0 : Select the Class Code for video device 1 : Select the Class Code for VGA device	AST1250 : 0
ROMA[16] : SuperIO configuration address selection 0 : Decode 0x2E (Select) 1 : Decode 0x4E	0
ROMA[17] : Enable BMC 2nd boot watchdog timer 0 : Disable 1 : Enable BMC 2nd boot watchdog timer start counting at power up. (Select) The watchdog timer was located at WDT2. After watchdog timeout, it will reset BMC and restart booting from the 2nd boot flash at CS1#. CS1# must be the same flash type as CS0# and could be the same firmware as CS0#.	0
ROMA[23,18] : Clock source selection 00 : 24 Mhz CLKIN 01 : 48 Mhz CLKIN (Select) 10 : 25Mhz CLKIN, 24Mhz USBCKI 11 : 25Mhz CLKIN, 48Mhz USBCKI	01
ROMA[19] : Disable ACPI function 0 : Enable ACPI 1 : Disable ACPI (Select)	1
ROMA[20] : Disable LPC to decode SuperIO 0x2E/0x4E address 0 : Enable address decoding 1 : Disable address decoding (Select)	1
ROMA[21] : Enable GPIOD pass-through mode 0 : Disable (Select) 1 : Enable pass-through at power on	0
ROMA[22] : Enable GPIOE pass-through mode 0 : Disable (Select) 1 : Enable pass-through at power on	0

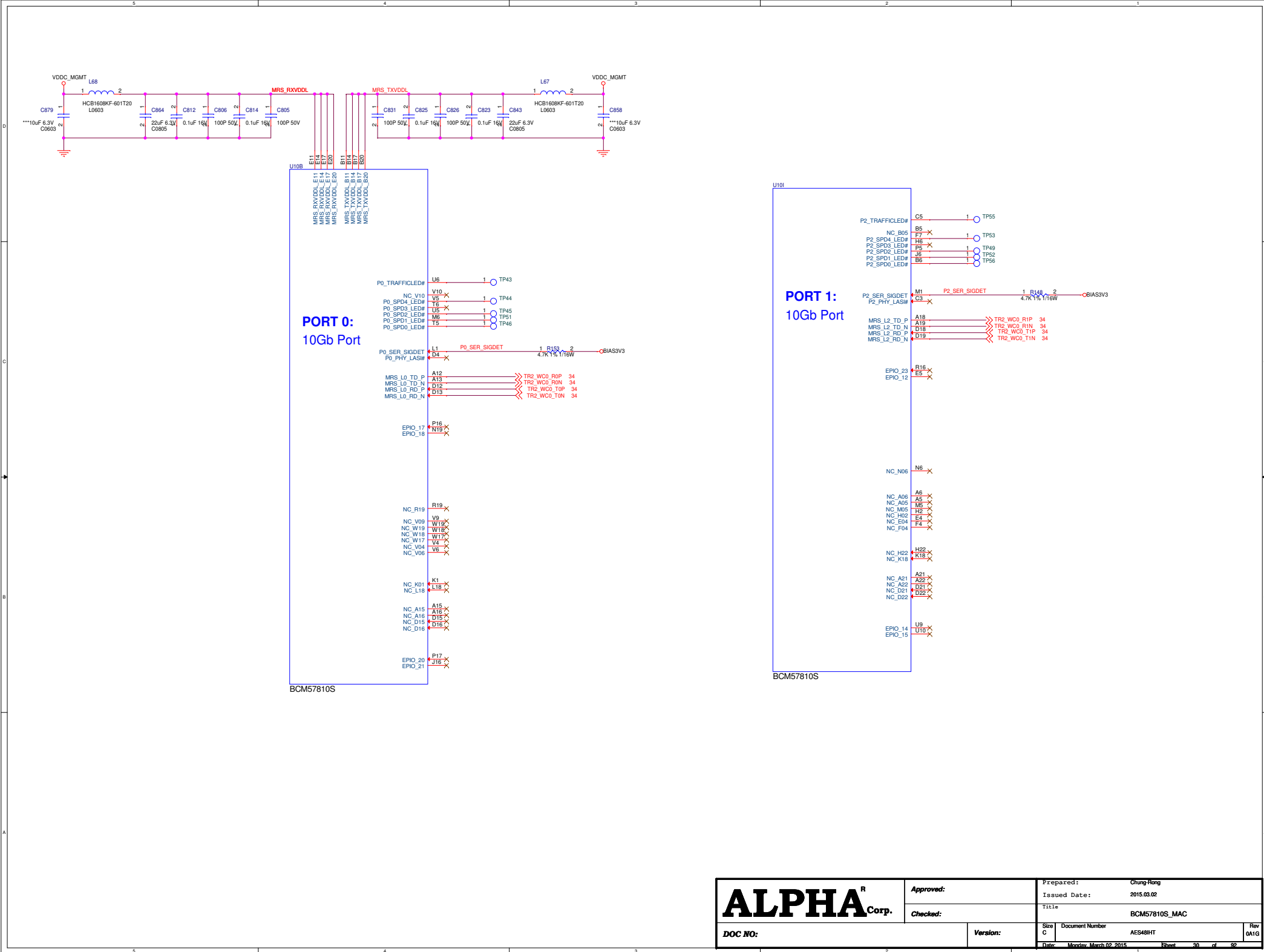


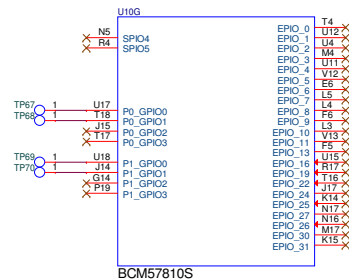
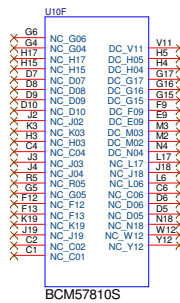
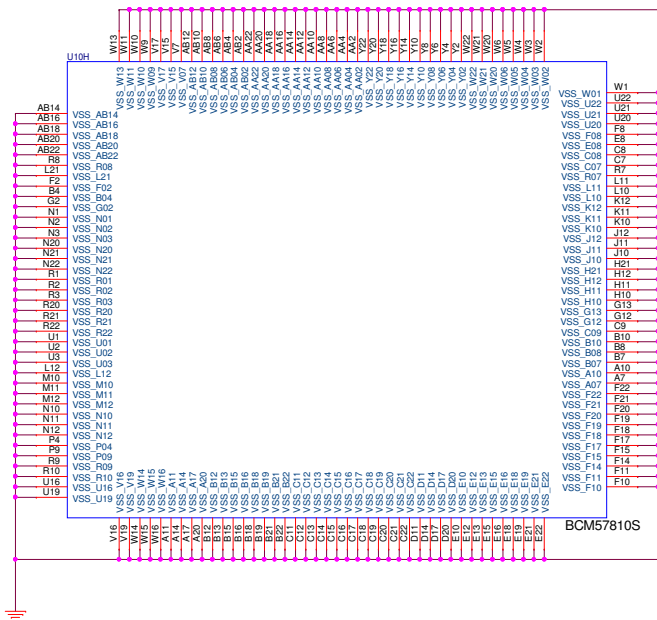
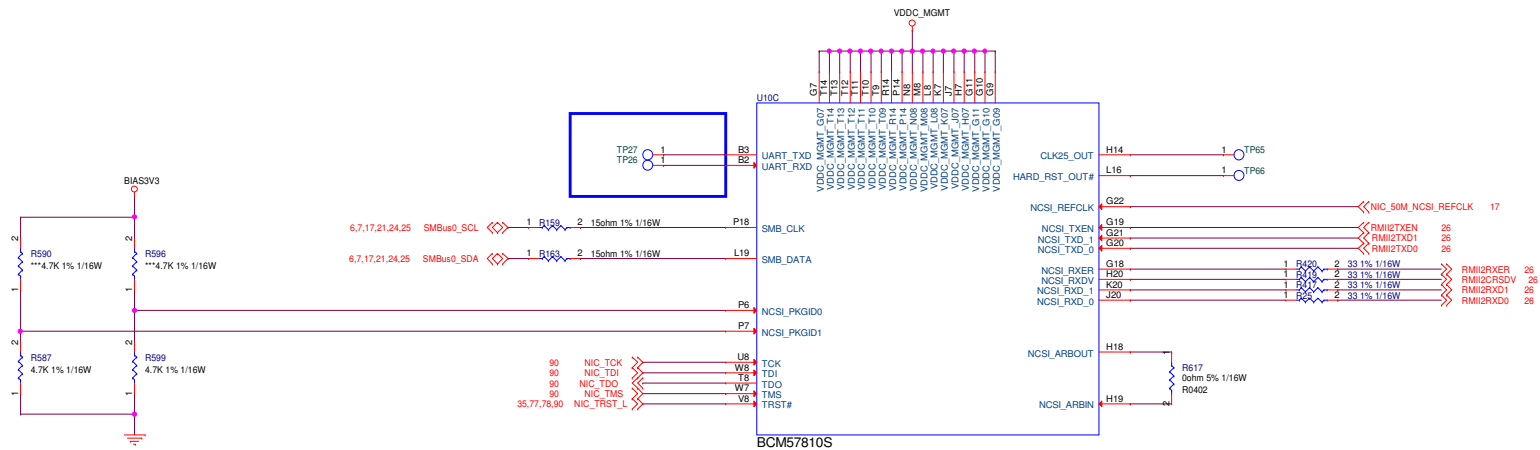




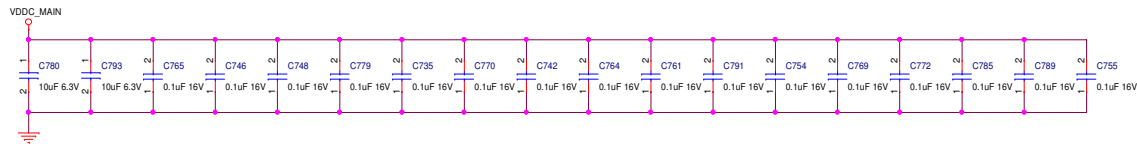
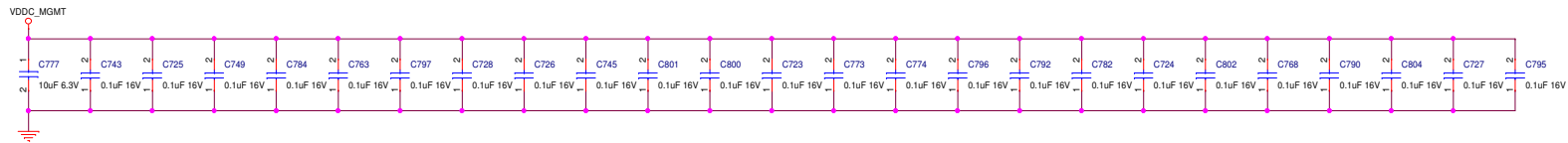
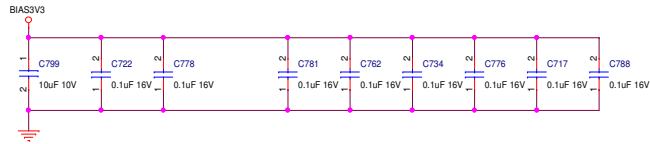
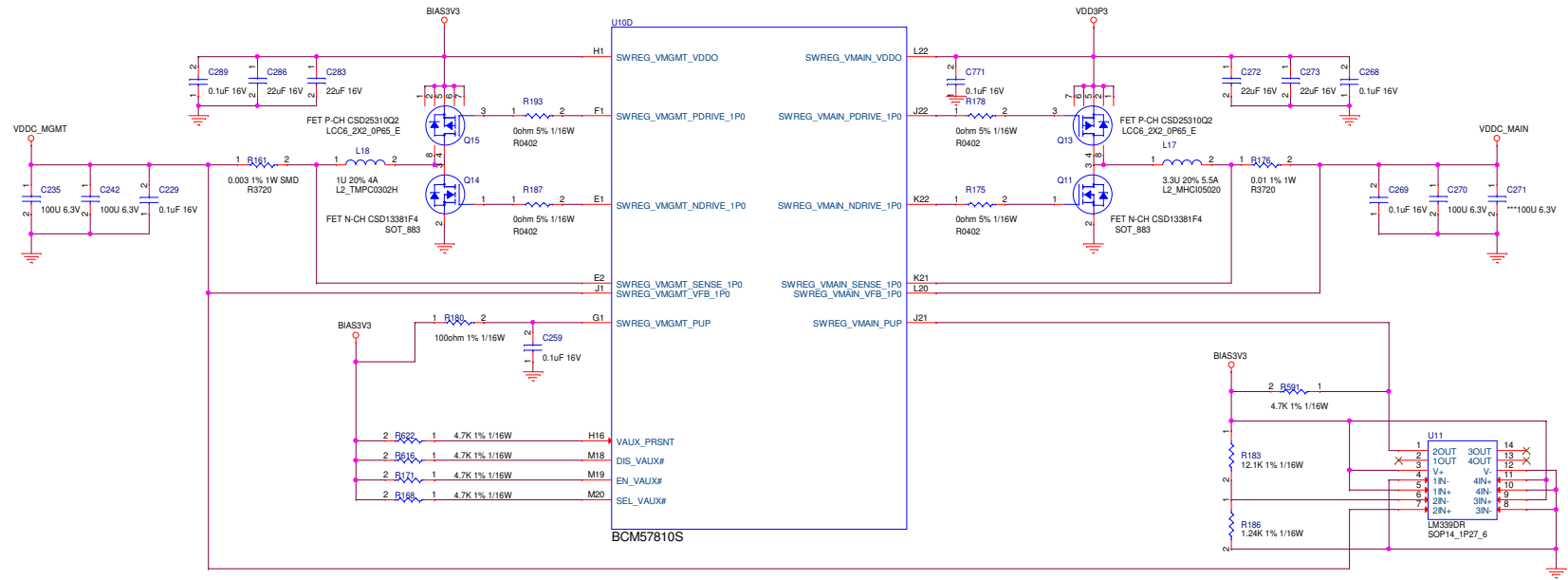


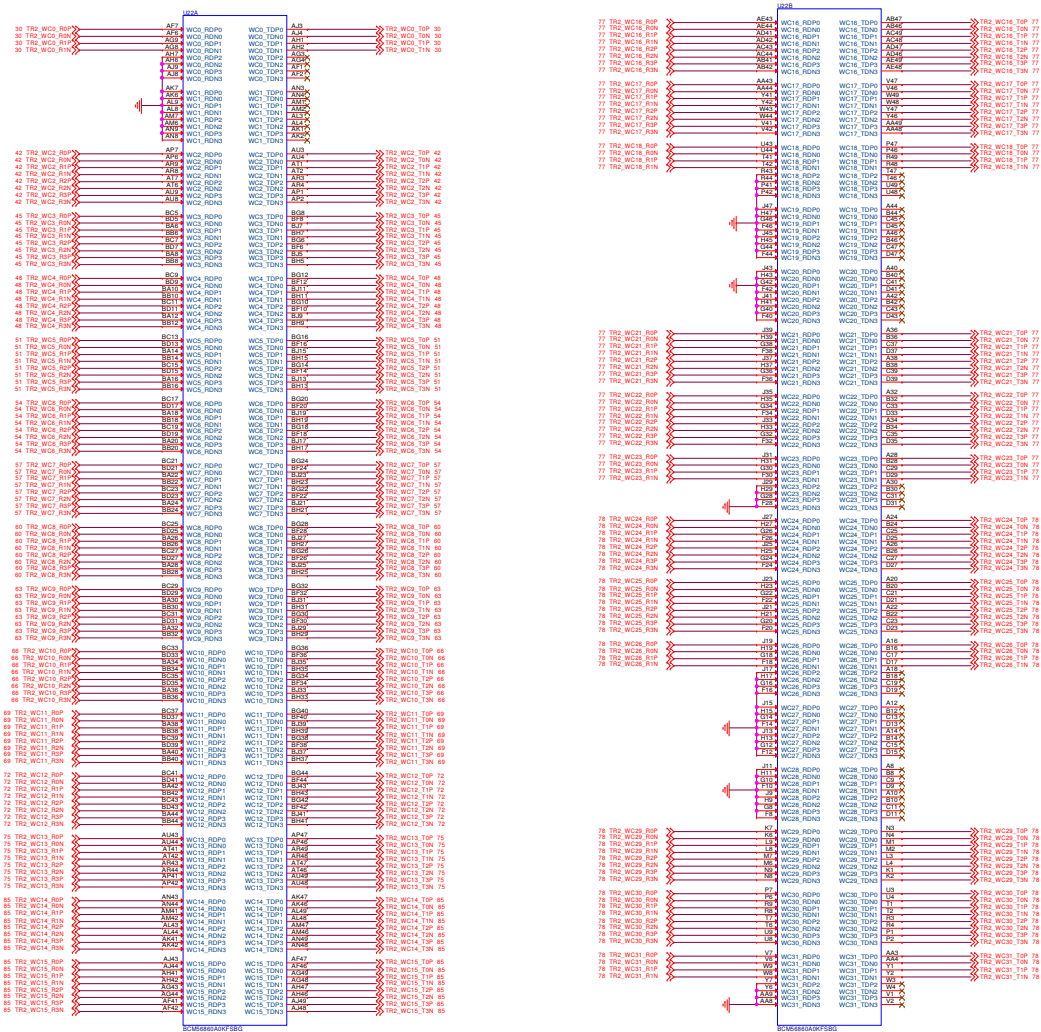




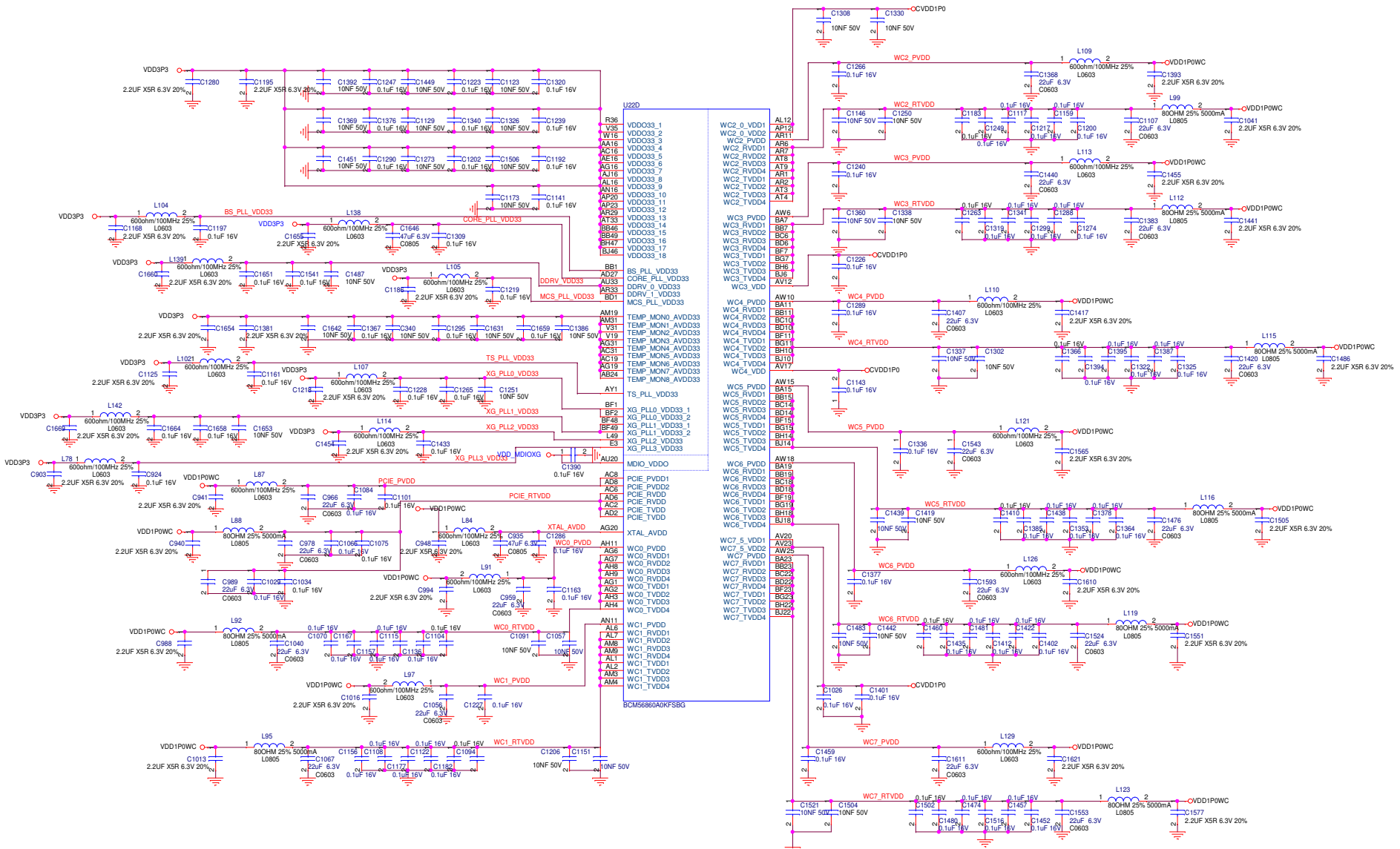






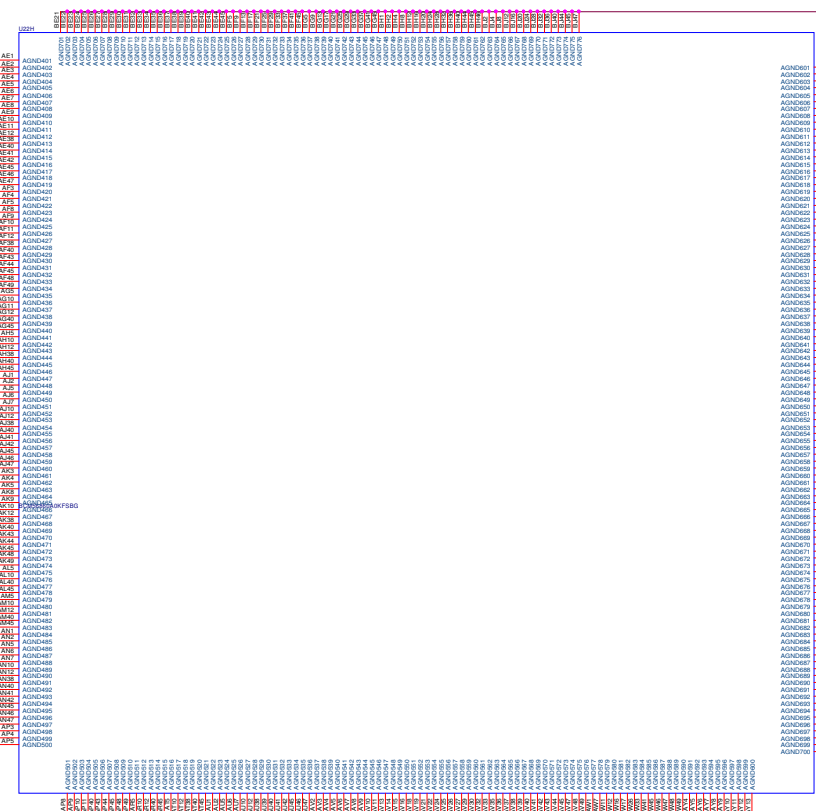
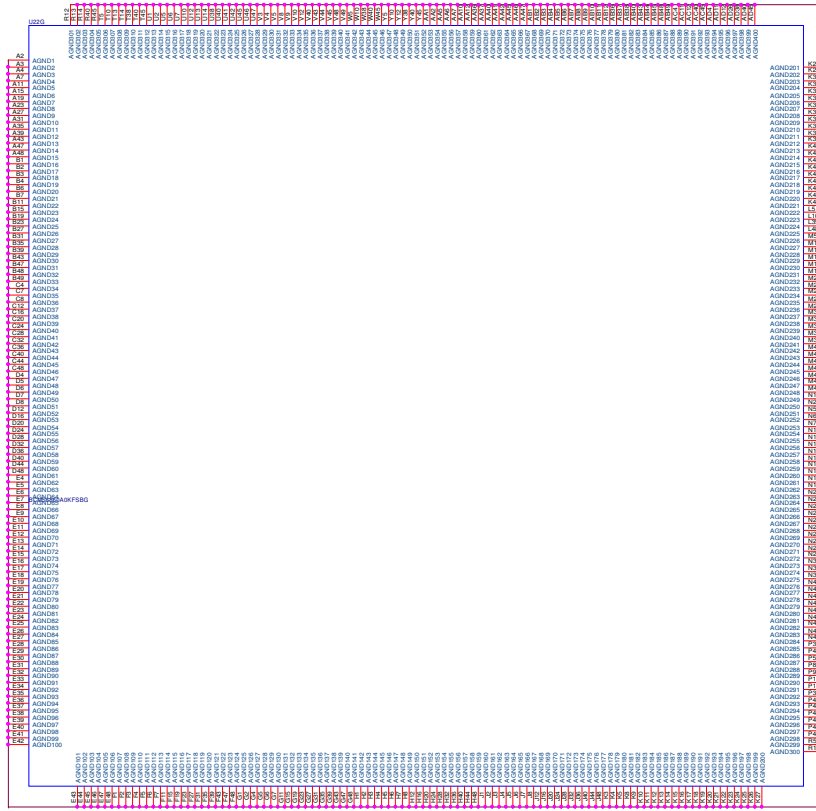






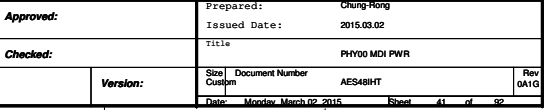


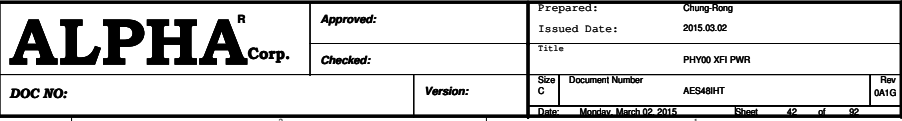


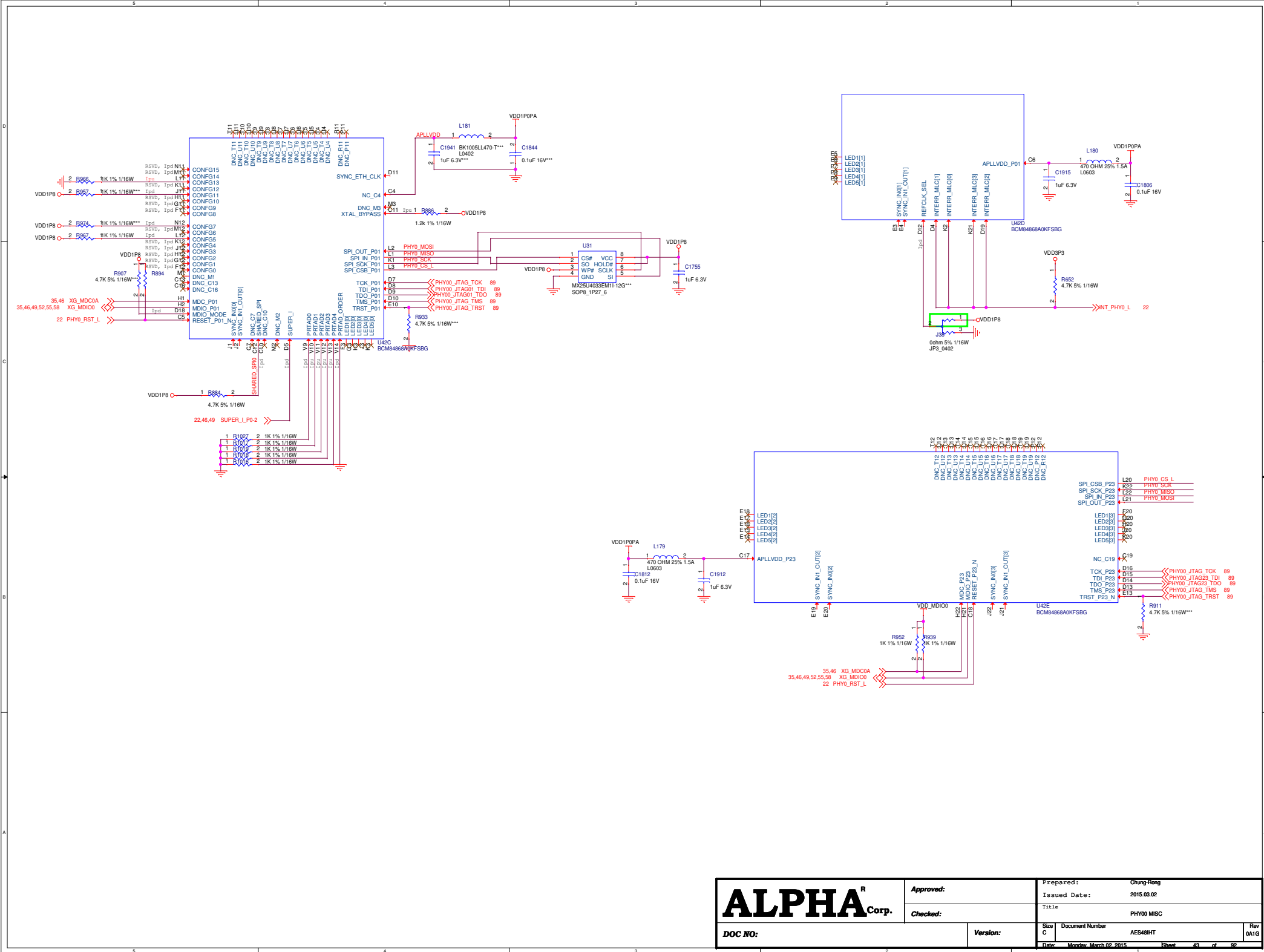


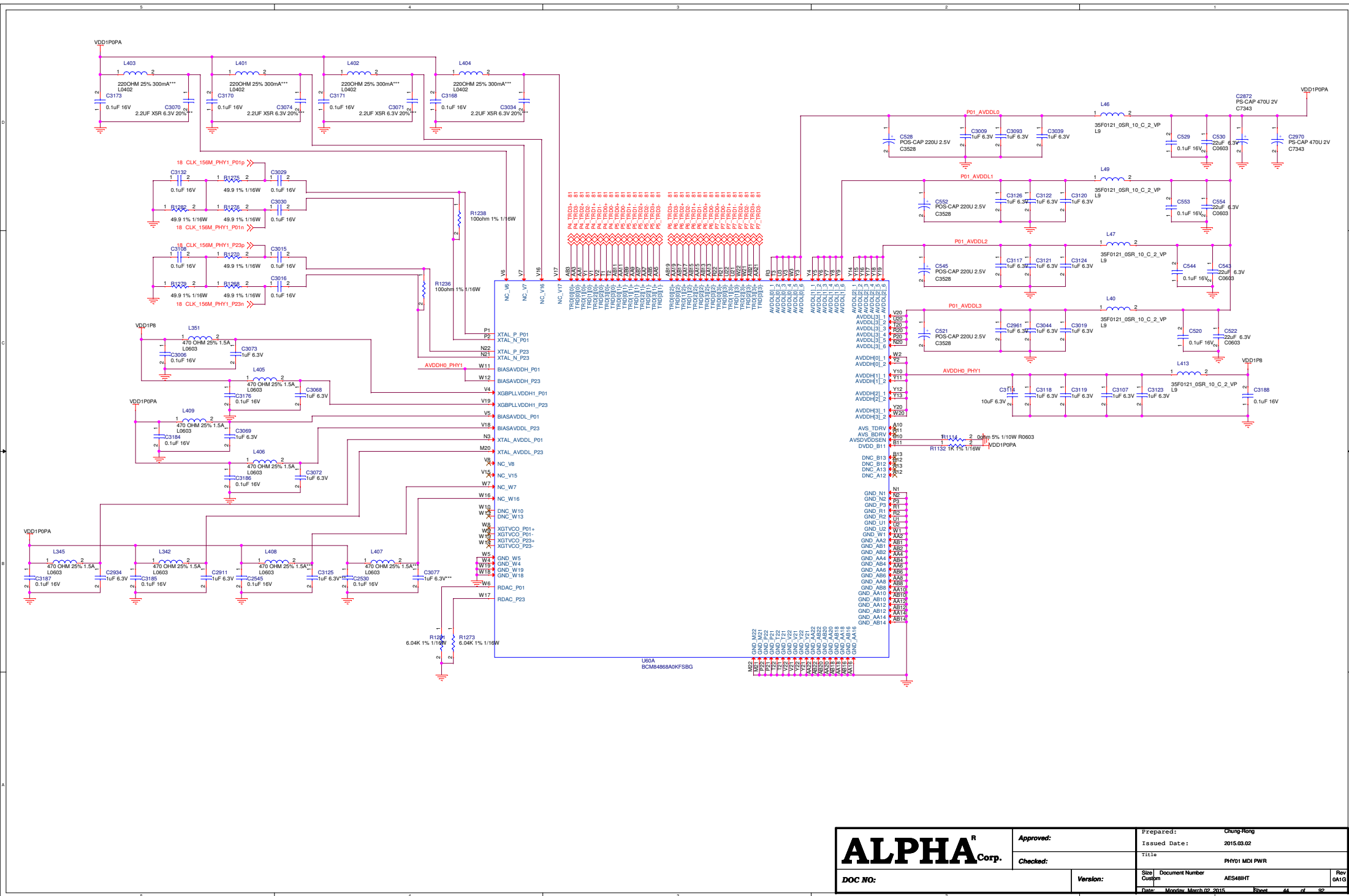












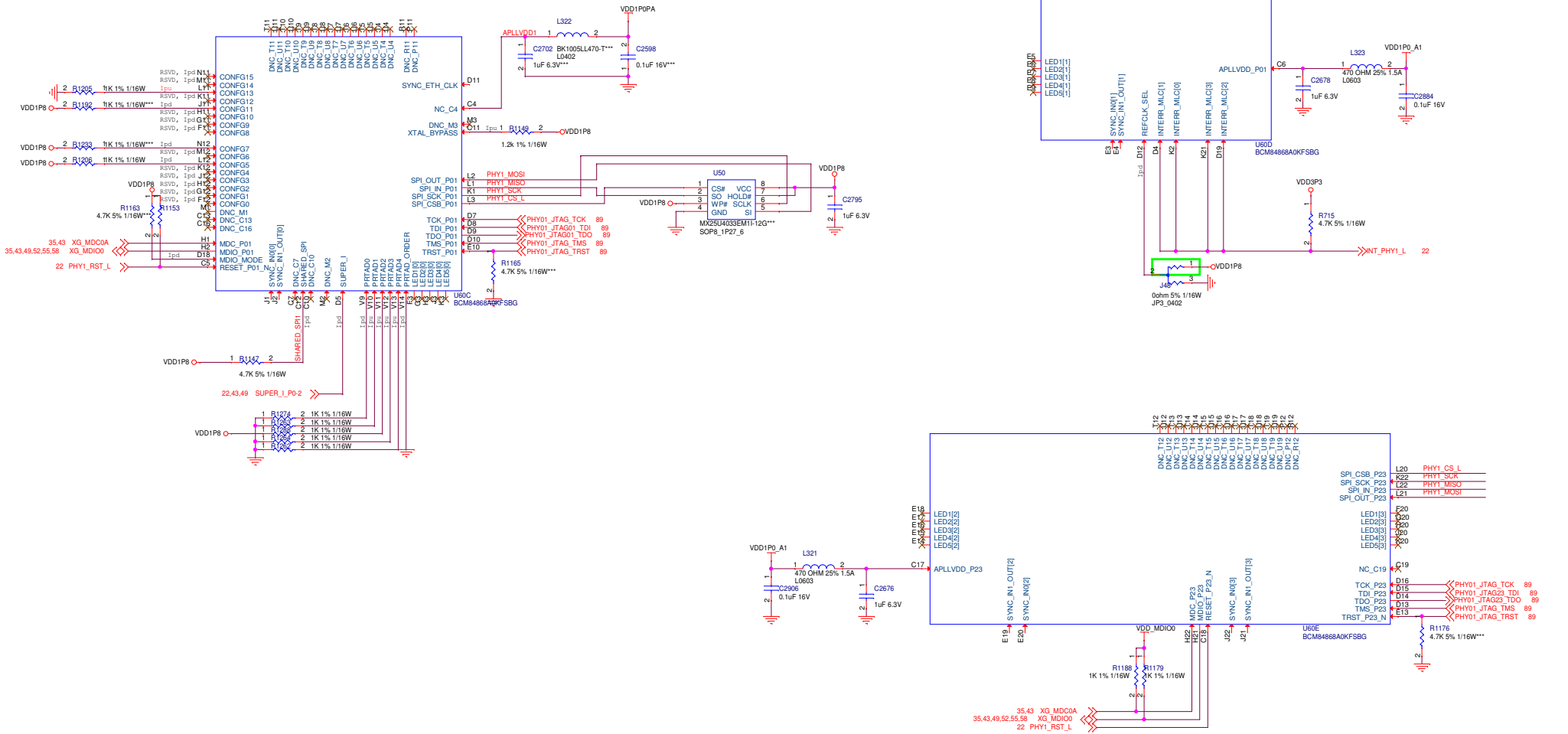
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DOC NO:

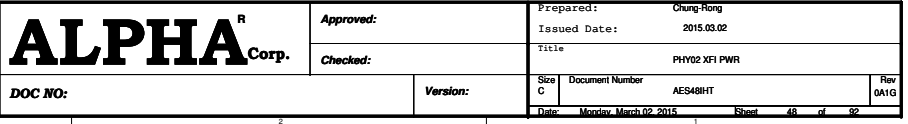
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Checked:		Issued Date: 2015.03.02	
Version:		Title: PHY01 MDI PWR	
Size	Document Number	AES48HT	Rev 0A1G
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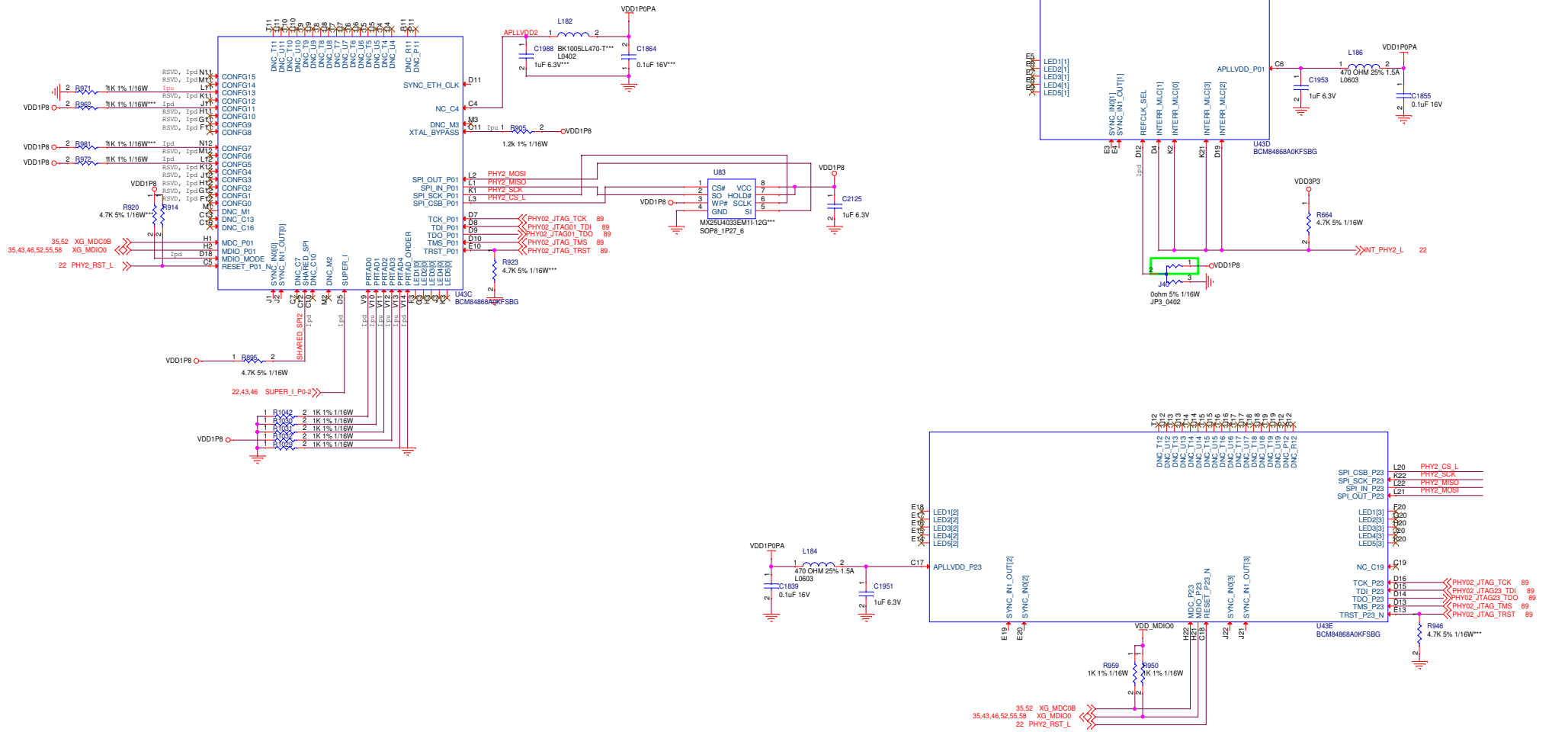




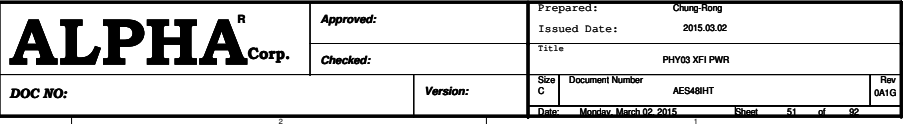






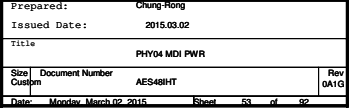


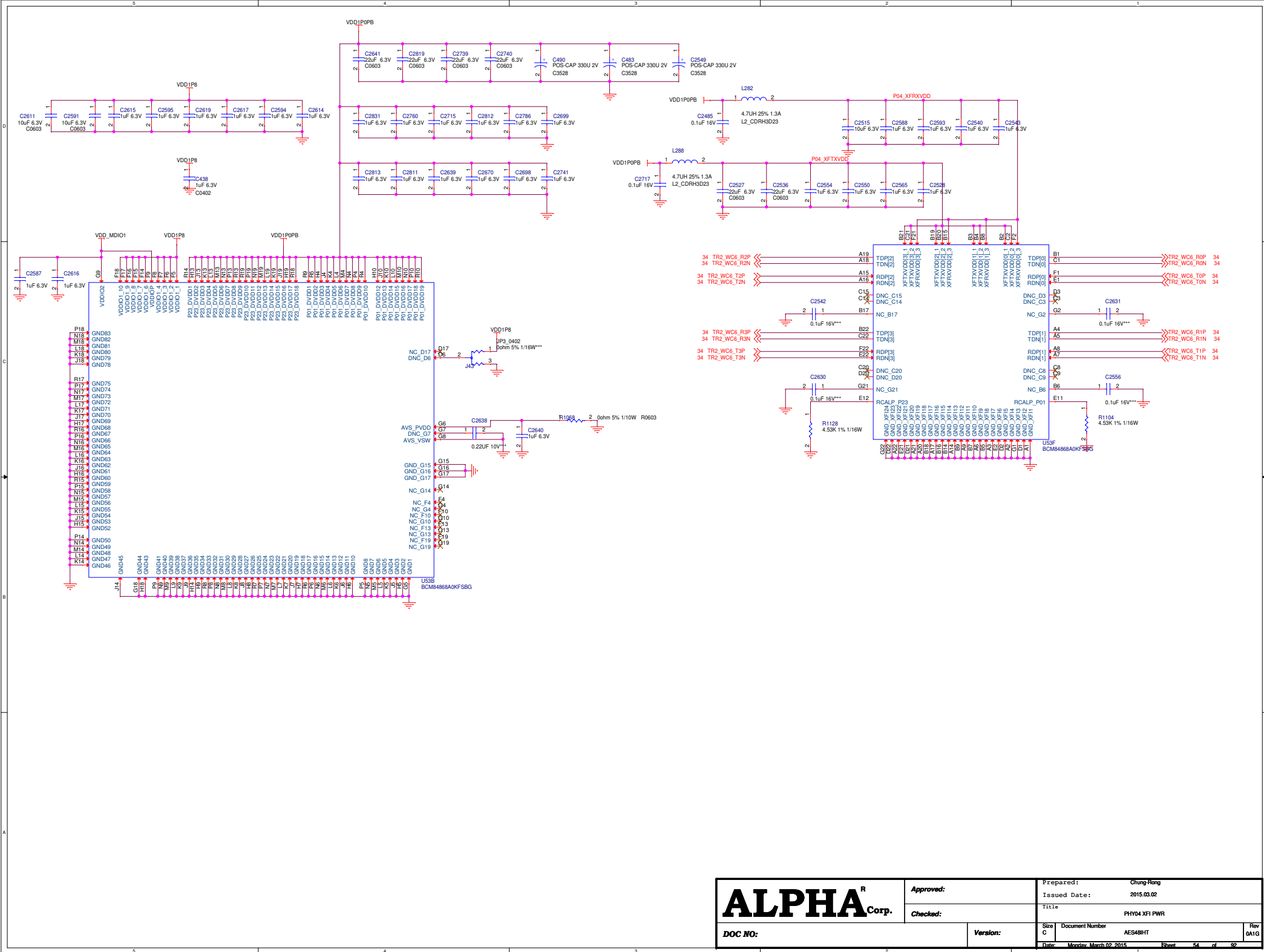




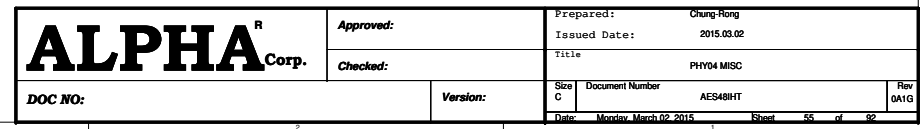


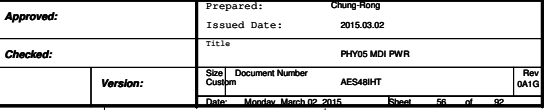






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		<b>Version:</b>		Title: PHY04 XFI PWR	
				Size C Document Number AES48HT	
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				Rev 0A1G	

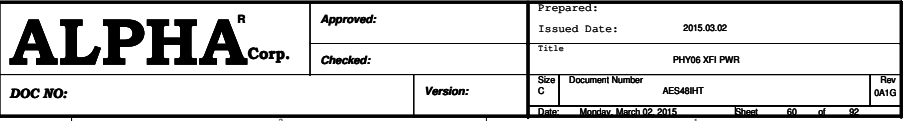




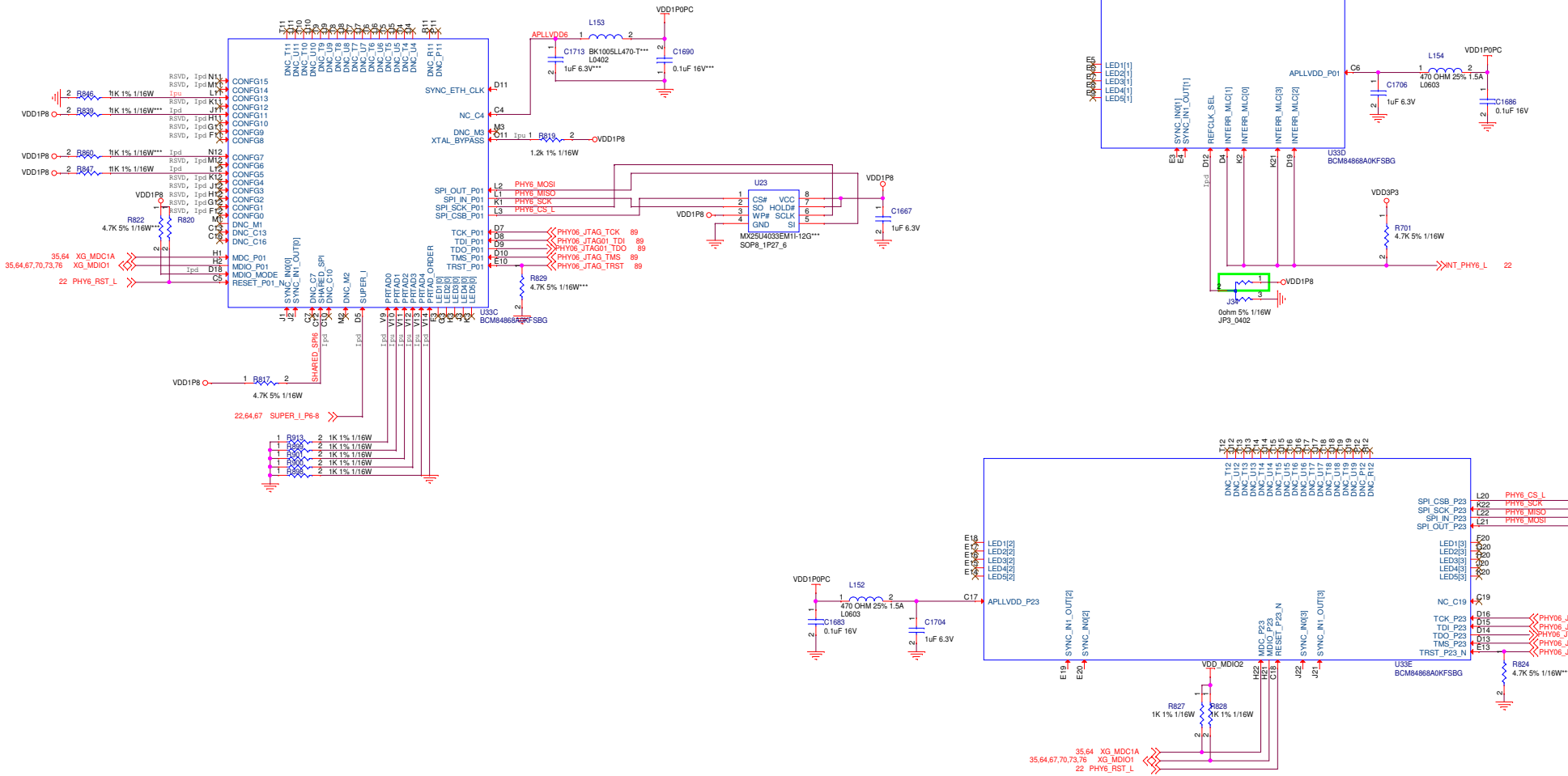


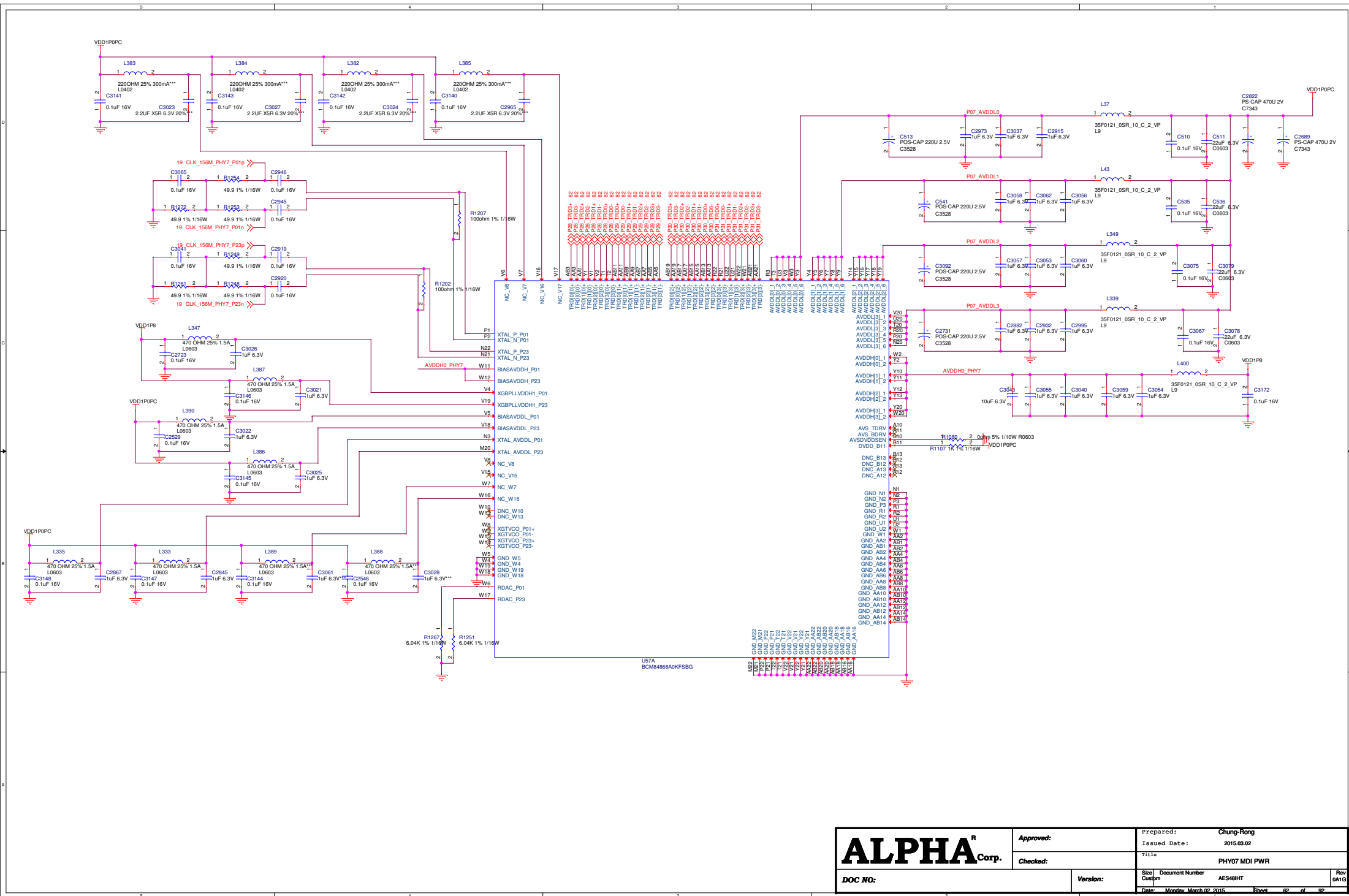








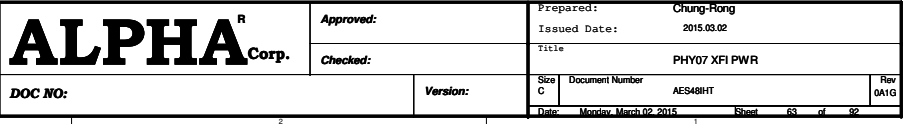


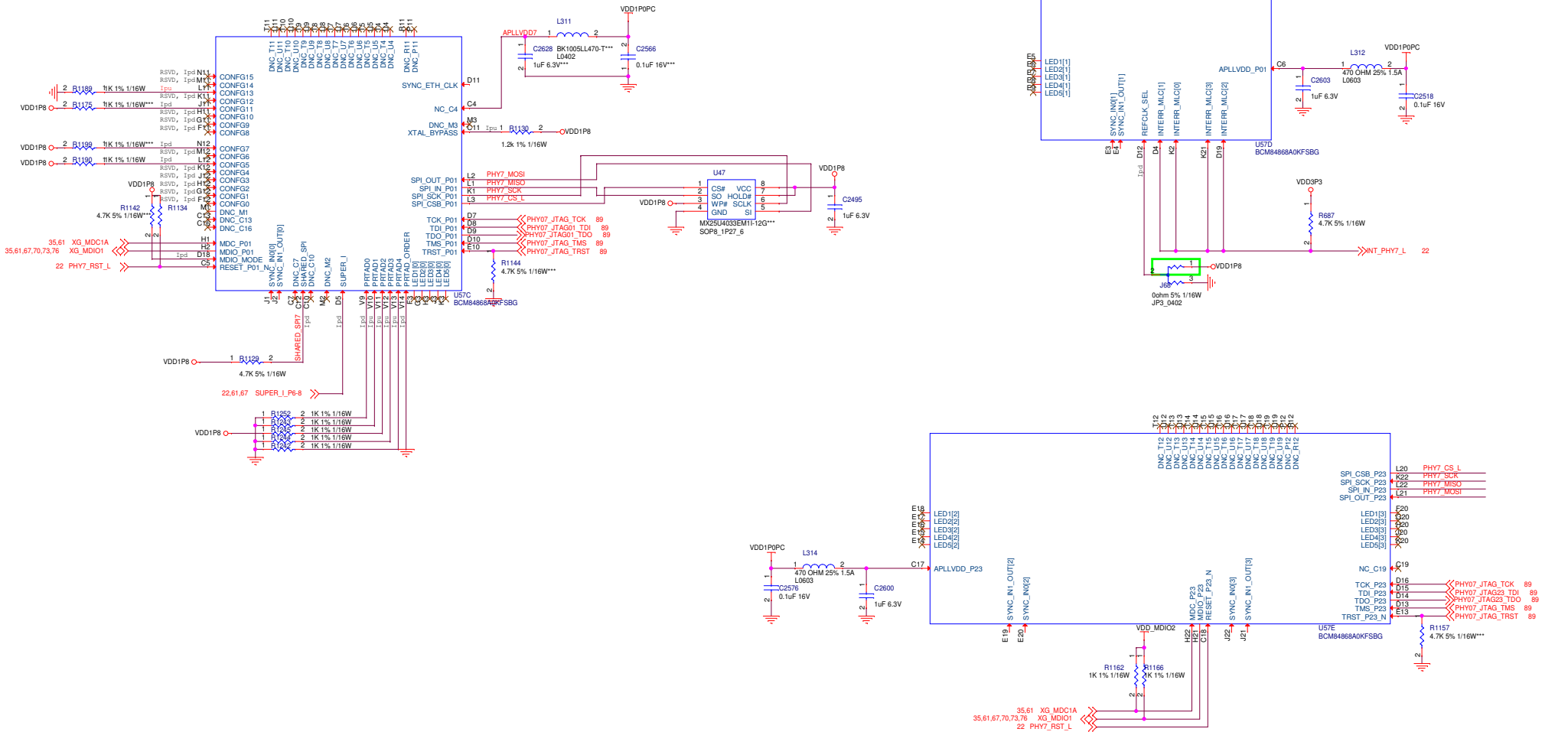


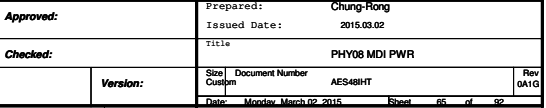
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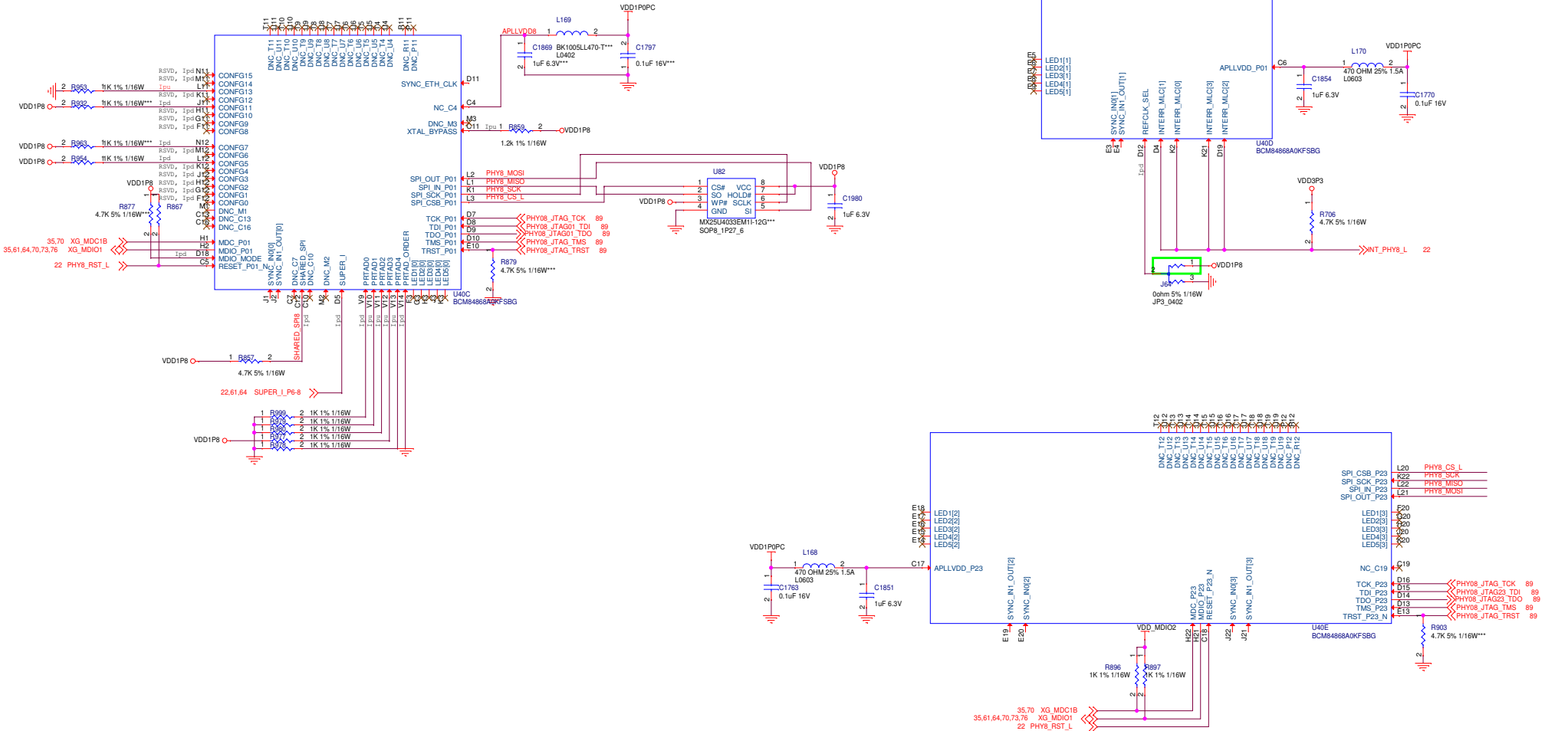
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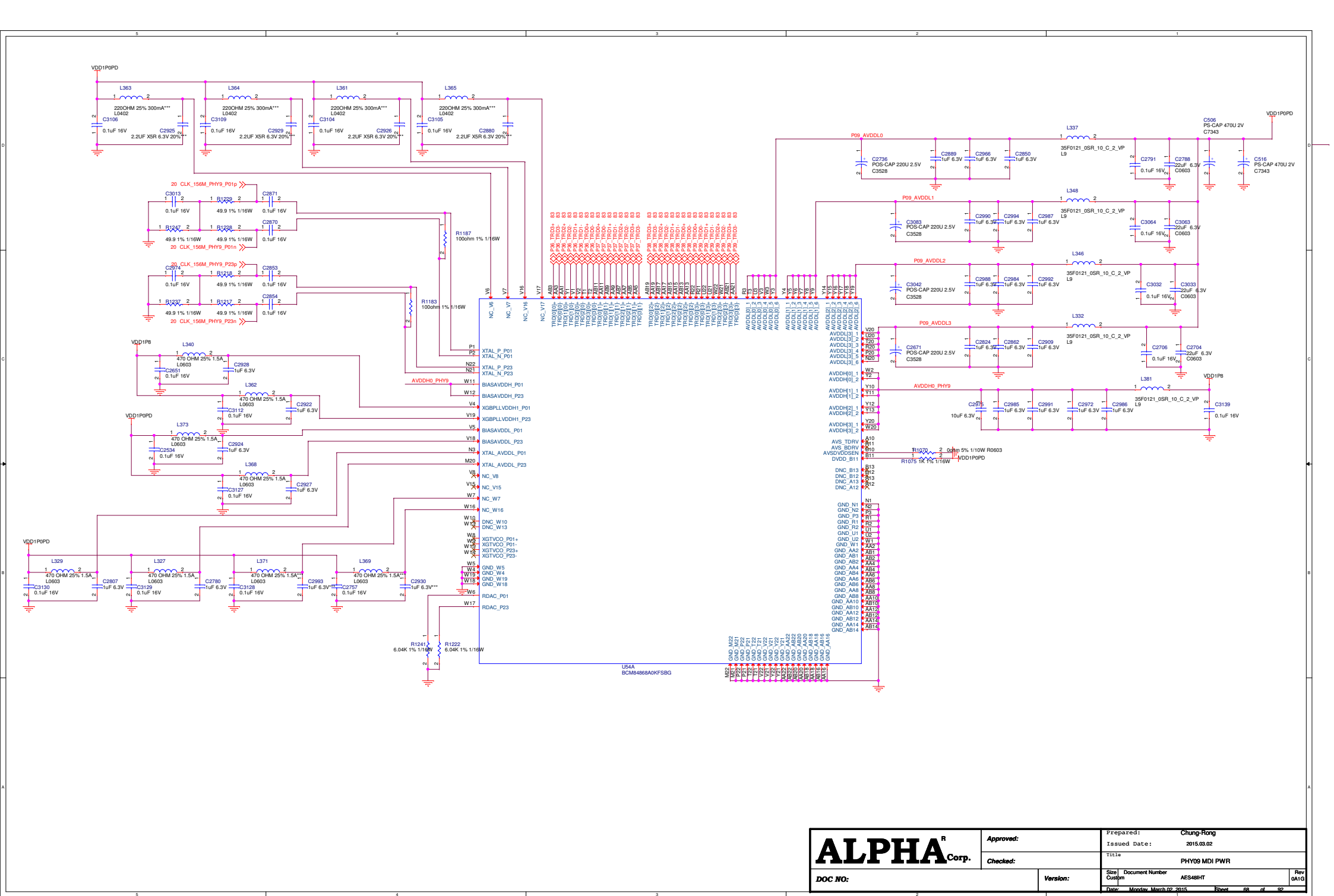










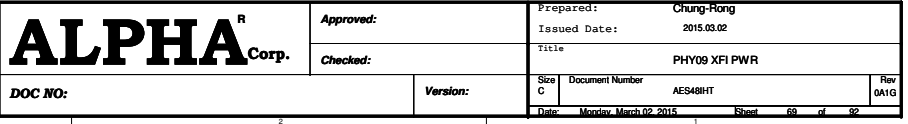


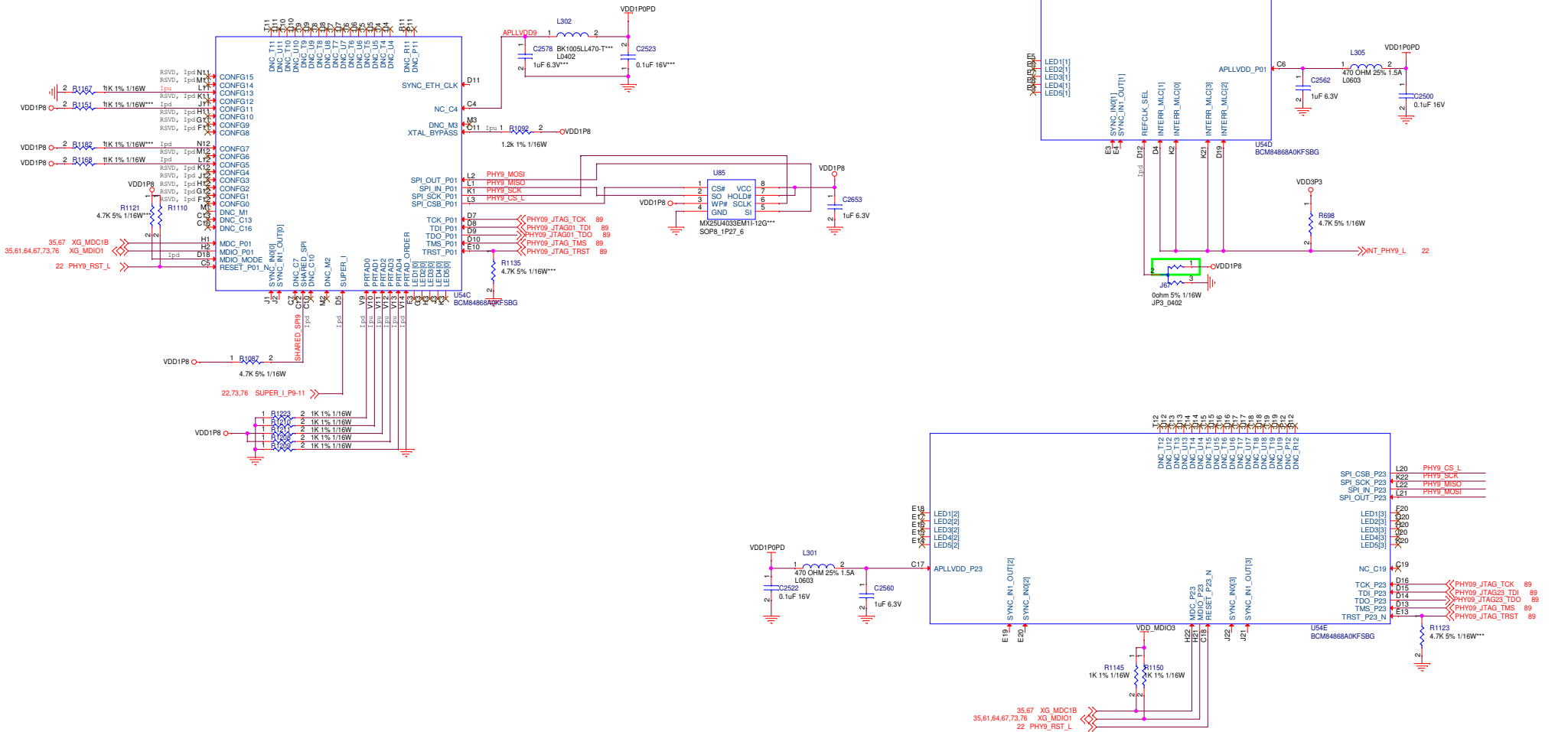
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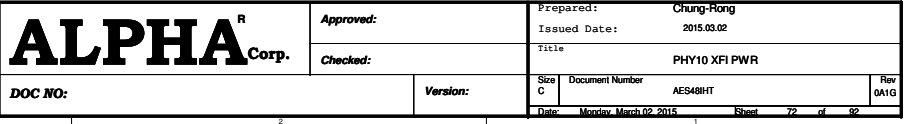
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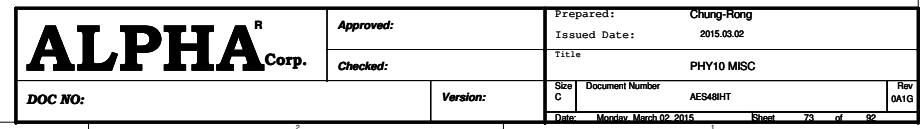






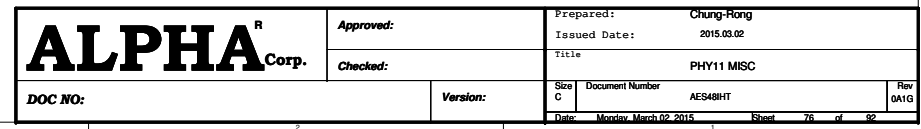














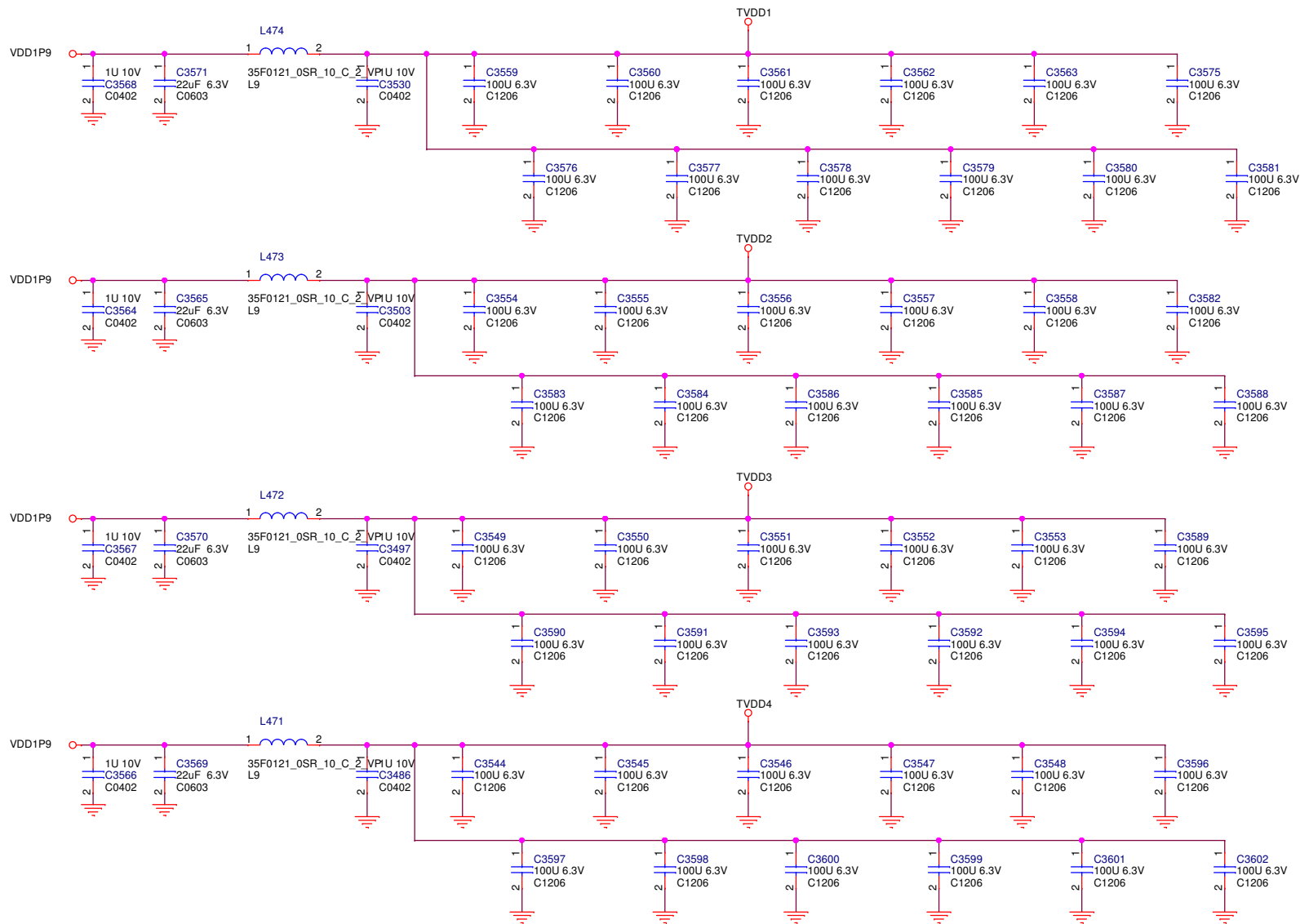




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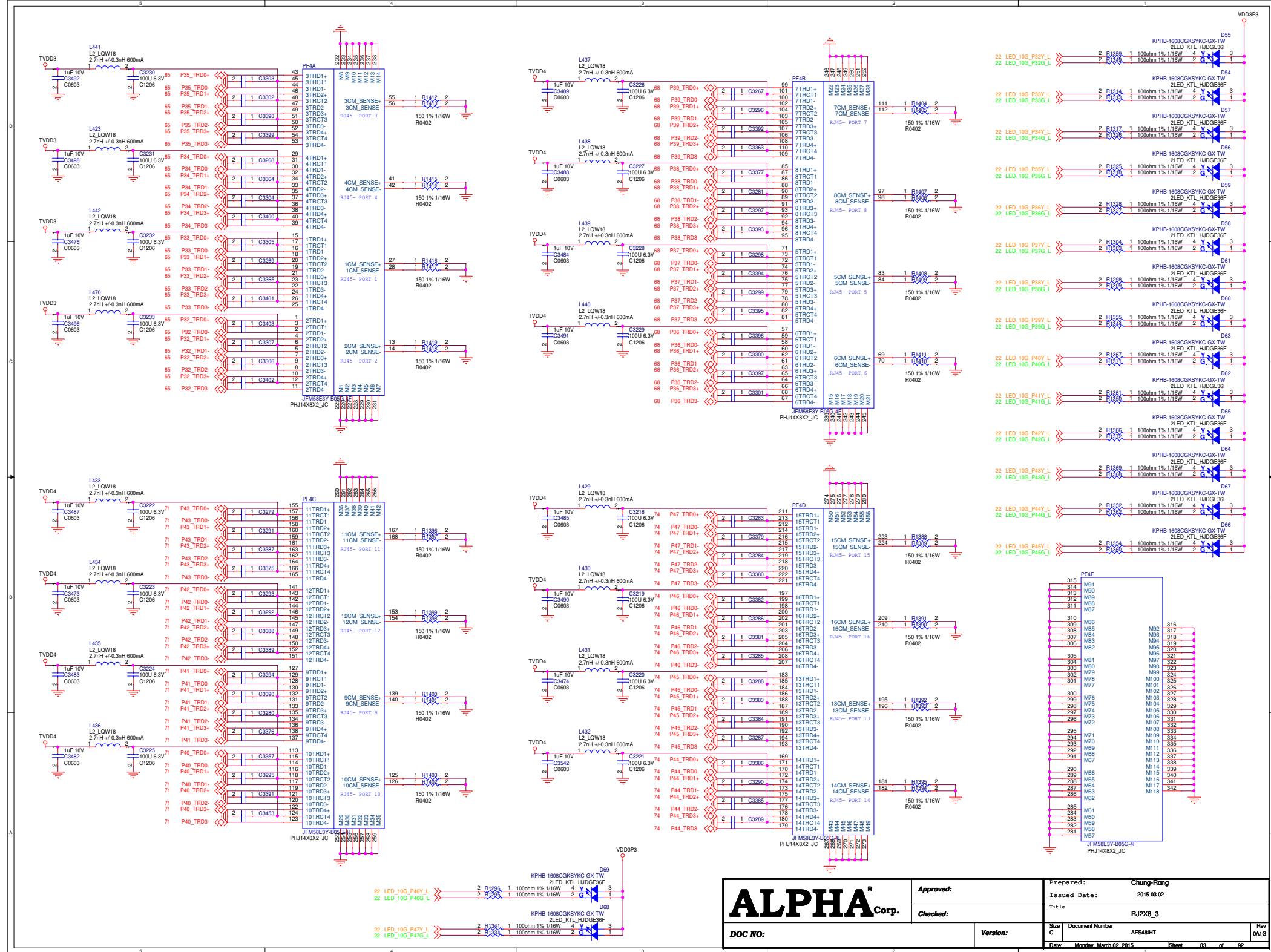


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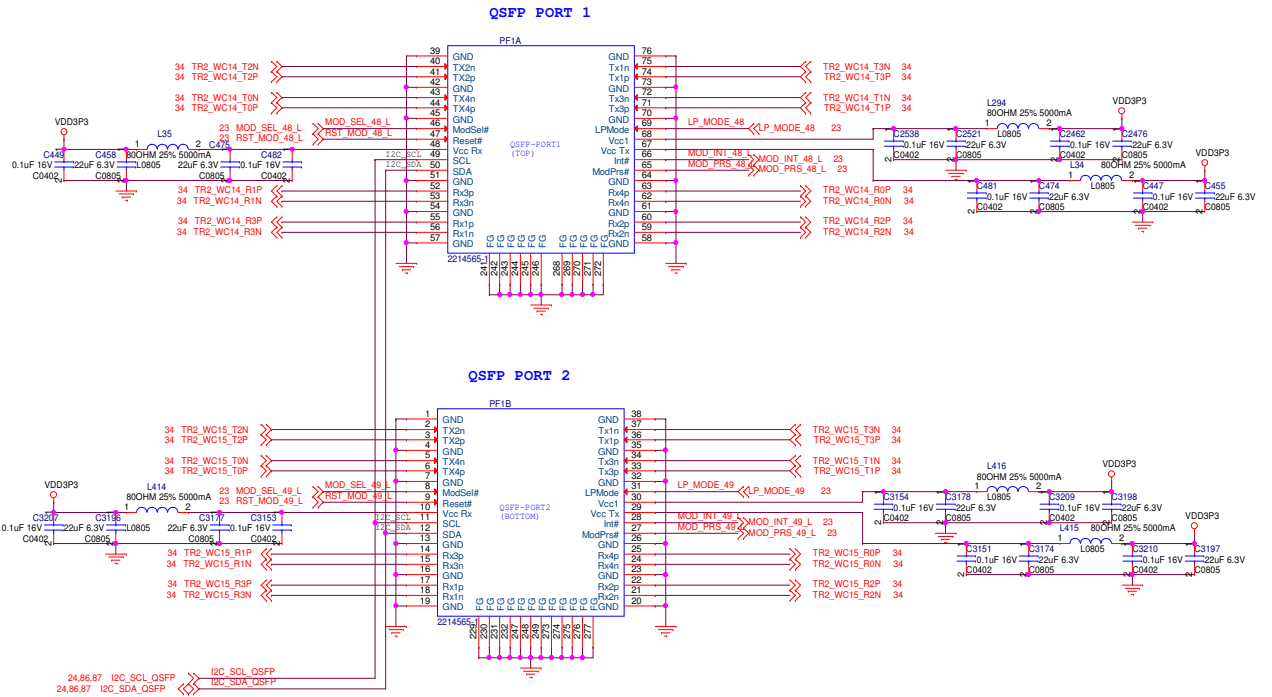
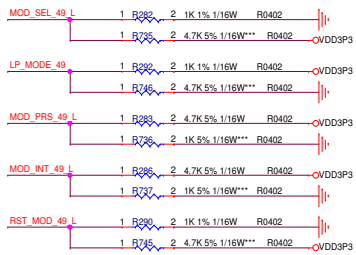
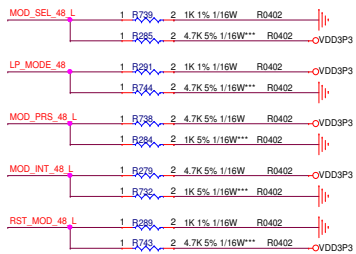
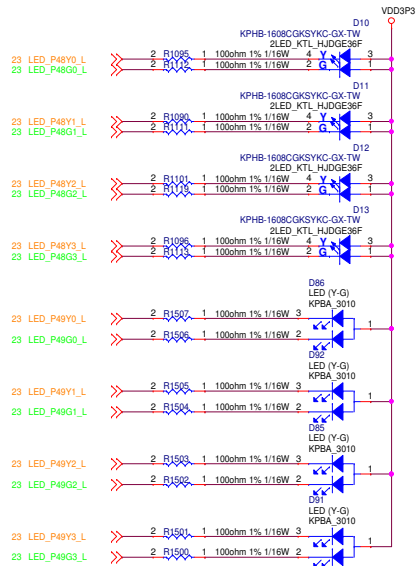
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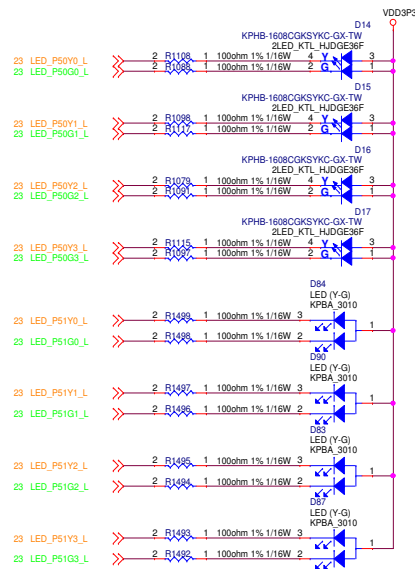
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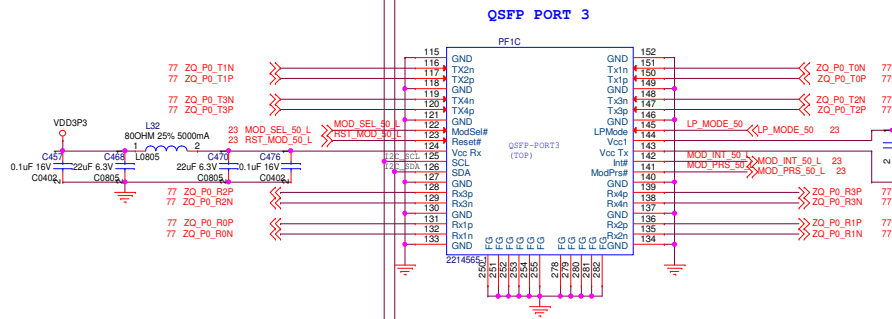
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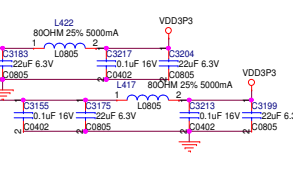
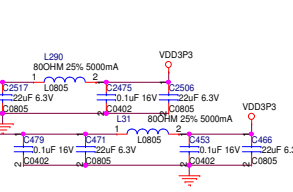
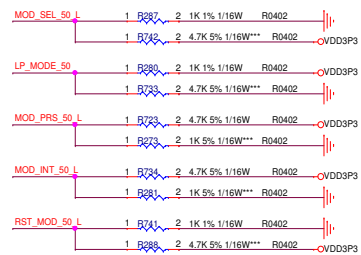
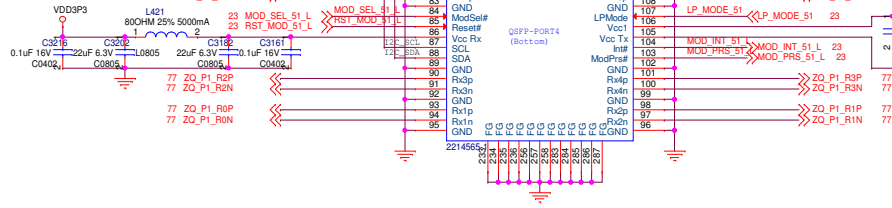


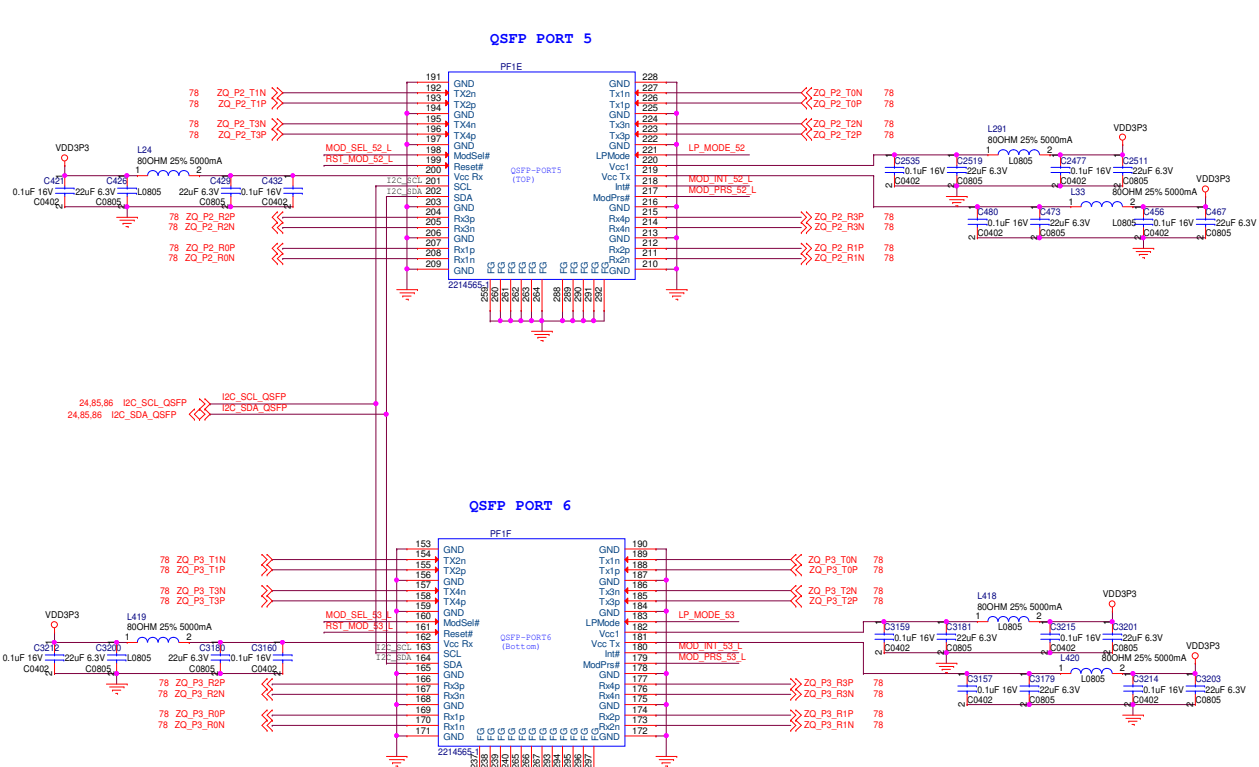
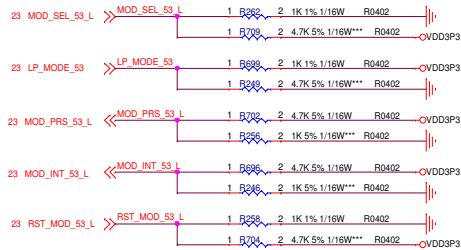
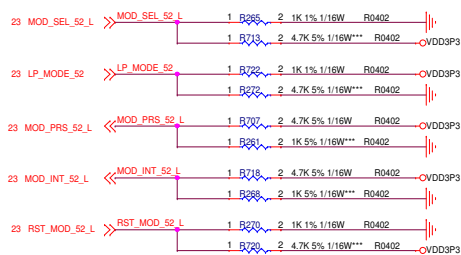
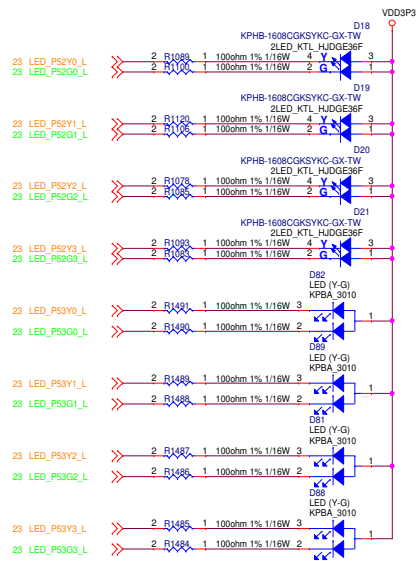


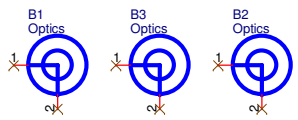
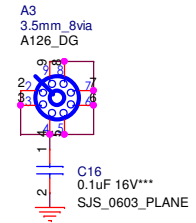
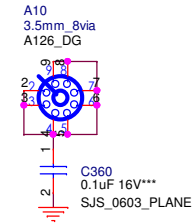
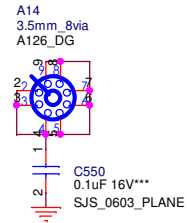
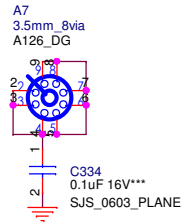
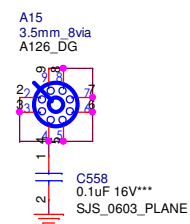
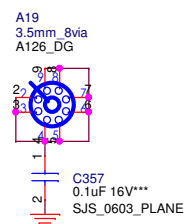
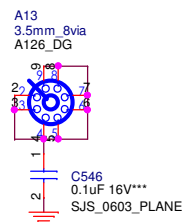
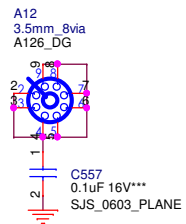
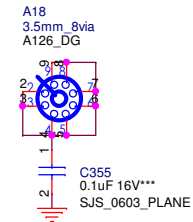
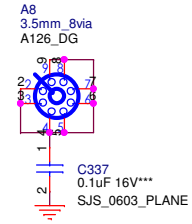
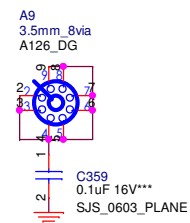
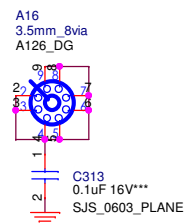
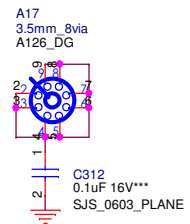
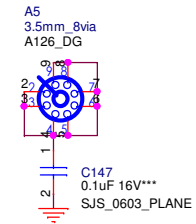
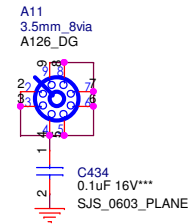
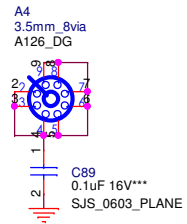
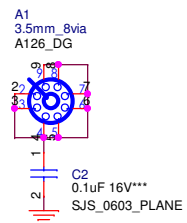
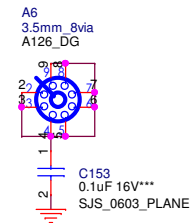
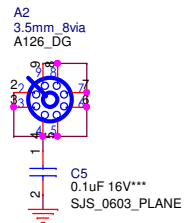
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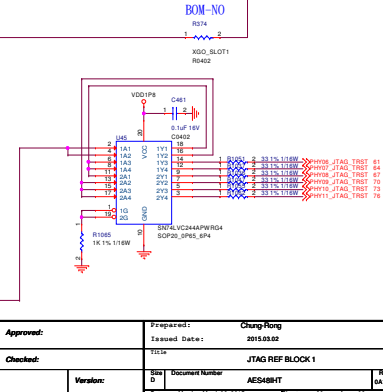
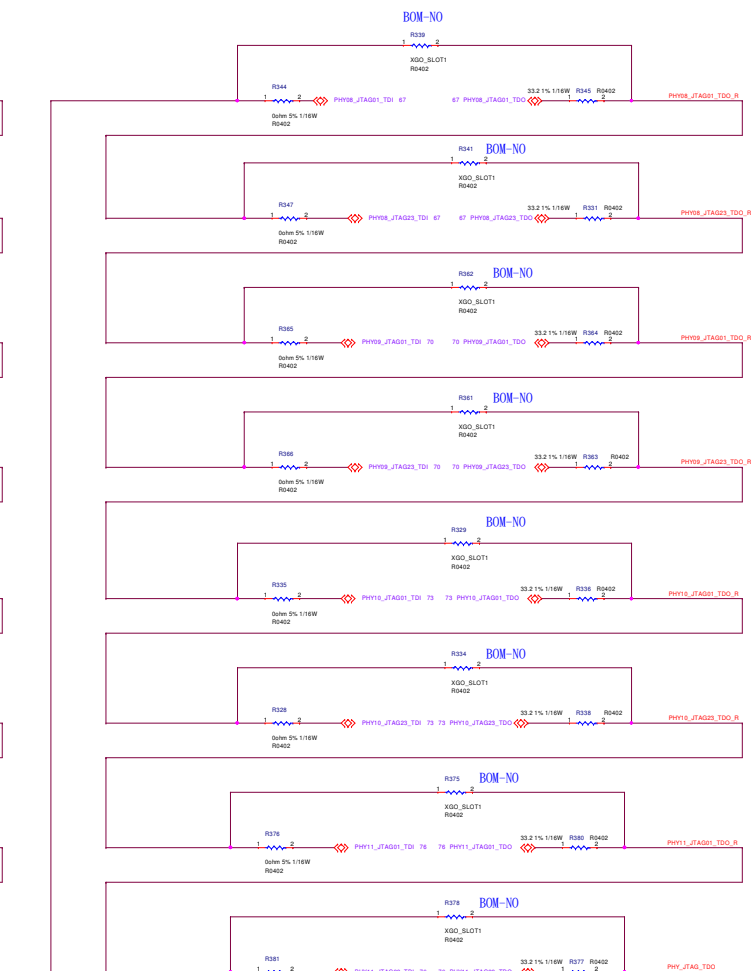
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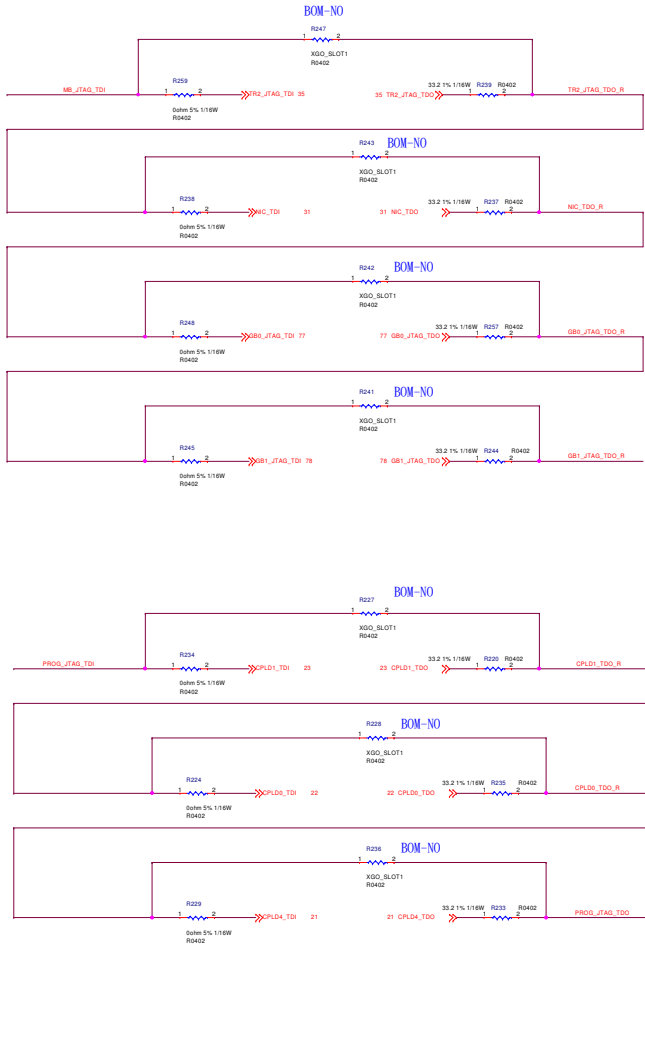


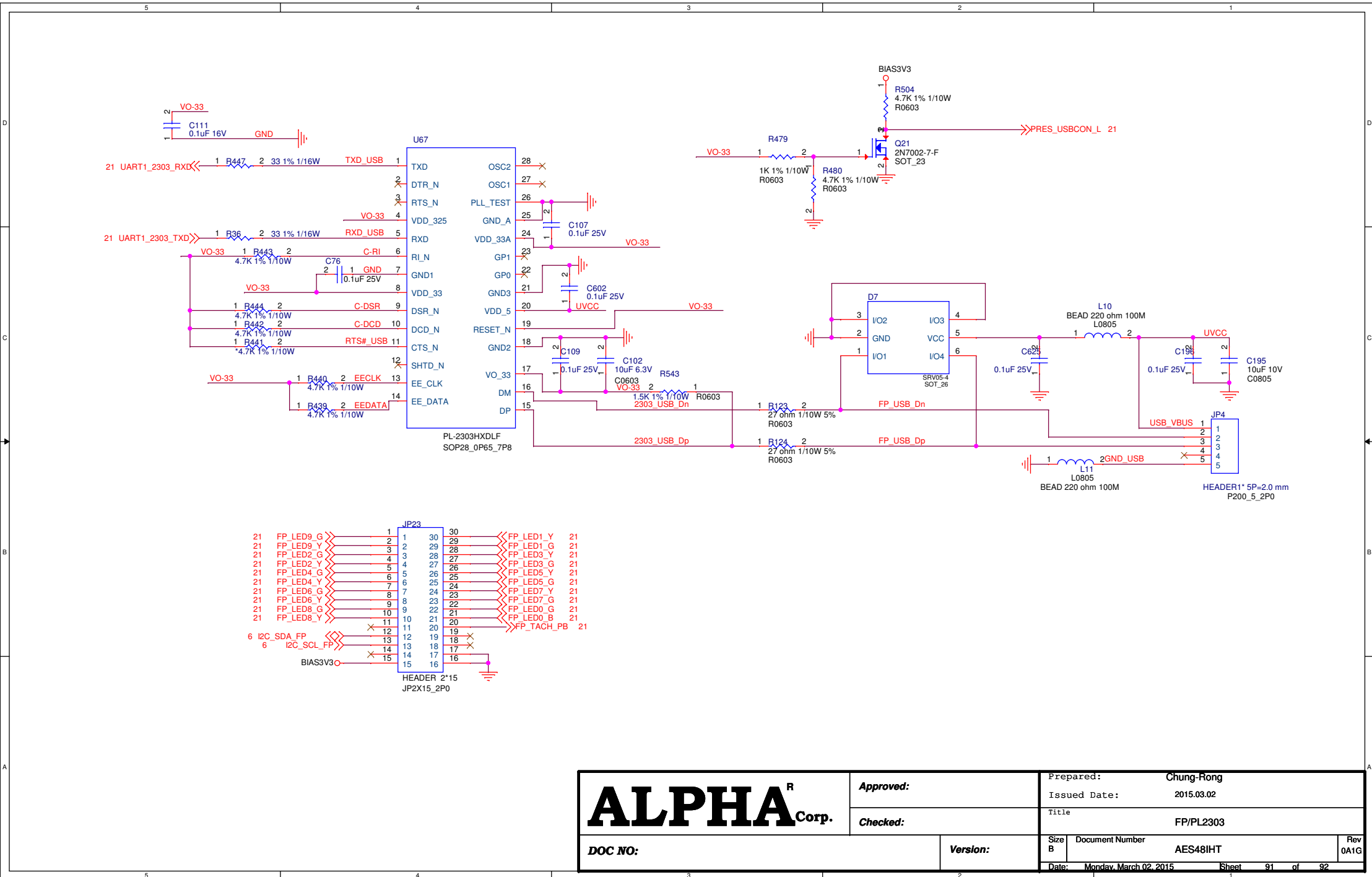




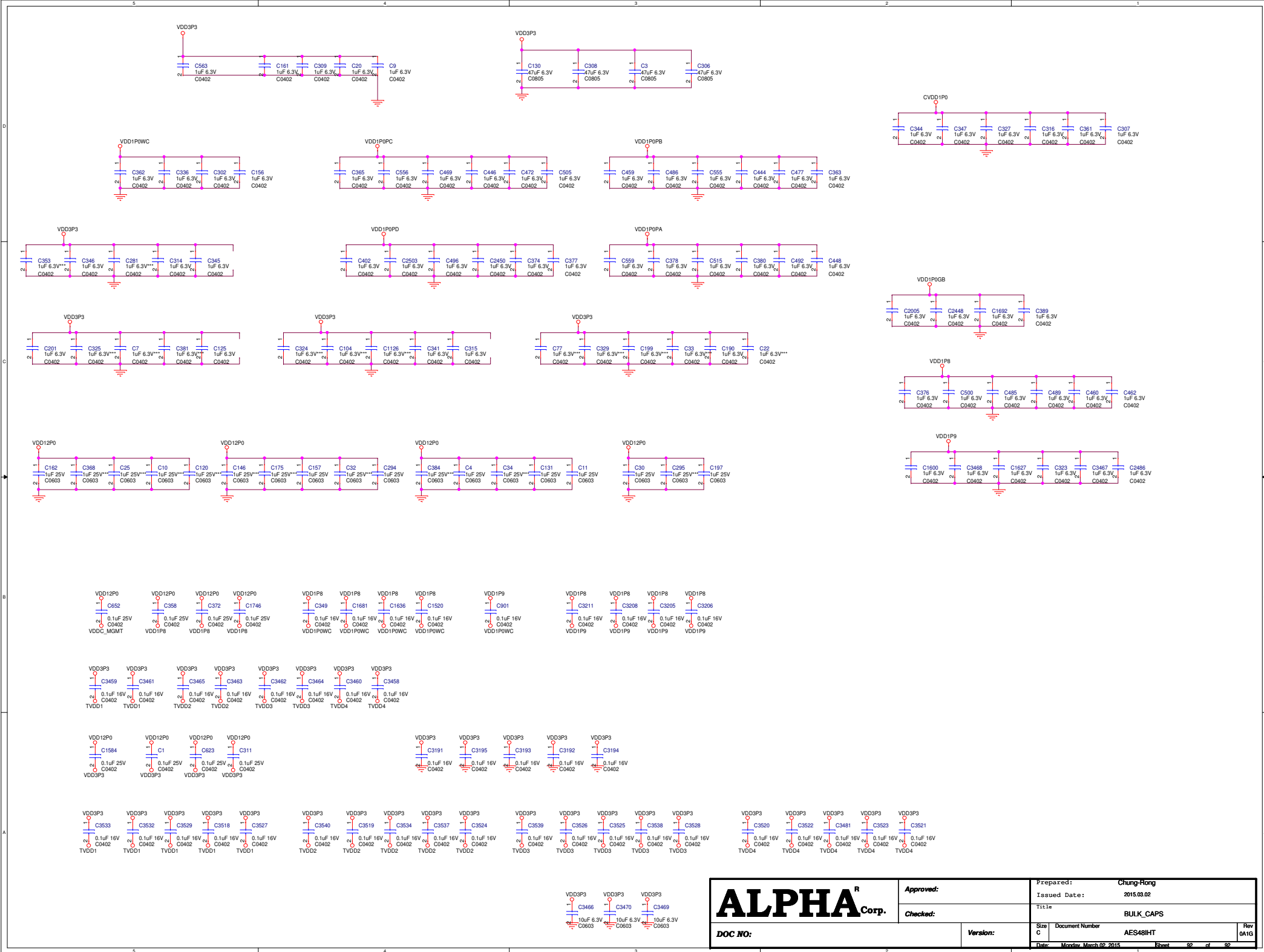
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