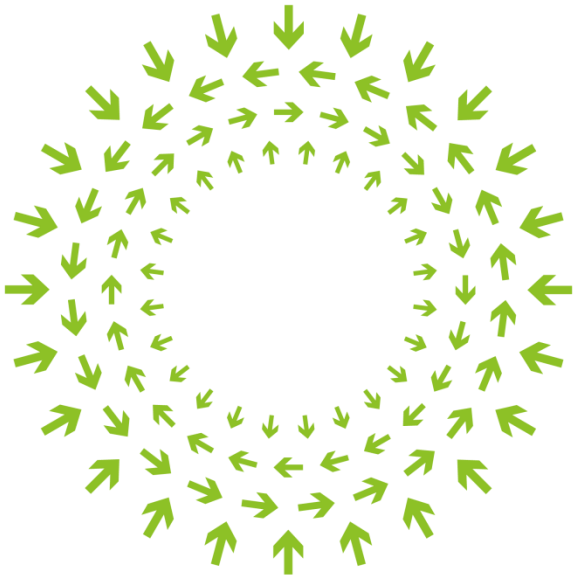

OPEN

Compute Project

UfiSpace S9500-30XS

Programming guide

Revision 1.0

Author: Eason Huang/Hector Zhang

License

Revision History

Revision	Date	Author	Description
1.0	Feb. 20, 2019	Eason Huang Hector Zhang	Initial Draft

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1 Overview

This document describes the programming interfaces of the S9500-30XS switch designed for Telco service application. The main purpose is to aid in porting software to the hardware platform.

By providing 10GbE, 25GbE, 100GbE high speed Ethernet ports and PTP/1588V2, SyncE timing synchronization features, S9500-30XS Telco switch enables service providers to deliver next-generation technologies such as 5G mobile Ethernet network, which requires higher data bandwidth and more precise timing synchronization.

With temperature-hardened, high port density, high-throughput, small form factor, low-power-consumption & redundancy (PSU and FAN) features, S9500-30XS Telco switch delivers high system reliability, Ethernet switching performance and intelligence to the network edge in a flexible 1U form factor that helps reduce infrastructure and administrative costs.

1.1 Physical Overview

Front View

Rear View

1.2 Feature Summary

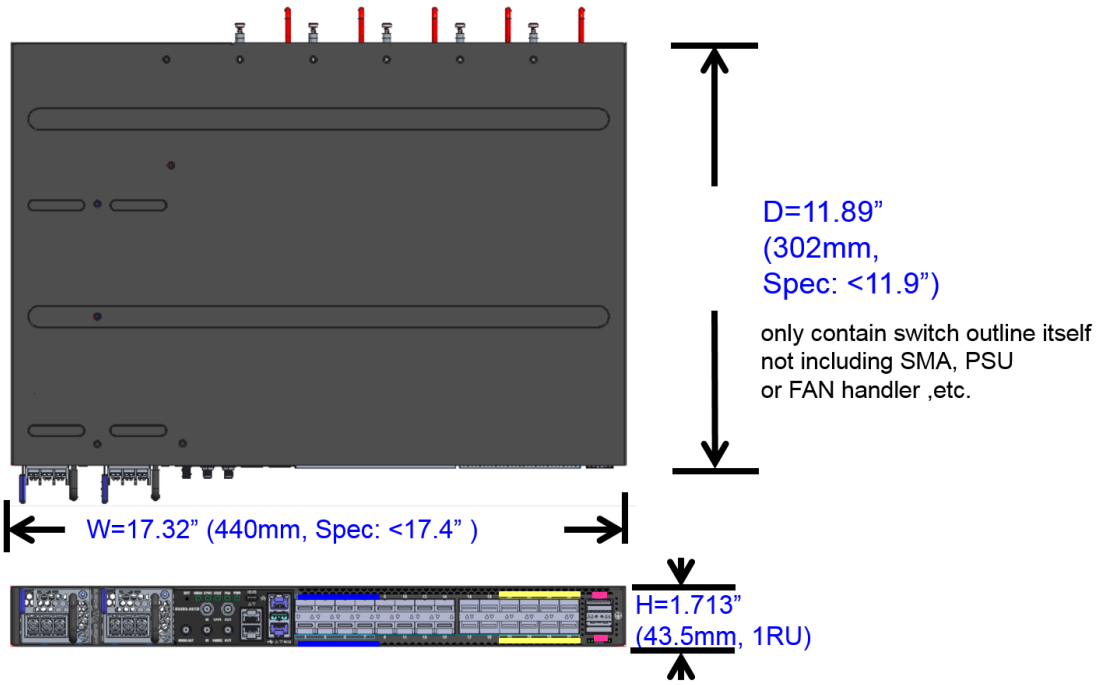
- 1+1 redundant power supply unit
  - 400W output
  - -36~72V DC input
  - Field replaceable
- 4+1 redundant fan module
  - 25000 RPM
  - Front to back air flow
  - Field replaceable
- Ethernet data ports:
  - 20 x 10GbE SFP+ ports
  - 8 x 25GbE SFP28 ports
  - 2 x 100GbE QSFP28 ports
- Timing Synchronization:
  - 1588V2 and SyncE with T-GM, T-TSC, T-TC, T-OC, T-BC support
  - Input source : GNSS/GPS, E1/T1, ToD, 1PPS and 10MHz
  - Output source : 1PPS and 10MHz
- Front/Real panel LED indicators:
  - 1 x power status LED
  - 1 x FAN status LED
  - 1 x system status LED
  - 1 x synchronization status LED
  - 1 x GNSS\GNSS status LED
  - Per port FAN status LED
  - Per port PSU status LED
  - Per port link status LED
- Management interfaces:
  - 1 x GbE OOB management port (CPU)
  - 1 x USB2.0 Type-A general purpose port
  - 1 x RS232 console port in RJ45 form factor
  - 1 x USB console port in Micro USB form factor
  - 1 x tact switch for system reset/reload default configuration

1.3 Mechanical Outline

S9500-30XS chassis is designed to meet cabinet with 19'' depth installation requirement. This 1RU system mechanical dimension is: 440mm (W) x 302mm (D) x 43.5mm (H).

Dimensions

	Inches	Millimeters
Length	11.89	302
Width	17.32	440
Height	1.71	43.5



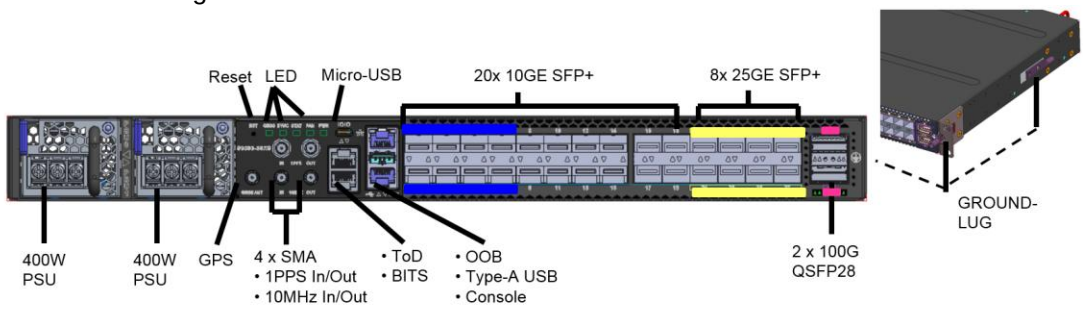
1.4 Front & Real Panel Design

➢ S9500-30XS front panel IO ports & LED include below functionalities:

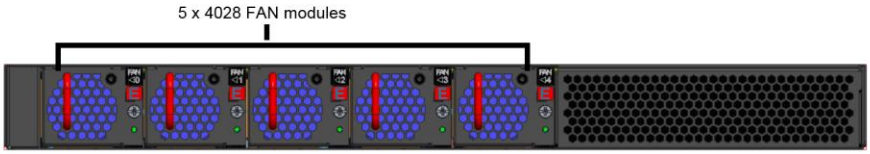
- Ethernet data ports
  - ✓ 2x 100G QSFP28 ports
  - ✓ 8x 25G SFP28 ports
  - ✓ 20x 10G SFP+ ports
- Timing synchronization ports
  - ✓ 1x GNSS port with SMA connector
  - ✓ 1x T1/E1 port with RJ45 form factor
  - ✓ 1x ToD port with RJ45 form factor
  - ✓ 4x SMA ports with 1PPS and 10MHz ref. clock input/output
- Management ports (Share between CPU and BMC)
  - ✓ 1x OOB port
  - ✓ 1x Type A USB port
  - ✓ 1x console port in RJ45
  - ✓ 1x console port in Micro-USB
- System status LED
  - ✓ Power status LED
  - ✓ FAN status LED
  - ✓ GNSS status LED
  - ✓ Synchronization status LED
- Ethernet ports LED
  - ✓ OOB copper ports LED
  - ✓ Data traffic fiber ports LED

- S9500-30XS Real panel design:
- FAN module
- FAN status LED

Detailed IO arrangement is shown as below:



Note: The blue bar under the I/O means those ports are capable for ER/ZR optics module.



1.5 LED Indicators

System LED Function/State	Meaning	Comment
PWR (Green/Yellow):		
OFF	No power.	
Solid Green	System power good	
Blinking Green	Heater is in process	
Solid Yellow	System power good but heater heating failed	
Blinking Yellow	System DC/DC power fail	
FAN (Green/Yellow):		
OFF	No power.	
Solid Green	All FAN modules work well	
Blinking Green	FANs are turned off in -30~-40°C environment	
Solid Yellow	One FAN module fail but system works well	
Blinking Yellow	One more FAN modules fail and need fix ASAP	
STATUS (Green/Yellow):		
OFF	System is powered off	
Solid Green	System boot complete	
Blinking Green	System in booting	

System LED Function/State	Meaning	Comment
Solid Yellow	BMC or BIOS boot failed	
Blinking Yellow	Reserved.	
GNSS (Green/Yellow):		
OFF	GNSS active antenna is open or not installed	
Solid Green	GNSS works well	
Blinking Green	System is locked to GNSS	
Solid Yellow	GNSS acquisition or tracking fail	
Blinking Yellow	GNSS antenna is short to ground	
SYNC (Green/Yellow):		
OFF	System timing/clock synchronization is disabled (Don't synchronize to external clock reference)	
Solid Green	System timing/clock is synchronized to external timing/clock reference (ex: GNSS, 1PPS, PTP, BITS, etc)	
Blinking Green	Reserved	
Solid Yellow	System timing/clock synchronization is in free-run or holdover mode	
Blinking Yellow	Reserved	

For SFP+, SFP28 and QSFP28 ports are controlled by serial LED interface of MAC.

Ethernet LED Function/State	Meaning	Comment
SFP+（port 0~19）(Green/Yellow):		
OFF	No link on the SFP+ port	
Solid Green	SFP+ port link at 10G mode	
Blinking Green	SFP+ port is transmitting at 10G mode	
Solid Yellow	SFP+ port link at 1G/100M mode	
Blinking Yellow	SFP+ port is transmitting at 1G/100M mode	
SFP28（port 20~27）(Green/Yellow):		
OFF	No link on the SFP28 port	
Solid Green	SFP28 port link at 25G mode	
Blinking Green	SFP28 port is transmitting at 25G mode	
Solid Yellow	SFP28 port link at 10G/1G mode	
Blinking Yellow	SFP28 port is transmitting at 10G/1G mode	
QSFP28（port 28~29）(Green/Yellow):		
OFF	No link on the QSFP28 port	

Ethernet LED Function/State	Meaning	Comment
Solid Green	QSFP28 port link at 100G mode	
Blinking Green	QSFP28 port is transmitting at 100G mode	
Solid Yellow	QSFP28 port link at 40G mode	
Blinking Yellow	QSFP28 port is transmitting at 40G mode	
QSFP28（port 28~29）(With break out cable) (Green/Yellow):		
OFF	No link on the QSFP28 port	
Solid Green	QSFP28 port link at 25G mode	
Blinking Green	QSFP28 port is transmitting at 25G mode	
Solid Yellow	QSFP28 port link at 10G mode	
Blinking Yellow	QSFP28 port is transmitting at 10G mode	
OOB port (Green/Yellow):		
OFF	No link on the OOB port	
Solid Green	OOB port link at 1G mode	
Blinking Green	OOB port is transmitting at 1G mode	
Solid Yellow	OOB port link at 10/100M mode	
Blinking Yellow	OOB port is transmitting at 10/100M mode	

1.6 Network Ports

1.6.1.1 Ports Assignment

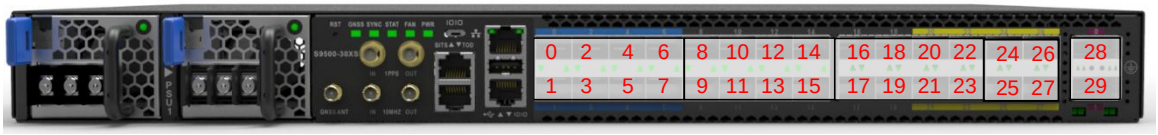


Table below shows the network ports numbering & speed:

Function	Port#	Speed	Notes
SFP+ Ports	P0	100M/1G/10G	ZR optics capable
	P1	100M/1G/10G	ZR optics capable
	P2	100M/1G/10G	ZR optics capable
	P3	100M/1G/10G	ZR optics capable
	P4	100M/1G/10G	ZR optics capable
	P5	100M/1G/10G	ZR optics capable
	P6	100M/1G/10G	ZR optics capable
	P7	100M/1G/10G	ZR optics capable
	P8	100M/1G/10G	PHY-less port
	P9	100M/1G/10G	PHY-less port
	P10	100M/1G/10G	PHY-less port
	P11	100M/1G/10G	PHY-less port
	P12	100M/1G/10G	PHY-less port

Function	Port#	Speed	Notes
	P13	100M/1G/10G	PHY-less port
	P14	100M/1G/10G	PHY-less port
	P15	100M/1G/10G	PHY-less port
	P16	100M/1G/10G	PHY-less port
	P17	100M/1G/10G	PHY-less port
	P18	100M/1G/10G	PHY-less port
	P19	100M/1G/10G	PHY-less port
SFP28 Ports	P20	1G/10G/25G	PHY-less port
	P21	1G/10G/25G	PHY-less port
	P22	1G/10G/25G	PHY-less port
	P23	1G/10G/25G	PHY-less port
	P24	1G/10G/25G	PHY-less port
	P25	1G/10G/25G	PHY-less port
	P26	1G/10G/25G	PHY-less port
	P27	1G/10G/25G	PHY-less port
QSFP28 Ports	P0-0	10G/40G/100G	ER4 optics capable
	P0-1	10G/40G/100G	ER4 optics capable
	P0-2	10G/40G/100G	ER4 optics capable
	P0-3	10G/40G/100G	ER4 optics capable
	P1-0	10G/40G/100G	ER4 optics capable
	P1-1	10G/40G/100G	ER4 optics capable
	P1-2	10G/40G/100G	ER4 optics capable
	P1-3	10G/40G/100G	ER4 optics capable

1.6.1.2 Ports Mapping

<table>
<tr><th colspan="2">Front Panel</th><th colspan="4">PHY</th><th colspan="4">MAC</th></tr>
<tr><th>Function</th><th>Port#</th><th>DEVICE</th><th>PORT#</th><th>MIIM</th><th>MIIM ADDR</th><th>DEVICE</th><th>SerDes Core</th><th>PORT#</th><th>Interface</th></tr>
<tr><td rowspan="24">SFP+ Ports</td><td>P0</td><td rowspan="7">BCM82780F</td><td>0</td><td rowspan="7">M1</td><td>00001</td><td rowspan="24">MAC BCM88470</td><td rowspan="4">PM10Q-6</td><td>24</td><td rowspan="24">XFI SFI</td></tr>
<tr><td>P1</td><td>1</td><td>00010</td><td>26</td></tr>
<tr><td>P2</td><td>2</td><td>00011</td><td>25</td></tr>
<tr><td>P3</td><td>3</td><td>00100</td><td>27</td></tr>
<tr><td>P4</td><td>4</td><td>00101</td><td rowspan="4">PM10Q-5</td><td>23</td></tr>
<tr><td>P5</td><td>5</td><td>00110</td><td>22</td></tr>
<tr><td>P6</td><td>6</td><td>00111</td><td>21</td></tr>
<tr><td>P7</td><td>7</td><td>01000</td><td>20</td></tr>
<tr><td>P8</td><td colspan="5" rowspan="12">MAC Internal SerDes</td><td rowspan="4">PM10Q-4</td><td>19</td></tr>
<tr><td>P9</td><td>18</td></tr>
<tr><td>P10</td><td>17</td></tr>
<tr><td>P11</td><td>16</td></tr>
<tr><td>P12</td><td rowspan="4">PM10Q-8</td><td>32</td></tr>
<tr><td>P13</td><td>33</td></tr>
<tr><td>P14</td><td>34</td></tr>
<tr><td>P15</td><td>35</td></tr>
<tr><td>P16</td><td rowspan="4">PM10Q-9</td><td>36</td></tr>
<tr><td>P17</td><td>37</td></tr>
<tr><td>P18</td><td>38</td></tr>
<tr><td>P19</td><td>39</td></tr>
<tr><td rowspan="4">SFP28 Ports</td><td>P20</td><td colspan="5" rowspan="4">MAC Internal SerDes</td><td rowspan="4">PM25-3</td><td>12</td></tr>
<tr><td>P21</td><td>13</td></tr>
<tr><td>P22</td><td>14</td></tr>
<tr><td>P23</td><td>15</td></tr>
</table>

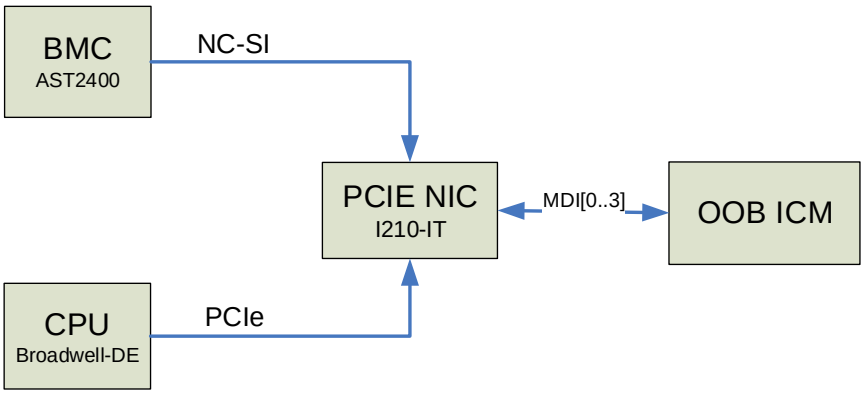
Front Panel		PHY				MAC			
Function	Port#	DEVICE	PORT#	MIIM	MIIM ADDR	DEVICE	SerDes Core	PORT#	Interface
	P24						PM25-2	8	
	P25							9	
	P26							10	
	P27							11	
QSFP28 Ports	P0-0	BCM82398	4-7	M0	00001	MAC BCM88470	PM25-1	3	CAUI4
	P0-1							2	
	P0-2							1	
	P0-3							0	
	P1-0		0-3		00101		PM25-0	7	
	P1-1							6	
	P1-2							5	
	P1-3							4	
xCPU MAC	Lane0					MAC BCM88470	PM10-7	30	10G-KR
	Lane1							28	10G-KR
								29	
								31	
OOB Port	P1 (CPU)	I210-IT #1	1	PCIe		CPU Broadwell-DE			PCIe

1.7 OOB Ports

The S9500-30XS switch includes 1standard GbE RJ45 port for out of band (OOB) management, shared between CPU and BMC. It supports the IEEE 802.3 specification for 10/100/1000Mbps operation.

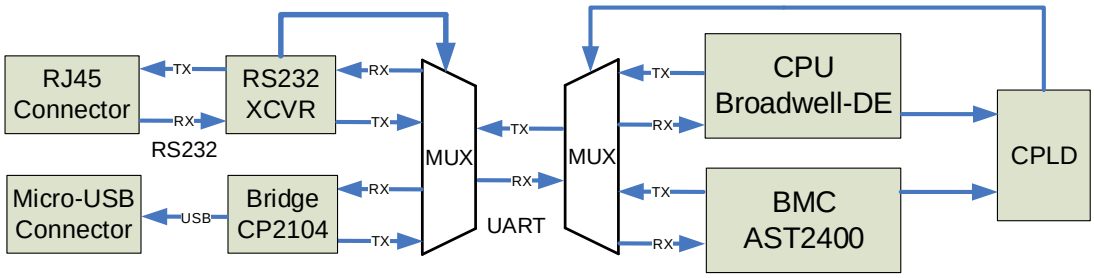
PCIe interface is routed between CPU & NIC I210-IT, OOB supports 10/100/1000Mbps operation. NC-SI is connected between BMC & NIC I210-IT, OOB speed is limited to 100Mbps in this case.

OOB to BMC can be disabled by BIOS.



1.8 Console Port

Two console ports available for S9500-30XS systems access, RS232 & Micro USB console. Both of them can be used for CPU or BMC access. The bound rate is 115200 by default. When either console port cable is plugged, it's active immediately, RJ45 port has higher priority when both ports are present. Console port connection diagram is shown as below:



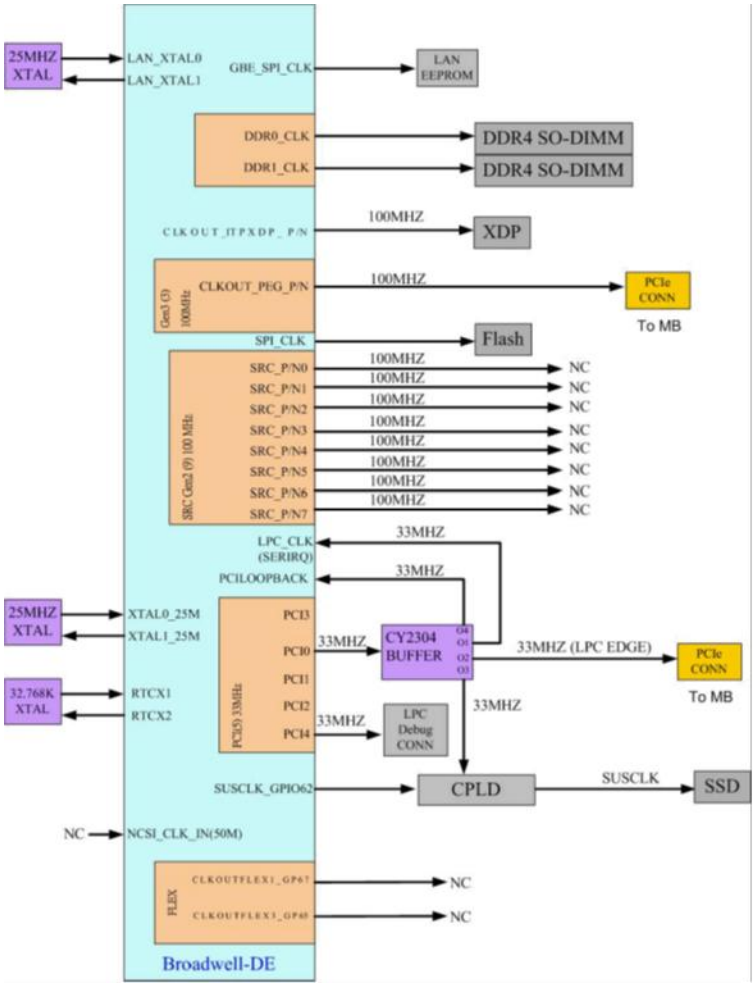
To use the Micro-USB console port, CP2102N driver need to be installed on host PC side.

To access the RJ45 RS232 interface, use a RS-232 to RJ45 adapter. Also, RJ45 RS232 is higher priority than Micro-USB and only activate RJ45 RS232 access if both interfaces are connected by user. The pin definition of the RS232 console port is shown as below.Pin3 is the TX signal from internal processor to external RS232 interface, and Pin6 is the RX signal from external RS232 interface to internal processor.

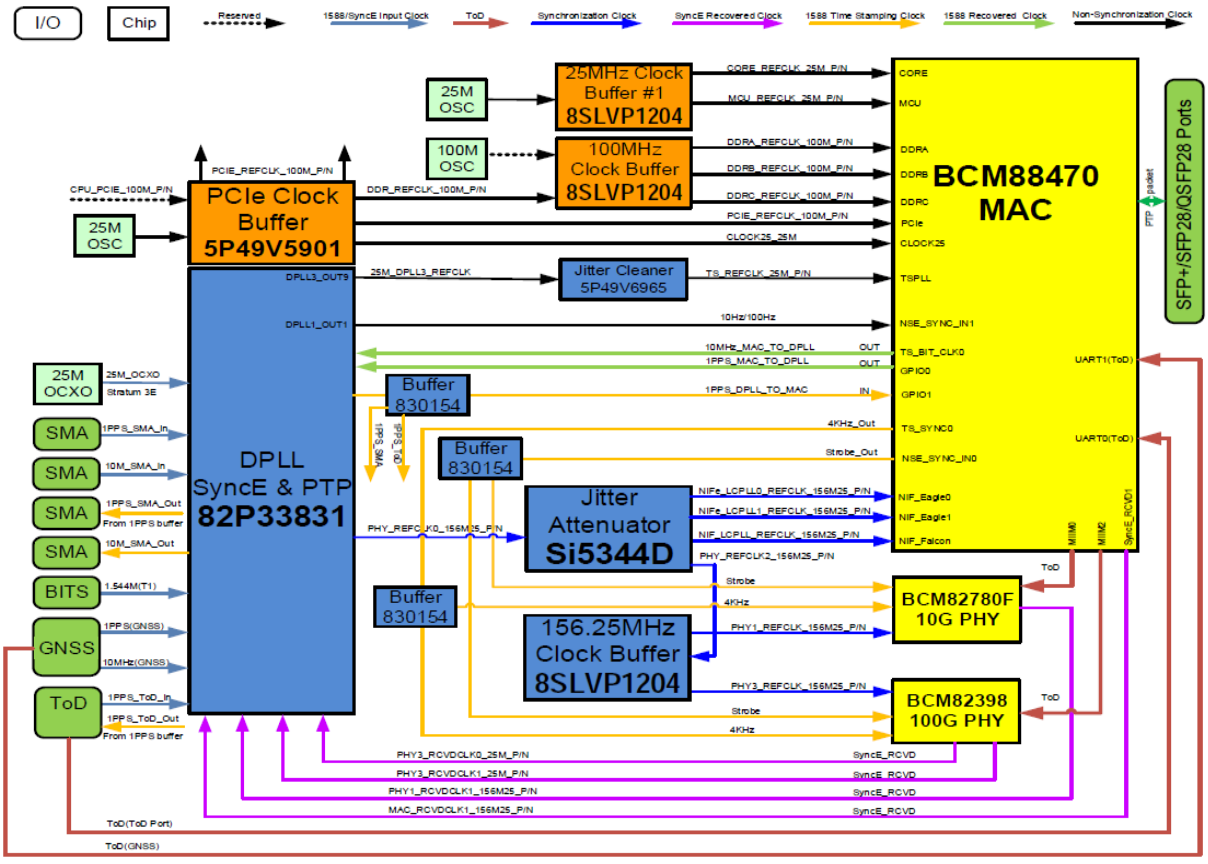
PIN #	Definition	Direction	Note
1	NC		
2	NC		
3	UART_TXD	Out	Console TX
4	GND		
5	GND		
6	UART_RXD	In	Console RX
7	GND		
8	GND		

1.9 Clock Tree

CPU Card

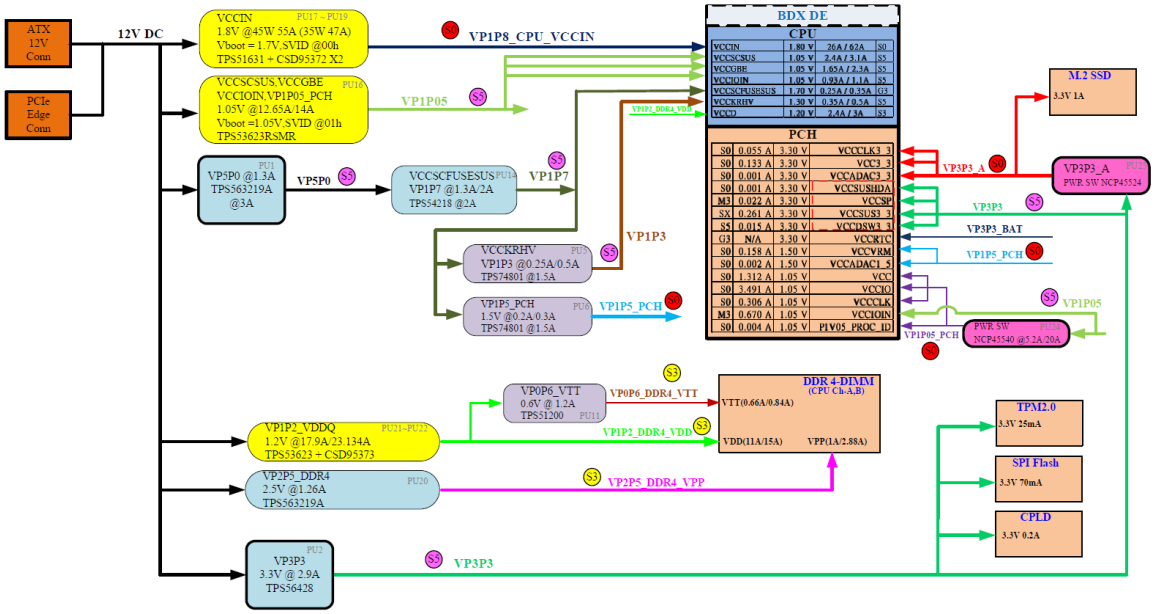

25MHZ XTAL
LAN_XTAL0
LAN_XTAL1
GBE_SPI_CLK
LAN EEPROM
DDR0_CLK
DDR1_CLK
DDR4 SO-DIMM
DDR4 SO-DIMM
CLKOUT_ITPXDP_P/N
100MHZ
XDP
CLKOUT_PEG_P/N
100MHZ
PCIe CONN
To MB
SPI_CLK
Flash
SRC_P/N0
SRC_P/N1
SRC_P/N2
SRC_P/N3
SRC_P/N4
SRC_P/N5
SRC_P/N6
SRC_P/N7
100MHZ
NC
LPC_CLK (SERIRQ)
33MHZ
PCILOOPBACK
25MHZ XTAL
XTAL0_25M
XTAL1_25M
PCI3
PCI0
PCI1
PCI2
PCI4
CY2304 BUFFER
33MHZ (LPC EDGE)
32.768K XTAL
RTCX1
RTCX2
LPC Debug CONN
SUSCLK_GPIO62
CPLD
SUSCLK
SSD
NC
NCSI_CLK_IN(50M)
FLEX
CLKOUTFLEX1_GP67
CLKOUTFLEX3_GP69
Broadwell-DE

Main board:

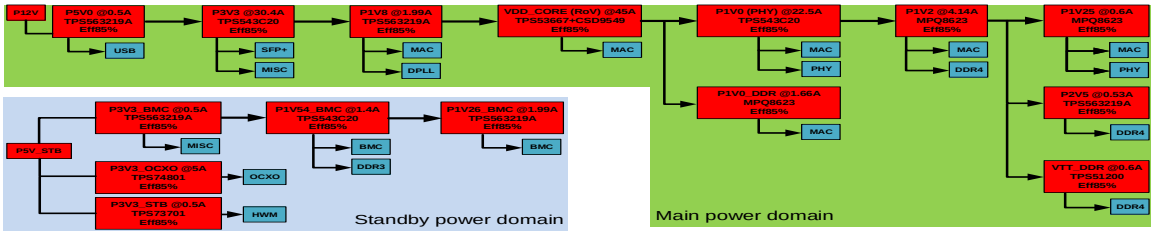


1.10 Power Tree

CPU Card

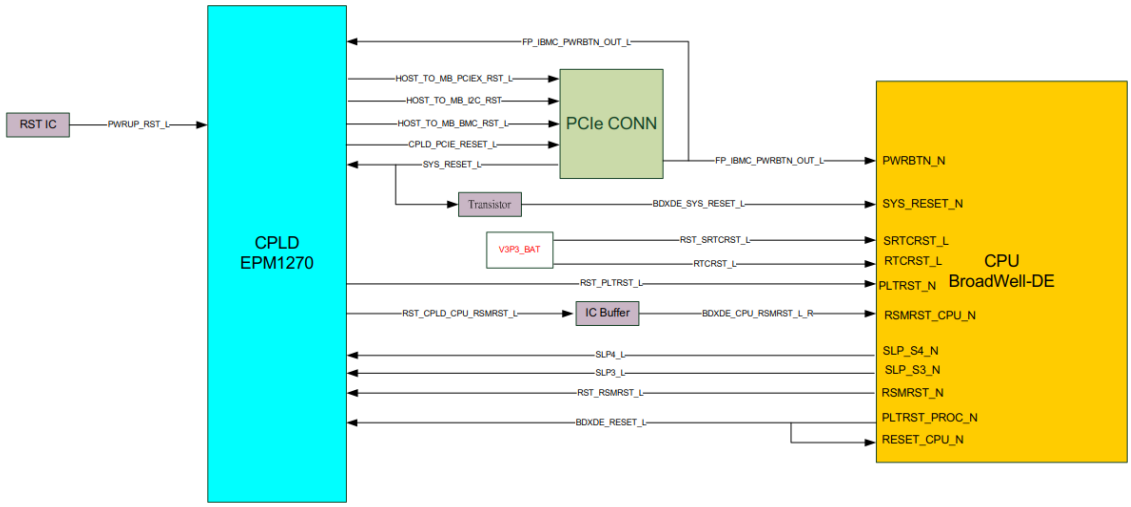


Main board:

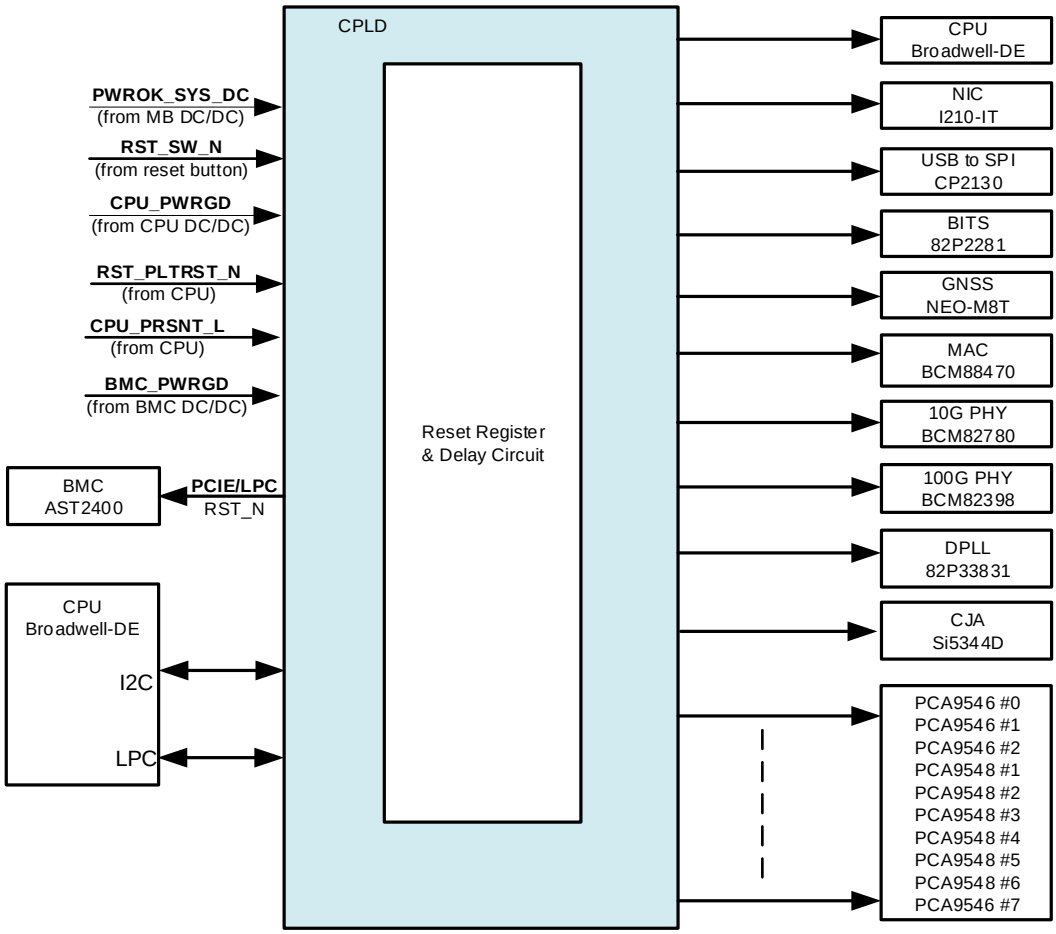


1.11 Reset Tree

CPU card

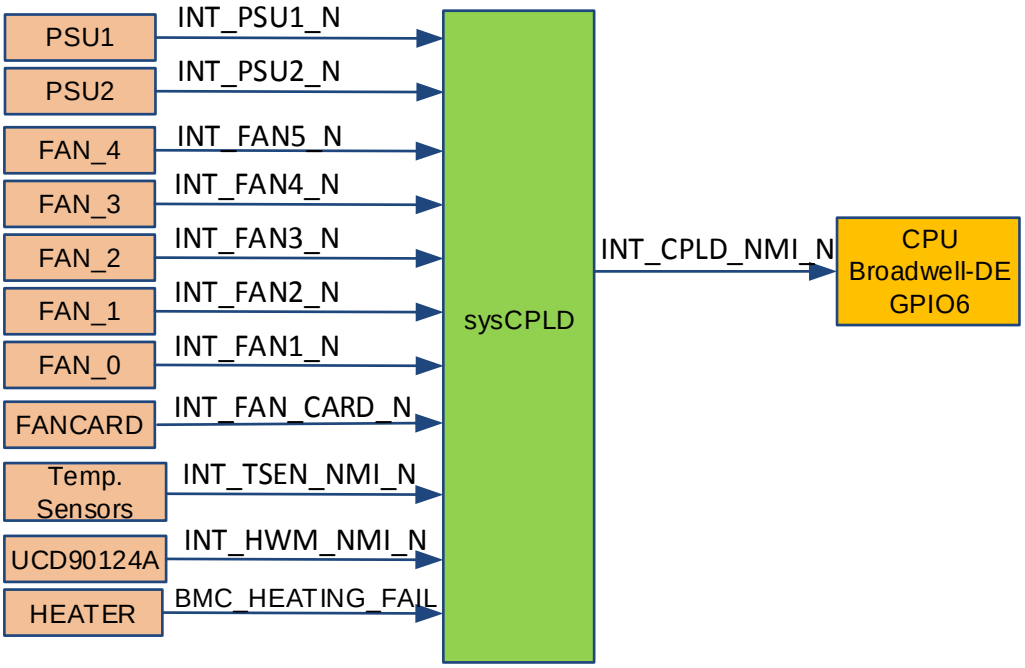


Main board



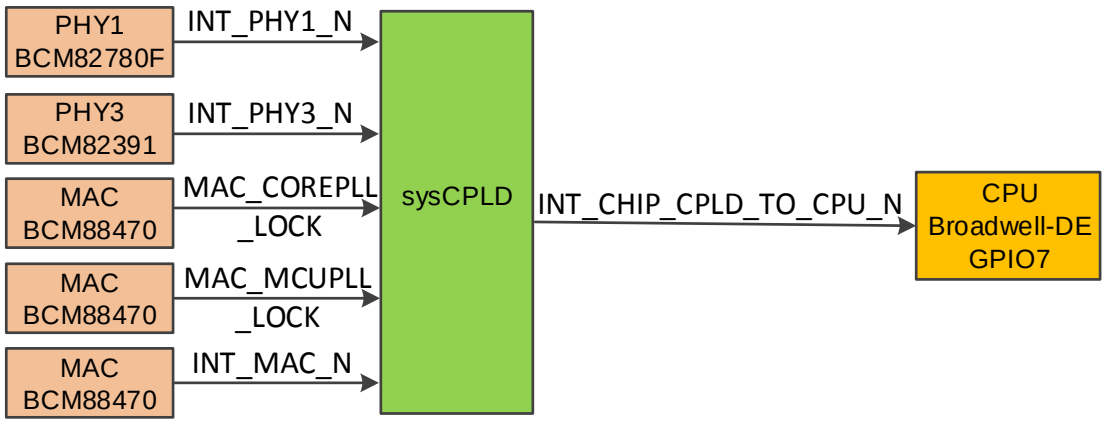
1.12 Interrupt Tree

1.12.1 Hardware Non-Maskable Interrupt



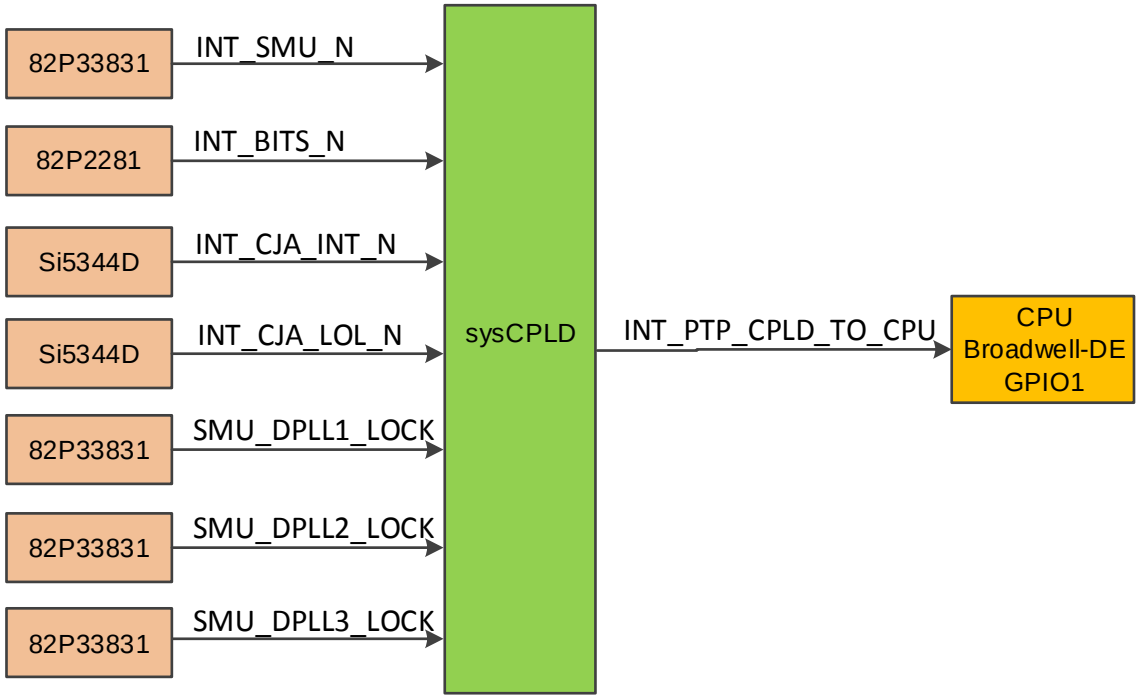
NMI Interrupt

1.12.2 Ethernet MAC/PHY Status Interrupt



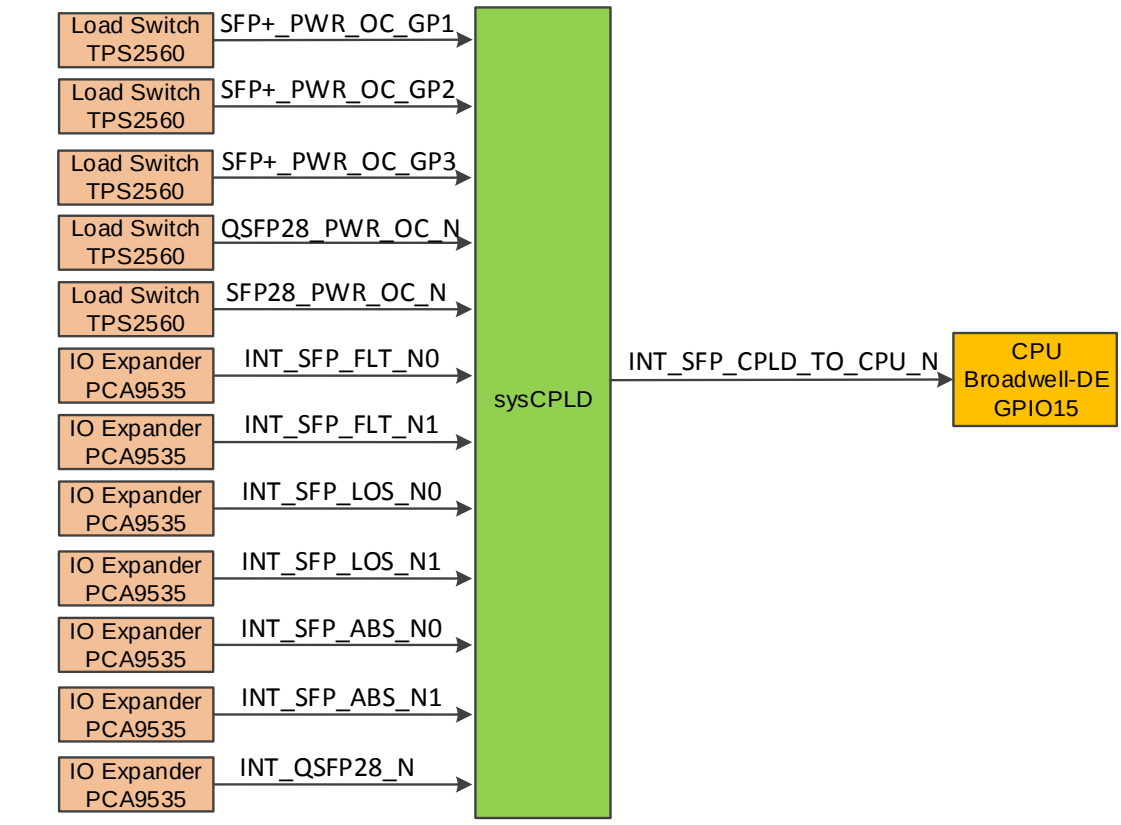
MAC &PHY Interrupt

1.12.3 SyncE and PTP Status Interrupt



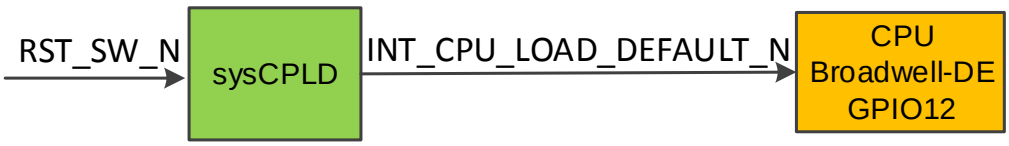
SyncE &PTP Interrupt

1.12.4 SFP+/QSFP28 Port Status Interrupt



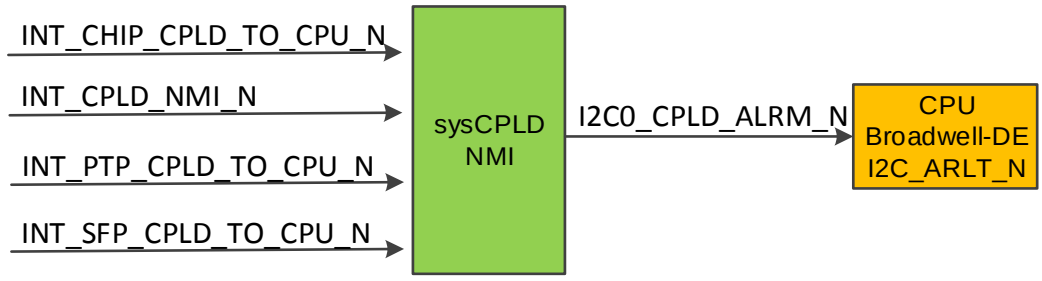
SFP Interrupt

1.12.5 Load Factory Default Interrupt



CPLD Alarm Interrupt

1.12.6 CPLD Alarm Interrupt



CPLD I2C Alarm Interrupt

2 Main System

This section describes in software view to access the system key interfaces in main system.

2.1 Memory and I/O Mapping

Fixed I/O ranges decoded by Broadwell-DE:

I/O Address	Read Target	Write Target	Internal Unit
00h-08h	DMA controller	DMA controller	DMA
09h-0Eh	reserved	DMA controller	DMA
0Fh	DMA controller	DMA controller	DMA
10h-18h	DMA controller	DMA controller	DMA
19h-1Eh	reserved	DMA controller	DMA
1Fh	DMA controller	DMA controller	DMA
20h-21h	Interrupt controller	Interrupt controller	interrupt
24h-25h	Interrupt controller	Interrupt controller	interrupt
28h-29h	Interrupt controller	Interrupt controller	interrupt
2Ch-2Dh	Interrupt controller	Interrupt controller	interrupt
2Eh-2Fh	LPC SIO	LPC SIO	Forwarded to LPC
30h-31h	Interrupt controller	Interrupt controller	interrupt
34h-35h	Interrupt controller	Interrupt controller	interrupt
38h-39h	Interrupt controller	Interrupt controller	interrupt
3Ch-3Dh	Interrupt controller	Interrupt controller	interrupt
40h-42h	Timer/Counter	Timer/Counter	PIT
43h	reserved	Timer/Counter	PIT
4Eh-4Fh	LPC SIO	LPC SIO	Forwarded to LPC
50h-52h	Timer/Counter	Timer/Counter	PIT
53h	reserved	Timer/Counter	PIT
60h	microcontroller	microcontroller	Forwarded to LPC
61h	NMI controller	NMI controller	Processor I/F
62h	microcontroller	microcontroller	Forwarded to LPC
64h	microcontroller	microcontroller	Forwarded to LPC
66h	microcontroller	microcontroller	Forwarded to LPC
70h	reserved	NMI and RTC controller	RTC
71h	RTC controller	RTC controller	RTC
72h	RTC controller	NMI and RTC controller	RTC
73h	RTC controller	RTC controller	RTC
74h	RTC controller	NMI and RTC controller	RTC
75h	RTC controller	RTC controller	RTC
76h	RTC controller	NMI and RTC controller	RTC
77h	RTC controller	RTC controller	RTC

80h	DMA controller, LPC, PCI or PCIe	DMA controller, LPC, PCI or PCIe	DMA
81h-83h	DMA controller	DMA controller	DMA
84h-86h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
87h	DMA controller	DMA controller	DMA
88h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
89h-8Bh	DMA controller	DMA controller	DMA
8Ch-8Eh	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
8Fh	DMA controller	DMA controller	DMA
90h-91h	DMA controller	DMA controller	DMA
92h	Reset generator	Reset generator	Processor I/F
93h-9Fh	DMA controller	DMA controller	DMA
A0h-A1h	Interrupt controller	Interrupt controller	interrupt
A4h-A5h	Interrupt controller	Interrupt controller	interrupt
A8h-A9h	Interrupt controller	Interrupt controller	interrupt
ACh-ADh	Interrupt controller	Interrupt controller	interrupt
B0h-B1h	Interrupt controller	Interrupt controller	interrupt
B2h-B3h	Power management	Power management	Power management
B4h-B5h	Interrupt controller	Interrupt controller	interrupt
B8h-B9h	Interrupt controller	Interrupt controller	interrupt
BCh-BDh	Interrupt controller	Interrupt controller	interrupt
C0h-D1h	DMA controller	DMA controller	DMA
D2h-DDh	reserved	DMA controller	DMA
DEh-DFh	DMA controller	DMA controller	DMA
F0h	Ferr#/interrupt controller	Ferr#/interrupt controller	Processor I/F

170h-177h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
1F0h-1F7h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
200h-207h	Gameport low	Gameport low	Forwarded to LPC
208h-20Fh	Gameport high	Gameport high	Forwarded to LPC
376h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
3F6h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
4D0h-4D1h	Interrupt controller	Interrupt controller	interrupt
CF9h	Reset generator	Reset generator	Processor I/F

Fixed I/O ranges decoded by Broadwell-DE:

Range name	Mappable	Size (bytes)	Target
ACPI	Anywhere in 64KB I/O space	6	Power management
IDE bus master	Anywhere in 64KB I/O space	1. 16 or 32 2. 16	1. SATA host controller #1, #2 2. IDE-R
Native IDE command	Anywhere in 64KB I/O space	8	1. SATA host controller #1, #2 2. IDE-R
Native IDE control	Anywhere in 64KB I/O space	4	1. SATA host controller #1, #2 2. IDE-R
SATA index/data pair	Anywhere in 64KB I/O space	1 6	1. SATA host controller #1, #2 2. IDE-R
SMBus	Anywhere in 64KB I/O space	3	SMB unit
TCO	96 bytes above ACPI base	3	TCO unit
GPIO	Anywhere in 64KB I/O space	128	GPIO unit
Parallel port	3 ranges in 64KB I/O space	8	LPC peripheral
Serial port 1	8 ranges in 64KB I/O space	8	LPC peripheral
Serial port 2	8 ranges in 64KB I/O space	8	LPC peripheral
Floppy disk controller	2 ranges in 64KB I/O space	8	LPC peripheral
LAN	Anywhere in 64KB I/O space	3	LAN unit
LPC generic 1	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 2	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 3	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 4	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
I/O trapping ranges	Anywhere in 64KB I/O space	1 to 256	Trap on backbone
PCI bridge	Anywhere in 64KB I/O space	I/O base/limit	PCI bridge
PCI-E root ports	Anywhere in 64KB I/O space	I/O base/limit	PCI-E root ports 1-8
KT	Anywhere in 64KB I/O space	8	KT

Memory decode ranges from processor perspective:

Memory range	target	Dependency/comments
0000 0000h-000D FFFFh 0010 0000h-TOM	Main memory	TOM registers in host controller
000E 0000h-000E FFFFh	LPC or SPI	Bit 6 in BIOS decode enable register is set
000F 0000h-000F FFFFh	LPC or SPI	Bit 7 in BIOS decode enable register is set
FEC_ _000h-FEC_ _040h	IOx APCI inside broadwell-de SoC	_ _ is controlled using APIC range select (ASEL) field and APIC enable (AEN) bit.
FEC1 0000h-FEC1 7FFFh	PCI-E port 1	PCI-E root port 1 I/OxAPIC enable (PAE) set
FEC1 8000h-FEC1 FFFFh	PCI-E port 2	PCI-E root port 2 I/OxAPIC enable (PAE) set
FEC2 0000h-FEC2 7FFFh	PCI-E port 3	PCI-E root port 3 I/OxAPIC enable (PAE) set
FEC2 8000h-FEC2 FFFFh	PCI-E port 4	PCI-E root port 4 I/OxAPIC enable (PAE) set
FEC3 0000h-FEC3 7FFFh	PCI-E port 5	PCI-E root port 5 I/OxAPIC enable (PAE) set
FEC3 8000h-FEC3 FFFFh	PCI-E port 6	PCI-E root port 6 I/OxAPIC enable (PAE) set
FEC4 0000h-FEC4 7FFFh	PCI-E port 7	PCI-E root port 7 I/OxAPIC enable (PAE) set
FEC4 8000h-FEC4 FFFFh	PCI-E port 8	PCI-E root port 8 I/OxAPIC enable (PAE) set
FFC0 0000h-FFC7 FFFFh	LPC or SPI (or PCI)	Bit 8 in BIOS decode enable register is set
FFC8 0000h-FFCF FFFFh	LPC or SPI (or PCI)	Bit 9 in BIOS decode enable register is set
FFD0 0000h-FFD7 FFFFh	LPC or SPI (or PCI)	Bit 10 in BIOS decode enable register is set
FFD8 0000h-FFDF FFFFh	LPC or SPI (or PCI)	Bit 11 in BIOS decode enable register is set
FFE0 0000h-FFE7 FFFFh	LPC or SPI (or PCI)	Bit 12 in BIOS decode enable register is set
FFE8 0000h-FFEF FFFFh	LPC or SPI (or PCI)	Bit 13 in BIOS decode enable register is set
FFF0 0000h-FFF7 FFFFh	LPC or SPI (or PCI)	Bit 14 in BIOS decode enable register is set
FFF8 0000h–FFFF FFFFh	LPC or SPI (or PCI)	Always enabled.
FF70 0000h–FF7F FFFFh	LPC or SPI (or PCI)	Bit 3 in BIOS Decode Enable register is set
FF60 0000h–FF6F FFFFh	LPC or SPI (or PCI)	Bit 2 in BIOS Decode Enable register is set
FF50 0000h–FF5F FFFFh	LPC or SPI (or PCI)	Bit 1 in BIOS Decode Enable register is set
FF40 0000h–FF4F FFFFh	LPC or SPI (or PCI)	Bit 0 in BIOS Decode Enable register is set
128 KB anywhere in 4 GB	Integrated LAN Controller	Enable using BAR in D25:F0
4 KB anywhere in 4 GB	Integrated LAN Controller	Enable using BAR in D25:F0
1 KB anywhere in 4 GB	USB EHCI Controller #1	Enable using standard PCI mechanism
64 KB anywhere in 4 GB	USB xHCI Controller	Enable using standard PCI mechanism
FED0 X000h–FED0 X3FFh	High Precision Event	BIOS determines “fixed” location which is
FED4 0000h–FED4 FFFFh	TPM on LPC	None
Memory Base/Limit	PCI Bridge	Enable using standard PCI mechanism
Prefetchable Memory	PCI Bridge	Enable using standard PCI mechanism
64 KB anywhere in 4 GB range	LPC	LPC Generic Memory Range. Enable using setting bit[0] of the LPC Generic
32 Bytes anywhere in 64-bit	SMBus	Enable using standard PCI mechanism
2 KB anywhere above 64 KB	SATA Host Controller #1	AHCI memory-mapped registers. Enable
Memory Base/Limit	PCI Express* Root Ports 1-	Enable using standard PCI mechanism
Prefetchable Memory	PCI Express Root Ports 1-8	Enable using standard PCI mechanism

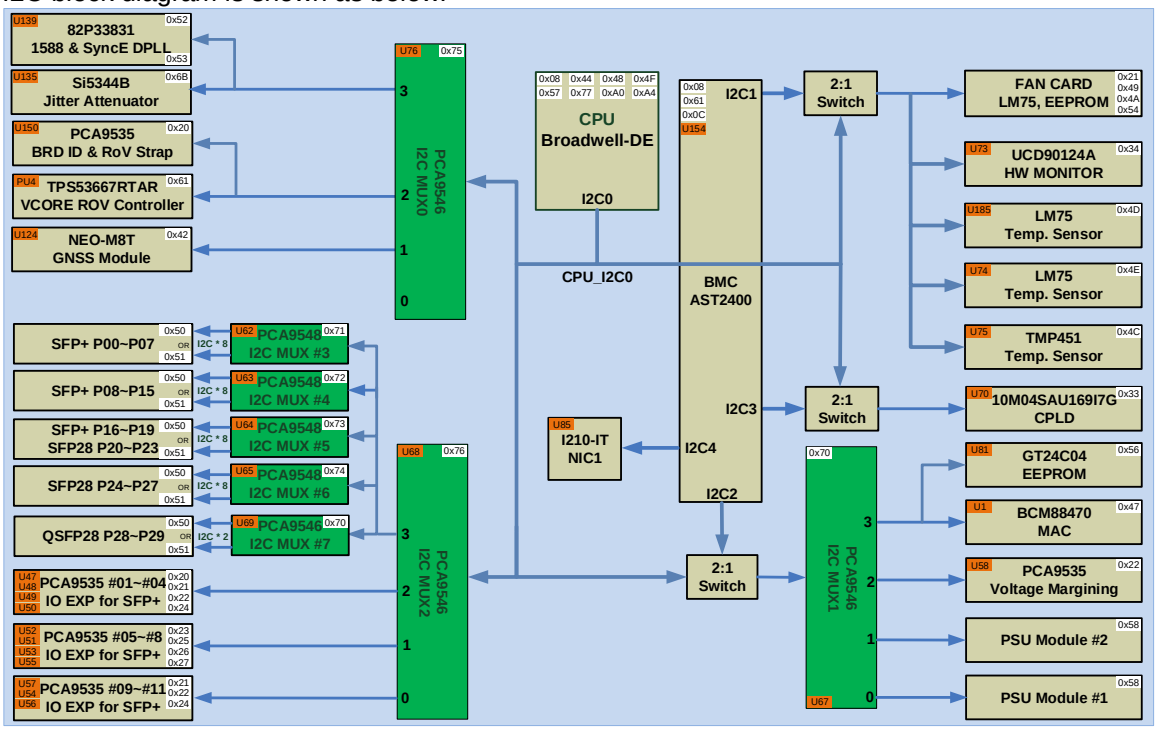
4 KB anywhere in 64-bit	Thermal Reporting	Enable using standard PCI mechanism
4 KB anywhere in 64-bit	Thermal Reporting	Enable using standard PCI mechanism
16 Bytes anywhere in 64-bit	Intel® MEI #1, #2	Enable using standard PCI mechanism
4 KB anywhere in 4 GB	KT	Enable using standard PCI mechanism
16 KB anywhere in 4 GB	Root Complex Register	Enable using setting bit[0] of the Root

2.2 SMbus

There is one SMbus, which is I2C compatible, on S9500-30XS controlled by CPU card. It is configured to operate in standard mode, 100KHz clock frequency. Four I2C buses from BMC are connected to switch board I2C devices with dedicated I2C muxs.

By default, some I2C components is designed to be accessed by CPU while others accessed by BMC, based on use case/access frequency. PTP components including GNSS module, DPLL, jitter attenuator and SFP+, QSFP28 ports are accessed by CPU, all other components are accessed by BMC. All I2C devices can be accessed by CPU or BMC, it can be done by enabling I2C mux.

I2C block diagram is shown as below:



Device address is summarized as below:

I2C Bus	I2C Mux Level 1	I2C Mux Level 2	Location	Device	Bit # / Channel #	I/O	Address <7:1> (7-bits)		Function
I2C Bus #0	I2C Mux #1 PCA9546	Channel 4	MAC	BCM88470			1000111	0x47	MAC register access and control
			EEPROM	GT24C04			1010001	0x56	SKU ID and build info. access
		Channel 3	IO EXP#1	PCA9535			0100000	0x20	Voltage high/Low Margin (for design verification & manufacturing test only)

	Channel 2	PSU #1	PSU			0100000	0x50 0x58	PSU EEPROM info. Access PSU MCU slave Address
	Channel 1	PSU #2	PSU			0100000	0x50 0x58	PSU EEPROM info. Access PSU MCU slave Address
I2C Mux #0 PCA9546	Channel 3	PTP DPLL	82P33831			101 0111	0x52 0x53	PTP & SyncE DPLL register access & control
		Jitter Attenuator	Si5344D			110 1011	0x6B	Jitter Attenuator register access & control
	Channel 2	IO EXP#0	PCA9535			010 0000	0x20	Board ID, Build version,, HW version
		MAC RoV	TPS53667			110 0001	0x61	Vcore voltage level adjust
	Channel 1	GNSS Module	NEO-M8T-0			100 0010	0x42	GNSS Module control
/	/	MB Temp. sensor	LM75			100 1101	0x4D	Switch board temperature sensor
/	/	MB Temp. sensor	LM75			100 1110	0x4E	Switch board temperature sensor
/	/	MB Temp. sensor	TMP451			100 1100	0x4C	Switch board temperature sensor
/	/	HWM	UCD90124A			011 0100	0x34	HWM power, FAN and thermal info, access
/	/	FAN Temp. sensor	LM75			100 1001	0x49	FAN board temperature sensor
/	/	FAN Temp. sensor	LM75			100 1010	0x4A	FAN board temperature sensor
/	/	FAN IO EXP#0	PCA9535			010 0001	0x21	Reserved
/	/	FAN EEPROM	GT24C04			101 0100	0x54	Reserved
/	/	CPLD	10M02SCU			011 0011	0x33	CPLD/FPGA register access & control
I2C Mux #2 PCA9546 Channel 1		IO Expander #2	PCA9535	I/O0.7	Out	0100010x	0x22	SFP+_P00_TX_DIS
				I/O0.6	Out			SFP+_P01_TX_DIS
				I/O0.5	Out			SFP+_P02_TX_DIS
				I/O0.4	Out			SFP+_P03_TX_DIS
				I/O0.3	Out			SFP+_P04_TX_DIS
				I/O0.2	Out			SFP+_P05_TX_DIS
				I/O0.1	Out			SFP+_P06_TX_DIS
				I/O0.0	Out			SFP+_P07_TX_DIS
				I/O1.7	Out			SFP+_P08_TX_DIS
				I/O1.6	Out			SFP+_P09_TX_DIS
				I/O1.5	Out			SFP+_P10_TX_DIS
				I/O1.4	Out			SFP+_P11_TX_DIS
				I/O1.3	Out			SFP+_P12_TX_DIS
				I/O1.2	Out			SFP+_P13_TX_DIS
				I/O1.1	Out			SFP+_P14_TX_DIS
				I/O1.0	Out			SFP+_P15_TX_DIS
		IO Expander #3	PCA9535	I/O0.7	Out	0100010x	0x24	SFP+_P16_TX_DIS
				I/O0.6	Out			SFP+_P17_TX_DIS

				I/O0.5	Out			SFP+_P18_TX_DIS
				I/O0.4	Out			SFP+_P19_TX_DIS
				I/O0.3	Out			SFP+_P20_TX_DIS
				I/O0.2	Out			SFP+_P21_TX_DIS
				I/O0.1	Out			SFP+_P22_TX_DIS
				I/O0.0	Out			SFP+_P23_TX_DIS
				I/O1.7	Out			SFP+_P24_TX_DIS
				I/O1.6	Out			SFP+_P25_TX_DIS
				I/O1.5	Out			SFP+_P26_TX_DIS
				I/O1.4	Out			SFP+_P27_TX_DIS
				I/O1.3	Out			NC
				I/O1.2	Out			NC
				I/O1.1	Out			NC
				I/O1.0	Out			NC
		IO Expander #4	PCA9535	I/O0.0	Out	0100001x	0x21	QSFP28_P1_INT_N
				I/O0.1	Out			QSFP28_P0_INT_N
				I/O0.2	Out			NC
				I/O0.3	Out			NC
				I/O0.4	Out			QSFP28_P1_PRSNT_N
				I/O0.5	Out			QSFP28_P0_PRSNT_N
				I/O0.6	Out			NC
				I/O0.7	Out			NC
				I/O1.0	Out			QSFP28_P1_LPMODE
				I/O1.1	Out			QSFP28_P0_LPMODE
				I/O1.2	Out			NC
				I/O1.3	Out			NC
				I/O1.4	Out			QSFP28_P1_RST_N
				I/O1.5	Out			QSFP28_P0_RST_N
				I/O1.6	Out			NC
				I/O1.7	Out			NC
	I2C Mux #3 PCA9546 Channel 2	IO Expander #5	PCA9535	I/O0.7	Out	0100101x	0x25	SFP+_P00_RATE_SEL
				I/O0.6	Out			SFP+_P01_RATE_SEL
				I/O0.5	Out			SFP+_P02_RATE_SEL
				I/O0.4	Out			SFP+_P03_RATE_SEL
				I/O0.3	Out			SFP+_P04_RATE_SEL

					I/O0.2	Out			SFP+_P05_RATE_SEL
					I/O0.1	Out			SFP+_P06_RATE_SEL
					I/O0.0	Out			SFP+_P07_RATE_SEL
					I/O1.7	Out			SFP+_P08_RATE_SEL
					I/O1.6	Out			SFP+_P09_RATE_SEL
					I/O1.5	Out			SFP+_P10_RATE_SEL
					I/O1.4	Out			SFP+_P11_RATE_SEL
					I/O1.3	Out			SFP+_P12_RATE_SEL
					I/O1.2	Out			SFP+_P13_RATE_SEL
					I/O1.1	Out			SFP+_P14_RATE_SEL
					I/O1.0	Out			SFP+_P15_RATE_SEL
			IO Expander #6	PCA9535	I/O0.7	In	0100110x	0x26	SFP+_P00_TX_FLT
					I/O0.6	In			SFP+_P01_TX_FLT
					I/O0.5	In			SFP+_P02_TX_FLT
					I/O0.4	In			SFP+_P03_TX_FLT
					I/O0.3	In			SFP+_P04_TX_FLT
					I/O0.2	In			SFP+_P05_TX_FLT
					I/O0.1	In			SFP+_P06_TX_FLT
					I/O0.0	In			SFP+_P07_TX_FLT
					I/O1.7	In			SFP+_P08_TX_FLT
					I/O1.6	In			SFP+_P09_TX_FLT
					I/O1.5	In			SFP+_P10_TX_FLT
					I/O1.4	In			SFP+_P11_TX_FLT
					I/O1.3	In			SFP+_P12_TX_FLT
					I/O1.2	In			SFP+_P13_TX_FLT
					I/O1.1	In			SFP+_P14_TX_FLT
					I/O1.0	In			SFP+_P15_TX_FLT
			IO Expander #7	PCA9535	I/O0.7	In	0100111x	0x27	SFP+_P16_TX_FLT
					I/O0.6	In			SFP+_P17_TX_FLT
					I/O0.5	In			SFP+_P18_TX_FLT
					I/O0.4	In			SFP+_P19_TX_FLT
					I/O0.3	In			SFP+_P20_TX_FLT
					I/O0.2	In			SFP+_P21_TX_FLT
					I/O0.1	In			SFP+_P22_TX_FLT
					I/O0.0	In			SFP+_P23_TX_FLT

				I/O1.7	In			SFP+_P24_TX_FLT
				I/O1.6	In			SFP+_P25_TX_FLT
				I/O1.5	In			SFP+_P26_TX_FLT
				I/O1.4	In			SFP+_P27_TX_FLT
				I/O1.3	In			NC
				I/O1.2	In			NC
				I/O1.1	In			NC
				I/O1.0	In			NC
		IO Expander #8	PCA9535	I/O0.7	Out	0100 001x	0x23	SFP+_P16_RATE_SEL
				I/O0.6	Out			SFP+_P17_RATE_SEL
				I/O0.5	Out			SFP+_P18_RATE_SEL
				I/O0.4	Out			SFP+_P19_RATE_SEL
				I/O0.3	Out			SFP+_P20_RATE_SEL
				I/O0.2	Out			SFP+_P21_RATE_SEL
				I/O0.1	Out			SFP+_P22_RATE_SEL
				I/O0.0	Out			SFP+_P23_RATE_SEL
	I2C Mux #4 PCA9546 Channel 3			I/O1.7	Out			SFP+_P24_RATE_SEL
				I/O1.6	Out			SFP+_P25_RATE_SEL
				I/O1.5	Out			SFP+_P26_RATE_SEL
				I/O1.4	Out			SFP+_P27_RATE_SEL
				I/O1.3	Out			NC
				I/O1.2	Out			NC
				I/O1.1	Out			NC
				I/O1.0	Out			NC
		IO Expander #9	PCA9535	I/O0.7	In	0100100x	0x24	SFP+_P16_RX_LOS
				I/O0.6	In			SFP+_P17_RX_LOS
				I/O0.5	In			SFP+_P18_RX_LOS
				I/O0.4	In			SFP+_P19_RX_LOS
				I/O0.3	In			SFP+_P20_RX_LOS
				I/O0.2	In			SFP+_P21_RX_LOS
				I/O0.1	In			SFP+_P22_RX_LOS
				I/O0.0	In			SFP+_P23_RX_LOS
				I/O1.7	In			SFP+_P24_RX_LOS
				I/O1.6	In			SFP+_P25_RX_LOS
				I/O1.5	In			SFP+_P26_RX_LOS

					I/O1.4	In			SFP+_P27_RX_LOS
					I/O1.3	In			NC
					I/O1.2	In			NC
					I/O1.1	In			NC
					I/O1.0	In			NC
			IO Expander #10	PCA9535	I/O0.7	In	0100000x	0x20	SFP+_P00_MOD_ABS
					I/O0.6	In			SFP+_P01_MOD_ABS
					I/O0.5	In			SFP+_P02_MOD_ABS
					I/O0.4	In			SFP+_P03_MOD_ABS
					I/O0.3	In			SFP+_P04_MOD_ABS
					I/O0.2	In			SFP+_P05_MOD_ABS
					I/O0.1	In			SFP+_P06_MOD_ABS
					I/O0.0	In			SFP+_P07_MOD_ABS
					I/O1.7	In			SFP+_P08_MOD_ABS
					I/O1.6	In			SFP+_P09_MOD_ABS
					I/O1.5	In			SFP+_P10_MOD_ABS
					I/O1.4	In			SFP+_P11_MOD_ABS
					I/O1.3	In			SFP+_P12_MOD_ABS
					I/O1.2	In			SFP+_P13_MOD_ABS
					I/O1.1	In			SFP+_P14_MOD_ABS
					I/O1.0	In			SFP+_P15_MOD_ABS
			IO Expander #11	PCA9535	I/O0.7	In	0100100x	0x22	SFP+_P16_MOD_ABS
					I/O0.6	In			SFP+_P17_MOD_ABS
					I/O0.5	In			SFP+_P18_MOD_ABS
					I/O0.4	In			SFP+_P19_MOD_ABS
					I/O0.3	In			SFP+_P20_MOD_ABS
					I/O0.2	In			SFP+_P21_MOD_ABS
					I/O0.1	In			SFP+_P22_MOD_ABS
					I/O0.0	In			SFP+_P23_MOD_ABS
					I/O1.7	In			SFP+_P24_MOD_ABS
					I/O1.6	In			SFP+_P25_MOD_ABS
					I/O1.5	In			SFP+_P26_MOD_ABS
					I/O1.4	In			SFP+_P27_MOD_ABS
					I/O1.3	In			NC
					I/O1.2	In			NC

				I/O1.1	In			NC
				I/O1.0	In			NC
		IO Expander #12	PCA9535	I/O0.7	In	0100001x	0x21	SFP+_P00_RX_LOS
				I/O0.6	In			SFP+_P01_RX_LOS
				I/O0.5	In			SFP+_P02_RX_LOS
				I/O0.4	In			SFP+_P03_RX_LOS
				I/O0.3	In			SFP+_P04_RX_LOS
				I/O0.2	In			SFP+_P05_RX_LOS
				I/O0.1	In			SFP+_P06_RX_LOS
				I/O0.0	In			SFP+_P07_RX_LOS
				I/O1.7	In			SFP+_P08_RX_LOS
				I/O1.6	In			SFP+_P09_RX_LOS
				I/O1.5	In			SFP+_P10_RX_LOS
				I/O1.4	In			SFP+_P11_RX_LOS
				I/O1.3	In			SFP+_P12_RX_LOS
				I/O1.2	In			SFP+_P13_RX_LOS
				I/O1.1	In			SFP+_P14_RX_LOS
				I/O1.0	In			SFP+_P15_RX_LOS
I2C Mux #5 PCA9546 Channel 4	I2C Mux #6 PCA9548	SFP+ Port 1	EEPROM	Channel 1	I/O	1010.000x	0x50	SFP+ Port 0 EEPROM access
		SFP+ Port 2	EEPROM	Channel 2	I/O	1010.000x	0x50	SFP+ Port 1 EEPROM access
		SFP+ Port 3	EEPROM	Channel 3	I/O	1010.000x	0x50	SFP+ Port 2 EEPROM access
		SFP+ Port 4	EEPROM	Channel 4	I/O	1010.000x	0x50	SFP+ Port 3 EEPROM access
		SFP+ Port 5	EEPROM	Channel 5	I/O	1010.000x	0x50	SFP+ Port 4 EEPROM access
		SFP+ Port 6	EEPROM	Channel 6	I/O	1010.000x	0x50	SFP+ Port 5 EEPROM access
		SFP+ Port 7	EEPROM	Channel 7	I/O	1010.000x	0x50	SFP+ Port 6 EEPROM access
		SFP+ Port 8	EEPROM	Channel 8	I/O	1010.000x	0x50	SFP+ Port 7 EEPROM access
	I2C Mux #7 PCA9548	SFP+ Port 9	EEPROM	Channel 1	I/O	1010.000x	0x50	SFP+ Port 8 EEPROM access
		SFP+ Port 10	EEPROM	Channel 2	I/O	1010.000x	0x50	SFP+ Port 9 EEPROM access
		SFP+ Port 11	EEPROM	Channel 3	I/O	1010.000x	0x50	SFP+ Port 10 EEPROM access
		SFP+ Port 12	EEPROM	Channel 4	I/O	1010.000x	0x50	SFP+ Port 11 EEPROM access
		SFP+ Port 13	EEPROM	Channel 5	I/O	1010.000x	0x50	SFP+ Port 12 EEPROM access
		SFP+ Port 14	EEPROM	Channel 6	I/O	1010.000x	0x50	SFP+ Port 13 EEPROM access
		SFP+ Port 15	EEPROM	Channel 7	I/O	1010.000x	0x50	SFP+ Port 14 EEPROM access
		SFP+ Port 16	EEPROM	Channel 8	I/O	1010.000x	0x50	SFP+ Port 15 EEPROM access

		I2C Mux #8 PCA9548	SFP+ Port 17	EEPROM	Channel 1	I/O	1010.000x	0x50	SFP+ Port 16 EEPROM access
			SFP+ Port 18	EEPROM	Channel 2	I/O	1010.000x	0x50	SFP+ Port 17 EEPROM access
			SFP+ Port 19	EEPROM	Channel 3	I/O	1010.000x	0x50	SFP+ Port 18 EEPROM access
			SFP+ Port 20	EEPROM	Channel 4	I/O	1010.000x	0x50	SFP+ Port 19 EEPROM access
			SFP+ Port 21	EEPROM	Channel 5	I/O	1010.000x	0x50	SFP+ Port 20 EEPROM access
			SFP+ Port 22	EEPROM	Channel 6	I/O	1010.000x	0x50	SFP+ Port 21 EEPROM access
			SFP+ Port 23	EEPROM	Channel 7	I/O	1010.000x	0x50	SFP+ Port 22 EEPROM access
			SFP+ Port 24	EEPROM	Channel 8	I/O	1010.000x	0x50	SFP+ Port 23 EEPROM access
		I2C Mux #6 PCA9548	SFP+ Port 25	EEPROM	Channel 1	I/O	1010.000x	0x50	SFP+ Port 24 EEPROM access
			SFP+ Port 26	EEPROM	Channel 2	I/O	1010.000x	0x50	SFP+ Port 25 EEPROM access
			SFP+ Port 27	EEPROM	Channel 3	I/O	1010.000x	0x50	SFP+ Port 26 EEPROM access
			SFP+ Port 28	EEPROM	Channel 4	I/O	1010.000x	0x50	SFP+ Port 27 EEPROM access
		I2C Mux #9 PCA9546	QSFP28 Port 0	EEPROM	Channel 4	I/O	1010.000x	0x50	QSFP28 Port 0 EEPROM access
			QSFP28 Port 1	EEPROM	Channel 3	I/O	1010.000x	0x50	QSFP28 Port 1 EEPROM access

2.3 GPIO

- GPIO configuration:
  - GPIO base address : Bus 0 Dev 1F Fun 0 offset 0x48-0x4B[15:7]
  - GPIO region size : 0x7F

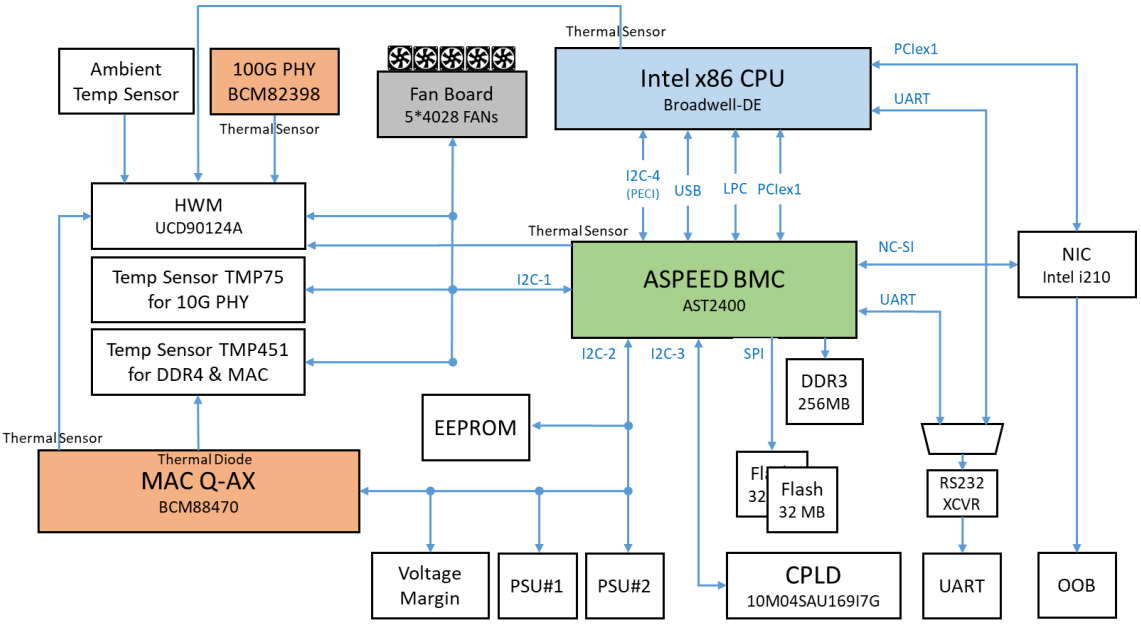
GPIO#	Signal	Description	BIOS default configuration
0	PU_BMBUSY_N_GPIO0	Not used	GPO_LOW
1	INT2_PCH_GPIO1_N	INT to CPU from Main CPLD	GPI
2	CPLD_PIRQE_L_GPIO2	PIRQE from CPU CPLD	GPI
3	CPLD_PIRQF_L_GPIO3	PIRQF from CPU CPLD	GPI
4	CPLD_PIRQG_L_GPIO4	PIRQG from CPU CPLD	GPI
5	CPLD_PIRQH_L_GPIO5	PIRQH from CPU CPLD	GPI
6	INT0_PCH_GPIO6_N	INT to CPU from Main CPLD	GPI
7	INT1_PCH_GPIO7_N	INT to CPU from Main CPLD	GPI
8	GPIO8_OCS	Not used	GPO_LOW
9	OC5_N_GPIO9	Not used	GPO_LOW
10	OC6_N_GPIO10	Not used	GPO_LOW
11	MB_HOST_3V3SB_ALERT_L	SMB alert	Native
12	INT3_PCH_GPIO12_N	INT to CPU from Main CPLD	GPI
13			

14	OC7_N_GPIO14	Not used	GPO_LOW
15	INT4_PCH_GPIO15_N	INT to CPU from Main CPLD	GPI
16	CPU_THROTTLE_L	CPU_THROTTLE_L to CPLD	GPO_HIGH
17	INT_TPM_N	INT from TPM	GPI
18	SRC1CLKRQ_N_GPIO18	Not used	GPO_LOW
19	RST_PCIE_PCH_N_GPIO19	HW Strap Boot BIOS Strap	GPO_LOW
20	SMI_ACTIVE_L	SMI_ACTIVE_L	GPO_HIGH
21	SATA0GP_GPIO21	Not used	GPO_LOW
22	SCLOCK_GPIO22	Not used	GPO_LOW
23	LDRQ1_N_GPIO23	Not used	GPO_LOW
24	H_EDGE_FAST_PROCHOT_L	H_EDGE_FAST_PROCHOT_L	GPO_HIGH
25	GPIO25	Not used	GPO_LOW
26	GPIO26	JTAG_TCK	GPO_HIGH
27	CPLD_GPIO27_MGPIO6	GPIO to CPU from CPU CPLD	GPI
28	BDXDE_ME_DRIVE_L	GPIO from CPU to CPU CPLD	GPO_HIGH
29	H_BDXDE_PROCHOT_DISABLE	H_BDXDE_PROCHOT_DISABLE	GPO_LOW
30	SUS_WARN_L	Not used	GPO_LOW
31	SMB_INA230_ALRT_PROCHOT_L	SMB_INA230_ALRT_PROCHOT_L	GPO_HIGH
32	MANUFACTURING_DET_L	Not used	GPO_LOW
33	PD_DMI_TERMINATION_GPIO33	HW Strap for DMI RX terminated	GPO_LOW
34			
35	NMI_EVENT_L	NMI_EVENT_L	Native
36	BIOS_ADV_FUNCTIONS_GPIO36	HW Strap DMMI TX terminated	GPO_LOW
37	ADR_TRIGGER_L_GPIO37	HW Strap Intel ME security	GPO_LOW
38	SLOAD_GPIO38	Not used	GPO_LOW
39	SDATAOUT0_GPIO39	Not used	GPO_LOW
40	OC1_N_GPIO40	Not used	GPO_LOW
41	OC2_N_GPIO41	Not used	GPO_LOW
42	OC3_N_GPIO42	Not used	GPO_LOW
43	OC4_N_GPIO43	Not used	GPO_LOW
44	JTAG_TDO	JTAG_TDO	GPI
45	JTAG_TDI	JTAG_TDI	GPI

46	JTAG_TMS	JTAG_TMS	GPI
47			
48	SDATAOUT1_GPIO48	Not used	GPO_LOW
49	SATA5GP_GPIO49	Not used	GPO_LOW
50	RST_TPM_N	Not used	GPO_HIGH
51	PU_GPIO51_GSXDOUT	HW Strap Boot BIOS Strap	GPO_LOW
52	PD_GPIO52_CPUSV	HW Strap	GPO_LOW
53	PD_GPIO53_GSXDIN	HW Strap DMI AC/DC coupling	GPO_LOW
54	TP_GPIO_54	CPU_BOOT_DONE	GPO_LOW
55	BIOS_RCVR_BOOT_L	HW Strap BIOS top block swap	GPI
56			
57	ME_RCVR_L	HW Strap ME FW update	Control by ME MGPIO5
58	SML1CLK_GPIO58_MGPIO11	Not used	GPO_LOW
59	OC0_N_GPIO59	Not used	GPO_LOW
60	SMB_SMLINK0_3V3SB_ALRT	SMLink0 alert	Native
61	SUS_STAT_N_GPIO61	Not used	GPO_LOW
62	CLK_M2_SUSCLK_ST	CLK_M2_SUSCLK_ST	Native
63			
64			
65	CLKOUTFLEX1_GPIO65	Not used	GPO_LOW
66			
67	CLKOUTFLEX3_GPIO67	Not used	GPO_LOW
68	TP_TACH_GPIO_68	Not used	GPO_LOW
69	TP_TACH_GPIO_69	Not used	GPO_LOW
70	TACH6_GPIO70	Not used	GPO_LOW
71	TACH7_GPIO71	Not used	GPO_LOW
72	GPIO72	Not used	GPO_LOW
73			
74	PCH_HOT_L	PCH_HOT_L	Native
75	SMB_SMLINK1_3V3SB_DAT	Not used	GPO_LOW

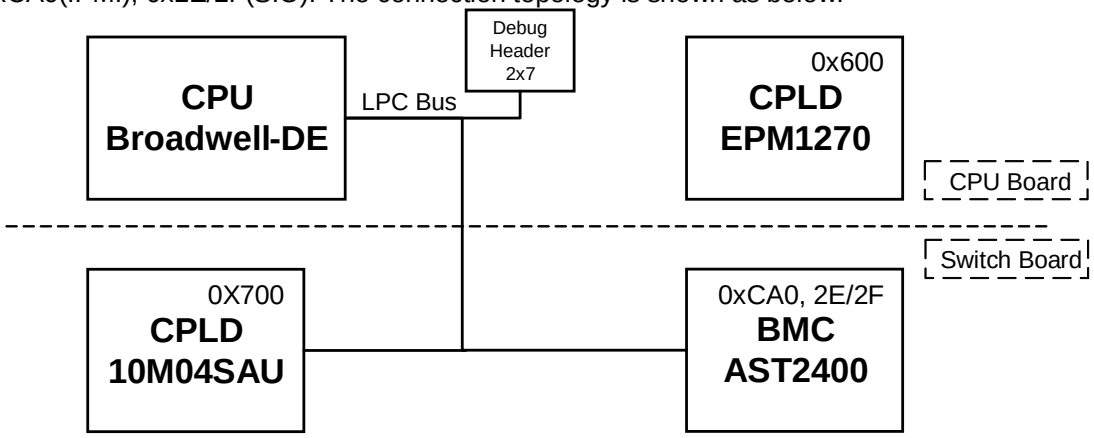
3 BMC Sub-system

In S9500-30XS switch, baseboard management controller (BMC) autonomous monitors system's health including temperature, voltage, fan speed, etc.



3.1 LPC

Low-pin-count interface is an important interface for communication among Broadwell-DE,CPLD and BMC. The OS running in x86 use this interface to communicate with BMC's IPMI message handler. LPC base address for CPU CPLD is 0x600, for MB CPLD is 0x700, for BMC is 0xCA0(IPMI), 0x2E/2F(SIO). The connection topology is shown as below.



3.2 GPIO

AST2400 Integrates one set of Parallel GPIO Controller with maximum 216 control pins, which are 28 sets, to provide general-purpose input/output functions. All functional parallel GPIOs of S9500-30XS switch in different group are listed as below, net names ended with '_N' means this signal is active low, otherwise it's active high or it's a mux select pin.

Group	Ball Name	Net Name	Direction	Function
GPIOA	GPIOA5	INT_VCORE_ALRT_N	Input	Interrupt get from MAC Vcore
	GPIOA6	RST_I2C_MUX1_N	Output / Input	PSU I2C Mux reset control. Pull high only when PWROK_SYS_DC=0
GPIOC	GPIOC0	CPU_ME_RCVR_L	Input	CPU ME recovery request
	GPIOC1	CPU_PROCHOT_L	Input	CPU hot monitor
	GPIOC2	CPU_CATERR_L	Input	CPU CAT error monitor
	GPIOC3	CPU_THERMTRIP_L	Input	CPU thermal trip monitor
	GPIOC4	INT_CPU_TO_BMC_N	Input	Interrupt get from CPU
	GPIOC5	INT_TSEN_NMI_N	Input	Interrupt get from thermal sensor
	GPIOC6	INT_NMI_CPLD_TO_BMC_N	Input	NMI interrupt from CPLD
	GPIOC7	INT_BMC_LOAD_DEFAULT_N	Input	BMC firmware/pass word load factory default request
GPIOE	GPIOE0	RST_SW_TO_CP2104	Output	Micro USB console reset control
	GPIOE1	BMC_UART_MUX_SEL	Output	Force console port switch to CPU
	GPIOE3	PWROK_SYS_DC	Input	Switching system Power OK
	GPIOE6	CPU_BOOT_DONE	Input	CPU boot done indication
	GPIOE7	CPU_TO_BMC_PWRGD	Input	CPU system Power OK
GPIOF	GPIOF1	FAN45_TACH_SW	Output	FAN4 or 5 TACH switching when FANs are controlled by HWM High: FAN4, Low: FAN5
	GPIOF2	FAN_BMC_CNTRL	Output	FAN control by BMC or HWM High: BMC, Low: HWM
	GPIOF4	RST_BMC_TO_RTC	Output	CPU RTC reset control
	GPIOF5	CPLD_CONFIG_SEL	Output	CPLD boot block select High: Block 1, Low: Block 0
GPIOK	GPIOK0	RTC_BAT_SENSE_EN_N	Output	RTC Vbat sense enable
	GPIOK1	INT_VCORE_VR_FAULT_N	Input	Interrupt when MAC Vcore fault
	GPIOK2	CPU_PRSNT_L	Input	CPU card presence signal
	GPIOK3	PSU_THERM_SHTDN_DIS_N	Output	Disable PSU shutdown system when over temperature
	GPIOK4	RST_CPU_PWRBTN_N	Output	CPU system power button control
	GPIOK5	INT_BMC_TO_CPU_N	Output	Interrupt from BMC to CPU
	GPIOK6	PSU1_PRSNT_N	Input	PSU#1 presence signal
	GPIOK7	PSU2_PRSNT_N	Input	PSU#2 presence signal
GPIOM	GPIOM3	PSU1_EEPROM_WP	Output	PSU#1 EEPROM write protect
	GPIOM4	PSU2_EEPROM_WP	Output	PSU#2 EEPROM write protect
	GPIOM5	I2C_CPLD_MUX_SEL	Output	CPLD I2C tied to CPU or BMC High: CPU, Low: BMC
	GPIOM6	BMC_USB_MUX_SEL	Output	Front panel USB port connected to CPU or BMC High: BMC, Low: CPU
	GPIOM7	I2C_HWM_CNTRL	Output	UCD90124A PMBus control output
GPION	GPION5	VMG_BMC_HEATER_EN	Output	Enable BMC handoff heater control
	GPION6	VMG_BMC_HEATER_LOW_BMC	Output	Heater Margin Low control
	GPION7	VMG_BMC_HEATER_HIGH_BMC	Output	Heater Margin High control
GPIOO	GPIOO0	HWM_FAN4_PRSNT_N	Input	FAN#4 Present signal
	GPIOO2	HWM_FAN3_PRSNT_N	Input	FAN#3 Present signal
	GPIOO4	HWM_FAN2_PRSNT_N	Input	FAN#2 Present signal
	GPIOO6	HWM_FAN1_PRSNT_N	Input	FAN#1 Present signal
GPIOP	GPIOP0	HWM_FAN0_PRSNT_N	Input	FAN#0 Present signal
	GPIOP2	PSU0_PWRON_N	Output	PSU#1 Power On control

	GPIOP3	PSU1_PWRON_N	Output	PSU#2 Power On control
	GPIOP4	PSU0_PWROK	Input	PSU#1 Power OK signal
	GPIOP5	PSU1_PWROK	Input	PSU#2 Power OK signal
GPIOQ	GPIOQ4	RST_BMC_TO_CPU_N	Output	Reset from BMC to CPU
	GPIOQ5	NMI_BMC_TO_CPU_N	Output	NMI interrupt from BMC to CPU
	GPIOQ6	INT_HWM_NMI_N	Input	UCD90124A Interrupt
	GPIOQ7	RST_HWM_N	Output	Reset from BMC to HWM

3.3 Management devices

Interface	Component	Element
LPC	Broadwell-DE	LPC
PECI	Broadwell-DE	PECI
NC-SI	Intel I210	NC-SI
PWM/ FANTACH	FAN	FAN0~4
ADC	P12V	VOLTAGE
	BMC_HEATER	VOLTAGE
	P2V5_VIN	VOLTAGE
	P1V0_DDR	VOLTAGE
	P5V0_VIN P5V_SB	VOLTAGE
	BMC_P1V26	VOLTAGE
	BMC_P1V538	VOLTAGE
	BMC_P3V3	VOLTAGE
I2C1	TMP75AIDGKR Address : 0x49	Internal Sensor
	TMP75AIDGKR Address : 0x4A	Internal Sensor
	UCD90124A Address :0x34	Monitor1
		Monitor2
		Monitor3
		Monitor4
		Monitor5
		Monitor6
		Monitor8
		Monitor9
		Monitor10
		Monitor11
		Monitor12
		Monitor13
		Fan0
		Fan1
		Fan2
		Fan3
		Fan4
	TMP75AIDGKR	Internal

	Address : 0x4D	Sensor
	TMP75AIDGKR Address : 0x4E	Internal Sensor
	TMP451AIDQF Address:0x4C	Internal Sensor
		External Sensor
		MCU Address:0x58
I2C3	CPLD	Address:0x33

4 CPLD

4.1 CPU board CPLD Resistor Mapping & Description

Offset	Register Name	Function/Notes
0x00	CPLD Revision	CPLD revision register
0x01	Status-0	Status register for reading input signals from BMC
0x02	Status-1	Status register for reading information of BIOS flash selection
0x03	Cntrl-0	Control register used to send signals to BMC
0x04	Cntrl-1	Control register used to send signals to BMC
0x05	Mask-0	
0x06	SKU ID	SKU ID register

CPU CPLD resistor description is shown as below:

CPLD Revision				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x00	D[3:0]	1011	RO	CPLD Revision Number, hardwired
	D[7:4]	0000	RO	CPLD Revision Number, hardwired

Status-0				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x01	D[0]	x	RO	Reserved
	D[1]	x	RO	Reserved
	D[2]	x	RO	Reserved
	D[3]	x	RO	Reserved
	D[4]	x	RO	Reserved
	D[5]	x	RO	Reserved
	D[6]	1	RW	BMC_to_HOST_INT_L Non-maskable Interrupt Request from BMC

Status-0				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[7]	1	RW	BMC_to_HOST_NMI_L Interrupt Request from BMC

Status-1				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x02	D[0]	x	RO	Reserved
	D[1]	x	RO	Reserved
	D[2]	x	RO	Reserved
	D[3]	x	RO	Reserved
	D[4]	x	RO	Reserved
	D[5]	x	RO	Reserved
	D[6]	x	RO	Reserved
	D[7]	x	RO	BIOS_MUXSEL Actual value of BIOS_MUXSEL. If the CPLD watchdog logic triggered, it will be different than this bit. Otherwise, it will be same value.
Status-1				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x02	D[0]	x	RO	Reserved
	D[1]	x	RO	Reserved
	D[2]	x	RO	Reserved
	D[3]	x	RO	Reserved
	D[4]	x	RO	Reserved
	D[5]	x	RO	Reserved
	D[6]	x	RO	Reserved
	D[7]	x	RO	BIOS_MUXSEL Actual value of BIOS_MUXSEL. If the CPLD watchdog logic triggered, it will be different than this bit. Otherwise, it will be same value.

Cntrl-0				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x03	D[0]	x	RW	Reserved
	D[1]	x	RW	Reserved
	D[2]	x	RW	Reserved
	D[3]	x	RW	Reserved
	D[4]	1	RW	HOST_to_BMC_INT_L Interrupt Request to BMC
	D[5]	1	RW	HOST_to_BMC_RST_L Reset signal to reset BMC from CPU
	D[6]	1	RW	Reserved
	D[7]	1	RW	HOST_to_MB_RST_L Reset signal to reset motherboard from CPU

Cntrl-1				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x04	D[0]	1	RW	WDT_RCVRY_EN This bit enables the watchdog recovery logic. It controls BIOS_MUX_SEL
	D[1]	1	RW	WDT_DOG_EN This bit enables the Watchdog timer during boot process. The CPU must disable this bit right after it boots. It is enabled upon power up or SYS_RS_L
	D[2]	x	RW	Reserved
	D[3]	x	RW	Reserved
	D[4]	x	RW	Reserved
	D[5]	x	RW	Reserved
	D[6]	x	RW	Reserved
	D[7]	0	RW	BIOS_MUX_SEL This bit is not reset with a hardware reset. It will default to its value when power up, only. This value is used to write to the BIOS MUX selector when watchdog recovery is disabled (WDT_RCVRY_EN=0).

Mask-0				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x05	D[0]	1	RW	PCIE_RESET_MASK Mask to disable CPLD_PCIE_RESET_N going to motherboard.
	D[1]	x	RW	Reserved
	D[2]	x	RW	Reserved
	D[3]	x	RW	Reserved
	D[4]	x	RW	Reserved
	D[5]	x	RW	Reserved
	D[6]	1	RW	BMC_to_HOST_INT_Mask Mask to disable BMC-to-Host Interrupt.
	D[7]	x	RW	Reserved

SKU ID				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x06	D[0]	1	RO	Build ID [1:0] = 01 00 : 1 01 : 2 10 : 3 11 : 4
	D[1]	0	RO	

SKU ID				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[2]	1	RO	HW_REV_ID[1..0]=11 Hardware Revision [1:0]= 10 00: Proto 01: Alpha 10: Beta 11: PVT
	D[3]	1	RO	
	D[4]	0	RO	SKU_ID[3..0] 0000 : Apache BroadWell-DE CPU board 0001 : Reserved : 1111 : Reserved
	D[5]	0	RO	
	D[6]	0	RO	
	D[7]	0	RO	

4.2 Main board CPLD Resistor Mapping & Description

Offset	Register Name	Function/Notes
0x00	Board ID	Reserved
0x01	Extend Board ID	Reserved
0x02	Code Version	CPLD firmware version
0x03	PLL Lock	DPLL & MAC lock status
0x04	DPLL Input Lost	IDT DPLL input loss control
0x05	Fan Present	FAN presence status
0x06	Multiple Interface Select	UART, I2C and 1PPS mux control
0x07	PTP Control	ToD port 1PPS & ToD input/output control
0x08	Power Status	PSU, BMC, MB, CPU power status
0x09	Power Control	USB and heater power control
0x0A	Port Over Current	SFP and USB ports over current interrupt
0x0B	Fan Interrupt	Fan status(stop or working) interrupt
0x0C	NMI Interrupt	Hardware(Thermal sensor, PSU, HWM, Heater) NMI interrupt
0x0D	MAC & PHY Interrupt	MAC & 10G, 100G PHY interrupt
0x0E	SyncE & PTP Interrupt	DPLL, JA, GNSS, BITS interrupt
0x0F	SFP Port Interrupt	SFP port transceivers interrupt
0x10	Miscellaneous Interrupt	Miscellaneous interrupt
0x11	Interrupt Mask	Interrupt to CPLD mask
0x12	Reset Status	CPU and reset button status
0x13	I2C Mux Reset	I2C mux reset control
0x14	BMC Reset	BMC reset control
0x15	MAC & PHY Reset	MAC, 10G, 100G PHY reset control
0x16	Miscellaneous Reset	DPLL, JA, BITS, GNSS, HWM and NIC reset control

0x17	Global Reset	Global reset control
0x18	System LED Control1	Front panel LED control
0x19	System LED Control2	Front panel LED control
0x1A	System LED Blinking	Front panel LED blinking rate control
0x1B	Fan4 & Fan5 TACH Switch	Fan4 & fan5 TACH to HWM control
0x1C	GNSS Status	GNSS status

Board ID				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x00	D[1:0]	00	RO	Build REV [1:0] Reserved
	D[3:2]	11	RO	HW REV[1:0] Reserved
	D[7:4]	1110	RO	Model ID [3:0] Reserved

Extend Board ID				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x01	D[3:0]	0001	RO	Board ID [3:0] Reserved
	D[7:4]	0000	RO	Reserved

CPLD Version				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x02	D[7:0]	00000000	RO	CPLD code Revision Bit[7:0]: 00000000: CPLD Code Revision is X.00 00000001: CPLD Code Revision is X.01 00000010: CPLD Code Revision is X.02 00000011: CPLD Code Revision is X.03 …

PLL Lock				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x03	D[0]	1	RO	SMU_DPLL1_LOCK 0：82P33831 DPLL1 is not locked 1：82P33831 DPLL1 is locked
	D[1]	1	RO	SMU_DPLL2_LOCK 0：82P33831 DPLL2 is not locked 1：82P33831 DPLL2 is locked
	D[2]	1	RO	SMU_DPLL3_LOCK 0：82P33831 DPLL3 is not locked 1：82P33831 DPLL3 is locked
	D[3]	1	RO	Reserved

PLL Lock				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[4]	1	RO	MAC_COREPLL_LOCK 0：MAC COREPLL is not lock 1：MAC COREPLL is lock
	D[5]	1	RO	MAC_MCUPLL_LOCK 0：MAC MCUPLL is not lock 1：MAC MCUPLL is lock
	D[6]	1	RO	Reserved
	D[7]	1	RO	Reserved

DPLL Input Lost				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x04	D[0]	1	RW	Reserved
	D[1]	1	RW	SMU_INPUT1_LOS_N 0：82P33831 input x lost assert 1：82P33831 input x lost de-assert
	D[2]	1	RW	Reserved
	D[3]	1	RW	Reserved
	D[4]	1	RW	Reserved
	D[5]	1	RW	Reserved
	D[6]	1	RW	Reserved
	D[7]	1	RW	Reserved

Fan Present				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x05	D[0]	0	RO	FAN1_PRSNT_N 0：Fan1 present 1：Fan1 absent
	D[1]	0	RO	FAN2_PRSNT_N 0：Fan2 present 1：Fan1 absent
	D[2]	0	RO	FAN3_PRSNT_N 0：Fan3 present 1：Fan3 absent
	D[3]	0	RO	FAN4_PRSNT_N 0：Fan4 present 1：Fan4 absent
	D[4]	0	RO	FAN5_PRSNT_N 0：Fan5 present 1：Fan5 absent
	D[5]	1	RO	Reserved
	D[6]	1	RO	Reserved
	D[7]	1	RO	Reserved

Multiple Interface Select				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x06	D[0]	0	RW	Reserved
	D[1]	0	RW	UART_CPU_BMC_MUX_SEL 0：UART console port connect to CPU 1：UART console port connect to BMC
	D[2]	1	RW	Reserved
	D[3]	0	RW	I2C0_MGMT_MUX_ SEL 0：BMC I2C2 control MGMT I2C device(BMC I2C2 connect to MGMT I2C) 1：CPU I2C0 control MGMT I2C device(CPU I2C0 connect to MGMT I2C)
	D[4]	0	RW	Reserve
	D[5]	0	RW	I2C0_HWM_MUX_SEL 0：Hardware monitor I2C connect to BMC I2C1 1：Hardware monitor I2C connect to CPU I2C0
	D[6]	1	RW	PTP_1PPS_MUX_SEL 0：DPLL FRSYNC 1PPS connect to CLK_PTP_1PPS_DPLL_TO_MAC 1：DPLL APLL1 1PPS connect to CLK_PTP_1PPS_DPLL_TO_MAC
	D[7]	1	RW	Reserved

PTP Control				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x07	D[0]	0	RW	PTP_TOD_RS422_TXD_EN 0：Disable ToD port UART TX 1：Enable ToD port UART TX
	D[1]	0	RW	PTP_TOD_RS422_RXD_EN_N 0：Enable ToD port UART RX 1：Disable ToD port UART RX
	D[2]	0	RW	PTP_1PPS_RS422_TXD_EN 0：Disable ToD 1PPS TX 1：Enable ToD 1PPS TX
	D[3]	0	RW	PTP_1PPS_RS422_RXD_EN_N 0：Enable ToD 1PPS RX 1：Disable ToD 1PPS RX
	D[4]	0	RW	Reserve
	D[5]	0	RW	Reserve
	D[6]	0	RW	Reserve
	D[7]	0	RW	Reserve

Power Status				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x08	D[0]	1	RO	PWROK_SYS_DC 0：Switching subsystem power is abnormal 1：Switching subsystem power is ok
	D[1]	1	RO	CPU_TO_CPLD_PWRGD 0：CPU power is not ready 1：CPU power is ok
	D[2]	1	RO	BMC_PWRGD 0：BMC power is not ready 1：BMC power is ok
	D[3]	0	RO	CPU_PRSNT_L 0：CPU is present 1：CPU is absent
	D[4]	1	RO	PSU1_PWROK 0：PSU1 Power is abnormal. 1：PSU1 Power is OK.
	D[5]	1	RO	PSU2_PWROK 0：PSU2 Power is abnormal. 1：PSU2 Power is OK.
	D[6]	0	RO	PSU1_PRSNT_N 0：PSU1 Present 1：PUS1 Absent
	D[7]	0	RO	PSU2_PRSNT_N 0：PSU2 Present 1：PUS2 Absent

Power Control				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x09	D[0]	0	RW	PWR_OFF_MAC 0：MAC power is normal 1：Turn off MAC power
	D[1]	0	RW	Reserved
	D[2]	0	RW	Reserved
	D[3]	1	RW	USB_PWR_EN 0：USB power is disabled 1：USB power is enabled
	D[4]	0	RW	BMC heater power enable 0：Normal 1：Force BMC heater power enabled
	D[5]	1	RW	Reserve

Power Control				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[6]	1	RW	Reserve
	D[7]	1	RW	Reserve

Port Over Current				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x0A	D[0]	1	RO	SFP+_PWR_OC_GP1 1：Normal 0：SFP+ port 0~7 over current
	D[1]	1	RO	SFP+_PWR_OC_GP2 1：Normal 0：SFP+ port 8~15 over current
	D[2]	1	RO	SFP+_PWR_OC_GP3 1：Normal 0：SFP+ port 16~19 over current
	D[3]	1	RO	QSFP28_PWR_OC_N 1：Normal 0：QSFP28 port 0~1 over current
	D[4]	1	RO	SFP28_PWR_OC_N 1：Normal 0：SFP28 port 21~27over current
	D[5]	1	RO	USB_PWR_OC_N 1：Normal 0：USB port over current
	D[6]	0	RO	Reserve
	D[7]	0	RO	Reserve

Fan Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x0B	D[0]	1	RO	INT_FAN1_N 0：Fan1 interrupt assert 1：Fan1 interrupt de-assert
	D[1]	1	RO	INT_FAN2_N 0：Fan2 interrupt assert 1：Fan2 interrupt de-assert
	D[2]	1	RO	INT_FAN3_N 0：Fan3 interrupt assert 1：Fan3 interrupt de-assert
	D[3]	1	RO	INT_FAN4_N 0：Fan4 interrupt assert 1：Fan4 interrupt de-assert

Fan Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[4]	1	RO	INT_FAN5_N 0：Fan5 interrupt assert 1：Fan5 interrupt de-assert
	D[5]	0	RO	Reserved
	D[6]	0	RO	Reserved
	D[7]	0	RO	Reserved

NMI Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x0C	D[0]	1	RO	INT_FAN_CARD_N 0：Fan card interrupt assert 1：Fan card interrupt de-assert
	D[1]	1	RO	INT_HWM_NMI_N 0：Hardware monitor interrupt assert 1：Hardware monitor interrupt de-assert
	D[2]	1	RO	INT_PSU1_N 0：PSU1 interrupt assert 1：PSU1 interrupt de-assert
	D[3]	1	RO	INT_PSU2_N 0：PSU2 interrupt assert 1：PSU2 interrupt de-assert
	D[4]	1	RO	BMC_HEATING_DONE 0：BMC heater interrupt assert (BMC heater time out) 1：BMC heater interrupt de-assert
	D[5]	0	RO	Reserved
	D[6]	0	RO	Reserved
	D[7]	0	RO	Reserved

MAC & PHY Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x0D	D[0]	1	RO	INT_MAC_N 0：MAC interrupt assert 1：MAC interrupt de-assert
	D[1]	1	RO	INT_PHY1_N 0：PHY1 interrupt assert 1：PHY1 interrupt de-assert
	D[2]	1	RO	INT_PHY3_N 0：PHY3 interrupt assert 1：PHY3 interrupt de-assert

MAC & PHY Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[3]	0	RO	Reserved
	D[4]	0	RO	Reserved
	D[5]	0	RO	Reserved
	D[6]	0	RO	Reserved
	D[7]	0	RO	Reserved

SyncE & PTP Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x0E	D[0]	1	RO	INT_CJA_INTR_N 0：Clock buffer Si5344D interrupt assert 1：Clock buffer Si5344D de-assert
	D[1]	1	RO	INT_CJA_LOL_N 0：Clock buffer Si5344D LOL interrupt assert 1：Clock buffer Si5344D LOL de-assert
	D[2]	1	RO	Reserved
	D[3]	1	RO	INT1_GNSS_N 0：GPS NEO-M8T-0 interrupt 1 assert 1：GPS NEO-M8T-0 interrupt 1 de-assert
	D[4]	1	RO	INT_BITS_N 0：BITS interrupt assert 1：BITS interrupt de-assert
	D[5]	1	RO	INT_SMU_N 0：DPLL interrupt assert 1：DPLL interrupt de-assert
	D[6]	0	RO	Reserved
	D[7]	0	RO	Reserved

SFP Port Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x0F	D[0]	1	RO	INT_SFP+_FLT_N0 0：INT_SFP+_FLT_N0 interrupt assert 1：INT_SFP+_FLT_N0 interrupt de-assert
	D[1]	1	RO	INT_SFP+_FLT_N1 0：INT_SFP+_FLT_N1 interrupt assert 1：INT_SFP+_FLT_N1 interrupt de-assert
	D[2]	1	RO	INT_SFP+_LOS_N0 0：INT_SFP+_LOS_N0 interrupt assert 1：INT_SFP+_LOS_N0 interrupt de-assert
	D[3]	1	RO	INT_SFP+_LOS_N1 0：INT_SFP+_LOS_N1 interrupt assert 1：INT_SFP+_LOS_N1 interrupt de-assert

SFP Port Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[4]	1	RO	INT_SFP+_ABS_N0 0：INT_SFP+_ABS_N0 interrupt assert 1：INT_SFP+_ABS_N0 interrupt de-assert
	D[5]	1	RO	INT_SFP+_ABS_N1 0：INT_SFP+_ABS_N1 interrupt assert 1：INT_SFP+_ABS_N1 interrupt de-assert
	D[6]	1	RO	INT_QSFP28_N 0：INT_QSFP28_N interrupt assert 1：INT_QSFP28_N interrupt de-assert
	D[7]	0	RO	Reserved

Miscellaneous Interrupt				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x10	D[0]	1	RO	INT_TSEN_ALRT_N 0：Temperature sensor interrupt assert 1：Temperature sensor interrupt de-assert
	D[1]	1	RO	INT_TSEN_NMI_N 0：Temperature sensor NMI interrupt assert 1：Temperature sensor NMI interrupt de-assert
	D[2]	1	RO	Reserved
	D[3]	1	RO	Reserved
	D[4]	1	RO	INT_HWM_ALERT_N 0：Hardware monitor alert assert 1：Hardware monitor alert de-assert
	D[5]	0	RO	Reserved
	D[6]	0	RO	Reserved
	D[7]	0	RO	Reserved

Interrupt Mask				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x11	D[0]	0	RW	Global Mask 0：Normal 1：Mask all interrupts
	D[1]	0	RW	Fan Interrupt Mask 0：Normal 1：Mask fan interrupts
	D[2]	0	RW	NMI Interrupt Mask 0：Normal 1：Mask NMI interrupts

Interrupt Mask				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[3]	0	RW	MAC & PHY Interrupt Mask 0：Normal 1：Mask MAC & PHY interrupts
	D[4]	0	RW	SyncE & PTP Interrupt Mask 0：Normal 1：Mask SyncE & PTP interrupts
	D[5]	0	RW	SFP Port Interrupt Mask 0：Normal 1：Mask SFP Port interrupts
	D[6]	0	RW	Miscellaneous Interrupt Mask 0：Normal 1：Mask Miscellaneous interrupts
	D[7]	0	RW	Reserve

Reset Status				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x12	D[0]	1	RO	RST_PLTRST_N 0：CPU platform reset assert 1：CPU platform reset de-assert
	D[1]	1	RO	RST_PCIE_CPU_TO_MB_N 0：PCIE CPU to main board reset assert 1：PCIE CPU to main board reset de-assert
	D[2]	1	RO	RST_SW_BTN_N 0：Switch Button reset assert 1：Switch Button reset de-assert
	D[3]	0	RO	Reserved
	D[4]	0	RO	Reserved
	D[5]	0	RO	Reserved
	D[6]	0	RO	Reserved
	D[7]	1	RO	RST_SW_BTN_N >5S (Load factory default) 0：Load system to factory default 1：No action

I2C Mux Reset				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x13	D[0]	1	RW	RST_I2C_MUX1_N 0：Reset I2C MUX1 1：Normal
	D[1]	1	RW	RST_I2C_MUX2_N 0：Reset I2C MUX2 1：Normal

I2C Mux Reset				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[2]	1	RW	RST_I2C_MUX3_N 0：Reset I2C MUX3 1：Normal
	D[3]	1	RW	RST_I2C_MUX4_N 0：Reset I2C MUX4 1：Normal
	D[4]	1	RW	RST_I2C_MUX5_N 0：Reset I2C MUX5 1：Normal
	D[5]	1	RW	RST_I2C_MUX6_N 0：Reset I2C MUX6 1：Normal
	D[6]	1	RW	RST_I2C_MUX7_N 0：Reset I2C MUX7 1：Normal
	D[7]	1	RW	Reserve

BMC Reset				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x14	D[0]	1	RW	Reserved
	D[1]	1	RW	RST_BMC_PCIE_N/ RST_BMC_LPC_N 0：Reset BMC PCIE/LPC 1：Normal
	D[2]	1	RW	Reserved
	D[3]	1	RW	Reserved
	D[4]	1	RW	RST_BMC_WDT_L 0：Reset BMC watch dog 1：Normal
	D[5]	0	RW	Reserved
	D[6]	0	RW	Reserved
	D[7]	0	RW	Reserved

MAC &PHY Reset				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x15	D[0]	1	RW	RST_MAC_N 0：Reset MAC 1：Normal
	D[1]	1	RW	RST_PHY1_N 0：Reset PHY1 1：Normal

MAC &PHY Reset				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[2]	1	RW	RST_PHY3_N 0：Reset PHY3 1：Normal
	D[3]	0	RW	Reserved
	D[4]	0	RW	Reserved
	D[5]	0	RW	Reserved
	D[6]	0	RW	Reserved
	D[7]	0	RW	Reserved

Miscellaneous Reset				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x16	D[0]	1	RW	RST_CJA_N 0：Reset clock buffer Si5344D 1：Normal
	D[1]	1	RW	RST_USB_BRIDGE_N 0：Reset USB bridge CP2130 1：Normal
	D[2]	1	RW	RST_SMU_N 0：Reset DPLL 82P33831 1：Normal
	D[3]	1	RW	Reserved
	D[4]	1	RW	RST_GNSS_N 0：Reset GNSS NEO-M8T 1：Normal
	D[5]	1	RW	RST_BITS_N 0：Reset BITS 82P2281 1：Normal
	D[6]	1	RW	RST_NIC1_N 0：Reset NIC1 I210 1：Normal
	D[7]	1	RW	RST_NIC1_PCIE_N 0：Reset NIC1 PCIE 1：Normal

Global Reset				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x17	D[0]	1	RW	Global reset 0：Reset Switch board 1：Normal
	D[1]	0	RW	Reserved
	D[2]	0	RW	Reserved

Global Reset				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[3]	0	RW	Reserved
	D[4]	0	RW	Reserved
	D[5]	0	RW	Reserved
	D[6]	0	RW	Reserved
	D[7]	0	RW	Reserved

System LED Control1				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x18	D[0]	0	RW	SYNC Status LED On/Off 0：Off 1：On
	D[1]	0	RW	SYNC Status LED color 0：Yellow 1：Green
	D[2]	0	RW	GNSS Status LED On/Off 0：Off 1：On
	D[3]	0	RW	GNSS Status LED color 0：Yellow 1：Green
	D[4]	0	RW	Reserved
	D[5]	0	RW	Reserved
	D[6]	0	RW	System Status LED On/Off 0：Off 1：On
	D[7]	0	RW	System Status LED color 0：Yellow 1：Green

System LED Control2				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x19	D[0]	0	RW	Reserved
	D[1]	0	RW	Reserved
	D[2]	0	RW	Reserved
	D[3]	0	RW	Reserved
	D[4]	0	RW	Reserved
	D[5]	0	RW	Reserved
	D[6]	0	RW	Reserved
	D[7]	0	RW	Reserved

System LED Blinking Control				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x1A	D[0]	0	RW	SYNC Status LED Blinking Status 0：Stable 1：Blinking
	D[1]	0	RW	GNSS Status LED Blinking Status 0：Stable 1：Blinking
	D[2]	0	RW	Reserved
	D[3]	0	RW	System Status LED Blinking Status 0：Stable 1：Blinking
	D[4]	0	RW	Reserved
	D[5]	0	RW	Reserved
	D[6]	0	RW	Reserved
	D[7]	0	RW	LED clear 0：Clear LED shift register 1：Normal

Fan4 & Fan5 TACH Switch				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x1B	D[0]	0	RW	Fan4 & Fan 5 tach in control mode 0：CPLD output 1Khz PWM to control FAN45_TACH_SW 1：FAN45_TACH_SW is controlled by write register D[1]
	D[1]	0	RW	Fan4 & Fan 5 tach in control 0：FAN45_TACH_SW is connected to HWM_FAN5_TACH_IN 1: FAN45_TACH_SW is connected to HWM_FAN4_TACH_IN
	D[2]	0	RW	Reserved
	D[3]	0	RW	Reserved
	D[4]	0	RW	Reserved
	D[5]	0	RW	Reserved
	D[6]	0	RW	Reserved
	D[7]	0	RW	Reserved

GNSS Status				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
0x1C	D[0]	1	RW	GNSS_ANT_SHORT_N 0：GNSS antenna is short 1：GNSS antenna is not short

GNSS Status				
Offset	**Bit Fields**	**Default**	**R/W**	**Description**
	D[1]	0	RW	GNSS_ANT_OPEN_N 0：GNSS antenna is open 1：GNSS antenna is not open
	D[2]	0	RW	Reserved
	D[3]	0	RW	Reserved
	D[4]	0	RW	Reserved
	D[5]	0	RW	Reserved
	D[6]	0	RW	Reserved
	D[7]	0	RW	Reserved