

REV	DESCRIPTION	ISSUE DATE
02XA1	ALPHA BUILD	2018.02.05
07XB1	BETA 1 BUILD	2018.06.09

# CSGR MAINBOARD

**20\*10G SFP+ Plus 8\*25G SFP28 Plus 2\*100G QSFP28 with SyncE & 1588V2 Support**

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07	MAC_BCM88470_CLK & MGMT	35	CPLD_10M04SAU169I7G	63	BMC_DC_3.3V TO 1.5V & 1.26V
08	MAC_BCM88470_SERDES	36	HW MONITOR_UCD90124A	64	DC_PWR UP SEQUENCE
09	MAC_BCM88470_DDRA & SDRAM	37	DC_PWR_BMC_HEATER	65	DC_PWR_12V TO 5V
10	MAC_BCM88470_DDRB & SDRAM	38	THERMAL SENSOR	66	DC_PWR_12V TO 3.3V
11	MAC_BCM88470_DDRC & SDRAM	39	IO EXPANDER1	67	DC_PWR_12V TO 1.8V
12	MAC_BCM88470_DDR_DECAPS1	40	IO EXPANDER2	68	DC_PWR_12V TO VCORE_CTRL
13	MAC_BCM88470_DDR_DECAPS2	41	I2C MUX1	69	DC_PWR_12V TO VCORE_DRVR
14	MAC_BCM88470_PWR1	42	I2C MUX2	70	DC_PWR_12V TO 1.0V
15	MAC_BCM88470_PWR2	43	PTP_GNSS MODULE	71	DC_PWR_12V TO 1.0V_DDR
16	MAC_BCM88470_GND	44	PTP_USB TO SPI BRIDGE	72	DC_PWR_12V TO 1.2V & 0.6V
17	PHY1_BCM82780_SERDES & MISC	45	PTP_T1/E1 RECEIVER	73	DC_PWR_12V TO 1.25V
18	PHY1_BCM82780_PWR & GND	46	PTP_T1/E1 & TOD IN/OUT	74	DC_PWR_12V TO 2.5V
19	PHY3_BCM82398	47	PTP_1PPS & 10MHZ IN/OUT	75	HOLES & BOM ONLY PARTS
20	CHIPSET JTAG CHAIN	48	PTP_PLL_82P33831		
21	CLOCK BUFFER1_1PPS & 4K	49	FAN CARD CONNECTOR		
22	CLOCK BUFFER2_156.25M	50	PSU PWR CONNECTOR		
23	LOCK BUFFER3_25M & 100M	51	CPU_PCIE X16 CONNECTOR		
24	PORT STATUS LED CONTROL	52	CPU_NIC1_I210-IT		
25	FIBER PORTS PWR SWITCH1	53	GBE OOB & USB PORT		
26	FIBER PORTS PWR SWITCH2	54	CONSOLE MUX & RS232 XCVR		
27	2x8 SFP+_CONN1_P01~P04	55	LED CARD HEADER & EEPROM		
28	2x8 SFP+_CONN1_P05~P08	56	BMC & CPU I2C MUX		

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# APACHE TELCO SWITCH DESIGN CHANGE HISTORY

Jan. 9, 2018. Release for Proto build.

Initial release.

Jun. 9, 2018. Release for Beta build.

BOM Manual:

202.01160.005 ==> 202.01160.015 / 202.01411.005

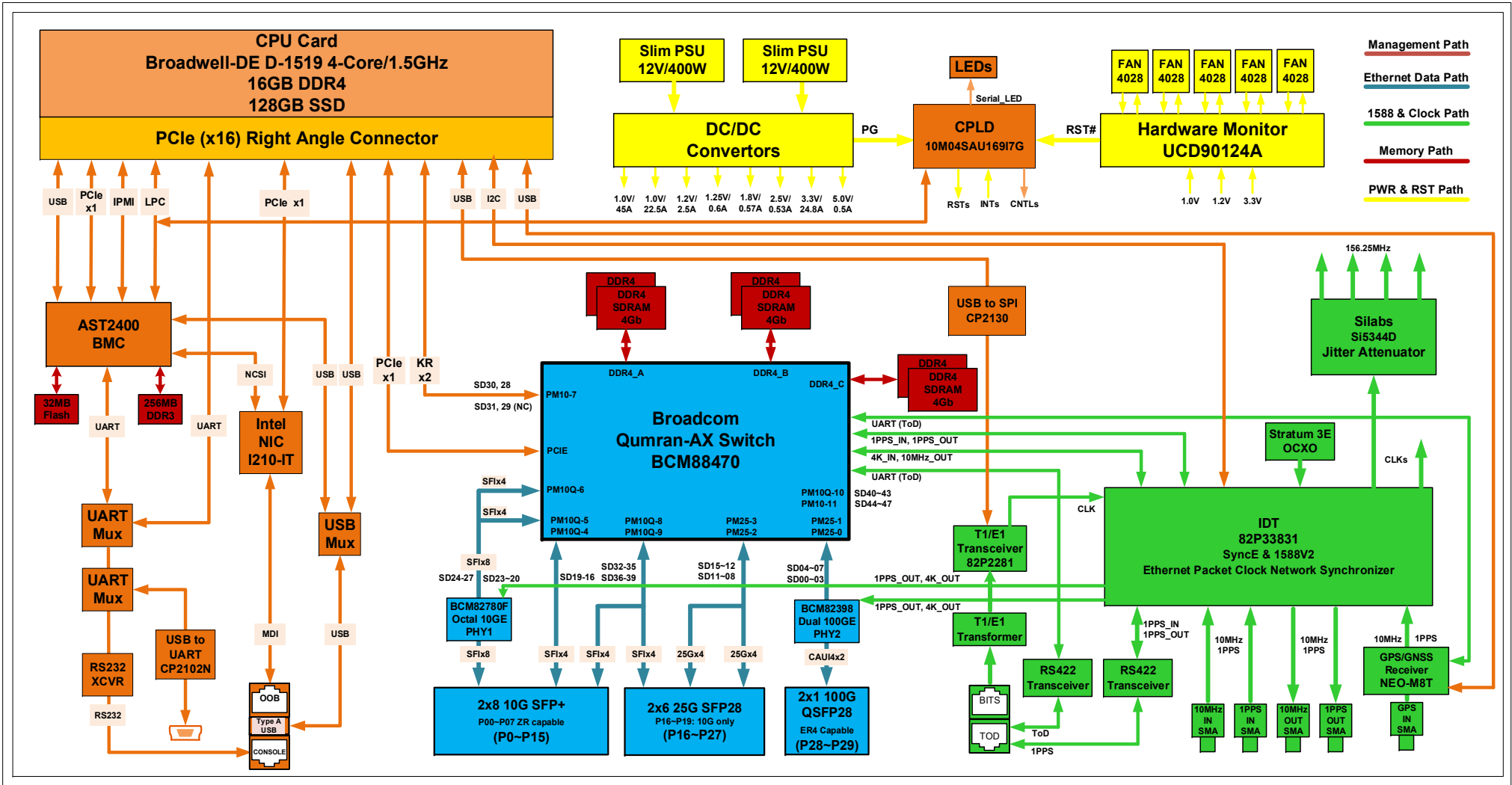
202.00009.005 ==> 202.00009.015

251.00681.005 ==> 251.00681.025

1. Change PHY BCM82391 to BCM82398 & remove PHY heater.
2. Change CPLD to 10M04SAU169I7G & IO pin assgiment update.
3. Change HWM UCD90910 to UCD90124A & connection change.
4. Add one more SPI flash for BMC dual boot function
5. Optimize BMC heater enable & output voltage adjust dessign.
6. Add PSU on/off control by HWM & thermal sensor
7. Port 20~P27 change from SFP+ to SFP28, cage change to 2\*6 SFP28
8. MAC & PHY 1588(1PPS/4K/10M) connection change
9. UART, thermal sensor & HWM I2C change to STB PWR
10. OSC, XTAL & 25M/100M/156.25M circuits optimization
11. Add LDO for OCXO & change OCXO to STB PWR
12. I2C bus connection change (CPLD, IO expander, I2C Mux)
13. Add additional pins on PCIe connector to/from CPU card
14. BMC GPIO pin assignment update and add dual boot flash
15. GNSS(antenna supervisor), BITS(TSCK in) & ToD(120ohm) circuit update
16. BOM option change to fix Alpha build issue

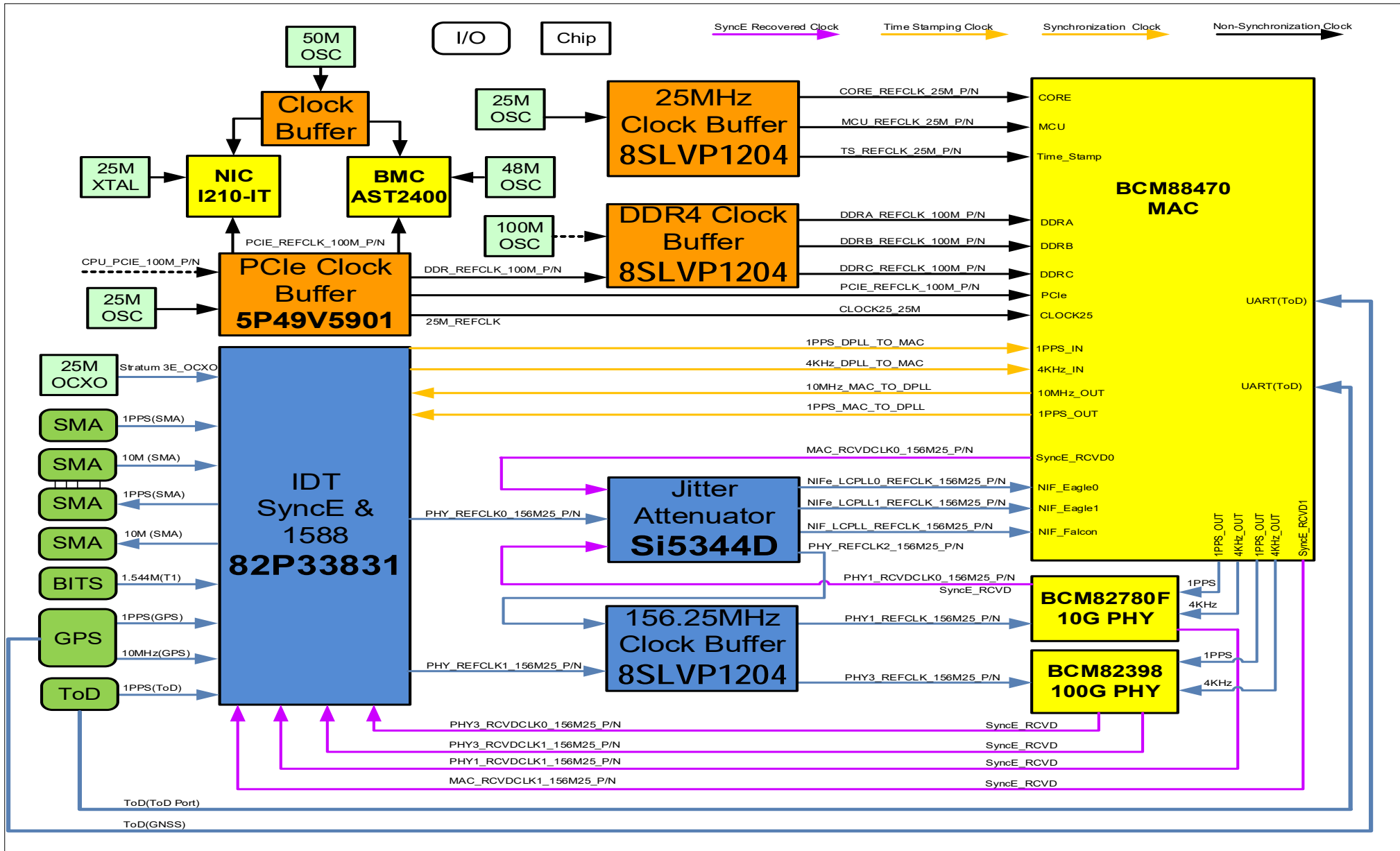
**DESIGN CHANGE HISTROY**

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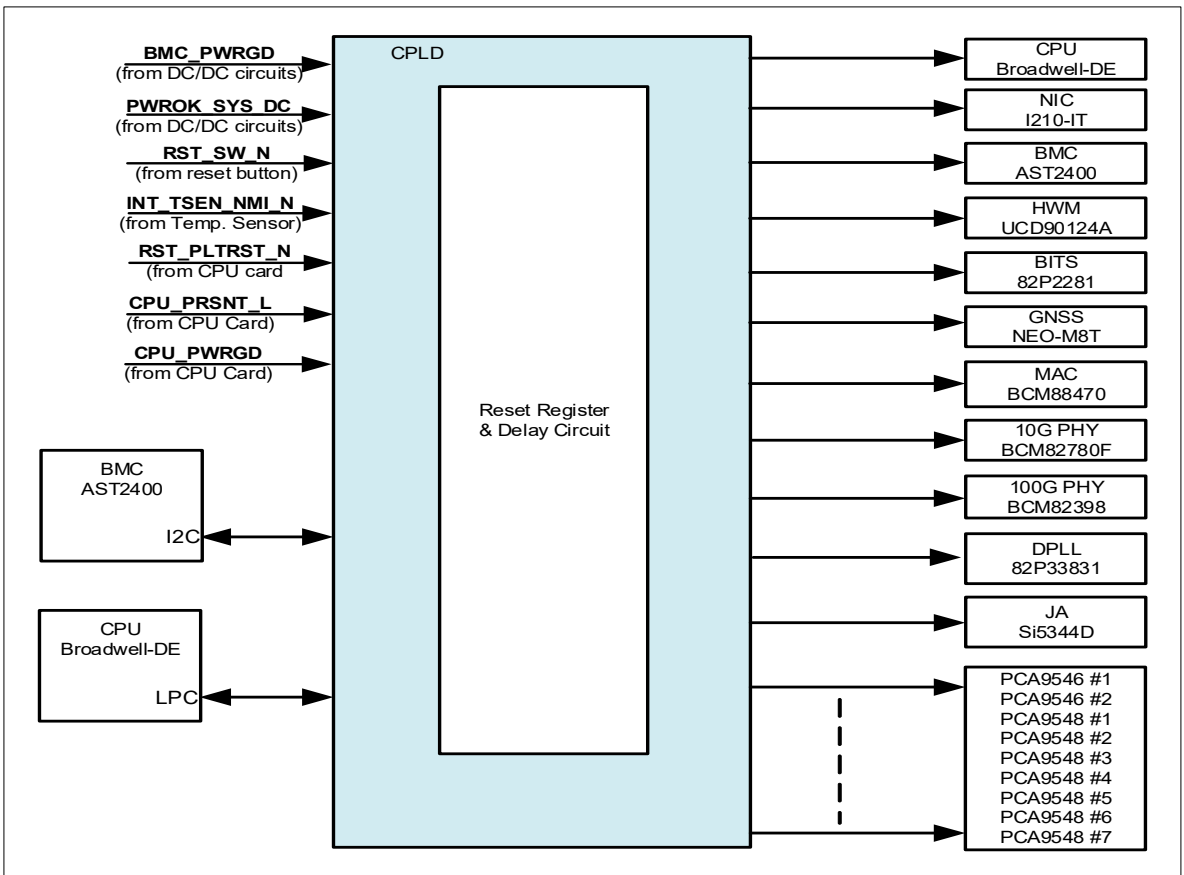
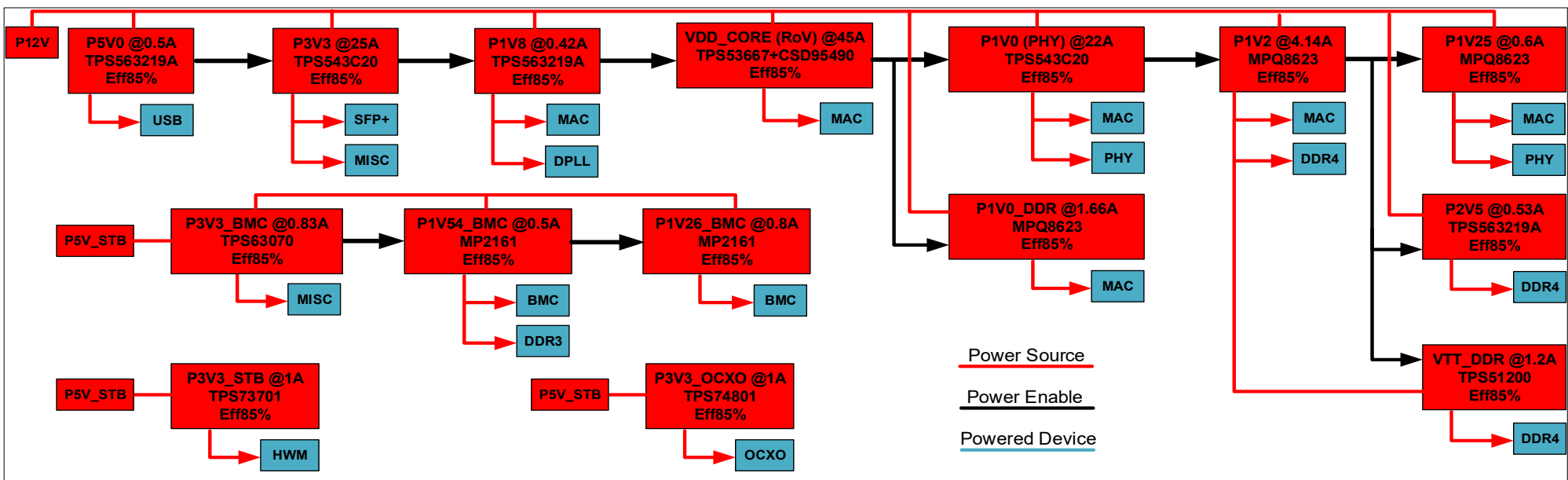


# SYSTEM BLOCK DIAGRAM

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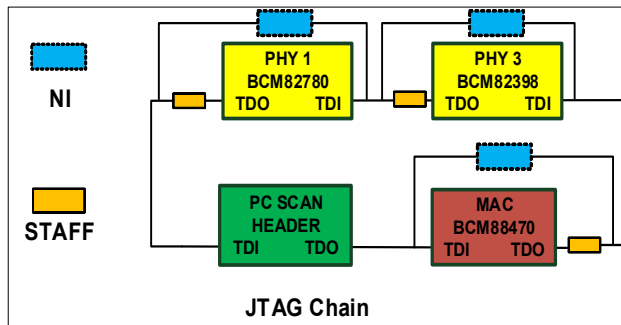
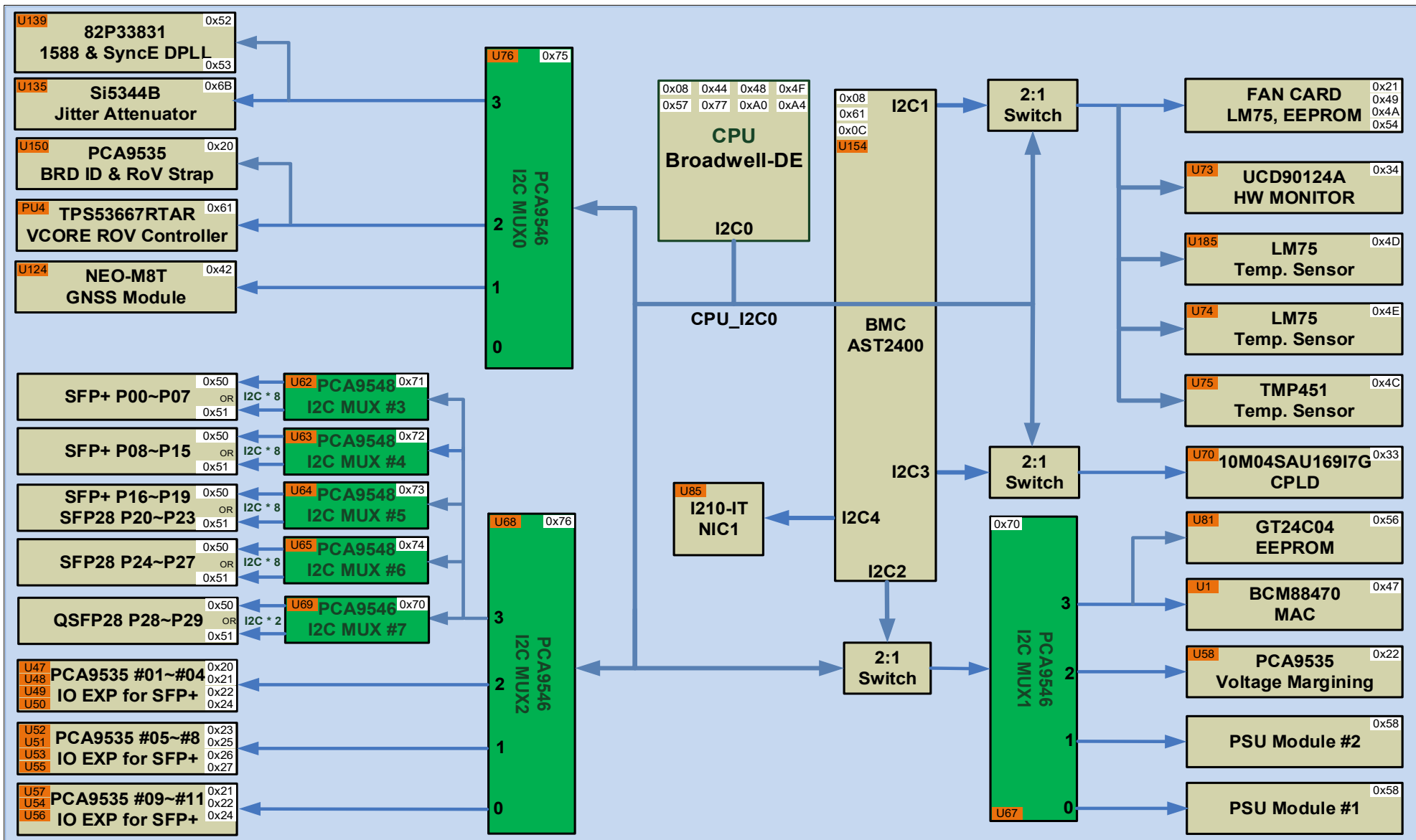
# CLOCK BLOCK DIAGRAM

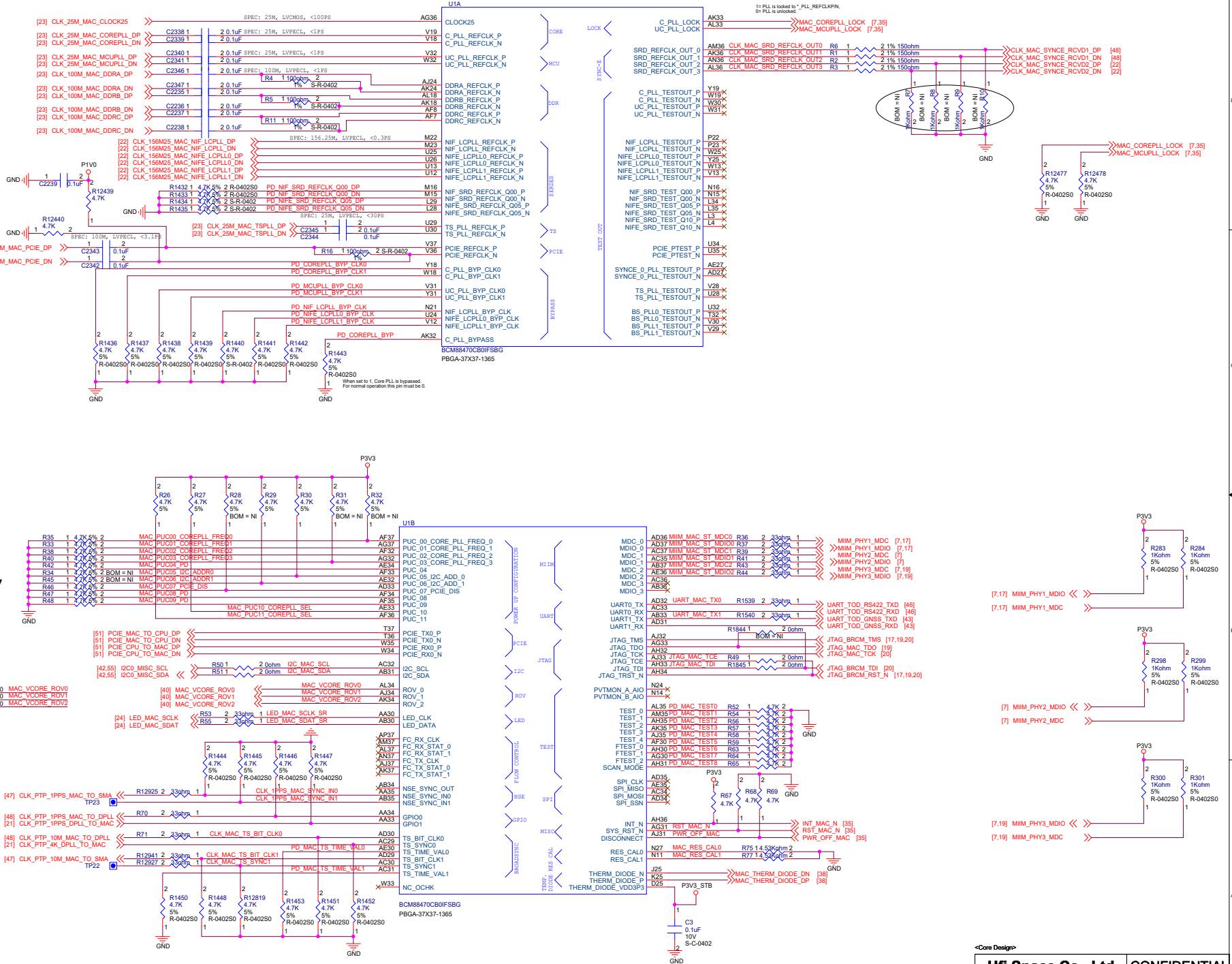


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# PWR & RST BLOCK DIAGRAM





Addr: 100011 Ox47

ROV[2:0]  
 000-->Initial State (1.00V)  
 001-->1.00V (Typical)  
 010-->0.85V  
 100-->1.04V

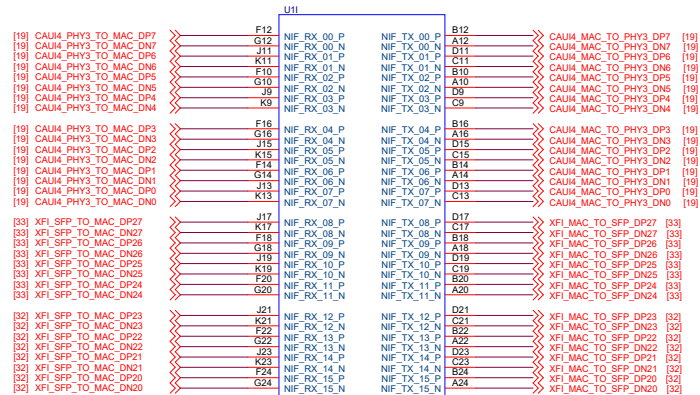
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# MAC\_BCM88470\_CLK & MGMT



BCM88470CBOIFSBG  
PBGA-37X37-1365



BCM88470CBOIFSBG  
PBGA-37X37-1365

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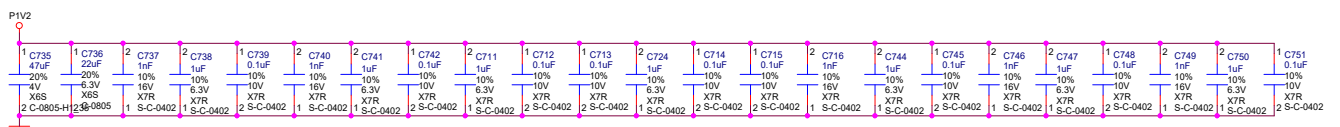
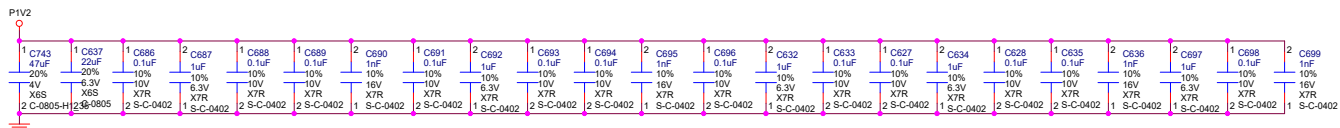
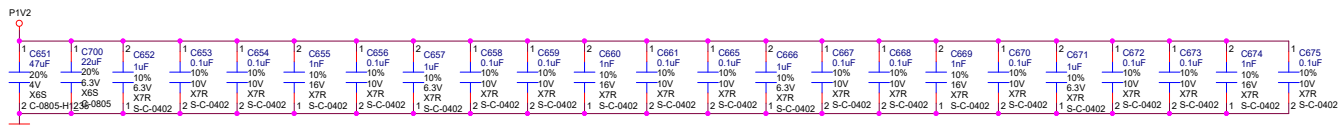








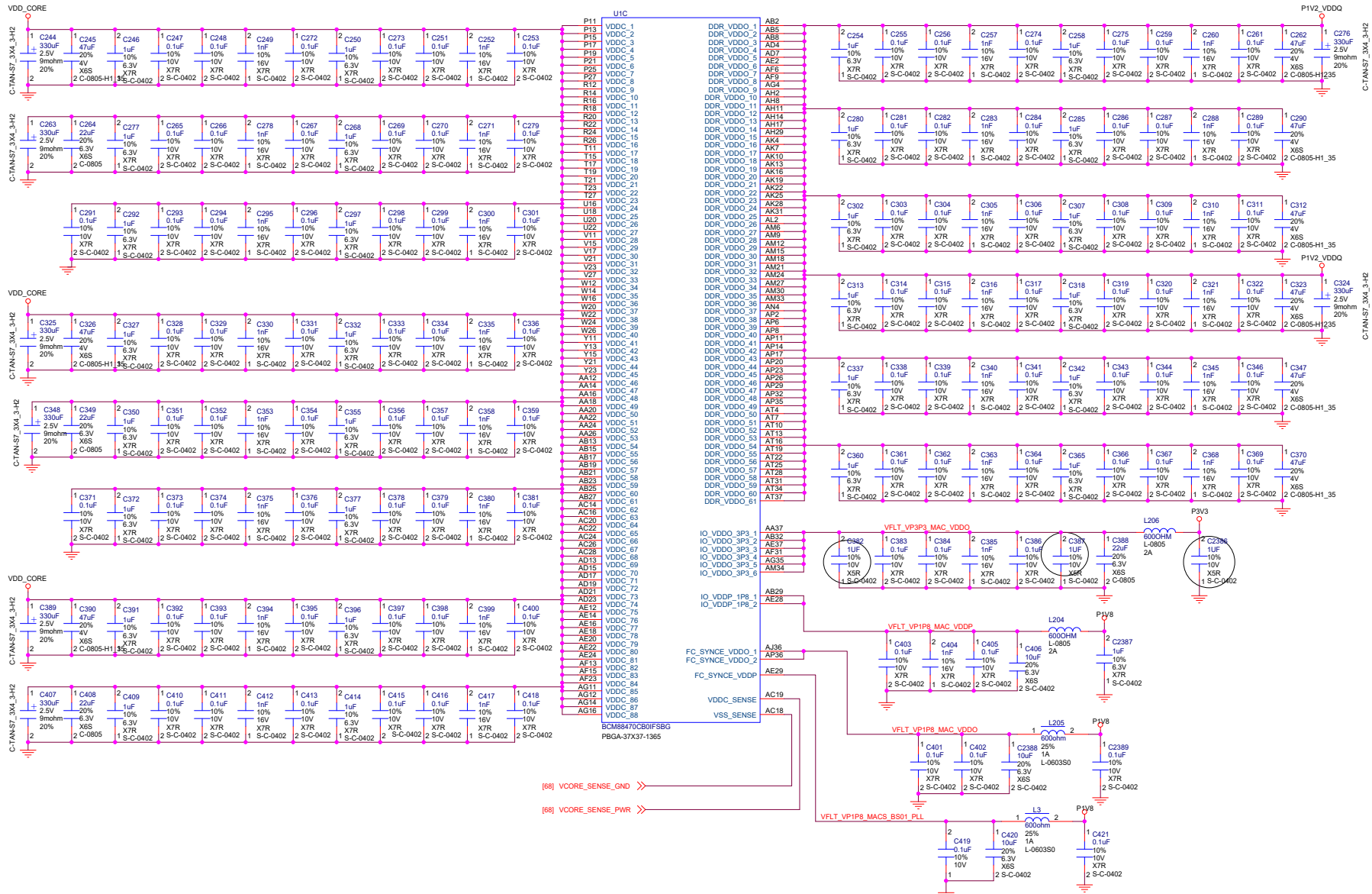




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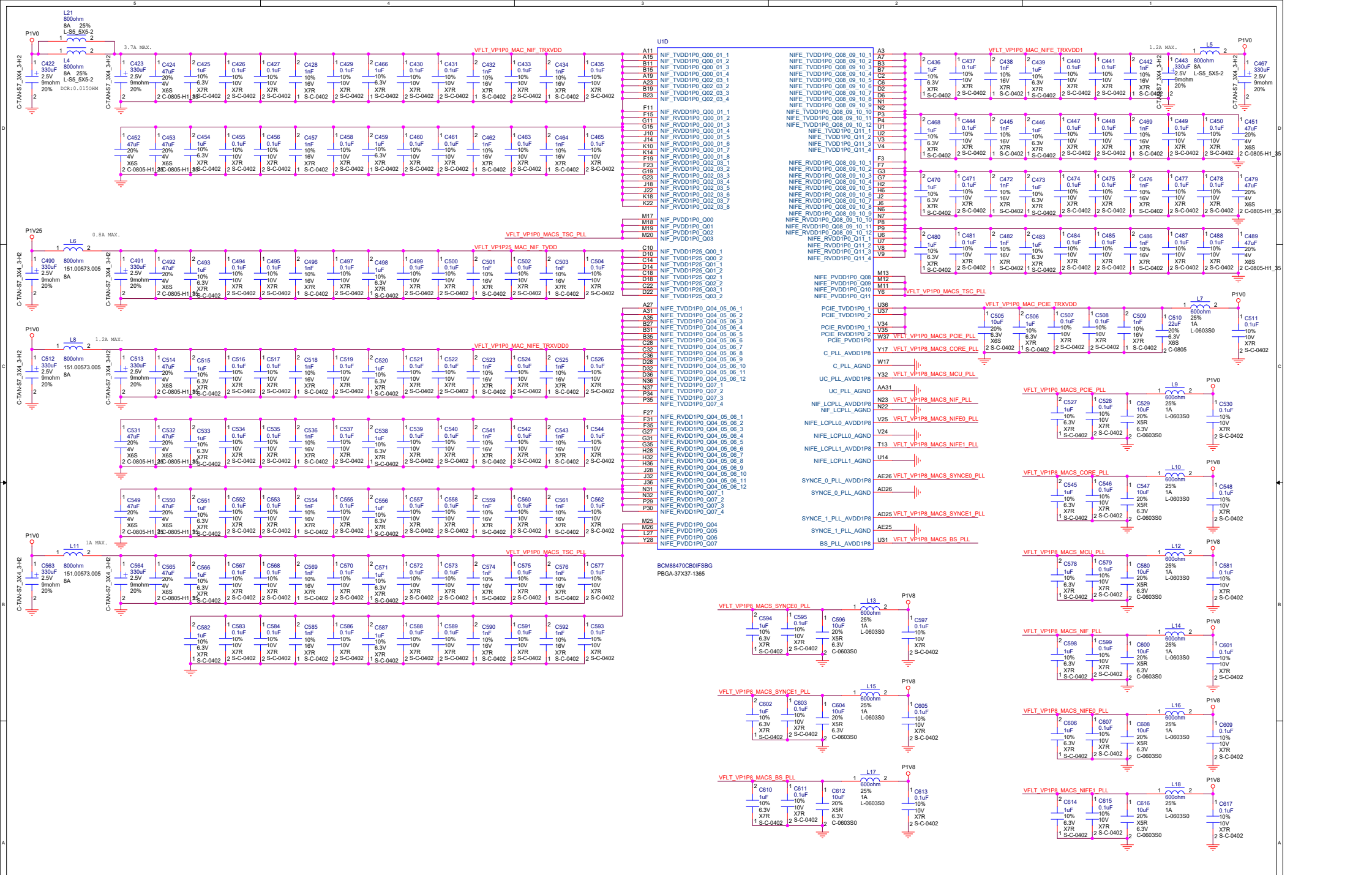
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# MAC\_BCM88470\_DDR\_DECAPS2



(B8) VCORE\_SENSE\_GND  
 (B8) VCORE\_SENSE\_PWR

# MAC\_BCM88470\_PWR1



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# MAC\_BCM88470\_PWR2

UJH		AE5	
P12	VSS_1	VSS_95	AE8
P14	VSS_2	VSS_96	AE13
P16	VSS_3	VSS_97	AE15
P18	VSS_4	VSS_98	AE17
P20	VSS_5	VSS_99	AE19
P24	VSS_6	VSS_100	AE21
P26	VSS_7	VSS_101	AE23
R11	VSS_8	VSS_102	AE31
R13	VSS_9	VSS_103	AE3
R15	VSS_10	VSS_104	AF12
R17	VSS_11	VSS_105	AF14
R19	VSS_12	VSS_106	AF16
R21	VSS_13	VSS_107	AF18
R23	VSS_14	VSS_108	AF20
R25	VSS_15	VSS_109	AF22
R27	VSS_16	VSS_110	AF24
R29	VSS_17	VSS_111	AF26
V16	VSS_18	VSS_112	AF29
V18	VSS_19	VSS_113	AG1
V20	VSS_20	VSS_114	AG3
V22	VSS_21	VSS_115	AG10
V24	VSS_22	VSS_116	AG13
V26	VSS_23	VSS_117	AG15
V28	VSS_24	VSS_118	AG19
V30	VSS_25	VSS_119	AG22
U11	VSS_26	VSS_120	AG23
U15	VSS_27	VSS_121	AG25
U17	VSS_28	VSS_122	AG27
U19	VSS_29	VSS_123	AG34
U21	VSS_30	VSS_124	AH5
U23	VSS_31	VSS_125	AH20
U27	VSS_32	VSS_126	AH25
V14	VSS_33	VSS_127	AH37
V16	VSS_34	VSS_128	C18
V18	VSS_35	VSS_129	C20
V20	VSS_36	VSS_130	C24
V22	VSS_37	VSS_131	C25
V24	VSS_38	VSS_132	AJ15
V26	VSS_39	VSS_133	AJ18
V28	VSS_40	VSS_134	AJ21
V30	VSS_41	VSS_135	AJ27
W12	VSS_42	VSS_136	AJ30
W14	VSS_43	VSS_137	AJ31
W16	VSS_44	VSS_138	AL5
W18	VSS_45	VSS_139	AL8
W20	VSS_46	VSS_140	AL11
W22	VSS_47	VSS_141	AL14
W24	VSS_48	VSS_142	AL17
W26	VSS_49	VSS_143	AL20
W28	VSS_50	VSS_144	AL23
W30	VSS_51	VSS_145	AL26
W32	VSS_52	VSS_146	AL29
W34	VSS_53	VSS_147	AL32
W36	VSS_54	VSS_148	AM3
W38	VSS_55	VSS_149	AN1
W40	VSS_56	VSS_150	AN7
W42	VSS_57	VSS_151	AN10
W44	VSS_58	VSS_152	AN13
W46	VSS_59	VSS_153	AN16
W48	VSS_60	VSS_154	AN19
W50	VSS_61	VSS_155	AN22
W52	VSS_62	VSS_156	AN25
W54	VSS_63	VSS_157	AN28
W56	VSS_64	VSS_158	AN31
W58	VSS_65	VSS_159	AN34
W60	VSS_66	VSS_160	AN35
W62	VSS_67	VSS_161	AP5
W64	VSS_68	VSS_162	AR3
W66	VSS_69	VSS_163	AR9
W68	VSS_70	VSS_164	AR9
W70	VSS_71	VSS_165	AR12
W72	VSS_72	VSS_166	AR15
W74	VSS_73	VSS_167	AR18
W76	VSS_74	VSS_168	AR21
W78	VSS_75	VSS_169	AR24
W80	VSS_76	VSS_170	AR27
W82	VSS_77	VSS_171	AR30
W84	VSS_78	VSS_172	AR33
W86	VSS_79	VSS_173	AR36
W88	VSS_80	VSS_174	AR36
W90	VSS_81	VSS_175	AR37
W92	VSS_82	VSS_176	AU1
W94	VSS_83	VSS_177	AU2
W96	VSS_84	VSS_178	AU8
W98	VSS_85	VSS_179	AU11
W100	VSS_86	VSS_180	AU14
W102	VSS_87	VSS_181	AU17
W104	VSS_88	VSS_182	AU20
W106	VSS_89	VSS_183	AU23
W108	VSS_90	VSS_184	AU26
W110	VSS_91	VSS_185	AU29
W112	VSS_92	VSS_186	AU32
W114	VSS_93	VSS_187	AU35
W116	VSS_94	VSS_188	AU35

BCM88470C80IFSBG  
PBGA-37X37-1365

UIK		E32	
A5	SRD_AGND_1	SRD_AGND_69	E32
A6	SRD_AGND_2	SRD_AGND_70	E33
A7	SRD_AGND_3	SRD_AGND_71	E34
A8	SRD_AGND_4	SRD_AGND_72	E35
A9	SRD_AGND_5	SRD_AGND_73	E36
A10	SRD_AGND_6	SRD_AGND_74	E37
A11	SRD_AGND_7	SRD_AGND_75	F1
A12	SRD_AGND_8	SRD_AGND_76	F9
A13	SRD_AGND_9	SRD_AGND_77	F13
A14	SRD_AGND_10	SRD_AGND_78	F17
A15	SRD_AGND_11	SRD_AGND_79	F21
A16	SRD_AGND_12	SRD_AGND_80	F25
A17	SRD_AGND_13	SRD_AGND_81	F29
A18	SRD_AGND_14	SRD_AGND_82	F33
A19	SRD_AGND_15	SRD_AGND_83	F37
A20	SRD_AGND_16	SRD_AGND_84	G1
A21	SRD_AGND_17	SRD_AGND_85	G5
A22	SRD_AGND_18	SRD_AGND_86	G9
A23	SRD_AGND_19	SRD_AGND_87	G13
A24	SRD_AGND_20	SRD_AGND_88	G17
A25	SRD_AGND_21	SRD_AGND_89	G21
A26	SRD_AGND_22	SRD_AGND_90	G25
A27	SRD_AGND_23	SRD_AGND_91	G29
A28	SRD_AGND_24	SRD_AGND_92	G33
A29	SRD_AGND_25	SRD_AGND_93	G37
A30	SRD_AGND_26	SRD_AGND_94	G41
A31	SRD_AGND_27	SRD_AGND_95	H4
A32	SRD_AGND_28	SRD_AGND_96	H8
A33	SRD_AGND_29	SRD_AGND_97	H12
A34	SRD_AGND_30	SRD_AGND_98	H16
A35	SRD_AGND_31	SRD_AGND_99	H20
A36	SRD_AGND_32	SRD_AGND_100	H24
A37	SRD_AGND_33	SRD_AGND_101	H28
A38	SRD_AGND_34	SRD_AGND_102	H32
A39	SRD_AGND_35	SRD_AGND_103	H36
A40	SRD_AGND_36	SRD_AGND_104	H40
A41	SRD_AGND_37	SRD_AGND_105	H44
A42	SRD_AGND_38	SRD_AGND_106	H48
A43	SRD_AGND_39	SRD_AGND_107	H52
A44	SRD_AGND_40	SRD_AGND_108	H56
A45	SRD_AGND_41	SRD_AGND_109	H60
A46	SRD_AGND_42	SRD_AGND_110	H64
A47	SRD_AGND_43	SRD_AGND_111	H68
A48	SRD_AGND_44	SRD_AGND_112	H72
A49	SRD_AGND_45	SRD_AGND_113	H76
A50	SRD_AGND_46	SRD_AGND_114	H80
A51	SRD_AGND_47	SRD_AGND_115	H84
A52	SRD_AGND_48	SRD_AGND_116	J4
A53	SRD_AGND_49	SRD_AGND_117	J8
A54	SRD_AGND_50	SRD_AGND_118	J12
A55	SRD_AGND_51	SRD_AGND_119	J16
A56	SRD_AGND_52	SRD_AGND_120	J20
A57	SRD_AGND_53	SRD_AGND_121	J24
A58	SRD_AGND_54	SRD_AGND_122	J28
A59	SRD_AGND_55	SRD_AGND_123	J32
A60	SRD_AGND_56	SRD_AGND_124	J36
A61	SRD_AGND_57	SRD_AGND_125	K4
A62	SRD_AGND_58	SRD_AGND_126	K8
A63	SRD_AGND_59	SRD_AGND_127	K12
A64	SRD_AGND_60	SRD_AGND_128	K16
A65	SRD_AGND_61	SRD_AGND_129	K20
A66	SRD_AGND_62	SRD_AGND_130	K24
A67	SRD_AGND_63	SRD_AGND_131	K28
A68	SRD_AGND_64	SRD_AGND_132	K32
A69	SRD_AGND_65	SRD_AGND_133	K36
A70	SRD_AGND_66	SRD_AGND_134	K40
A71	SRD_AGND_67	SRD_AGND_135	K44
A72	SRD_AGND_68	SRD_AGND_136	K48
A73	SRD_AGND_68	SRD_AGND_136	K52

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UHL		N26	
K24	SRD_AGND_137	SRD_AGND_205	N26
K26	SRD_AGND_138	SRD_AGND_206	N28
K27	SRD_AGND_139	SRD_AGND_207	N33
K28	SRD_AGND_140	SRD_AGND_208	P5
K29	SRD_AGND_141	SRD_AGND_209	P10
K30	SRD_AGND_142	SRD_AGND_210	P28
K31	SRD_AGND_143	SRD_AGND_211	P33
K32	SRD_AGND_144	SRD_AGND_212	R1
K33	SRD_AGND_145	SRD_AGND_213	R2
K34	SRD_AGND_146	SRD_AGND_214	R5
K35	SRD_AGND_147	SRD_AGND_215	R6
K36	SRD_AGND_148	SRD_AGND_216	R7
K37	SRD_AGND_149	SRD_AGND_217	R10
L1	SRD_AGND_150	SRD_AGND_218	R28
L2	SRD_AGND_151	SRD_AGND_219	R31
L3	SRD_AGND_152	SRD_AGND_220	R32
L4	SRD_AGND_153	SRD_AGND_221	R37
L5	SRD_AGND_154	SRD_AGND_222	R37
L6	SRD_AGND_155	SRD_AGND_223	T3
L7	SRD_AGND_156	SRD_AGND_224	T4
L8	SRD_AGND_157	SRD_AGND_225	T5
L9	SRD_AGND_158	SRD_AGND_226	T8
L10	SRD_AGND_159	SRD_AGND_227	T9
L11	SRD_AGND_160	SRD_AGND_228	T10
L12	SRD_AGND_161	SRD_AGND_229	T28
L13	SRD_AGND_162	SRD_AGND_230	T29
L14	SRD_AGND_163	SRD_AGND_231	T30
L15	SRD_AGND_164	SRD_AGND_232	T31
L16	SRD_AGND_165	SRD_AGND_233	T33
L17	SRD_AGND_166	SRD_AGND_234	T34
L18	SRD_AGND_167	SRD_AGND_235	T35
L19	SRD_AGND_168	SRD_AGND_236	U5
L20	SRD_AGND_169	SRD_AGND_237	U10
L21	SRD_AGND_170	SRD_AGND_238	U33
L22	SRD_AGND_171	SRD_AGND_239	V5
L23	SRD_AGND_172	SRD_AGND_240	V10
L24	SRD_AGND_173	SRD_AGND_241	V33
L25	SRD_AGND_174	SRD_AGND_242	W1
L26	SRD_AGND_175	SRD_AGND_243	W2
L27	SRD_AGND_176	SRD_AGND_244	W5
L28	SRD_AGND_177	SRD_AGND_245	W6
L29	SRD_AGND_178	SRD_AGND_246	W7
L30	SRD_AGND_179	SRD_AGND_247	W10
L31	SRD_AGND_180	SRD_AGND_248	W28
L32	SRD_AGND_181	SRD_AGND_249	W29
L33	SRD_AGND_182	SRD_AGND_250	W36
L34	SRD_AGND_183	SRD_AGND_251	Y1
L35	SRD_AGND_184	SRD_AGND_252	Y2
L36	SRD_AGND_185	SRD_AGND_253	Y3
L37	SRD_AGND_186	SRD_AGND_254	Y4
L38	SRD_AGND_187	SRD_AGND_255	Y5
L39	SRD_AGND_188	SRD_AGND_256	Y7
L40	SRD_AGND_189	SRD_AGND_257	Y8
L41	SRD_AGND_190	SRD_AGND_258	Y9
L42	SRD_AGND_191	SRD_AGND_259	Y10
L43	SRD_AGND_192	SRD_AGND_260	Y27
L44	SRD_AGND_193	SRD_AGND_261	Y29
L45	SRD_AGND_194	SRD_AGND_262	Y33
L46	SRD_AGND_195	SRD_AGND_263	Y34
L47	SRD_AGND_196	SRD_AGND_264	Y35
L48	SRD_AGND_197	SRD_AGND_265	Y36
L49	SRD_AGND_198	SRD_AGND_266	Y37
L50	SRD_AGND_199	SRD_AGND_267	Y38
L51	SRD_AGND_200	SRD_AGND_268	Y39
L52	SRD_AGND_201	SRD_AGND_269	Y40
L53	SRD_AGND_202	SRD_AGND_270	AA6
L54	SRD_AGND_203	SRD_AGND_271	AA28
L55	SRD_AGND_204	SRD_AGND_271	AA29

BCM88470C80IFSBG  
PBGA-37X37-1365

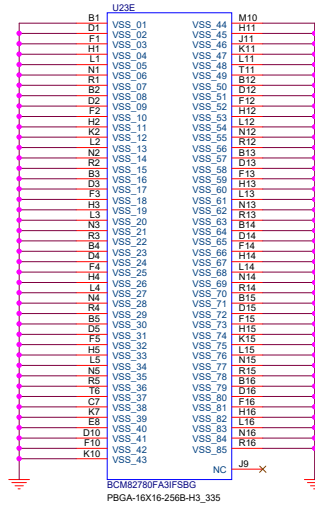
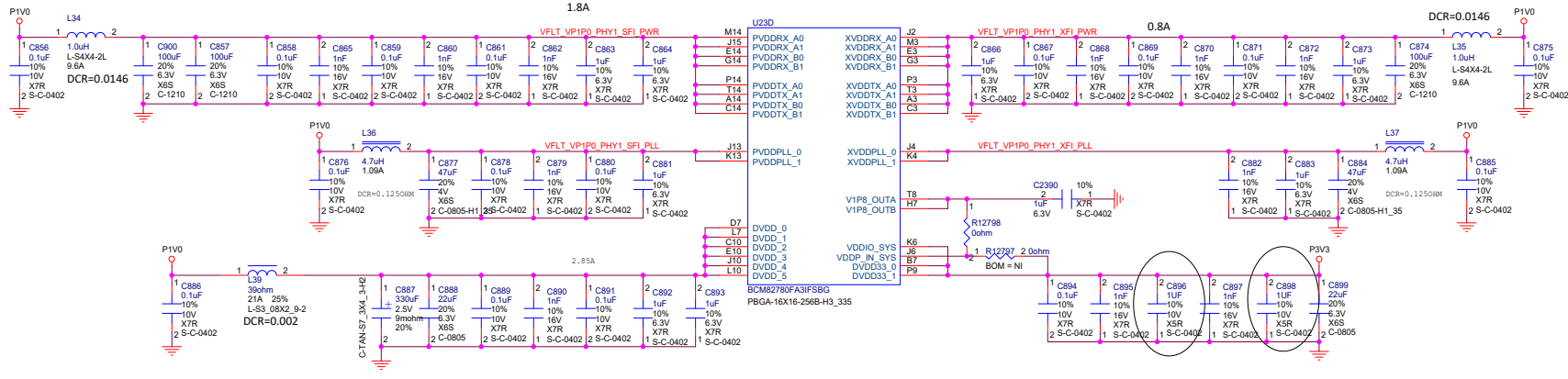
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<b>Ufi Space Co., Ltd.</b>		<b>CONFIDENTIAL</b>
Title <b>CSGR MAINBOARD</b>		
Size <b>C</b>	Document Number <b>T990089T00</b>	Rev <b>07XB1</b>
Date: <b>15/10/16</b>	Thursday, January 31, 2019	Sheet 16 of 75

# MAC\_BCM88470\_GND





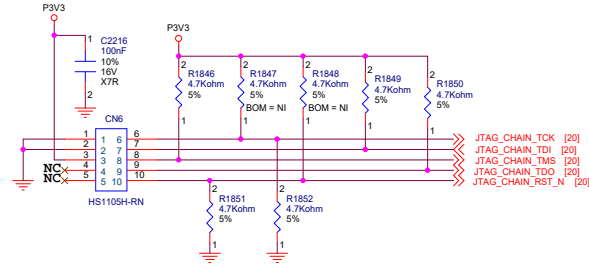


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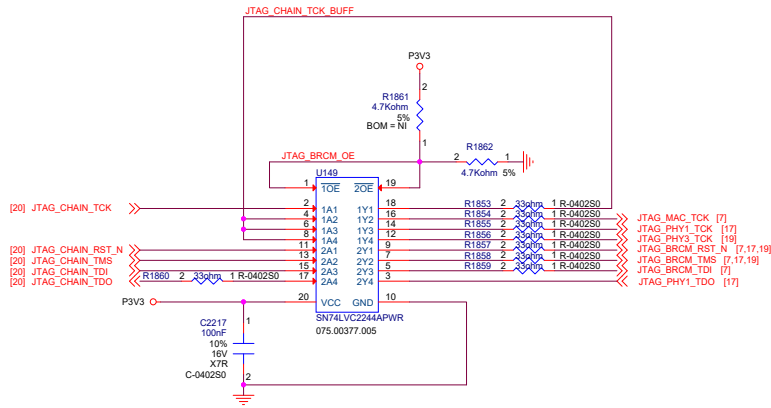
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Title CSGR MAINBOARD		
Size C	Document Number Project: T990089T00	Rev 07XB1
Date: 15/10/16	Thursday, January 31, 2019	Sheet 18 of 75

# PHY1\_BCM82780\_PWR & GND



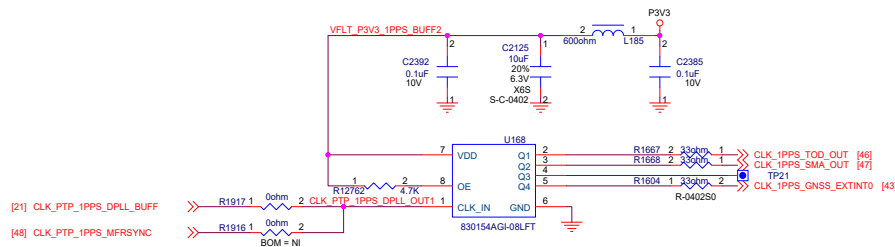
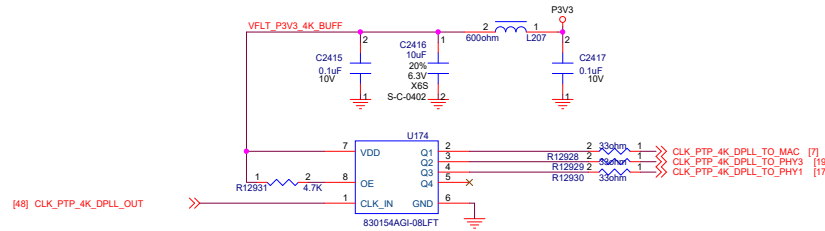
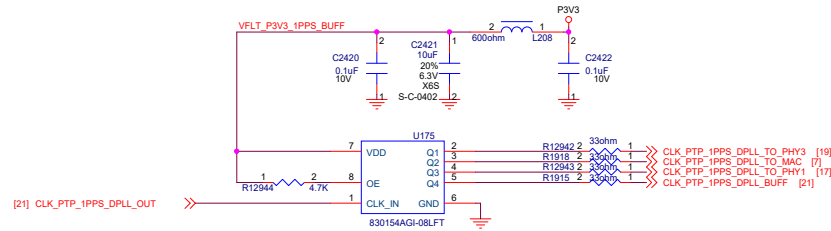
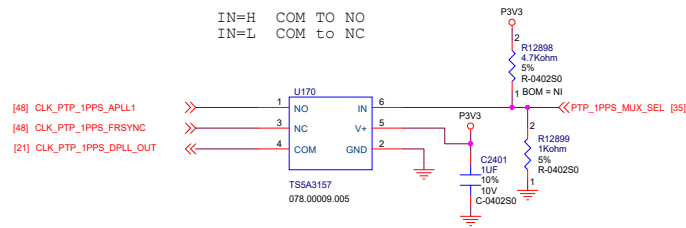


BRCM CHIPS PCSCAN CHAIN



# CHIPSET JTAG CHAIN

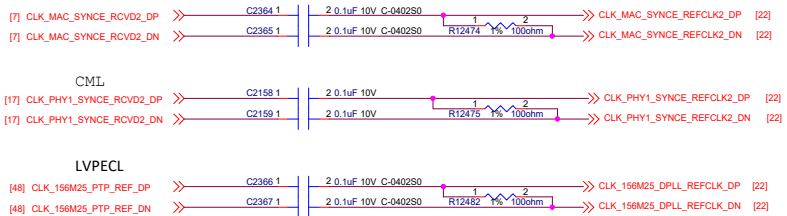
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Title CSGR MAINBOARD		
Size C	Document Number T990089T00	Rev 07XB1
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<Core Design>

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Title CSGR MAINBOARD		
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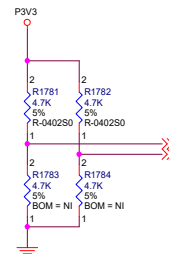
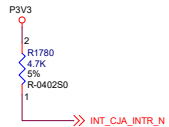
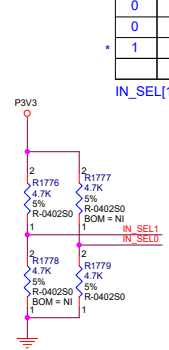
# CLOCK BUFFER1\_1PPS & 4K



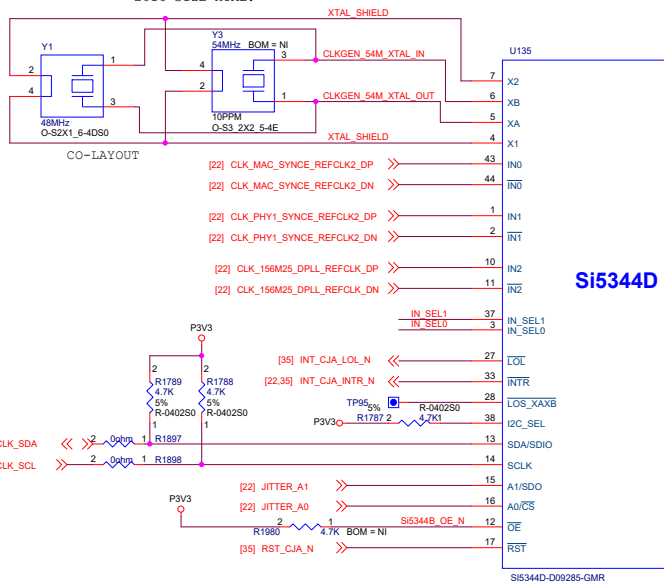
IN_SEL[1:0]	Selected Input
0 0	IN0
0 1	IN1
1 0	IN2

IN\_SEL[1:0] : Internal pulled up

An internal register bit selects XTAL or REFCLK mode. Default is XTAL mode.  
NEED CHANGE TO 48MHZ  
2016 SIZE XTAL.

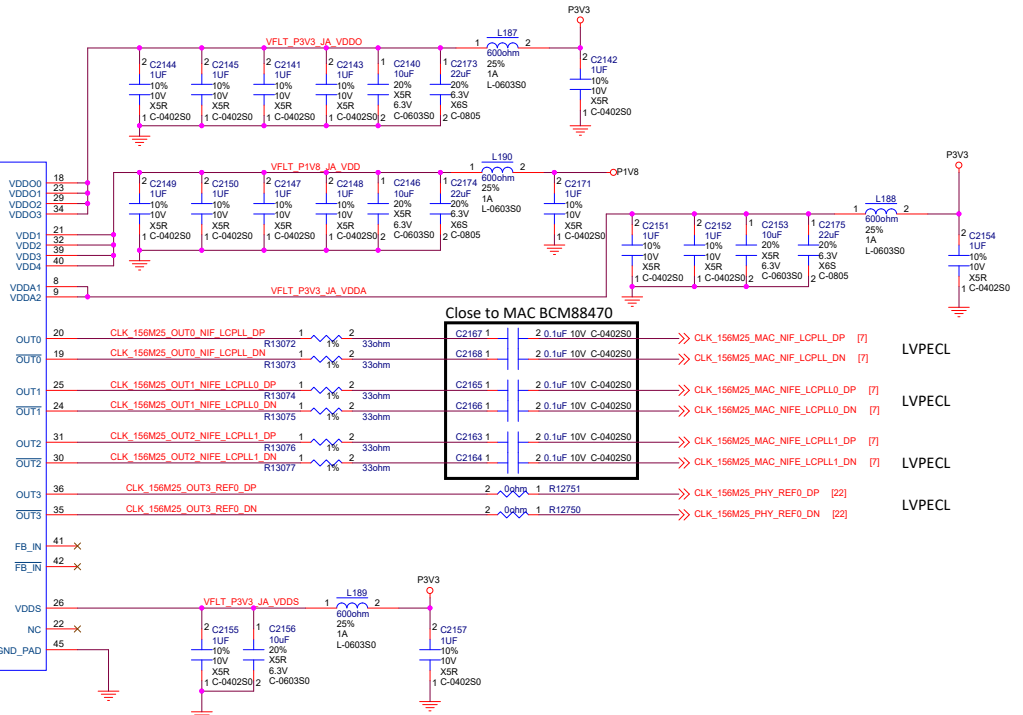


I2C address: 11010 A1 A0 : 0x6B

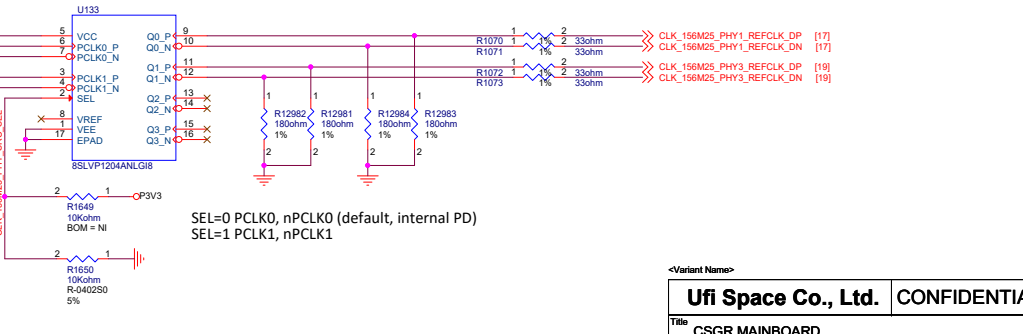


/OE : Internal pulled low  
/RST : Internal pulled up

RST pin is internally pulled up with a ~20 kΩ resistor to the voltage selected by the IO\_VDD\_SEL bit



Close to MAC BCM88470



SEL=0 PCLK0, nPCLK0 (default, internal PD)  
SEL=1 PCLK1, nPCLK1

<Variant Name>

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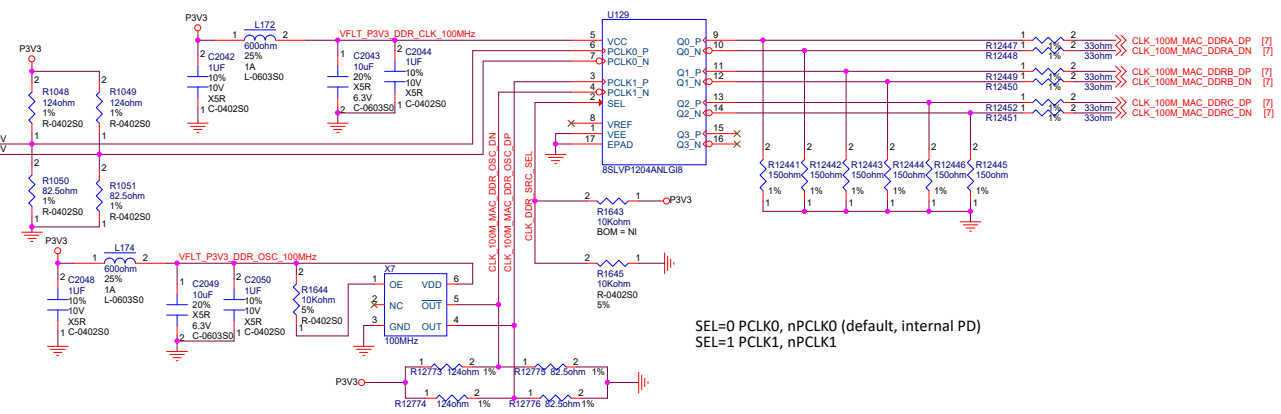
Title: **CSGR MAINBOARD**

Size: C Document Number: **T990089T00** Rev: **07XB1**

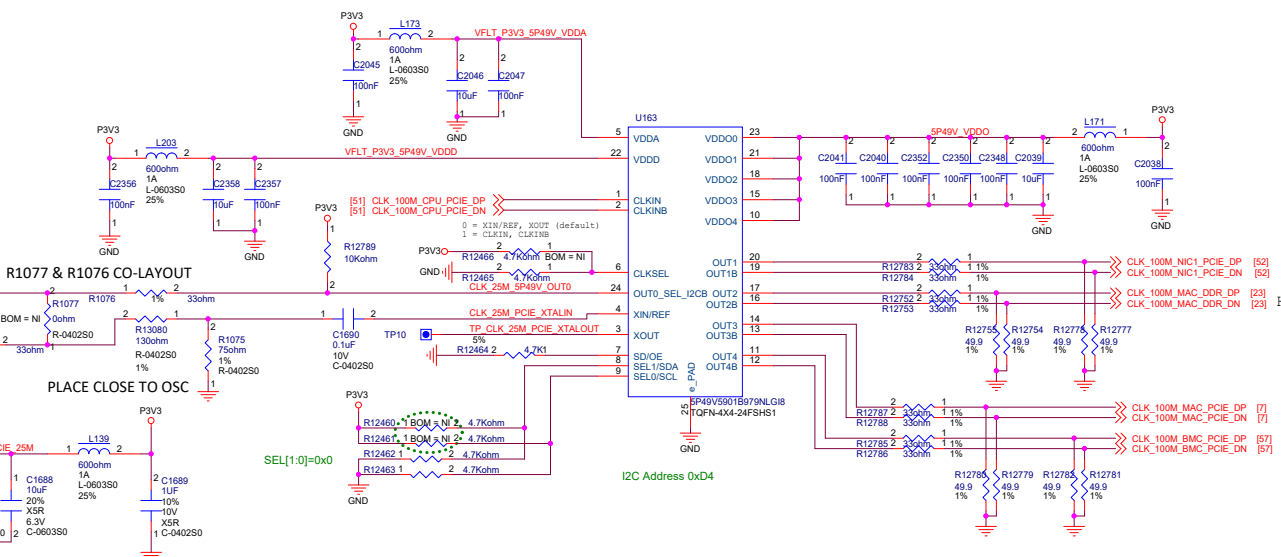
Date: 15.10.17 Thursday, January 31, 2019 Sheet 22 of 75

# CLOCK BUFFER2\_156.25M

[23] CLK\_100M\_MAC\_DDR\_DP  
[23] CLK\_100M\_MAC\_DDR\_DN



SEL=0 PCLK0, nPCLK0 (default, internal PD)  
SEL=1 PCLK1, nPCLK1



R1077 & R1076 CO-LAYOUT

PLACE CLOSE TO OSC

I2C Address 0x04

ENABLE CONTROL VDD OUT  
25MHz  
140.00245.005  
O-3\_2X2\_5-4J50

OSC\_PCIE\_25M OE

R1074 4.7kOhm  
R-040250 5%

C1687 100nF  
C1688 100nF  
C1689 100nF

C2051 25%  
C2052 25%  
C2053 25%

R1079 124ohm  
R-040250 1%

R1080 124ohm  
R-040250 1%

R1081 82.5ohm  
R-040250 1%

R1082 82.5ohm  
R-040250 1%

R1647 10kOhm  
R-040250 5%

R1648 10kOhm  
R-040250 5%

R1649 10kOhm  
R-040250 5%

R1650 10kOhm  
R-040250 5%

R1651 10kOhm  
R-040250 5%

R1652 10kOhm  
R-040250 5%

R1653 10kOhm  
R-040250 5%

R1654 10kOhm  
R-040250 5%

R1655 10kOhm  
R-040250 5%

R1656 10kOhm  
R-040250 5%

R1657 10kOhm  
R-040250 5%

R1658 10kOhm  
R-040250 5%

R1659 10kOhm  
R-040250 5%

R1660 10kOhm  
R-040250 5%

R1661 10kOhm  
R-040250 5%

R1662 10kOhm  
R-040250 5%

R1663 10kOhm  
R-040250 5%

R1664 10kOhm  
R-040250 5%

R1665 10kOhm  
R-040250 5%

R1666 10kOhm  
R-040250 5%

R1667 10kOhm  
R-040250 5%

R1668 10kOhm  
R-040250 5%

R1669 10kOhm  
R-040250 5%

R1670 10kOhm  
R-040250 5%

R1671 10kOhm  
R-040250 5%

R1672 10kOhm  
R-040250 5%

R1673 10kOhm  
R-040250 5%

R1674 10kOhm  
R-040250 5%

R1675 10kOhm  
R-040250 5%

R1676 10kOhm  
R-040250 5%

R1677 10kOhm  
R-040250 5%

R1678 10kOhm  
R-040250 5%

R1679 10kOhm  
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R1680 10kOhm  
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R1681 10kOhm  
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R1688 10kOhm  
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R1690 10kOhm  
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R1691 10kOhm  
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R1692 10kOhm  
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R1693 10kOhm  
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R1694 10kOhm  
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R1695 10kOhm  
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R1696 10kOhm  
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R1697 10kOhm  
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R1698 10kOhm  
R-040250 5%

R1699 10kOhm  
R-040250 5%

R1700 10kOhm  
R-040250 5%

R1701 10kOhm  
R-040250 5%

R1702 10kOhm  
R-040250 5%

R1703 10kOhm  
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R1704 10kOhm  
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R1705 10kOhm  
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R1711 10kOhm  
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R1772 10kOhm  
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R1773 10kOhm  
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R1774 10kOhm  
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R1775 10kOhm  
R-040250 5%

R1776 10kOhm  
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R1779 10kOhm  
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R1789 10kOhm  
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R1790 10kOhm  
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R1792 10kOhm  
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R1793 10kOhm  
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R1794 10kOhm  
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R1795 10kOhm  
R-040250 5%

R1796 10kOhm  
R-040250 5%

R1797 10kOhm  
R-040250 5%

R1798 10kOhm  
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R1800 10kOhm  
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R1801 10kOhm  
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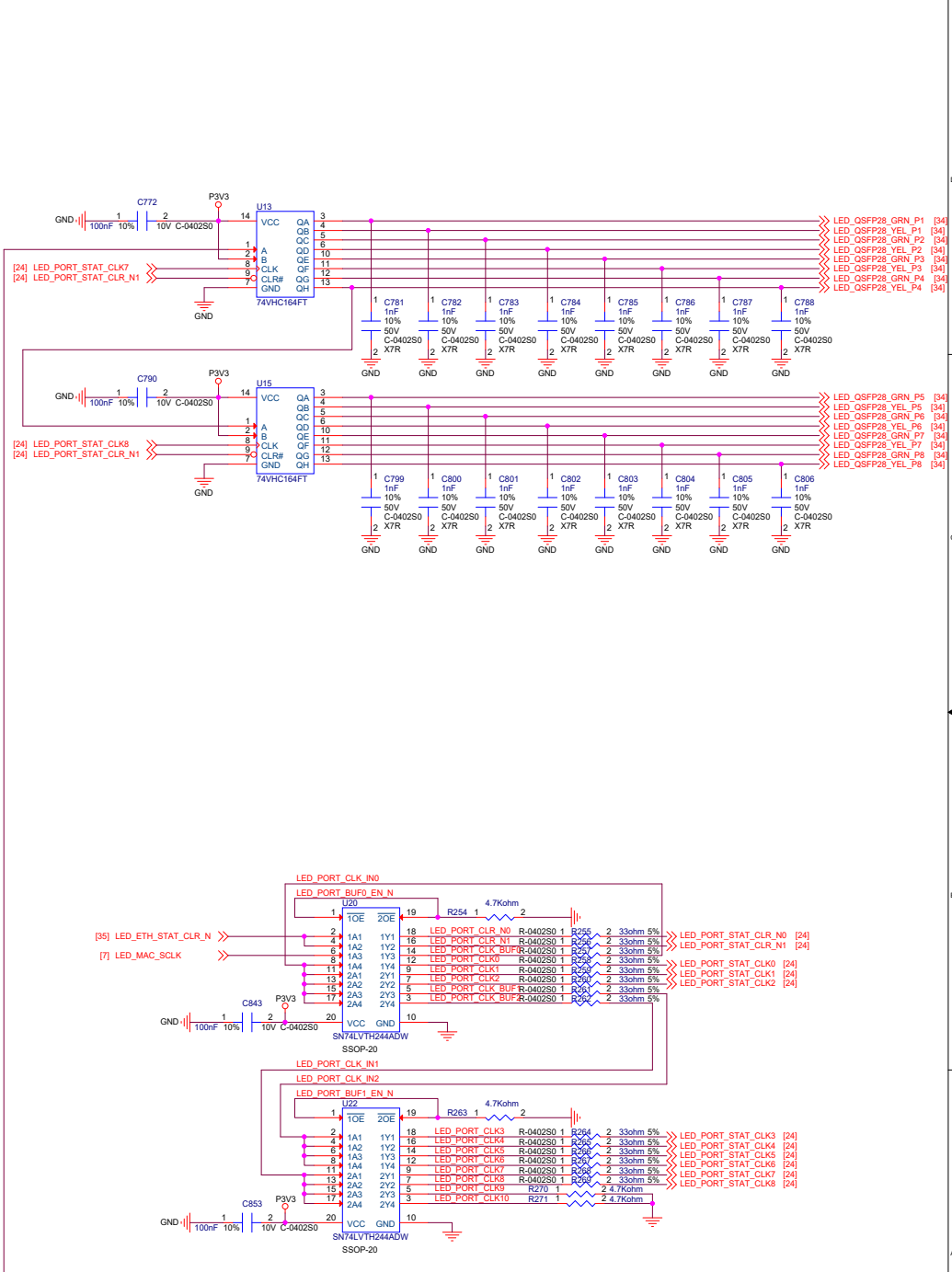
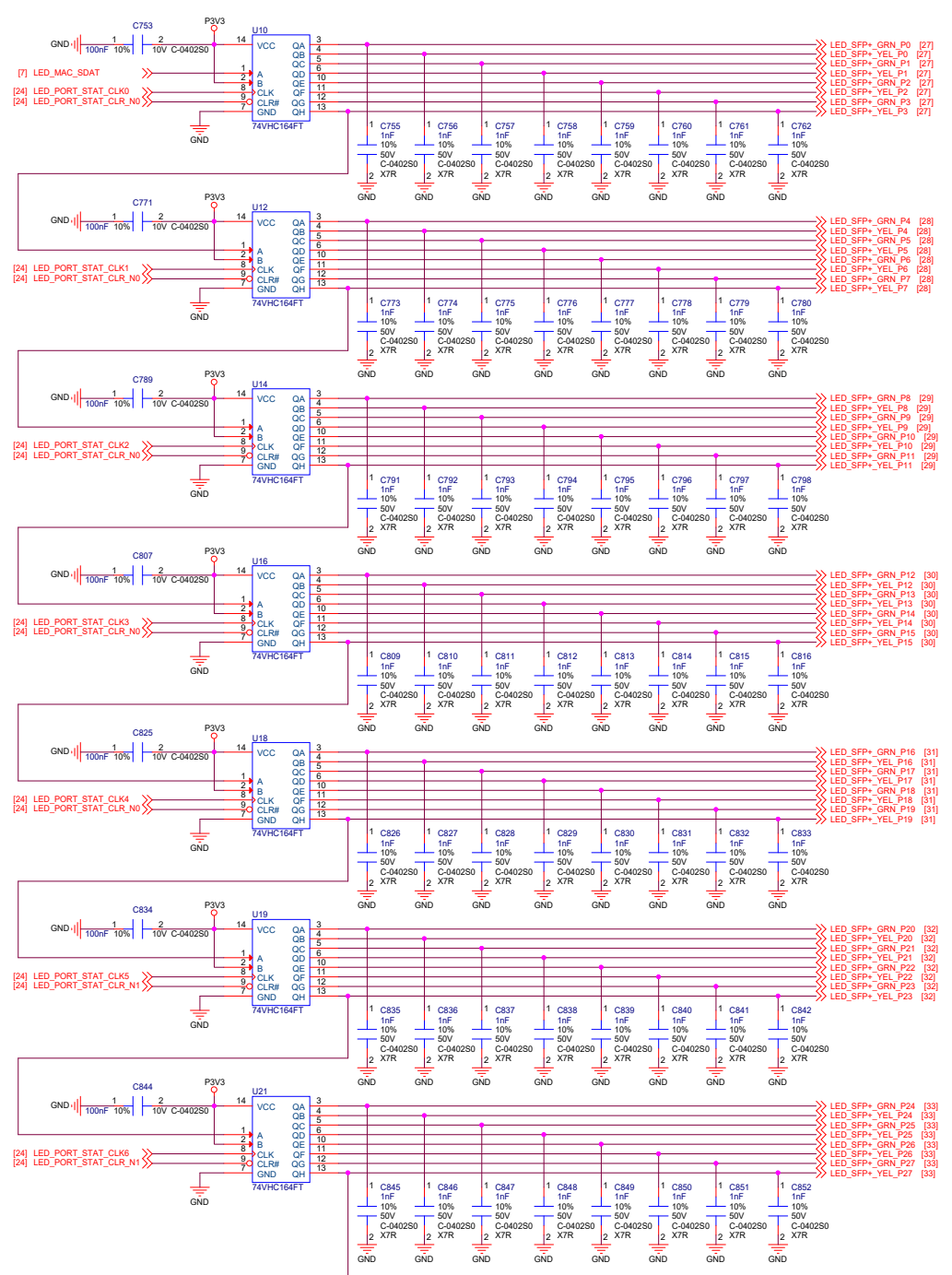
R1802 10kOhm  
R-040250 5%

R1803 10kOhm  
R-040250 5%

R1804 10kOhm  
R-040250 5%

R1805 10kOhm  
R-040250 5%

# PORT STATUS LED CONTROL



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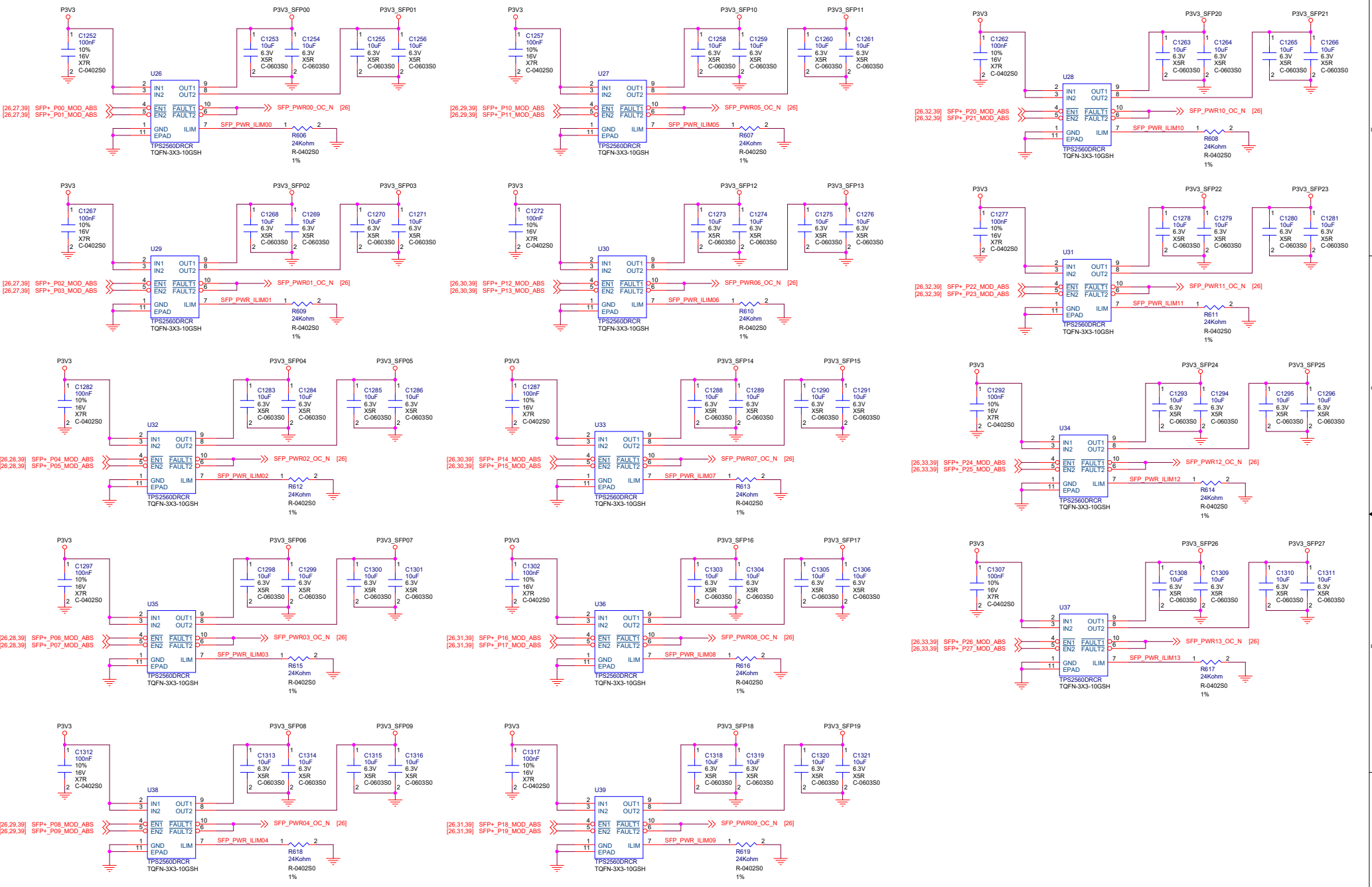
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Title: **CSGR MAINBOARD**

Size: **C** Document Number: **T990089T00** Rev: **07X81**

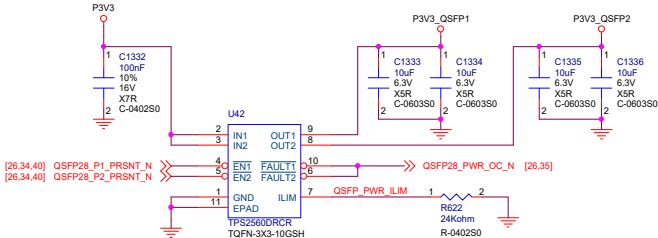
Date: **15.10.16** Thursday, January 31, 2019 Sheet **24** of **75**





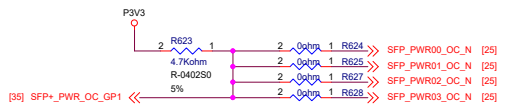
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<b>Ufi Space Co., Ltd.</b>		<b>CONFIDENTIAL</b>	
Title <b>CSGR MAINBOARD</b>			
Size C	Document Number <b>T990089T00</b>	Rev 07XB1	
Date: 15.10.16	Thursday, January 31, 2019	Sheet 25 of 75	

# FIBER PORTS PWR SWITCH1

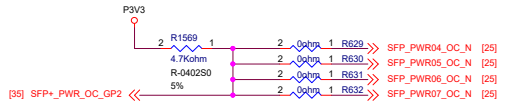


[26.34.40] OSFP28\_P1\_PRSNT\_N  
[26.34.40] OSFP28\_P2\_PRSNT\_N

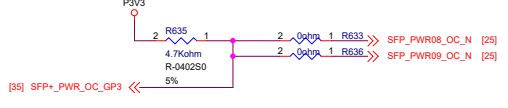
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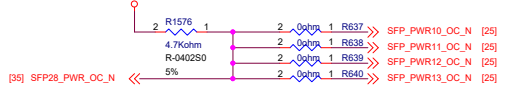
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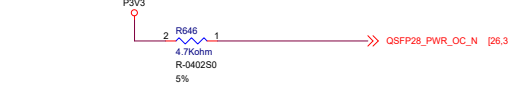
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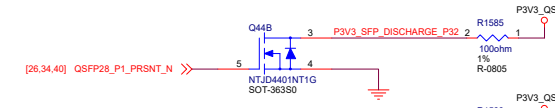
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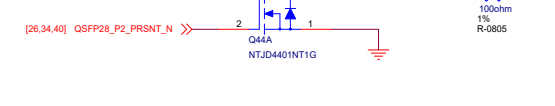
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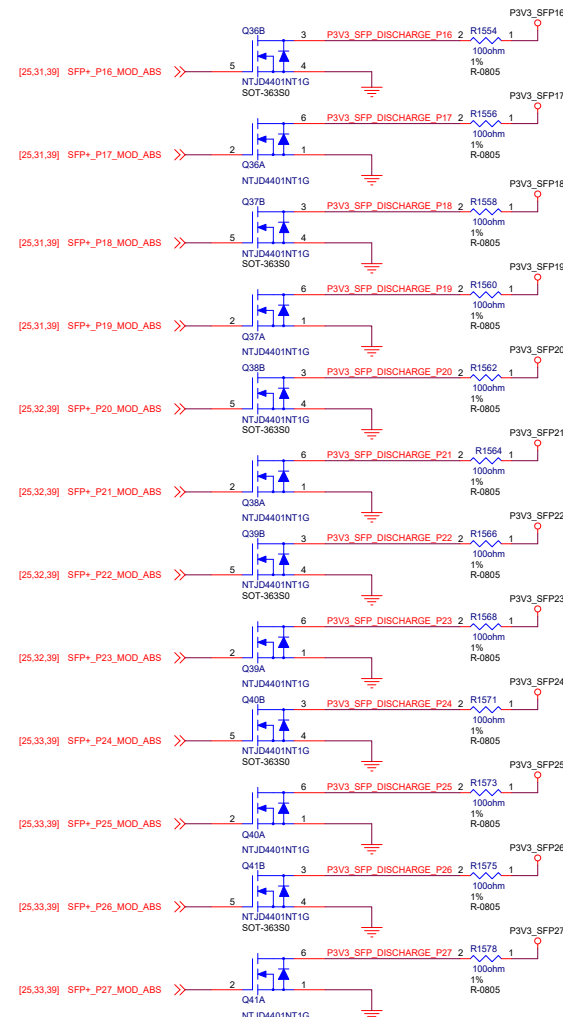
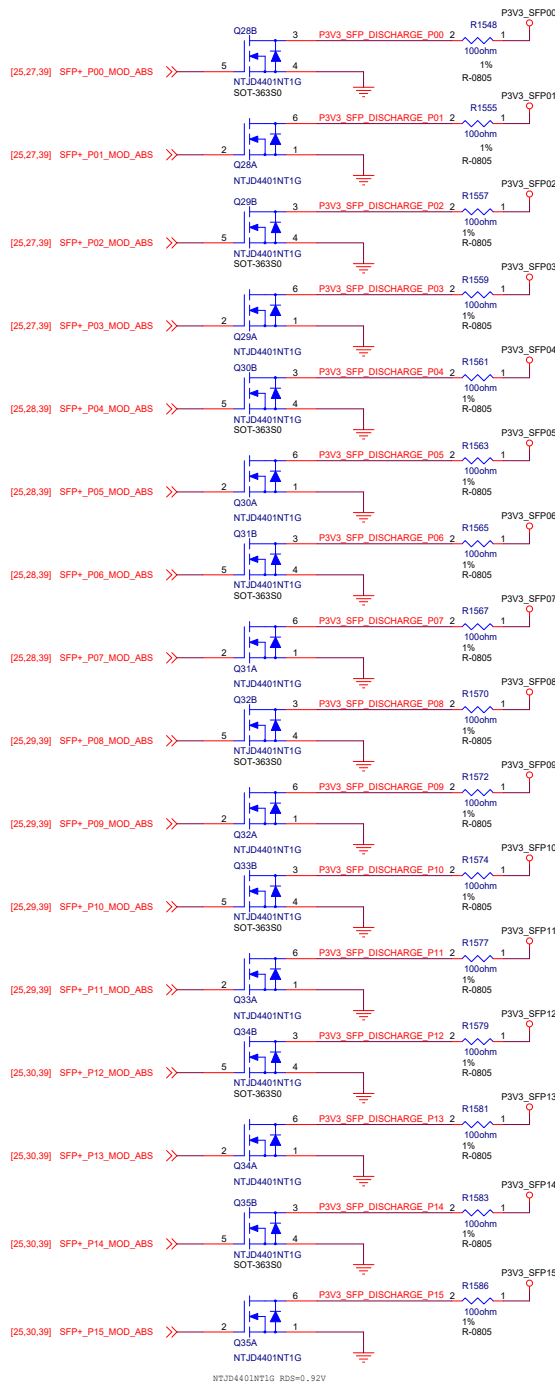
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[26.34.40] OSFP28\_P2\_PRSNT\_N

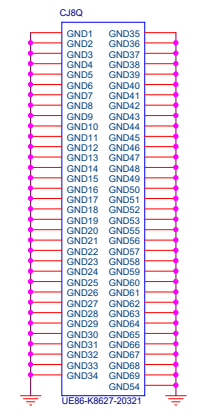
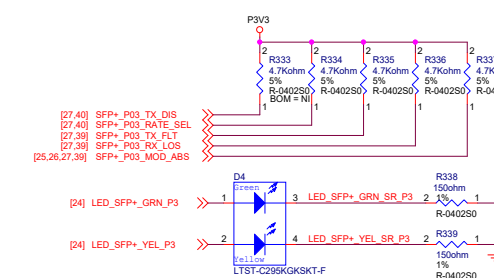
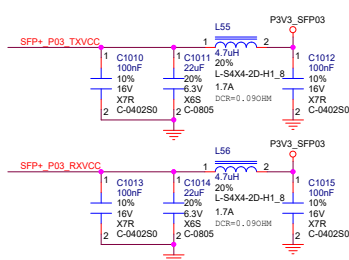
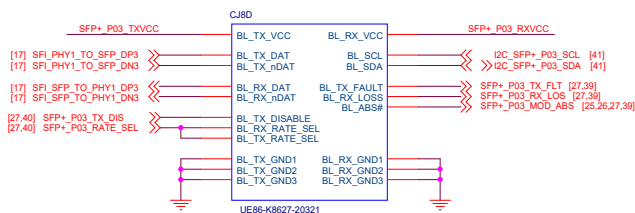
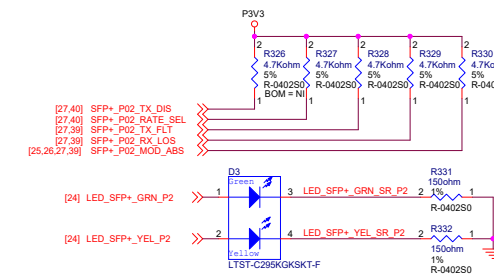
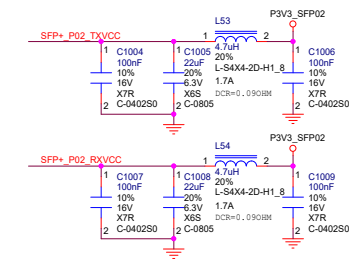
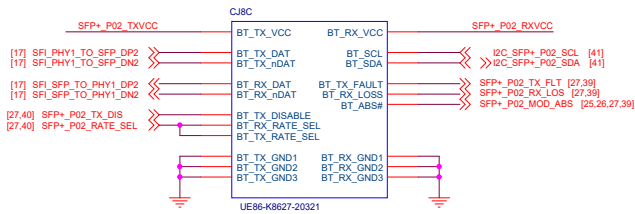
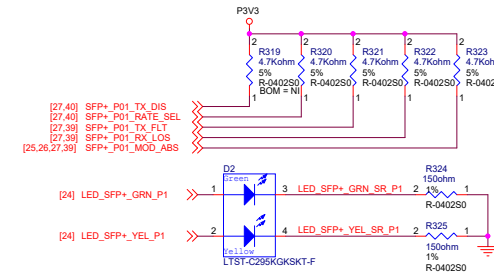
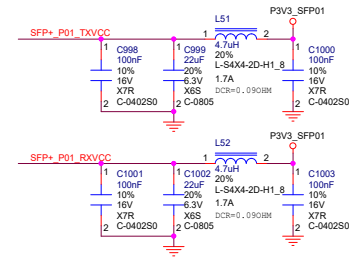
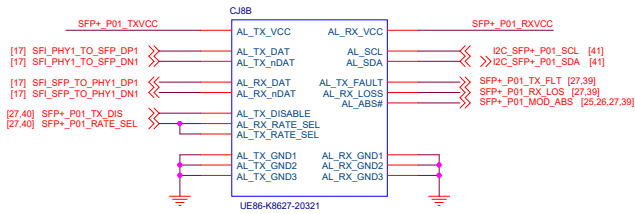
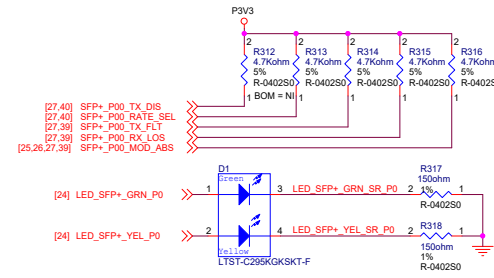
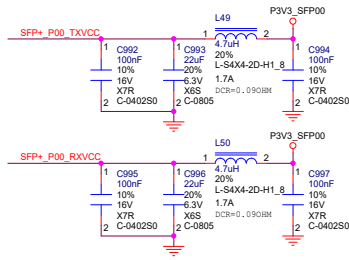
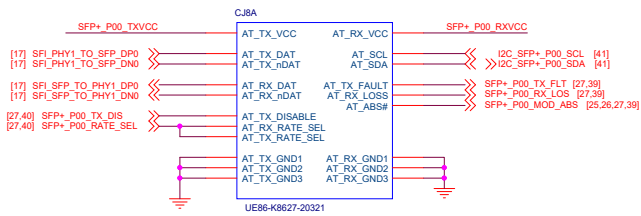


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<b>Ufi Space Co., Ltd.</b>		<b>CONFIDENTIAL</b>
Title CSGR MAINBOARD		
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# FIBER PORTS PWR SWITCH2

Footprint???



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<Core Design>

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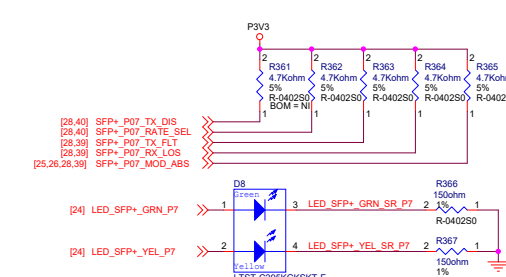
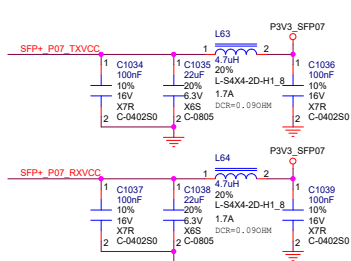
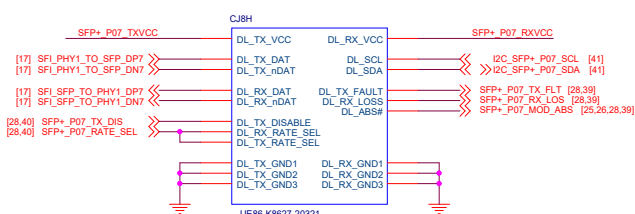
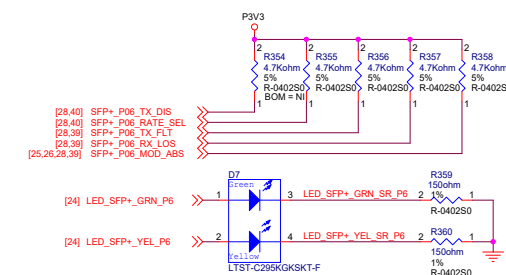
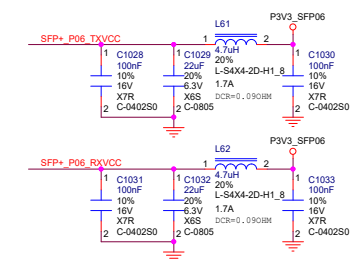
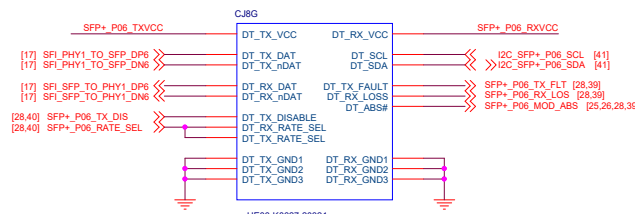
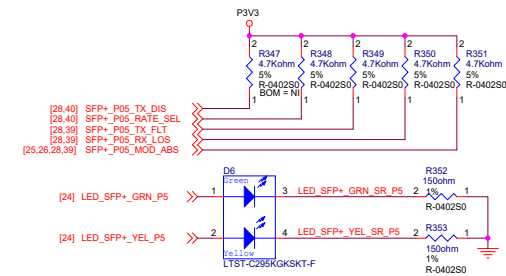
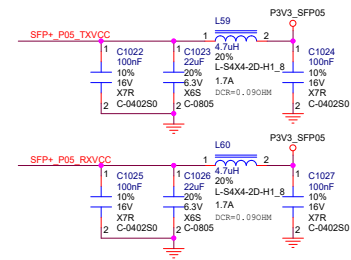
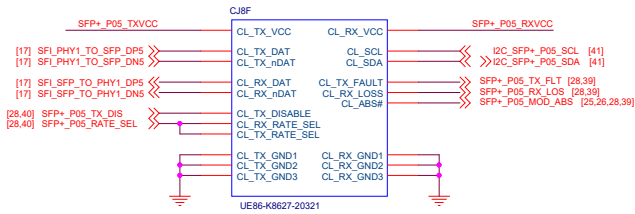
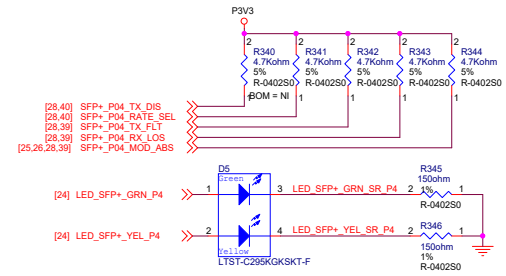
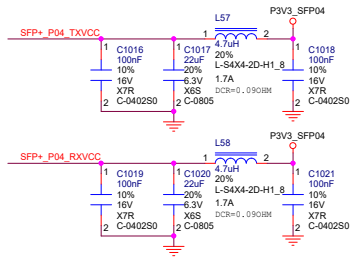
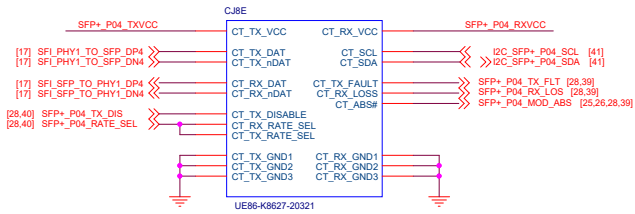
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C: Project: **T990089T00** Rev: 07XB1

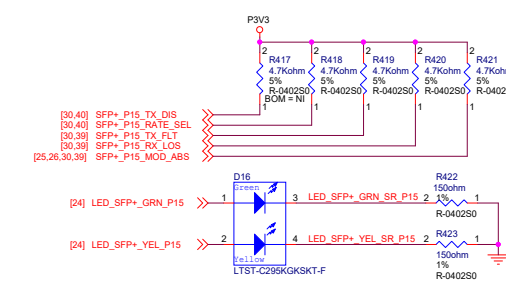
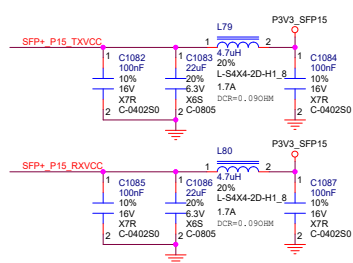
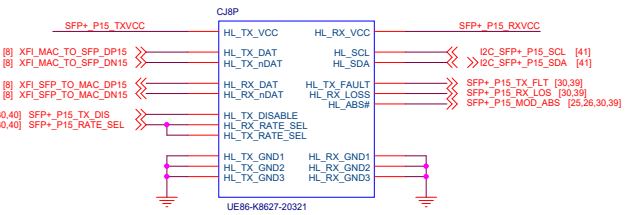
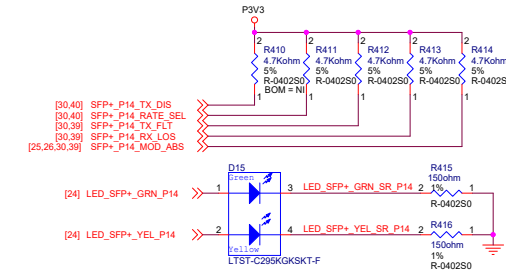
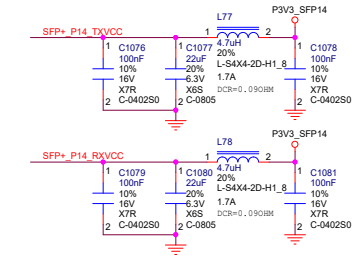
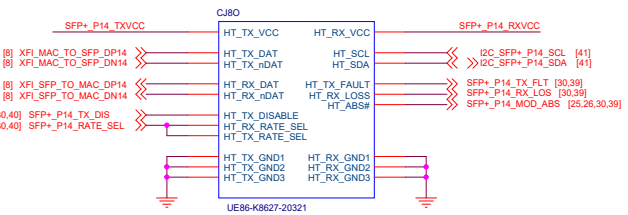
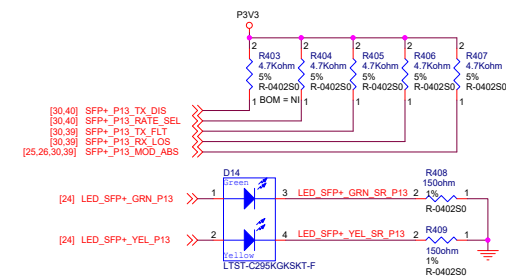
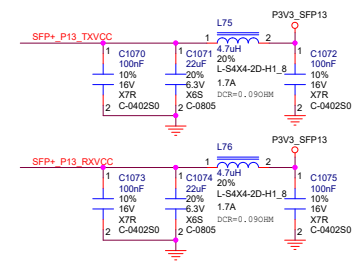
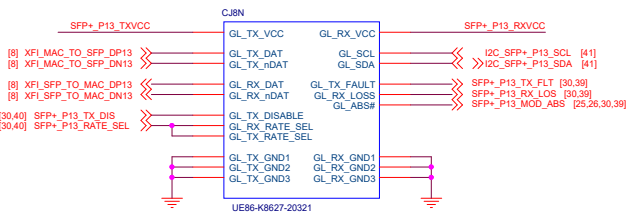
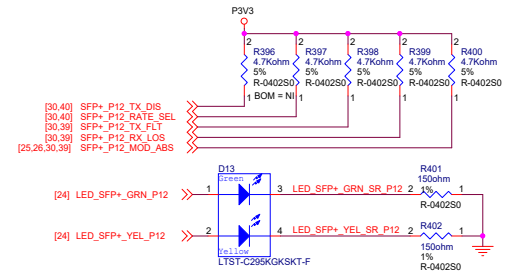
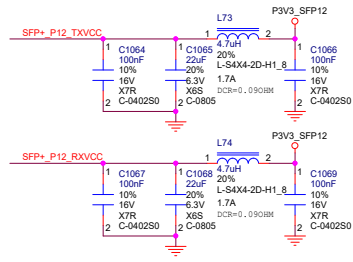
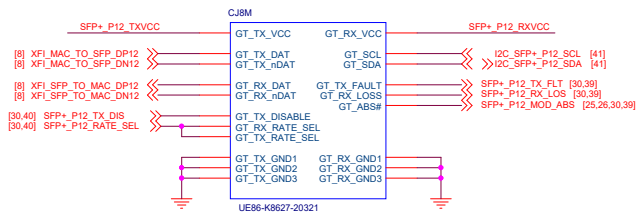
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# 2x8 SFP+ CONN1\_P01~P04



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1	3	5	7	9	11	13	15	17	19	21	23	25	27	Z1
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<Core Design>

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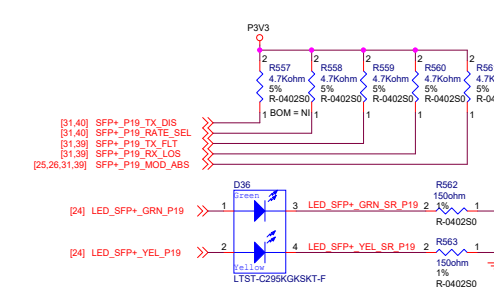
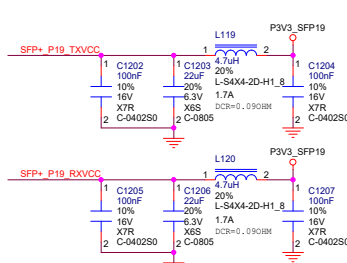
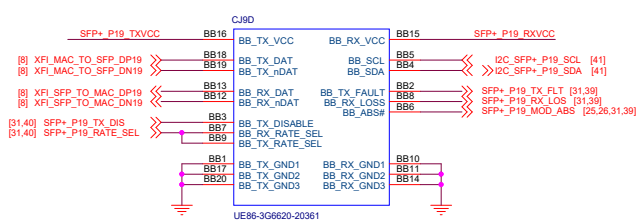
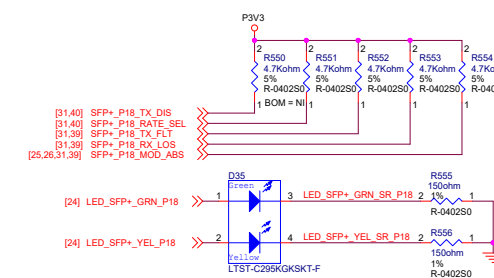
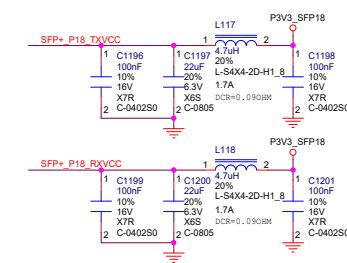
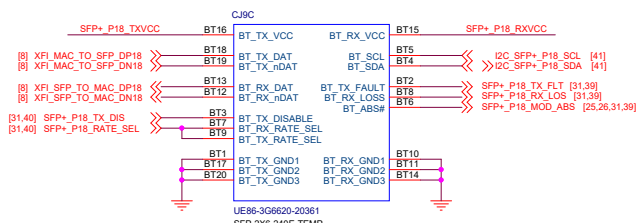
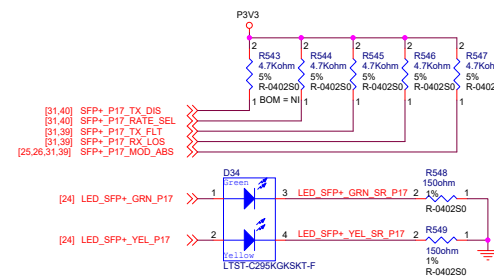
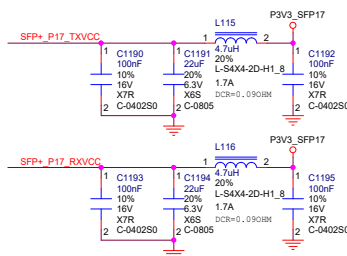
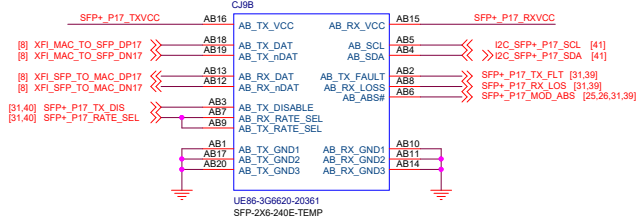
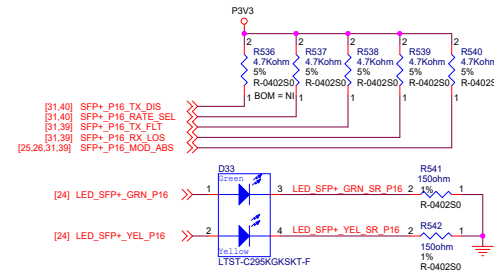
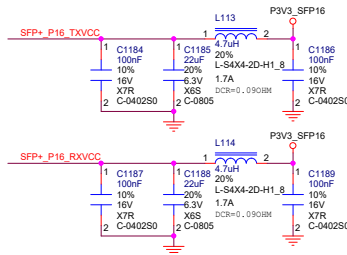
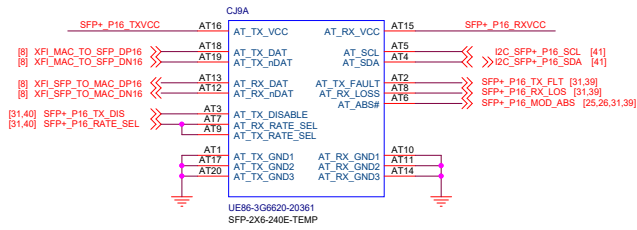
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# 2x8 SFP+ CONN1\_P13~P16

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S2	GND2	GND52	S52
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S4	GND4	GND54	S54
S5	GND5	GND55	S55
S6	GND6	GND56	S56
S7	GND7	GND57	S57
S8	GND8	GND58	S58
S9	GND9	GND59	S59
S10	GND10	GND60	S60
S11	GND11	GND61	S61
S12	GND12	GND62	S62
S13	GND13	GND63	S63
S14	GND14	GND64	S64
S15	GND15	GND65	S65
S16	GND16	GND66	S66
S17	GND17	GND67	S67
S18	GND18	GND68	S68
S19	GND19	GND69	S69
S20	GND20	GND70	S70
S21	GND21	GND71	S71
S22	GND22	GND72	S72
S23	GND23	GND73	S73
S24	GND24	GND74	S74
S25	GND25	GND75	S75
S26	GND26	GND76	S76
S27	GND27	GND77	S77
S28	GND28	GND78	S78
S29	GND29	GND79	S79
S30	GND30	GND80	S80
S31	GND31	GND81	S81
S32	GND32	GND82	S82
S33	GND33	GND83	S83
S34	GND34	GND84	S84
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S46	GND46	GND96	S96
S47	GND47	GND97	S97
S48	GND48	GND98	S98
S49	GND49	GND99	S99
S50	GND50	GND99	S99

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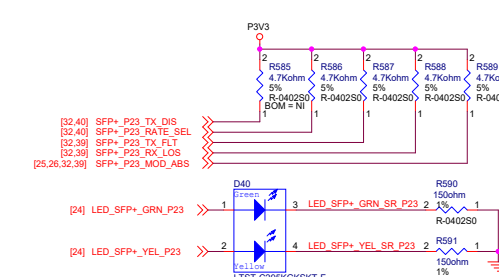
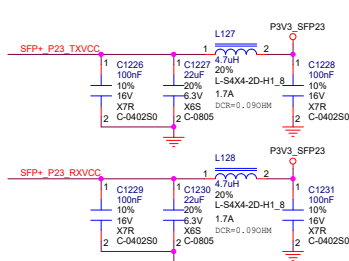
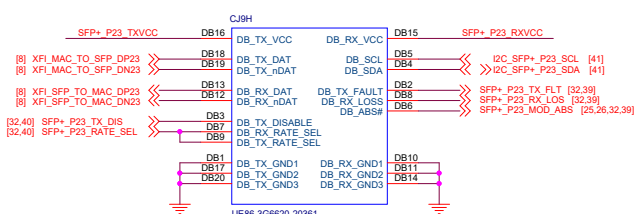
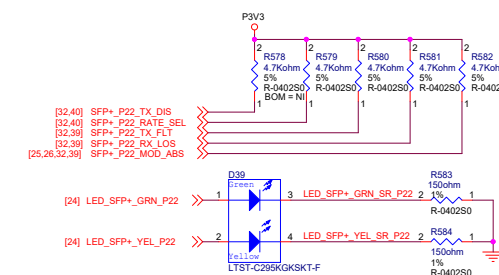
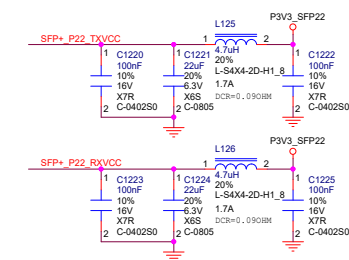
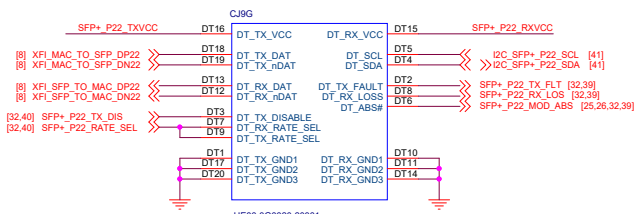
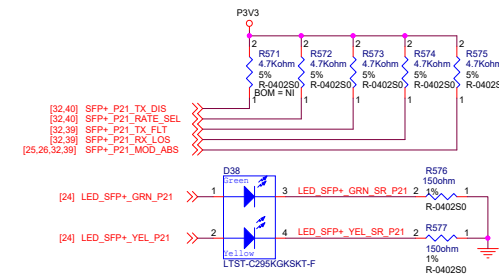
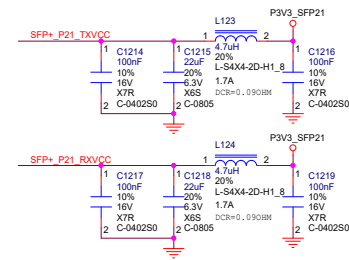
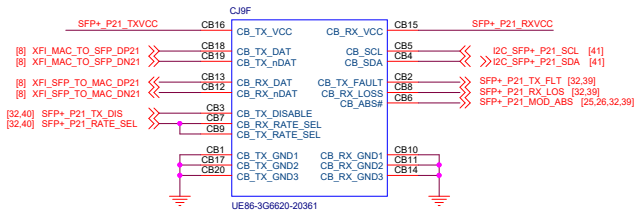
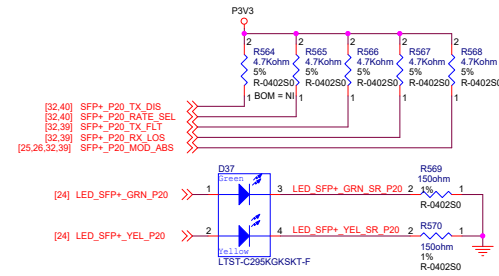
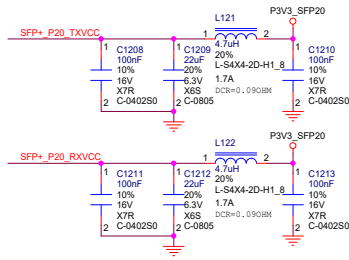
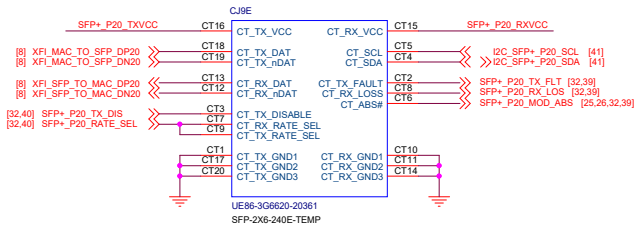
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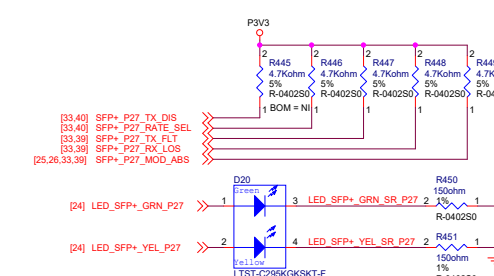
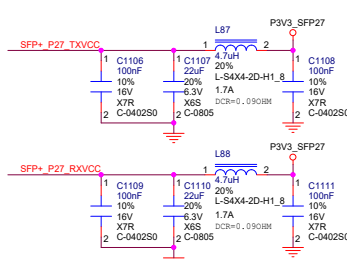
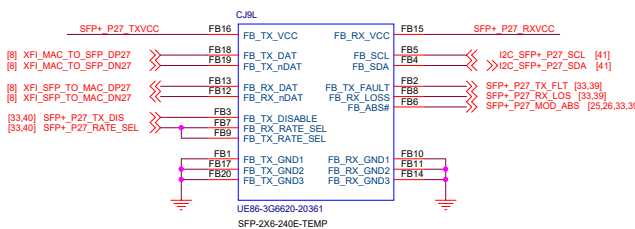
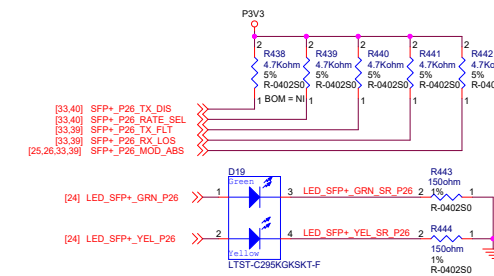
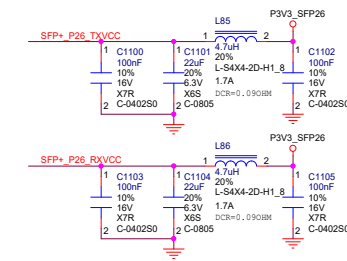
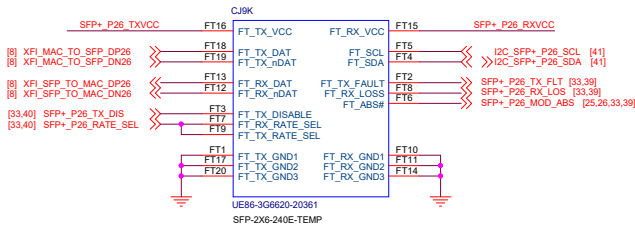
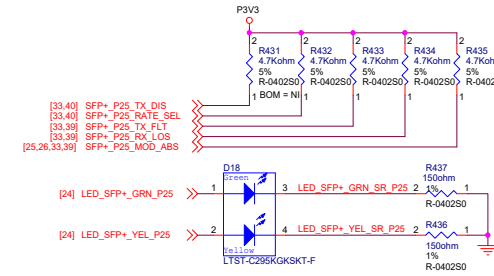
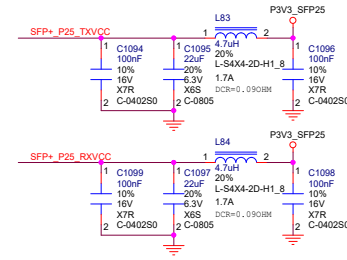
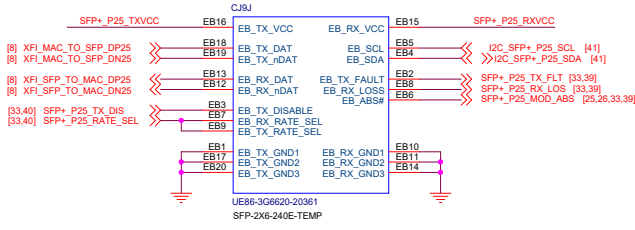
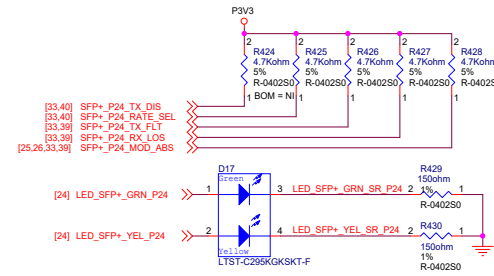
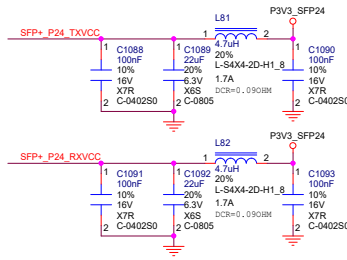
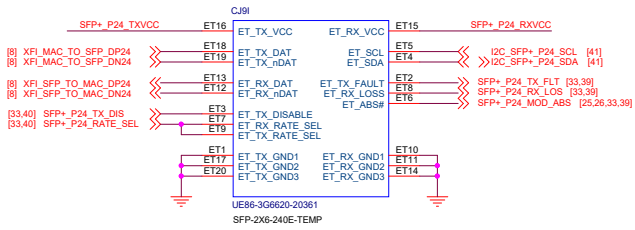
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2x6 SFP28\_CONN2\_P17~P20

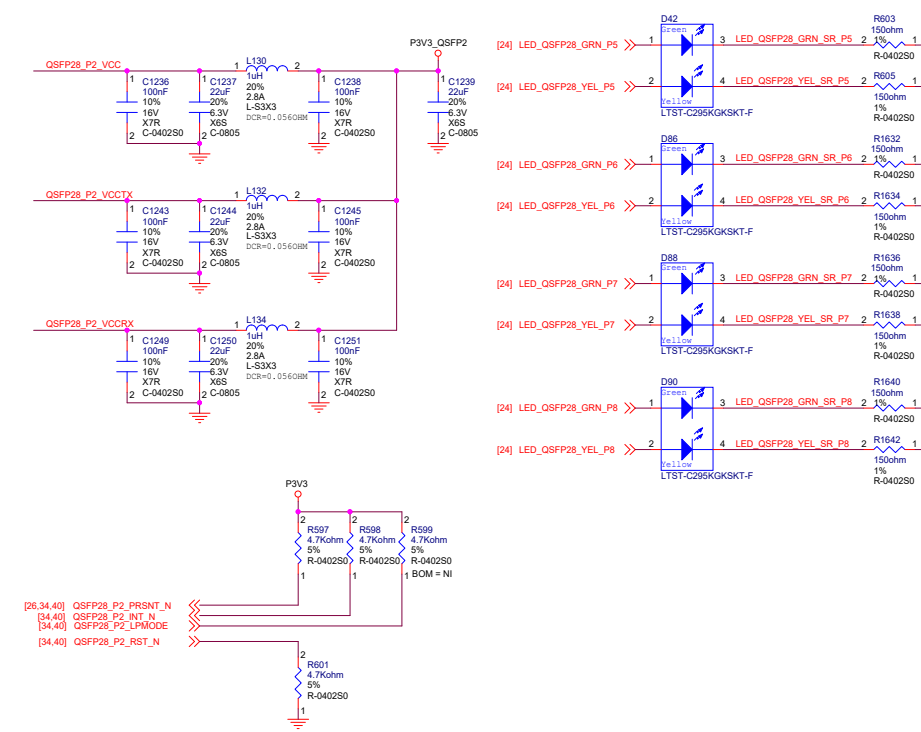
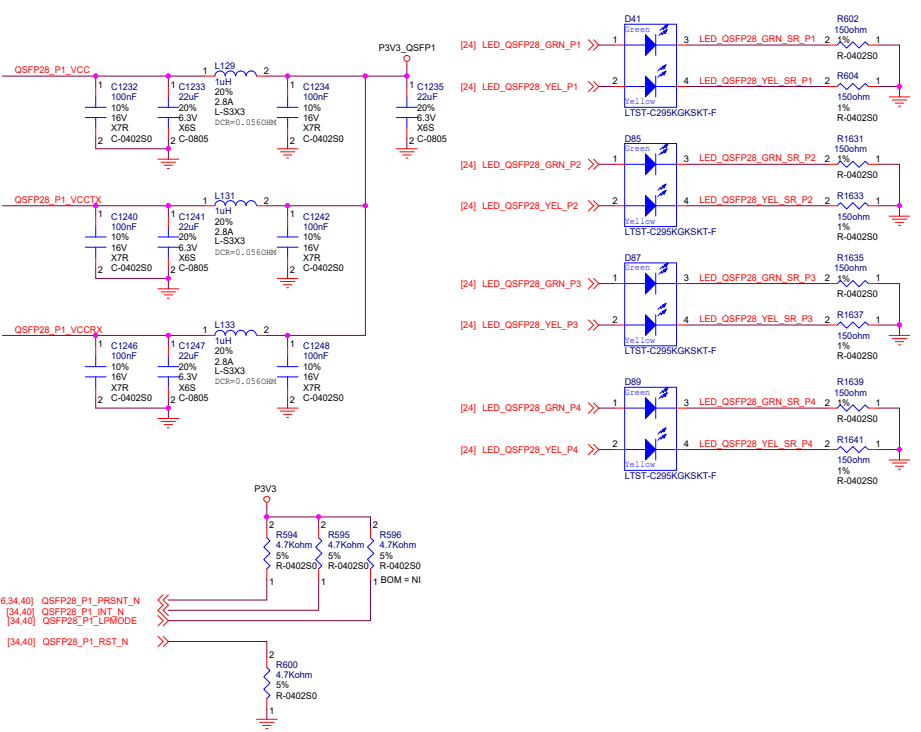
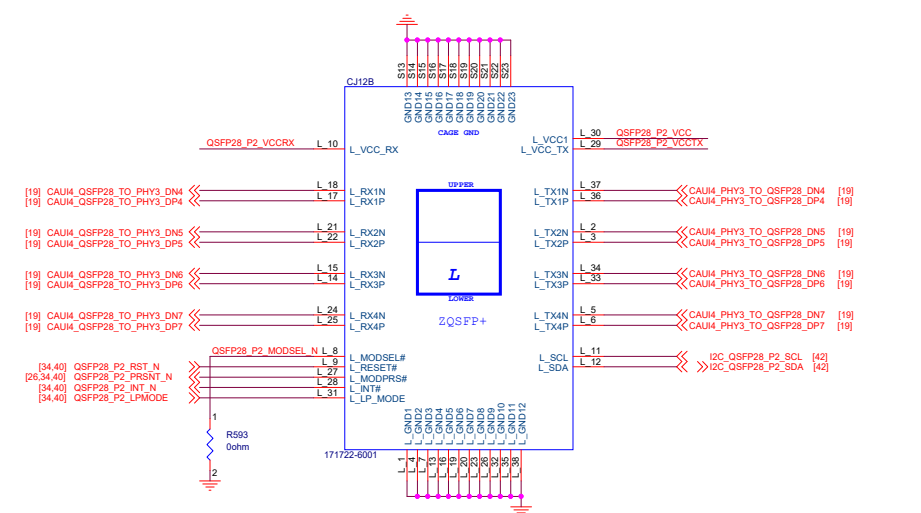
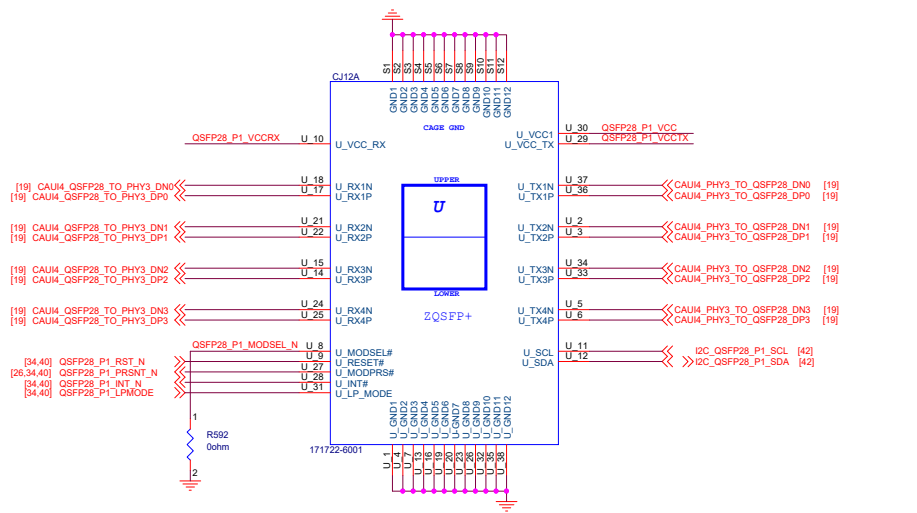


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1	3	5	7	9	11	13	15	17	19	21	23	25	27	21
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# 2x1 QSFP28 CONN3\_P33~P34

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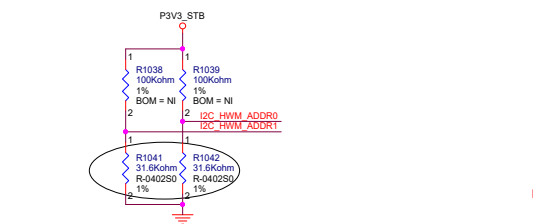
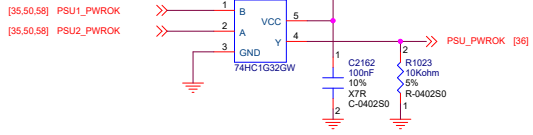
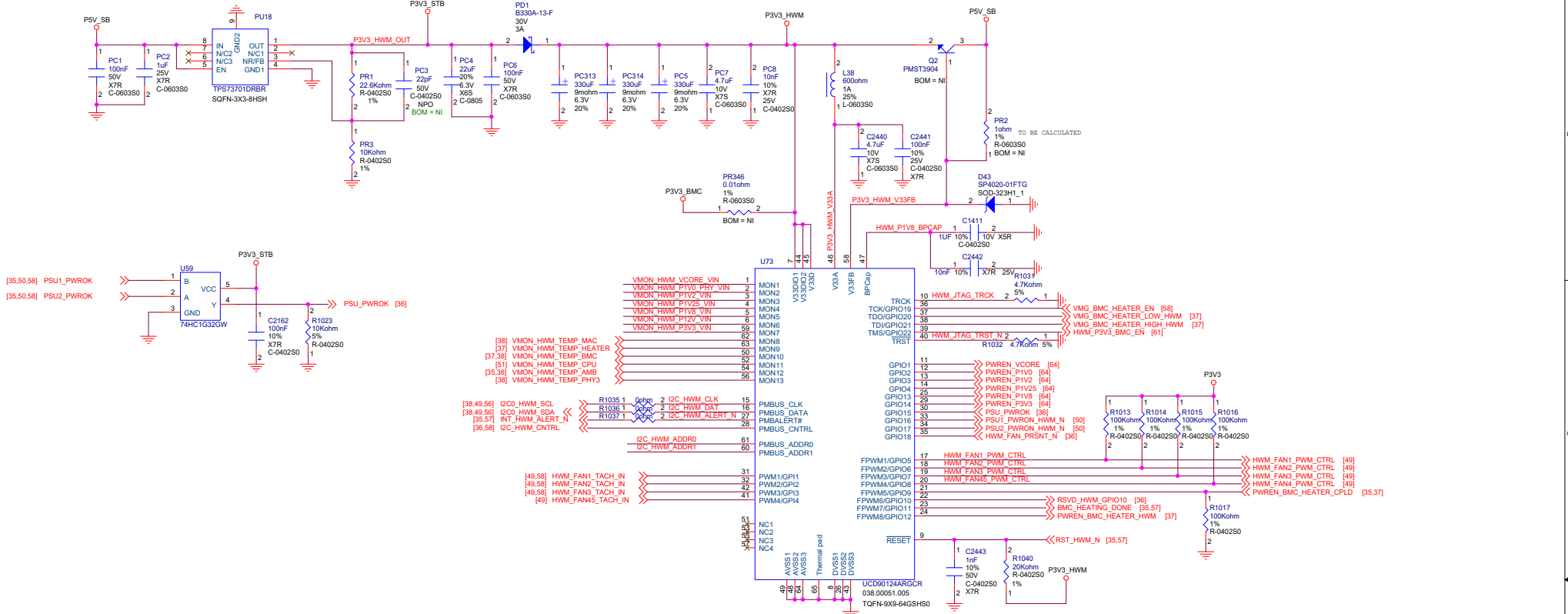
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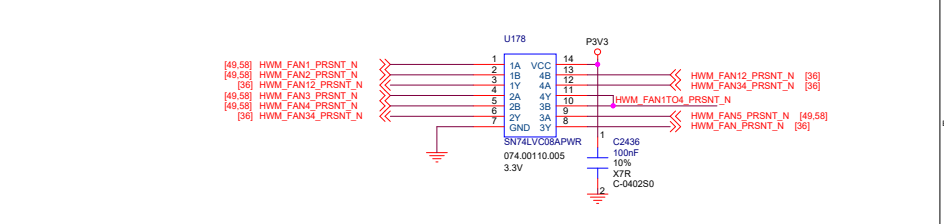
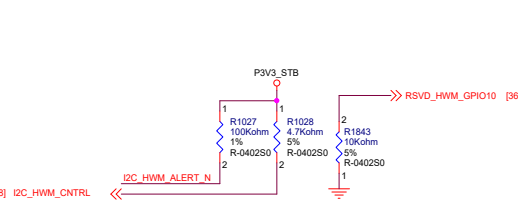
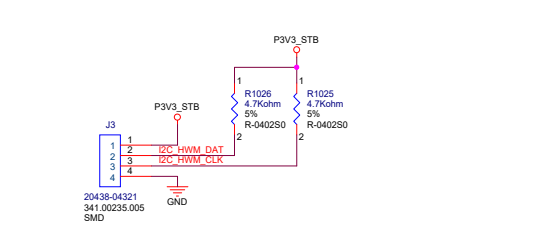
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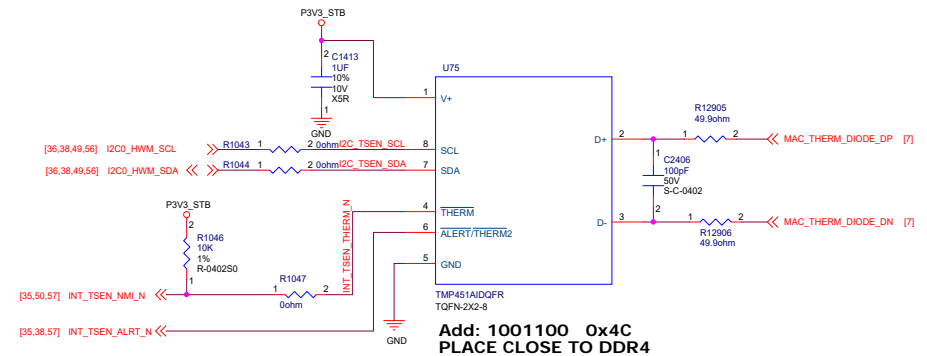
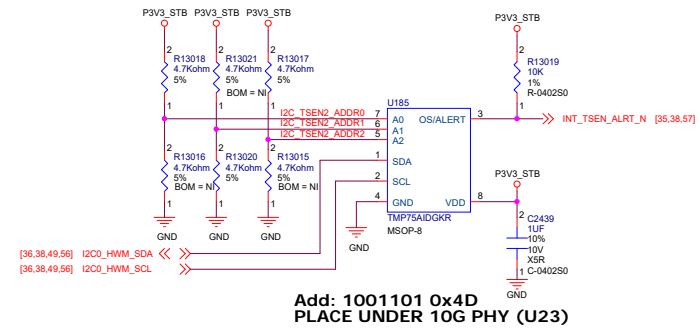
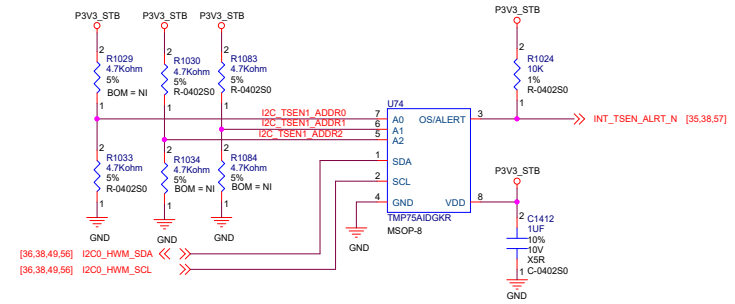
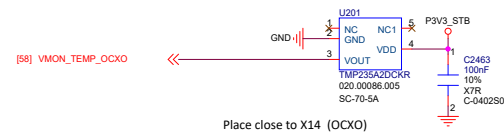
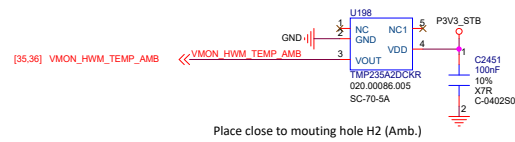
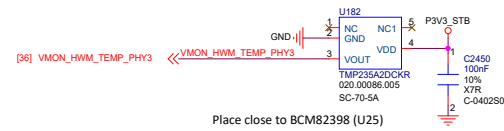
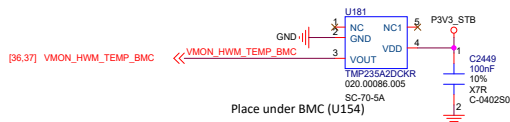
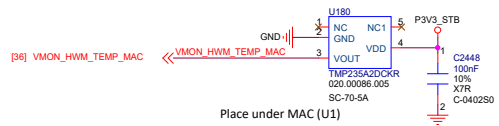
PMBus Add: 12x4+4=52 OX34



**<Core Design>**  
**Ufi Space Co., Ltd. CONFIDENTIAL**  
 Title: CSGR MAINBOARD  
 Size: Document Number  
 C Project: T770994T00 Rev: 07XB1  
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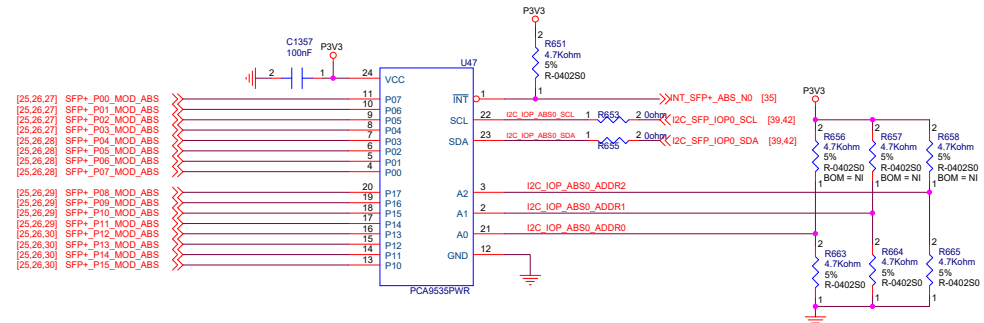
# HWM MONITOR\_UCD90124A



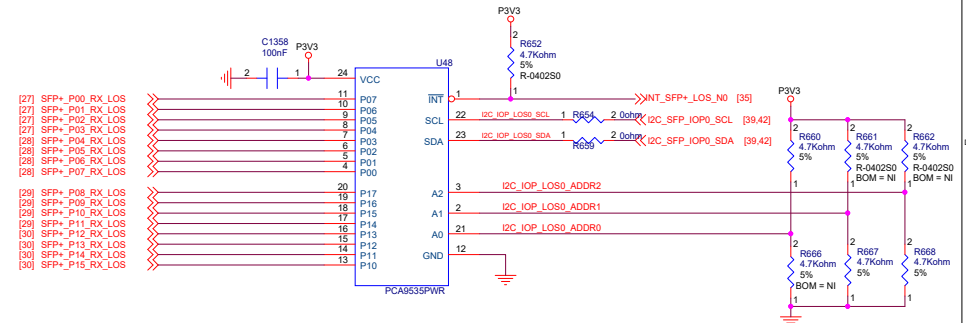


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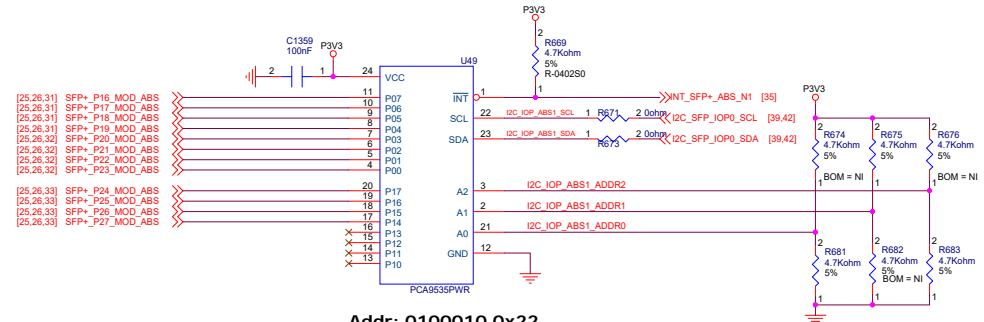
<b>Ufi Space Co., Ltd.</b>		<b>CONFIDENTIAL</b>	
Title CSGR MAINBOARD			
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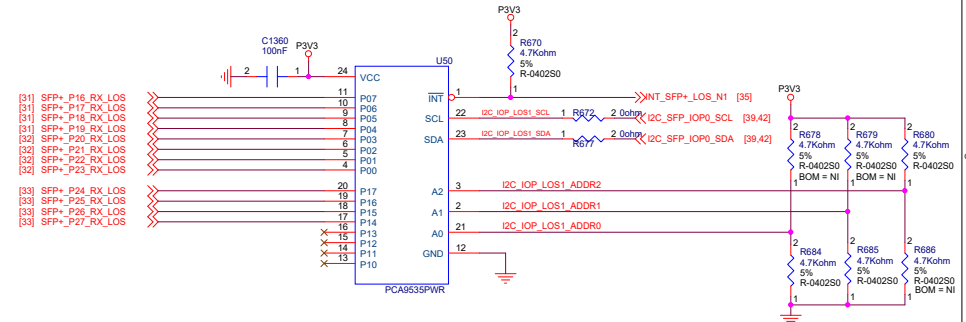
Addr: 010000 0x20



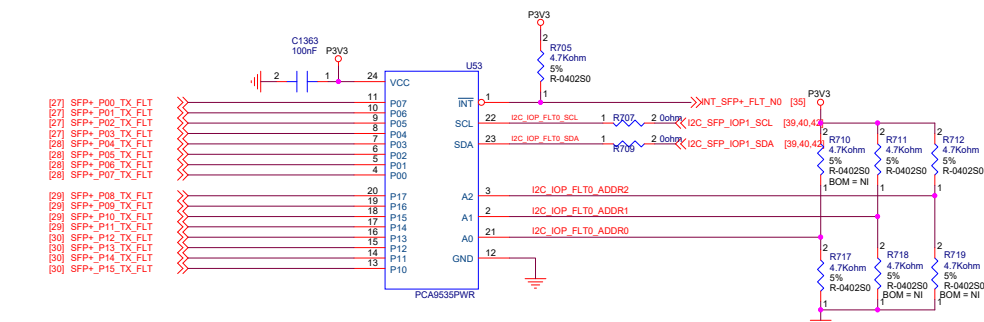
Addr: 010001 0x21



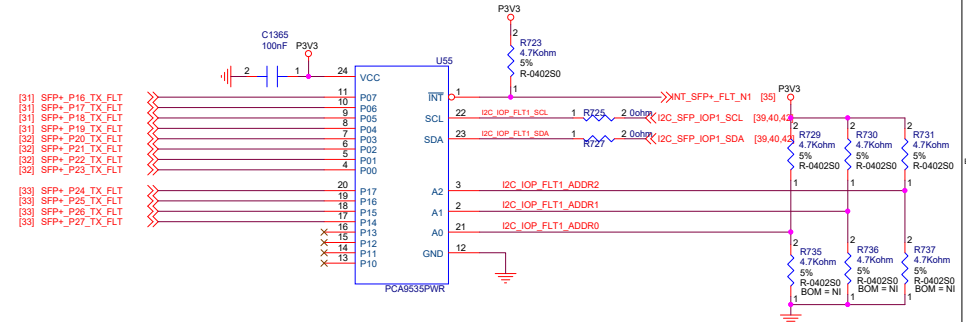
Addr: 010010 0x22



Addr: 010010 0x24



Addr: 010011 0x26



Addr: 010011 0x27

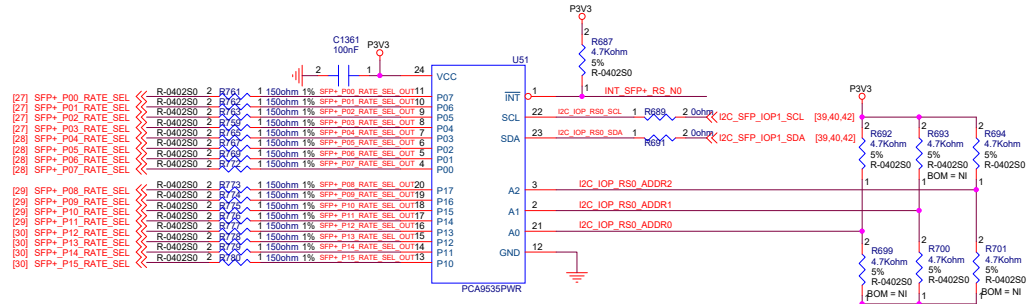
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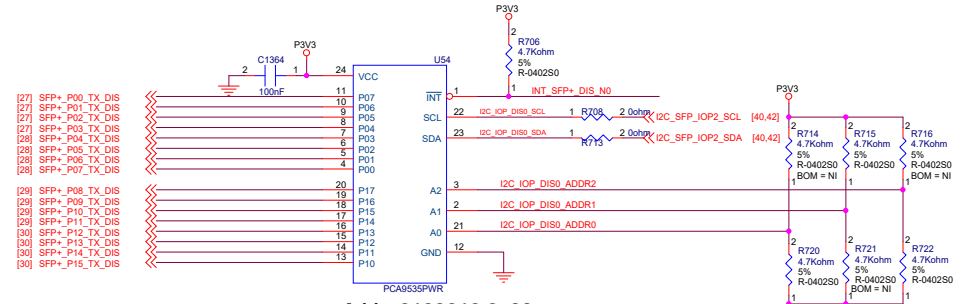
Title: CSGR MAINBOARD

Size: C Document Number: T990089T00 Rev: 07XB1

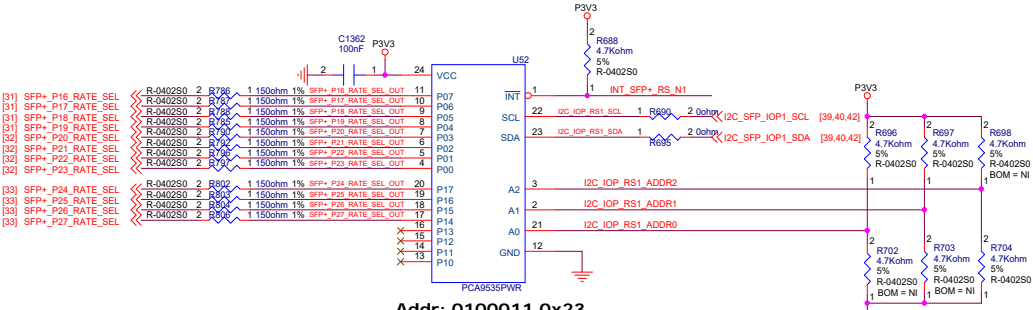
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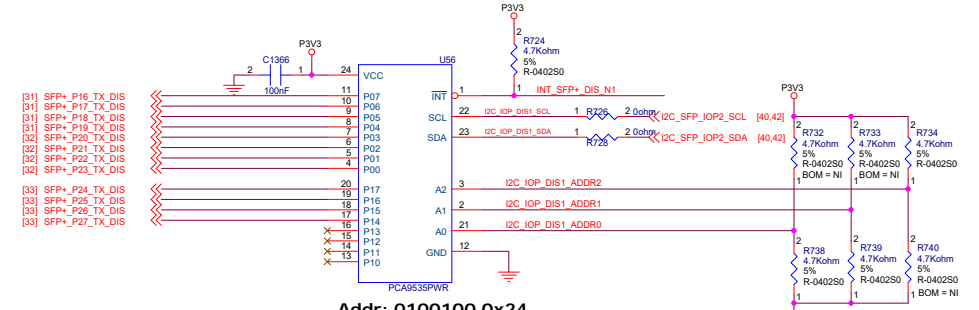
Addr: 0100101 Ox25



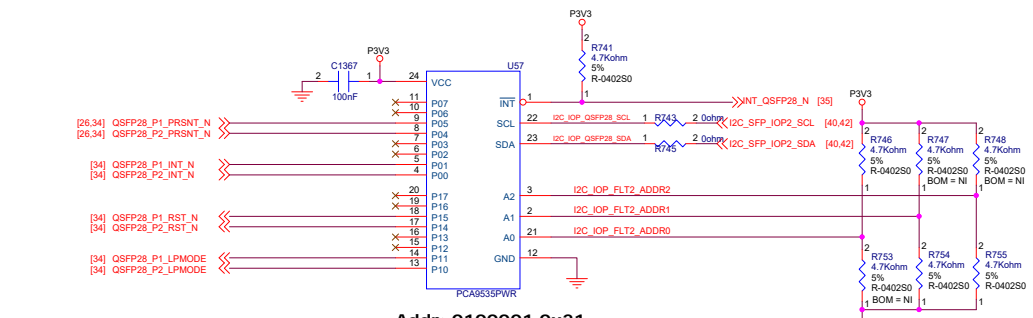
Addr: 0100010 Ox22



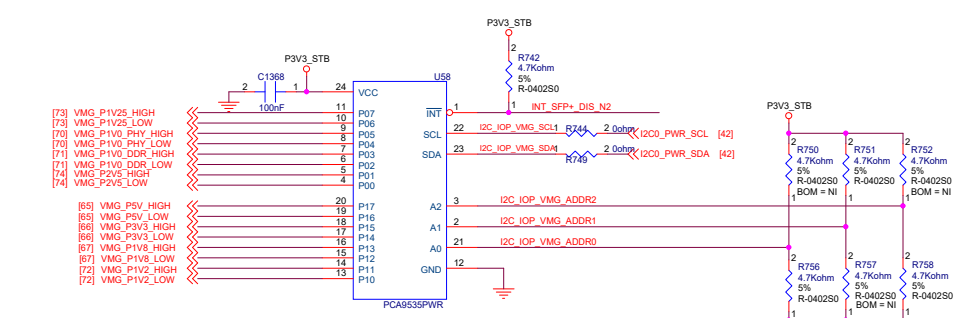
Addr: 0100011 Ox23



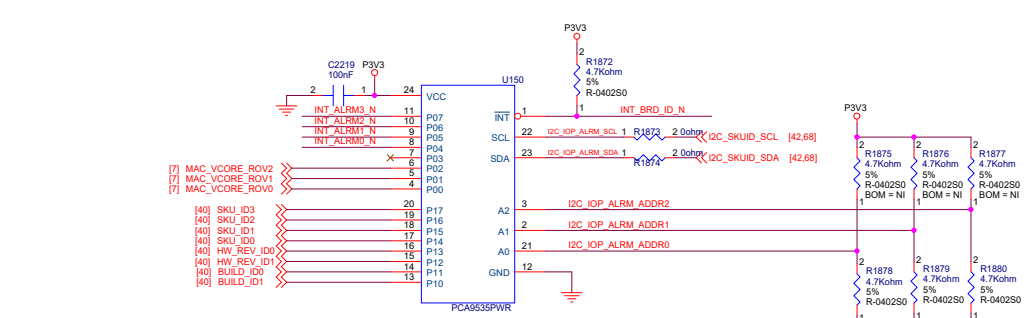
Addr: 0100100 Ox24



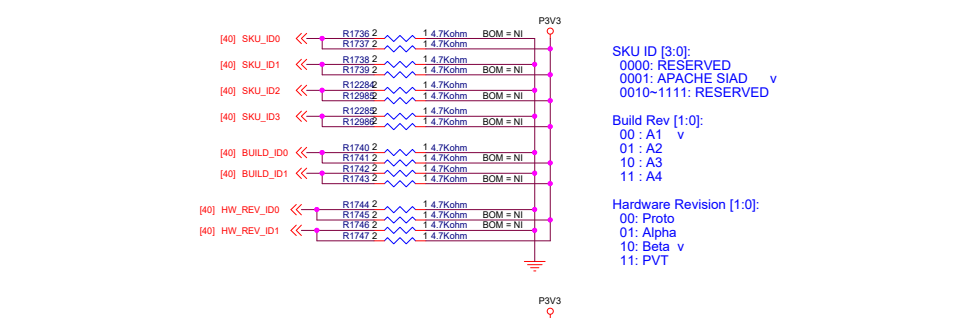
Addr: 0100001 Ox21



Addr: 0100010 Ox22



Addr: 0100000 Ox20



Addr: 0100010 Ox22

SKU ID [3:0]:  
 0000: RESERVED  
 0001: APACHE SIAD v  
 0010-1111: RESERVED

Build Rev [1:0]:  
 00: A1 v  
 01: A2  
 10: A3  
 11: A4

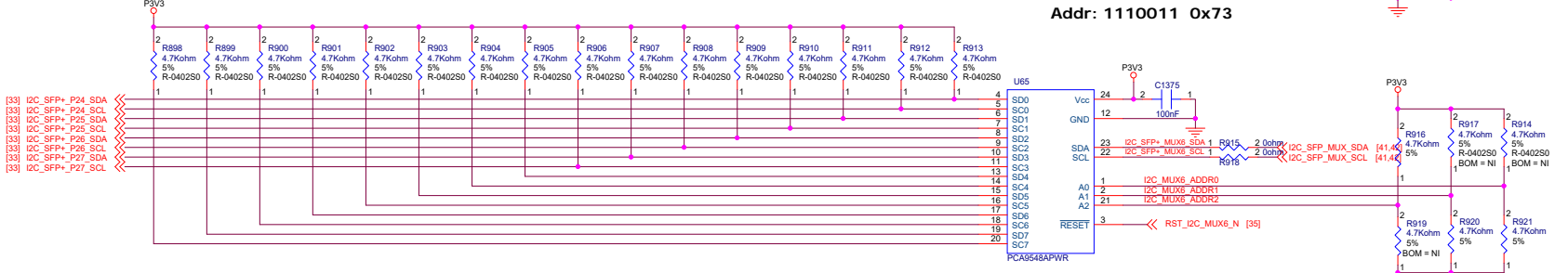
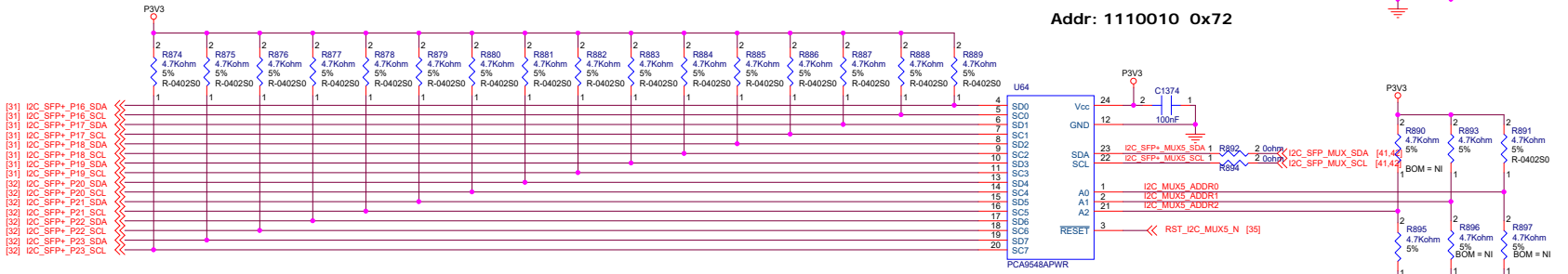
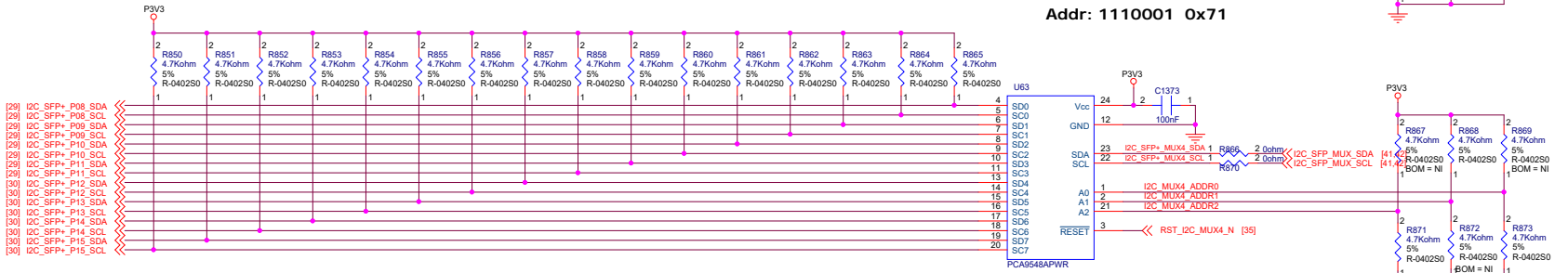
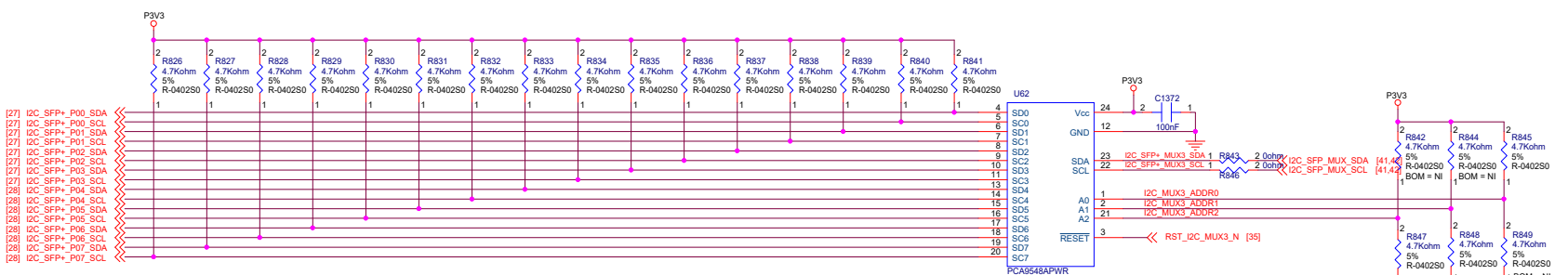
Hardware Revision [1:0]:  
 00: Proto  
 01: Alpha  
 10: Beta v  
 11: PVT

<Core Design>

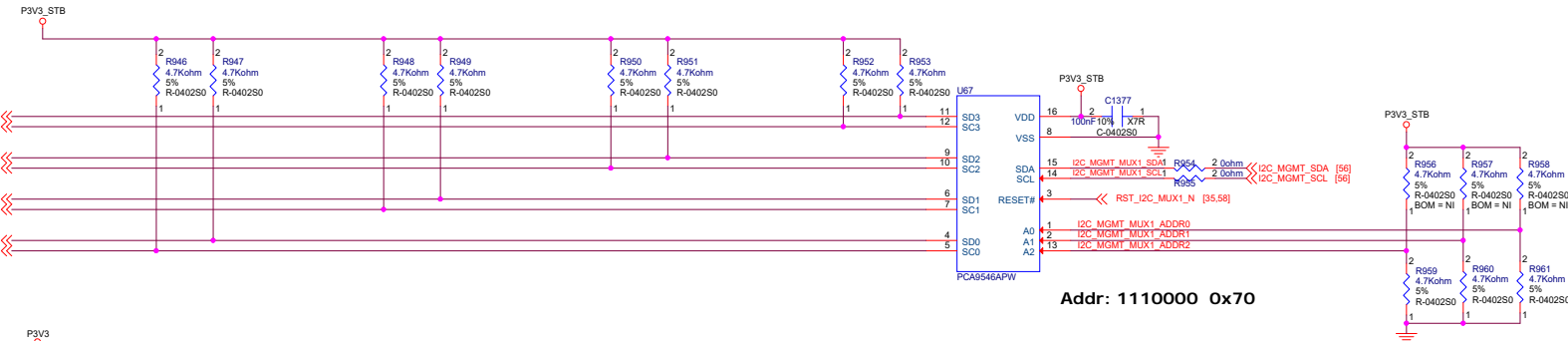
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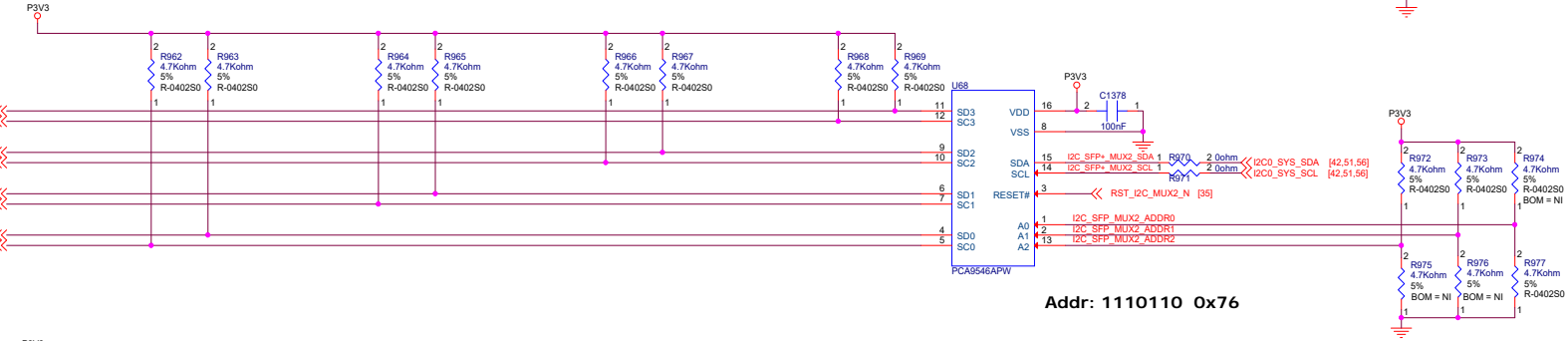


MAC	EPRGM	[7,55] I2C0_MISC_SDA [7,55] I2C0_MISC_SCL
VCORE	MARGINING	[40] I2C0_PWR_SDA [40] I2C0_PWR_SCL
PSU0		[50] I2C0_PSU1_SDA [50] I2C0_PSU1_SCL
PSU1		[50] I2C0_PSU2_SDA [50] I2C0_PSU2_SCL



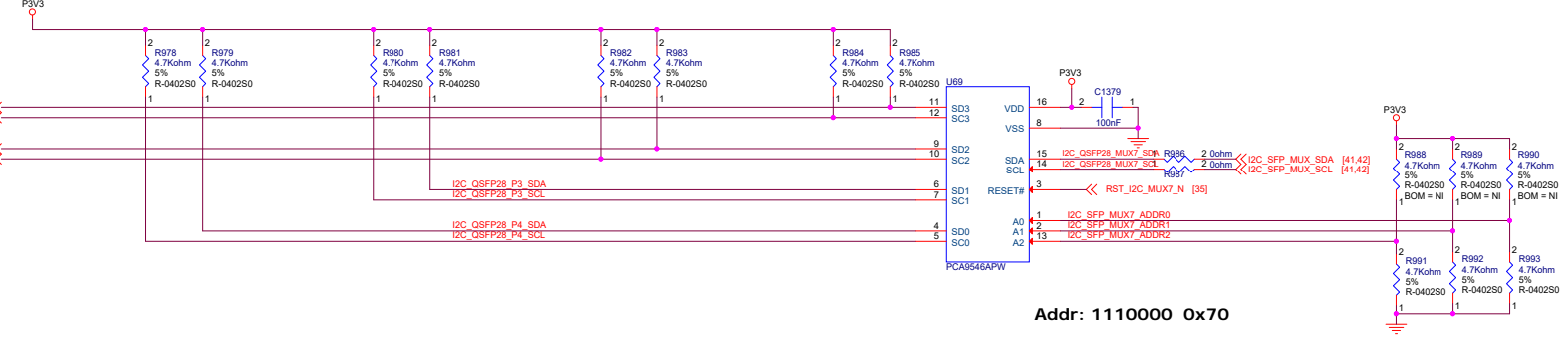
Addr: 1110000 0x70

[41,42] I2C_SFP_MUX2_SDA [41,42] I2C_SFP_MUX2_SCL
[39] I2C_SFP_IOP0_SDA [39] I2C_SFP_IOP0_SCL
[39,40] I2C_SFP_IOP1_SDA [39,40] I2C_SFP_IOP1_SCL
[40] I2C_SFP_IOP2_SDA [40] I2C_SFP_IOP2_SCL



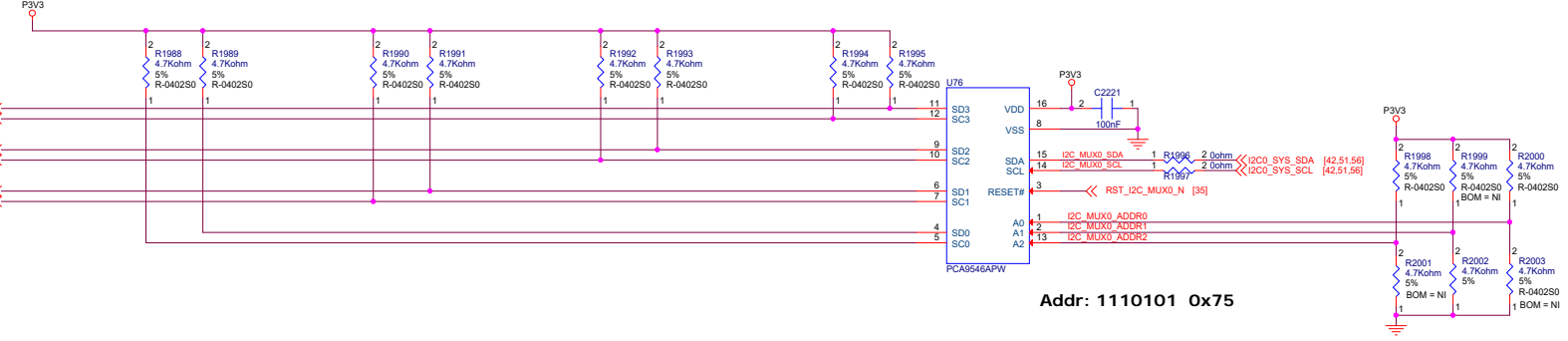
Addr: 1110110 0x76

[34] I2C_QSFP28_P1_SDA [34] I2C_QSFP28_P1_SCL
[34] I2C_QSFP28_P2_SDA [34] I2C_QSFP28_P2_SCL



Addr: 1110000 0x70

[22,48] I2C_CLK_SDA [22,48] I2C_CLK_SCL
[40,68] I2C_SKUID_SDA [40,68] I2C_SKUID_SCL
[43] I2C_GNSS_SDA [43] I2C_GNSS_SCL

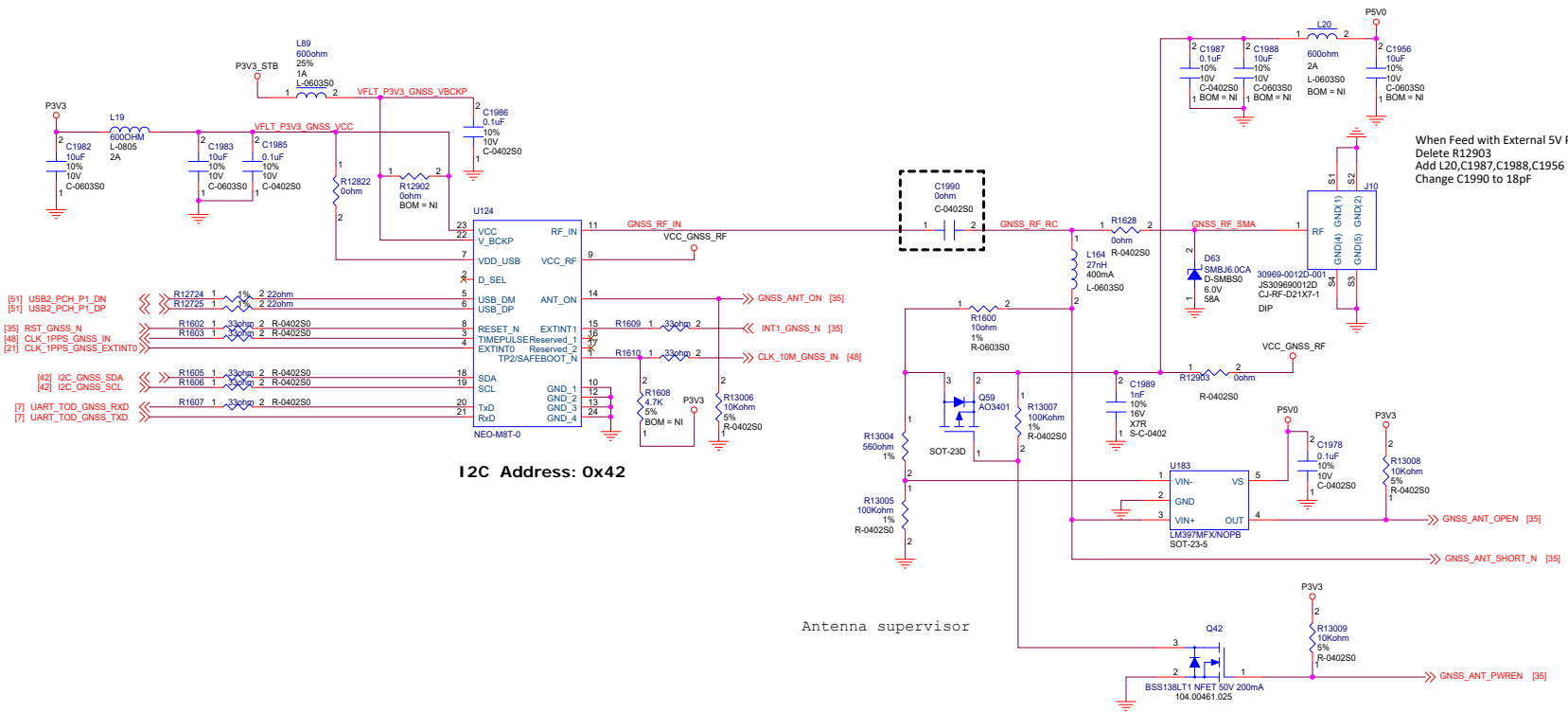


Addr: 1110101 0x75

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# I2C MUX2



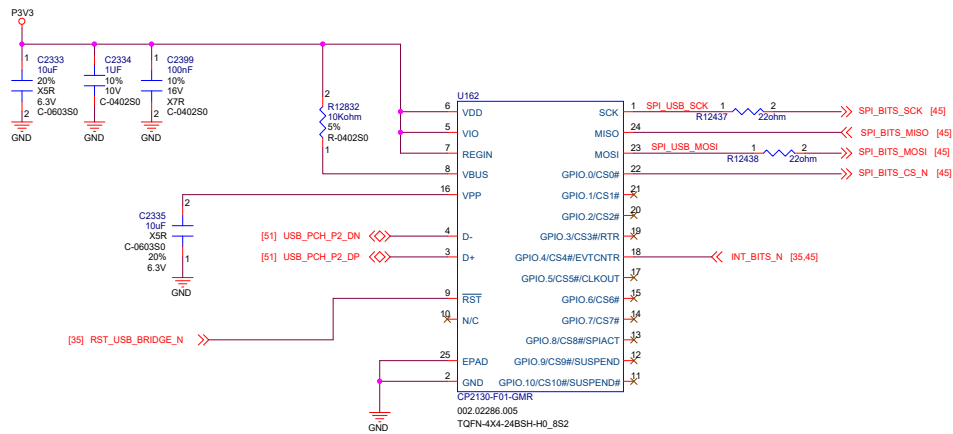
When Feed with External 5V PWR:  
Delete R12903  
Add L20, C1987, C1988, C1956  
Change C1990 to 18pF

Antenna supervisor

1. CPU configure GNSS module to set ANT\_ON=1 during initialization.
2. CPLD set ANT\_PWREN=1 when receive ANT\_ON=1 signal from GNSS.
3. CPLD issue PTP interrupt if ANT\_SHORT\_N=0.
4. CPLD turn on/off GNSS LED per ANT\_SHORT\_N status.
5. ANT\_OPTEN=1, NO ANTENNA IS INSTALLED OR PASSIVE ANTENNA IS PLUGED.
6. ANT\_OPTEN=0, ACTIVE ANTENNA IS INSTALLED.

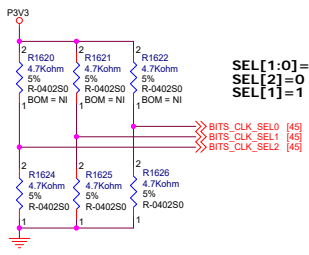
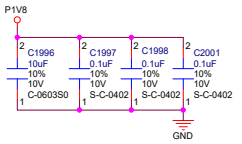
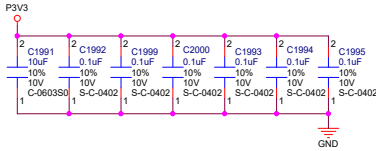
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<b>Ufi Space Co., Ltd.</b>		<b>CONFIDENTIAL</b>
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# PTP\_GNSS MODULE

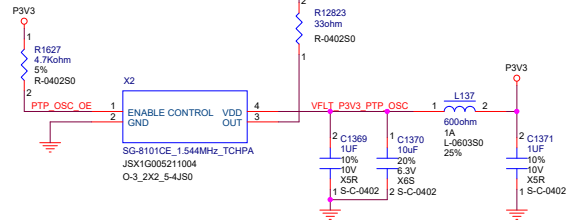


<Variant Name>		
<b>Ufi Space Co., Ltd.</b>		<b>CONFIDENTIAL</b>
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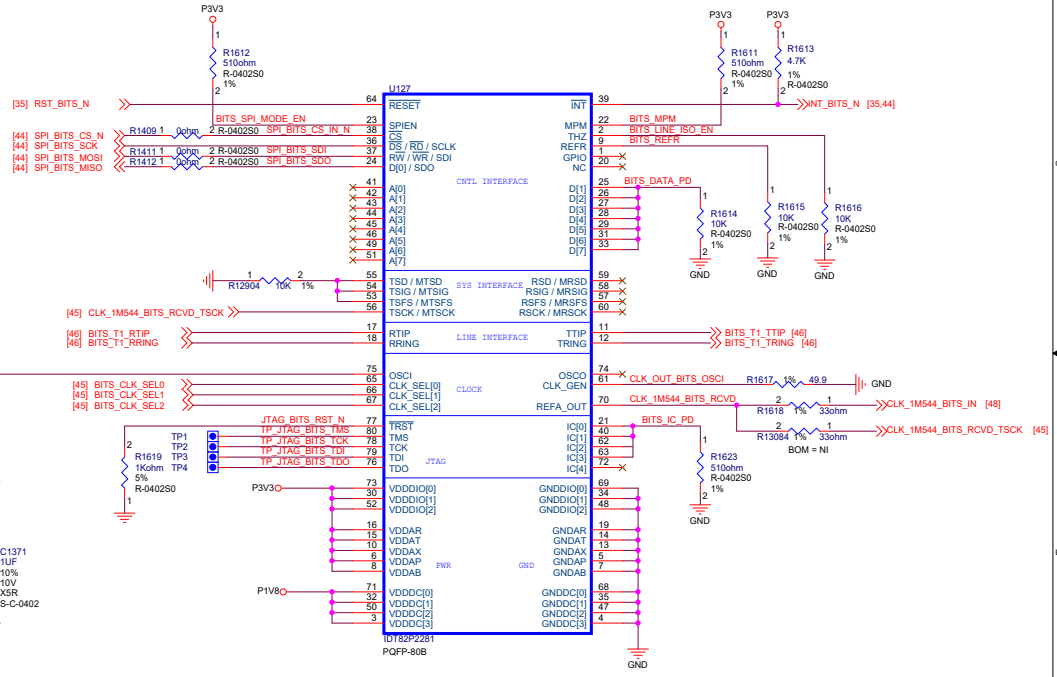
# PTP\_USB TO SPI BRIDGE



SEL[1:0]=00 N=1  
 SEL[2]=0 N\*1.544MHz  
 SEL[1]=1 N\*2.048MHz

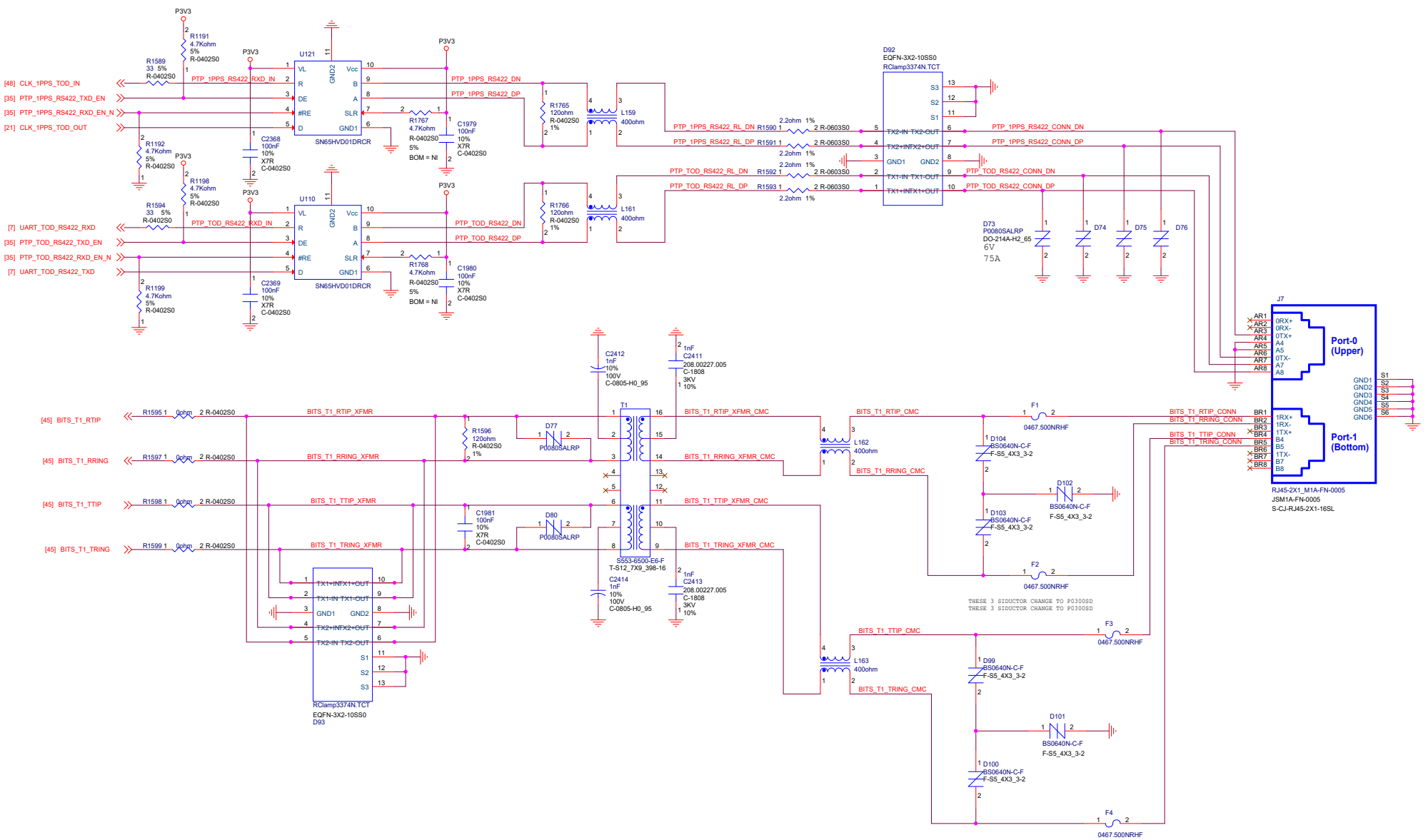


OSC: N\*1.544



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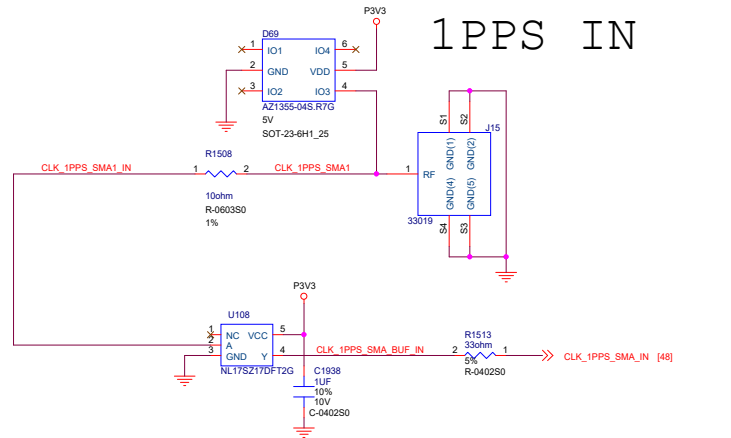
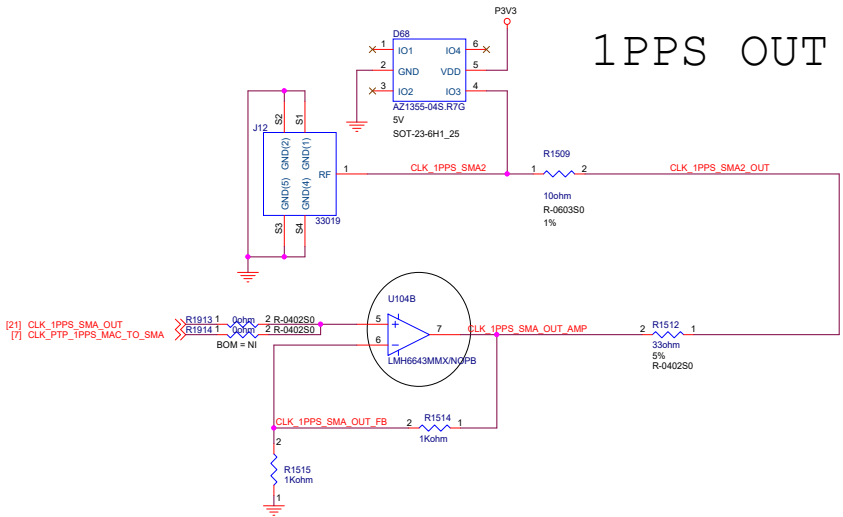
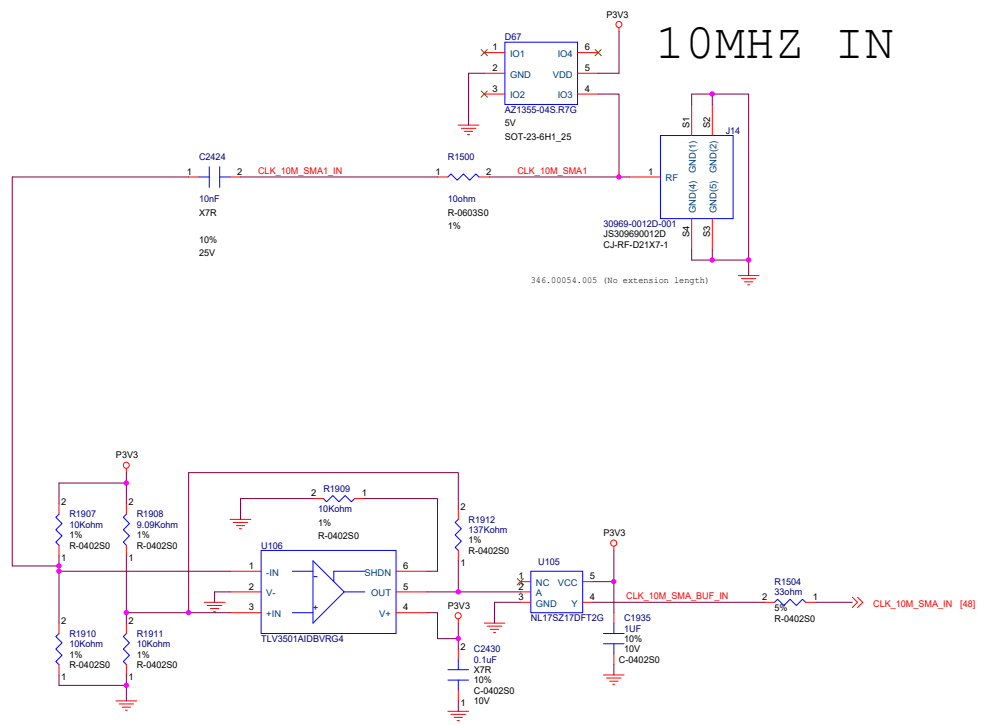
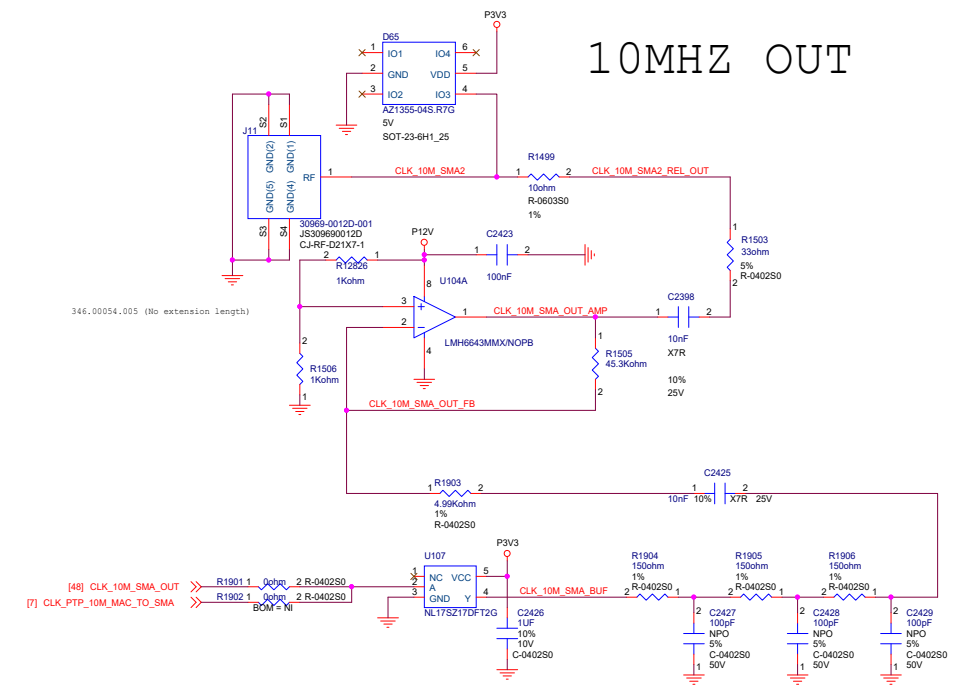
# PTP\_T1/E1 RECEIVER



<Core Design>

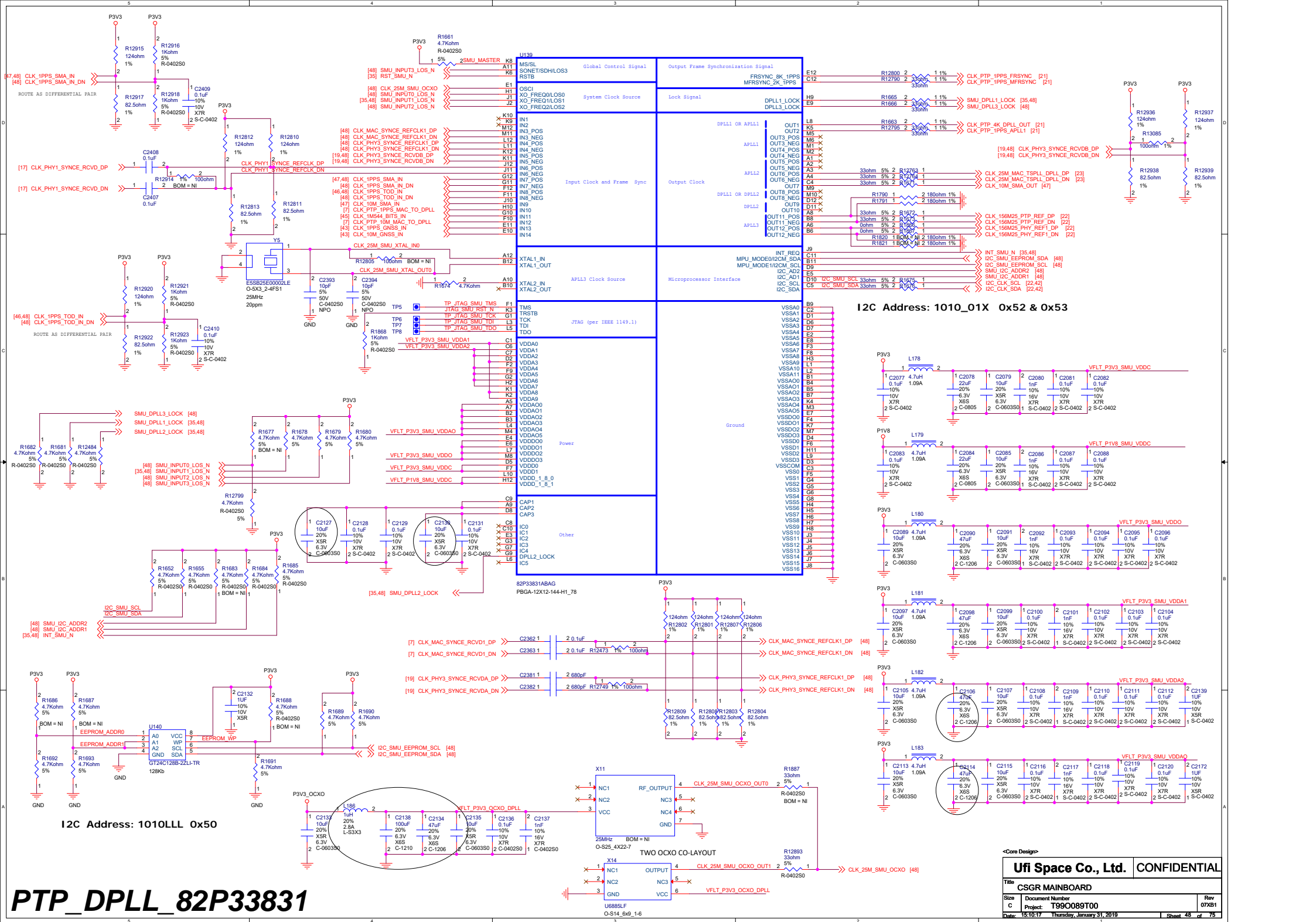
<b>Ufi Space Co., Ltd.</b>		<b>CONFIDENTIAL</b>
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# T1/E1 & TOD IN/OUT



# PTP\_1PPS & 10MHZ IN/OUT

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[47,48] CLK\_IPPS\_SMA\_IN  
[48] CLK\_IPPS\_SMA\_IN\_DN

[17] CLK\_PHY1\_SYNC\_RCVD\_DP  
[17] CLK\_PHY1\_SYNC\_RCVD\_DN

[46,48] CLK\_IPPS\_TOD\_IN  
[48] CLK\_IPPS\_TOD\_IN\_DN

[48] SMU\_I2C\_ADDR1  
[48] SMU\_I2C\_ADDR2  
[35,48] INT\_SMU\_N

I2C Address: 1010LLL 0x50

[48] SMU\_INPUTS\_LOS\_N  
[35,48] SMU\_INPUT1\_LOS\_N  
[48] SMU\_INPUT2\_LOS\_N  
[48] SMU\_INPUT3\_LOS\_N

[48] CLK\_MAC\_SYNC\_REFCLK1\_DP  
[48] CLK\_MAC\_SYNC\_REFCLK1\_DN  
[48] CLK\_PHY3\_SYNC\_REFCLK1\_DP  
[48] CLK\_PHY3\_SYNC\_REFCLK1\_DN  
[19,48] CLK\_PHY3\_SYNC\_RCVD\_DP  
[19,48] CLK\_PHY3\_SYNC\_RCVD\_DN

TP5  
TP6  
TP7  
TP8

VFLT\_P3V3\_SMU\_VDDA1  
VFLT\_P3V3\_SMU\_VDDA2

VFLT\_P3V3\_SMU\_VDDA0  
VFLT\_P3V3\_SMU\_VDDC  
VFLT\_P1V8\_SMU\_VDDC

[7] CLK\_MAC\_SYNC\_RCVD1\_DP  
[7] CLK\_MAC\_SYNC\_RCVD1\_DN

[19] CLK\_PHY3\_SYNC\_RCVD1\_DP  
[19] CLK\_PHY3\_SYNC\_RCVD1\_DN

[48] SMU\_I2C\_ADDR1  
[48] SMU\_I2C\_ADDR2  
[35,48] INT\_SMU\_N

[7] CLK\_MAC\_SYNC\_REFCLK1\_DP  
[7] CLK\_MAC\_SYNC\_REFCLK1\_DN

[48] SMU\_I2C\_ADDR1  
[48] SMU\_I2C\_ADDR2  
[35,48] INT\_SMU\_N

Global Control Signal  
Output Frame Synchronization Signal  
Lock Signal

System Clock Source

Input Clock and Frame Sync

APB1 Clock Source

JTAG (per IEEE 1149.1)

Power

Other

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

Microprocessor Interface

FRSYNC\_8K\_IPPS  
MFRSYNC\_2K\_IPPS

SMU\_DPLL\_LOCK [35,48]  
SMU\_DPLL2\_LOCK [35,48]

CLK\_PTP\_4K\_DPLL\_OUT [21]  
CLK\_PTP\_IPPS\_FRSYNC [21]  
CLK\_PTP\_IPPS\_MFRSYNC [21]

CLK\_25M\_MAC\_TSPDLL\_DP [23]  
CLK\_25M\_MAC\_TSPDLL\_DN [23]  
CLK\_10M\_SMA\_OUT [47]

CLK\_156M25\_PTP\_REF\_DP [22]  
CLK\_156M25\_PTP\_REF\_DN [22]  
CLK\_156M25\_PHY\_REF1\_DP [22]  
CLK\_156M25\_PHY\_REF1\_DN [22]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

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I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

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I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

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I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

INT\_SMU\_N [35,48]  
I2C\_SMU\_EEPROM\_SDA [48]  
I2C\_SMU\_EEPROM\_SCL [48]  
SMU\_I2C\_ADDR1 [48]  
SMU\_I2C\_ADDR2 [48]  
I2C\_I2C\_ADDR1 [48]  
I2C\_I2C\_ADDR2 [48]  
I2C\_CLK\_SCL [22,42]  
I2C\_CLK\_SDA [22,42]

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CSGR MAINBOARD

Project: T990089T00

Rev: 07X81

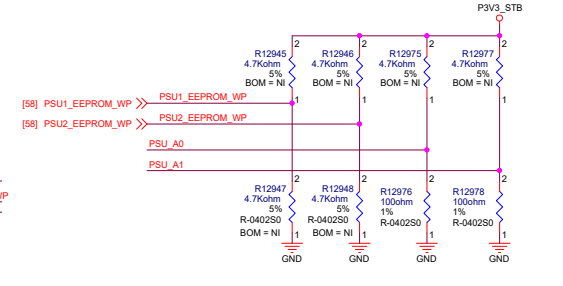
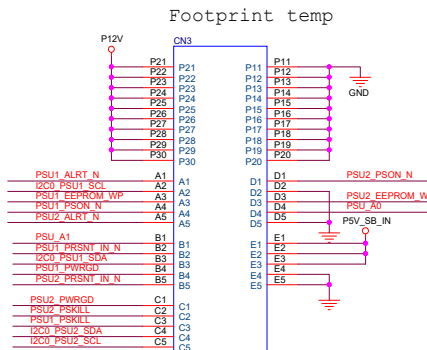
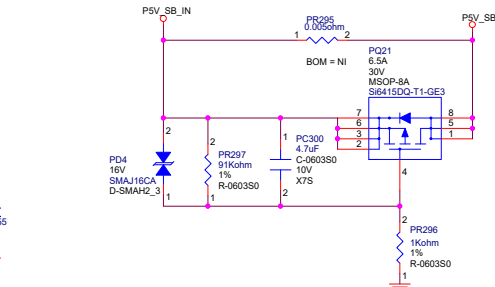
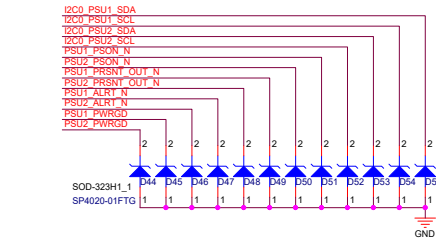
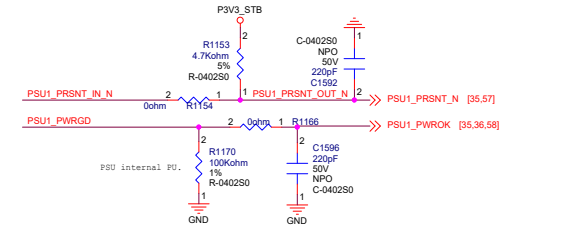
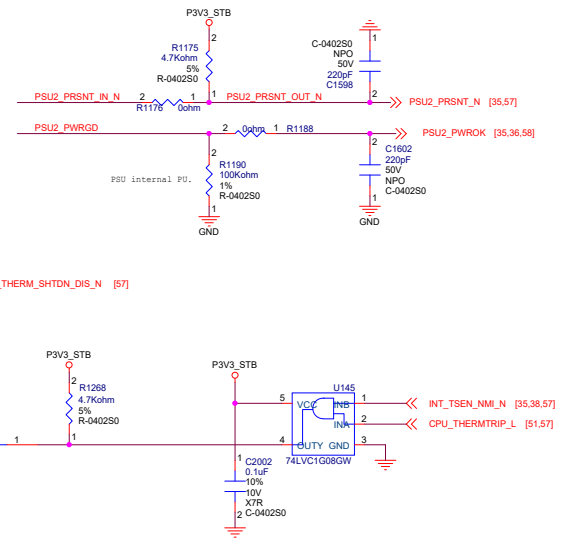
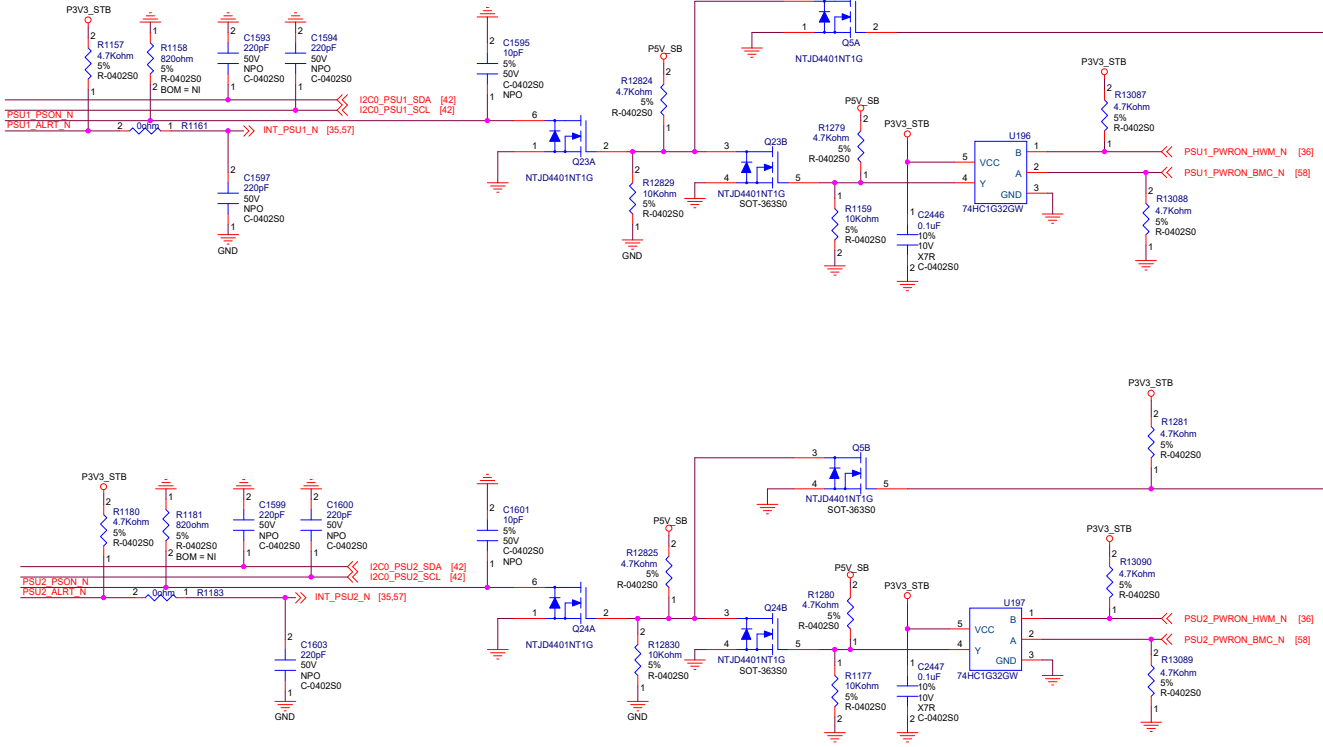
Date: 15/10/17 Thursday, January 31, 2019

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PTP\_DPLL\_82P33831







PSU CONNECTOR 1  
EEPROM I2C Addr. A0h, 1010000, 0x50  
MCU I2C Addr. B0h, 1011000, 0x58

PSU CONNECTOR 2  
EEPROM I2C Addr. A0h, 1010000, 0x50  
MCU I2C Addr. B0h, 1011000, 0x58

# PSU PWR CONNECTOR

<Core Design>

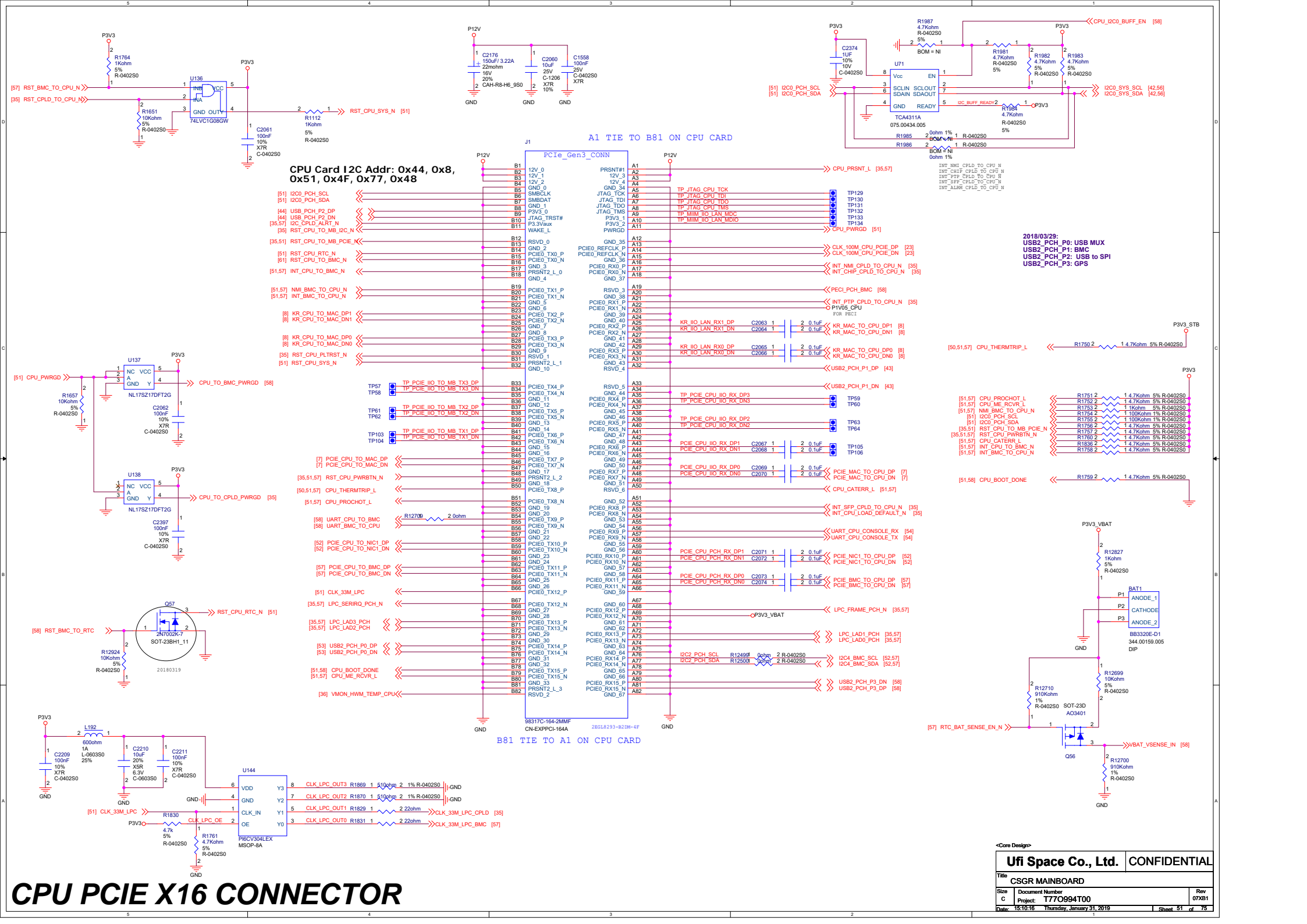
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Title: **CSGR MAINBOARD**

Size: C Document Number: **T990089T00** Rev: **07XB1**

Project: **T990089T00**

Date: **15/10/16** Thursday, January 31, 2019 Sheet **50** of **75**



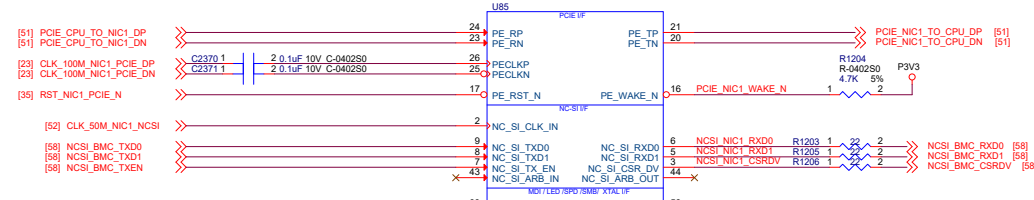
# CPU PCIE X16 CONNECTOR

**<Core Design>**

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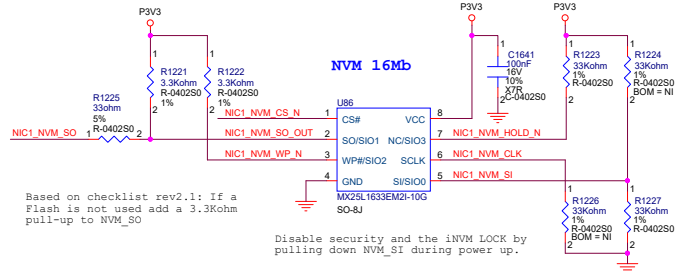
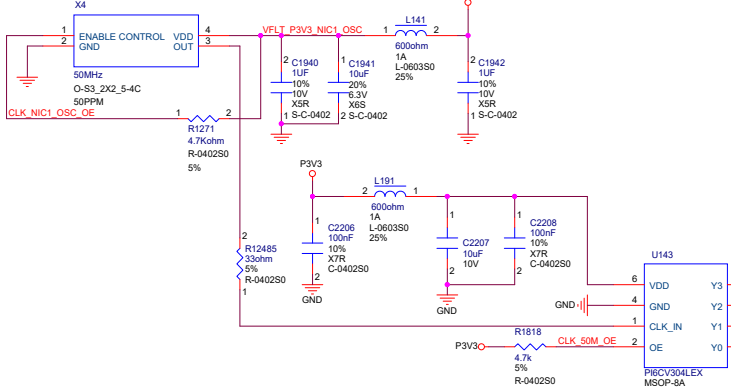
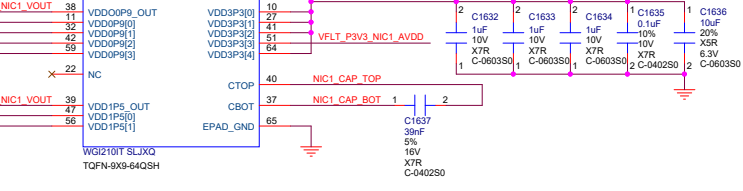
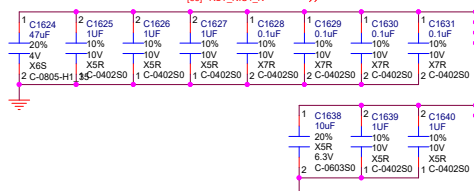
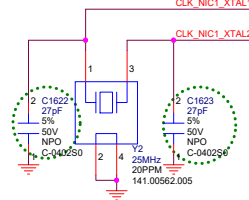
**Title: CSGR MAINBOARD**

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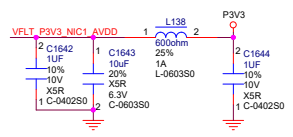
SMBUS: FOR DEBUG ONLY  
 [51] I2C4\_BMC\_SCL  
 [51] I2C4\_BMC\_SDA  
 [57] I2C4\_NIC\_ARL\_T\_N

NOTE: Default SMBus Address is 0xC2



Based on checklist rev2.1: If a Flash is not used add a 3.3Kohm pull-up to NVM\_SO

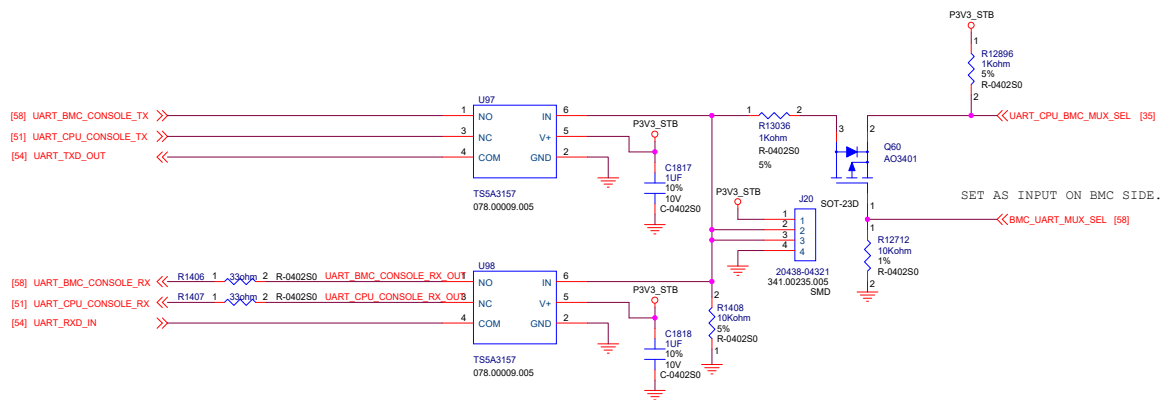
Disable security and the INVM LOCK by pulling down NVM\_SI during power up.



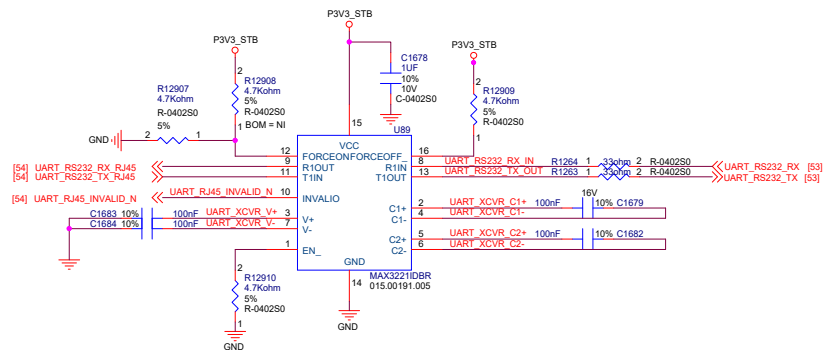
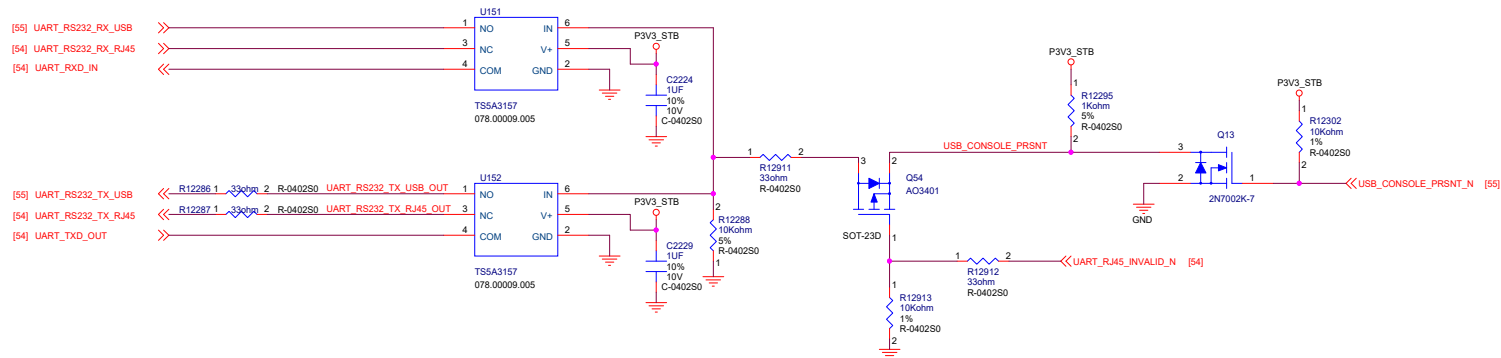
# CPU\_NIC1\_I210-IT

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Title: CSGR MAINBOARD	
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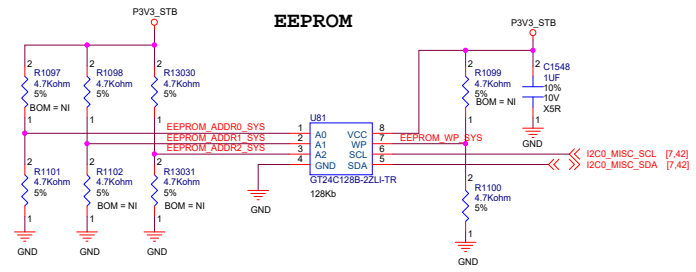
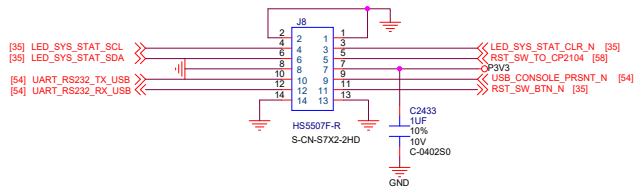
IN=H COM TO NO  
IN=L COM to NC



<Core Design>

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Title CSGR MAINBOARD		
Size C	Document Number Project: T770994T00	Rev 07XB1
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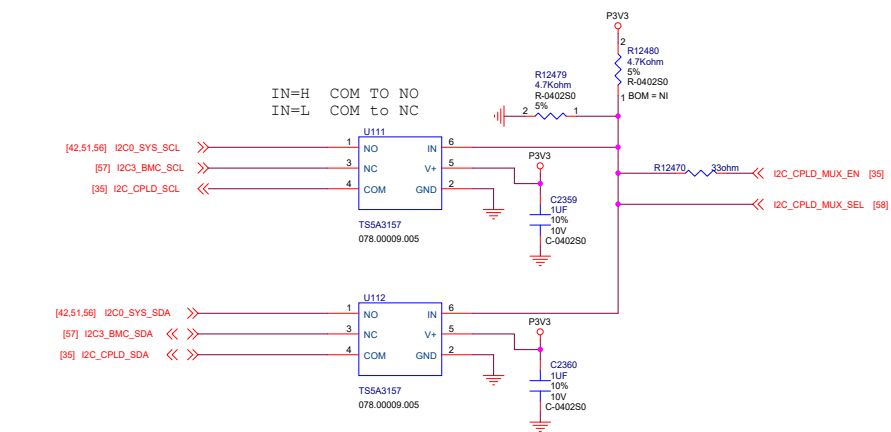
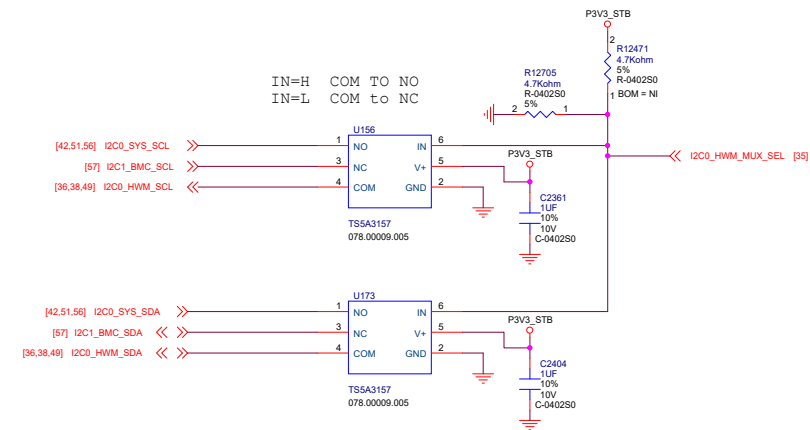
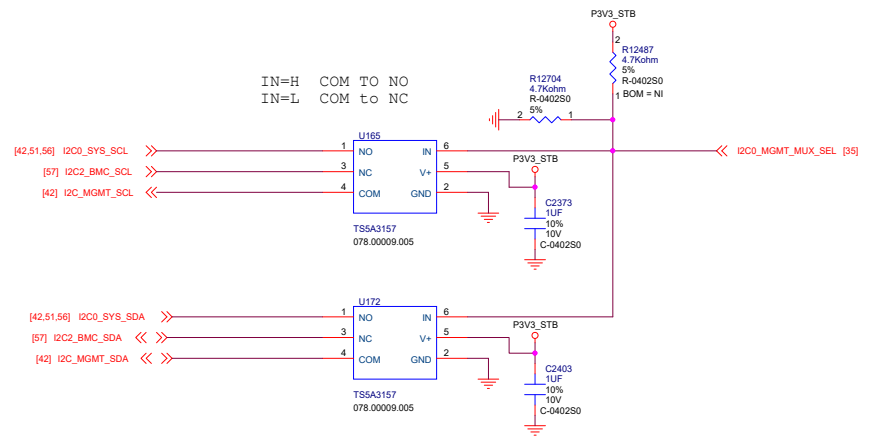
# CONSOLE MUX & RS232 XCVR



Addr: 1010110 0x56

<Core Design>		
<b>Ufi Space Co., Ltd.</b>		<b>CONFIDENTIAL</b>
Title CSGR MAINBOARD		
Size C	Document Number Project: T770994T00	Rev 07XB1
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# LED CARD HEADER & EEPROM



<Core Design>

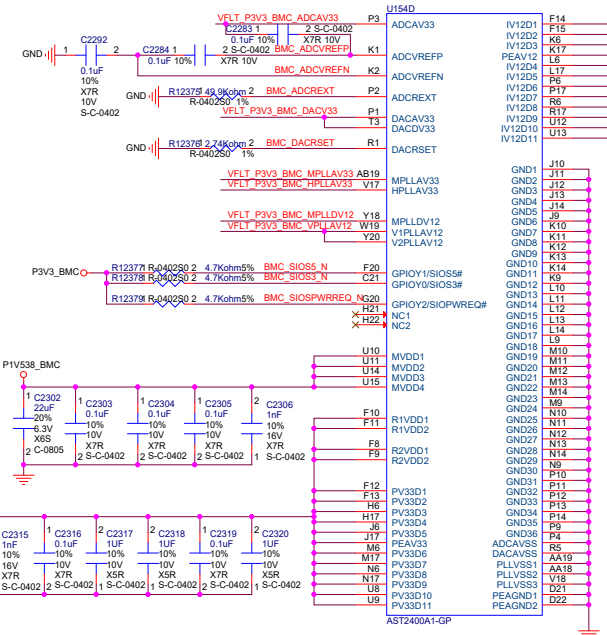
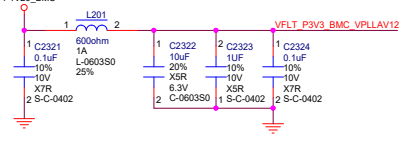
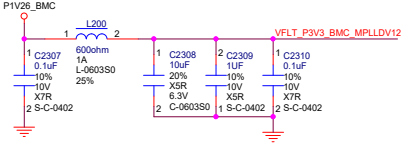
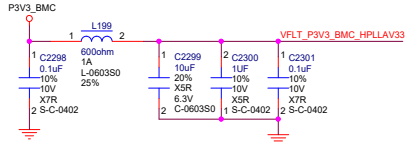
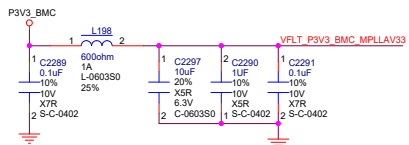
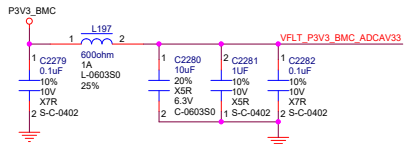
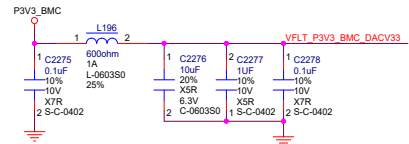
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Title		CSGR MAINBOARD	
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C	T990089T00	07XB1	
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<Core Design>

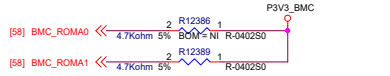
<b>Ufi Space Co., Ltd.</b>		<b>CONFIDENTIAL</b>
Title CSGR MAINBOARD		
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# BMC\_AST2400\_PWR & GND

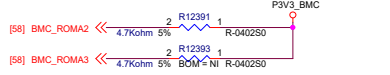
TXD5:Disable ARM ICE reset mode  
 0 : Enable ICE reset mode  
 1 : Disable ARM ICE reset mode (default)



ROMA[1:0] : ARM CPU boot code selection  
 00 : Boot from NOR flash memory  
 01 : Boot from NAND flash memory  
 10 : Boot from SPI flash memory (default)  
 11 : Disable ARM CPU operation



ROMA[3:2] : VGA memory size selection  
 00 : Select 8 MB VGA memory  
 01 : Select 16 MB VGA memory (default)  
 10 : Select 32 MB VGA memory  
 11 : Select 64 MB VGA memory

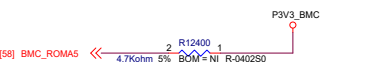


ROMA[4] : Boot flash memory extended option  
 NOR type flash: data bus width selection  
 0 : Select 8 bits interface  
 1 : Select 16 bits interface

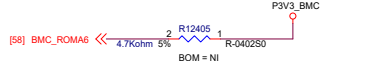
SPI type flash: boot address mode selection  
 0 : Boot with 24 bits address mode (default)  
 1 : Boot with 32 bits address mode



ROMA[5] : Enable VGA BIOS ROM  
 0 : No VGA BIOS ROM (for on-board application) (default)  
 1 : Enable VGA BIOS ROM (for add-on application)



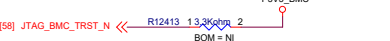
ROMA[6] : Define MAC#1 interface  
 0 : RMII/NCSEI (default)  
 1 : RGMII



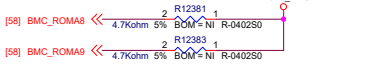
ROMA[7] : Define MAC#2 interface  
 0 : RMII/NCSEI (default)  
 1 : RGMII



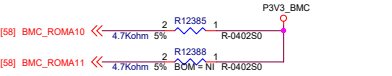
NTRST:Reserved  
 \*\*\*



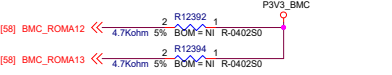
ROMA[9:8] : H-PLL default clock frequency selection  
 00 : Select 384 MHz (default)  
 01 : Select 360 MHz  
 10 : Select 336 MHz  
 11 : Select 204 MHz



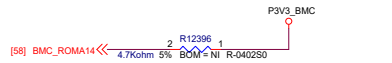
ROMA[11:10] : CPU/AHB clock frequency ratio selection  
 00 : Select CPU:AHB = 1:1  
 01 : Select CPU:AHB = 2:1 (default)  
 10 : Select CPU:AHB = 4:1  
 11 : Select CPU:AHB = 3:1



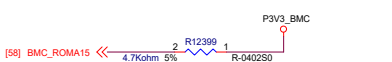
ROMA[13:12] : SPI mode selection  
 00 : Disable SPI interface (default)  
 01 : Enable SPI Master  
 10 : Enable SPI Master and SPI Slave to AHB Bridge  
 11 : Enable SPI Bypass



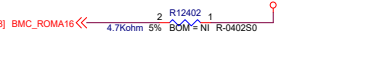
ROMA[14] : Enable LPC dedicated reset pin function  
 0 : LPC reset is shared with PCI reset pin. (default)  
 1 : LPC reset is shared with GPIOB4.



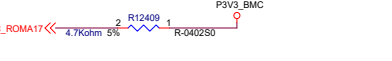
ROMA[15] : VGA Class Code selection  
 0 : Select the Class Code for video device  
 1 : Select the Class Code for VGA device (default)



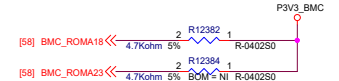
ROMA[16] : SuperIO configuration address selection  
 0 : Decode 0x2E (default)  
 1 : Decode 0x4E



ROMA[17] : Enable BMC 2nd boot watchdog timer  
 0 : Disable  
 1 : Enable BMC 2nd boot watchdog timer start counting at power up.  
 The watchdog timer was located at WDT2. After watchdog timeout, it will reset BMC and restart booting from the 2nd boot flash at CS1#. CS1# must be the same flash type as CS0# and could be the same firmware as CS0#. (default)



ROMA[23:18] : Clock source selection  
 00 : 24 MHz CLKIN  
 01 : 48 MHz CLKIN (default)  
 10 : 25MHz CLKIN, 24MHz USBCKI  
 11 : 25MHz CLKIN, 48MHz USBCKI



ROMA[19] : Disable ACPI function  
 0 : Enable ACPI  
 1 : Disable ACPI (default)



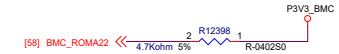
ROMA[20] : Disable LPC to decode GPIO  
 0x2E/0x4E address  
 0 : Enable address decoding (default)  
 1 : Disable address decoding



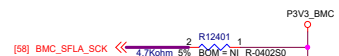
ROMA[21] : Enable GPIO pass-through mode  
 0 : Disable (default)  
 1 : Enable pass-through at power on



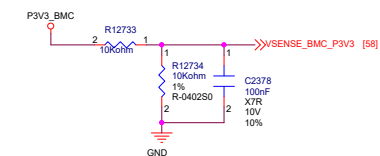
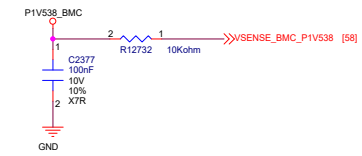
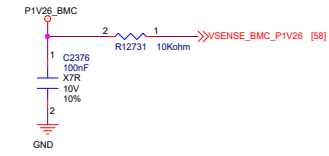
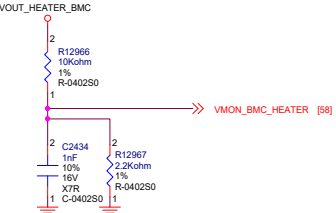
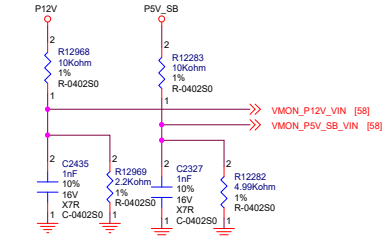
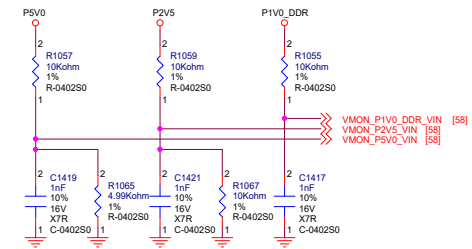
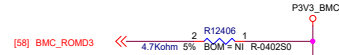
ROMA[22] : Enable GPIOE pass-through mode  
 0 : Disable (default)  
 1 : Enable pass-through at power on



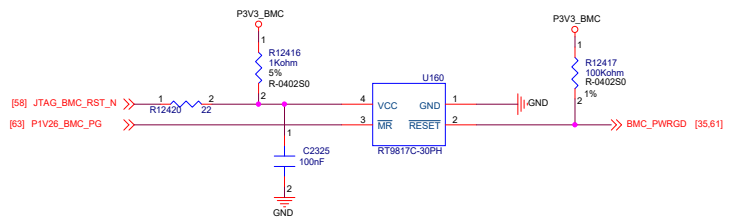
ROMD[2:0]:010:DDR3 SDRAM with CL=6, CWL=5



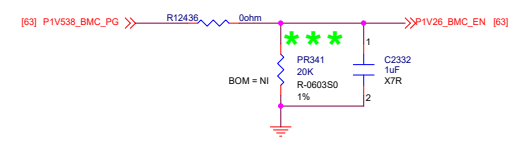
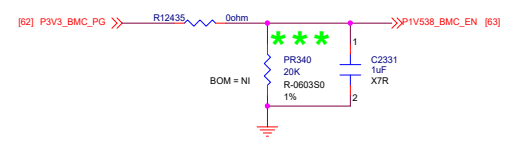
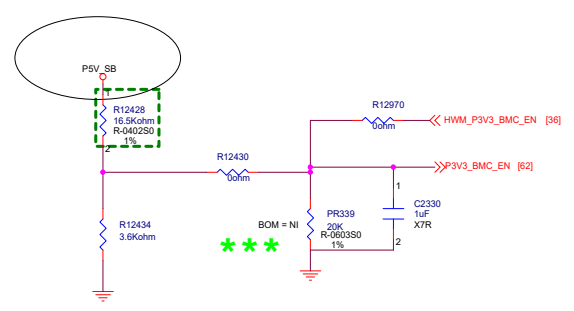
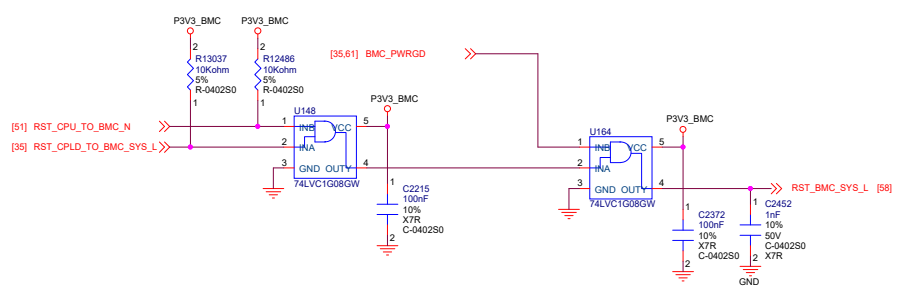
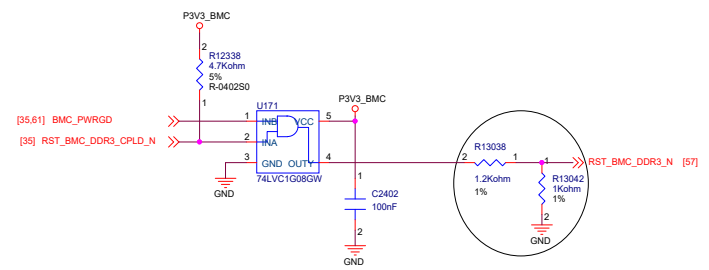
ROMD[7:3] : Reserved for Software DRAM type selection



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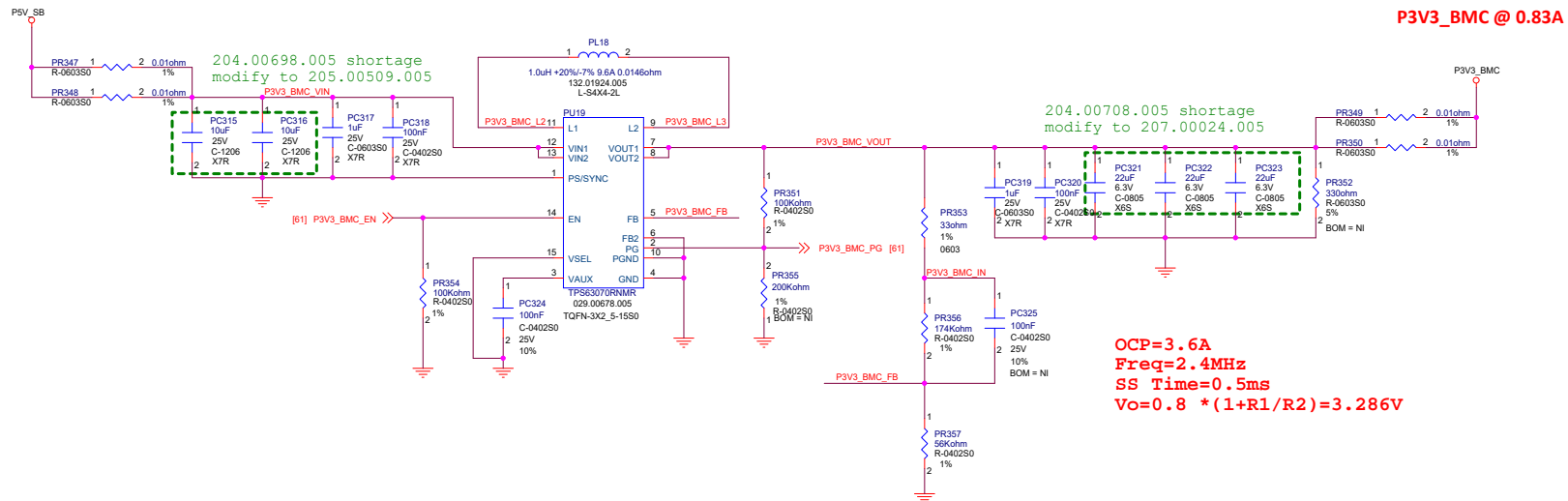
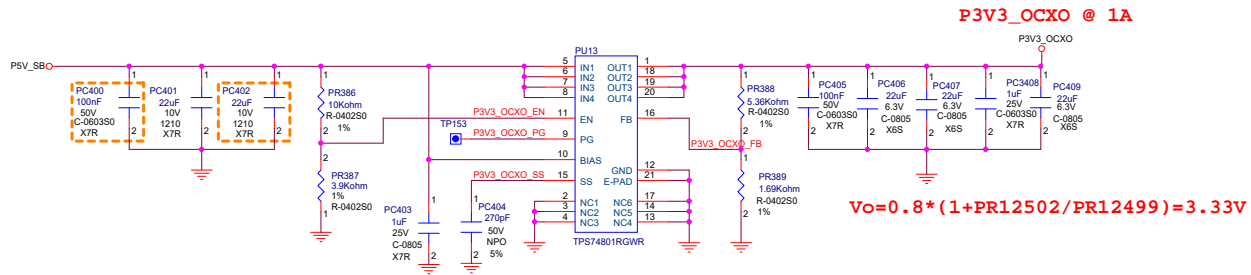


RT9817 is push pull type with 220ms delay



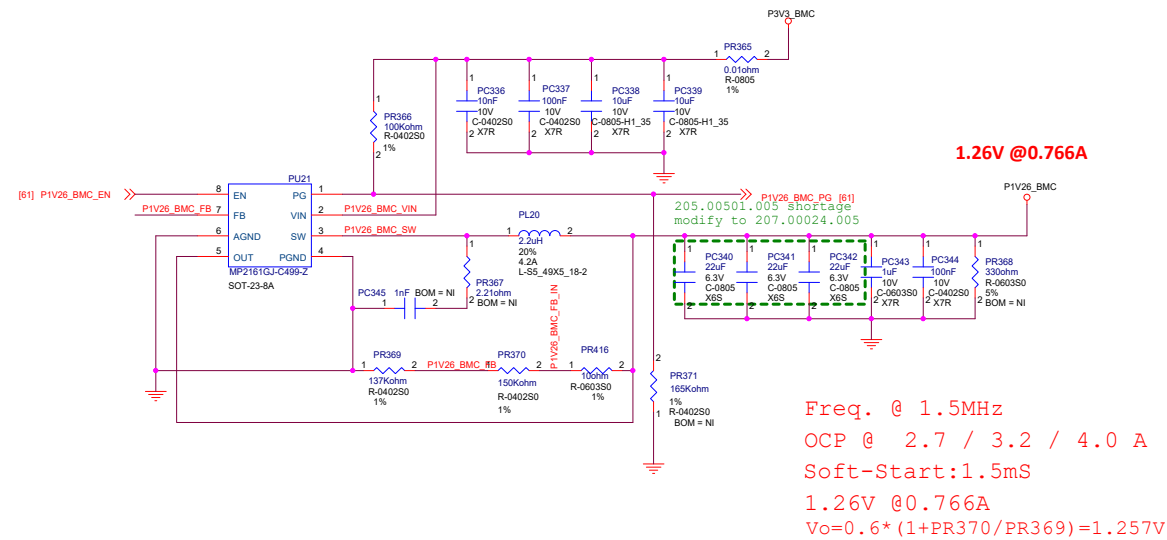
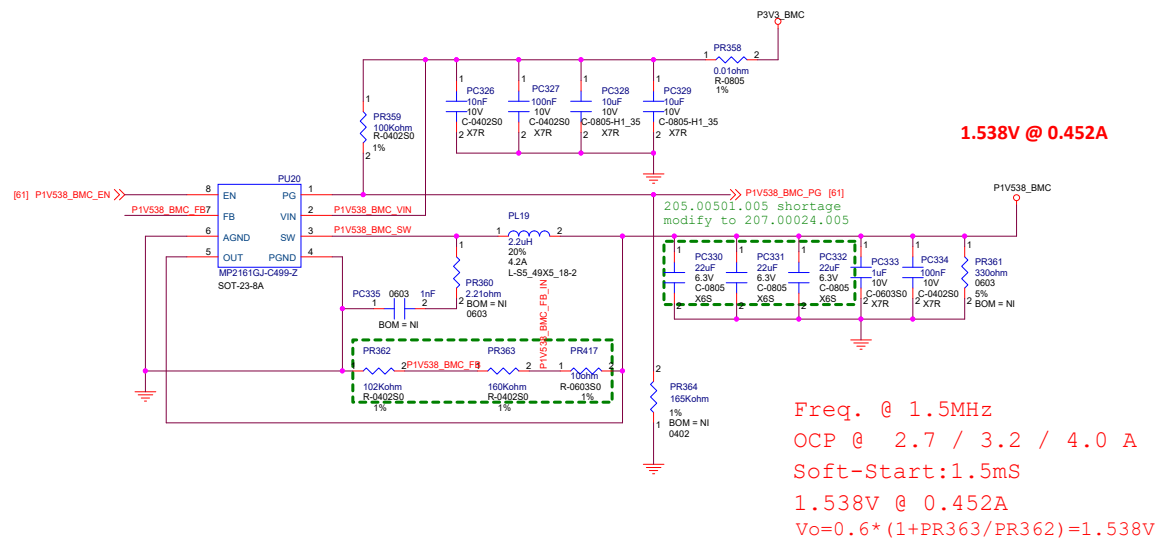
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# BMC\_PWR SEQUENCE & RESET



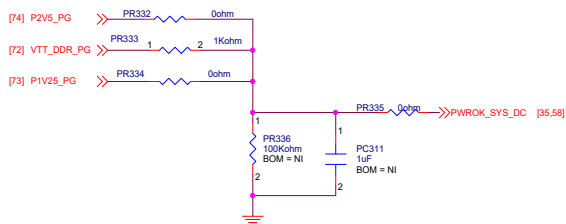
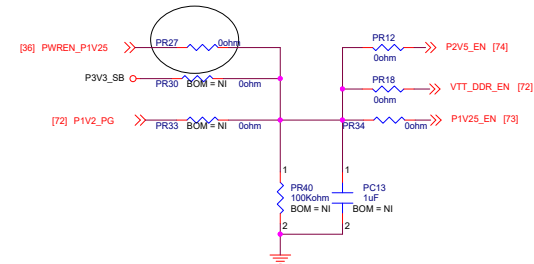
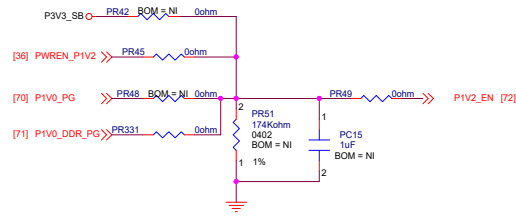
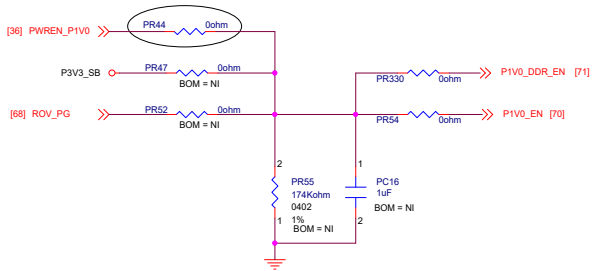
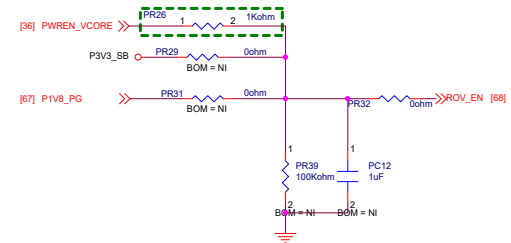
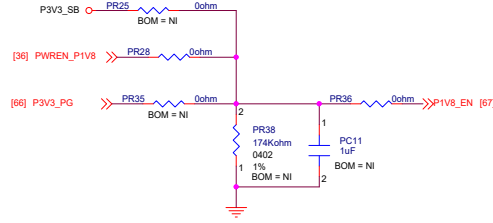
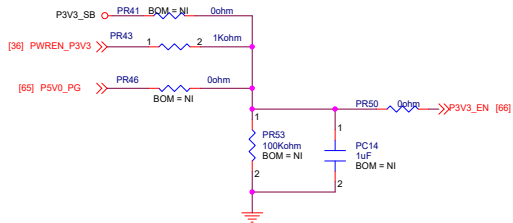
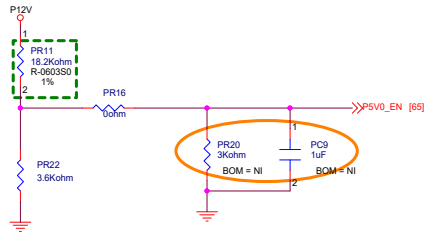
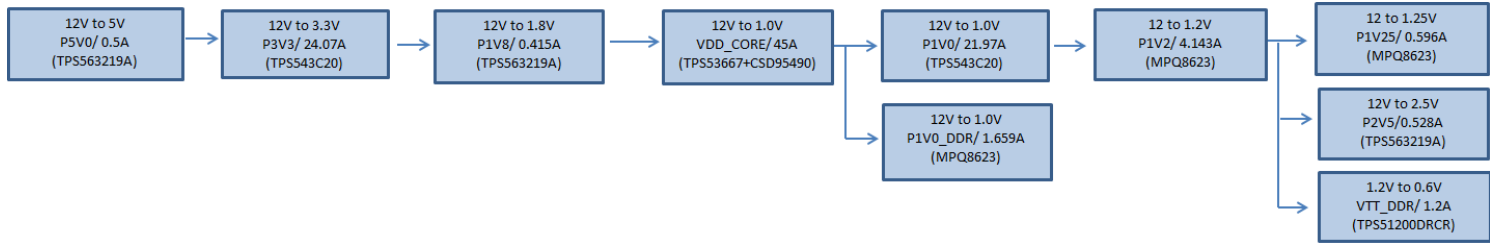
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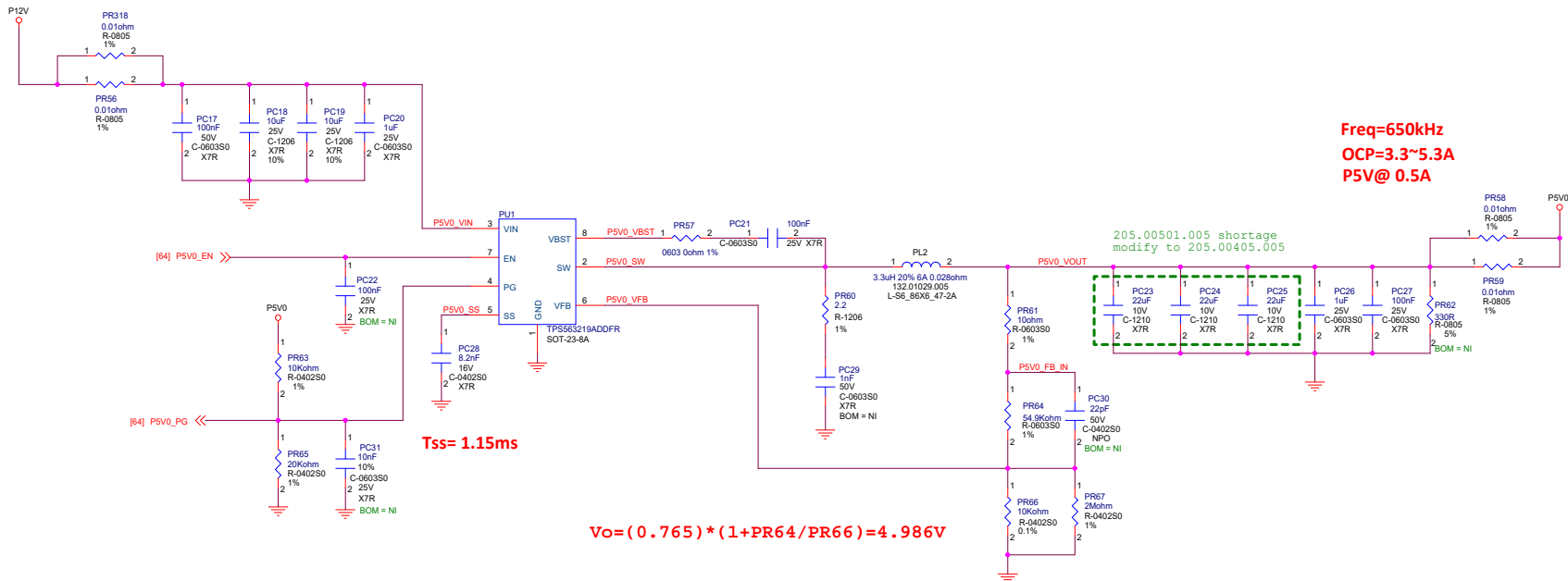
# BMC\_DC\_3.3V TO 1.538V & 1.26V



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# DC\_PWR UP SEQUENCE

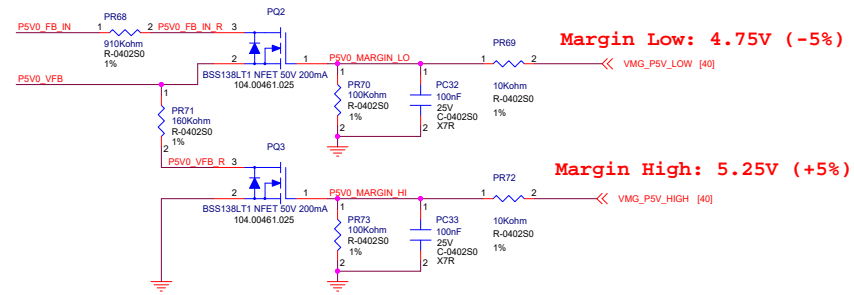




Freq=650kHz  
 OCP=3.3~5.3A  
 P5V@ 0.5A

Tss= 1.15ms

$$V_o = (0.765) * (1 + PR64 / PR66) = 4.986V$$



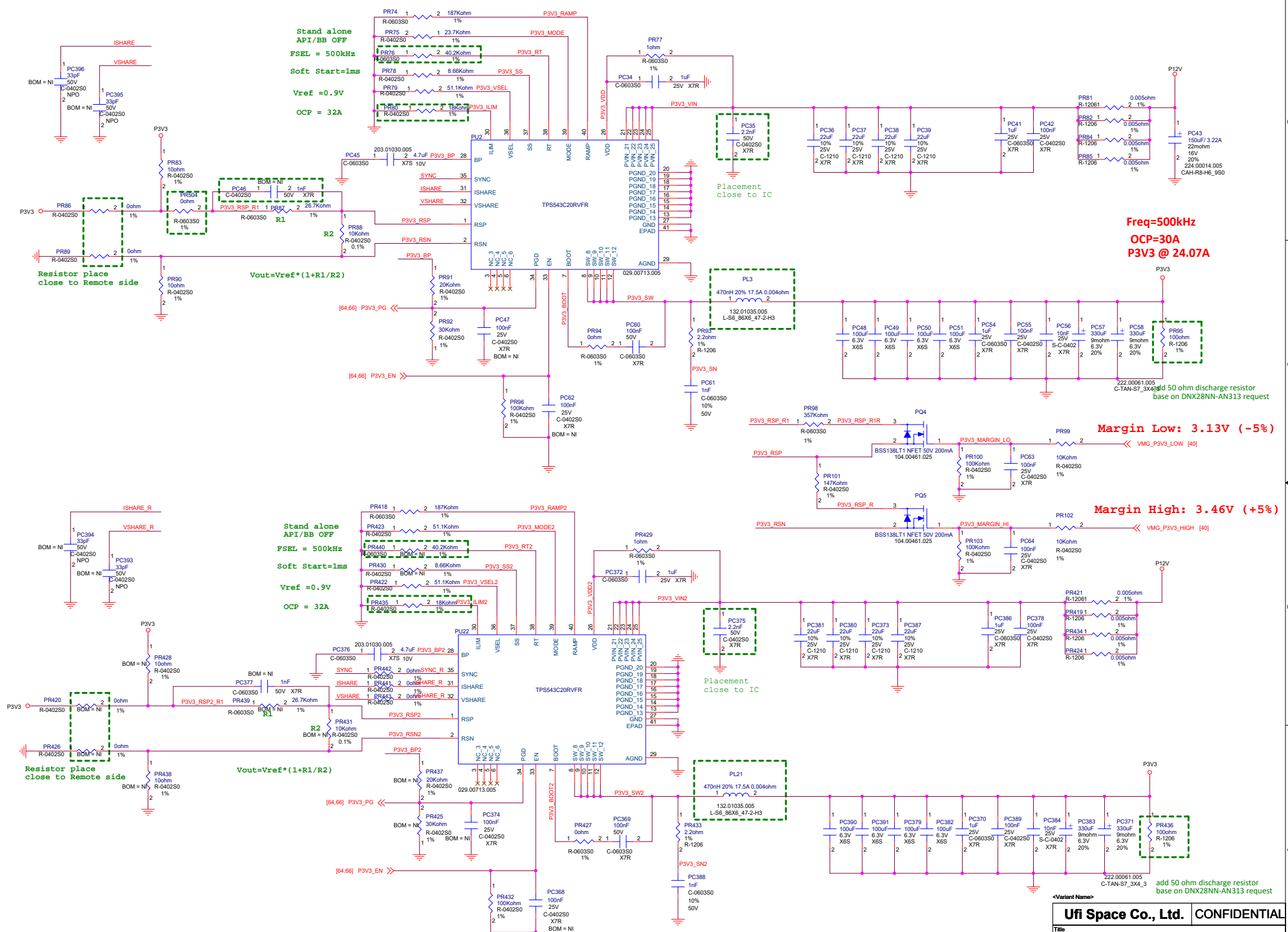
Margin Low: 4.75V (-5%)

Margin High: 5.25V (+5%)

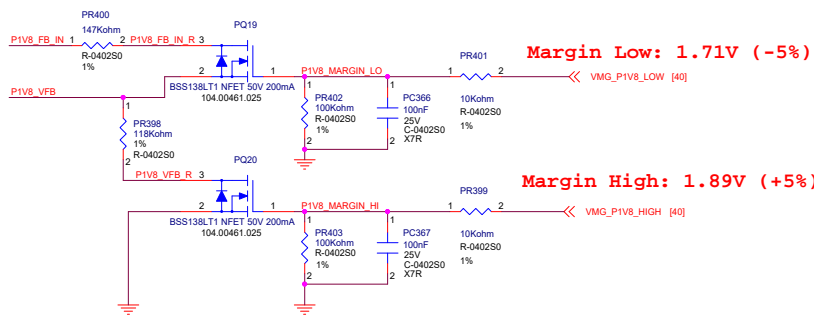
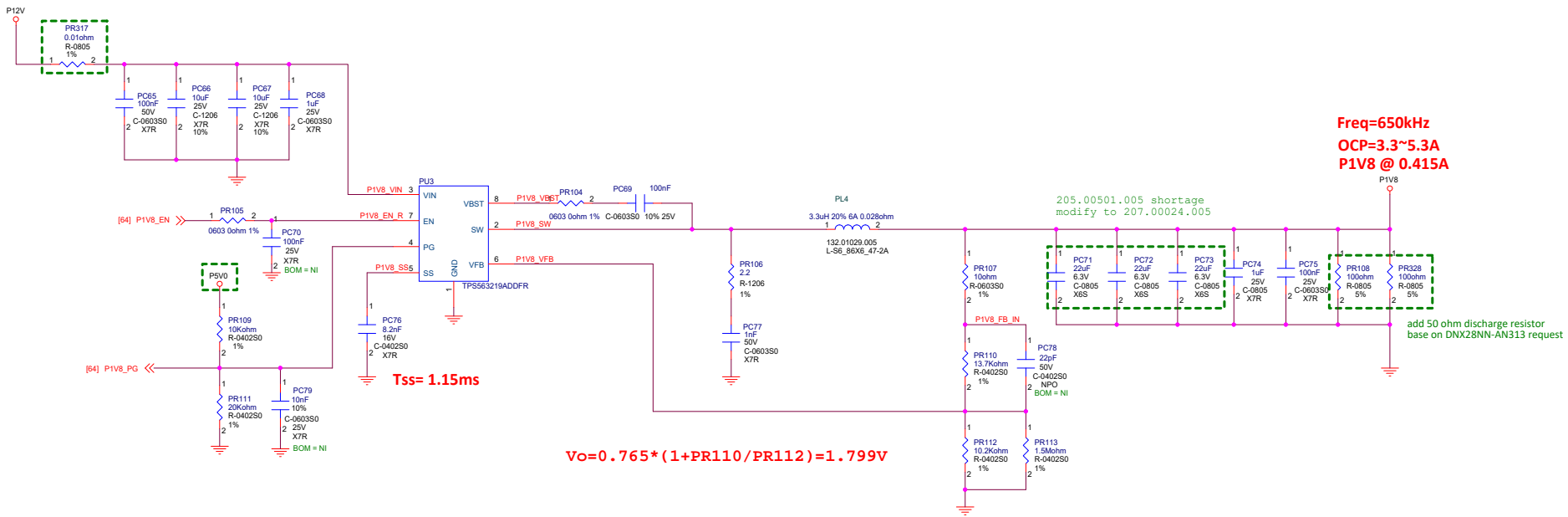
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# DC\_PWR\_12V TO 5V

# DC\_PWR\_12V TO 3.3V



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Freq=650kHz  
 OCP=3.3~5.3A  
 P1V8 @ 0.415A

Tss=1.15ms

$$V_o = 0.765 * (1 + PR110 / PR112) = 1.799V$$

Margin Low: 1.71V (-5%)

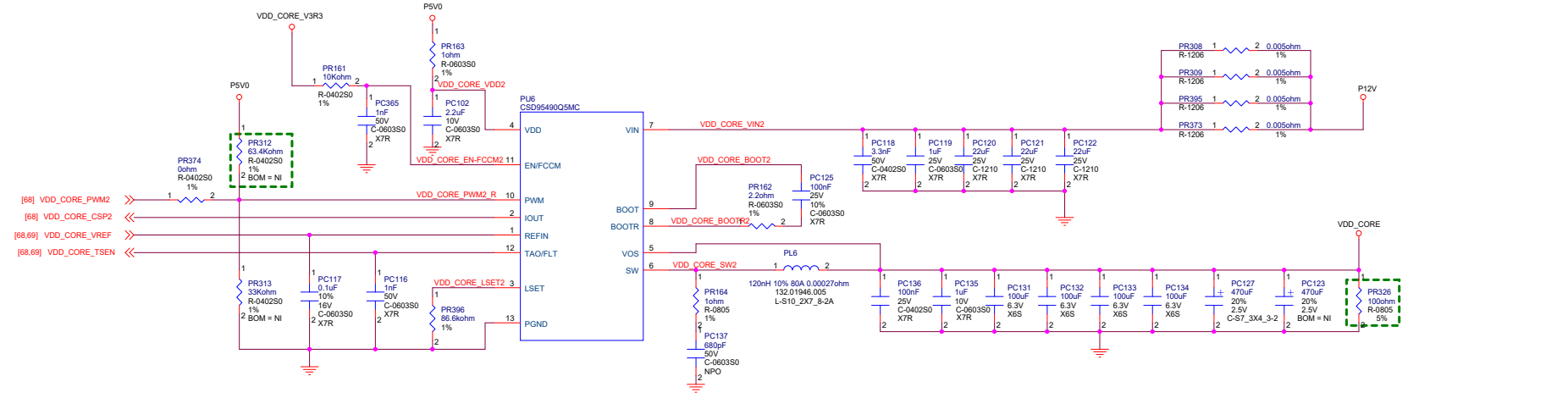
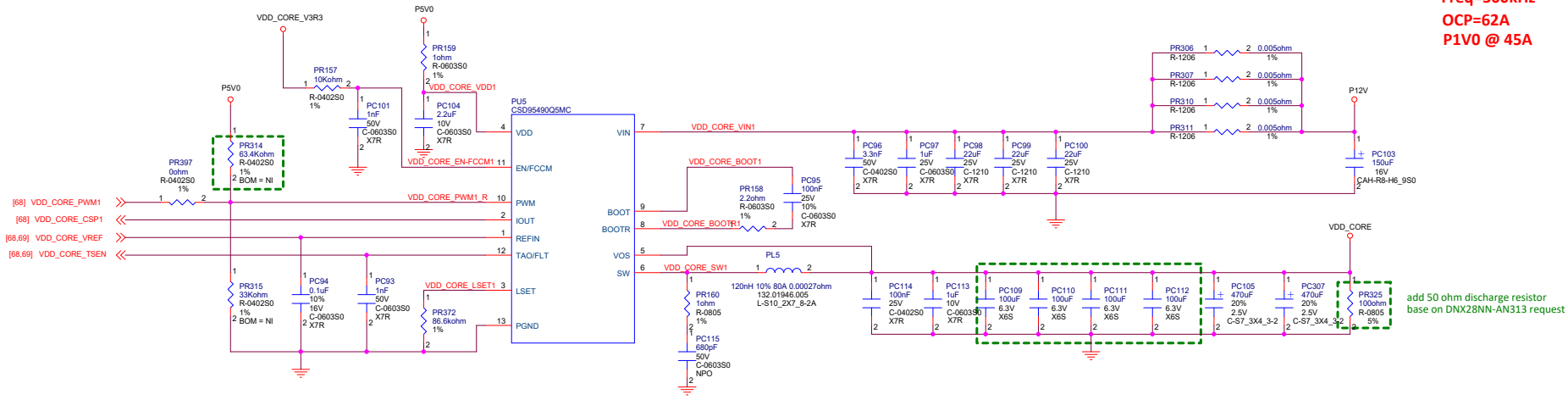
Margin High: 1.89V (+5%)

<Variant Name>

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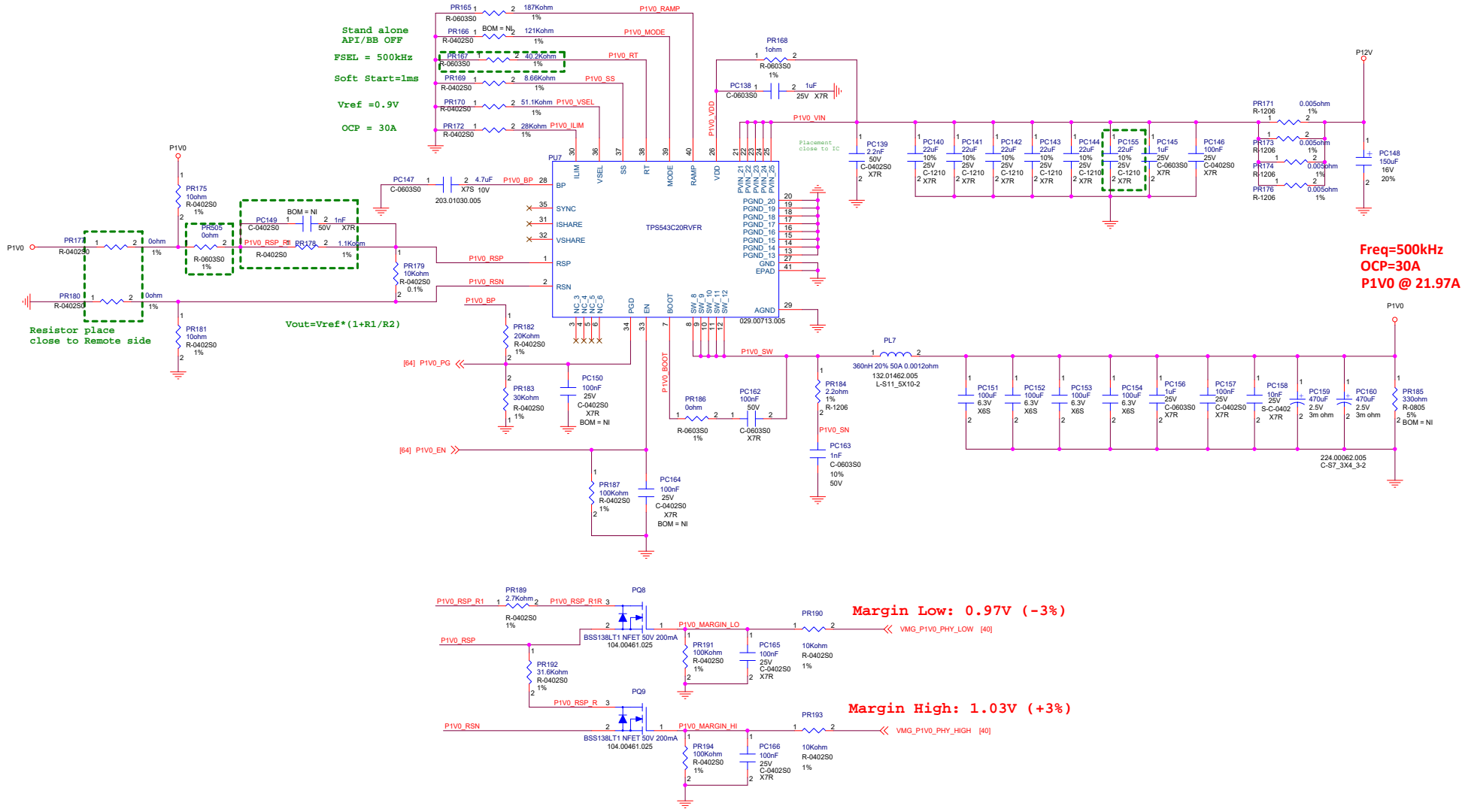
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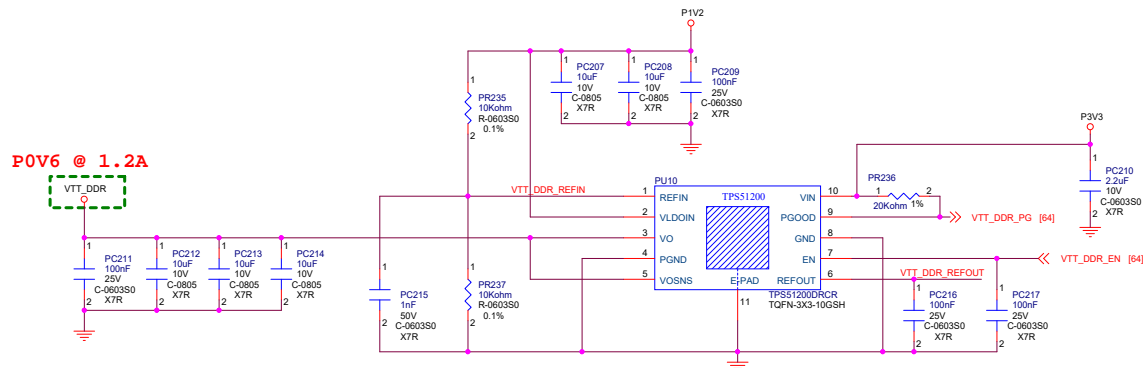
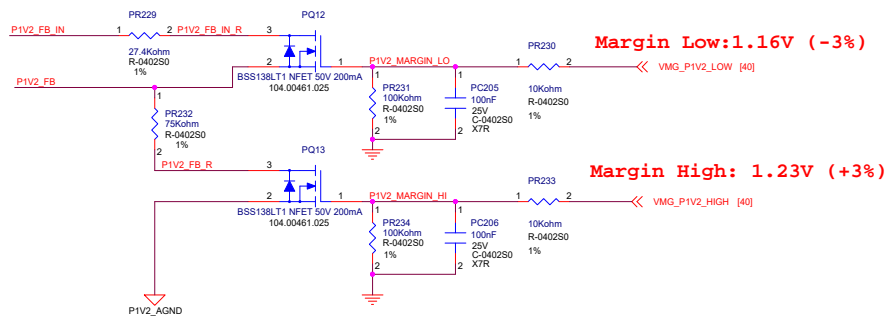
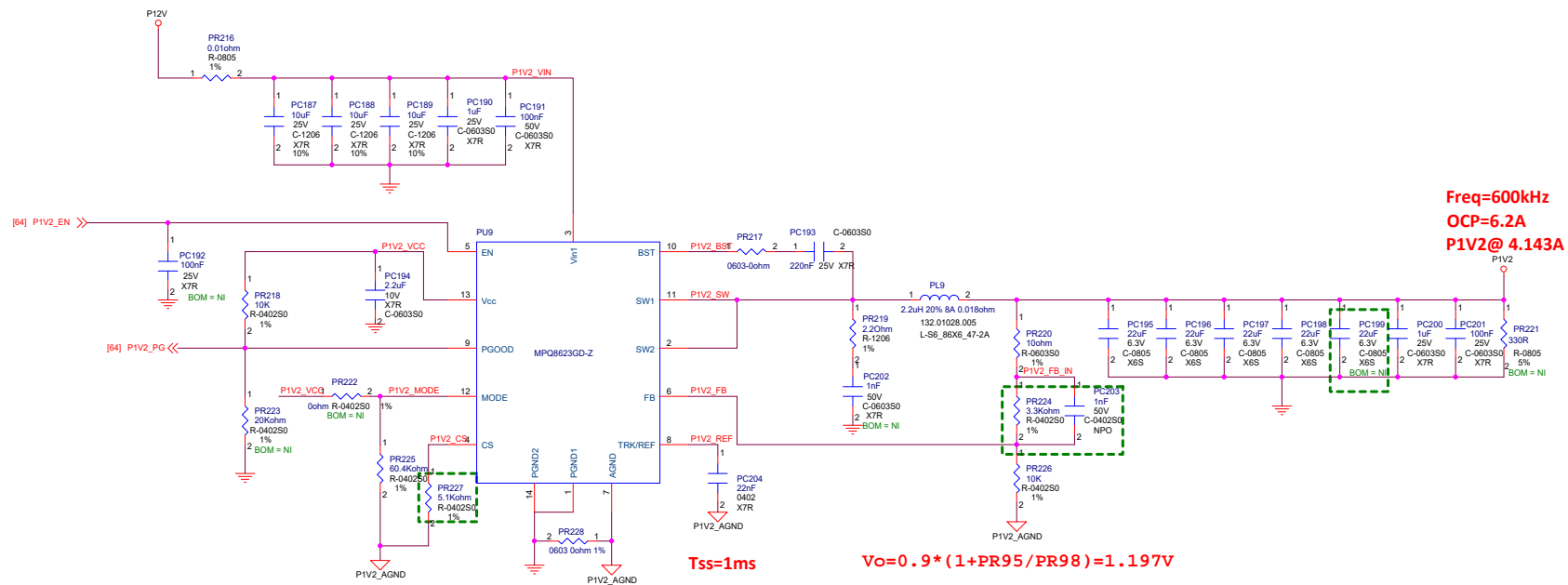
# DC\_PWR\_12V TO VCORE\_DRV1



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# DC\_PWR\_12V TO 1.0V



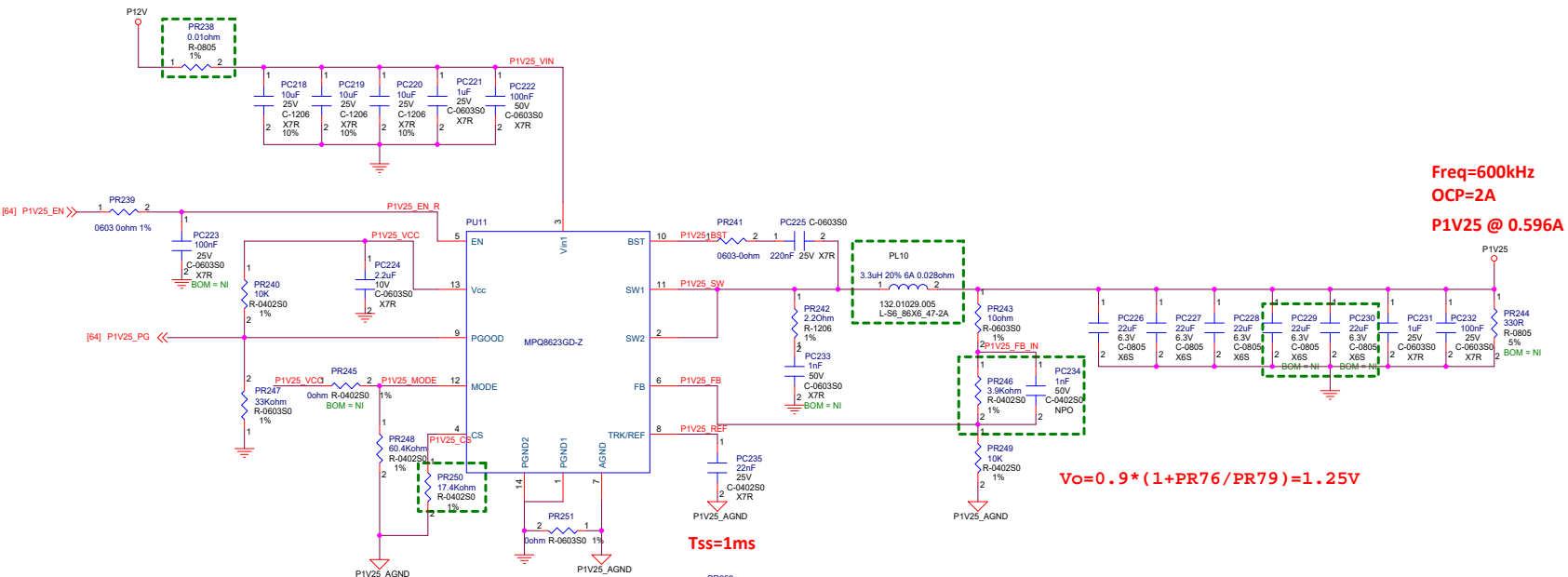


<Core Design>

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# DC\_PWR\_12V TO 1.2V & 0.6V

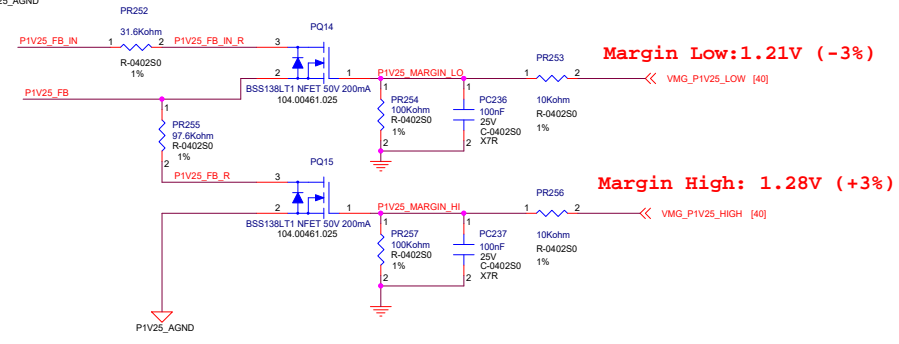




Freq=600kHz  
 OCP=2A  
 P1V25 @ 0.596A

$$V_o = 0.9 * (1 + PR76 / PR79) = 1.25V$$

Tss=1ms

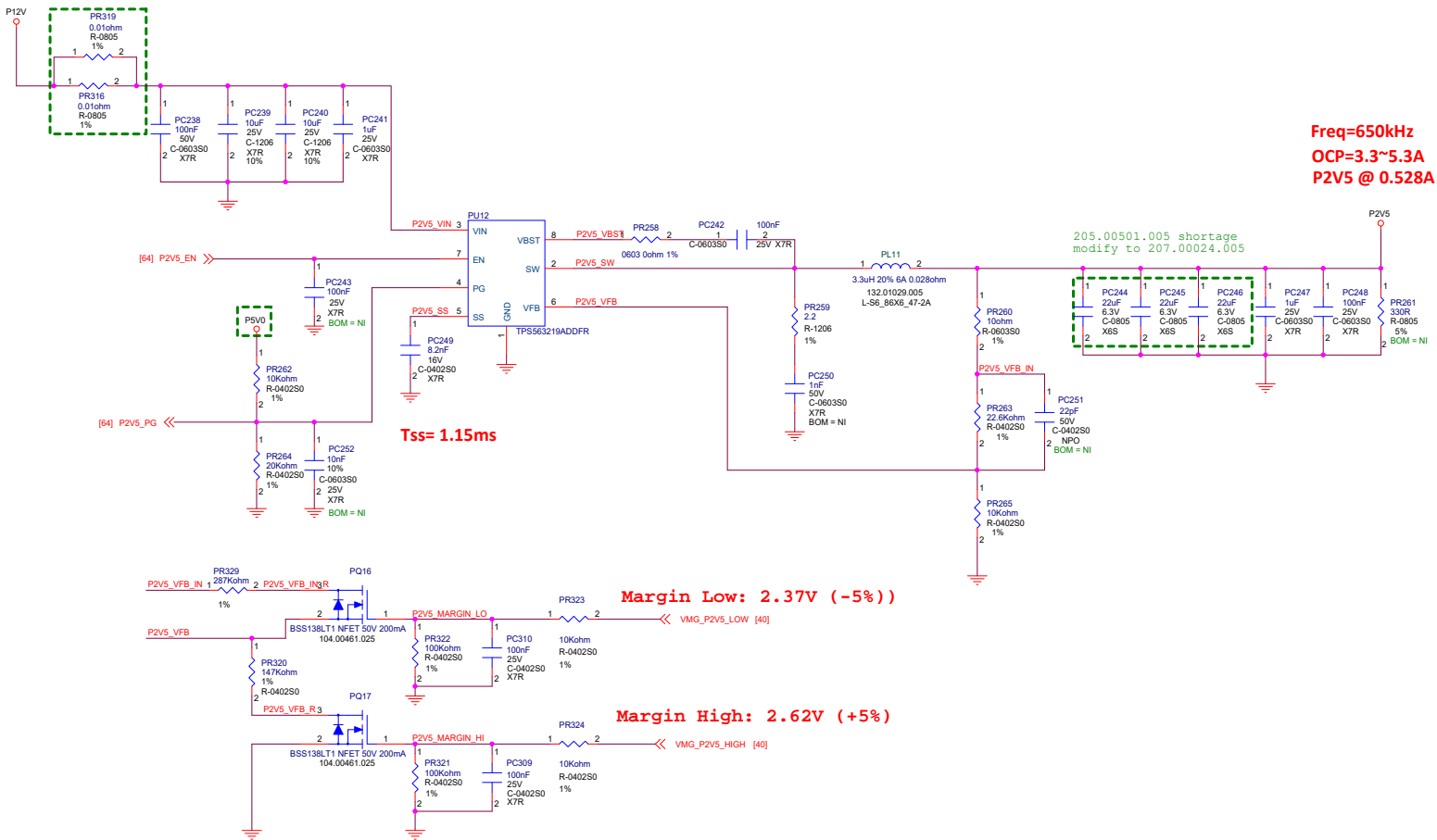


Margin Low: 1.21V (-3%)

Margin High: 1.28V (+3%)

# DC\_PWR\_12V TO 1.25V

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**Freq=650kHz**  
**OCP=3.3~5.3A**  
**P2V5 @ 0.528A**

**Tss=1.15ms**

**Margin Low: 2.37V (-5%)**

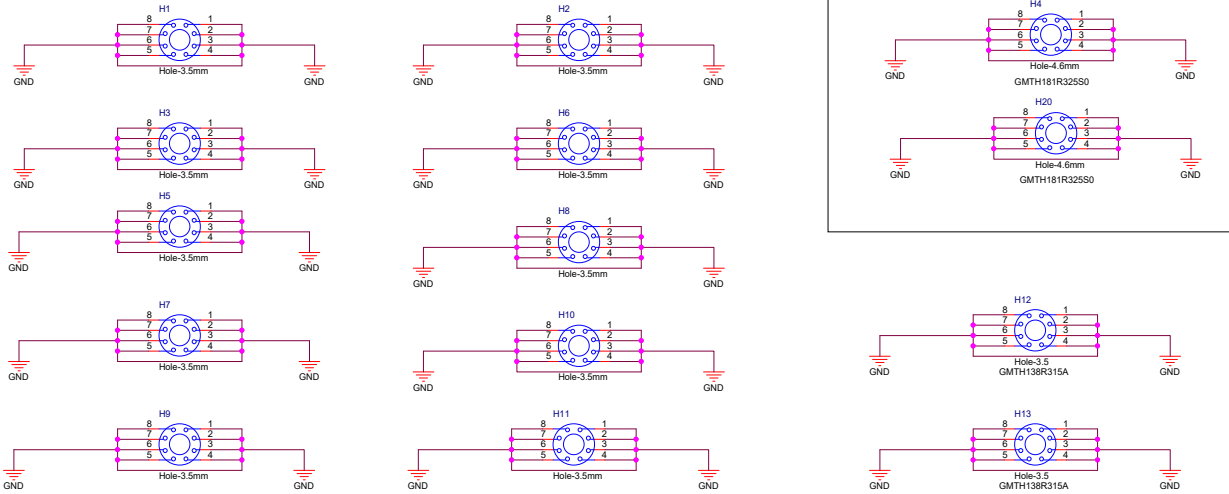
**Margin High: 2.62V (+5%)**

205.00501.005 shortage  
modify to 207.00024.005

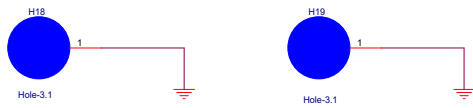
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# DC\_PWR\_12V TO 2.5V

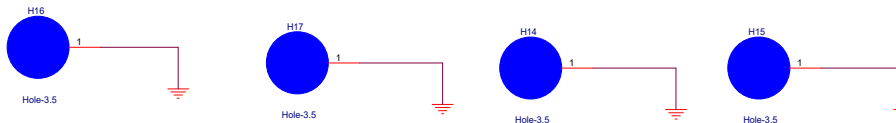
### MOUNTING HOLES



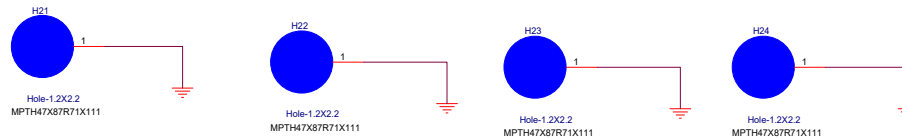
### PHY's HEATSINK HOLES



### MAC's HEATSINK HOLES



### OCXO SHIELDING COVER HOLES



SN_LABEL R03.00899.005	PCB R04.01088.015	BMC_LABEL JSS008
SN_LABEL SN Label	PCB	BMC_LABEL Legal Fee Sticker
HEATER [SKP2020L70 5-5.5 GRM	HS1 R00.00728.005	HS2 R00.00747.005
BMC_HEATER Heater	FOR_BCM92391 HS_PHY_100G	FOR_BCM92780 HS_PHY_10G
COVER R26.05346.005		
OCXO SHIELDING COVER SHIELDING COVER		

<Core Design>

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