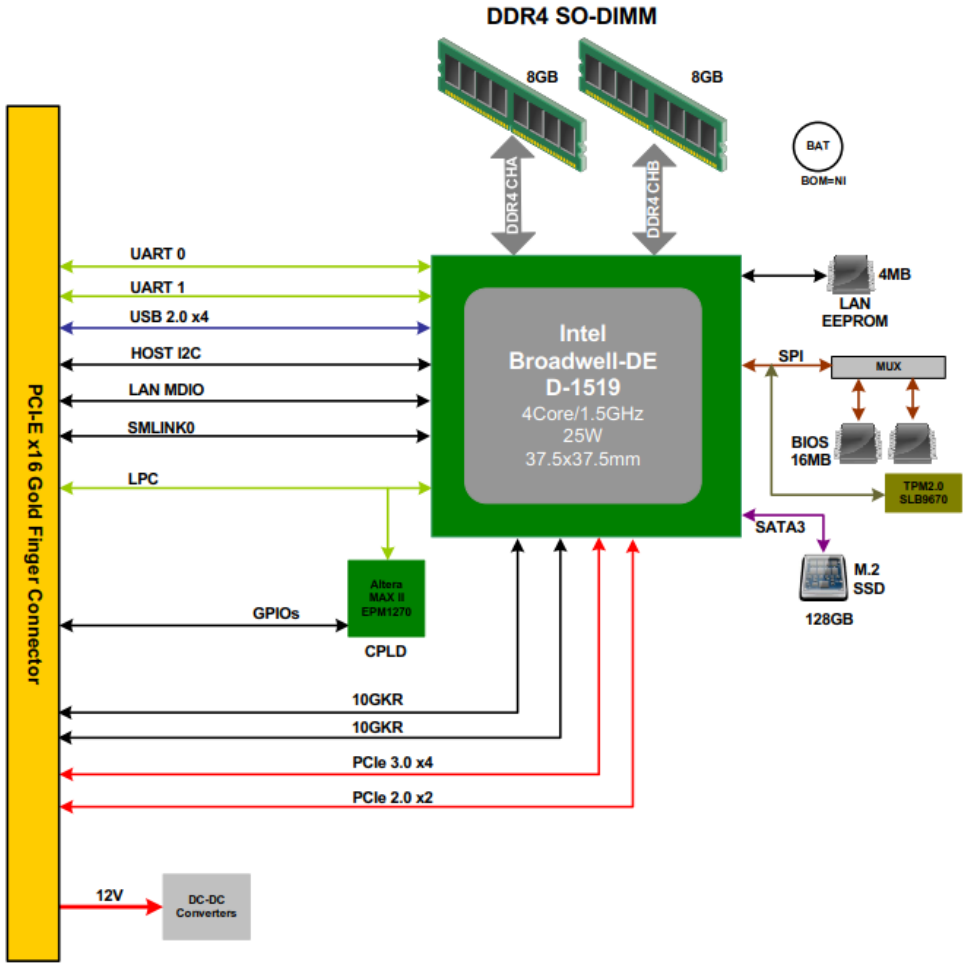
CSGR CPU



<Core Design>

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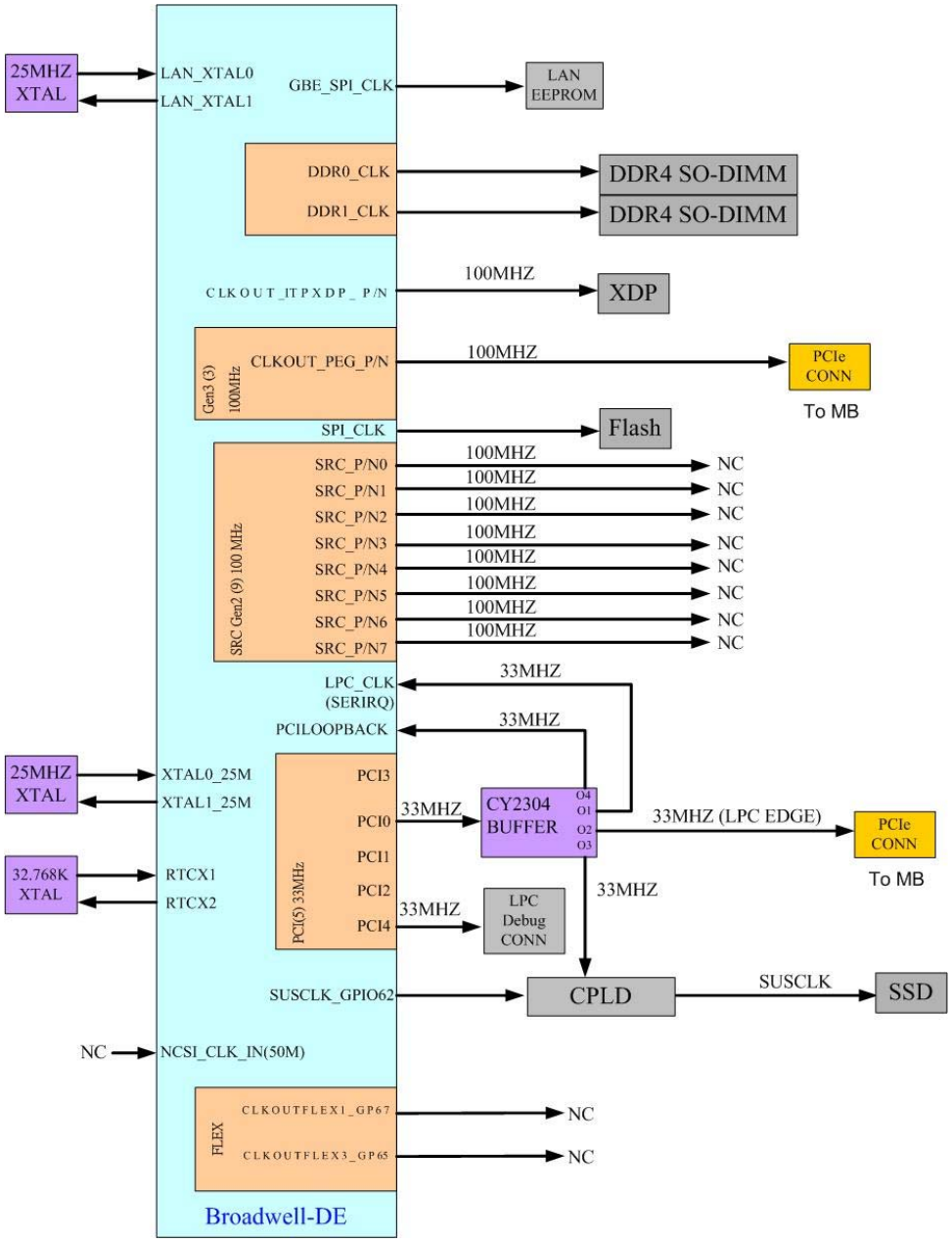

<Core Design>

Ufi Space Co., Ltd.	CONFIDENTIAL
Title: 03. CLOCK DIAGRAM	
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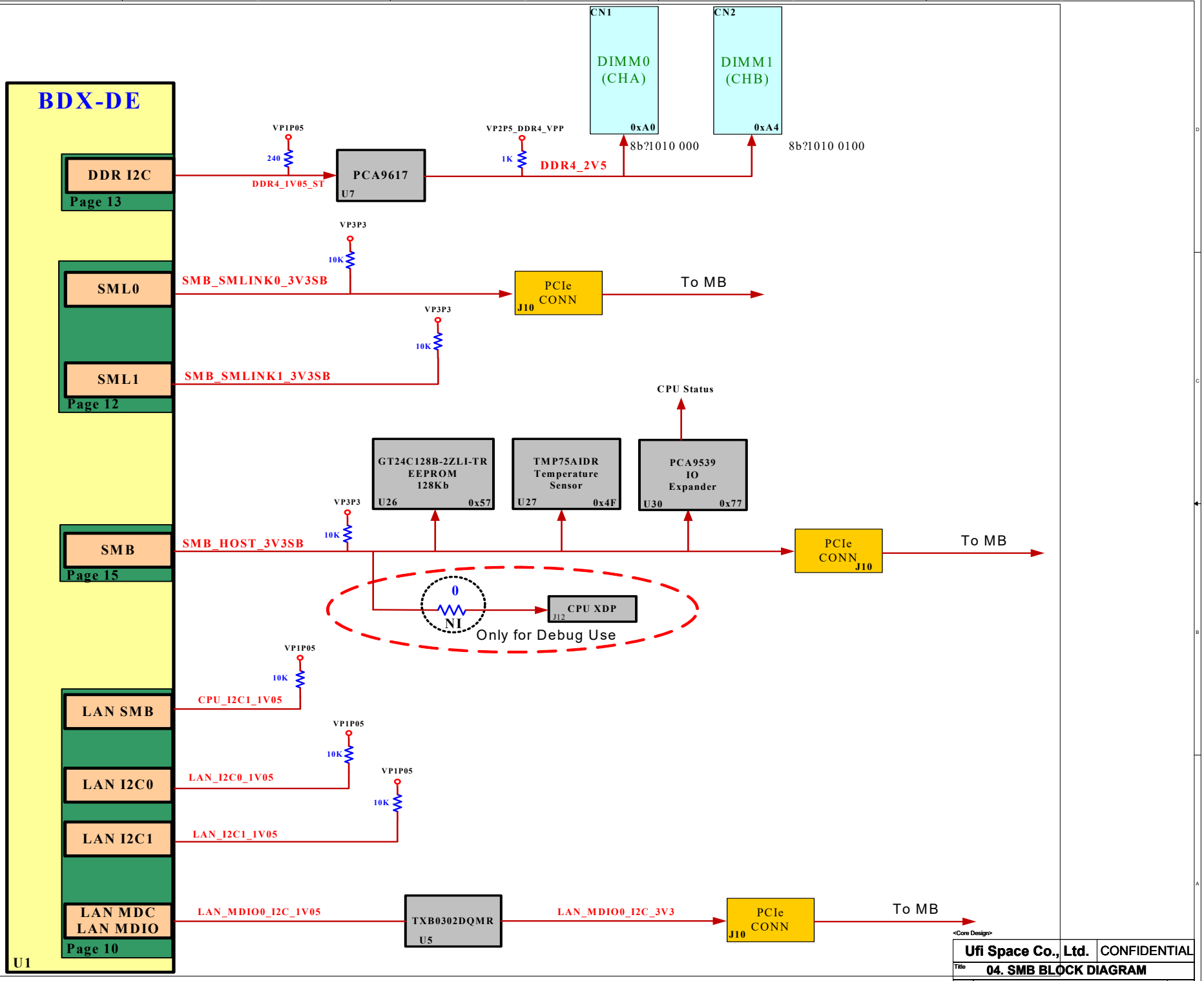

<Core Design>

Ufi Space Co., Ltd.		CONFIDENTIAL
Title	04. SMB BLOCK DIAGRAM	
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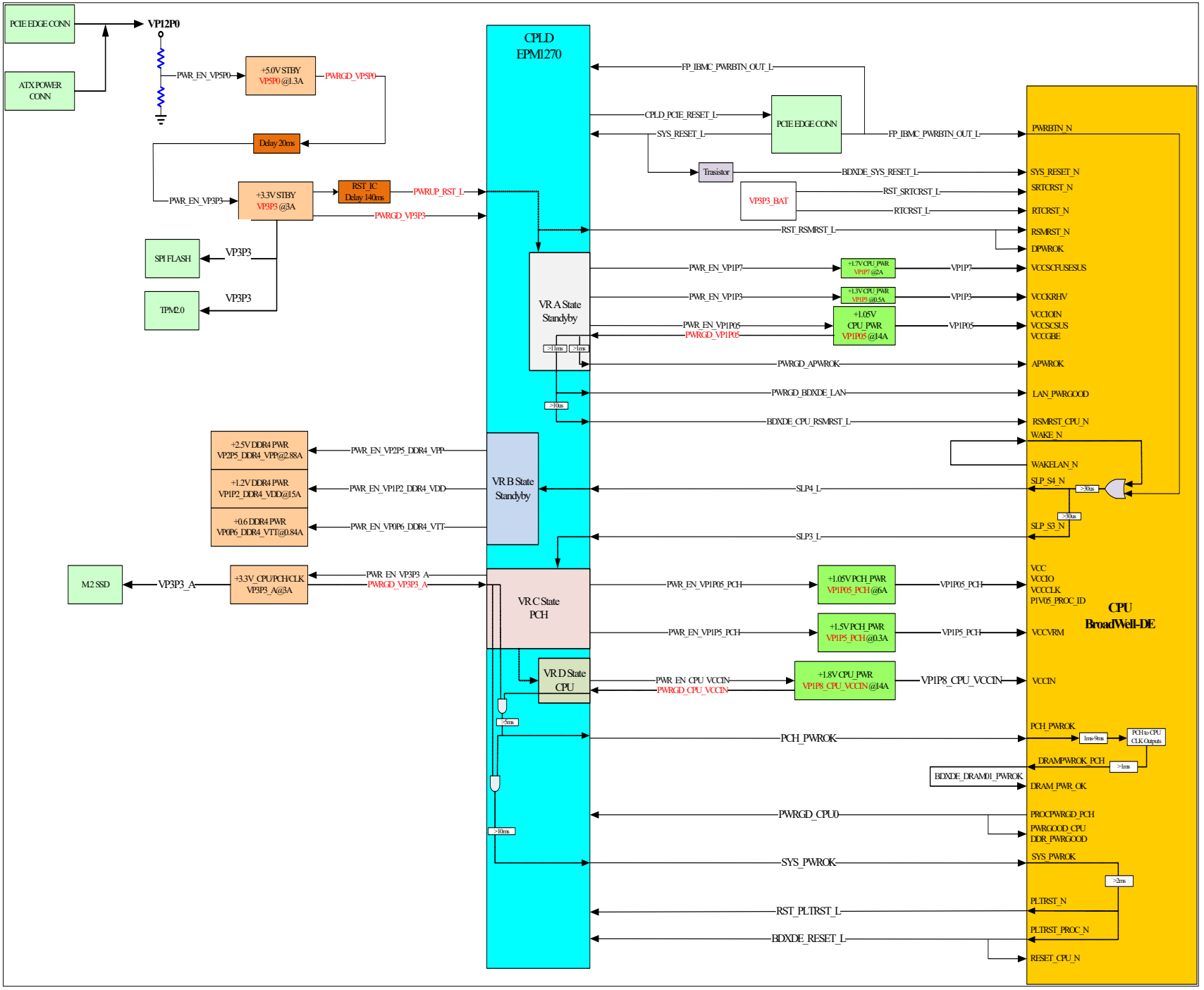

<Core Design>

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Title	05. RESET BLOCK DIAGRAM	
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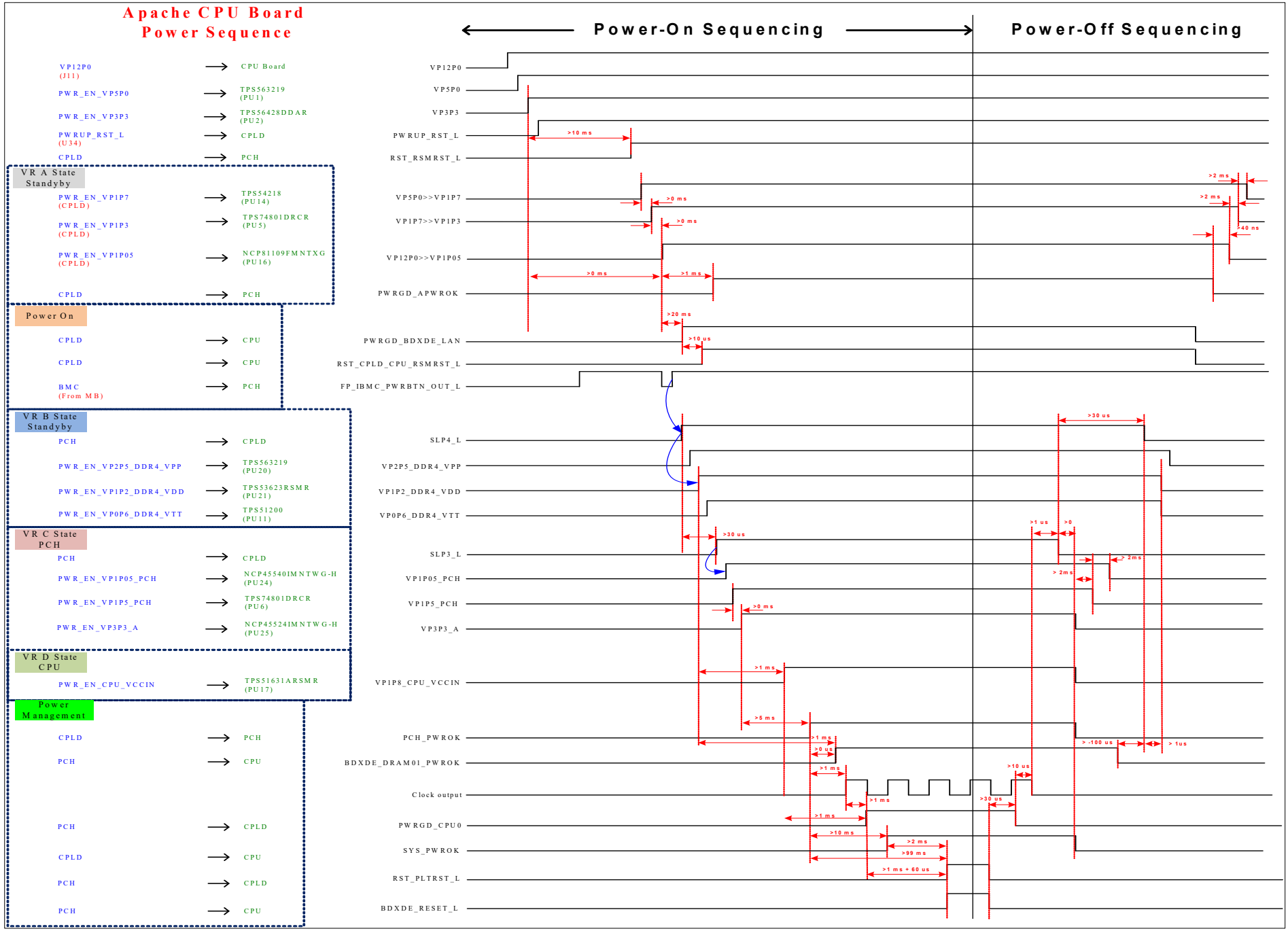
Apache CPU Board Power Sequence



<Core Design>

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Title: 06. POWER SEQUENCE		
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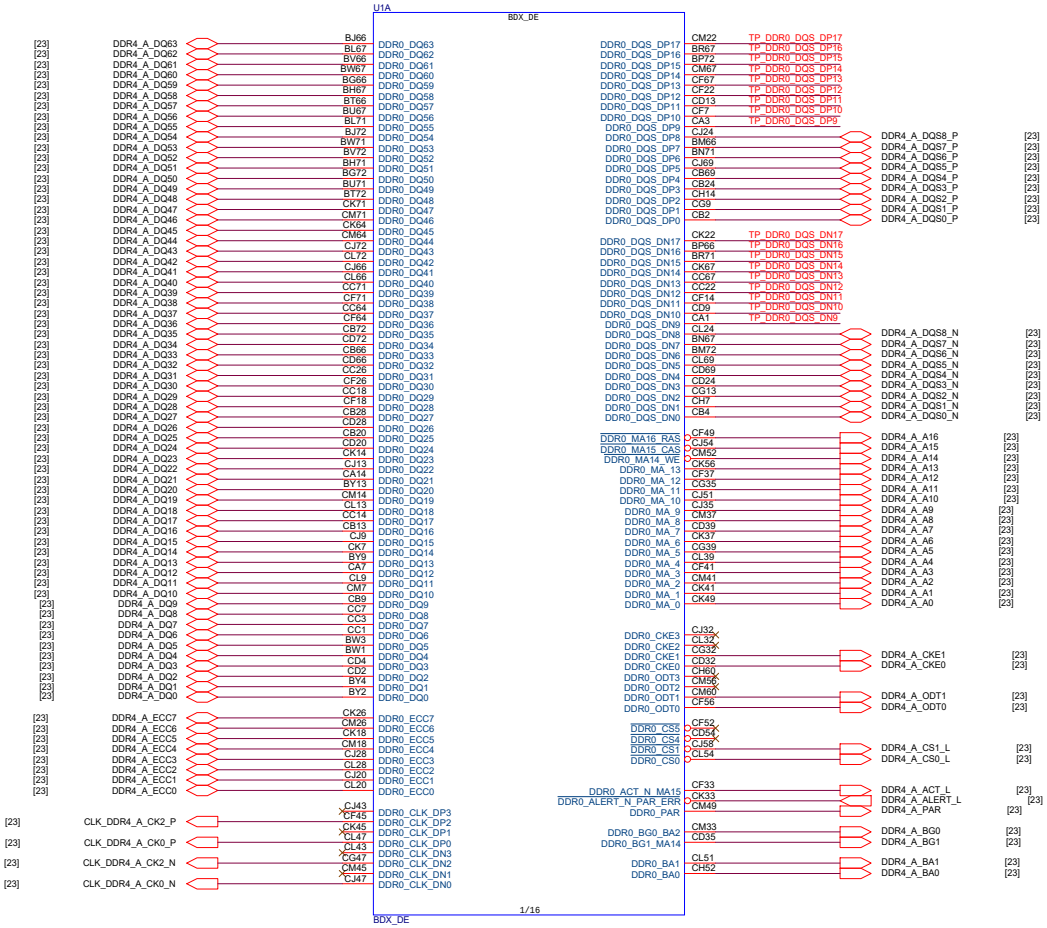
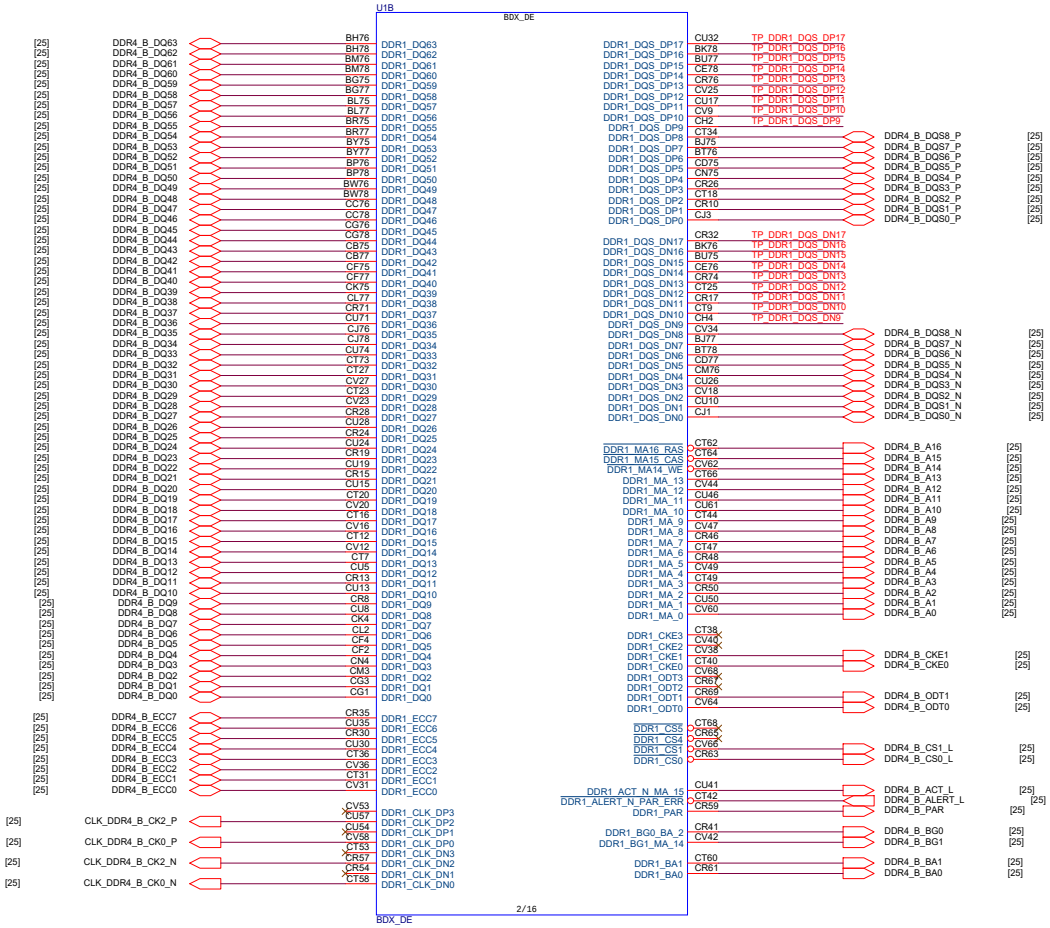

U1A
BDX_DE
DDR0_DQ63
DDR0_DQ62
DDR0_DQ61
DDR0_DQ60
DDR0_DQ59
DDR0_DQ58
DDR0_DQ57
DDR0_DQ56
DDR0_DQ55
DDR0_DQ54
DDR0_DQ53
DDR0_DQ52
DDR0_DQ51
DDR0_DQ50
DDR0_DQ49
DDR0_DQ48
DDR0_DQ47
DDR0_DQ46
DDR0_DQ45
DDR0_DQ44
DDR0_DQ43
DDR0_DQ42
DDR0_DQ41
DDR0_DQ40
DDR0_DQ39
DDR0_DQ38
DDR0_DQ37
DDR0_DQ36
DDR0_DQ35
DDR0_DQ34
DDR0_DQ33
DDR0_DQ32
DDR0_DQ31
DDR0_DQ30
DDR0_DQ29
DDR0_DQ28
DDR0_DQ27
DDR0_DQ26
DDR0_DQ25
DDR0_DQ24
DDR0_DQ23
DDR0_DQ22
DDR0_DQ21
DDR0_DQ20
DDR0_DQ19
DDR0_DQ18
DDR0_DQ17
DDR0_DQ16
DDR0_DQ15
DDR0_DQ14
DDR0_DQ13
DDR0_DQ12
DDR0_DQ11
DDR0_DQ10
DDR0_DQ9
DDR0_DQ8
DDR0_DQ7
DDR0_DQ6
DDR0_DQ5
DDR0_DQ4
DDR0_DQ3
DDR0_DQ2
DDR0_DQ1
DDR0_DQ0
DDR0_ECC7
DDR0_ECC6
DDR0_ECC5
DDR0_ECC4
DDR0_ECC3
DDR0_ECC2
DDR0_ECC1
DDR0_ECC0
DDR0_CLK_DP3
DDR0_CLK_DP2
DDR0_CLK_DP1
DDR0_CLK_DP0
DDR0_CLK_DN3
DDR0_CLK_DN2
DDR0_CLK_DN1
DDR0_CLK_DN0
DDR0_DQS_DP17
DDR0_DQS_DP16
DDR0_DQS_DP15
DDR0_DQS_DP14
DDR0_DQS_DP13
DDR0_DQS_DP12
DDR0_DQS_DP11
DDR0_DQS_DP10
DDR0_DQS_DP9
DDR0_DQS_DP8
DDR0_DQS_DP7
DDR0_DQS_DP6
DDR0_DQS_DP5
DDR0_DQS_DP4
DDR0_DQS_DP3
DDR0_DQS_DP2
DDR0_DQS_DP1
DDR0_DQS_DP0
DDR0_DQS_DN17
DDR0_DQS_DN16
DDR0_DQS_DN15
DDR0_DQS_DN14
DDR0_DQS_DN13
DDR0_DQS_DN12
DDR0_DQS_DN11
DDR0_DQS_DN10
DDR0_DQS_DN9
DDR0_DQS_DN8
DDR0_DQS_DN7
DDR0_DQS_DN6
DDR0_DQS_DN5
DDR0_DQS_DN4
DDR0_DQS_DN3
DDR0_DQS_DN2
DDR0_DQS_DN1
DDR0_DQS_DN0
DDR0_MA16_RAS
DDR0_MA15_CAS
DDR0_MA14_WE
DDR0_MA_13
DDR0_MA_12
DDR0_MA_11
DDR0_MA_10
DDR0_MA_9
DDR0_MA_8
DDR0_MA_7
DDR0_MA_6
DDR0_MA_5
DDR0_MA_4
DDR0_MA_3
DDR0_MA_2
DDR0_MA_1
DDR0_MA_0
DDR0_CKE3
DDR0_CKE2
DDR0_CKE1
DDR0_CKE0
DDR0_ODT3
DDR0_ODT2
DDR0_ODT1
DDR0_ODT0
DDR0_CS3
DDR0_CS2
DDR0_CS1
DDR0_CS0
DDR0_ACT_N_MA15
DDR0_ALERT_N_PAR_ERR
DDR0_PAR
DDR0_BG0_BA2
DDR0_BG1_MA14
DDR0_BA1
DDR0_BA0
1/16
BDX_DE



<Core Design>

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Ufi Space Co., Ltd.	CONFIDENTIAL
Title: 09. CPU PCIE	
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CAD:
TO PLACE CAPS CLOSE TO U1 LESS THAN 1"

U1D
BDX_DE

2018/05/17: Remove LAN SMBus

10GE Port #	Device
0	10GE SWITCH
1	10GE SWITCH

2018/05/21
1. Add pull up resistors R468,R469

<Core Design>

Ufi Space Co., Ltd. CONFIDENTIAL

Title: 10. CPU 10GBE LAN

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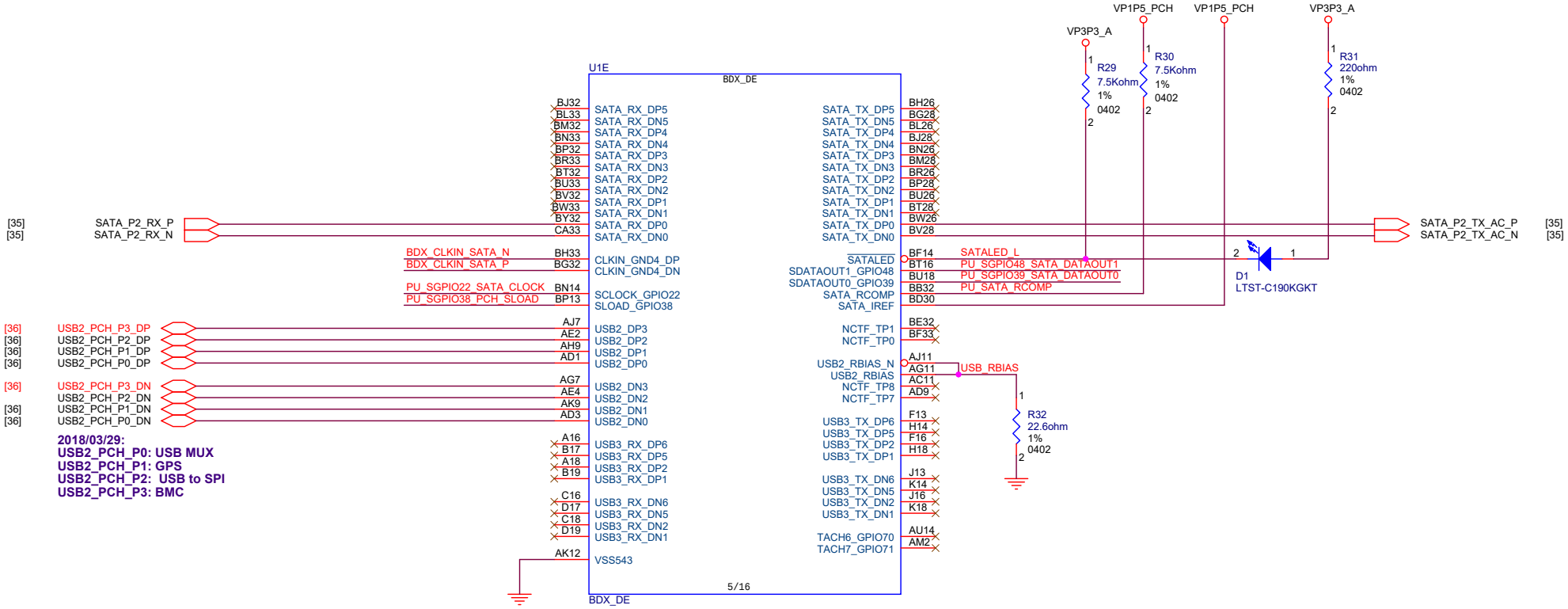

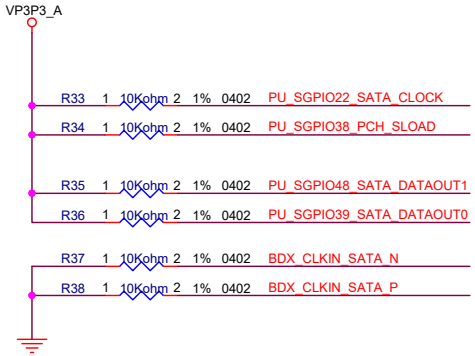

Device/Conn.	USB 2.0
GOLD FINGER CONN	0

CONN.	SATA
M.2 CONN	0
GOLD FINGER CONN	1

<Core Design>

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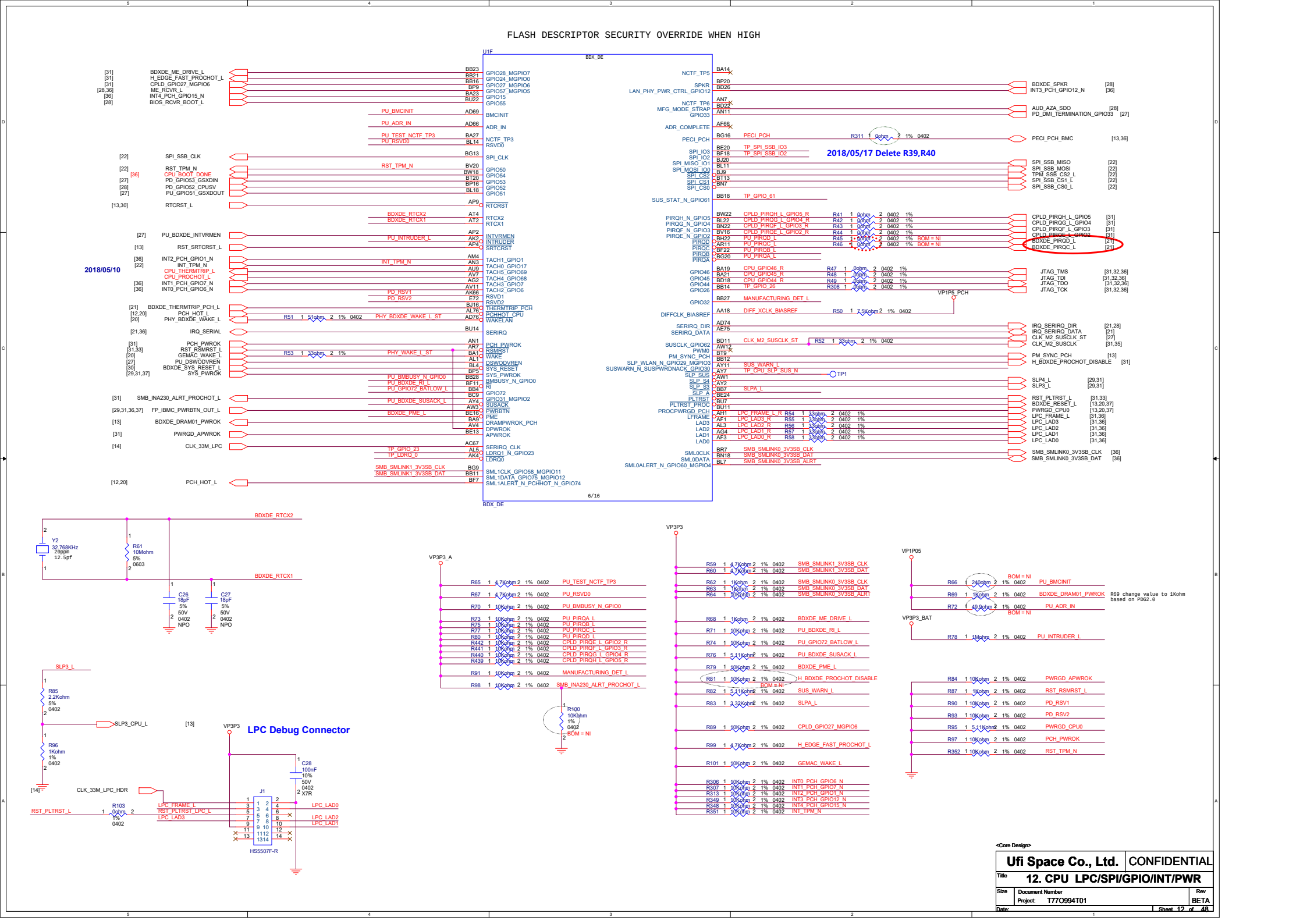
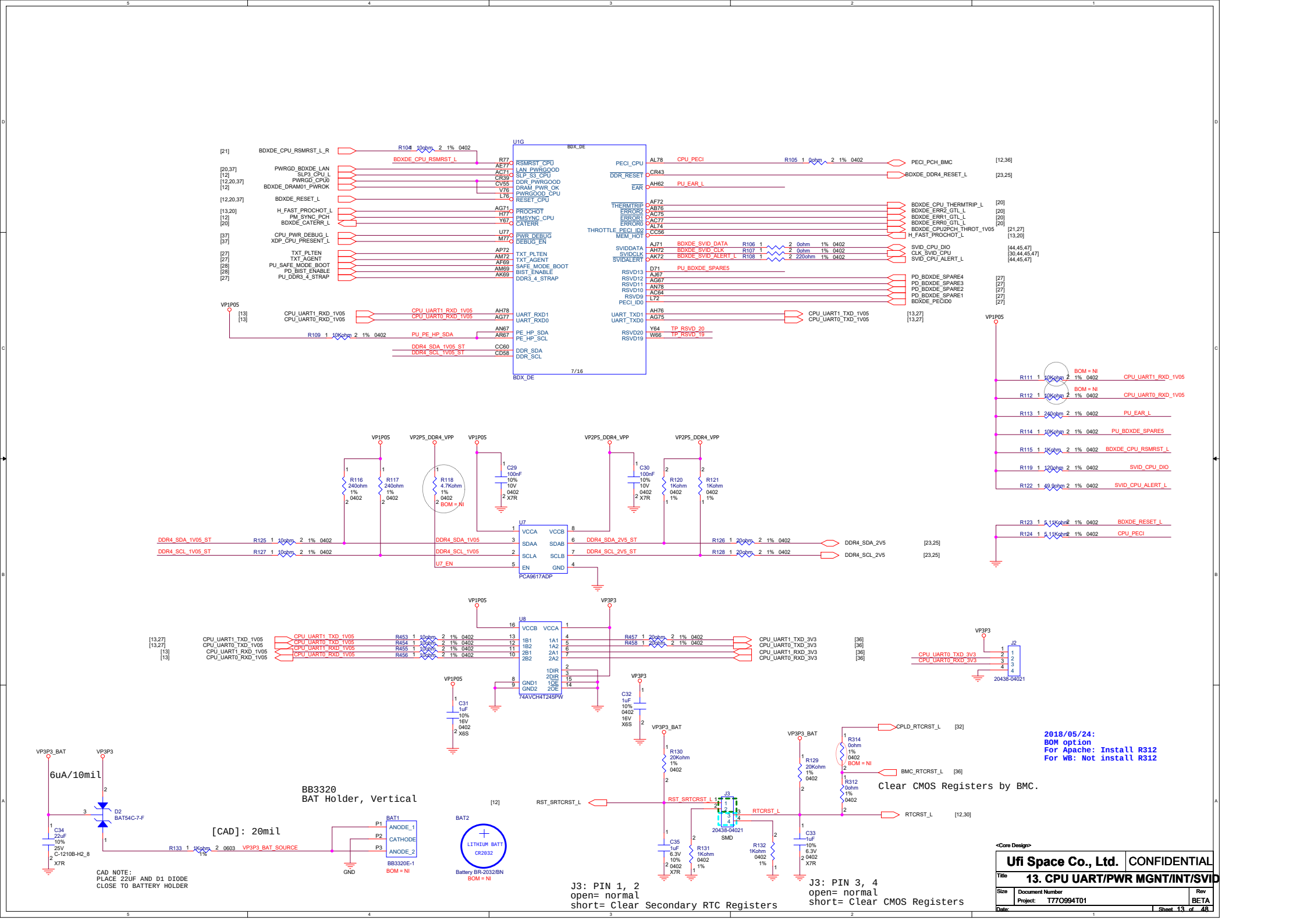
FLASH DESCRIPTOR SECURITY OVERRIDE WHEN HIGH




U1G
BDX_DE
BDXDE_CPU_RSMRST_L_R
R104 10ohm 2 1% 0402
BDXDE_CPU_RSMRST_L
PWRGD_BDXDE_LAN
SLP3_CPU_L
PWRGD_CPU0
BDXDE_DRAM01_PWROK
BDXDE_RESET_L
H_FAST_PROCHOT_L
PM_SYNC_PCH
BDXDE_CATERR_L
CPU_PWR_DEBUG_L
XDP_CPU_PRESENT_L
TXT_PLTEN
TXT_AGENT
PU_SAFE_MODE_BOOT
PD_BIST_ENABLE
PU_DDR3_4_STRAP
RSMRST_CPU
LAN_PWRGOOD
SLP_S3_CPU
DDR_PWRGOOD
DRAM_PWR_OK
PWRGOOD_CPU
RESET_CPU
PROCHOT
PMSYNC_CPU
CATERR
PWR_DEBUG
DEBUG_EN
TXT_PLTEN
TXT_AGENT
SAFE_MODE_BOOT
BIST_ENABLE
DDR3_4_STRAP
PECI_CPU
DDR_RESET
EAR
THERMTRIP
ERROR2
ERROR1
ERROR0
THROTTLE_PECI_ID2
MEM_HOT
SVIDDATA
SVIDCLK
SVIDALERT
RSVD13
RSVD12
RSVD11
RSVD10
RSVD9
PECI_ID0
UART_TXD1
UART_TXD0
RSVD20
RSVD19
PE_HP_SDA
PE_HP_SCL
DDR_SDA
DDR_SCL
7/16
CPU_PECI
PU_EAR_L
PU_BDXDE_SPARE5
BDXDE_SVID_DATA
BDXDE_SVID_CLK
BDXDE_SVID_ALERT_L
CPU_UART1_RXD_1V05
CPU_UART0_RXD_1V05
CPU_UART1_TXD_1V05
CPU_UART0_TXD_1V05
TP_RSVD_20
TP_RSVD_19
DDR4_SDA_1V05_ST
DDR4_SCL_1V05_ST
PU_PE_HP_SDA
R105 0ohm 2 1% 0402
R106 0ohm 1% 0402
R107 0ohm 1% 0402
R108 220ohm 1% 0402
PECI_PCH_BMC
BDXDE_DDR4_RESET_L
BDXDE_CPU_THERMTRIP_L
BDXDE_ERR2_GTL_L
BDXDE_ERR1_GTL_L
BDXDE_ERR0_GTL_L
BDXDE_CPU2PCH_THROT_1V05
H_FAST_PROCHOT_L
SVID_CPU_DIO
CLK_SVID_CPU
SVID_CPU_ALERT_L
PD_BDXDE_SPARE4
PD_BDXDE_SPARE3
PD_BDXDE_SPARE2
PD_BDXDE_SPARE1
BDXDE_PECID0
VP1P05
R111 10Kohm 2 1% 0402 BOM = NI CPU_UART1_RXD_1V05
R112 10Kohm 2 1% 0402 BOM = NI CPU_UART0_RXD_1V05
R113 240ohm 2 1% 0402 PU_EAR_L
R114 10Kohm 2 1% 0402 PU_BDXDE_SPARE5
R115 1Kohm 2 1% 0402 BDXDE_CPU_RSMRST_L
R119 120ohm 2 1% 0402 SVID_CPU_DIO
R122 49.9ohm 2 1% 0402 SVID_CPU_ALERT_L
VP2P5_DDR4_VPP
R116 240ohm 1% 0402
R117 240ohm 1% 0402
R118 4.7Kohm 1% 0402 BOM = NI
C29 100nF 10% 10V 0402 X7R
C30 100nF 10% 10V 0402 X7R
R120 1Kohm 0402 1%
R121 1Kohm 0402 1%
U7
VCCA VCCB SDAA SDAB SCLA SCLB EN GND
PCA9617ADP
U7_EN
R125 10ohm 2 1% 0402
R127 10ohm 2 1% 0402
R126 20ohm 2 1% 0402
R128 20ohm 2 1% 0402
DDR4_SDA_2V5
DDR4_SCL_2V5
R123 5.11Kohm 2 1% 0402 BDXDE_RESET_L
R124 5.11Kohm 2 1% 0402 CPU_PECI
U8
VCCB VCCA 1B1 1B2 2B1 2B2 1A1 1A2 2A1 2A2 1DIR 2DIR 1OE 2OE GND1 GND2
74AVCH4T245PW
R453 10ohm 2 1% 0402
R454 10ohm 2 1% 0402
R455 10ohm 2 1% 0402
R456 10ohm 2 1% 0402
R457 20ohm 2 1% 0402
R458 20ohm 2 1% 0402
CPU_UART1_TXD_3V3
CPU_UART0_TXD_3V3
CPU_UART1_RXD_3V3
CPU_UART0_RXD_3V3
J2
20438-04021
VP3P3_BAT
6uA/10mil
D2
BAT54C-7-F
C34 22uF 10% 25V C-1210B-H2_8 X7R
R133 1Kohm 2 0603 1% VP3P3_BAT_SOURCE
CAD NOTE:
PLACE 22UF AND D1 DIODE
CLOSE TO BATTERY HOLDER
BB3320
BAT Holder, Vertical
[CAD]: 20mil
BAT1
P1 P2 P3 ANODE_1 CATHODE ANODE_2
BB3320E-1
BOM = NI
GND
BAT2
LITHIUM BATT
CR2032
Battery BR-2032/BN
BOM = NI
C31 1uF 10% 16V 0402 X6S
C32 1uF 10% 0402 16V X6S
R130 20Kohm 1% 0402
R129 20Kohm 1% 0402
R314 0ohm 1% 0402 BOM = NI
R312 0ohm 1% 0402
BMC_RTCRST_L
CPLD_RTCRST_L
RTCRST_L
RST_SRTCRST_L
J3
20438-04021
SMD
C35 1uF 6.3V 10% 0402 X7R
R131 1Kohm 0402 1%
R132 1Kohm 0402 1%
C33 1uF 10% 6.3V 0402 X7R
2018/05/24:
BOM option
For Apache: Install R312
For WB: Not install R312
Clear CMOS Registers by BMC.
J3: PIN 1, 2
open= normal
short= Clear Secondary RTC Registers
J3: PIN 3, 4
open= normal
short= Clear CMOS Registers
<Core Design>
Ufi Space Co., Ltd.
CONFIDENTIAL
Title
13. CPU UART/PWR MGNT/INT/SVID
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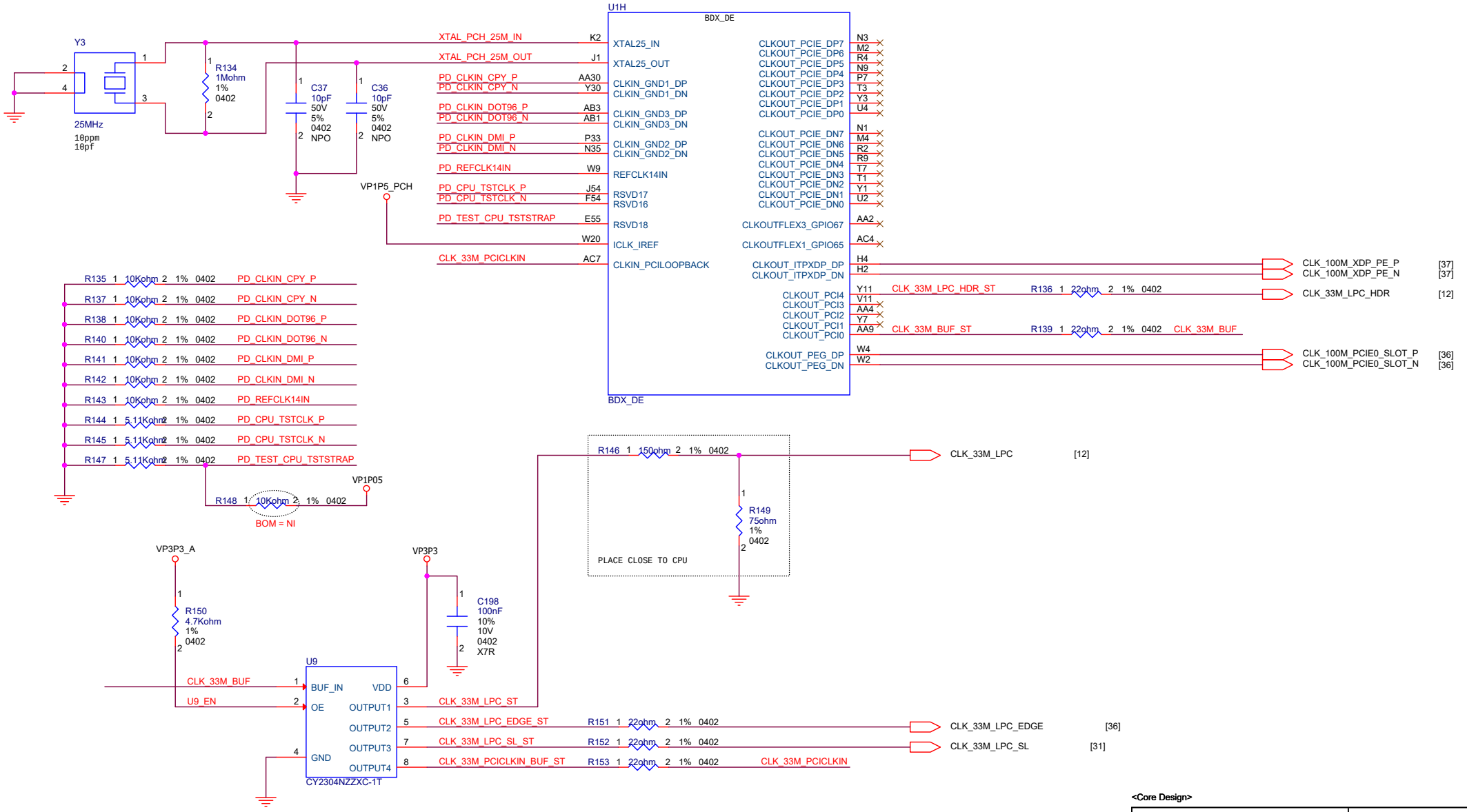

<Core Design>

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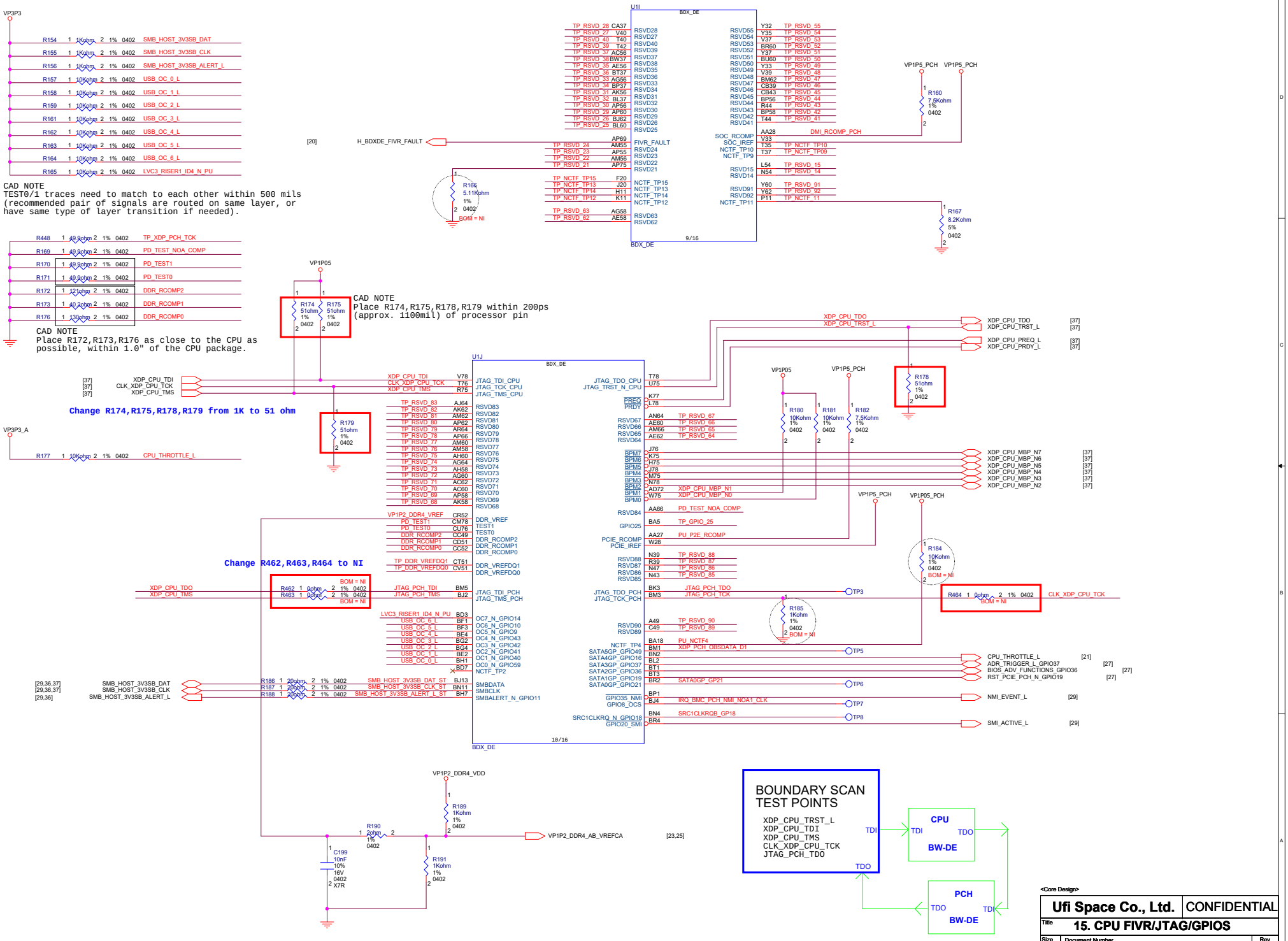
VP3P3
R154 1 1Kohm 2 1% 0402 SMB_HOST_3V3SB_DAT
R155 1 1Kohm 2 1% 0402 SMB_HOST_3V3SB_CLK
R156 1 1Kohm 2 1% 0402 SMB_HOST_3V3SB_ALERT_L
R157 1 10Kohm 2 1% 0402 USB_OC_0_L
R158 1 10Kohm 2 1% 0402 USB_OC_1_L
R159 1 10Kohm 2 1% 0402 USB_OC_2_L
R161 1 10Kohm 2 1% 0402 USB_OC_3_L
R162 1 10Kohm 2 1% 0402 USB_OC_4_L
R163 1 10Kohm 2 1% 0402 USB_OC_5_L
R164 1 10Kohm 2 1% 0402 USB_OC_6_L
R165 1 10Kohm 2 1% 0402 LVC3_RISER1_ID4_N_PU
CAD NOTE
TEST0/1 traces need to match to each other within 500 mils
(recommended pair of signals are routed on same layer, or
have same type of layer transition if needed).
U1I
BDX_DE
[20] H_BDXDE_FIVR_FAULT
R166 5.11Kohm 1% 0402 BOM = NI
R160 7.5Kohm 1% 0402
VP1P5_PCH
DMI_RCOMP_PCH
R167 8.2Kohm 5% 0402
9/16
R448 1 49.9ohm 2 1% 0402 TP_XDP_PCH_TCK
R169 1 49.9ohm 2 1% 0402 PD_TEST_NOA_COMP
R170 1 49.9ohm 2 1% 0402 PD_TEST1
R171 1 49.9ohm 2 1% 0402 PD_TEST0
R172 1 121ohm 2 1% 0402 DDR_RCOMP2
R173 1 40.2ohm 2 1% 0402 DDR_RCOMP1
R176 1 130ohm 2 1% 0402 DDR_RCOMP0
CAD NOTE
Place R172,R173,R176 as close to the CPU as
possible, within 1.0" of the CPU package.
VP1P05
R174 51ohm 1% 0402
R175 51ohm 1% 0402
CAD NOTE
Place R174,R175,R178,R179 within 200ps
(approx. 1100mil) of processor pin
U1J
BDX_DE
XDP_CPU_TDI
CLK_XDP_CPU_TCK
XDP_CPU_TMS
Change R174,R175,R178,R179 from 1K to 51 ohm
R179 51ohm 1% 0402
VP3P3_A
R177 1 10Kohm 2 1% 0402 CPU_THROTTLE_L
XDP_CPU_TDO
XDP_CPU_TRST_L
XDP_CPU_PREQ_L
XDP_CPU_PRDY_L
R178 51ohm 1% 0402
R180 10Kohm 1% 0402
R181 10Kohm 1% 0402
R182 7.5Kohm 1% 0402
XDP_CPU_MBP_N7
XDP_CPU_MBP_N6
XDP_CPU_MBP_N5
XDP_CPU_MBP_N4
XDP_CPU_MBP_N3
XDP_CPU_MBP_N2
Change R462,R463,R464 to NI
R462 1 0ohm 2 1% 0402 BOM = NI
R463 1 0ohm 2 1% 0402 BOM = NI
R464 1 0ohm 2 1% 0402 BOM = NI
R184 10Kohm 1% 0402 BOM = NI
R185 1Kohm 1% 0402 BOM = NI
JTAG_PCH_TDI
JTAG_PCH_TMS
JTAG_PCH_TDO
JTAG_PCH_TCK
CLK_XDP_CPU_TCK
TP3
TP5
TP6
TP7
TP8
CPU_THROTTLE_L
ADR_TRIGGER_L_GPIO37
BIOS_ADV_FUNCTIONS_GPIO36
RST_PCIE_PCH_N_GPIO19
NMI_EVENT_L
SMI_ACTIVE_L
10/16
SMB_HOST_3V3SB_DAT
SMB_HOST_3V3SB_CLK
SMB_HOST_3V3SB_ALERT_L
R186 1 20ohm 2 1% 0402
R187 1 20ohm 2 1% 0402
R188 1 20ohm 2 1% 0402
VP1P2_DDR4_VDD
R189 1Kohm 1% 0402
R190 20ohm 1% 0402
C199 10nF 10% 16V 0402 X7R
R191 1Kohm 1% 0402
VP1P2_DDR4_AB_VREFCA [23,25]
BOUNDARY SCAN
TEST POINTS
XDP_CPU_TRST_L
XDP_CPU_TDI
XDP_CPU_TMS
CLK_XDP_CPU_TCK
JTAG_PCH_TDO
CPU
BW-DE
PCH
BW-DE
<Core Design>
Ufi Space Co., Ltd.
CONFIDENTIAL
Title
15. CPU FIVR/JTAG/GPIOS
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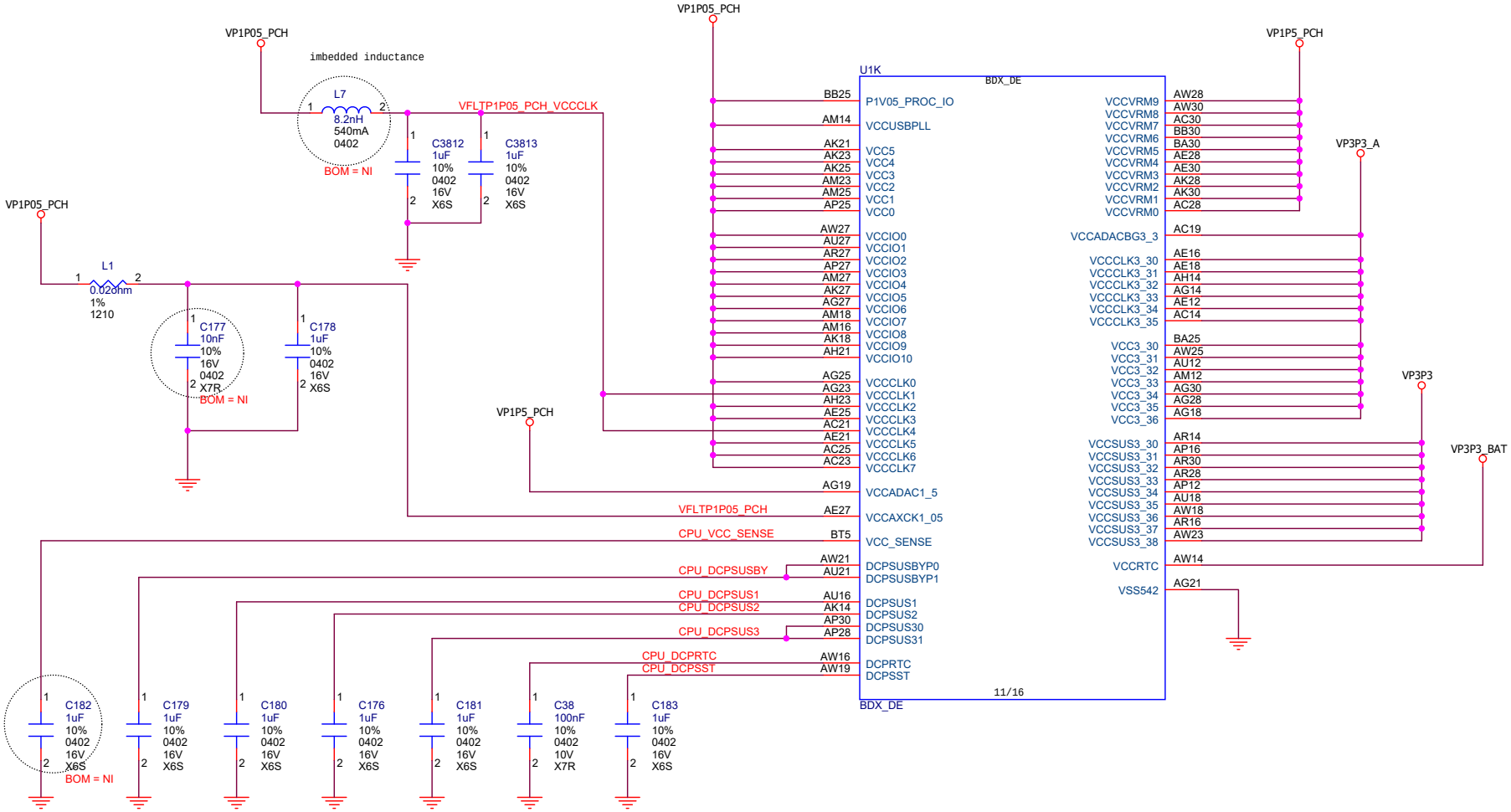

<Core Design>

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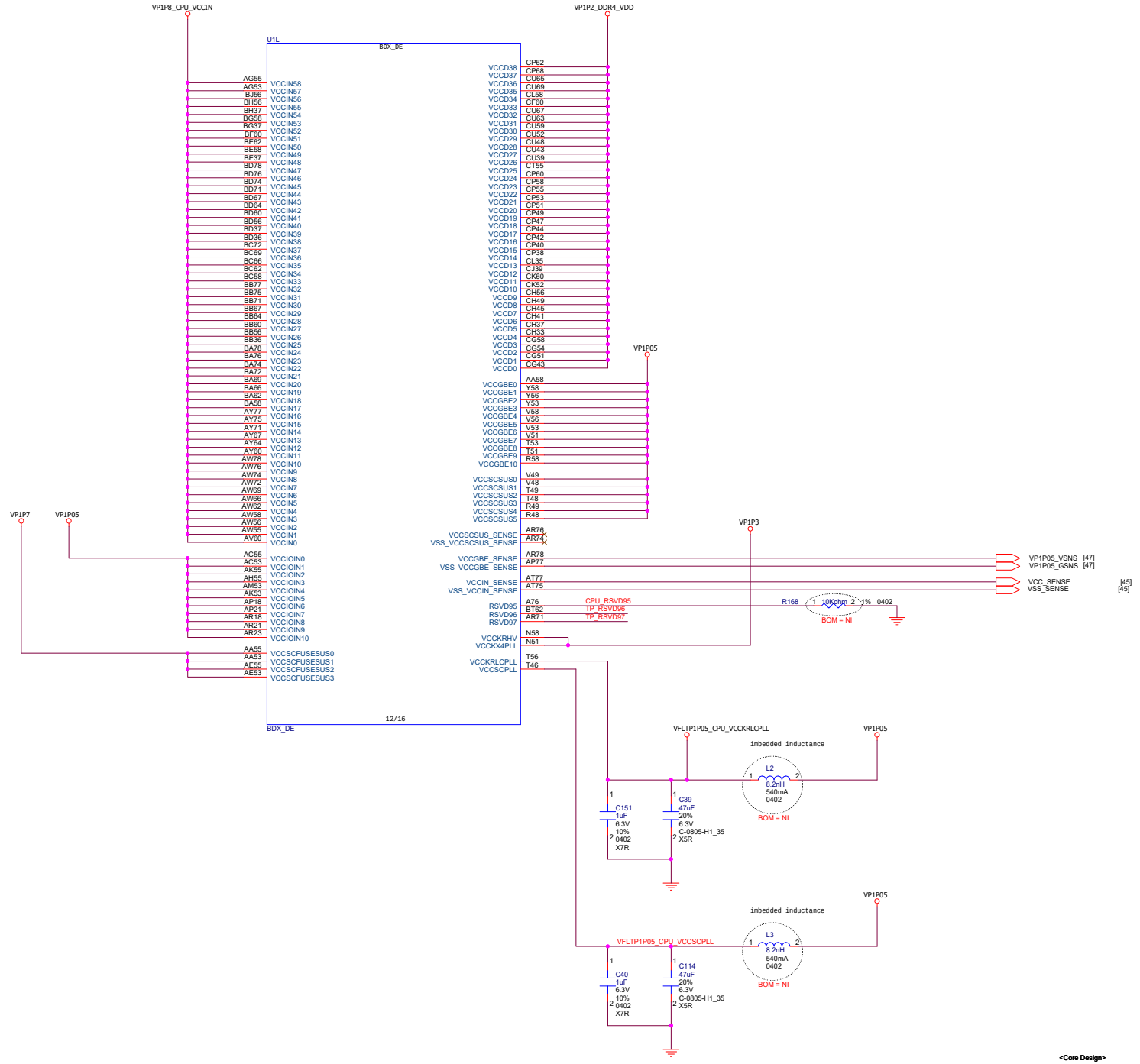

<Core Design>

Ufi Space Co., Ltd.		CONFIDENTIAL
Title	17. CPU POWER (2/2)	
Size	Document Number	Rev
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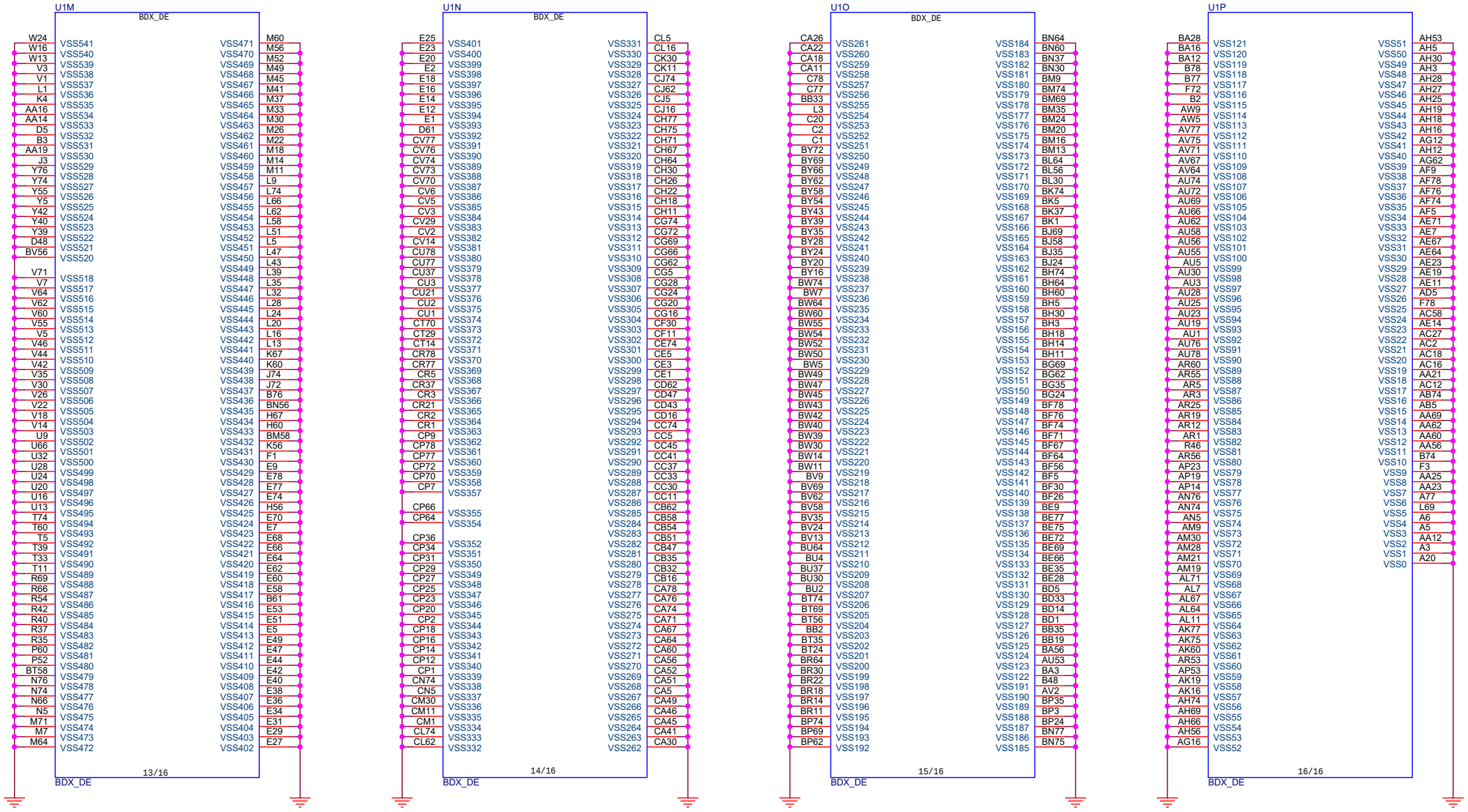

<Core Design>

Ufi Space Co., Ltd.		CONFIDENTIAL
Title	**18. CPU GND**	
Size	Document Number Project: T77O994T01	Rev BETA
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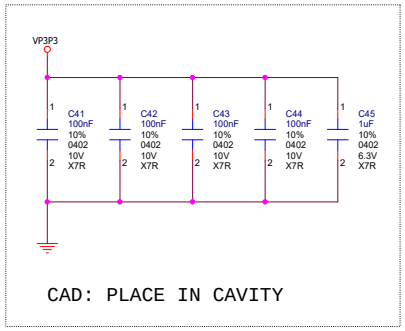

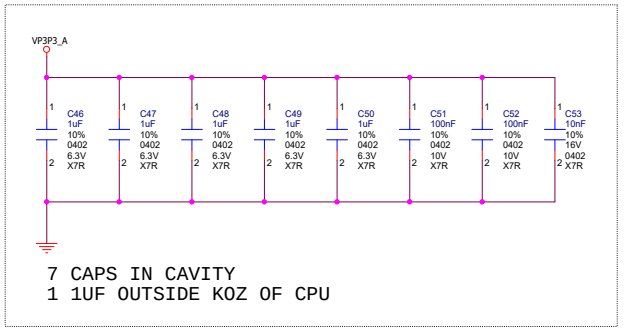

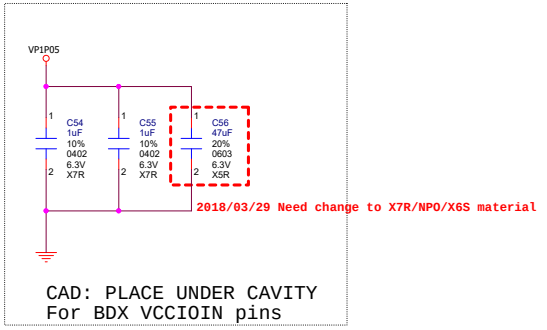

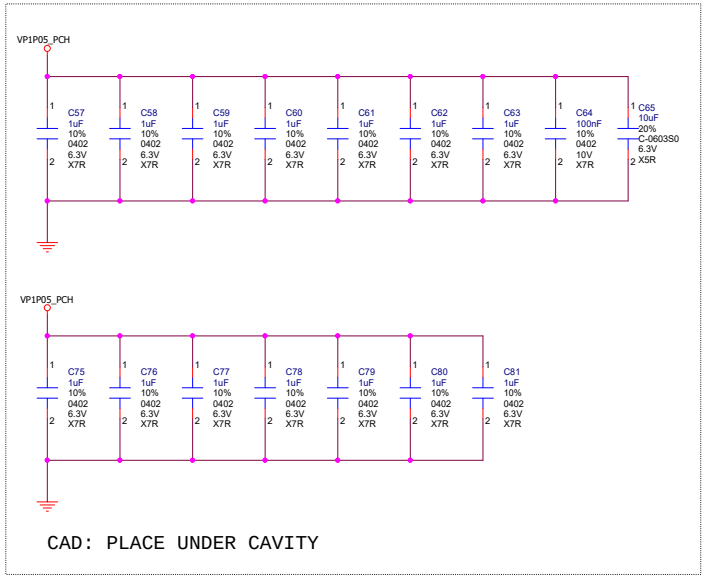

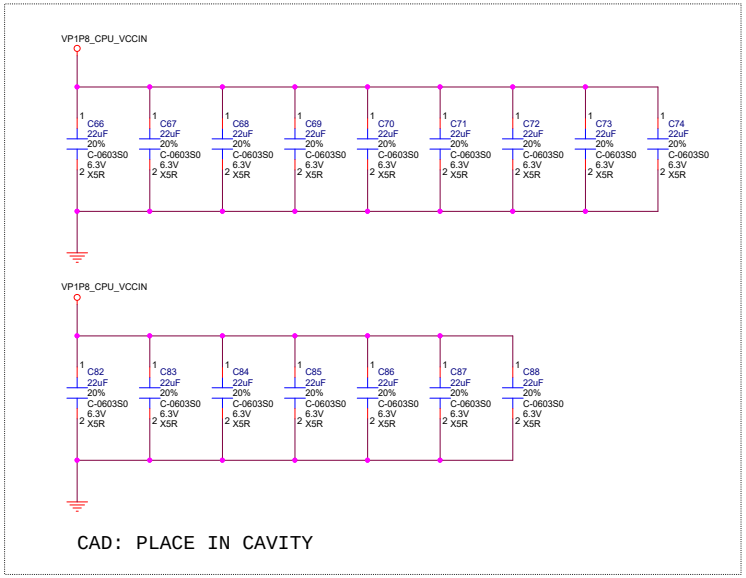

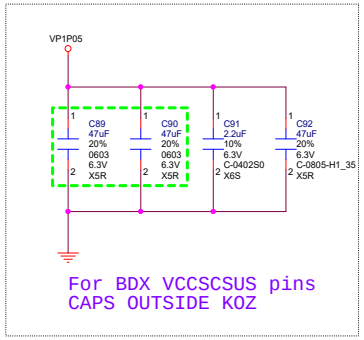

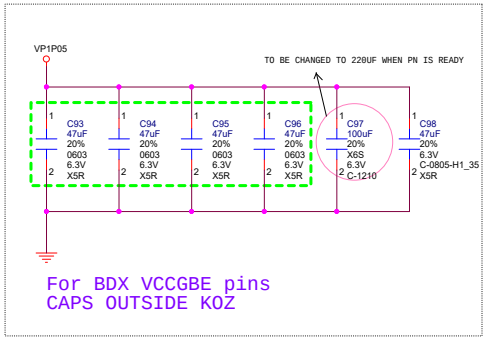

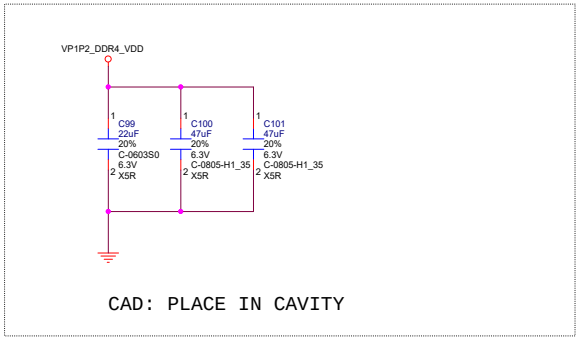

<Core Design>

Ufi Space Co., Ltd.	CONFIDENTIAL
Title: 19. CPU DECOUPLING	
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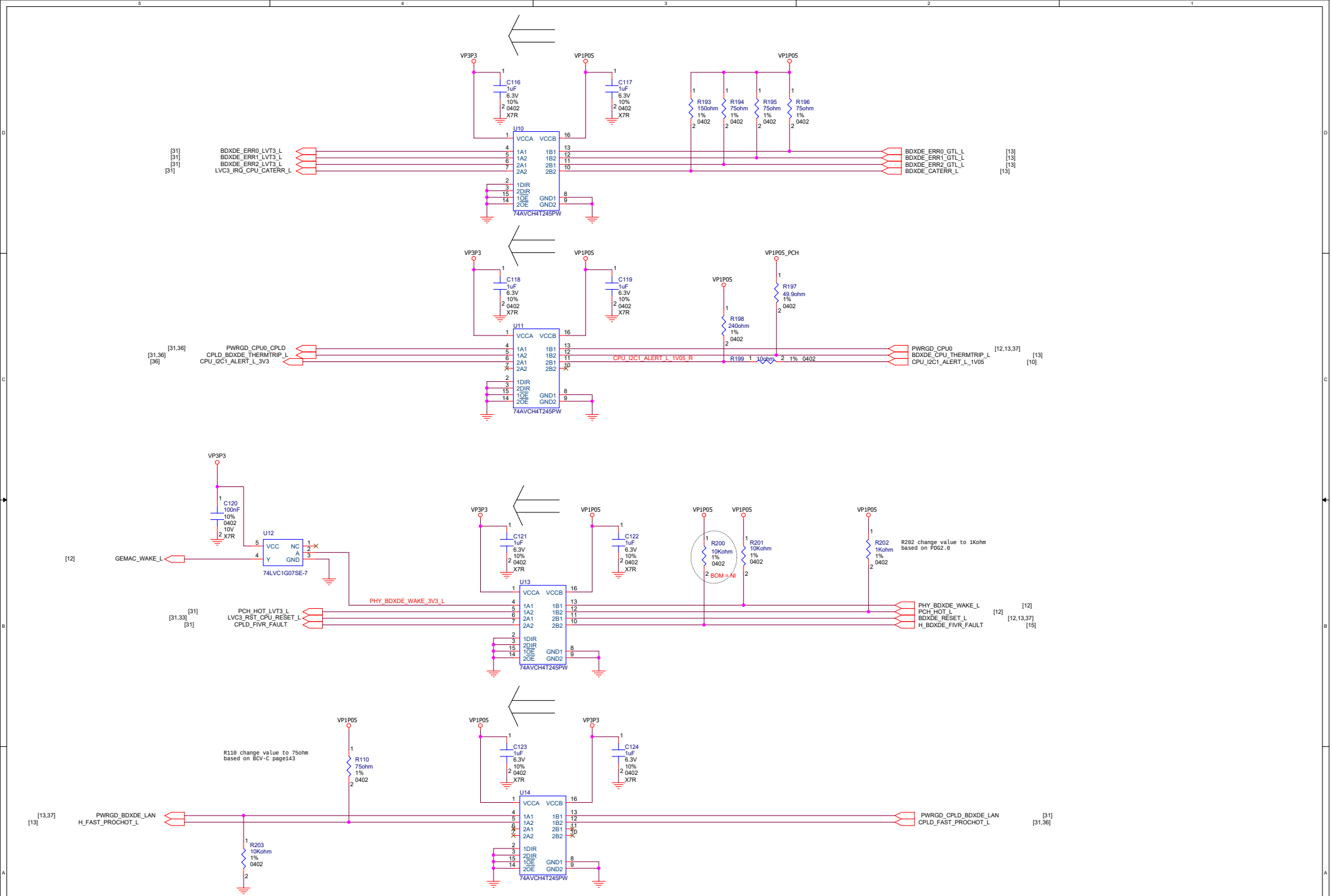

<Core Design>

Ufi Space Co., Ltd.	CONFIDENTIAL
Title: 20. CPU TRANSLATORS (1/2)	
Size	Document Number: Project: T77O994T01 — Rev: BETA
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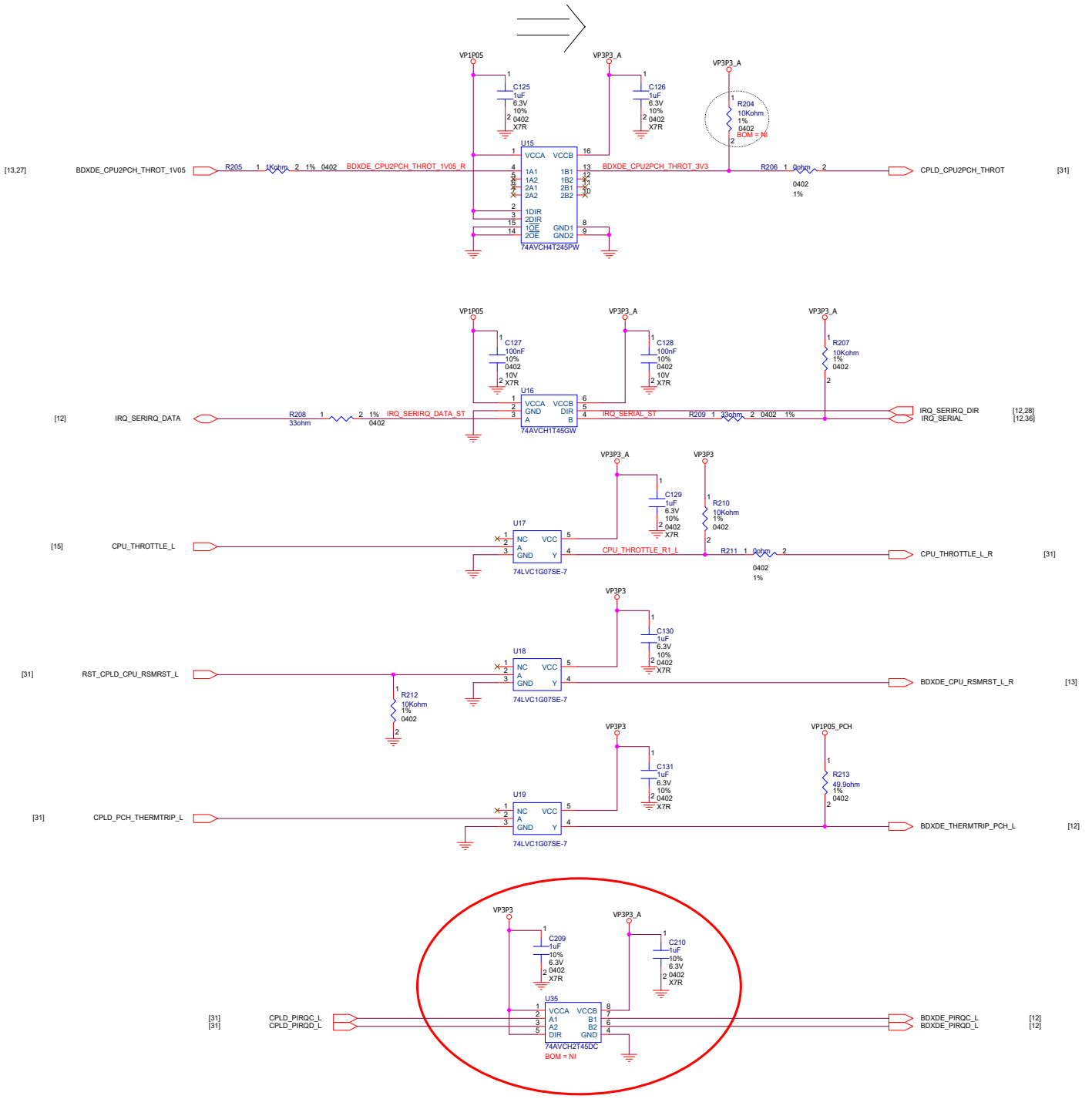

<Core Design>

Ufi Space Co., Ltd.		CONFIDENTIAL
Title	21. CPU TRANSLATORS (2/2)	
Size	Document Number	Rev
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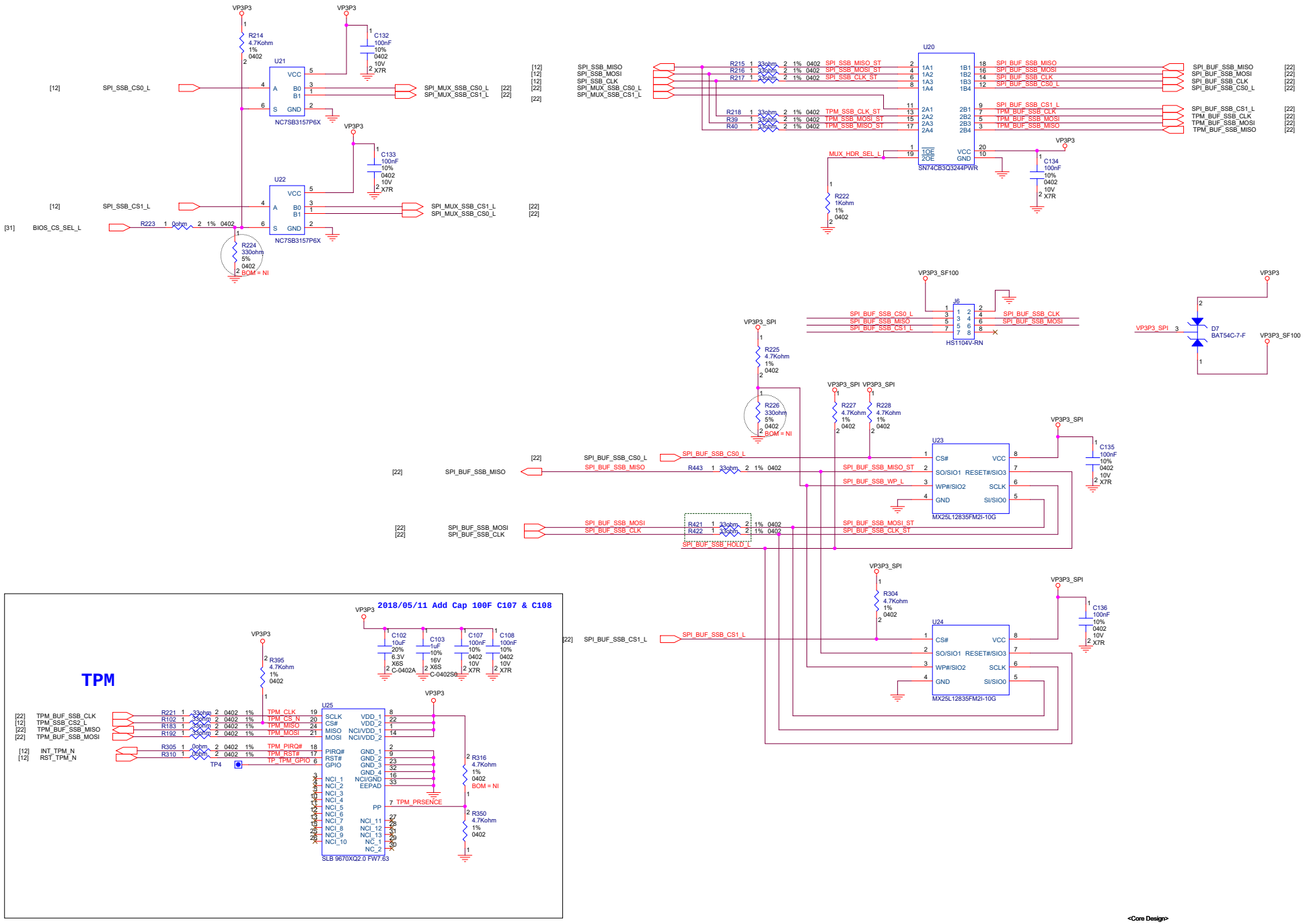

<core_design>
Ufi Space Co., Ltd.	CONFIDENTIAL
Title: 22. CPU BIOS SPI FLASH/TPM	
Size	Document Number: Project: T77O994T01 — Rev: BETA
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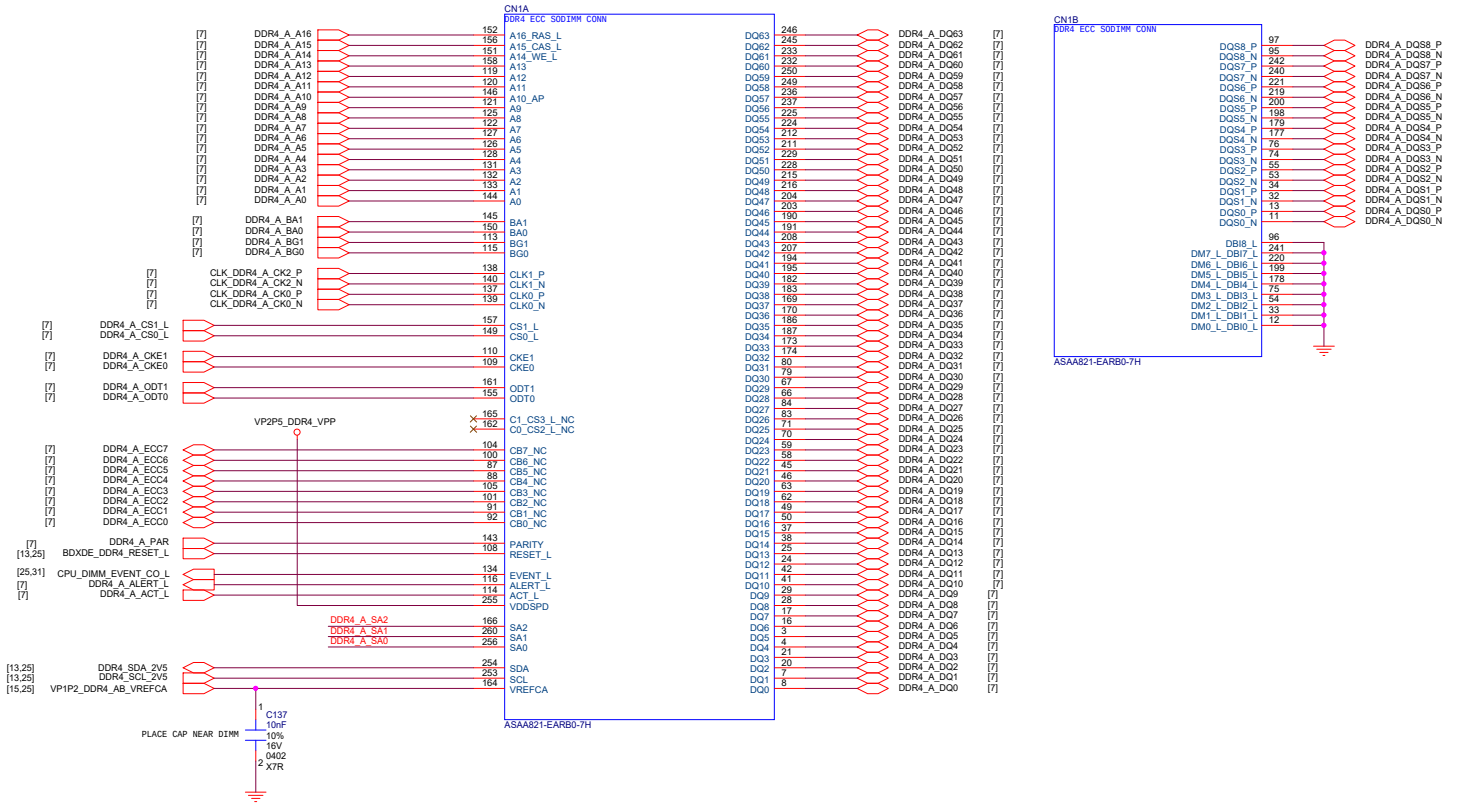
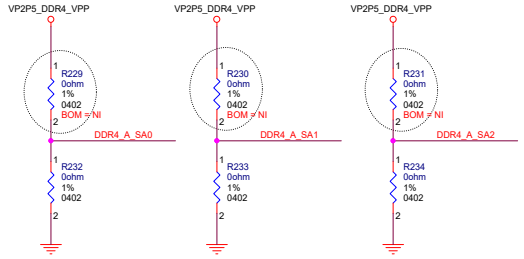
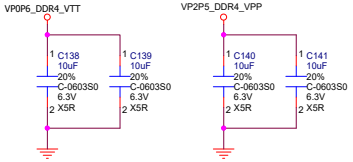
</core_design>

DDR4 CHA SOCKET



I2C Address = 0xA0 (DIMM0) Channel A
I2C Address = 0xA4 (DIMM1) Channel B





<Core Design>

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Title	23. DDR4 CHA SOCKET	
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DDR4 CHA SOCKET PWR

<Core Design>

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Title: 24. DDR4 CHA SOCKET PWR	
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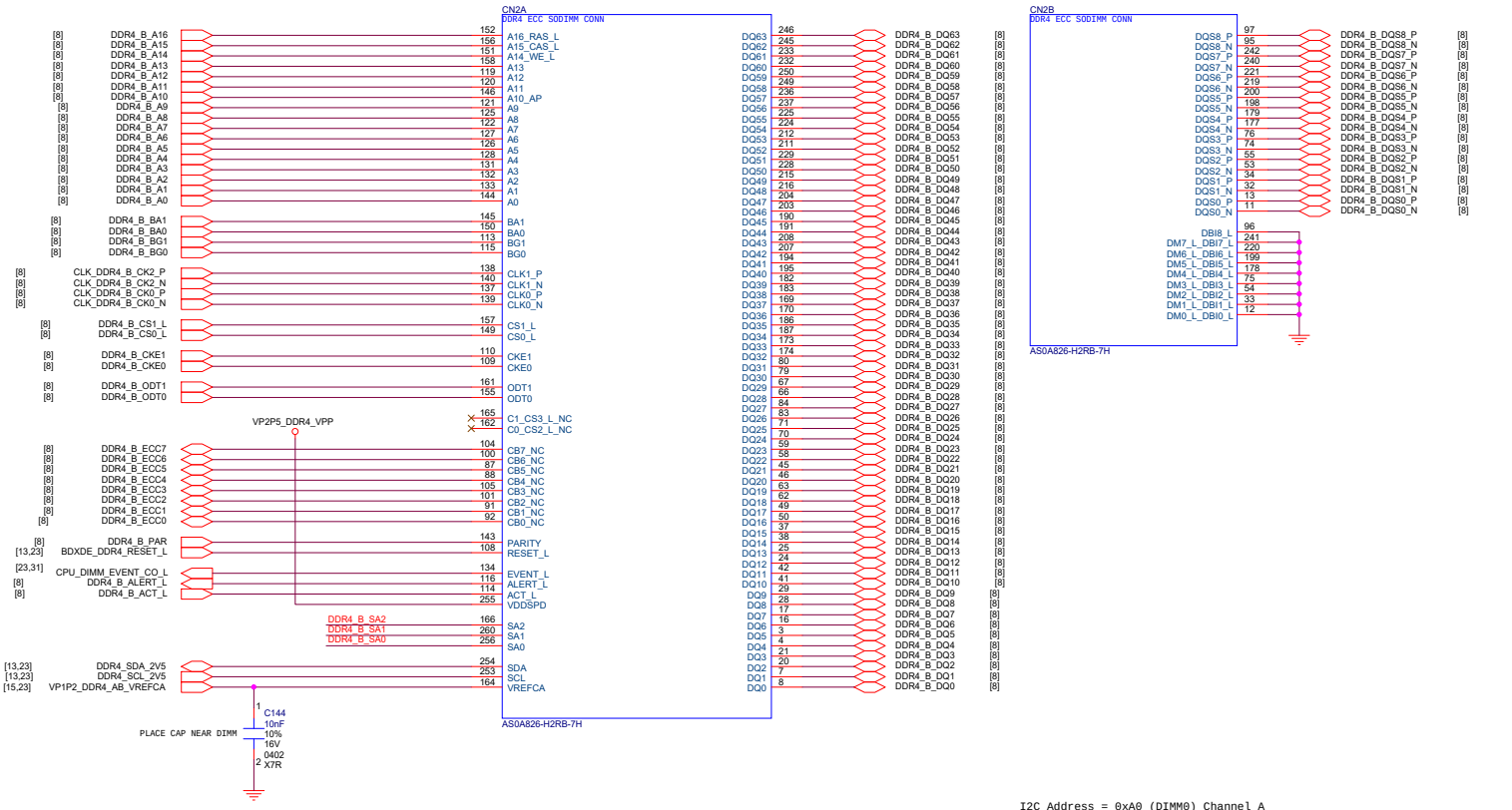
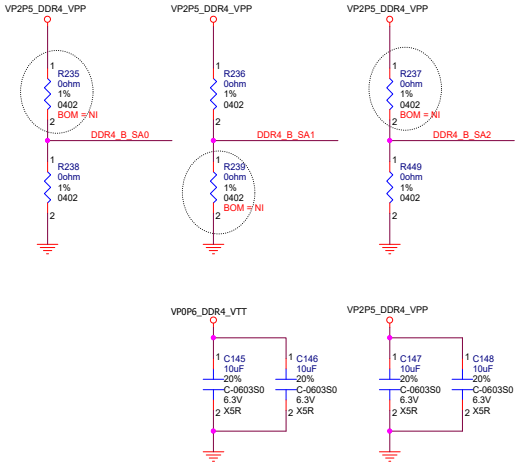
DDR4 CHB SOCKET



I2C Address = 0xA0 (DIMM0) Channel A
I2C Address = 0xA4 (DIMM1) Channel B



<Core Design>

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Title	25. DDR4 CHB SOCKET	
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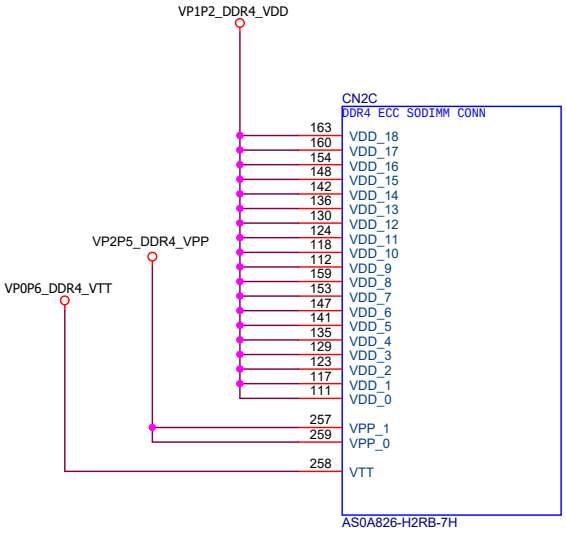
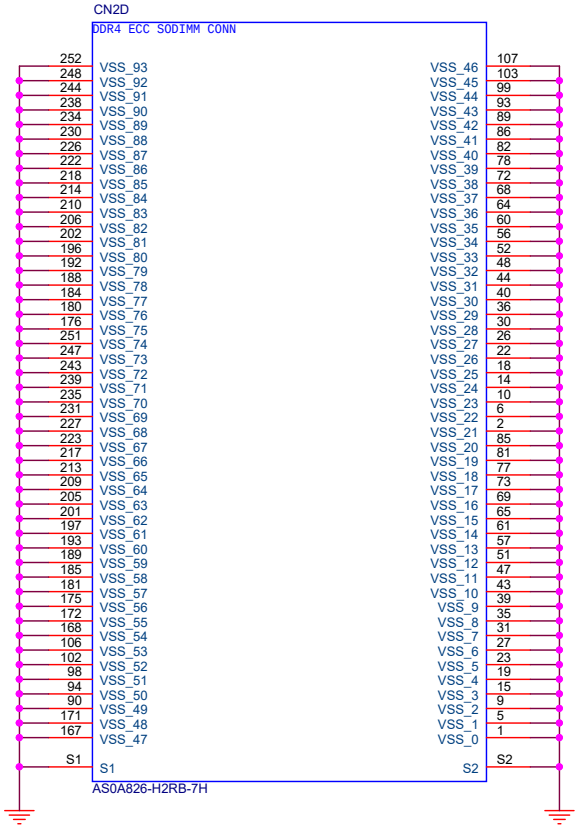
DDR4 CHB SOCKET PWR





<Core Design>

Ufi Space Co., Ltd.	CONFIDENTIAL
Title: 26. DDR4 CHB SOCKET PWR	
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GP51_GSXDOUT

1

R240 10Kohm 0402 1%
R244 1Kohm 0402 1%
BOM = NI
PU_GPIO51_GSXDOUT [12]

BOOT BIOS STRAPS (BBS)		
GNT[51]_GSXDOUT BBS[1]	SATA1GP_GP19 BBS[0]	
0	0	LPC
0	1	NAND
1	0	PCI
1	1	SPI (Default)

SATA1GP_GP19

1

R241 10Kohm 0402 1%
R245 1Kohm 0402 1%
BOM = NI
RST_PCIE_PCH_N_GPIO19 [15]

DOCKEN_N

0

R242 1Kohm 0402 1%
R246 10Kohm 0402 1%
BOM = NI
PD_DMI_TERMINATION_GPIO33 [12]

DMI RX TERMINATION WHEN AC-COUPLED MODE:
0 = DMI RX IS TERMINATED TO VSS.(DEFAULT)
1 = DMI RX IS TERMINATED TO VCC/2.

GP53_GSXDIN

0

R243 10Kohm 0402 1%
R247 1Kohm 0402 1%
BOM = NI
PD_GPIO53_GSXDIN [12]

DMI AC OR DC COUPLEING MODE
0 = DMI IS IN AC-COUPLING MODE
1 = DMI IS IN DC-COUPLING MODE

BIOS_ADV_FUNCTION

0

R248 1Kohm 0402 1%
R253 10Kohm 0402 1%
BOM = NI
BIOS_ADV_FUNCTIONS_GPIO36 [15]

THIS SIGNAL HAS A WEAK INTERNAL PULL-DOWN.
THIS SIGNAL ONLY TAKES EFFECT IF DMI IS CONFIGURED IN DCCOUPLED MODE
0 = DMI TX IS TERMINATED TO VSS.(DEFAULT)
1 = DMI TX IS TERMINATED TO VCC/2.

ADR_TRIGGER

SATA3 GP37

1

R249 1Kohm 0402 1%
R254 10Kohm 0402 1%
BOM = NI
ADR_TRIGGER_L_GPIO37 [15]

TLS CONFIDENTIALITY
0 = DISABLE INTEL ME CRPTO TRANSPORT LAYER SECURITY (TLS) CIPHTER SUITE (NO CONFIDENTIALITY)
1 = ENABLE INTEL ME CRPTO TRANSPORT LAYER SECURITY (TLS) CIPHTER SUITE (WITH CONFIDENTIALITY)(DEFAULT)

SUSCLK

GP62

1

R250 10Kohm 0402 1%
R255 1Kohm 0402 1%
BOM = NI
CLK_M2_SUSCLK_ST [12]

PLL ON-DIE VOLTAGE REGULATOR ENABLE.
1 = ENABLED
0 = DDISABLED
WEAK INTERNAL PU (15K-40K).

NCSI_TRI_EN

0

R251 5.11Kohm 1% 0402
R256 5.11Kohm 1% 0402
BOM = NI
LAN_NCSI_TRI_EN_L [10]

CPU2PCH_THROT

0

R252 5.11Kohm 1% 0402
R257 5.11Kohm 1% 0402
BOM = NI
BDXDE_CPU2PCH_THROT_1V05 [13,21]

SPARE[0]

0

R258 5.11Kohm 1% 0402
R263 5.11Kohm 1% 0402
BOM = NI
BDXDE_PECID0 [13]

PECI_ID[2:0]=000B

SPARE[1]

0

R259 5.11Kohm 1% 0402
R264 5.11Kohm 1% 0402
BOM = NI
PD_BDXDE_SPARE1 [13]

THIS IS THE DISABLE TO THE SC PCU RESET FSM
0 = PMC FSB BRINGS UP SOUTH COMPLEX
1 = PCODE BRINGS UP SOUTH COMPLEX OF PMC

SPARE[2]

0

R260 5.11Kohm 1% 0402
R265 5.11Kohm 1% 0402
BOM = NI
PD_BDXDE_SPARE2 [13]

BYPASSES THE CRYSTAL CLOCK TO THE SCPLL
1'B0 = PICKS THE 25MHZ KR CRYSTAL CLOCK AS THE REFERENCE TO SCPLL (DEFAULT)
1'B1 = FORCES THE TEST DOCK FROM TSTCLK_SC PINS

SPARE[3]

0

R261 5.11Kohm 1% 0402
R266 5.11Kohm 1% 0402
BOM = NI
PD_BDXDE_SPARE3 [13]

SELECTS B/W FUNCTIONAL AND TEST MODE IN THE KX4 PLL
1'B0 = NO TEST CLOCK OVERRIDE(DEFAULT)
1'B1 = TEST CLOCK OVERRIDE

SPARE[4]

0

R262 5.11Kohm 1% 0402
R267 5.11Kohm 1% 0402
BOM = NI
PD_BDXDE_SPARE4 [13]

1'B0 = NORMAL REFERENCE CLOCK PATH WITH CR BASE REFERENCE CLOCK SELECTION(DEFAULT)
1'B1 = FORCE "REGULAR" REFERENCE CLOCKS TO BE SENT TO THE KX4 PLLS AS LONG AS TSTCLK_KX4_STRAP[2]=1'B0

UART_TXD[0]

0

R268 5.11Kohm 1% 0402
R274 5.11Kohm 1% 0402
BOM = NI
CPU_UART0_TXD_1V05 [13]

UART_TXD[1]

0

R269 5.11Kohm 1% 0402
R275 5.11Kohm 1% 0402
BOM = NI
CPU_UART1_TXD_1V05 [13]

NCSI_ARB_OUT

1

R270 5.11Kohm 1% 0402
R276 5.11Kohm 1% 0402
BOM = NI
LVC1_LAN_NCSI_ARB_OUT [10]

SELECTS B/W THE COMBINED AND SEPERATE VRS
1: USING COMBINED P1V05 VR (DEFAULT)
0: ALL RAILS HAVE SEPERATE VRS

DSWODVREN

1

R271 5.11Kohm 1% 0402
PU_DSWODVREN [12]

DSWODVREN: DEEP SLEEP WELL ON-DIE VOLTAGE REGULATOR ENABLE
1: DSW ODVR IS ENABLED (DEFAULT).
0: DSW ODVR IS DISABLED.

NCSI_RXD_1

0

R272 5.11Kohm 1% 0402
R277 5.11Kohm 1% 0402
BOM = NI
LAN_NCSI_RXD1 [10]

ENABLE/DISABLE MANAGEBILITY TRAFFIC
DEFAULT LOW - DISABLED
1'B0 = LAN AVAILABLE IN S5 FOR WOL (DEFAULT)
1'B1 = LAN NOT AVAILABLE IN S5.
MANAGEBILITY DISABLED.
NO ON-DIE PU / PDN

INTVRMEN

1

R273 330Kohm 1% 0402
PU_BDXDE_INTVRMEN [12]

INTERNAL VRM ENABLE:
THIS SIGNAL IS USED TO ENABLE OR DISABLE THE INTEGRATED 1.05V REGULATOR FOR THE SUSPEND WELL ON THE WBG.
PU: ENABLE VR (DEFAULT).
PD: DISABLES VR..
PD OPTION NOT BEING PROVIDED.

10GBE_MDIO_DIR_CTL_1

1

R278 5.11Kohm 1% 0402
R283 5.11Kohm 1% 0402
BOM = NI
LAN_10GE_P1_MDIO_DIR_1V05 [10]

2'B00 = BOTH LAN PORTS ARE DISABLED.
NOTE: IN THIS MODE MANAGEABILITY IS NOT FUNCTIONAL AND MUST NOT BE ENABLED IN NVM CONTROL WORD 1.
2'B01 = PORT 1 IS DISABLED. PORT 0 IS ENABLED.
2'B10 = RESERVED
2'B11 = BOTH PORT0 & 1 ARE ENABLED.(DEFAULT)

10GBE_MDIO_DIR_CTL_0

1

R279 5.11Kohm 1% 0402
R284 5.11Kohm 1% 0402
BOM = NI
LAN_10GE_P0_MDIO_DIR_1V05 [10]

DDR3_4_STRAP

1

R280 240ohm 1% 0402
R285 240ohm 1% 0402
BOM = NI
PU_DDR3_4_STRAP [13]

SELECTS BETWEEN DDR4 & DDR3:
1 = DDR4
0 = DDR3

TXT_PLTEN

1

R282 240ohm 1% 0402
BOM = NI
TXT_PLTEN [13]

PLATFORM ENABLE STRAP.
0 = THE PLATFORM IS NOT INTEL TXT ENABLED.
1 = DEFAULT. THE PLATFORM IS INTEL TXT ENABLED

TXT_AGENT

1

R281 240ohm 1% 0402
R286 240ohm 1% 0402
BOM = NI
TXT_AGENT [13]

TXT AGENT (DRIVES TXT TRANSANCTIONS):
1 = CPU IS TXT_AGENT
0 = CPU IS NOT TXT_AGENT

<Core Design>

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Title: 27. CPU STRAPS (1/2)

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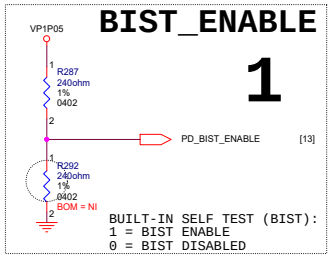

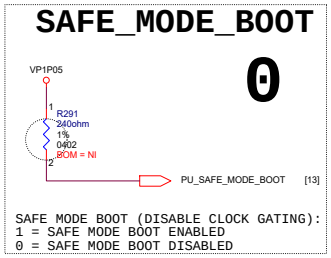

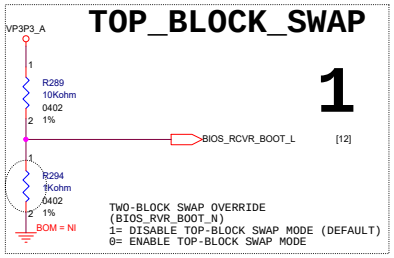

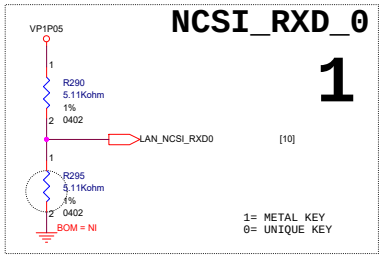

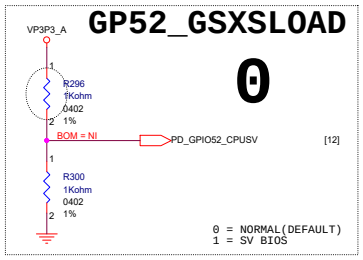

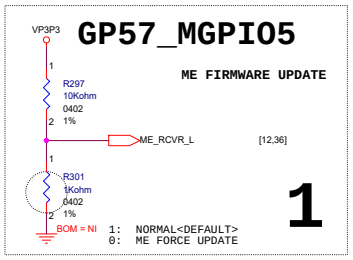

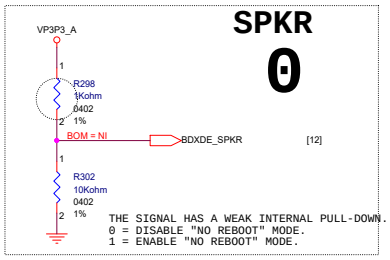

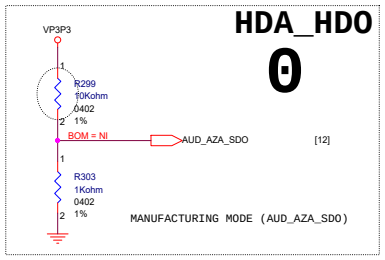

STRAP NAME	DEFAULT	DESCRIPTION
BOOT BIOS STRAPS (GP19, GP51)	1,1	BOOT BIOS DESTINATION 0 1 RESERVED 1 0 RESERVED 1 1 SPI (DEFAULT) 0 0 LPC
DMI_TERMINATION	0	DMI TX TERMINATION WHEN DCCOUPLED MODE. 0 = DMI TX IS TERMINATED TO VSS. 1 = DMI TX IS TERMINATED TO VCC/2.
BIOS_ADV_FUNCTIONS	0	DMI RX TERMINATION WHEN AC-COUPLED MODE: 0 = DMI RX IS TERMINATED TO VSS.(DEFAULT) 1 = DMI RX IS TERMINATED TO VCC/2.
GSXDIN	0	DMI AC OR DC COUPLING? 0 = DMI IS IN AC-COUPLING MODE (SERVER/WORKSTATION ONLY, NOT MEANT FOR DESKTOP/MOBILE). 1 = DMI IS IN DC-COUPLING MODE (DESKTOP, MOBILE OR SERVER/WORKSTATION).
ADR_TRIGGER	1	TLS CONFIDENTIALITY 0 = DISABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) 1 = ENABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS)
SUSCLK	1	TLS CONFIDENTIALITY 0 = DISABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS) 1 = ENABLE INTEL ME CRYPTO TRANSPORT LAYER SECURITY (TLS)
NCSI_TRI_EN CPU2PCH_THROT SPARE[0]	0,0,0	STRAPS HERE TO IDENTIFY WHICH SOCKET IS WHICH IN ORDER FOR PECI TO WORK
SPARE[1]	0	THIS IS THE DISABLE TO THE SC PCU RESET FSM 0 = PMC FSB BRINGS UP SOUTH COMPLEX 1 = PCODE BRINGS UP SOUTH COMPLEX OF PMC
SPARE[2]	0	BYPASSES THE CRYSTAL CLOCK TO THE SCPLL 0 = PICKS THE 25MHZ KR CRYSTAL CLOCK AS THE REFERENCE TO SCPLL (DEFAULT) 1 = FORCES THE TEST CLOCK FROM TSTCLK_SC PINS
SPARE[3]	0	SELECTS B/W FUNCTIONAL AND TEST MODE IN THE KX4 PLL 0 = NO TEST CLOCK OVERRIDE (DEFAULT) 1 = TEST CLOCK OVERRIDE
SPARE[4]	0	SELECTS B/W FUNCTIONAL AND TEST MODE IN THE KX4 PLL 0 = NORMAL REFERENCE CLOCK PATH WITH CR BASED REFERENCE CLOCK SELECTION (DEFAULT) 1 = FORCE "REGULAR" REFERENCE CLOCKS TO BE SENT TO THE KX4 PLLS
UART_TXD[0]	0	JTAG PORT FOR NORTH COMPLEX TAP 0 = GB#_SDP* PINS ARE USED AS FUNCTIONAL PIN OR CAN BE USED FOR SC TAPS THROUGH TAP PROGRAMMING. (DEFAULT) 1 = PINS ARE USED AS JTAG PORT FOR NC TAP
UART_TXD[1]	0	CONTROLS THE SECURITY ATTRIBUTES ON THE NVM – FOR PRE-PRODUCTION USAGE 0 = DISABLES NVM SECURITY (DEFAULT) 1 = SECURITY ENABLED

STRAP NAME	DEFAULT	DESCRIPTION
NCSI_ARB_OUT	1	USING COMBINED P1V05
DSWODVREN	1	0 = DISABLE INTEGRATED DEEPSX WELL (DSW) ON-DIE VOLTAGE REGULATOR. THIS MODE IS ONLY SUPPORTED FOR TESTING ENVIRONMENTS. 1 = ENABLE DSW 3.3V-TO-1.05V INTEGRATED DEEPSX WELL (DSW) ON-DIE VOLTAGE REGULATOR.
NCSI_RXD_1	0	ENABLE/DISABLE MANAGEBILITY TRAFFIC 0 = LAN AVAILABLE IN S5 FOR WOL (DEFAULT) 1 = LAN NOT AVAILABLE IN S5. MANAGEBILITY DISABLED.
INTVRMEN	1	INTEGRATED VRMS 0 = DCPSUS1, DCPSUS2 AND DCPSUS3 ARE POWERED FROM AN EXTERNAL POWER SOURCE. SERVERS SHOULD NOT PULL THE STRAP LOW. 1 = INTEGRATED VRMS ENABLED.
10GBE_MDIO_DIR_CTL_0 10GBE_MDIO_DIR_CTL_1	1,1	00 = BOTH LAN PORTS ARE DISABLED. 01 = PORT 1 IS DISABLED. PORT 0 IS ENABLED. 10 = RESERVED 11 = BOTH PORT0 & 1 ARE ENABLED. (DEFAULT)
DDR3_4_STRAP	1	1 = DDR4 0 = DDR3
TXT_PLTEN	1	(INTEL? TXT) PLATFORM ENABLE STRAP. 0 = THE PLATFORM IS NOT INTEL TXT ENABLED. 1 = DEFAULT. THE PLATFORM IS INTEL TXT ENABLED
TXT_AGENT	1	TXT AGENT (DRIVES TXT TRANSANCTIONS): 1 = CPU IS TXT_AGENT 0 = CPU IS NOT TXT_AGENT
BIST_ENABLE	1	BUILT-IN SELF TEST (BIST): 1 = BIST ENABLED 0 = BIST DISABLED
SAFE_MODE_BOOT	0	SAFE MODE BOOT (DISABLE CLOCK GATING): 1 = SAFE MODE BOOT ENABLED 0 = SAFE MODE BOOT DISABLED

<Core Design>

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Title: 28. CPU STRAPS (2/2)

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CPU I2C address:
1. 0x4F --Temp sensor:
2. 0x57 -- EEPROM address
3. 0x77 -- PCA9539 IO EXP address
4. 0xA0 -- (DIMM0) Channel A
5. 0xA4 -- (DIMM1) Channel B
6. 0x44 -- SOC legacy SMBus ARP slave address
7. 0x48 -- Diag Service SMBus address
8. 0x08 -- SMBus Host Controller

[15,36,37] SMB_HOST_3V3SB_CLK
[15,36,37] SMB_HOST_3V3SB_DAT

VP3P3

C152 100nF 10% 0402 10V X7R

U26 M24128-BRDW6TP
I2C Address : 7b'101_0111 (0x57)

R317 0ohm 1% 0402 I2C_EEPROM_SCL
R318 0ohm 1% 0402 I2C_EEPROM_SDA

R319 330ohm

R444 4.7Kohm 1% 0402
R445 4.7Kohm 1% 0402
R315 4.7Kohm 1% 0402

R320 330ohm R-0402S0 5% BOM = NI
R321 330ohm R-0402S0 5% BOM = NI
R446 330ohm R-0402S0 5% BOM = NI

2018/05/15
1.Add pull up/down resistors on EEPROM address pins
2.Change the CPU's EEPROM address from 0x51 to 0x57 to avoid the I2C address conflict

[36] ADC_CPU_TEMP_SENSOR

U36 TMP235A2DCKR 020.00086.005 SC-70-5A

2018/04/17 Add ADC Thermal Sensor

Place close to Broadwell-DE(U1)

R322 4.7Kohm 1% 0402

U27 TMP75AIDR
I2C Address : 7b'100_1111 (0x4F)

R323 0ohm 1% 0402 I2C_TEMP_SENSOR_SDA
R324 0ohm 1% 0402 I2C_TEMP_SENSOR_SCL

SMB_HOST_3V3SB_ALERT_L [15,29,36]

C153 100nF 10% 0402 10V X7R

U28 74LVC1G07SE-7

SMI_ACTIVE_L_R R325 0ohm 1% 0402 SMI_ACTIVE_L_BUF
SMI_ACTIVE_L [15]

U29 74LVC1G07SE-7

NMI_EVENT_L_R R330 0ohm 1% 0402 NMI_EVENT_L_BUF
NMI_EVENT_L [15]

SMI_ACTIVE_L_R R326 4.7Kohm 1% 0402
NMI_EVENT_L_R R327 4.7Kohm 1% 0402

SMI_ACTIVE_L R332 4.7Kohm 1% 0402
NMI_EVENT_L R333 4.7Kohm 1% 0402

R328 0ohm 1% 0402
R329 0ohm 1% 0402

R331 4.7Kohm 1% 0402

C154 100nF 10% 0402 10V X7R

[15,29,36] SMB_HOST_3V3SB_ALERT_L

R334 4.7Kohm 1% 0402
R335 4.7Kohm 1% 0402

R336 4.7Kohm 1% 0402 BOM = NI
R337 4.7Kohm 1% 0402 BOM = NI

U30 PCA9539PW
I2C Address : 7b'111_0111 (0X77)

I2C_IO_EXP_SCL
I2C_IO_EXP_SDA

C155 1uF 10% 0402 16V X6S

I/O_0.7	CPLD_ERROR2_L_LATCH	[31]
I/O_0.6	CPLD_ERROR1_L_LATCH	[31]
I/O_0.5	CPLD_ERROR0_L_LATCH	[31]
I/O_0.4	CPLD_CATERR_L_LATCH	[31]
I/O_0.3	CPLD_PCHHOT_L_LATCH	[31]
I/O_0.2	CPLD_PROCHOT_L_LATCH	[31]
I/O_0.1		
I/O_0.0		
I/O_1.7	CPLD_THERMTRIP_L_LATCH	[31]
I/O_1.6	SYS_PWROK	[12,31,37]
I/O_1.5	SLP3_L	[12,31]
I/O_1.4	SYS_RESET_L	[30,31,36,37]
I/O_1.3	FP_IBMC_PWRBTN_OUT_L	[12,31,36,37]
I/O_1.2	CPLD_PLTRST_L_LATCH	[31]
I/O_1.1	SLP4_L	[12,31]
I/O_1.0	CPLD_CLEAR_LATCH	[31]

<Core Design>

Ufi Space Co., Ltd.		CONFIDENTIAL
Title	29. EEPROM/SENSOR/IO EXPANDER	
Size	Document Number	Rev
	Project: T77O994T01	BETA
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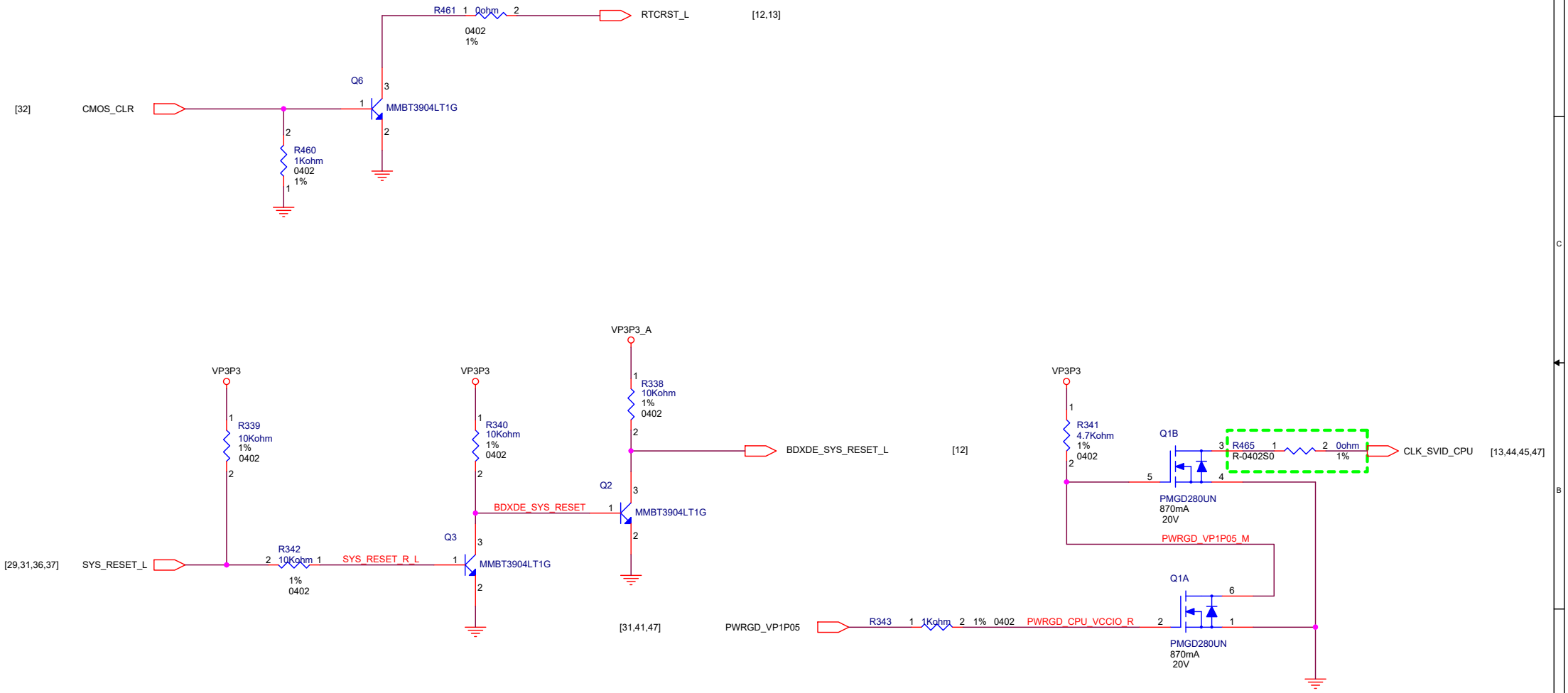
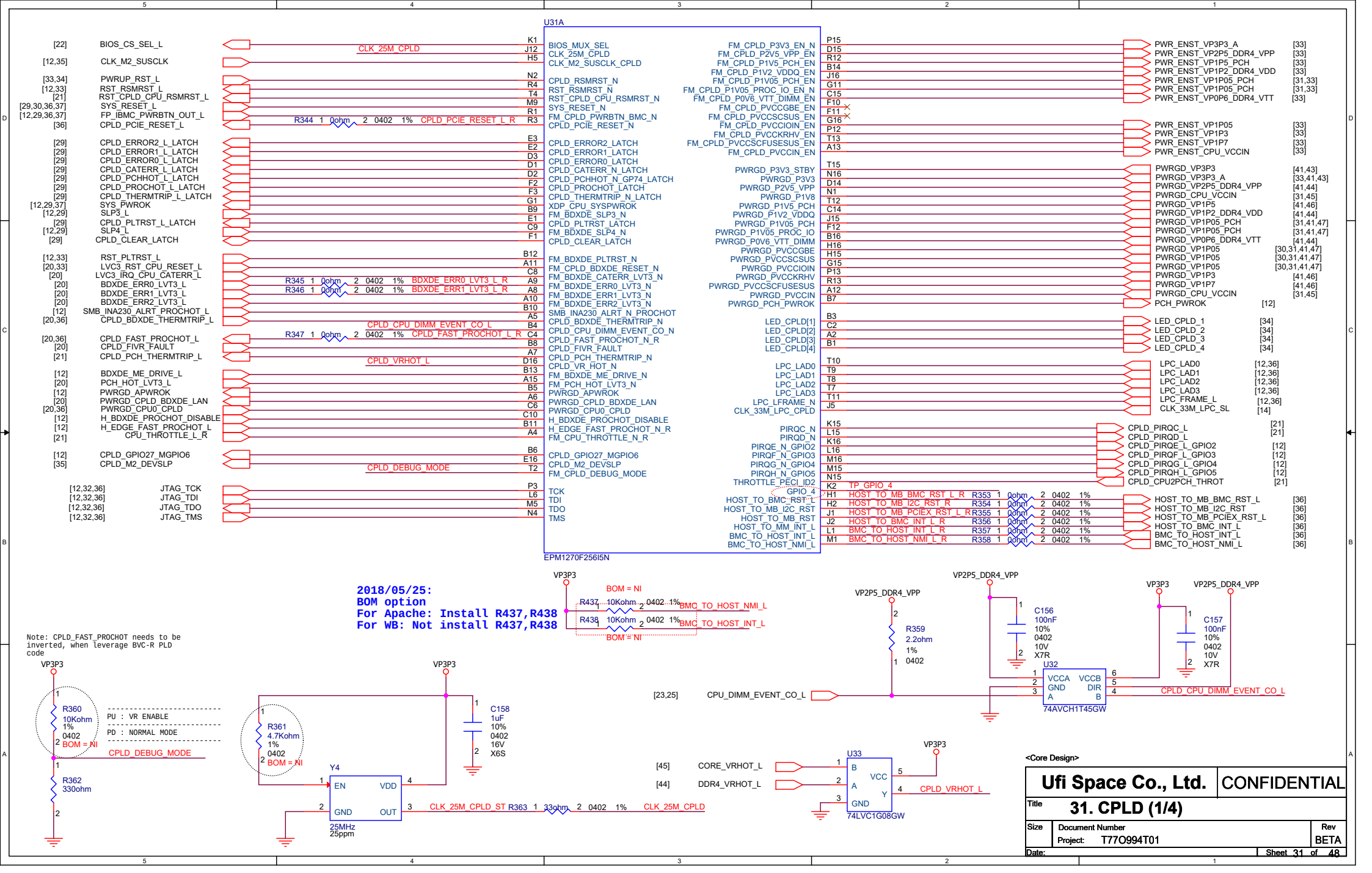


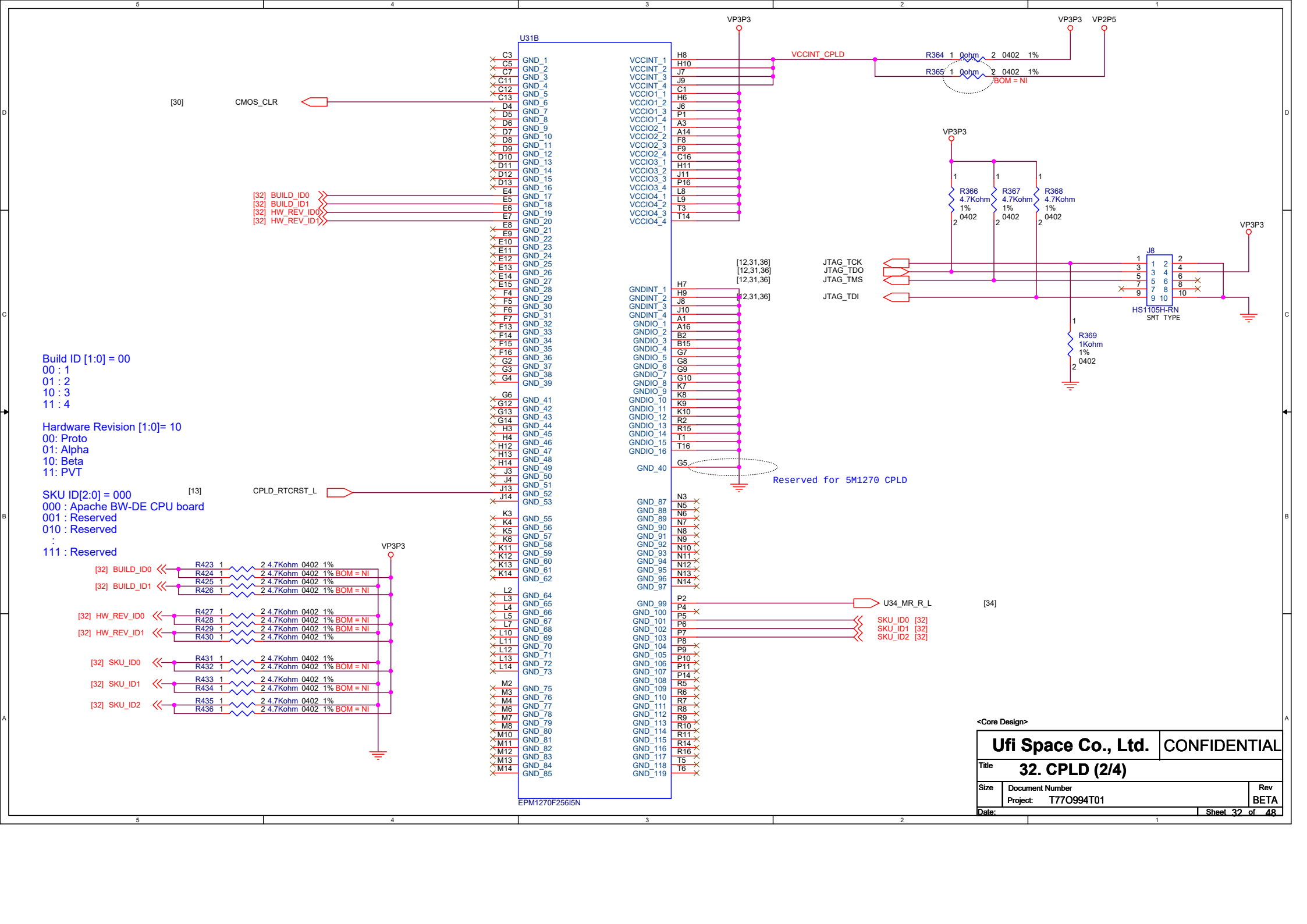
<Core Design>

Ufi Space Co., Ltd.		CONFIDENTIAL
Title	30. CPU MSIC	
Size	Document Number Project: T77O994T01	Rev BETA
Date:		Sheet 30 of 48



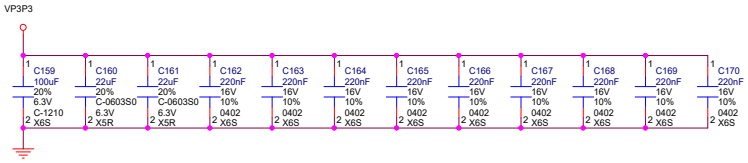
<Core Design>

Ufi Space Co., Ltd.	CONFIDENTIAL	
Title: 31. CPLD (1/4)		
Size	Document Number / Project: T77O994T01	Rev: BETA
Date:	Sheet 31 of 48	

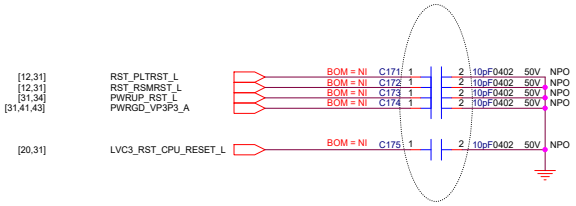


<Core Design>

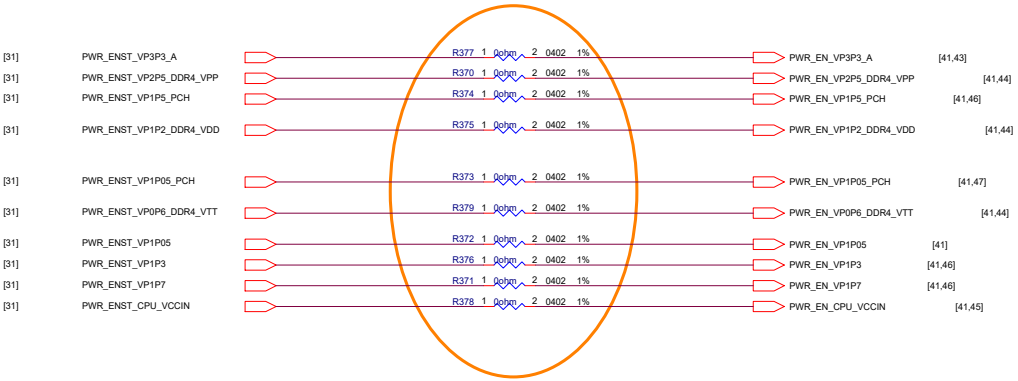
Ufi Space Co., Ltd.	CONFIDENTIAL
Title: 32. CPLD (2/4)	
Size	Document Number / Project: T77O994T01 — Rev: BETA
Date:	Sheet 32 of 48



For compliance suggestion

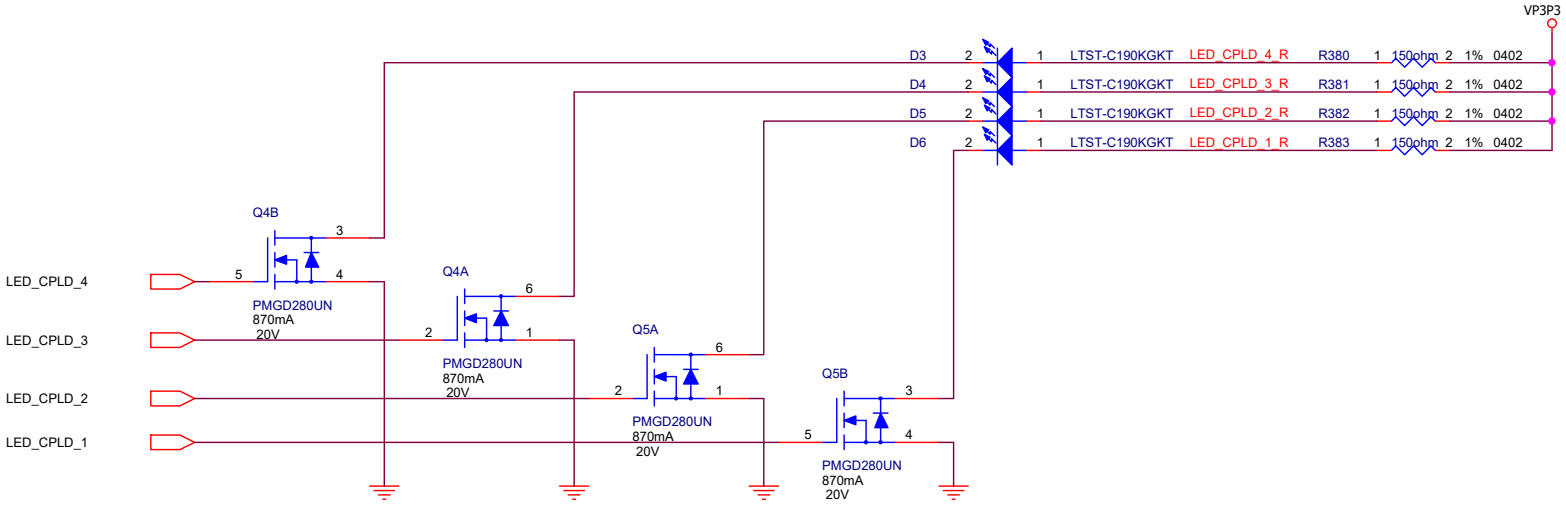


5/10 Add 0 ohm resistors for power debug

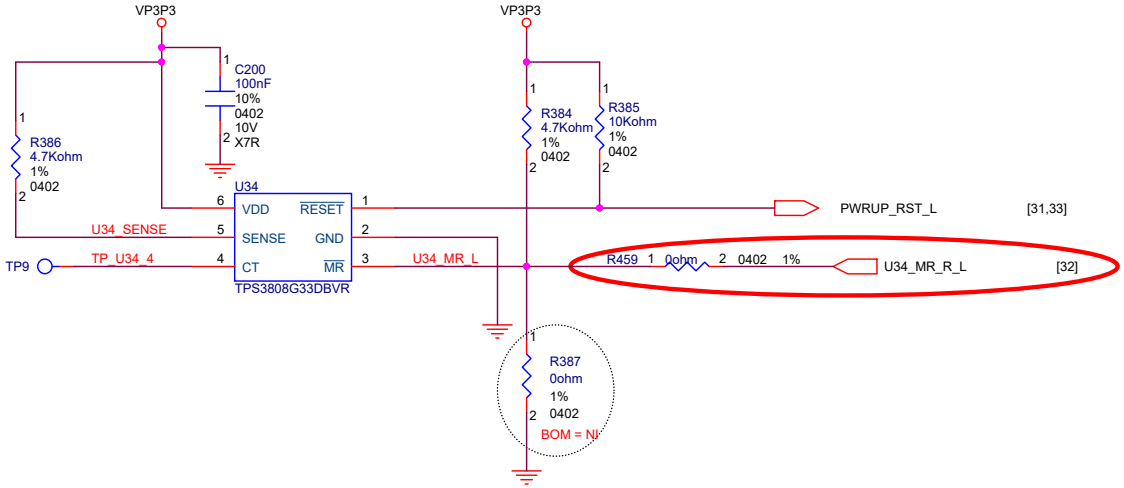


<Core Design>

Ufi Space Co., Ltd.	CONFIDENTIAL
Title: 33. CPLD (3/4)	
Size	Document Number: T77O994T01 — Rev: BETA
Date:	Sheet 33 of 48

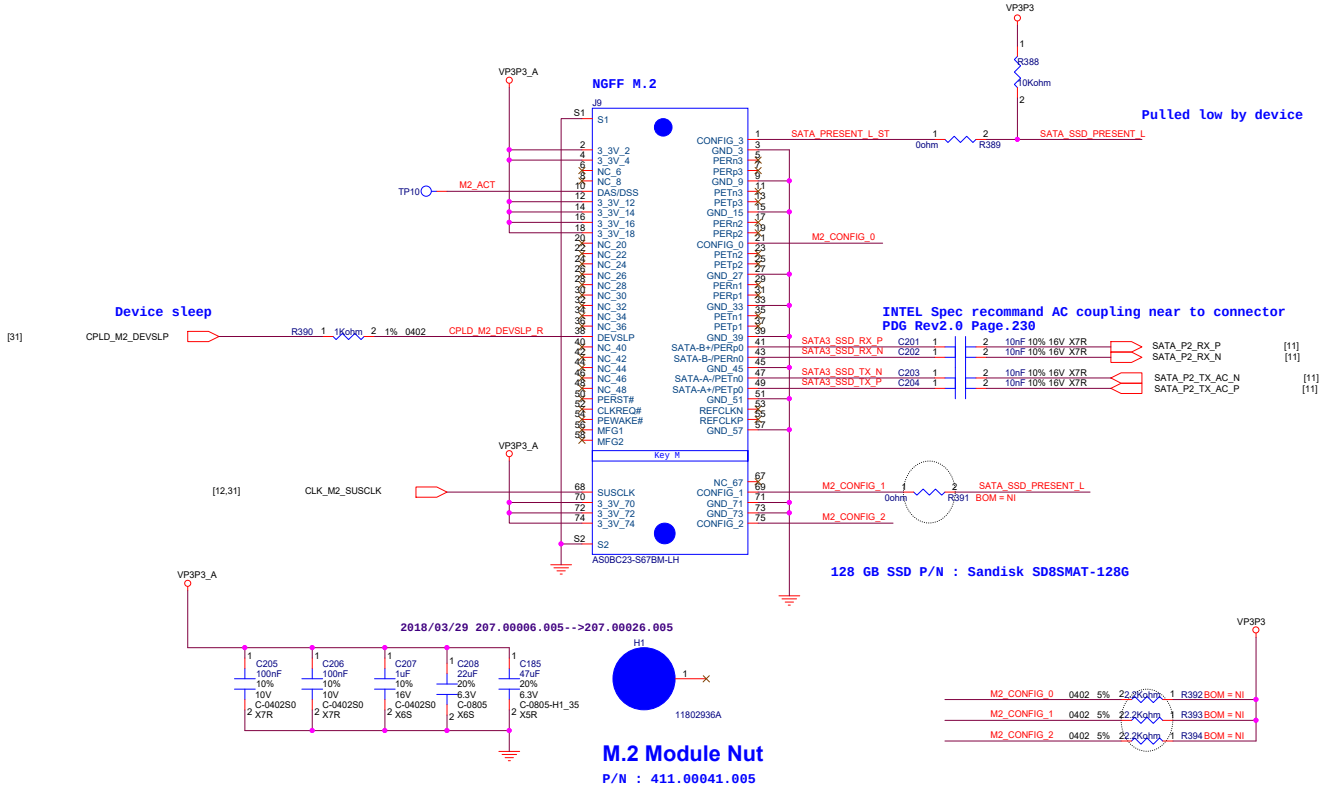


CPLD RESET IC



<Core Design>

Ufi Space Co., Ltd.	CONFIDENTIAL
Title: 34. CPLD (4/4)	
Size	Document Number / Project: T77O994T01 — Rev: BETA
Date:	Sheet 34 of 48



<Core Design>

Ufi Space Co., Ltd.	CONFIDENTIAL
Title: 35. M.2 CONN	
Size	Document Number / Project: T77O994T01 — Rev: BETA
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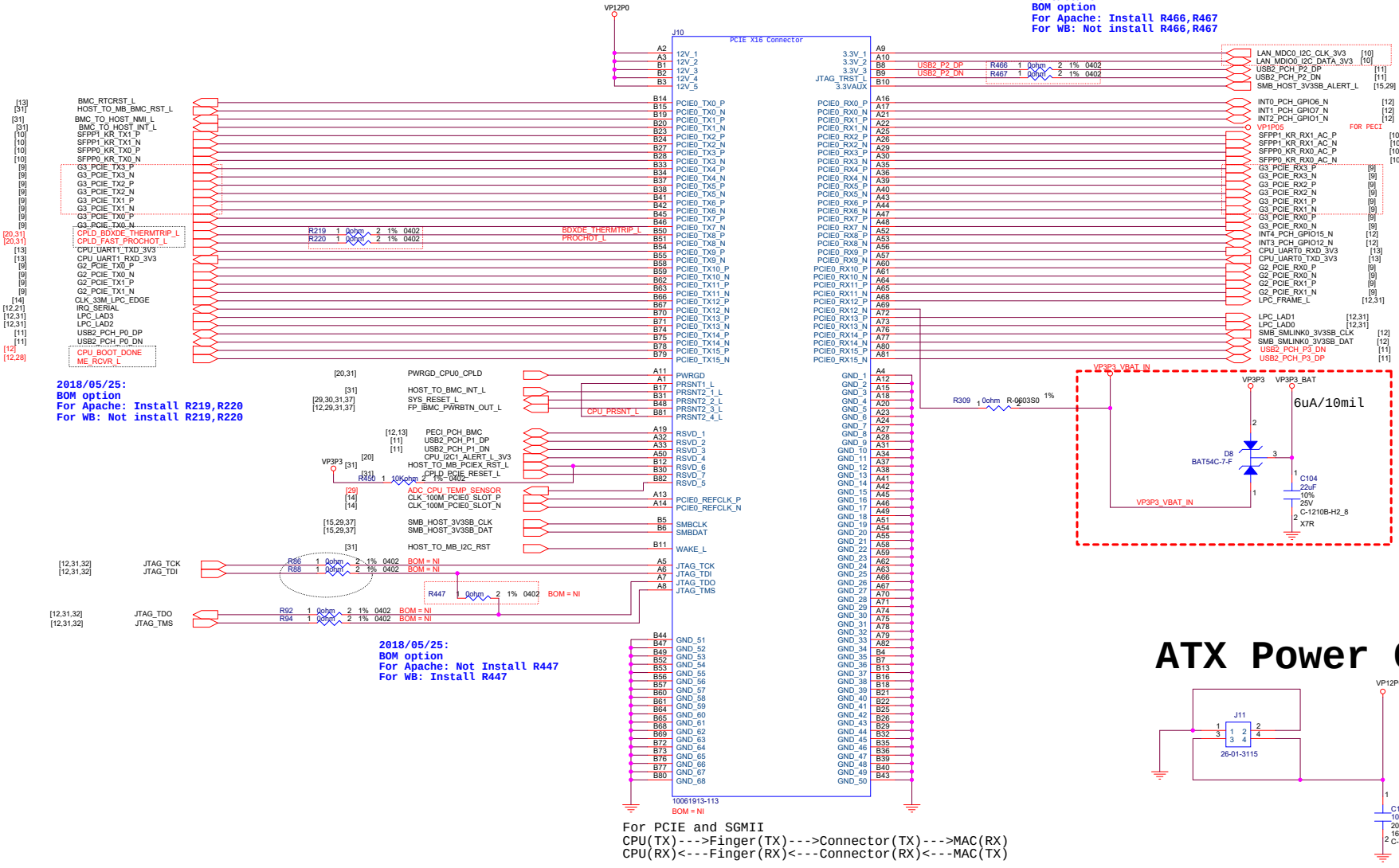
Gold Finger Connector



For PCIE and SGMII
CPU(TX)--->Finger(TX)--->Connector(TX)--->MAC(RX)
CPU(RX)<---Finger(RX)<---Connector(RX)<---MAC(TX)

[CAD]: 20mil

ATX Power Connector

<Core Design>

Ufi Space Co., Ltd.	CONFIDENTIAL
Title: 36. GOLD FINGER CONN	
Size	Document Number / Project: T77O994T01 — Rev: BETA
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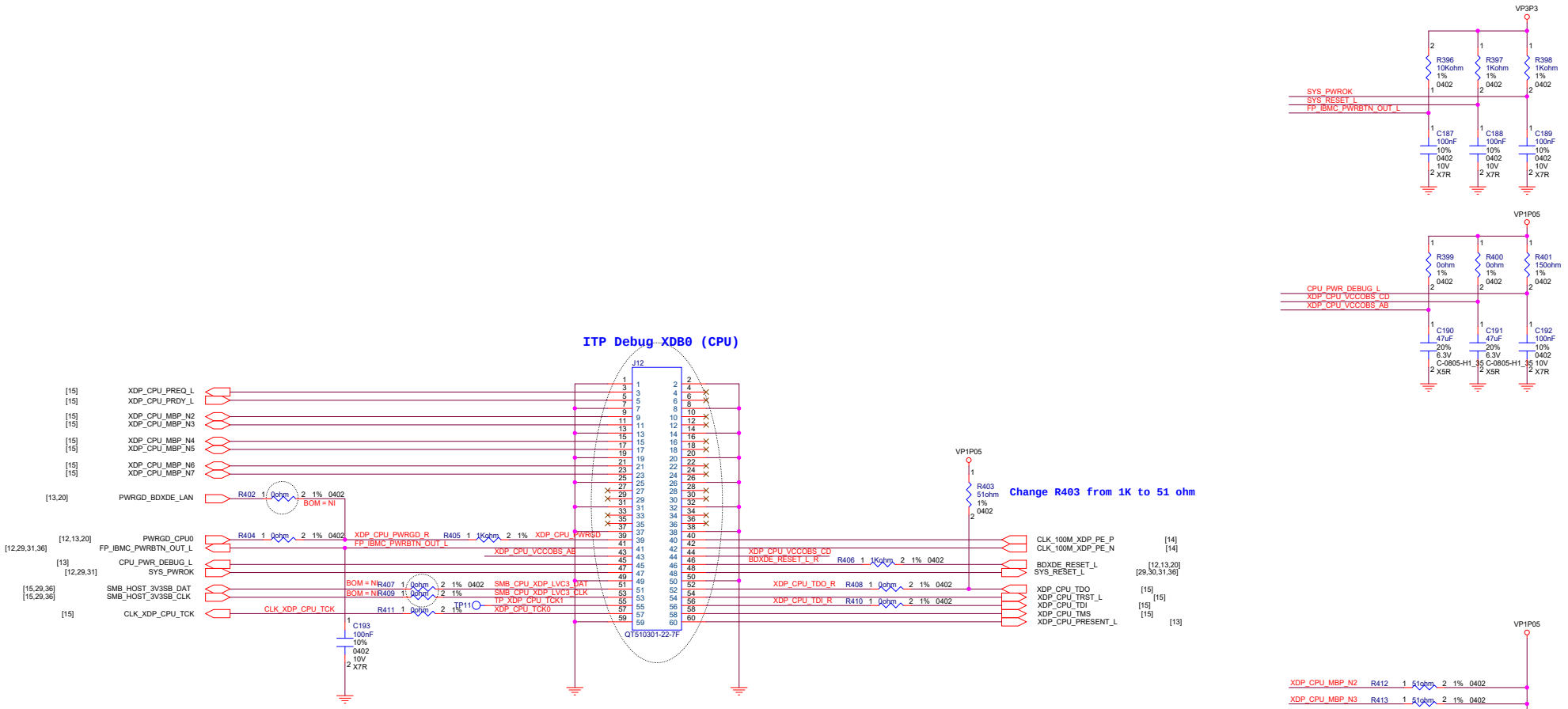

PLACE ALL THE CAPACITORS CLOSE TO THE XDP PIN.
FOR THE COUPLES OF LINES WITH DOUBLE CAPACITOR, ADD ONE PER XDP CONNECTOR

<Core Design>

Ufi Space Co., Ltd.	CONFIDENTIAL
Title: 37. MISC: ITP/XTP CONN	
Size	Document Number: Project: T77O994T01 — Rev: BETA
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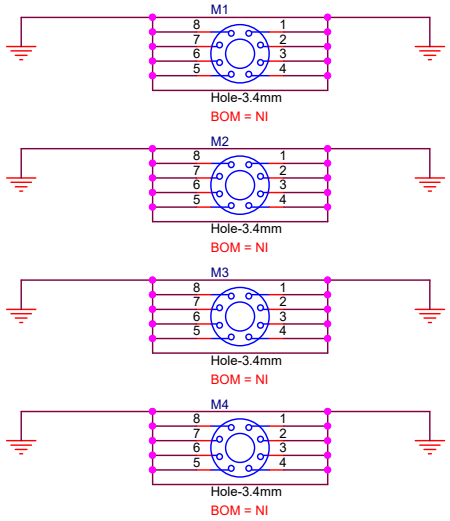
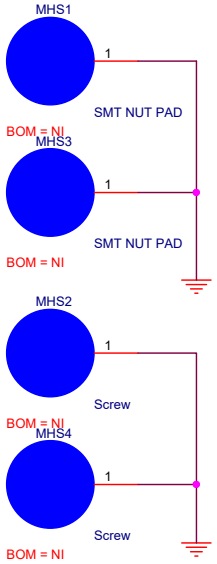


SMT NUT for Heatsink Assembled



BOM ONLY PARTS

BOM ONLY PARTS

P/N: 503.00860.005 LABEL BLANK	P/N: 400.00727.015 HEAT SINK CPU
P/N: 309.00149.015 PCB	P/N: JSCPUBP7045-B BRACKET CPU
P/N: JSDHM24-A28M41 SSD 128GB	P/N: 401.00024.005 SCREW M2.5 4mm
P/N: JSM4DS-8GMSQW0 SODIMM 8GB	P/N: TBD SPONGE EVA 62*14*2.3mm
P/N: JSM4DS-8GMSQW0 SODIMM 8GB	P/N: TBD SPONGE EVA 62*14*6mm

<Core Design>

Ufi Space Co., Ltd.	CONFIDENTIAL
Title: 38. MISCELLANEOUS	
Size	Document Number / Project: T77O994T01 — Rev: BETA
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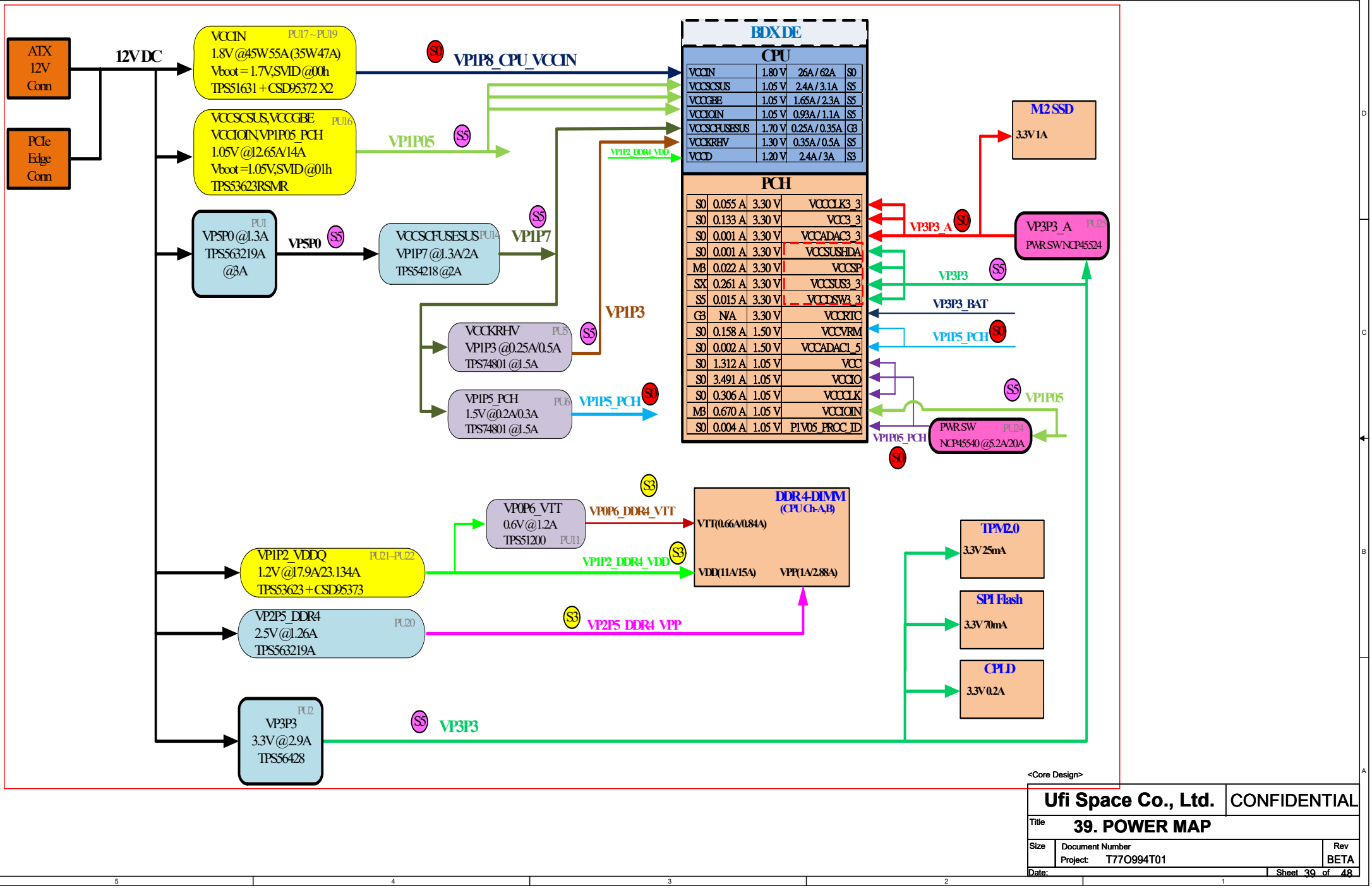

<Core Design>

Ufi Space Co., Ltd.		CONFIDENTIAL
Title	39. POWER MAP	
Size	Document Number Project: T77O994T01	Rev BETA
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INDEX	FUNCTION	MAX AMPS	Apache LABEL	BASED ON	Apache PAGE	INPUT
1	CPU_VCCIN_1.8V	55	VP1P8_CPU_VCCIN	TPS51631ARSMR	45	VP12P0
2	CPU_1.05V	14	VP1P05	TPS53623RSMR	47	VP12P0
3	CPU_1.7V	2	VP1P7	TPS54218RTER	46	VP5P0
4	CPU_1.3V	1.5	VP1P3	TPS74801DRCR	46	VP1P7
5	CPU_PCH_1.05V	14	VP1P05_PCH	NCP45540IMNTWG-H	47	VP1P05
6	CPU_PCH_1.5V	1.5	VP1P5_PCH	TPS74801DRCR	46	VP1P7
7	DDR4_1.2V	23	VP1P2_DDR4_VDD	TPS53623RSMR	44	VP12P0
8	DDR4_0.6V	1.2	VP0P6_DDR4_VTT	TPS51200DRCT	44	VP1P2_DDR4_VDD
9	DDR4_2.5V	1.26	VP2P5_DDR4_VPP	TPS563219A	44	VP12P0
10	5.0V STBY	1.3	VP5P0	TPS563219A	42	VP12P0
11	3.3V STBY	3	VP3P3	TPS56428DDAR	43	VP12P0
12	3.3V	3	VP3P3A	NCP45524IMNTWG-H	43	VP3P3

<Core Design>

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Title: 40. POWER TABLE

Size | Document Number | Rev

Project: T77O994T01 | BETA

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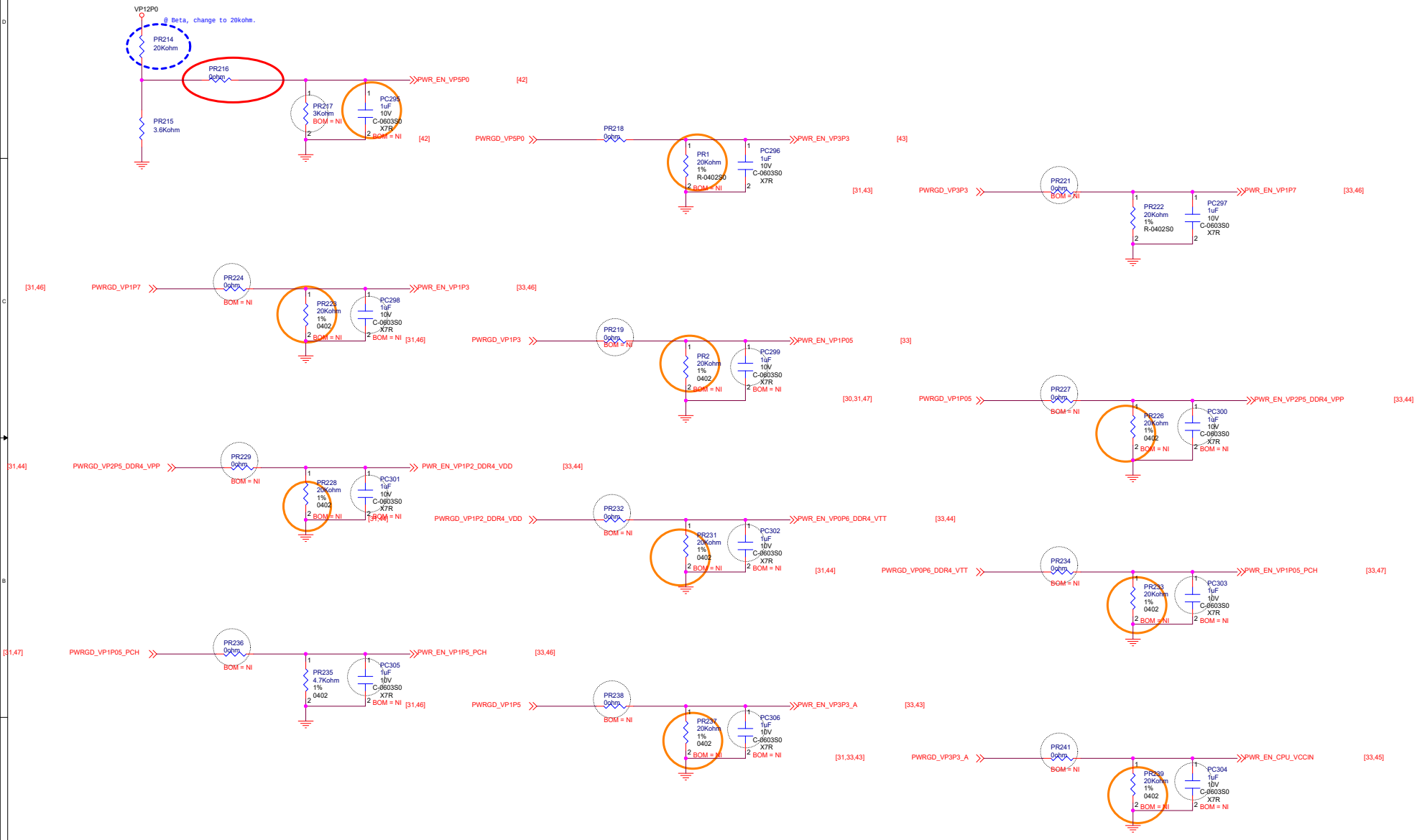
Power up Sequence



<Core Design>

Ufi Space Co., Ltd.		CONFIDENTIAL
Title	41.POWER SEQUENCE	
Size	Document Number	Rev
	Project: T77O994T01	BETA
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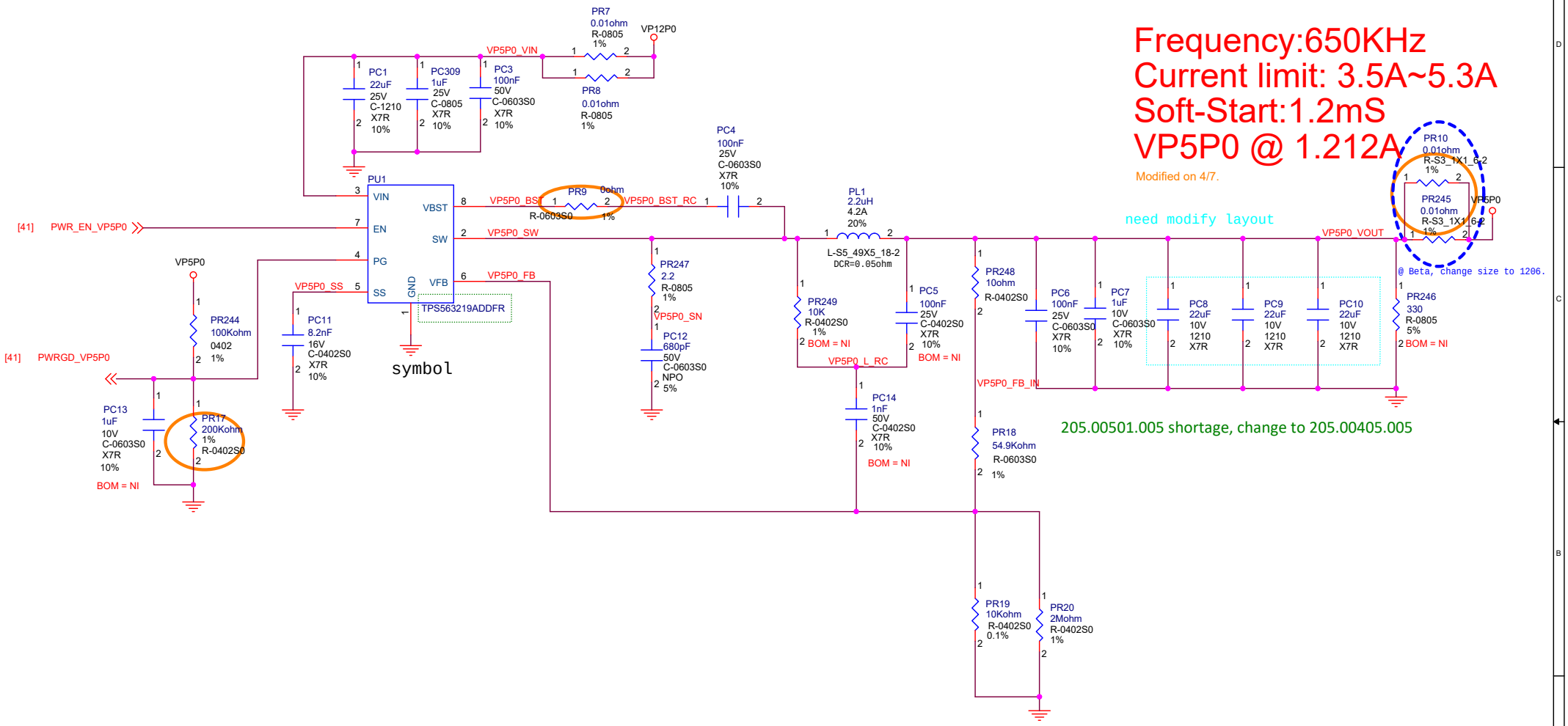

<Core Design>

Ufi Space Co., Ltd.	CONFIDENTIAL
Title: 42. 5V	
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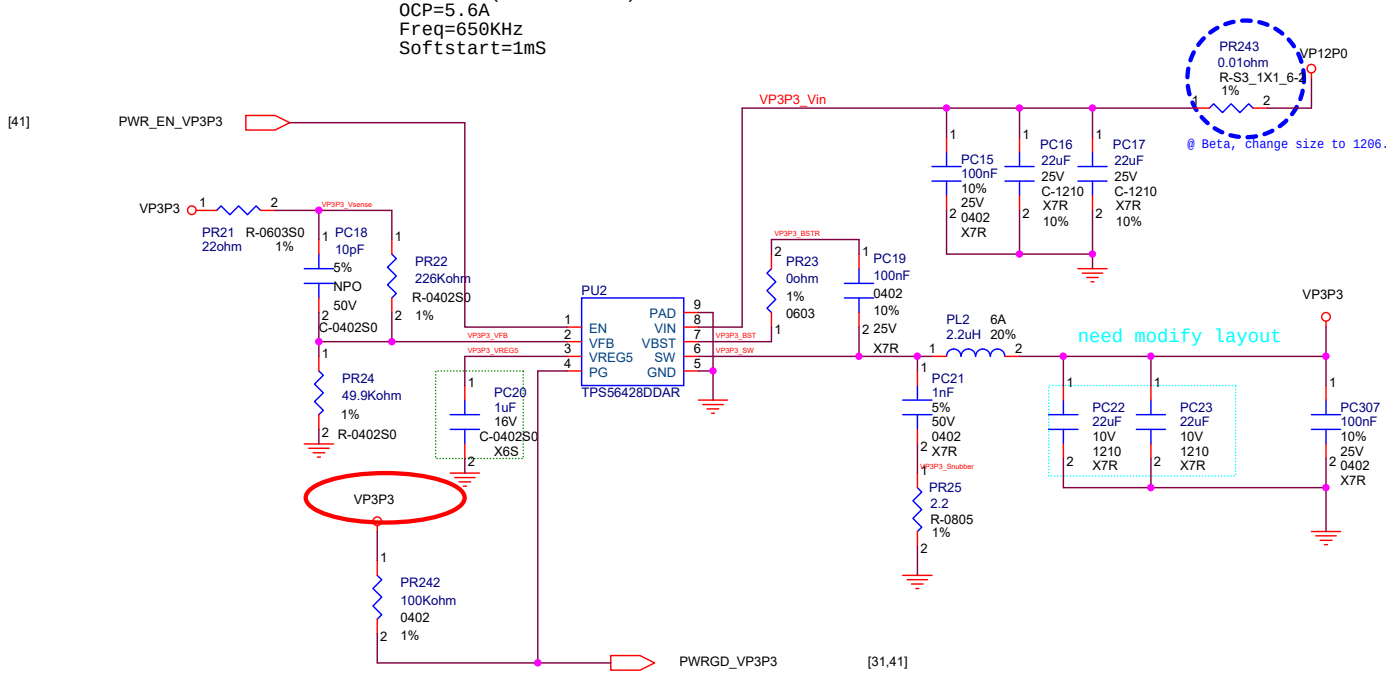
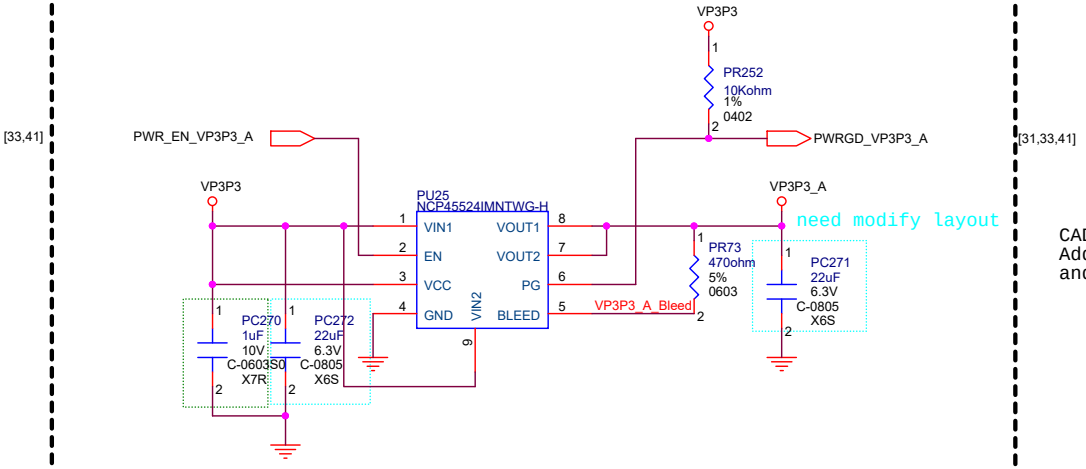
VP3V3 TPS56428 @ 2.886A

Modified on 4/7.

Vo=0.6V*(1+PR22/PR24)=3.317V
OCP=5.6A
Freq=650KHz
Softstart=1mS



VP3P3_A NCP45524



CAD NOTE:
Add divider circuit can make Enable pin not floating, and to avoid turn on /turn off error action.

<Core Design>

Ufi Space Co., Ltd.	CONFIDENTIAL	
Title: 43. 3.3V		
Size	Document Number Project: T77O994T01	Rev BETA
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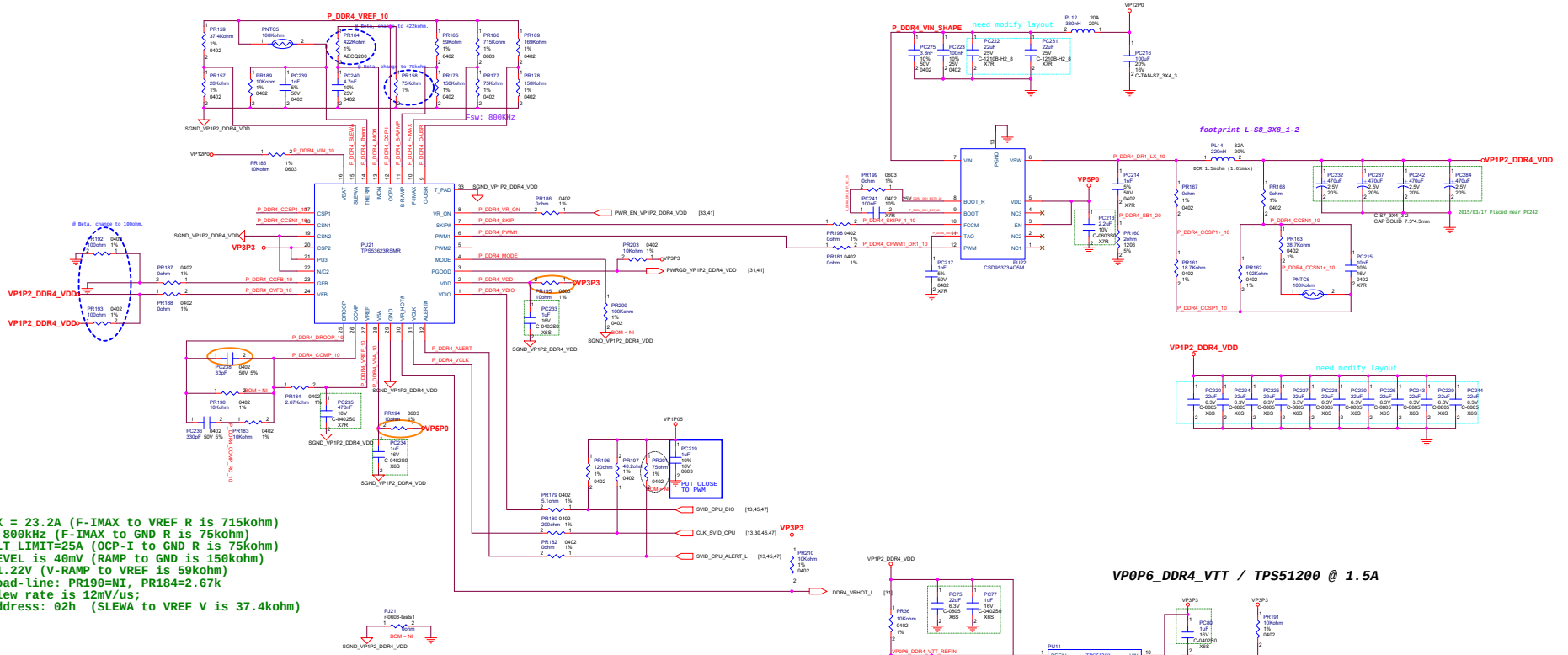
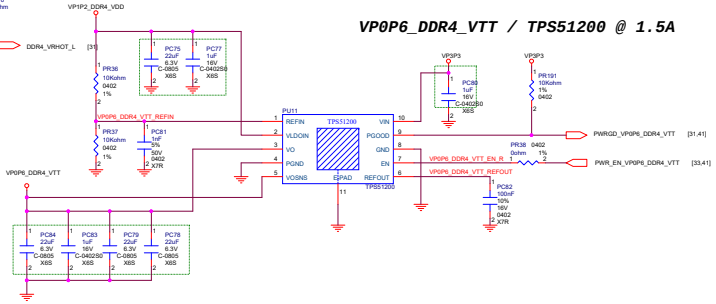
VP1P2_DDR4_VDD TPS53623 @ 22.934Amax (17.9A TDC)

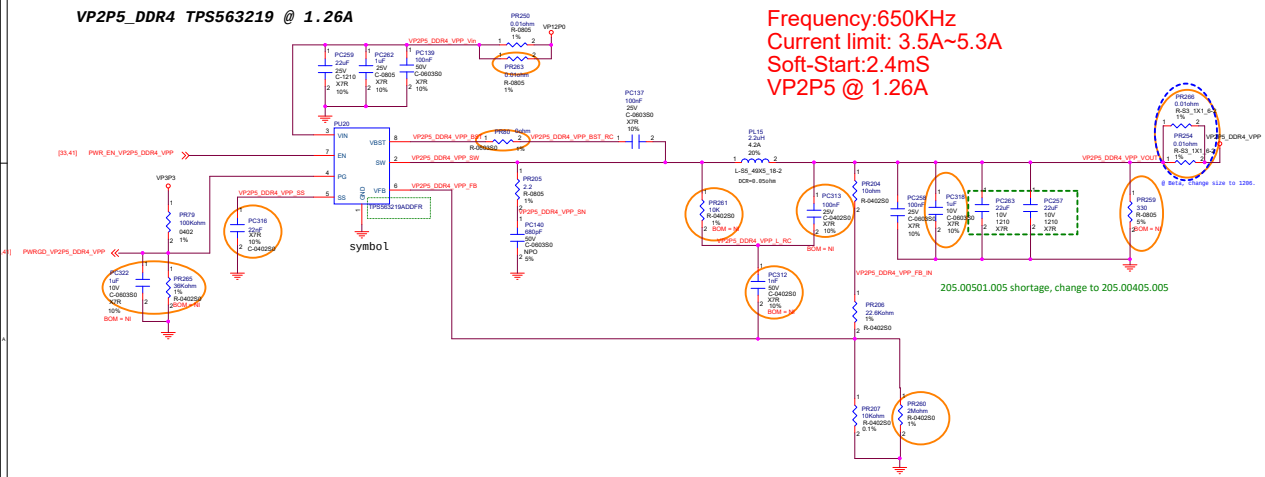


1. ICC_MAX = 23.2A (F-IMAX to VREF R is 715kohm)
2. Freq = 800kHz (F-IMAX to GND R is 75kohm)
3. OC_FAULT_LIMIT=25A (OCP-I to GND R is 75kohm)
4. RAMP LEVEL is 40mV (RAMP to GND is 150kohm)
5. VBOOT=1.22V (V-RAMP to VREF is 59kohm)
6. Zero Load-line: PR190=NI, PR184=2.67k
7. Vout slew rate is 12mV/us;
8. SVID Address: 02h (SLEWA to VREF V is 37.4kohm)

VP0P6_DDR4_VTT / TPS51200 @ 1.5A



VP2P5_DDR4 TPS563219 @ 1.26A



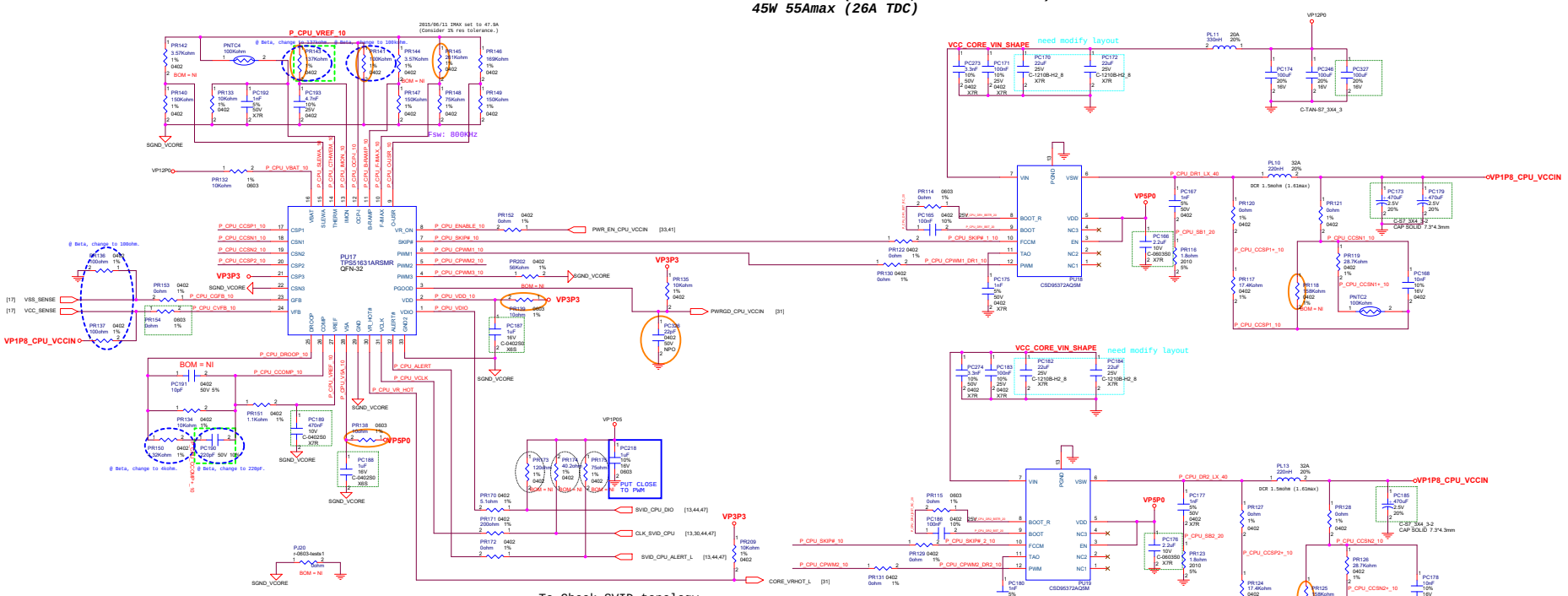
Frequency:650KHz
Current limit: 3.5A~5.3A
Soft-Start:2.4mS
VP2P5 @ 1.26A

205.00501.005 shortage, change to 205.00405.005

<Core Design>

Ufi Space Co., Ltd.		CONFIDENTIAL
Title	44. 2.5V / 1.2V / 0.6V	
Size	Document Number	Rev
	Project T77O994T01	BETA
Date:		Sheet 44 of 48

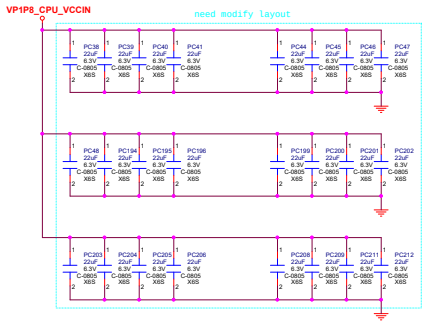
VCC_Core TPS51631A @ 25W 34Amax (15A TDC)
35W 47Amax (21A TDC, OCP set to 65A)
45W 55Amax (26A TDC)



To Check SVID topology

1. ICC_MAX = 57A (F-IMAX to VREF R is 261k)
2. Freq = 800kHz (F-IMAX to GND R is 75kohm)
3. OC_FAULT_LIMIT=70A (OCP-I to GND R is 100kohm)
4. RAMP_LEVEL is 40mV (RAMP to GND R is 150kohm)
5. VBOOT= 1.7V (RAMP to VREF R is OPEN)
6. Load-line: 1.5mV/A (PR151 is 1.1kohm)
7. Vout slew rate is 20mV/us (SLEWA to GND R is 150kohm)
8. SVID Address: 00h (SLEWA to VREF R is OPEN)
9. OSR disable (PWM3 to GND R is OPEN)

NI these two resistors to enable PWM2



<Core Design>

Ufi Space Co., Ltd.		CONFIDENTIAL
Title: 45. 1.8V		
Size	Document Number / Project: T77O994T01	Rev: BETA
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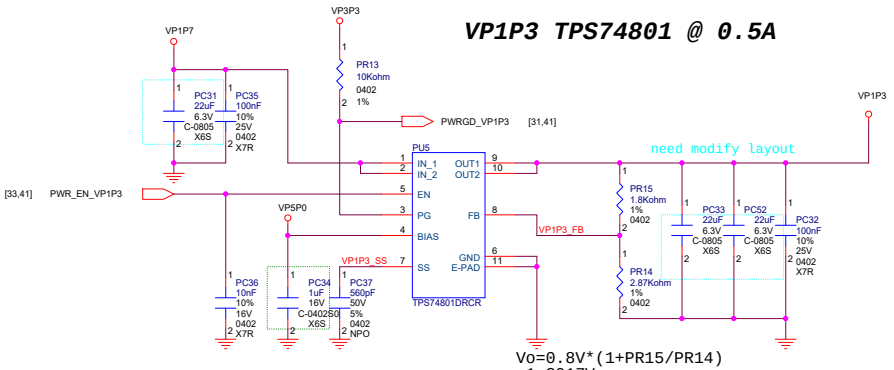
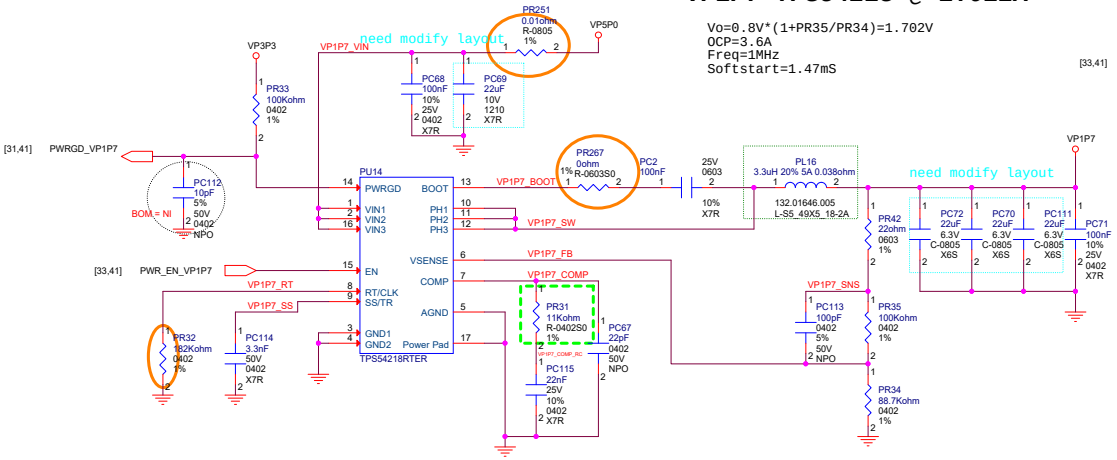
VP1P3 TPS74801 @ 0.5A



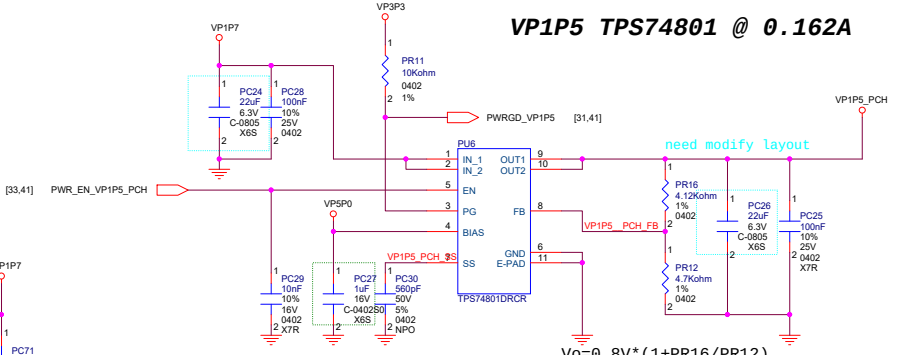
Vo=0.8V*(1+PR15/PR14)
=1.3017V

VP1P7 TPS54218 @ 1.012A

Vo=0.8V*(1+PR35/PR34)=1.702V
OCP=3.6A
Freq=1MHz
Softstart=1.47mS



VP1P5 TPS74801 @ 0.162A



Vo=0.8V*(1+PR16/PR12)
=1.501V

<Core Design>

Ufi Space Co., Ltd.		CONFIDENTIAL
Title	46.1.7V / 1.5V / 1.3V	
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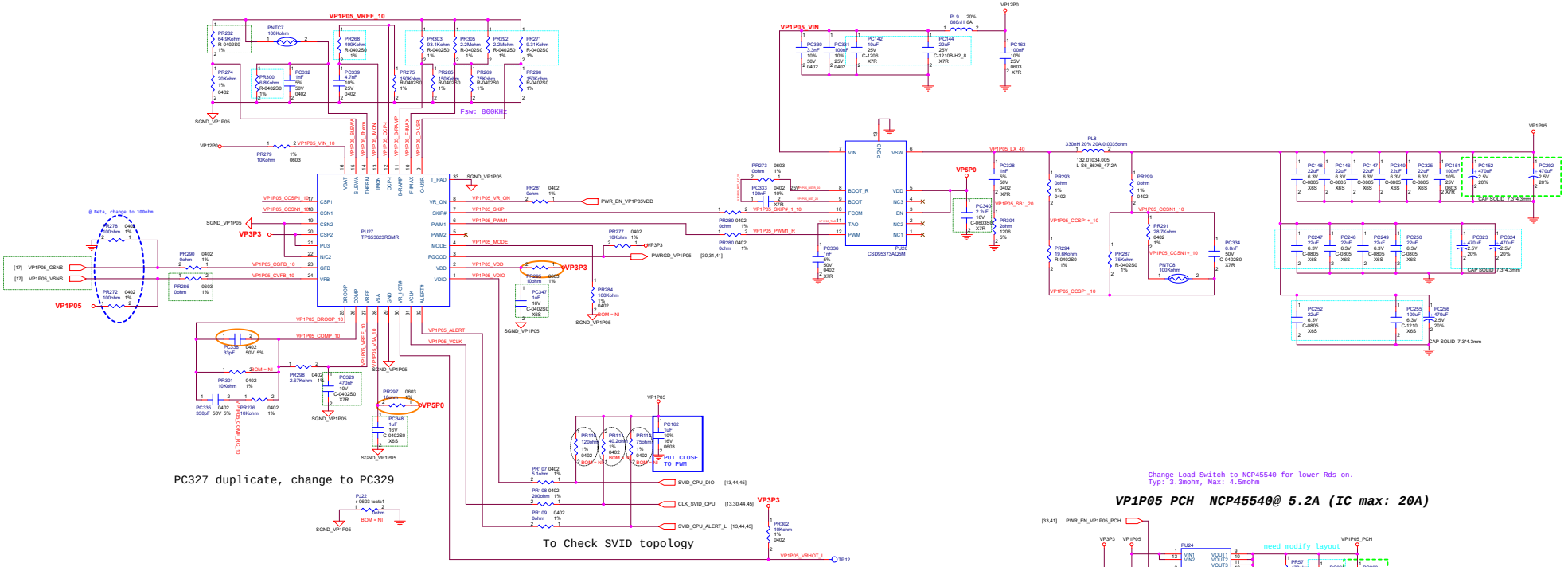
VP1P05_Combined @ 14Amax (12.65A TDC)



PC327 duplicate, change to PC329

To Check SVID topology

Change Load Switch to NCP45540 for lower Rds-on.
Typ: 3.3mohm, Max: 4.5mohm

VP1P05_PCH NCP45540@ 5.2A (IC max: 20A)

1. ICC_MAX = 15.2A (F-IMAX to VREF R is 1100k)
2. Freq = 800kHz (F-IMAX to GND R is 75kohm)
3. OC_FAULT_LIMIT=20A (OCP-I to GND R is 150kohm)
4. RAMP LEVEL is 40mV (RAMP to GND is 150kohm)
5. VBOOT=1.049V (V-RAMP to VREF is 93.1kohm)
6. Zero Load-line: PR301=NI, PR298=2.67k
7. Vout slew rate is 12mV/us;
8. SVID Address: 01h (SLEWA to VREF V is 64.9kohm)

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REVISION HISTORY:

REV	DATE	DESCRIPTION
Alpha	2018/01/19	1. Release for Alpha build.
Beta	2018/04/02	1. Page 47: PWR solution change (temp spec issue) Change NCP81109FMNTXG to TPS53623RSMR 2. Page 31: Add revision ID for CPLD 3. Page 13: NI R314, delete J4, change J3 to 1*4PIN SMD header
	2018/04/17	1. Page 11/Page 36: Add USB2_PCH_P3 for GPS 2. Page 36: Add ME_RCVR_L control by BMC 3. Page 29: Add ADC Thermal Sensor U36, place close to Broadwell-DE(U1) 4. PWR Sche modify: a. Page45: PR154 modify to 0603 size[262.01619.005] b. Page47: PR286 modify to 0603 size[262.01619.005] modify "VP1P05_GSNS", "VP1P05_VSNS" c. Page46: PL16 modify to 3.3uH[132.01646.005] d. Page42&Page 44: PU1,PU20 modify to TPS563219A[029.00700.005]
	2018/05/09	1. Page46: PR31 modify to 11kohm(261.00912.005) 2. Page44: PC77,PC83 modify to 1uF/0402[202.01411.005];Delete PC76 PC75,PC78,PC79,PC84 modify to 22uF/0805[207.00024.005] 3. Page30: Add R465/0 ohm[261.01173.005]
	2018/05/15	1. Page29: Add pull up/down on EEPROM address pins
	2018/05/17	1. Page10: Remove SMBus, delete U6,C105,C106,R22~R28 2. Page12: Delete NI parts R39,R40[0ohm/0402] 3. Page31: Delete R447
	2018/05/21	1. Page29: Change the CPU's EEPROM address from 0x51 to 0x57 to avoid the I2C address conflict 2. Page10: Add pull up resistors R468,R469[10kohm/0402/NI] 3. Page36: Add R219,R220,R466,R467[0ohm/0402],R447(NI)

REV	DATE	DESCRIPTION

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