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25G SFP28 Dual Port OCP 2.0 NIC Mezzanine Card

Version 1.0

Author: MiTAC Engineers

Reversion History

Date	Description
08/18/2018	Version1.0

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Contents

1 Summary	4
1.1 Block Diagram	4
1.2 Standard features.....	4
1.3 Board stack-up.....	6
2 Interface Connector	7
2.1 Signal Definitions	7
2.2 Connector Pinout	9
2.3 Retimers/Repeaters	11
2.4 Power	11
3 Mechanical Control Outline	12
4 Thermal	14
5 Standoffs and screws for assembly	14
6 Performance	15

Table of Figures

Figure 1: OCP mezzanine block diagram	4
Figure 2: Connector stackup example	6
Figure 3: Mechanical control outline for the OCP mezzanine card	12

Table of Tables

Table 1: OCP mezzanine board feature	4
Table 2: Connector manufacturing part numbers	7
Table 3: OCP mezzanine connector signal definitions	7
Table 4: OCP mezzanine connector pinout	9
Table 5: OCP mezzanine power ratings	11

1 Summary

This document specifies a technical design implementation to define 25G Ethernet card which meets the requirements of OCP Mezzanine card 2.0 type-A design, and the heat sink design could let this card to be able to deployment in OCP server or standard server. The scope is to define the requirements and constraints from hardware perspective, and to fully specify the functional elements and the interfaces of the product architecture.

1.1 Block Diagram

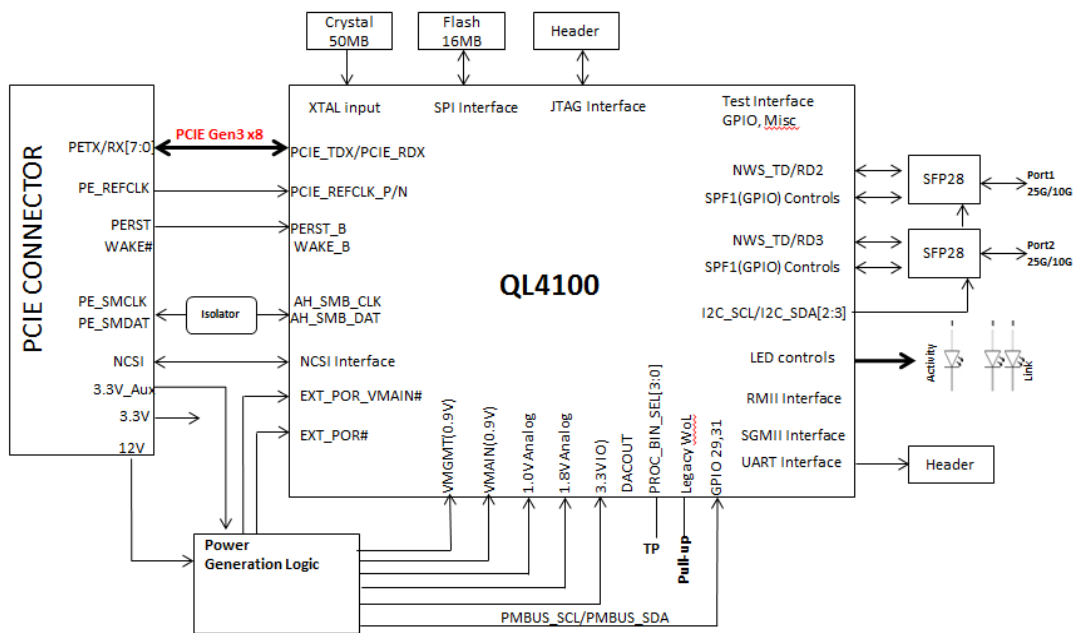


Figure 1: OCP mezzanine block diagram

1.2 Standard features

Table 1: OCP mezzanine board feature

Model	OCP 25G dual ML41202-2P
QL41202	<ul style="list-style-type: none"> ● Cavium Ethernet Controller QL41202. ● PCI Express v3.0 (8Gbps), v2.1 (5Gbps), v1.1 (2.5Gbps) ● PCI Express x8, x4, x1 lane ● Ports: dual 25Gbps or dual 10Gbps ● Support offload traffic types RDMA over Converged Ethernet (RoCE) on each of the ports and also support Internet wide area RDMA protocol (iWARP). ● Support data center bridging (DCB), including IEEE 802.1Qbb (Priority-based Flow Control) and 802.1Qaz (Enhanced Transmission Selection), and features capability for Edge Virtual Bridging (IEEE 802.1Qbg) and Bridge

Model	OCP 25G dual ML41202-2P
	<p>Port Extension (IEEE 802.1Qbh)</p> <ul style="list-style-type: none"> ● Integrate the network controller-sideband interface (NC-SI) ● Support at gigabit speeds over the serial gigabit media independent interface (SGMII) ● Support receive side scaling (RSS), single root I/O virtualization (SR-IOV), VLAN tagging, Layer 2 priority encoding, link aggregation, and full-duplex flow control 802.3 functions in the MAC ● Support IEEE 1588 PTP (Precision Timing Protocol) and IEEE 802.1AS, providing a method of synchronization between master and slave clock over a LAN ● Complies with the management component transport protocol (MCTP) over the system management bus (SMBus) standard ● Support L2 NIC (PXE boot) ● Wake-on-LAN (WoL) ● Support NPAR ● 525-pin 19mm x 19mm flip chip-plastic ball grid array (FC-PBGA) ● Maximum power consumption : 15 W
PCIe support	<ul style="list-style-type: none"> ● PCI Express v3.0 (8Gbps), v2.1 (5Gbps), v1.1 (2.5Gbps), x8, x4, x1 lane
Interface	<ul style="list-style-type: none"> ● Two external SFP28 connector. ● Equalization and retiming are provided in transmit and receive direction.
Temperature sensor	<ul style="list-style-type: none"> ● Ti TMP421AIDCNR. (Address: 0x3E meet OCP spec 2.0) ● SMBus™ SERIAL INTERFACE. ● REMOTE DIODE SENSOR. ● LOCAL TEMPERATURE SENSOR.
Flash	<ul style="list-style-type: none"> ● MX25L128 SPI Flash 128Mb Memory for Cavium boot. ● Storing product configuration information
FRU	<ul style="list-style-type: none"> ● M24C64-RDW6TP. (Address: 0xA2 meet OCP spec 2.0) ● Record PCB or vendor information.
Form Factor	<ul style="list-style-type: none"> ● Compatible OCP type-A SKU card.
NCSI	<ul style="list-style-type: none"> ● The adapter supports a slave Network Controller Sideband Interface (NC-SI) that can be connected to BMC (PS. Hardware design on product)
ESD and Surge Protection	<ul style="list-style-type: none"> ● Provides 2 kV of ESD protection. (Just plan not yet be verified) ● HBM: 2000 V. (Just plan not yet be verified)

1.3 Board stack-up

10-layer PCB Stack-Up

IT170GRA1				50 +/-5.0 ohm		85 +/- 8.5 ohm		100+/- 10.0 ohm	
				A組 單端		B組 差動		E組 差動	
層別疊構	材料規格	ER	預計厚度	原稿	AVG	原稿	AVG	原稿	AVG
				線寬	ohm	線寬/間距	ohm	線寬/間距	ohm
L1 SM	-		0.70						
L1 TOP	Cu+plating		1.60	4		4/5		3.5/10	
PP			2.56						
L2	1.0 oz		1.20						
CORE			4.00						
L3	1.0 oz		1.20	5		4.5/4		4.5/10.5	
PP			11.00						
L4	1.0 oz		1.20	5		4.5/4		4.5/10.5	
CORE			4.00						
L5	1.0 oz		1.20						
PP			6.12						
L6	1.0 oz		1.20						
CORE			4.00						
L7	1.0 oz		1.20	5		4.5/4		4.5/10.5	
PP			11.00						
L8	1.0 oz		1.20	5		4.5/4		4.5/10.5	
CORE			4.00						
L9	1.0 oz		1.20						
PP			2.56						
L10 BOT	Cu+plating		1.60	4		4/5		3.5/10	
L10 SM	-		0.70						
		總板厚:	62.04						
			1.58						

2. Interface Connector

The connector interfaces between the OCP mezzanine card and the motherboard use the FCI solution. The mezzanine card uses a FCI-Amphenol 61083-124402LF (male) connector and interfaces to the motherboard through a FCI 10135583-641402LF (female) connector. Table 2 lists the manufacturing part numbers (MPNs).

Table 2: Connector manufacturing part numbers

Manufacturer	Mezzanine card connector MPN	Mating (MB) connector MPN
FCI-Amphenol	61083-124402LF	10135583-641402LF

The stackup height of the OCP Card is 11.4mm, with a 7.7mm OCP Card and a 3.7mm MB connector. In this configuration, it is expected that taller components would be placed on the top side of the printed circuit board (PCB), as shown below in Figure 2.

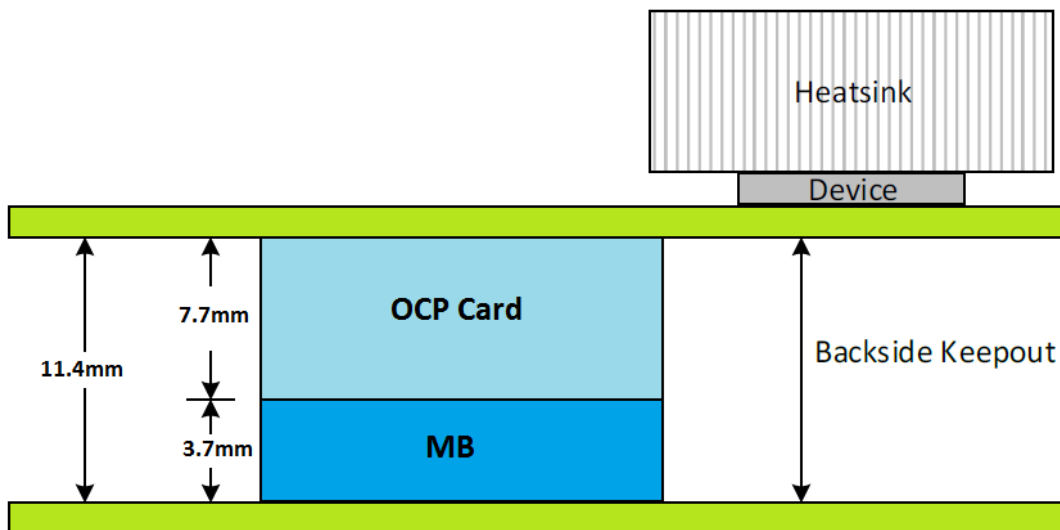


Figure 2: Connector stackup example

2.1 Signal Definitions

Table 3 defines the signals used in the OCP mezzanine interface.

Table 3: OCP mezzanine connector signal definitions

Mezzanine Connector			
61	P12V_STBY	1	GND
62	P12V_STBY	2	P5V_AUX
63	P12V_STBY	3	P5V_AUX
64	GND	4	P5V_AUX
65	GND	5	GND

66	P3V3_AUX	6	GND
67	GND	7	P3V3_AUX
68	GND	8	GND
69	P3V3_OCP	9	GND
70	P3V3_OCP	10	P3V3_OCP
71	P3V3_OCP	11	P3V3_OCP
72	P3V3_OCP	12	P3V3_OCP
73	GND	13	P3V3_OCP
74	P3V3_AUX	14	NCSI_RCSDV
75	SMB_LAN_3V3STB_CLK	15	NCSI_50M_RCLK
76	SMB_LAN_3V3STB_DAT	16	NCSI_TXEN
77	IRQ_LVC3_WAKE_N	17	RST_PERST1_MEZZ_N
78	NCSI_RXER	18	SMB_LAN_3V3STB_CLK
79	GND	19	SMB_LAN_3V3STB_DAT
80	NCSI_TXD0	20	GND
81	NCSI_TXD1	21	GND
82	GND	22	NCSI_RXD0
83	GND	23	NCSI_RXD1
84	CLK_100M_MEZZ_DP	24	GND
85	CLK_100M_MEZZ_DN	25	GND
86	GND	26	NC
87	GND	27	NC
88	MEZZ_PCIE_RX_DP0	28	GND
89	MEZZ_PCIE_RX_DN0	29	GND
90	GND	30	MEZZ_PCIE_TX_DP0
91	GND	31	MEZZ_PCIE_TX_DN0
92	MEZZ_PCIE_RX_DP1	32	GND
93	MEZZ_PCIE_RX_DN1	33	GND
94	GND	34	MEZZ_PCIE_TX_DP1
95	GND	35	MEZZ_PCIE_TX_DN1
96	MEZZ_PCIE_RX_DP2	36	GND
97	MEZZ_PCIE_RX_DN2	37	GND
98	GND	38	MEZZ_PCIE_TX_DP2
99	GND	39	MEZZ_PCIE_TX_DN2

100	MEZZ_PCIE_RX_DP3	40	GND
101	MEZZ_PCIE_RX_DN3	41	GND
102	GND	42	MEZZ_PCIE_TX_DP3
103	GND	43	MEZZ_PCIE_TX_DN3
104	MEZZ_PCIE_RX_DP4	44	GND
105	MEZZ_PCIE_RX_DN4	45	GND
106	GND	46	MEZZ_PCIE_TX_DP4
107	GND	47	MEZZ_PCIE_TX_DN4
108	MEZZ_PCIE_RX_DP5	48	GND
109	MEZZ_PCIE_RX_DN5	49	GND
110	GND	50	MEZZ_PCIE_TX_DP5
111	GND	51	MEZZ_PCIE_TX_DN5
112	MEZZ_PCIE_RX_DP6	52	GND
113	MEZZ_PCIE_RX_DN6	53	GND
114	GND	54	MEZZ_PCIE_TX_DP6
115	GND	55	MEZZ_PCIE_TX_DN6
116	MEZZ_PCIE_RX_DP7	56	GND
117	MEZZ_PCIE_RX_DN7	57	GND
118	GND	58	MEZZ_PCIE_TX_DP7
119	GND	59	MEZZ_PCIE_TX_DN7
120	GND	60	GND

2.2 Connector Pinout

Table 4 lists the pinout for the 64-pin OCP mezzanine connector.

Table 4: OCP mezzanine connector pinout

Connector A			
Signal	Pin	Pin	Signal
P12V_AUX/P12V	A61	A1	MEZZ_PRSN1A1_N /BASEBOARD_A_ID
P12V_AUX/P12V	A62	A2	P5V_AUX
P12V_AUX/P12V	A63	A3	P5V_AUX
GND	A64	A4	P5V_AUX
GND	A65	A5	GND
P3V3_AUX	A66	A6	GND
GND	A67	A7	P3V3_AUX
GND	A68	A8	GND

P3V3	A69	A9	GND
P3V3	A70	A10	P3V3
P3V3	A71	A11	P3V3
P3V3	A72	A12	P3V3
GND	A73	A13	P3V3
LAN_3V3STB_ALERT_N	A74	A14	NCSI_CRSDV
SMB_LAN_3V3STB_CLK	A75	A15	NCSI_RCLK
SMB_LAN_3V3STB_DAT	A76	A16	NCSI_TXEN
PCIE_WAKE_N	A77	A17	PERST_NO
NCSI_RXER	A78	A18	MEZZ_SMCLK
GND	A79	A19	MEZZ_SMDATA
NCSI_TXD0	A80	A20	GND
NCSI_TXD1	A81	A21	GND
GND	A82	A22	NCSI_RXD0
GND	A83	A23	NCSI_RXD1
CLK_100M_MEZZ0_DP	A84	A24	GND
CLK_100M_MEZZ0_DN	A85	A25	GND
GND	A86	A26	CLK_100M_MEZZ1_DP
GND	A87	A27	CLK_100M_MEZZ1_DN
MEZZ_TX_DP_C<0>	A88	A28	GND
MEZZ_TX_DN_C<0>	A89	A29	GND
GND	A90	A30	MEZZ_RX_DP<0>
GND	A91	A31	MEZZ_RX_DN<0>
MEZZ_TX_DP_C<1>	A92	A32	GND
MEZZ_TX_DN_C<1>	A93	A33	GND
GND	A94	A34	MEZZ_RX_DP<1>
GND	A95	A35	MEZZ_RX_DN<1>
MEZZ_TX_DP_C<2>	A96	A36	GND
MEZZ_TX_DN_C<2>	A97	A37	GND
GND	A98	A38	MEZZ_RX_DP<2>
GND	A99	A39	MEZZ_RX_DN<2>
MEZZ_TX_DP_C<3>	A100	A40	GND
MEZZ_TX_DN_C<3>	A101	A41	GND
GND	A102	A42	MEZZ_RX_DP<3>
GND	A103	A43	MEZZ_RX_DN<3>
MEZZ_TX_DP_C<4>	A104	A44	GND
MEZZ_TX_DN_C<4>	A105	A45	GND
GND	A106	A46	MEZZ_RX_DP<4>
GND	A107	A47	MEZZ_RX_DN<4>
MEZZ_TX_DP_C<5>	A108	A48	GND
MEZZ_TX_DN_C<5>	A109	A49	GND
GND	A110	A50	MEZZ_RX_DP<5>
GND	A111	A51	MEZZ_RX_DN<5>
MEZZ_TX_DP_C<6>	A112	A52	GND
MEZZ_TX_DN_C<6>	A113	A53	GND
GND	A114	A54	MEZZ_RX_DP<6>
GND	A115	A55	MEZZ_RX_DN<6>
MEZZ_TX_DP_C<7>	A116	A56	GND
MEZZ_TX_DN_C<7>	A117	A57	GND
GND	A118	A58	MEZZ_RX_DP<7>
GND	A119	A59	MEZZ_RX_DN<7>
MEZZ_PRSENTA2_N	A120	A60	GND

2.3 Retimers/Repeaters

No Retimers/Repeaters on this OCP Mezz card.

2.4 Power

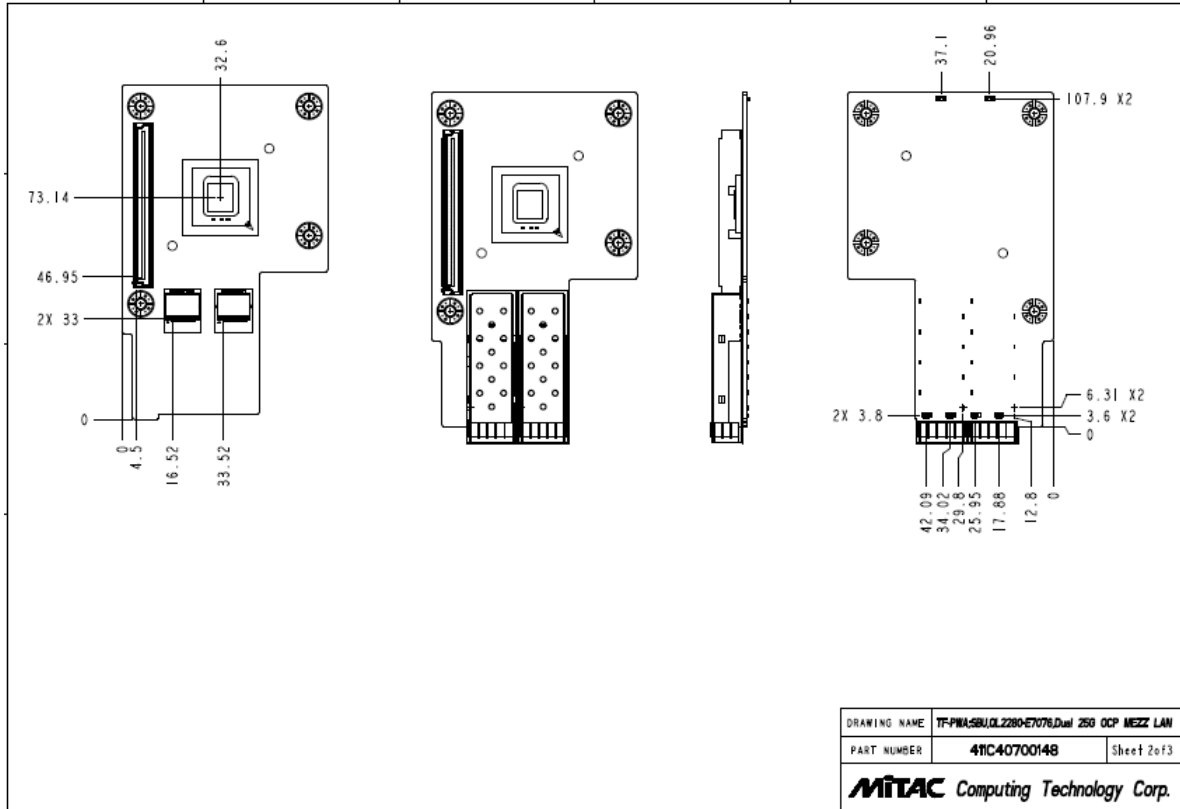
Table 5 shows the mezzanine power rates for total of the power rails, it's follow stand OCP2.0 Spec. Note that the maximum power consumption for of the mezzanine card is 15 W. Besides, QL41202 chip power consumption also listed below.

Table 5: OCP mezzanine power ratings

Power Rail	Voltage Tolerance	# of pins	Current Capability	Status
P12V_AUX/P12V	±8%(max)	3	2.4A	Auxiliary Power/Normal Power
P5V_AUX	±9%(max)	3	2.4A	Auxiliary power
P3V3_AUX	±5%(max)	2	1.6A	Auxiliary power
P3V3	±5%(max)	8	6.4A	Normal power

3 Mechanical Control Outline

Figure 3 shows the mechanical outline requirements for the OCP mezzanine card.



Form factor follow OCP V2.0 suggestion

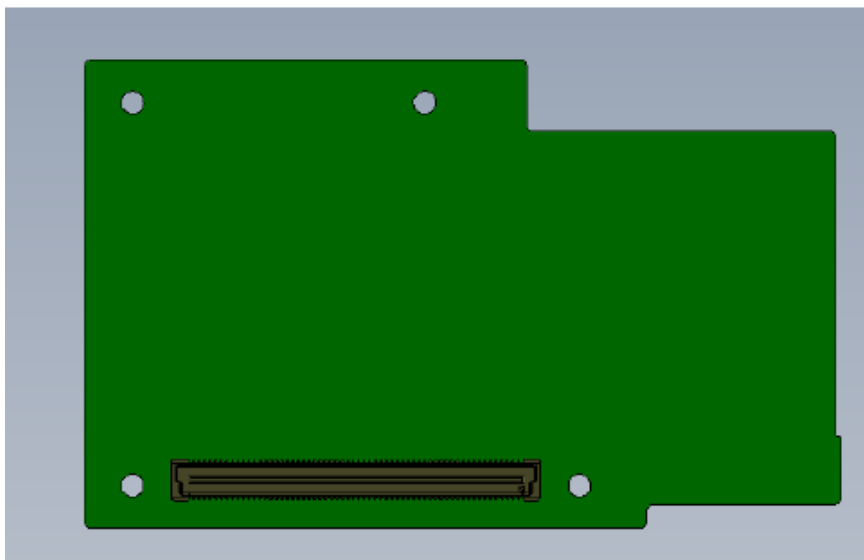


Figure 6: Default Form Factor in Horizontal Plane

Same location as OCP suggestion for the port and LED

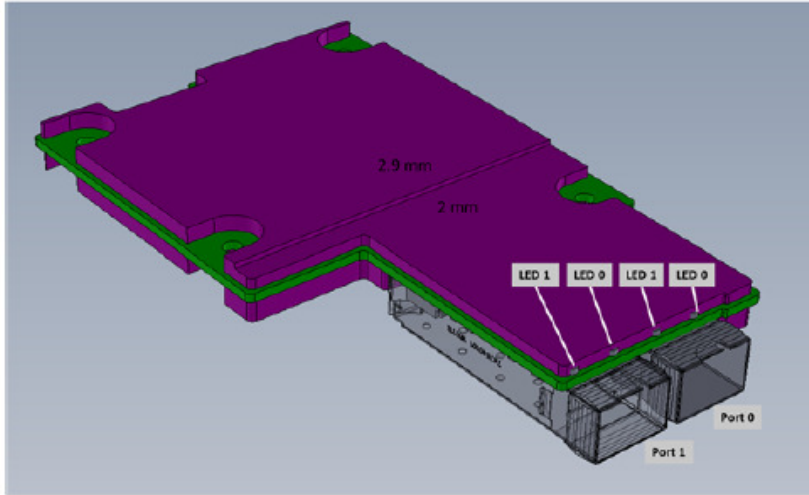


Figure 22: Single/Dual SFP+/SFP28 port Mezzanine card port and LED location

NOTES: (UNLESS OTHERWISE SPECIFIED):

1. REFERENCE DOCUMENTS:
1-1 ASME Y14.5M-1994.
2. INTERPRET DIMENSIONS PER ASME Y14.5M-1994.
3. THE DIMENSIONS SPECIFIED IN THE DRAWING MUST FOLLOW TOLERANCE TABLE. (STRENGTHEN: PLEASE REFER TO GENERAL FILE FOR DETAIL DEFINE).
4. THIS DRAWING IS FOR CHECKING PHYSICAL DIMENSIONS AND FEATURES OF THE BOARD ONLY. FOR ACTUAL PCB, REFER TO GENERAL FILE TOLERANCE TABLE.
5. MATERIAL: SHALL FOLLOW GENERAL FILES DEFINITION. BOARD CONSTRUCTION SHALL BE SOLDER MASK OVER SAWE COPPER.
6. COMPONENTS DIMENSIONED TO PIN 1.
7. DRAWING FOR EACH DESIGNER REFERENCE ONLY. EACH LAYOUT SHALL MATCH LATEST PRO-E TOP FILE.
8. PCB DRAWING IS FOR MITAC INTERNAL REFERENCE ONLY. PCB VENDOR SHALL REFER TO PCB BOARD DRAWING ONLY AND FOLLOW GENERAL FILES FOR PCB FABRICATION.
9. UPON RECEIVING THIS FABRICATION DRAWING AND CONFIRMING ALL THE DESIGN REQUIREMENTS WITH MITAC, THE CONTRACTOR/MANUFACTURER OF THIS SUBJECT PART SHOULD IMMEDIATELY FOLLOW PROCEDURE TO LOG IN MITAC ESP SYSTEM TO REVIEW ENVIRONMENTAL REQUIREMENT LISTED IN THE SYSTEM FOR PROPOSED MATERIAL SELECTION. COLLECT ENVIRONMENTAL COMPLIANCE DOCUMENTS (TEST REPORTS/MSDS/SDS) BASED ON MITAC REQUIREMENT, AND UPLOAD THOSE DOCUMENTS TO ESP SYSTEM FOR MITAC ASSESSMENT.

ITEM	DESCRIPTION	PART NO.	Q'TY
1	TF-CON; SBU, ORACLE, 1090450, ZSPF+, 10Pin*2, 0.8mm, R/A, GOLD 30u", LCP, BLACK, UL 94V-0	29100000020	2
2	TF-IC; LAN, SBU, QL41202, FC-PBGA, 525Pin, Gen3 PCI Express Converged 25G	28407000379	1
3	TF-LED; SBU, ORG, WATER CLEAR, 25mA, 2V, 600nm, 70mcd, 0603(1608)	29415000201	2
4	TF-LED; SBU, ROUND, GREEN, D3MM, R/A, W/HOLDER, SMT	29415000344	2
5	TF-LED; SBU, GRN/YEL, WATER CLEAR, 20/25mA, 3.3/2.0V, 520/585.5nm, 112/57mcd, 240.8mm	29415000327	2
6	TF-CON; FINE PITCH HDR, SBU, 60Pin*2, 0.8mm, MA, ST, GOLD 8u", TWO SIDE, NATURE, LCP(Liquid Crystal Polymer)	29130000063	1
7	TF-CONNECTOR CAGE; SBU, ZSPF+ cage, 1 part, tray, nickel plating, QL2280-E7076	34C40700004	2
8	TF-PCB; SBU, QL2280-E7076, Dual 25G OCP MEZZ LAN, ROA, 110.05 x 68mm, T=1.57mm, Immersion Silver, 10 Layer	316C40700020	1

TOL C										DATE	TREATMENT	MATERIAL	SEE NOTES	REVISION	ROA
RANGE	MI	SI	P1	P2	8	UNIT	SCALE	DRAWING NAME	PART NUMBER	DESIGNED	CHECKED	APPROVED	41C4070048	Sheet 1 of 3	
0-6	.05	0.1	.05	0.2	.05	mm	1.000	TF-PWA,SBU,QL2280-E7076,Dual 25G OCP MEZZ LAN							
>6-30	0.1	0.2	.15	.05	.15										
>30-60	.15	.25	0.2	.25	.25										
>60-100	.15	0.3	.25	.45	.25										
>100-315	0.2	.35	0.4	0.6	0.6										
>315-800	.25	0.5	0.7	1.1	0.8										

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Figure 3: Mechanical control outline for the OCP mezzanine card

4 Thermal

The mezzanine card is presented with an approaching airflow temperature of 70°C and a flow rate of 0.61m/s. No downstream airflow requirements are placed on the mezzanine card.

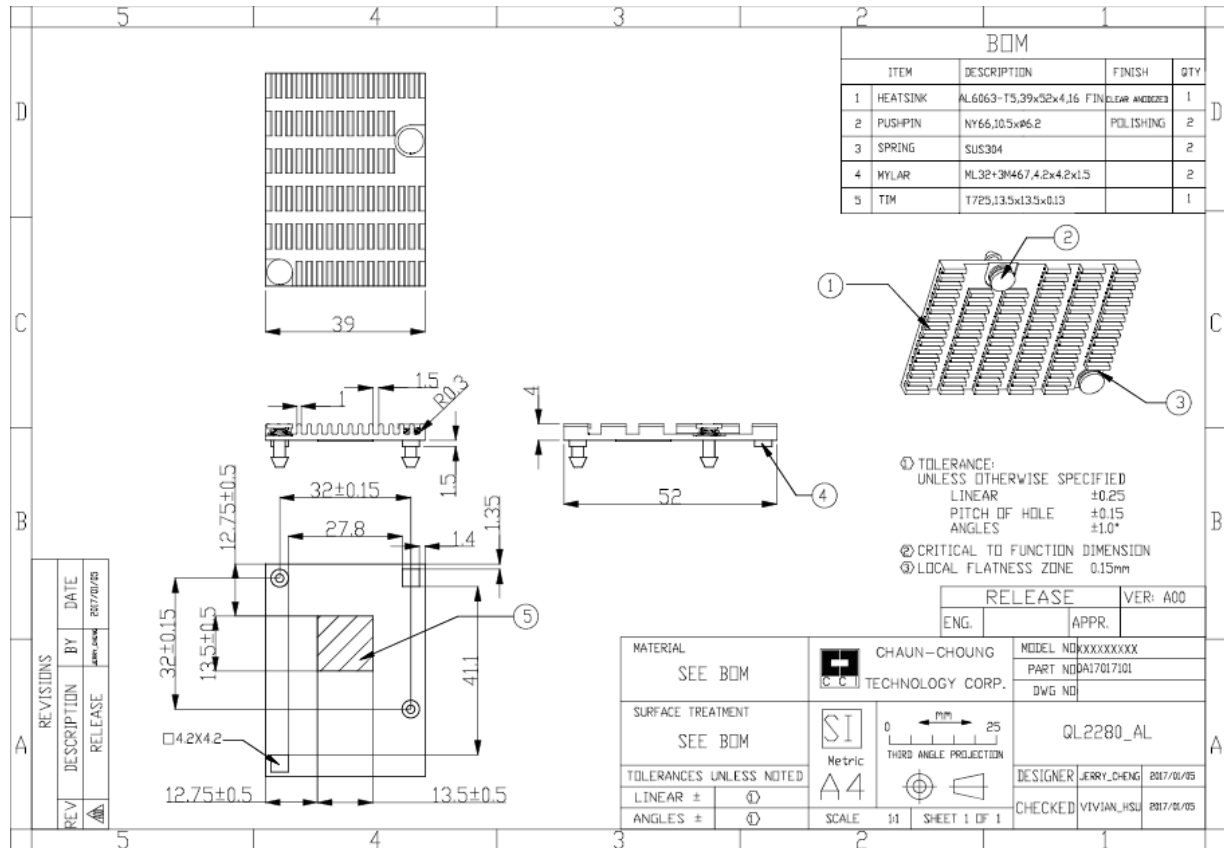


Figure 4: Thermal heat sink design

5 Standoffs and Screws for Assembly

The standoffs that hold the OCP mezzanine card on the motherboard are soldered, therefore the OCP mezzanine card manufacturer needs to supply only two 6-32 screws with the mezzanine cards. The screws are to be provided loose in a bag and secured during assembly of the card to the motherboard.

6 Performance

Test config	Description			
System	Leopard			
CPU	Intel Xeon E5-2678 v3 @ 2.50GHz x2			
DIMM	Micro MTA18ASF1G72PZ-2G1 DDR4 PC4-2133 8GB			
Lan Cable	Mellanox_MCP2M00-A003 REV:A3_Passive Copper cable, ETH, up to 25Gb/s, SFP28, 3m, 30AWG			
OCP card	Description	FW	Driver	OS
OCP 25G dual ML41202-2P	SM_NH2_E54_5411C4070022_25G SFP28 X2 Qlogic MEZZ CARD_QL2280_UOA1	8.18.11.0	kmod-qlgc-fastlinq-8.15.7.0-1.rhel7u3.x86_64.rpm qlgc-fastlinq-8.15.7.0-1.rhel7u3.src.rpm qlgc-libqedr-8.15.2.0-1.rhel7u3.src.rpm qlgc-libqedr-8.15.2.0-1.rhel7u3.x86_64.rpm	RHEL 7.3
OCP card	Result	Setting		
OCP 25G dual ML41202-2P	port0 : 23509 Mbits/sec port1 : 23511 Mbits/sec	iperf -c 192.168.1.50 -f m -t 86400 -P 4 -M 1500		
Note: iPerf result by back to back test				