EDGECORE Networks Corporation

Edgecore AS7900-32X

Switch Specification

Revision 1.1

OPEN

Compute Project

Revision History

Revision	Date	Author	Description
1.0	3/13/2018	Jeff Catlin	Initial Release
1.1	3/24/2018	Jeff Catlin	Minor clean up

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Description	**Manufacturer**	**Part Number**
T2080 CPU	Freescale	T2080NSN8TTB
SDRAM (8GB per channel)	UNIGEN	UG10U7211P8UU-BDE *2
USB to NAND Flash 8GB	ATP	AF8GSSGH-AC2
NOR Flash 128MB	MICRON	JS28F00AM29EWHA
Trusted Platform Module (TPM)	ST	ST33ZP24AR28PVSK
mSATA Connector	TE	1775838-2
M.2 connector	CONCRAFT	213BAAA32FA
SD Connector	CVILUX	CSD-09A001D
Switching Silicon	Broadcom	56980
10/100/1000 PHY	Broadcom	BCM54616S
Fans	AVC	DFPH0456B2UY006
CPLD (2)	Lattice	LCMXO3LF-1300C-5BG256C 2.5/3.3V caBGA256
CPLD	Lattice	LCMXO3LF-4300C-5BG324C 2.5V/3.3V caBGA324

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Scope

This document outlines the technical specifications for the Edgecore AS7900-32X Open Switch Platform submitted to the Open Compute Foundation.

Overview

This document describes the technical specifications of the AS7900-32X Leaf/Spine switch designed by Edgecore Networks Corporation. The AS7900-32X is a cost optimized switch design focused on Leaf/Spine deployments which support 400/100G. The AS7900-32X switch supports thirty-two QSFP-DD ports that each can operate at 10/25/40/50/100/200/400G modes of operation (different per port configurations supported based upon speed selected).

The AS7900-32X is a PHY-Less design with the QSFP28-DD connections directly attaching to the Serdes interfaces of the Broadcom 56980 switching silicon providing the lowest cost, latency, and power. The AS7900-32X supports traditional features found in Top of Rack / Leaf / Spine switches such as:

- Redundant field replaceable power supply and fan units
- Support for “Front to Back” or “Back to Front” air flow direction
- The AS7900-32X supports various Open Source CPU modules offered by Edgecore Networks which include the following:
    - Atom based C2538 based CPU module made publicly available through the OCP accepted AS7712-32X design

http://files.opencompute.org/oc/public.php?service=files&t=3d2271fd0e40a66725a747030487d571

    - Xeon based D-1518 based CPU module made publicly available through the OCP accepted AS7800-64X design

http://files.opencompute.org/oc/public.php?service=files&t=d2b4bfed8dfc024a1f2ece0db57118ee

    - Freescale T2080 based CPU module which is referenced in this specification

The AS7900-32X is a 1RU design that supports standard 19” rack deployments as well as standard 21” Open Rack deployments with the ORSA-1RU.

1.0 Introduction

The AS7900-32X is a 1U high and 536mm deep chassis based on Broadcom switching silicon. The physical layer consists of 32 ports of 400G QSFP DD. The chassis has a nominal operating temperature range of 0 to +45 Degree C.

The following are key features of the product:

- Redundant and hot-swappable PS (1+1)
- Redundant and hot swappable fans (5+1)
- 1U Rack mountable
- 32x400G QSFP-DD ports
- CPU module
  - CPU: Freescale T2080
  - DDR SDRAM: DDR SDRAM: 8GB x 2 with ECC (DDR3 SO-DIMM)
  - NAND Flash memory : 128MB
  - mSATA: 32GB MLC (Reserve)
- m.2: 128GB MLC Internal USB port (5V/1A)
- Environmental 0 to +45 degree C operation

1.1. Reference Documents

Broadcom BCM56980 Data Sheet

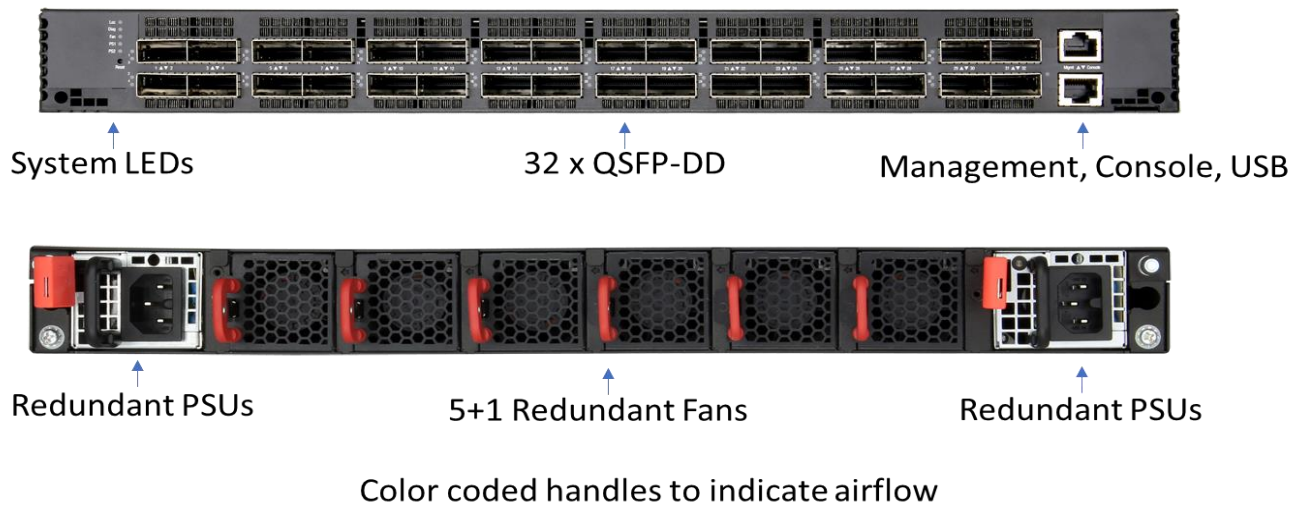
1.2. Acronyms and Terminology

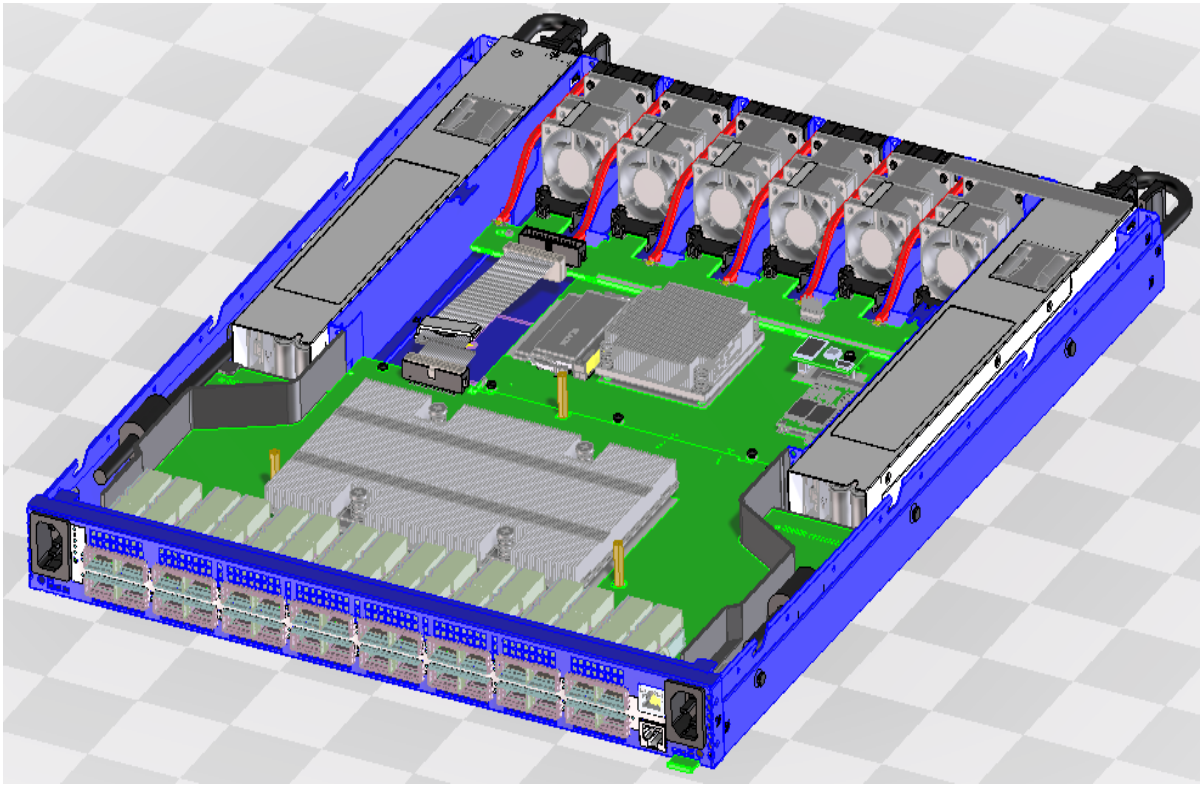
POR	Power On Configuration
PSU	Power Supply Unit

2. Hardware Architecture

2.1. Overview

The AS7900-32X provides 32x 400G QSFP-DD ports, one 1Gb port for management and control, one serial console port, and one USB port.





AS7900-32X	
CPU sub-system	CPU: Freescale T2080 1.8G DDRIII SDRAM: 8GB x 2 1600MHz with ECC (SO-DIMM) DDR3L NOR Flash (Boot): 128MB m.2: 128GB MLC and up to 512GB.
Management	UART RS232 console port RJ45,Out-band Management Ethernet port RJ45
MAC	BROADCOM BCM56980, 12.8T /256-SerDes
Ethernet Ports	32 x QSFP-DD ,
PCB	8-Layers, TU-872 for CPU module 24-Layers, TU-933+ for Mainboard 4-Layers, FR4,Tg 150 for FAN board
Power Supply	1300W PSU back to front airflow, front to back airflow, AC and DC inputs 1+1 redundant load-sharing, hot-swappable
Cooling	6 fan-tray modules with 6 pcs of 40mm x40mm x 56mm 12V fans, hot-swappable
Dimension	536 mm (L: Depth) x 438.4mm (W: Width) x 43.5 mm (H: Height maximum)

Table 2-1 System Overview

2.2. Block Diagram

The AS7900-32X provides 32x400G Ports on the board and supports 1 x 1G ports for management and control. It is formed by BCM56980, 12.8T switch controller. The host system includes two banks of 8GBDDR3SO-DIMM, 128MB Flash, watchdog timer, thermal detector and other glue logic.

The Base unit uses 12VDC and 5VDC from the Hot Swap Power module. The on-board DC/DC is used to generate 5V/3.3V/ 1.8V/1.2V/ 0.9V/ 0.8V from 12VDC

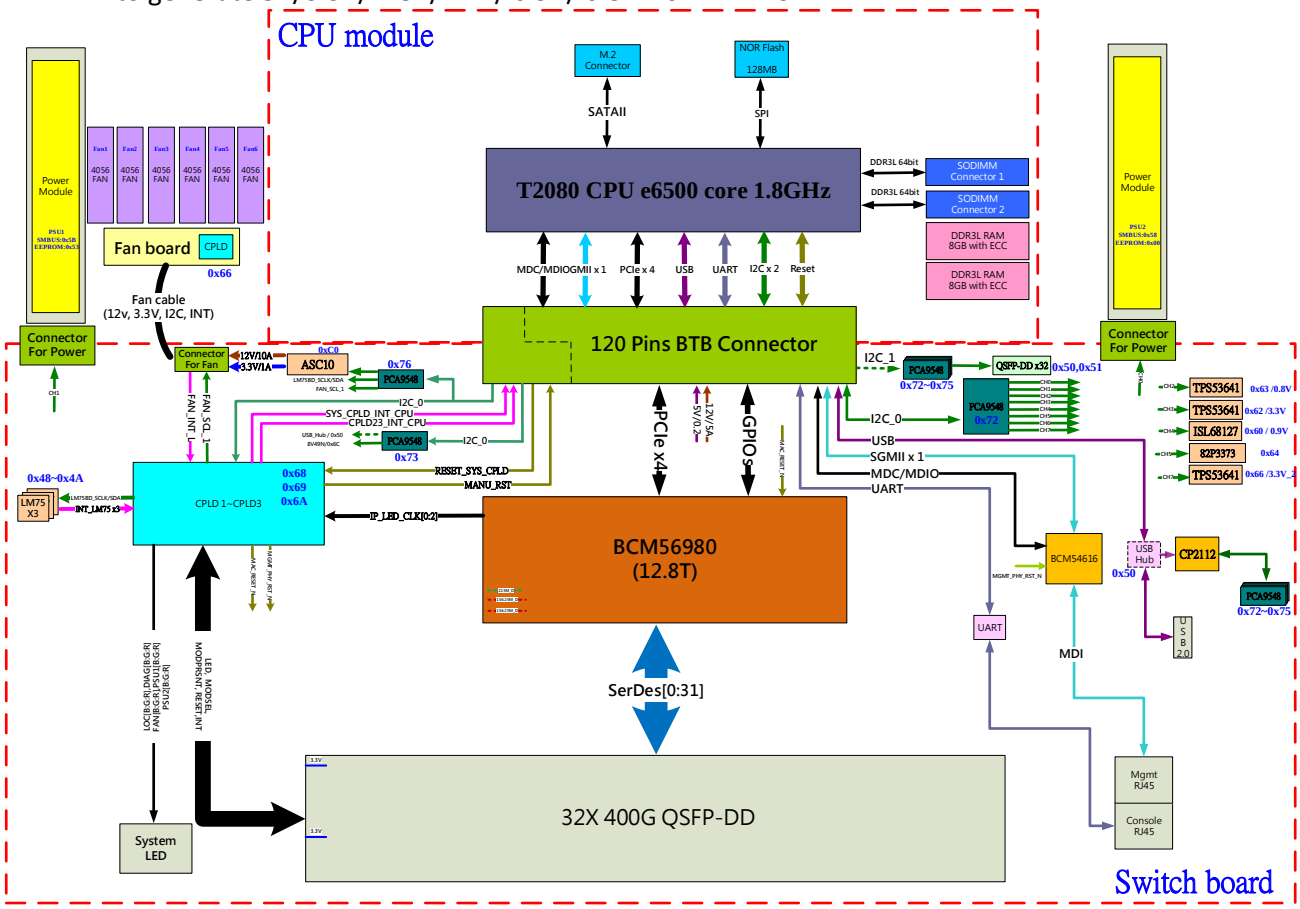


Figure 2-1 Block Diagram

2.2.1. Clock Tree

This Clock Generator is IDT 8V49NS0412NLGI8, It's input reference Clock is 25MHZ, It can generate differentia signals, like 25MHz x1 ,156.25MHz x 9 . Use 1x4 25MHz Clock buffer sourced from IDT 8V49N to BCM56980.

BCM56980 PCIE 100MHz and Core 50MHz used from 5P49V5901B558NLGI8 Clock Generator.

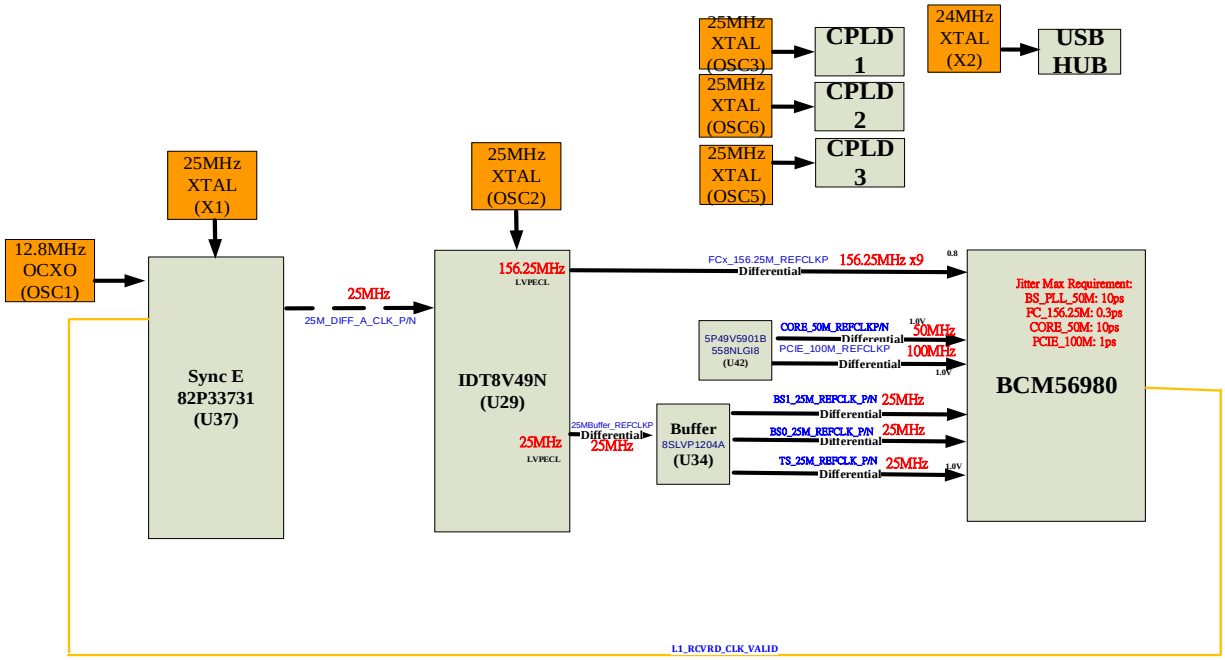


Figure 2-2 Switch board clock Tree

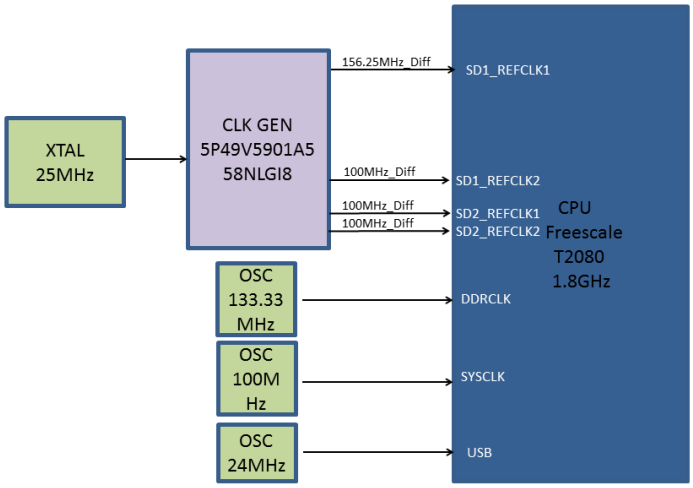


Figure 2-3 CPU board clock Tree

2.2.2. Power Tree

The power supply produces 12V output and standby 5V output, but the system only uses 12V output to convert other low system voltage.

The DC/DC is also shut down when the temperature is higher than the shutdown threshold of the thermal sensors.

The system power sequence is starting from high voltage to low voltage.

The following is the power tree topology.

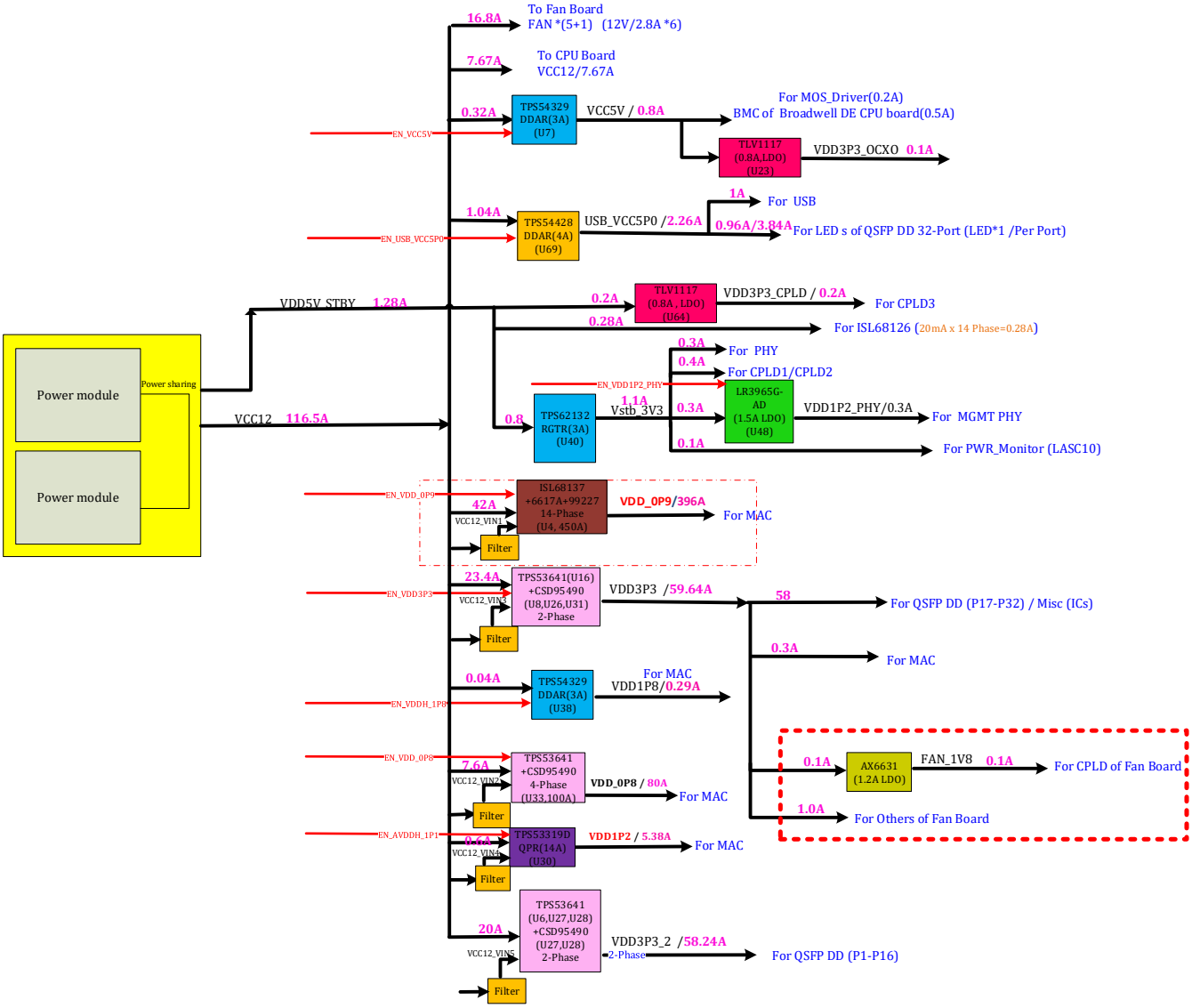


Figure 2-4 Switch board Power Tree

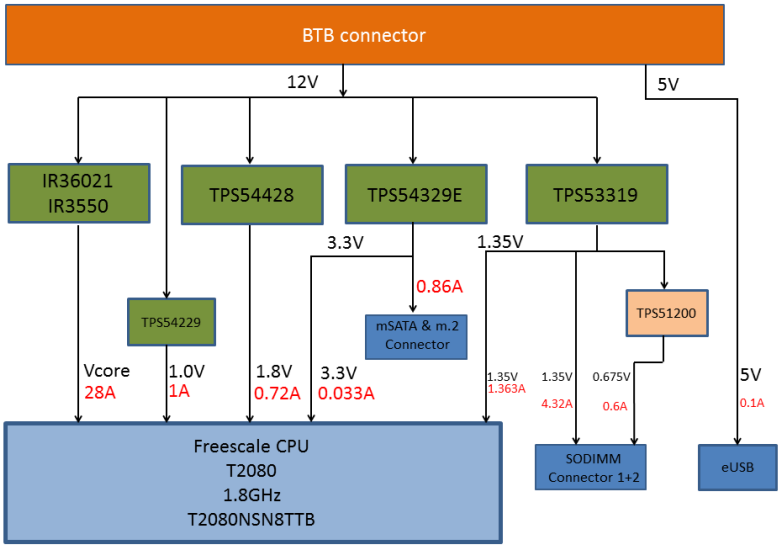


Figure 2-5 CPU board Power Tree

2.2.3. Reset Tree

The reset system is described below.

1. The CPU board and switch board will be power on. And the reset monitor IC will check DC power voltage if reach the threshold.
2. The monitor IC will send Power_RST signal to CPLD if all power is OK.
3. CPLD pass the MANU_RST signal to CPU board, and hold the all reset signals of switch board's device
4. CPU get the switch board's MANU_RST signal from switch board's CPLD, it means switch is ready to boot up. CPU board will check itself status and pull up Reset_SYS_CPLD signal to switch's CPLD to boot up switch board.
5. When switch's CPLD get the Reset_SYS_CPLD signal, switch's CPLD will pass to all device on switch to boot up device.
6. When the system running, the switch's CPLD has different register for every device's rest signal. CPU can reset switch's device separately via switch's CPLD register.

If CPU wants to reset itself without main board system, CPU can set "1" in "reset_lock" register of main board's CPLD1 (0x0B).Main board CPLD1 will block "reset_sys_cpld" signal to CPLD1, and main board CPLD1 will send "reset_lock" signal to CPU to indicate the "reset_lock" register status. The default value of "reset_lock" register is "0".

The following is the reset tree topology.

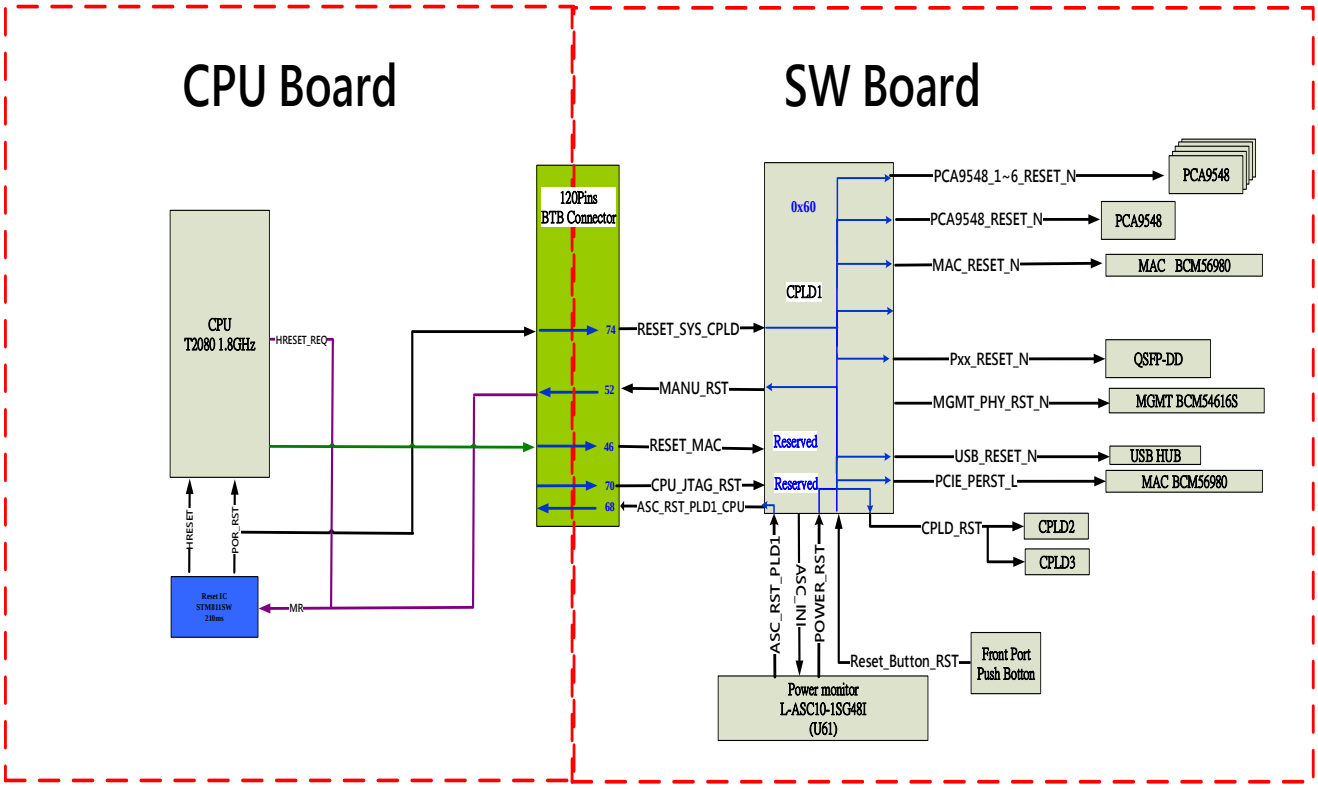


Figure 2-6 Main Board Reset Tree

2.3. LED Indicator

The system has 5 status LEDs and port LEDs. The 5 status LEDs are for PWR1, PWR2, Diag ,Fan, and LOC. The 32-Port LEDs are for 32 Ports QSFP-DD .

The 5 system LED is on left side.

The port numbering scheme on the front panel is starting from 1 to 32, even on Bottom, odd on Top, left to right.

2.3.1. System LED

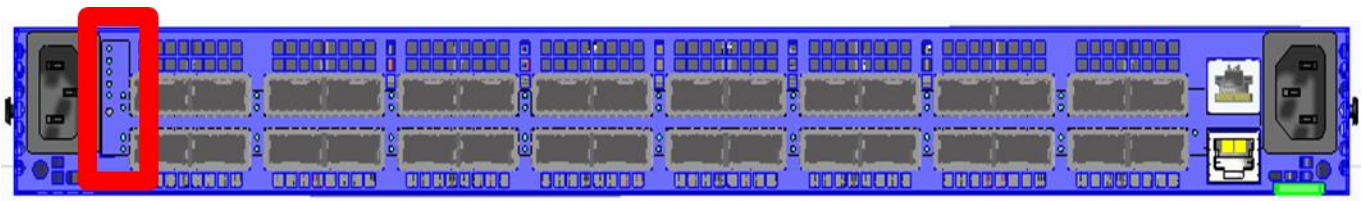


Figure 2-7 System LED

LABEL	COLOR	DESCRIPTION
PS1 (Power Supply Status)	Green	This power is operating normally.
	Amber	PWR present but not power on or this power is fault.
	Off	Power supply not present.
PS2 (Power Supply Status)	Green	This power is operating normally.
	Amber	PWR present but not power on or this power is fault.
	Off	Power supply not present.
Diag (Diagnostic)	Green	System self-diagnostic test successfully completed.
	Amber	System self-diagnostic test has detected a fault. (Fan, thermal or any interface fault.)
FAN	Green	System FAN operating normally.
	Amber	Fan tray present buy system FAN is fault.
	OFF	System OFF
LOC	Amber Flashing	Flashing by remote management command. Assists the technician in finding the right device for service in the rack.
	OFF	Not a particular switch that technician need to find

Table 2-2 System LED Definition

2.3.2. Port LED

There are 32 RGB LEDs for 32 ports and each port is with 1 RGB LED. Each port has 8 lanes, so 1 RGB LED is indicates 8 Lane of each port. The QSFP-DD port can run in 400G/4x100G or 100G/4x25G breakout mode. Note: The LEDs flash to indicate activity.

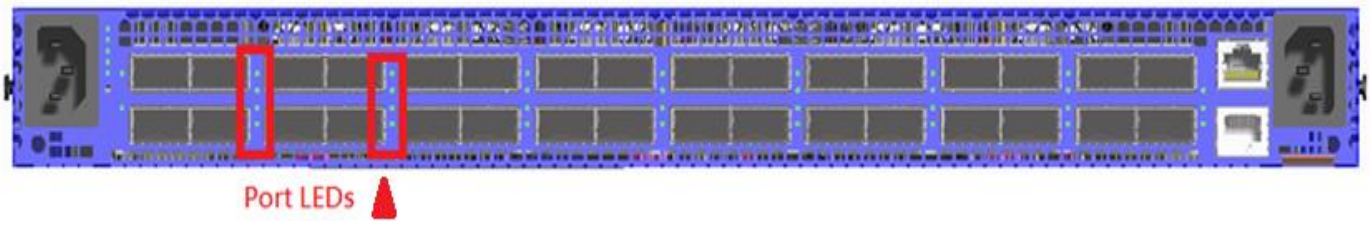


Figure 2-9 Port LED

The CPLD2 drivers: Port 1~Port16: the R/G/B LEDs and Dual Color LEDs.
The CPLD3 drivers: Port 17 ~ Port32: the R/G/B LEDs and Dual Color LEDs

LED	CONDITION	STATUS
QSFP-DD Port LED in 400G mode (Port 1 ~32)	On/Flashing Green	QSFP-DD port has a valid link at 400G. Flashing indicates activity.
	Off	There is no link on the port.
QSFP-DD Port LED in 100G mode (Port 1 ~32)	On/Flashing Blue	QSFP-DD port has a valid link at 100G. Flashing indicates activity.
	Off	There is no link on the port.
QSFP-DD Port LED in 40G (Port 1 ~32)	On/Flashing Amber	QSFP-DD port has a valid link at 40G. Flashing indicates activity.
	Off	There is no link on the port.
QSFP-DD Port LED in 25G (Port 1 ~32)	On/Flashing White	QSFP-DD port has a valid link at 25 Flashing indicates activity.
	Off	There is no link on the port.
QSFP-DD Port LED in 10G (Port 1 ~32)	On/Flashing Purple	QSFP-DD port has a valid link at 10 Flashing indicates activity.
	Off	There is no link on the port.
OOB LED (Activity)	Flashing	Flashing indicates activity
	Off	There is no link on the port

2.3.3. Management Port LED

The management port support 1G/ 100M / 10M speed.

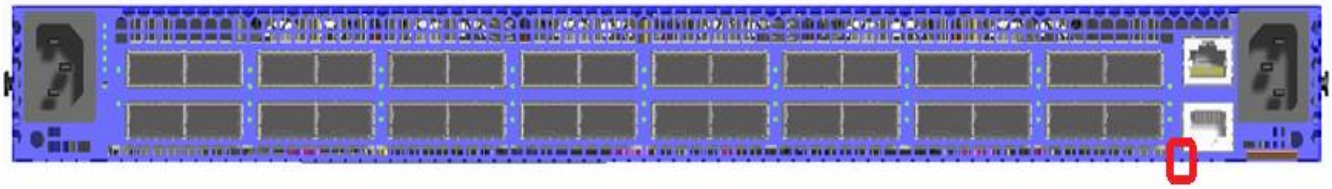


Figure 2-10 Management Port LED

LED	Color	Mode
LED	Green ON	Linked
	Green Toggle	Activity
	off	Not Present

Table 2-3 Management Port LED Definition

2.3.4. Reset Button

There has a reset button on the front panel to reboot the system.

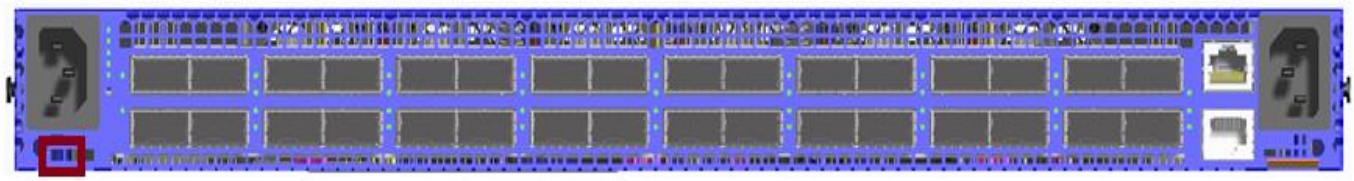


Figure 2-11 Front reset button

3. CPU Sub-system

Features:

- 4 e6500 cores built on Power Architecture® technology sharing a 2 MB L2
- 512 KB CoreNet platform cache (CPC)
- Hierarchical interconnect fabric
  - CoreNet fabric supporting coherent and non-coherent transactions with prioritization and bandwidth allocation amongst CoreNet end-points
  - Queue Manager (QMan) fabric supporting packet-level queue management and quality of service scheduling
- One 32-/64-bit DDR3 SDRAM memory controller
  - DDR3 and DDR3L with ECC and interleaving support
  - Memory pre-fetch engine
- Data Path Acceleration Architecture (DPAA) incorporating acceleration for the following functions:
  - Packet parsing, classification, and distribution (Frame Manager 1.1)
  - Queue management for scheduling, packet sequencing, and congestion management

    (Queue Manager 1.1)
  - Hardware buffer management for buffer allocation and de-allocation(Buffer Manager

    1.1)
  - Cryptography Acceleration (SEC 5.2)
  - RegEx Pattern Matching Acceleration (PME 2.1)
  - Decompression/Compression Acceleration (DCE1.0)
  - DPAA chip-to-chip interconnect via RapidIO Message Manager (RMan 1.0)
- 16 SerDes lanes at up to 10 GBaud
- 8 Ethernet interfaces, supporting combinations of:

- Up to four 10 Gbps Ethernet MACs
- Up to eight 1 Gbps Ethernet MACs
- Up to four 2.5Gbps Ethernet MACs
- IEEE Std 1588™ support

- High-speed peripheral interfaces
  - Four PCI Express controllers (two support PCIe 2.0 and two support PCIe 3.0)
  - Two Serial RapidIO 2.0 controllers running at up to 5 GBaud with Type 11 messaging and Type 9 data streaming support
- Additional peripheral interfaces
  - Two Serial ATA (SATA 2.0) controllers
  - Two high-speed USB 2.0 controllers with integrated PHY
  - Enhanced secure digital host controller (SD/MMC/eMMC)
  - Enhanced Serial peripheral interface (eSPI)
  - Four I2C controllers
  - Four 2-pin UARTs or two 4-pin UARTs
  - Integrated flash controller supporting NAND and NOR flash
- Three 8-channel DMA engines
- 896 FC-PBGA package, 25 mm x 25 mm, 0.8mm pitch

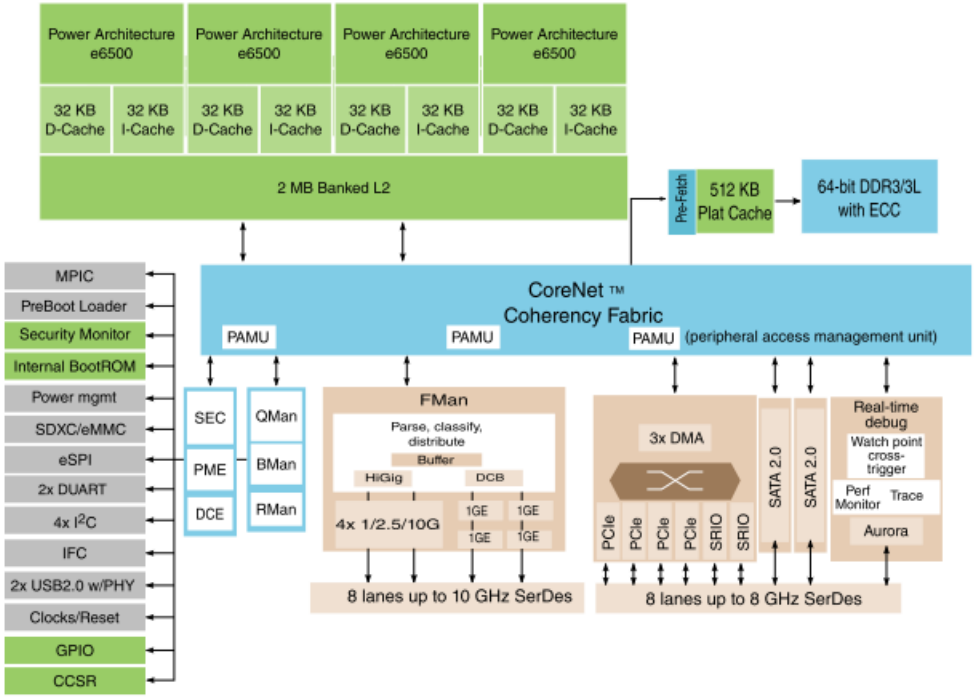


Figure 3-1 CPU all interface

T2080 Power up Sequence

The device requires that its power rails are applied in a specific sequence in order to ensure proper device operation. These Requirements are as follows for power up:

Bring up VDD, SnVDD, USB_SVDD, VDD_LP, USB_HVDD, LVDD, DVDD, CVDD, USB_OVDD, OVDD, TH_VDD, AVDD (cores, platform, DDR), G1VDD, XnVDD, and AVDD_SDn_PLLn. Drive PROG_SFP = GND.

• PORESET_B input must be driven asserted and held during this step.

Power supplies in step 1 have no ordering requirement with respect to one another except for the USB power supplies per the following note.

NOTE:

a. USB_SVDD supply must ramp before or after the USB_HVDD and USB_OVDD supplies have ramped. The supply set that ramp first must reach 90% of its final value before a supply from the other set can be ramped up.

b. USB_HVDD and USB_OVDD supplies among themselves are sequence independent.

All supplies must be at their stable values within 75 ms

3.1. Memory Space Map

Type	Base Address	Size	Actual Size	Component	Notes
System Memory Space		16GB	16GB	DDR3L SODIMM SDRAM	8GB x 2
m.2 SSD		128GB	128GB	m.2 SSD	m.2 SSD x1 (2280)
Local Bus Memory Space		128MB	128MB	Boot NOR FLASH	

Table 3-1 Memory Space Map

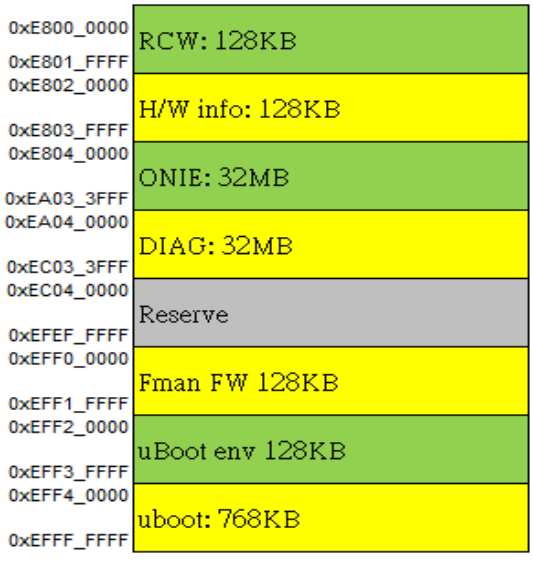


Figure 3-2 NOR Flash Memory map

3.2. CPU JATG interface

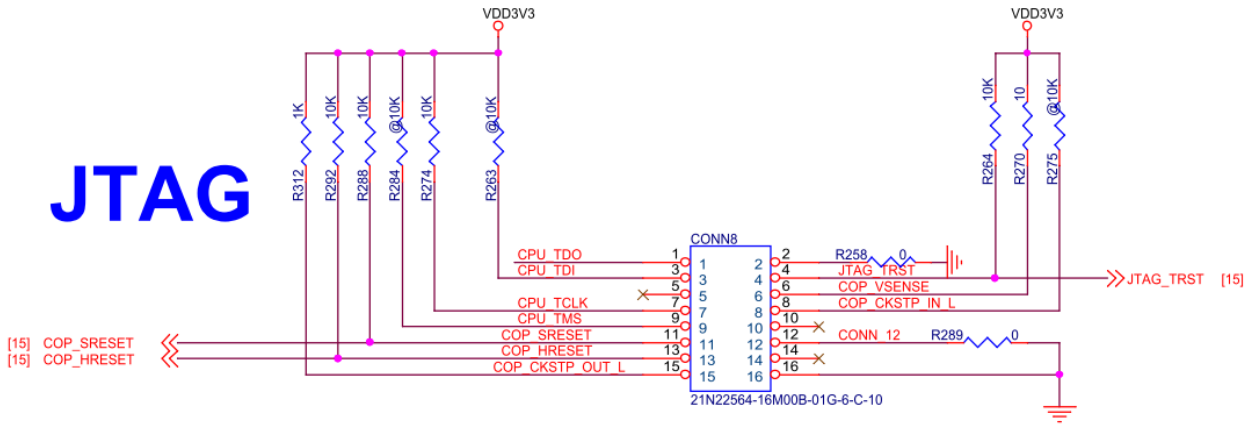


Figure 3-3 JTAG Sch

3.3. High speed peripheral interface

T2080 has high-speed peripheral interfaces which connect via 10 lanes of 5-GHz SerDes to a common crossbar switch referred to as OCeaN. High-speed I/O interface standards are supported : PCI Express (PCIe), serial RapidIO (sRIO), RMan and SATA. The T2080 integrates three PCI Express controllers and two serial RapidIO controllers plus a RapidIO message manager (RMan) and a SATA controller.

Controller	Serder lane	Interface	Notes
XFI1	SD1_TX0/RX0	XFI	BCM56930
XFI2	SD1_TX1/RX1	XFI	BCM56930
SGMII	SD1_TX2/RX2	SGMII	BCM54616S
SGMII	SD1_TX3/RX3	Reserved	
PCIe4	SD1_TX4/RX4	PCIe	BCM56930
PCIe4	SD1_TX5/RX5	PCIe	BCM56930
PCIe4	SD1_TX6/RX6	PCIe	BCM56930
PCIe4	SD1_TX7/RX7	PCIe	BCM56930
PCIe1	SD2_TX0/RX0	Reserved	
PCIe1	SD2_TX1/RX1	Reserved	
PCIe1	SD2_TX2/RX2	Reserved	
PCIe1	SD2_TX3/RX3	Reserved	
PCIe2	SD2_TX4/RX4	PCIe	FPGA
PCIe2	SD2_TX5/RX5	Reserved	
SATA1	SD2_TX6/RX6	SATA	mSATA form factor
SATA2	SD2_TX7/RX7	SATA	m.2 form factor

Table 3-2 High Speed MAPPING TABLE

- Serder lane : SD2_TX4/RX4 only for AS7760/AS7762
- Serder lane : SD2_TX6/RX6 only support for AS7760 CPU
- Serder lane : SD2_TX7/RX7
  - For AS7760 CPU, only support m.2 2240
  - For AS7762/7772 CPU, it can support m.2 2240 and m.2 2280.

3.4. GPIO

Pin Number	Pin Name	Function Description
U25.E19	GPIO1.9	Not used
U25.C18	GPIO1.10	Not used
U25.D21	GPIO1.11	Not used
U25.G19	GPIO1.12	Not used
U25.A11	GPIO1.13 - ASLEEP	For ASLEEP use
U25.A20	GPIO1.14	Not used
U25.J1	GPIO1.15 - UART1_TXD_R	For UART1_SOUT
U25.K3	GPIO1.16 - UART2_TXD_R	For UART2_SOUT
U25.J3	GPIO1.17 - UART1_RXD	For UART1_SIN
U25.F2	GPIO1.18 - UART2_RXD	For UART2_SIN
U25.G1	GPIO1.19 - UART1_RTS_R	For UART1_RTS_B
U25.J4	GPIO1.20 - TPMSTB_N	For TPM module used
U25.L4	GPIO1.21 - UART1_CTS	For UART1_CTS_B
U25.F1	GPIO1.22 - PP_N	For TPM module used
U25.C10	GPIO1.23 - CPLD1_INT_to_cpu	For CPLD Interrupt used (IRQ3)
U25.H12	GPIO1.24 - CPLD2_INT_to_cpu	For CPLD Interrupt used (IRQ4)
U25.D11	GPIO1.25 - VCORE_SM_Alert_to_cpu	For DC/DC IR36021 Interrupt used (IRQ5)
U25.P5	GPIO1.26 - TPMIRQ_to_CPU	For TPM module Interrupt used (IRQ6)
U25.P3	GPIO1.27 - LM75BD_INT_to_CPU	For LM75 (0x4B) Interrupt used (IRQ7)
U25.P6	GPIO1.28 - MAC_INT_L_to_CPU	For Mainboard Interrupt used (IRQ8)
U25.P4	GPIO1.29	Not used
U25.J5	GPIO1.30	Not used
U25.D1	GPIO1.31	Not used
U25.E3	GPIO2.0 - GPIO2_00	For CPLD upgrade used.
U25.K6	GPIO2.1 - GPIO2_01	For CPLD upgrade used.
U25.H5	GPIO2.2 - GPIO2_02	For CPLD upgrade used.
U25.L6	GPIO2.3 - GPIO2_03	For CPLD upgrade used.

U25.A3	GPIO2.4 - SD_CMD	For SD card used
U25.D2	GPIO2.5 - SD_DATA0	For SD card used
U25.D3	GPIO2.6 - SD_DATA1	For SD card used
U25.H6	GPIO2.7 - SD_DATA2	For SD card used
U25.G5	GPIO2.8 - SD_DATA3	For SD card used
U25.C4	GPIO2.9 - SD_CLK_R	For SD card used
U25.F17	GPIO2.10 - FC_CS1_N	Not used and pull high.
U25.D19	GPIO2.11 - FC_CS2_N	Not used and pull high.
U25.B17	GPIO2.12	Not used
U25.F18	GPIO2.13	Not used
U25.A17	GPIO2.14	Not used
U25.F19	GPIO2.15 - IFC_PERR_N	Not used and pull high.
U25.E17	GPIO2.25 - CPU_LAD25	For IFC NOR Flash used
U25.D16	GPIO2.26 - CPU_LAD26	For IFC NOR Flash used
U25.G17	GPIO2.27 - CPU_LAD27	For IFC NOR Flash used
U25.F16	GPIO2.28 - CPU_LAD28	For IFC NOR Flash used
U25.G16	GPIO2.29 – CPU_LAD29	For IFC NOR Flash used
U25.B21	GPIO2.30 - CPU_LAD30	For IFC NOR Flash used
U25.E16	GPIO2.31 - CPU_LAD31	Not used
U25.T3	GPIO3.0	Not used
U25.V4	GPIO3.1	Not used
U25.V2	GPIO3.2	Not used
U25.U1	GPIO3.3	Not used
U25.W5	GPIO3.4	Not used
U25.V3	GPIO3.5	Not used
U25.W2	GPIO3.6	Not used
U25.W1	GPIO3.7	Not used
U25.R4	GPIO3.11	Not used
U25.N2	GPIO3.12	Not used
U25.N1	GPIO3.13	Not used
U25.T6	GPIO3.14	Not used
U25.M3	GPIO3.15	Not used
U25.P1	GPIO3.16	Not used
U25.M2	GPIO3.17	Not used

U25.L1	GPIO3.18	Not used
U25.N6	GPIO3.19	Not used
U25.N5	GPIO3.20	Not used
U25.R5	GPIO3.21	Not used
U25.L3	GPIO3.22	Not used
U25.M4	GPIO3.23	Not used
U25.V5	GPIO3.24	Not used
U25.U3	GPIO3.25	Not used
U25.U5	GPIO3.26	Not used
U25.W6	GPIO3.27	Not used
U25.R2	GPIO3.28	Not used
U25.U4	GPIO3.29	Not used
U25.T2	GPIO3.30	Not used
U25.R1	GPIO3.31	Not used
U25.J6	GPIO4.0 - CPU_I2C3_SCL	For I2C used
U25.J2	GPIO4.1 - CPU_I2C3_SDA	For I2C used
U25.K1	GPIO4.2 - CPU_I2C4_SCL	For I2C used
U25.M1	GPIO4.3 - CPU_I2C4_SDA	For I2C used
U25.L5	GPIO4.4 - DMA1_DREQ0	Not used
U25.E1	GPIO4.5 - CPU_JTAG_RST	For Mainboard GPIO application
U25.K5	GPIO4.6 - UCD9090_ALERT_L	For Mainboard GPIO application
U25.F3	GPIO4.7 - DMA2_DREQ0	Not used
U25.H1	GPIO4.8 - 1PPS_CPU_to_CPU	For Mainboard 1588 function used
U25.G3	GPIO4.9 - RESET_MAC_to_CPU	For Mainboard GPIO application
U25.E4	GPIO4.24 - SD_CD	For SD Card used
U25.F4	GPIO4.25 - SD_WP	For SD Card used
U25.T1	GPIO4.28	Not used
U25.R3	GPIO4.29	Not used

Table 3-3 GPIO MAPPING TABLE

4. Switch Sub-system

The AS7900-32X utilizes the Broadcom BCM56980 Tomahawk III which supports 32 ports of 400G. The BCM56980 Interfaces to the CPU through PCIe interfaces used to transfer any packet to or from CPU. The PCI interface is configured as PCIe Gen2 x 4 lanes.

4.1. Configurations of MAC (BCM56980)

Pin Number	Pin Name	Function Description
U23	MHOST0_BOOT_DEV	1= Boot from EEPROM

4.1.1. POR of MAC (BCM56980)

HW reset must remain asserted for at least 80ms after all supplies are UP Power-Up

1. 3.3V supply ramp-up rate must be slower than 1V/200us → 660us min,(10ms max).
2. Ramp-up rate for all other supplies must be slower than 1V/50us →@0.8V 40us min,@0.9V 45us min,@1.2V 60us min.
3. Power-up delay of VDD Core from VDDO3P3 : 0ms min.
4. Power-up delay of VDD0P8 ,VDD1P2,VDD1P8 from VDD Core : 0ms min.
5. All supplies must reach their final stable voltage levels within 10ms. and stable.

Power-Down

• When the device is powered DOWN, the core voltage, VDDC, must ramp down to <0.1V and maintain this level for at least 20ms,
Before being powered back ON.

4.2. Port Mapping

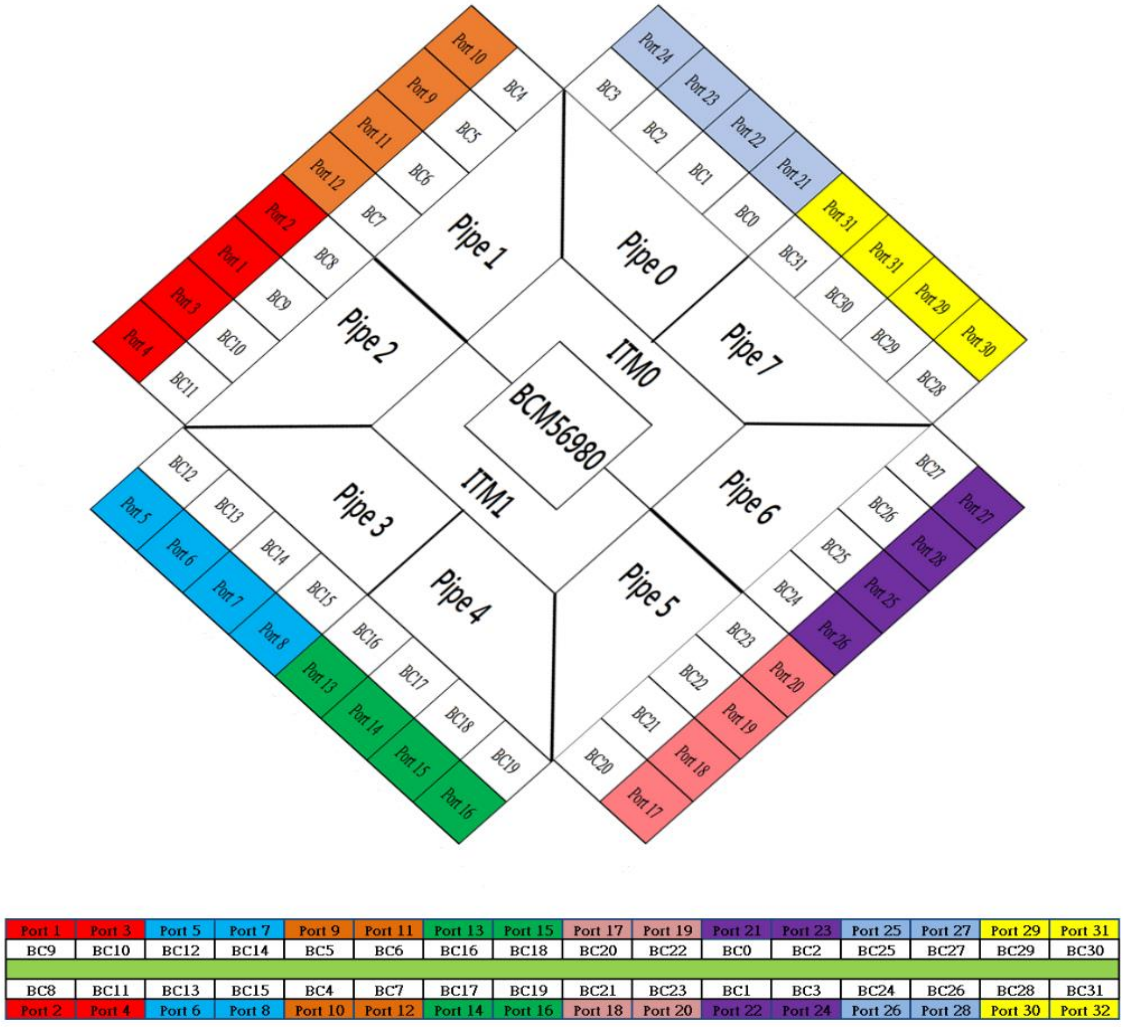


Figure 4-1 Physical Port mapping

PIN NAME	NET NAME	QSFP-DD Port	QSFP-DD_CHANNEL	Swapping Details	QSFP-DD connector
BC9_TD3N	P1_ISG30_TX0_N	QSFP-DD1	TX4_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN12
BC9_TD3P	P1_ISG30_TX0_P		TX4_N		
BC9_TD0P	P1_ISG30_TX1_N		TX8_P		
BC9_TD0N	P1_ISG30_TX1_P		TX8_N		
BC9_TD1P	P1_ISG30_TX2_N		TX3_P		
BC9_TD1N	P1_ISG30_TX2_P		TX3_N		
BC9_TD5P	P1_ISG30_TX3_N		TX1_P		
BC9_TD5N	P1_ISG30_TX3_P		TX1_N		

BC9_TD4N	P1_ISG30_TX4_N		TX7_P		
BC9_TD4P	P1_ISG30_TX4_P		TX7_N		
BC9_TD7P	P1_ISG30_TX5_N		TX5_P		
BC9_TD7N	P1_ISG30_TX5_P		TX5_N		
BC9_TD2P	P1_ISG30_TX6_N		TX6_P		
BC9_TD2N	P1_ISG30_TX6_P		TX6_N		
BC9_TD6P	P1_ISG30_TX7_N		TX2_P		
BC9_TD6N	P1_ISG30_TX7_P		TX2_N		
BC9_RD0N	P1_ISG30_RX0_N		RX5_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC9_RD0P	P1_ISG30_RX0_P		RX5_N		
BC9_RD4P	P1_ISG30_RX1_N		RX2_P		
BC9_RD4N	P1_ISG30_RX1_P		RX2_N		
BC9_RD5P	P1_ISG30_RX2_N		RX6_P		
BC9_RD5N	P1_ISG30_RX2_P		RX6_N		
BC9_RD1P	P1_ISG30_RX3_N		RX4_P		
BC9_RD1N	P1_ISG30_RX3_P		RX4_N		
BC9_RD6N	P1_ISG30_RX4_N		RX3_P		
BC9_RD6P	P1_ISG30_RX4_P		RX3_N		
BC9_RD3N	P1_ISG30_RX5_N		RX1_P		
BC9_RD3P	P1_ISG30_RX5_P		RX1_N		
BC9_RD2N	P1_ISG30_RX6_N		RX8_P		
BC9_RD2P	P1_ISG30_RX6_P		RX8_N		
BC9_RD7P	P1_ISG30_RX7_N		RX7_P		
BC9_RD7N	P1_ISG30_RX7_P		RX7_N		
BC8_TD6P	P2_ISG31_TX0_N		TX6_P		
BC8_TD6N	P2_ISG31_TX0_P		TX6_N		
BC8_TD7N	P2_ISG31_TX1_N		TX5_P		
BC8_TD7P	P2_ISG31_TX1_P		TX5_N		
BC8_TD4P	P2_ISG31_TX2_N		TX1_P		
BC8_TD4N	P2_ISG31_TX2_P	QSFP-DD2	TX1_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN31
BC8_TD5N	P2_ISG31_TX3_N		TX3_P		
BC8_TD5P	P2_ISG31_TX3_P		TX3_N		
BC8_TD2N	P2_ISG31_TX4_N		TX7_P		
BC8_TD2P	P2_ISG31_TX4_P		TX7_N		
BC8_TD1P	P2_ISG31_TX5_N		TX8_P		

BC8_TD1N	P2_ISG31_TX5_P		TX8_N		
BC8_TD0N	P2_ISG31_TX6_N		TX2_P		
BC8_TD0P	P2_ISG31_TX6_P		TX2_N		
BC8_TD3P	P2_ISG31_TX7_N		TX4_P		
BC8_TD3N	P2_ISG31_TX7_P		TX4_N		
BC8_RD4P	P2_ISG31_RX0_N		RX4_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC8_RD4N	P2_ISG31_RX0_P		RX4_N		
BC8_RD7P	P2_ISG31_RX1_N		RX3_P		
BC8_RD7N	P2_ISG31_RX1_P		RX3_N		
BC8_RD5P	P2_ISG31_RX2_N		RX8_P		
BC8_RD5N	P2_ISG31_RX2_P		RX8_N		
BC8_RD6N	P2_ISG31_RX3_N		RX7_P		
BC8_RD6P	P2_ISG31_RX3_P		RX7_N		
BC8_RD3P	P2_ISG31_RX4_N		RX1_P		
BC8_RD3N	P2_ISG31_RX4_P		RX1_N		
BC8_RD2N	P2_ISG31_RX5_N		RX5_P		
BC8_RD2P	P2_ISG31_RX5_P		RX5_N		
BC8_RD1N	P2_ISG31_RX6_N		RX2_P		
BC8_RD1P	P2_ISG31_RX6_P		RX2_N		
BC8_RD0N	P2_ISG31_RX7_N		RX6_P		
BC8_RD0P	P2_ISG31_RX7_P		RX6_N		
BC10_TD6N	P3_ISG28_TX0_N	QSFP-DD3	TX4_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN22
BC10_TD6P	P3_ISG28_TX0_P		TX4_N		
BC10_TD0P	P3_ISG28_TX1_N		TX2_P		
BC10_TD0N	P3_ISG28_TX1_P		TX2_N		
BC10_TD3P	P3_ISG28_TX2_N		TX8_P		
BC10_TD3N	P3_ISG28_TX2_P		TX8_N		
BC10_TD7P	P3_ISG28_TX3_N		TX7_P		
BC10_TD7N	P3_ISG28_TX3_P		TX7_N		
BC10_TD1N	P3_ISG28_TX4_N		TX5_P		
BC10_TD1P	P3_ISG28_TX4_P		TX5_N		
BC10_TD5P	P3_ISG28_TX5_N		TX3_P		
BC10_TD5N	P3_ISG28_TX5_P		TX3_N		
BC10_TD4N	P3_ISG28_TX6_N		TX1_P		
BC10_TD4P	P3_ISG28_TX6_P		TX1_N		

BC10_TD2P	P3_ISG28_TX7_N		TX6_P		
BC10_TD2N	P3_ISG28_TX7_P		TX6_N		
BC10_RD7N	P3_ISG28_RX0_N		RX1_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC10_RD7P	P3_ISG28_RX0_P		RX1_N		
BC10_RD4N	P3_ISG28_RX1_N		RX8_P		
BC10_RD4P	P3_ISG28_RX1_P		RX8_N		
BC10_RD2P	P3_ISG28_RX2_N		RX6_P		
BC10_RD2N	P3_ISG28_RX2_P		RX6_N		
BC10_RD5P	P3_ISG28_RX3_N		RX2_P		
BC10_RD5N	P3_ISG28_RX3_P		RX2_N		
BC10_RD0P	P3_ISG28_RX4_N		RX7_P		
BC10_RD0N	P3_ISG28_RX4_P		RX7_N		
BC10_RD6P	P3_ISG28_RX5_N		RX5_P		
BC10_RD6N	P3_ISG28_RX5_P		RX5_N		
BC10_RD1P	P3_ISG28_RX6_N		RX6_P		
BC10_RD1N	P3_ISG28_RX6_P		RX6_N		
BC10_RD3N	P3_ISG28_RX7_N		RX3_P		
BC10_RD3P	P3_ISG28_RX7_P		RX3_N		
BC11_TD2P	P4_ISG29_TX0_N	QSFP-DD4	TX4_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN41
BC11_TD2N	P4_ISG29_TX0_P		TX4_N		
BC11_TD3N	P4_ISG29_TX1_N		TX2_P		
BC11_TD3P	P4_ISG29_TX1_P		TX2_N		
BC11_TD0P	P4_ISG29_TX2_N		TX6_P		
BC11_TD0N	P4_ISG29_TX2_P		TX6_N		
BC11_TD1N	P4_ISG29_TX3_N		TX5_P		
BC11_TD1P	P4_ISG29_TX3_P		TX5_N		
BC11_TD5P	P4_ISG29_TX4_N		TX1_P		
BC11_TD5N	P4_ISG29_TX4_P		TX1_N		
BC11_TD7P	P4_ISG29_TX5_N		TX3_P		
BC11_TD7N	P4_ISG29_TX5_P		TX3_N		
BC11_TD4N	P4_ISG29_TX6_N		TX7_P		
BC11_TD4P	P4_ISG29_TX6_P		TX7_N		
BC11_TD6N	P4_ISG29_TX7_N		TX8_P		
BC11_TD6P	P4_ISG29_TX7_P		TX8_N		
BC11_RD3P	P4_ISG29_RX0_N		RX3_P	QSFP-DD CHANNELS	
BC11_RD3N	P4_ISG29_RX0_P		RX3_N		

BC11_RD7P	P4_ISG29_RX1_N		RX2_P	SWAPPED WITH IN THE QUAD	
BC11_RD7N	P4_ISG29_RX1_P		RX2_N		
BC11_RD1P	P4_ISG29_RX2_N		RX5_P		
BC11_RD1N	P4_ISG29_RX2_P		RX5_N		
BC11_RD2N	P4_ISG29_RX3_N		RX7_P		
BC11_RD3P	P4_ISG29_RX3_P		RX7_N		
BC11_RD6N	P4_ISG29_RX4_N		RX1_P		
BC11_RD6P	P4_ISG29_RX4_P		RX1_N		
BC11_RD4N	P4_ISG29_RX5_N		RX4_P		
BC11_RD4P	P4_ISG29_RX5_P		RX4_N		
BC11_RD0N	P4_ISG29_RX6_N		RX8_P		
BC11_RD0P	P4_ISG29_RX6_P		RX8_N		
BC11_RD5N	P4_ISG29_RX7_N		RX6_P		
BC11_RD5P	P4_ISG29_RX7_P		RX6_N		
BC12_TD6N	P5_ISG27_TX0_N	QSFP-DD5	TX4_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN13
BC12_TD6P	P5_ISG27_TX0_P		TX4_N		
BC12_TD5N	P5_ISG27_TX1_N		TX7_P		
BC12_TD5P	P5_ISG27_TX1_P		TX7_N		
BC12_TD0P	P5_ISG27_TX2_N		TX8_P		
BC12_TD0N	P5_ISG27_TX2_P		TX8_N		
BC12_TD1P	P5_ISG27_TX3_N		TX3_P		
BC12_TD1N	P5_ISG27_TX3_P		TX3_N		
BC12_TD2N	P5_ISG27_TX4_N		TX5_P		
BC12_TD2P	P5_ISG27_TX4_P		TX5_N		
BC12_TD7N	P5_ISG27_TX5_N		TX6_P		
BC12_TD7P	P5_ISG27_TX5_P		TX6_N		
BC12_TD4N	P5_ISG27_TX6_N		TX1_P		
BC12_TD4P	P5_ISG27_TX6_P		TX1_N		
BC12_TD3P	P5_ISG27_TX7_N		TX2_P		
BC12_TD3N	P5_ISG27_TX7_P		TX2_N		
BC12_RD3P	P5_ISG27_RX0_N		RX2_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC12_RD3N	P5_ISG27_RX0_P		RX2_N		
BC12_RD5N	P5_ISG27_RX1_N		RX8_P		
BC12_RD5P	P5_ISG27_RX1_P		RX8_N		
BC12_RD7N	P5_ISG27_RX2_N		RX5_P		
BC12_RD7P	P5_ISG27_RX2_P		RX5_N		

BC12_RD2N	P5_ISG27_RX3_N		RX6_P		
BC12_RD2P	P5_ISG27_RX3_P		RX6_N		
BC12_RD4P	P5_ISG27_RX4_N		RX1_P		
BC12_RD4N	P5_ISG27_RX4_P		RX1_N		
BC12_RD6P	P5_ISG27_RX5_N		RX4_P		
BC12_RD6N	P5_ISG27_RX5_P		RX4_N		
BC12_RD1N	P5_ISG27_RX6_N		RX7_P		
BC12_RD1P	P5_ISG27_RX6_P		RX7_N		
BC12_RD0N	P5_ISG27_RX7_N		RX3_P		
BC12_RD0P	P5_ISG27_RX7_P		RX3_N		
BC13_TD3P	P6_ISG26_TX0_N		TX5_P		
BC13_TD3N	P6_ISG26_TX0_P		TX5_N		
BC13_TD2P	P6_ISG26_TX1_N		TX6_P		
BC13_TD2N	P6_ISG26_TX1_P		TX6_N		
BC13_TD0N	P6_ISG26_TX2_N		TX1_P		
BC13_TD0P	P6_ISG26_TX2_P		TX1_N		
BC13_TD1P	P6_ISG26_TX3_N		TX3_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC13_TD1N	P6_ISG26_TX3_P		TX3_N		
BC13_TD4P	P6_ISG26_TX4_N		TX2_P		
BC13_TD4N	P6_ISG26_TX4_P		TX2_N		
BC13_TD5N	P6_ISG26_TX5_N		TX7_P		
BC13_TD5P	P6_ISG26_TX5_P		TX7_N		
BC13_TD7N	P6_ISG26_TX6_N	QSFP-DD6	TX8_P		CONN32
BC13_TD7P	P6_ISG26_TX6_P		TX8_N		
BC13_TD6P	P6_ISG26_TX7_N		TX4_P		
BC13_TD6N	P6_ISG26_TX7_P		TX4_N		
BC13_RD5P	P6_ISG26_RX0_N		RX3_P		
BC13_RD5N	P6_ISG26_RX0_P		RX3_N		
BC13_RD1N	P6_ISG26_RX1_N		RX6_P		
BC13_RD1P	P6_ISG26_RX1_P		RX6_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC13_RD4N	P6_ISG26_RX2_N		RX7_P		
BC13_RD4P	P6_ISG26_RX2_P		RX7_N		
BC13_RD7P	P6_ISG26_RX3_N		RX8_P		
BC13_RD7N	P6_ISG26_RX3_P		RX8_N		
BC13_RD6N	P6_ISG26_RX4_N		RX4_P		
BC13_RD6P	P6_ISG26_RX4_P		RX4_N		

BC13_RD2P	P6_ISG26_RX5_N		RX5_P		
BC13_RD2N	P6_ISG26_RX5_P		RX5_N		
BC13_RD3N	P6_ISG26_RX6_N		RX1_P		
BC13_RD3P	P6_ISG26_RX6_P		RX1_N		
BC13_RD0P	P6_ISG26_RX7_N		RX2_P		
BC13_RD0N	P6_ISG26_RX7_P		RX2_N		
BC14_TD6P	P7_ISG25_TX0_N		TX2_P		
BC14_TD6N	P7_ISG25_TX0_P		TX2_N		
BC14_TD5N	P7_ISG25_TX1_N		TX8_P		
BC14_TD5P	P7_ISG25_TX1_P		TX8_N		
BC14_TD4P	P7_ISG25_TX2_N		TX7_P		
BC14_TD4N	P7_ISG25_TX2_P		TX7_N		
BC14_TD7N	P7_ISG25_TX3_N		TX4_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC14_TD7P	P7_ISG25_TX3_P		TX4_N		
BC14_TD0N	P7_ISG25_TX4_N		TX5_P		
BC14_TD0P	P7_ISG25_TX4_P		TX5_N		
BC14_TD3P	P7_ISG25_TX5_N		TX3_P		
BC14_TD3N	P7_ISG25_TX5_P		TX3_N		
BC14_TD1N	P7_ISG25_TX6_N		TX6_P		
BC14_TD1P	P7_ISG25_TX6_P		TX6_N		
BC14_TD2N	P7_ISG25_TX7_N	QSFP-DD7	TX1_P		CONN14
BC14_TD2P	P7_ISG25_TX7_P		TX1_N		
BC14_RD6N	P7_ISG25_RX0_N		RX5_P		
BC14_RD6P	P7_ISG25_RX0_P		RX5_N		
BC14_RD3P	P7_ISG25_RX1_N		RX8_P		
BC14_RD3N	P7_ISG25_RX1_P		RX8_N		
BC14_RD7P	P7_ISG25_RX2_N		RX1_P		
BC14_RD7N	P7_ISG25_RX2_P		RX1_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC14_RD5P	P7_ISG25_RX3_N		RX2_P		
BC14_RD5N	P7_ISG25_RX3_P		RX2_N		
BC14_RD1P	P7_ISG25_RX4_N		RX4_P		
BC14_RD1N	P7_ISG25_RX4_P		RX4_N		
BC14_RD0N	P7_ISG25_RX5_N		RX3_P		
BC14_RD0P	P7_ISG25_RX5_P		RX3_N		
BC14_RD4N	P7_ISG25_RX6_N		RX6_P		
BC14_RD4P	P7_ISG25_RX6_P		RX6_N		

BC14_RD2N	P7_ISG25_RX7_N		RX7_P		
BC14_RD2P	P7_ISG25_RX7_P		RX7_N		
BC15_TD5N	P8_ISG24_TX0_N	QSFP-DD8	TX2_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN33
BC15_TD5P	P8_ISG24_TX0_P		TX2_N		
BC15_TD7N	P8_ISG24_TX1_N		TX4_P		
BC15_TD7P	P8_ISG24_TX1_P		TX4_N		
BC15_TD6P	P8_ISG24_TX2_N		TX6_P		
BC15_TD6N	P8_ISG24_TX2_P		TX6_N		
BC15_TD1P	P8_ISG24_TX3_N		TX5_P		
BC15_TD1N	P8_ISG24_TX3_P		TX5_N		
BC15_TD0N	P8_ISG24_TX4_N		TX4_P		
BC15_TD0P	P8_ISG24_TX4_P		TX4_N		
BC15_TD3P	P8_ISG24_TX5_N		TX3_P		
BC15_TD3N	P8_ISG24_TX5_P		TX3_N		
BC15_TD4P	P8_ISG24_TX6_N		TX7_P		
BC15_TD4N	P8_ISG24_TX6_P		TX7_N		
BC15_TD2P	P8_ISG24_TX7_N		TX8_P		
BC15_TD2N	P8_ISG24_TX7_P		TX8_N		
BC15_RD6P	P8_ISG24_RX0_N		RX3_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC15_RD6N	P8_ISG24_RX0_P		RX3_N		
BC15_RD2N	P8_ISG24_RX1_N		RX4_P		
BC15_RD2P	P8_ISG24_RX1_P		RX4_N		
BC15_RD5N	P8_ISG24_RX2_N		RX7_P		
BC15_RD5P	P8_ISG24_RX2_P		RX7_N		
BC15_RD4P	P8_ISG24_RX3_N		RX5_P		
BC15_RD4N	P8_ISG24_RX3_P		RX5_N		
BC15_RD7N	P8_ISG24_RX4_N		RX8_P		
BC15_RD7P	P8_ISG24_RX4_P		RX8_N		
BC15_RD1P	P8_ISG24_RX5_N		RX2_P		
BC15_RD1N	P8_ISG24_RX5_P		RX2_N		
BC15_RD0N	P8_ISG24_RX6_N		RX1_P		
BC15_RD0P	P8_ISG24_RX6_P		RX1_N		
BC15_RD3P	P8_ISG24_RX7_N		RX6_P		
BC15_RD3N	P8_ISG24_RX7_P		RX6_N		
BC5_TD5P	P9_ISG3_TX0_N	QSFP-DD9	TX3_P		CONN11

BC5_TD5N	P9_ISG3_TX0_P		TX3_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC5_TD7P	P9_ISG3_TX1_N		TX5_P		
BC5_TD7N	P9_ISG3_TX1_P		TX5_N		
BC5_TD4P	P9_ISG3_TX2_N		TX1_P		
BC5_TD4N	P9_ISG3_TX2_P		TX1_N		
BC5_TD1N	P9_ISG3_TX3_N		TX8_P		
BC5_TD1P	P9_ISG3_TX3_P		TX8_N		
BC5_TD6P	P9_ISG3_TX4_N		TX2_P		
BC5_TD6N	P9_ISG3_TX4_P		TX2_N		
BC5_TD0P	P9_ISG3_TX5_N		TX7_P		
BC5_TD0N	P9_ISG3_TX5_P		TX7_N		
BC5_TD3N	P9_ISG3_TX6_N		TX4_P		
BC5_TD3P	P9_ISG3_TX6_P		TX4_N		
BC5_TD2P	P9_ISG3_TX7_N		TX6_P		
BC5_TD2N	P9_ISG3_TX7_P		TX6_N		
BC5_RD0P	P9_ISG3_RX0_N		RX5_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC5_RD0N	P9_ISG3_RX0_P		RX5_N		
BC5_RD4P	P9_ISG3_RX1_N		RX6_P		
BC5_RD4N	P9_ISG3_RX1_P		RX6_N		
BC5_RD5N	P9_ISG3_RX2_N		RX4_P		
BC5_RD5P	P9_ISG3_RX2_P		RX4_N		
BC5_RD2N	P9_ISG3_RX3_N		RX8_P		
BC5_RD2P	P9_ISG3_RX3_P		RX8_N		
BC5_RD3P	P9_ISG3_RX4_N		RX1_P		
BC5_RD3N	P9_ISG3_RX4_P		RX1_N		
BC5_RD7N	P9_ISG3_RX5_N		RX3_P		
BC5_RD7P	P9_ISG3_RX5_P		RX3_N		
BC5_RD6P	P9_ISG3_RX6_N		RX7_P		
BC5_RD6N	P9_ISG3_RX6_P		RX7_N		
BC5_RD1P	P9_ISG3_RX7_N		RX2_P		
BC5_RD1N	P9_ISG3_RX7_P		RX2_N		
BC4_TD6P	P10_ISG2_TX0_N	QSFP-DD10	TX1_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN30
BC4_TD6N	P10_ISG2_TX0_P		TX1_N		
BC4_TD5P	P10_ISG2_TX1_N		TX5_P		
BC4_TD5N	P10_ISG2_TX1_P		TX5_N		
BC4_TD7N	P10_ISG2_TX2_N		TX3_P		

BC4_TD7P	P10_ISG2_TX2_P		TX3_N		
BC4_TD1N	P10_ISG2_TX3_N		TX7_P		
BC4_TD1P	P10_ISG2_TX3_P		TX7_N		
BC4_TD4P	P10_ISG2_TX4_N		TX6_P		
BC4_TD4N	P10_ISG2_TX4_P		TX6_N		
BC4_TD0P	P10_ISG2_TX5_N		TX8_P		
BC4_TD0N	P10_ISG2_TX5_P		TX8_N		
BC4_TD3N	P10_ISG2_TX6_N		TX2_P		
BC4_TD3P	P10_ISG2_TX6_P		TX2_N		
BC4_TD2P	P10_ISG2_TX7_N		TX4_P		
BC4_TD2N	P10_ISG2_TX7_P		TX4_N		
BC4_RD4N	P10_ISG2_RX0_N		RX8_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC4_RD4P	P10_ISG2_RX0_P		RX8_N		
BC4_RD5P	P10_ISG2_RX1_N		RX4_P		
BC4_RD5N	P10_ISG2_RX1_P		RX4_N		
BC4_RD7P	P10_ISG2_RX2_N		RX7_P		
BC4_RD7N	P10_ISG2_RX2_P		RX7_N		
BC4_RD3N	P10_ISG2_RX3_N		RX3_P		
BC4_RD3P	P10_ISG2_RX3_P		RX3_N		
BC4_RD6N	P10_ISG2_RX4_N		RX2_P		
BC4_RD6P	P10_ISG2_RX4_P		RX2_N		
BC4_RD2P	P10_ISG2_RX5_N		RX6_P		
BC4_RD2N	P10_ISG2_RX5_P		RX6_N		
BC4_RD1N	P10_ISG2_RX6_N		RX1_P		
BC4_RD1P	P10_ISG2_RX6_P		RX1_N		
BC4_RD0N	P10_ISG2_RX7_N		RX5_P		
BC4_RD0P	P10_ISG2_RX7_P		RX5_N		
BC6_TD0N	P11_ISG1_TX0_N		TX4_P		
BC6_TD0P	P11_ISG1_TX0_P		TX4_N		
BC6_TD5N	P11_ISG1_TX1_N		TX8_P		
BC6_TD5P	P11_ISG1_TX1_P		TX8_N		
BC6_TD1P	P11_ISG1_TX2_N	QSFP-DD11	TX7_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN23
BC6_TD1N	P11_ISG1_TX2_P		TX7_N		
BC6_TD6P	P11_ISG1_TX3_N		TX2_P		
BC6_TD6N	P11_ISG1_TX3_P		TX2_N		
BC6_TD7N	P11_ISG1_TX4_N		TX3_P		

BC6_TD7P	P11_ISG1_TX4_P		TX3_N		
BC6_TD4P	P11_ISG1_TX5_N		TX1_P		
BC6_TD4N	P11_ISG1_TX5_P		TX1_N		
BC6_TD2P	P11_ISG1_TX6_N		TX6_P		
BC6_TD2N	P11_ISG1_TX6_P		TX6_N		
BC6_TD3P	P11_ISG1_TX7_N		TX5_P		
BC6_TD3N	P11_ISG1_TX7_P		TX5_N		
BC6_RD7P	P11_ISG1_RX0_N		RX5_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC6_RD7N	P11_ISG1_RX0_P		RX5_N		
BC6_RD2P	P11_ISG1_RX1_N		RX7_P		
BC6_RD2N	P11_ISG1_RX1_P		RX7_N		
BC6_RD1P	P11_ISG1_RX2_N		RX2_P		
BC6_RD1N	P11_ISG1_RX2_P		RX2_N		
BC6_RD6N	P11_ISG1_RX3_N		RX1_P		
BC6_RD6P	P11_ISG1_RX3_P		RX1_N		
BC6_RD4N	P11_ISG1_RX4_N		RX6_P		
BC6_RD4P	P11_ISG1_RX4_P		RX6_N		
BC6_RD0N	P11_ISG1_RX5_N		RX8_P		
BC6_RD0P	P11_ISG1_RX5_P		RX8_N		
BC6_RD3P	P11_ISG1_RX6_N		RX3_P		
BC6_RD3N	P11_ISG1_RX6_P		RX3_N		
BC6_RD5N	P11_ISG1_RX7_N		RX4_P		
BC6_RD5P	P11_ISG1_RX7_P		RX4_N		
BC7_TD2P	P12_ISG0_TX0_N		TX2_P		
BC7_TD2N	P12_ISG0_TX0_P		TX2_N		
BC7_TD1N	P12_ISG0_TX1_N		TX6_P		
BC7_TD1P	P12_ISG0_TX1_P		TX6_N		
BC7_TD3N	P12_ISG0_TX2_N		TX8_P		
BC7_TD3P	P12_ISG0_TX2_P		TX8_N		
BC7_TD0P	P12_ISG0_TX3_N	QSFP-DD12	TX5_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN42
BC7_TD0N	P12_ISG0_TX3_P		TX5_N		
BC7_TD5P	P12_ISG0_TX4_N		TX1_P		
BC7_TD5N	P12_ISG0_TX4_P		TX1_N		
BC7_TD4N	P12_ISG0_TX5_N		TX3_P		
BC7_TD4P	P12_ISG0_TX5_P		TX3_N		
BC7_TD7P	P12_ISG0_TX6_N		TX7_P		

BC7_TD7N	P12_ISG0_TX6_P		TX7_N		
BC7_TD6N	P12_ISG0_TX7_N		TX4_P		
BC7_TD6P	P12_ISG0_TX7_P		TX4_N		
BC7_RD1P	P12_ISG0_RX0_N		RX7_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC7_RD1N	P12_ISG0_RX0_P		RX7_N		
BC7_RD4N	P12_ISG0_RX1_N		RX2_P		
BC7_RD4P	P12_ISG0_RX1_P		RX2_N		
BC7_RD0N	P12_ISG0_RX2_N		RX8_P		
BC7_RD0P	P12_ISG0_RX2_P		RX8_N		
BC7_RD3P	P12_ISG0_RX3_N		RX1_P		
BC7_RD3N	P12_ISG0_RX3_P		RX1_N		
BC7_RD5N	P12_ISG0_RX4_N		RX4_P		
BC7_RD5P	P12_ISG0_RX4_P		RX4_N		
BC7_RD6P	P12_ISG0_RX5_N		RX6_P		
BC7_RD6N	P12_ISG0_RX5_P		RX6_N		
BC7_RD7P	P12_ISG0_RX6_N		RX5_P		
BC7_RD7N	P12_ISG0_RX6_P		RX5_N		
BC7_RD2N	P12_ISG0_RX7_N		RX7_P		
BC7_RD2P	P12_ISG0_RX7_P		RX7_N		
BC16_TD3N	P13_ISG22_TX0_N		TX4_P		
BC16_TD3P	P13_ISG22_TX0_P		TX4_N		
BC16_TD2P	P13_ISG22_TX1_N		TX8_P		
BC16_TD2N	P13_ISG22_TX1_P		TX8_N		
BC16_TD1N	P13_ISG22_TX2_N		TX3_P		
BC16_TD1P	P13_ISG22_TX2_P		TX3_N		
BC16_TD0P	P13_ISG22_TX3_N		TX1_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN15
BC16_TD0N	P13_ISG22_TX3_P		TX1_N		
BC16_TD4N	P13_ISG22_TX4_N	QSFP-DD13	TX7_P		
BC16_TD4P	P13_ISG22_TX4_P		TX7_N		
BC16_TD6N	P13_ISG22_TX5_N		TX5_P		
BC16_TD6P	P13_ISG22_TX5_P		TX5_N		
BC16_TD7P	P13_ISG22_TX6_N		TX6_P		
BC16_TD7N	P13_ISG22_TX6_P		TX6_N		
BC16_TD5P	P13_ISG22_TX7_N		TX2_P		
BC16_TD5N	P13_ISG22_TX7_P		TX2_N		
BC16_RD5P	P13_ISG22_RX0_N		RX1_P		

BC16_RD5N	P13_ISG22_RX0_P		RX1_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC16_RD0P	P13_ISG22_RX1_N		RX5_P		
BC16_RD0N	P13_ISG22_RX1_P		RX5_N		
BC16_RD3N	P13_ISG22_RX2_N		RX4_P		
BC16_RD3P	P13_ISG22_RX2_P		RX4_N		
BC16_RD6N	P13_ISG22_RX3_N		RX3_P		
BC16_RD6P	P13_ISG22_RX3_P		RX3_N		
BC16_RD7P	P13_ISG22_RX4_N		RX8_P		
BC16_RD7N	P13_ISG22_RX4_P		RX8_N		
BC16_RD1P	P13_ISG22_RX5_N		RX2_P		
BC16_RD1N	P13_ISG22_RX5_P		RX2_N		
BC16_RD2N	P13_ISG22_RX6_N		RX6_P		
BC16_RD2P	P13_ISG22_RX6_P		RX6_N		
BC16_RD4P	P13_ISG22_RX7_N		RX7_P		
BC16_RD4N	P13_ISG22_RX7_P		RX7_N		
BC17_TD1N	P14_ISG23_TX0_N	QSFP-DD14	TX6_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN34
BC17_TD1P	P14_ISG23_TX0_P		TX6_N		
BC17_TD3N	P14_ISG23_TX1_N		TX5_P		
BC17_TD3P	P14_ISG23_TX1_P		TX5_N		
BC17_TD2P	P14_ISG23_TX2_N		TX1_P		
BC17_TD2N	P14_ISG23_TX2_P		TX1_N		
BC17_TD4N	P14_ISG23_TX3_N		TX3_P		
BC17_TD4P	P14_ISG23_TX3_P		TX3_N		
BC17_TD0P	P14_ISG23_TX4_N		TX7_P		
BC17_TD0N	P14_ISG23_TX4_P		TX7_N		
BC17_TD7P	P14_ISG23_TX5_N		TX8_P		
BC17_TD7N	P14_ISG23_TX5_P		TX8_N		
BC17_TD6N	P14_ISG23_TX6_N		TX2_P		
BC17_TD6P	P14_ISG23_TX6_P		TX2_N		
BC17_TD5P	P14_ISG23_TX7_N		TX4_P		
BC17_TD5N	P14_ISG23_TX7_P		TX4_N		
BC17_RD1P	P14_ISG23_RX0_N		RX8_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC17_RD1N	P14_ISG23_RX0_P		RX8_N		
BC17_RD0N	P14_ISG23_RX1_N		RX4_P		
BC17_RD0P	P14_ISG23_RX1_P		RX4_N		
BC17_RD3P	P14_ISG23_RX2_N		RX3_P		

BC17_RD3N	P14_ISG23_RX2_P		RX3_N		
BC17_RD6N	P14_ISG23_RX3_N		RX5_P		
BC17_RD6P	P14_ISG23_RX3_P		RX5_N		
BC17_RD5P	P14_ISG23_RX4_N		RX2_P		
BC17_RD5N	P14_ISG23_RX4_P		RX2_N		
BC17_RD7P	P14_ISG23_RX5_N		RX1_P		
BC17_RD7N	P14_ISG23_RX5_P		RX1_N		
BC17_RD2N	P14_ISG23_RX6_N		RX7_P		
BC17_RD2P	P14_ISG23_RX6_P		RX7_N		
BC17_RD4P	P14_ISG23_RX7_N		RX6_P		
BC17_RD4N	P14_ISG23_RX7_P		RX6_N		
BC18_TD6P	P15_ISG21_TX0_N	QSFP-DD15	TX4_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN24
BC18_TD6N	P15_ISG21_TX0_P		TX4_N		
BC18_TD5P	P15_ISG21_TX1_N		TX8_P		
BC18_TD5N	P15_ISG21_TX1_P		TX8_N		
BC18_TD4P	P15_ISG21_TX2_N		TX7_P		
BC18_TD4N	P15_ISG21_TX2_P		TX7_N		
BC18_TD7N	P15_ISG21_TX3_N		TX2_P		
BC18_TD7P	P15_ISG21_TX3_P		TX2_N		
BC18_TD0N	P15_ISG21_TX4_N		TX3_P		
BC18_TD0P	P15_ISG21_TX4_P		TX3_N		
BC18_TD3P	P15_ISG21_TX5_N		TX1_P		
BC18_TD3N	P15_ISG21_TX5_P		TX1_N		
BC18_TD2N	P15_ISG21_TX6_N		TX5_P		
BC18_TD2P	P15_ISG21_TX6_P		TX5_N		
BC18_TD1P	P15_ISG21_TX7_N		TX6_P		
BC18_TD1N	P15_ISG21_TX7_P		TX6_N		
BC18_RD5P	P15_ISG21_RX0_N		RX6_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC18_RD5N	P15_ISG21_RX0_P		RX6_N		
BC18_RD3N	P15_ISG21_RX1_N		RX2_P		
BC18_RD3P	P15_ISG21_RX1_P		RX2_N		
BC18_RD0P	P15_ISG21_RX2_N		RX8_P		
BC18_RD0N	P15_ISG21_RX2_P		RX8_N		
BC18_RD7P	P15_ISG21_RX3_N		RX1_P		
BC18_RD7N	P15_ISG21_RX3_P		RX1_N		
BC18_RD1N	P15_ISG21_RX4_N		RX7_P		

BC18_RD1P	P15_ISG21_RX4_P		RX7_N		
BC18_RD4N	P15_ISG21_RX5_N		RX4_P		
BC18_RD4P	P15_ISG21_RX5_P		RX4_N		
BC18_RD2P	P15_ISG21_RX6_N		RX3_P		
BC18_RD2N	P15_ISG21_RX6_P		RX3_N		
BC18_RD6N	P15_ISG21_RX7_N		RX5_P		
BC18_RD6P	P15_ISG21_RX7_P		RX5_N		
BC19_TD2P	P16_ISG20_TX0_N	QSFP-DD16	TX2_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN13
BC19_TD2N	P16_ISG20_TX0_P		TX2_N		
BC19_TD0P	P16_ISG20_TX1_N		TX6_P		
BC19_TD0N	P16_ISG20_TX1_P		TX6_N		
BC19_TD1P	P16_ISG20_TX2_N		TX8_P		
BC19_TD1N	P16_ISG20_TX2_P		TX8_N		
BC19_TD3N	P16_ISG20_TX3_N		TX5_P		
BC19_TD3P	P16_ISG20_TX3_P		TX5_N		
BC19_TD5P	P16_ISG20_TX4_N		TX7_P		
BC19_TD5N	P16_ISG20_TX4_P		TX7_N		
BC19_TD6N	P16_ISG20_TX5_N		TX4_P		
BC19_TD6P	P16_ISG20_TX5_P		TX4_N		
BC19_TD7P	P16_ISG20_TX6_N		TX1_P		
BC19_TD7N	P16_ISG20_TX6_P		TX1_N		
BC19_TD4N	P16_ISG20_TX7_N		TX3_P		
BC19_TD4P	P16_ISG20_TX7_P		TX3_N		
BC19_RD4P	P16_ISG20_RX0_N		RX3_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC19_RD4N	P16_ISG20_RX0_P		RX3_N		
BC19_RD6P	P16_ISG20_RX1_N		RX6_P		
BC19_RD6N	P16_ISG20_RX1_P		RX6_N		
BC19_RD0N	P16_ISG20_RX2_N		RX7_P		
BC19_RD0P	P16_ISG20_RX2_P		RX7_N		
BC19_RD5P	P16_ISG20_RX3_N		RX5_P		
BC19_RD5N	P16_ISG20_RX3_P		RX5_N		
BC19_RD2N	P16_ISG20_RX4_N		RX2_P		
BC19_RD2P	P16_ISG20_RX4_P		RX2_N		
BC19_RD1P	P16_ISG20_RX5_N		RX8_P		
BC19_RD1N	P16_ISG20_RX5_P		RX8_N		
BC19_RD7N	P16_ISG20_RX6_N		RX4_P		

BC19_RD7P	P16_ISG20_RX6_P		RX4_N		
BC19_RD3N	P16_ISG20_RX7_N		RX1_P		
BC19_RD3P	P16_ISG20_RX7_P		RX1_N		
BC21_TD3P	P17_ISG19_TX0_N		RX4_P		
BC21_TD3N	P17_ISG19_TX0_P		RX4_N		
BC21_TD0N	P17_ISG19_TX1_N		TX8_P		
BC21_TD0P	P17_ISG19_TX1_P		TX8_N		
BC21_TD2P	P17_ISG19_TX2_N		TX7_P		
BC21_TD2N	P17_ISG19_TX2_P		TX7_N		
BC21_TD6N	P17_ISG19_TX3_N		TX3_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC21_TD6P	P17_ISG19_TX3_P		TX3_N		
BC21_TD5P	P17_ISG19_TX4_N		TX6_P		
BC21_TD5N	P17_ISG19_TX4_P		TX6_N		
BC21_TD4N	P17_ISG19_TX5_N		TX1_P		
BC21_TD4P	P17_ISG19_TX5_P		TX1_N		
BC21_TD7P	P17_ISG19_TX6_N		TX5_P		
BC21_TD7N	P17_ISG19_TX6_P		TX5_N		
BC21_TD1N	P17_ISG19_TX7_N		TX2_P		
BC21_TD1P	P17_ISG19_TX7_P	QSFP-DD17	TX2_N		CONN9
BC21_RD3N	P17_ISG19_RX0_N		RX1_P		
BC21_RD3P	P17_ISG19_RX0_P		RX1_N		
BC21_RD0P	P17_ISG19_RX1_N		RX5_P		
BC21_RD0N	P17_ISG19_RX1_P		RX5_N		
BC21_RD4N	P17_ISG19_RX2_N		RX6_P		
BC21_RD4P	P17_ISG19_RX2_P		RX6_N		
BC21_RD1P	P17_ISG19_RX3_N		RX4_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC21_RD1N	P17_ISG19_RX3_P		RX4_N		
BC21_RD5N	P17_ISG19_RX4_N		RX2_P		
BC21_RD5P	P17_ISG19_RX4_P		RX2_N		
BC21_RD6P	P17_ISG19_RX5_N		RX8_P		
BC21_RD6N	P17_ISG19_RX5_P		RX8_N		
BC21_RD7N	P17_ISG19_RX6_N		RX3_P		
BC21_RD7P	P17_ISG19_RX6_P		RX3_N		
BC21_RD2N	P17_ISG19_RX7_N		RX7_P		
BC21_RD2P	P17_ISG19_RX7_P		RX7_N		

BC20_TD7N	P18_ISG18_TX0_N	QSFP-DD18	TX5_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN28
BC20_TD7P	P18_ISG18_TX0_P		TX5_N		
BC20_TD6P	P18_ISG18_TX1_N		TX1_P		
BC20_TD6N	P18_ISG18_TX1_P		TX1_N		
BC20_TD0N	P18_ISG18_TX2_N		TX6_P		
BC20_TD0P	P18_ISG18_TX2_P		TX6_N		
BC20_TD4P	P18_ISG18_TX3_N		TX3_P		
BC20_TD4N	P18_ISG18_TX3_P		TX3_N		
BC20_TD1P	P18_ISG18_TX4_N		TX7_P		
BC20_TD1N	P18_ISG18_TX4_P		TX7_N		
BC20_TD2N	P18_ISG18_TX5_N		TX8_P		
BC20_TD2P	P18_ISG18_TX5_P		TX8_N		
BC20_TD5P	P18_ISG18_TX6_N		TX2_P		
BC20_TD5N	P18_ISG18_TX6_P		TX2_N		
BC20_TD3N	P18_ISG18_TX7_N		TX4_P		
BC20_TD3P	P18_ISG18_TX7_P		TX4_N		
BC20_RD7N	P18_ISG18_RX0_N		RX8_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC20_RD7P	P18_ISG18_RX0_P		RX8_N		
BC20_RD6N	P18_ISG18_RX1_N		RX3_P		
BC20_RD6P	P18_ISG18_RX1_P		RX3_N		
BC20_RD5N	P18_ISG18_RX2_N		RX4_P		
BC20_RD5P	P18_ISG18_RX2_P		RX4_N		
BC20_RD4P	P18_ISG18_RX3_N		RX2_P		
BC20_RD4N	P18_ISG18_RX3_P		RX2_N		
BC20_RD2N	P18_ISG18_RX4_N		RX5_P		
BC20_RD2P	P18_ISG18_RX4_P		RX5_N		
BC20_RD1P	P18_ISG18_RX5_N		RX6_P		
BC20_RD1N	P18_ISG18_RX5_P		RX6_N		
BC20_RD0N	P18_ISG18_RX6_N		RX7_P		
BC20_RD0P	P18_ISG18_RX6_P		RX7_N		
BC20_RD3P	P18_ISG18_RX7_N		RX1_P		
BC20_RD3N	P18_ISG18_RX7_P		RX1_N		
BC22_TD5N	P19_ISG17_TX0_N	QSFP-DD19	TX4_P	QSFP-DD CHANNELS SWAPPED	CONN10
BC22_TD5P	P19_ISG17_TX0_P		TX4_N		
BC22_TD6P	P19_ISG17_TX1_N		TX2_P		
BC22_TD6N	P19_ISG17_TX1_P		TX2_N		

BC22_TD7N	P19_ISG17_TX2_N		TX8_P	WITH IN THE QUAD	
BC22_TD7P	P19_ISG17_TX2_P		TX8_N		
BC22_TD0N	P19_ISG17_TX3_N		TX7_P		
BC22_TD0P	P19_ISG17_TX3_P		TX7_N		
BC22_TD4P	P19_ISG17_TX4_N		TX5_P		
BC22_TD4N	P19_ISG17_TX4_P		TX5_N		
BC22_TD2P	P19_ISG17_TX5_N		TX3_P		
BC22_TD2N	P19_ISG17_TX5_P		TX3_N		
BC22_TD1N	P19_ISG17_TX6_N		TX1_P		
BC22_TD1P	P19_ISG17_TX6_P		TX1_N		
BC22_TD3N	P19_ISG17_TX7_N		TX6_P		
BC22_TD3P	P19_ISG17_TX7_P		TX6_N		
BC22_RD6N	P19_ISG17_RX0_N		RX1_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC22_RD6P	P19_ISG17_RX0_P		RX1_N		
BC22_RD3N	P19_ISG17_RX1_N		RX3_P		
BC22_RD3P	P19_ISG17_RX1_P		RX3_N		
BC22_RD7P	P19_ISG17_RX2_N		RX5_P		
BC22_RD7N	P19_ISG17_RX2_P		RX5_N		
BC22_RD1P	P19_ISG17_RX3_N		RX2_P		
BC22_RD1N	P19_ISG17_RX3_P		RX2_N		
BC22_RD2P	P19_ISG17_RX4_N		RX7_P		
BC22_RD2N	P19_ISG17_RX4_P		RX7_N		
BC22_RD5P	P19_ISG17_RX5_N		RX6_P		
BC22_RD5N	P19_ISG17_RX5_P		RX6_N		
BC22_RD0N	P19_ISG17_RX6_N		RX4_P		
BC22_RD0P	P19_ISG17_RX6_P		RX4_N		
BC22_RD4N	P19_ISG17_RX7_N		RX8_P		
BC22_RD4P	P19_ISG17_RX7_P		RX8_N		
BC23_TD1P	P20_ISG16_TX0_N	QSFP-DD20	TX2_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN29
BC23_TD1N	P20_ISG16_TX0_P		TX2_N		
BC23_TD3P	P20_ISG16_TX1_N		TX6_P		
BC23_TD3N	P20_ISG16_TX1_P		TX6_N		
BC23_TD2N	P20_ISG16_TX2_N		TX5_P		
BC23_TD2P	P20_ISG16_TX2_P		TX5_N		
BC23_TD0N	P20_ISG16_TX3_N		TX7_P		
BC23_TD0P	P20_ISG16_TX3_P		TX7_N		

BC23_TD6P	P20_ISG16_TX4_N		TX1_P		
BC23_TD6N	P20_ISG16_TX4_P		TX1_N		
BC23_TD4P	P20_ISG16_TX5_N		TX3_P		
BC23_TD4N	P20_ISG16_TX5_P		TX3_N		
BC23_TD5N	P20_ISG16_TX6_N		TX8_P		
BC23_TD5P	P20_ISG16_TX6_P		TX8_N		
BC23_TD7P	P20_ISG16_TX7_N		TX4_P		
BC23_TD7N	P20_ISG16_TX7_P		TX4_N		
BC23_RD2N	P20_ISG16_RX0_N		RX7_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC23_RD2P	P20_ISG16_RX0_P		RX7_N		
BC23_RD0N	P20_ISG16_RX1_N		RX8_P		
BC23_RD0P	P20_ISG16_RX1_P		RX8_N		
BC23_RD3P	P20_ISG16_RX2_N		RX3_P		
BC23_RD3N	P20_ISG16_RX2_P		RX3_N		
BC23_RD1P	P20_ISG16_RX3_N		RX4_P		
BC23_RD1N	P20_ISG16_RX3_P		RX4_N		
BC23_RD4P	P20_ISG16_RX4_N		RX2_P		
BC23_RD4N	P20_ISG16_RX4_P		RX2_N		
BC23_RD6N	P20_ISG16_RX5_N		RX5_P		
BC23_RD6P	P20_ISG16_RX5_P		RX5_N		
BC23_RD5N	P20_ISG16_RX6_N		RX6_P		
BC23_RD5P	P20_ISG16_RX6_P		RX6_N		
BC23_RD7P	P20_ISG16_RX7_N		RX1_P		
BC23_RD7N	P20_ISG16_RX7_P		RX1_N		
BC0_TD3P	P21_ISG7_TX0_N	QSFP-DD21	TX4_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN16
BC0_TD3N	P21_ISG7_TX0_P		TX4_N		
BC0_TD2N	P21_ISG7_TX1_N		TX8_P		
BC0_TD2P	P21_ISG7_TX1_P		TX8_N		
BC0_TD0N	P21_ISG7_TX2_N		TX7_P		
BC0_TD0P	P21_ISG7_TX2_P		TX7_N		
BC0_TD4P	P21_ISG7_TX3_N		TX3_P		
BC0_TD4N	P21_ISG7_TX3_P		TX3_N		
BC0_TD6P	P21_ISG7_TX4_N		TX1_P		
BC0_TD6N	P21_ISG7_TX4_P		TX1_N		
BC0_TD7N	P21_ISG7_TX5_N		TX5_P		
BC0_TD7P	P21_ISG7_TX5_P		TX5_N		

BC0_TD5N	P21_ISG7_TX6_N		TX6_P		
BC0_TD5P	P21_ISG7_TX6_P		TX6_N		
BC0_TD1P	P21_ISG7_TX7_N		TX2_P		
BC0_TD1N	P21_ISG7_TX7_P		TX2_N		
BC0_RD3P	P21_ISG7_RX0_N		RX6_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC0_RD3N	P21_ISG7_RX0_P		RX6_N		
BC0_RD1P	P21_ISG7_RX1_N		RX2_P		
BC0_RD1N	P21_ISG7_RX1_P		RX2_N		
BC0_RD2N	P21_ISG7_RX2_N		RX5_P		
BC0_RD2P	P21_ISG7_RX2_P		RX5_N		
BC0_RD6N	P21_ISG7_RX3_N		RX1_P		
BC0_RD6P	P21_ISG7_RX3_P		RX1_N		
BC0_RD4P	P21_ISG7_RX4_N		RX4_P		
BC0_RD4N	P21_ISG7_RX4_P		RX4_N		
BC0_RD5N	P21_ISG7_RX5_N		RX8_P		
BC0_RD5P	P21_ISG7_RX5_P		RX8_N		
BC0_RD7P	P21_ISG7_RX6_N		RX3_P		
BC0_RD7N	P21_ISG7_RX6_P		RX3_N		
BC0_RD0N	P21_ISG7_RX7_N		RX7_P		
BC0_RD0P	P21_ISG7_RX7_P		RX7_N		
BC1_TD1P	P22_ISG6_TX0_N	QSFP-DD22	TX6_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN35
BC1_TD1N	P22_ISG6_TX0_P		TX6_N		
BC1_TD4P	P22_ISG6_TX1_N		TX5_P		
BC1_TD4N	P22_ISG6_TX1_P		TX5_N		
BC1_TD3P	P22_ISG6_TX2_N		TX1_P		
BC1_TD3N	P22_ISG6_TX2_P		TX1_N		
BC1_TD2N	P22_ISG6_TX3_N		TX3_P		
BC1_TD2P	P22_ISG6_TX3_P		TX3_N		
BC1_TD0N	P22_ISG6_TX4_N		TX7_P		
BC1_TD0P	P22_ISG6_TX4_P		TX7_N		
BC1_TD7N	P22_ISG6_TX5_N		TX8_P		
BC1_TD7P	P22_ISG6_TX5_P		TX8_N		
BC1_TD5N	P22_ISG6_TX6_N		TX6_P		
BC1_TD5P	P22_ISG6_TX6_P		TX6_N		
BC1_TD6P	P22_ISG6_TX7_N		TX4_P		
BC1_TD6N	P22_ISG6_TX7_P		TX4_N		

BC1_RD2N	P22_ISG6_RX0_N		RX5_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC1_RD2P	P22_ISG6_RX0_P		RX5_N		
BC1_RD1P	P22_ISG6_RX1_N		RX8_P		
BC1_RD1N	P22_ISG6_RX1_P		RX8_N		
BC1_RD3P	P22_ISG6_RX2_N		RX3_P		
BC1_RD3N	P22_ISG6_RX2_P		RX3_N		
BC1_RD6N	P22_ISG6_RX3_N		RX6_N		
BC1_RD6P	P22_ISG6_RX3_P		RX6_P		
BC1_RD0N	P22_ISG6_RX4_N		RX4_P		
BC1_RD0P	P22_ISG6_RX4_P		RX4_N		
BC1_RD7N	P22_ISG6_RX5_N		RX5_P		
BC1_RD7P	P22_ISG6_RX5_P		RX5_N		
BC1_RD4N	P22_ISG6_RX6_N		RX6_N		
BC1_RD4P	P22_ISG6_RX6_P		RX6_P		
BC1_RD5P	P22_ISG6_RX7_N		RX7_N		
BC1_RD5N	P22_ISG6_RX7_P		RX7_P		
BC2_TD6N	P23_ISG5_TX0_N	QSFP-DD23	TX2_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN17
BC2_TD6P	P23_ISG5_TX0_P		TX2_N		
BC2_TD4N	P23_ISG5_TX1_N		TX4_P		
BC2_TD4P	P23_ISG5_TX1_P		TX4_N		
BC2_TD5P	P23_ISG5_TX2_N		TX7_P		
BC2_TD5N	P23_ISG5_TX2_P		TX7_N		
BC2_TD7P	P23_ISG5_TX3_N		TX8_P		
BC2_TD7N	P23_ISG5_TX3_P		TX8_N		
BC2_TD1N	P23_ISG5_TX4_N		TX3_N		
BC2_TD1P	P23_ISG5_TX4_P		TX3_P		
BC2_TD0P	P23_ISG5_TX5_N		TX1_N		
BC2_TD0N	P23_ISG5_TX5_P		TX1_P		
BC2_TD2P	P23_ISG5_TX6_N		TX5_N		
BC2_TD2N	P23_ISG5_TX6_P		TX5_P		
BC2_TD3N	P23_ISG5_TX7_N		TX6_N		
BC2_TD3P	P23_ISG5_TX7_P		TX6_P		
BC2_RD5P	P23_ISG5_RX0_N		RX5_N	QSFP-DD CHANNELS SWAPPED	
BC2_RD5N	P23_ISG5_RX0_P		RX5_P		
BC2_RD4N	P23_ISG5_RX1_N		RX6_N		
BC2_RD4P	P23_ISG5_RX1_P		RX6_P		

BC2_RD2N	P23_ISG5_RX2_N		RX2_P	WITH IN THE QUAD	
BC2_RD2P	P23_ISG5_RX2_P		RX2_N		
BC2_RD6N	P23_ISG5_RX3_N		RX3_N		
BC2_RD6P	P23_ISG5_RX3_P		RX3_P		
BC2_RD7P	P23_ISG5_RX4_N		RX8_N		
BC2_RD7N	P23_ISG5_RX4_P		RX8_P		
BC2_RD3P	P23_ISG5_RX5_N		RX3_P		
BC2_RD3N	P23_ISG5_RX5_P		RX3_N		
BC2_RD1P	P23_ISG5_RX6_N		RX7_P		
BC2_RD1N	P23_ISG5_RX6_P		RX7_N		
BC2_RD0N	P23_ISG5_RX7_N		RX4_P		
BC2_RD0P	P23_ISG5_RX7_P		RX4_N		
BC3_TD2P	P24_ISG4_TX0_N		TX2_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN36
BC3_TD2N	P24_ISG4_TX0_P		TX2_P		
BC3_TD4N	P24_ISG4_TX1_N		TX8_N		
BC3_TD4P	P24_ISG4_TX1_P		TX8_P		
BC3_TD7P	P24_ISG4_TX2_N		TX6_N		
BC3_TD7N	P24_ISG4_TX2_P		TX6_P		
BC3_TD1P	P24_ISG4_TX3_N		TX5_P		
BC3_TD1N	P24_ISG4_TX3_P		TX5_N		
BC3_TD3P	P24_ISG4_TX4_N		TX7_P		
BC3_TD3N	P24_ISG4_TX4_P		TX7_N		
BC3_TD5N	P24_ISG4_TX5_N		TX1_P		
BC3_TD5P	P24_ISG4_TX5_P	QSFP-DD24	TX1_N		
BC3_TD0N	P24_ISG4_TX6_N		TX3_P		
BC3_TD0P	P24_ISG4_TX6_P		TX3_N		
BC3_TD6N	P24_ISG4_TX7_N		TX4_P		
BC3_TD6P	P24_ISG4_TX7_P		TX4_N		
BC3_RD2N	P24_ISG4_RX0_N		RX1_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC3_RD2P	P24_ISG4_RX0_P		RX1_N		
BC3_RD1P	P24_ISG4_RX1_N		RX3_P		
BC3_RD1N	P24_ISG4_RX1_P		RX3_N		
BC3_RD0N	P24_ISG4_RX2_N		RX7_P		
BC3_RD0P	P24_ISG4_RX2_P		RX7_N		
BC3_RD4N	P24_ISG4_RX3_N		RX2_N		
BC3_RD4P	P24_ISG4_RX3_P		RX2_P		

BC3_RD3P	P24_ISG4_RX4_N		RX8_P		
BC3_RD3N	P24_ISG4_RX4_P		RX8_N		
BC3_RD6N	P24_ISG4_RX5_N		RX4_P		
BC3_RD6P	P24_ISG4_RX5_P		RX4_N		
BC3_RD7P	P24_ISG4_RX6_N		RX5_N		
BC3_RD7N	P24_ISG4_RX6_P		RX5_P		
BC3_RD5N	P24_ISG4_RX7_N		RX6_P		
BC3_RD5P	P24_ISG4_RX7_P		RX6_N		
BC25_TD1P	P25_ISG15_TX0_N		TX4_P		
BC25_TD1N	P25_ISG15_TX0_P		TX4_N		
BC25_TD2P	P25_ISG15_TX1_N		TX8_N		
BC25_TD2N	P25_ISG15_TX1_P		TX8_P		
BC25_TD3P	P25_ISG15_TX2_N		TX7_N		
BC25_TD3N	P25_ISG15_TX2_P		TX7_P		
BC25_TD4P	P25_ISG15_TX3_N		TX3_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC25_TD4N	P25_ISG15_TX3_P		TX3_P		
BC25_TD0N	P25_ISG15_TX4_N		TX1_N		
BC25_TD0P	P25_ISG15_TX4_P		TX1_P		
BC25_TD6P	P25_ISG15_TX5_N		TX5_N		
BC25_TD6N	P25_ISG15_TX5_P		TX5_P		
BC25_TD7N	P25_ISG15_TX6_N		TX6_N		
BC25_TD7P	P25_ISG15_TX6_P	QSFP-DD25	TX6_P		CONN18
BC25_TD5P	P25_ISG15_TX7_N		TX2_N		
BC25_TD5N	P25_ISG15_TX7_P		TX2_P		
BC25_RD2N	P25_ISG15_RX0_N		RX5_N		
BC25_RD2P	P25_ISG15_RX0_P		RX5_P		
BC25_RD3N	P25_ISG15_RX1_N		RX3_P		
BC25_RD3P	P25_ISG15_RX1_P		RX3_N		
BC25_RD0N	P25_ISG15_RX2_N		RX2_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC25_RD0P	P25_ISG15_RX2_P		RX2_P		
BC25_RD4P	P25_ISG15_RX3_N		RX4_N		
BC25_RD4N	P25_ISG15_RX3_P		RX4_P		
BC25_RD6N	P25_ISG15_RX4_N		RX7_P		
BC25_RD6P	P25_ISG15_RX4_P		RX7_N		
BC25_RD1P	P25_ISG15_RX5_N		RX6_N		
BC25_RD1N	P25_ISG15_RX5_P		RX6_P		

BC25_RD5N	P25_ISG15_RX6_N		RX8_N		
BC25_RD5P	P25_ISG15_RX6_P		RX8_P		
BC25_RD7P	P25_ISG15_RX7_N		RX1_P		
BC25_RD7N	P25_ISG15_RX7_P		RX1_N		
BC24_TD5P	P26_ISG14_TX0_N	QSFP-DD26	TX6_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN37
BC24_TD5N	P26_ISG14_TX0_P		TX6_N		
BC24_TD0P	P26_ISG14_TX1_N		TX1_P		
BC24_TD0N	P26_ISG14_TX1_P		TX1_N		
BC24_TD6N	P26_ISG14_TX2_N		TX3_P		
BC24_TD6P	P26_ISG14_TX2_P		TX3_N		
BC24_TD7P	P26_ISG14_TX3_N		TX5_P		
BC24_TD7N	P26_ISG14_TX3_P		TX5_N		
BC24_TD4N	P26_ISG14_TX4_N		TX7_P		
BC24_TD4P	P26_ISG14_TX4_P		TX7_N		
BC24_TD3N	P26_ISG14_TX5_N		TX8_P		
BC24_TD3P	P26_ISG14_TX5_P		TX8_N		
BC24_TD2P	P26_ISG14_TX6_N		TX2_P		
BC24_TD2N	P26_ISG14_TX6_P		TX2_N		
BC24_TD1N	P26_ISG14_TX7_N		TX4_P		
BC24_TD1P	P26_ISG14_TX7_P		TX4_N		
BC24_RD4P	P26_ISG14_RX0_N		RX7_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC24_RD4N	P26_ISG14_RX0_P		RX7_P		
BC24_RD5P	P26_ISG14_RX1_N		RX3_P		
BC24_RD5N	P26_ISG14_RX1_P		RX3_N		
BC24_RD0N	P26_ISG14_RX2_N		RX2_N		
BC24_RD0P	P26_ISG14_RX2_P		RX2_P		
BC24_RD6N	P26_ISG14_RX3_N		RX4_P		
BC24_RD6P	P26_ISG14_RX3_P		RX4_N		
BC24_RD7P	P26_ISG14_RX4_N		RX8_P		
BC24_RD7N	P26_ISG14_RX4_P		RX8_N		
BC24_RD1P	P26_ISG14_RX5_N		RX6_N		
BC24_RD1N	P26_ISG14_RX5_P		RX6_P		
BC24_RD3P	P26_ISG14_RX6_N		RX1_N		
BC24_RD3N	P26_ISG14_RX6_P		RX1_P		
BC24_RD2N	P26_ISG14_RX7_N		RX5_N		
BC24_RD2P	P26_ISG14_RX7_P		RX5_P		

BC27_TD1N	P27_ISG13_TX0_N	QSFP-DD27	TX2_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN19
BC27_TD1P	P27_ISG13_TX0_P		TX2_N		
BC27_TD5P	P27_ISG13_TX1_N		TX8_P		
BC27_TD5N	P27_ISG13_TX1_P		TX8_N		
BC27_TD3N	P27_ISG13_TX2_N		TX4_P		
BC27_TD3P	P27_ISG13_TX2_P		TX4_N		
BC27_TD2P	P27_ISG13_TX3_N		TX6_P		
BC27_TD2N	P27_ISG13_TX3_P		TX6_N		
BC27_TD4N	P27_ISG13_TX4_N		TX7_P		
BC27_TD4P	P27_ISG13_TX4_P		TX7_N		
BC27_TD0N	P27_ISG13_TX5_N		TX3_N		
BC27_TD0P	P27_ISG13_TX5_P		TX3_P		
BC27_TD7N	P27_ISG13_TX6_N		TX1_P		
BC27_TD7P	P27_ISG13_TX6_P		TX1_N		
BC27_TD6P	P27_ISG13_TX7_N		TX5_N		
BC27_TD6N	P27_ISG13_TX7_P		TX5_P		
BC27_RD2N	P27_ISG13_RX0_N		RX5_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC27_RD2P	P27_ISG13_RX0_P		RX5_P		
BC27_RD3P	P27_ISG13_RX1_N		RX1_N		
BC27_RD3N	P27_ISG13_RX1_P		RX1_P		
BC27_RD6N	P27_ISG13_RX2_N		RX4_P		
BC27_RD6P	P27_ISG13_RX2_P		RX4_N		
BC27_RD1P	P27_ISG13_RX3_N		RX2_N		
BC27_RD1N	P27_ISG13_RX3_P		RX2_P		
BC27_RD0N	P27_ISG13_RX4_N		RX6_N		
BC27_RD0P	P27_ISG13_RX4_P		RX6_P		
BC27_RD7P	P27_ISG13_RX5_N		RX3_P		
BC27_RD7N	P27_ISG13_RX5_P		RX3_N		
BC27_RD4N	P27_ISG13_RX6_N		RX7_P		
BC27_RD4P	P27_ISG13_RX6_P		RX7_N		
BC27_RD5N	P27_ISG13_RX7_N		RX8_N		
BC27_RD5P	P27_ISG13_RX7_P		RX8_P		
BC26_TD3P	P28_ISG12_TX0_N	QSFP-DD28	TX4_N	QSFP-DD CHANNELS SWAPPED	CONN38
BC26_TD3N	P28_ISG12_TX0_P		TX4_P		
BC26_TD5P	P28_ISG12_TX1_N		TX2_N		

BC26_TD5N	P28_ISG12_TX1_P		TX2_P	WITH IN THE QUAD	
BC26_TD6P	P28_ISG12_TX2_N		TX6_N		
BC26_TD6N	P28_ISG12_TX2_P		TX6_P		
BC26_TD0P	P28_ISG12_TX3_N		TX1_P		
BC26_TD0N	P28_ISG12_TX3_P		TX1_N		
BC26_TD7N	P28_ISG12_TX4_N		TX5_N		
BC26_TD7P	P28_ISG12_TX4_P		TX5_P		
BC26_TD4N	P28_ISG12_TX5_N		TX3_P		
BC26_TD4P	P28_ISG12_TX5_P		TX3_N		
BC26_TD1N	P28_ISG12_TX6_N		TX8_P		
BC26_TD1P	P28_ISG12_TX6_P		TX8_N		
BC26_TD2P	P28_ISG12_TX7_N		TX7_P		
BC26_TD2N	P28_ISG12_TX7_P		TX7_N		
BC26_RD7P	P28_ISG12_RX0_N		RX3_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC26_RD7N	P28_ISG12_RX0_P		RX3_N		
BC26_RD1N	P28_ISG12_RX1_N		RX6_P		
BC26_RD1P	P28_ISG12_RX1_P		RX6_N		
BC26_RD5N	P28_ISG12_RX2_N		RX5_N		
BC26_RD5P	P28_ISG12_RX2_P		RX5_P		
BC26_RD4N	P28_ISG12_RX3_N		RX8_P		
BC26_RD4P	P28_ISG12_RX3_P		RX8_N		
BC26_RD2N	P28_ISG12_RX4_N		RX2_N		
BC26_RD2P	P28_ISG12_RX4_P		RX2_P		
BC26_RD0P	P28_ISG12_RX5_N		RX4_P		
BC26_RD0N	P28_ISG12_RX5_P		RX4_N		
BC26_RD6N	P28_ISG12_RX6_N		RX7_P		
BC26_RD6P	P28_ISG12_RX6_P		RX7_N		
BC26_RD3N	P28_ISG12_RX7_N		RX1_P		
BC26_RD3P	P28_ISG12_RX7_P		RX1_N		
BC29_TD2P	P29_ISG11_TX0_N	QSFP-DD29	TX4_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN20
BC29_TD2N	P29_ISG11_TX0_P		TX4_P		
BC29_TD6P	P29_ISG11_TX1_N		TX5_N		
BC29_TD6N	P29_ISG11_TX1_P		TX5_P		
BC29_TD5N	P29_ISG11_TX2_N		TX8_N		
BC29_TD5P	P29_ISG11_TX2_P		TX8_P		
BC29_TD0N	P29_ISG11_TX3_N		TX7_N		

BC29_TD0P	P29_ISG11_TX3_P		TX7_P		
BC29_TD3N	P29_ISG11_TX4_N		TX3_P		
BC29_TD3P	P29_ISG11_TX4_P		TX3_N		
BC29_TD1N	P29_ISG11_TX5_N		TX1_P		
BC29_TD1P	P29_ISG11_TX5_P		TX1_N		
BC29_TD4P	P29_ISG11_TX6_N		TX6_N		
BC29_TD4N	P29_ISG11_TX6_P		TX6_P		
BC29_TD7N	P29_ISG11_TX7_N		TX2_N		
BC29_TD7P	P29_ISG11_TX7_P		TX2_P		
BC29_RD1N	P29_ISG11_RX0_N		RX8_P	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC29_RD1P	P29_ISG11_RX0_P		RX8_N		
BC29_RD0P	P29_ISG11_RX1_N		RX1_P		
BC29_RD0N	P29_ISG11_RX1_P		RX1_N		
BC29_RD3N	P29_ISG11_RX2_N		RX5_P		
BC29_RD3P	P29_ISG11_RX2_P		RX5_N		
BC29_RD7P	P29_ISG11_RX3_N		RX3_P		
BC29_RD7N	P29_ISG11_RX3_P		RX3_N		
BC29_RD6N	P29_ISG11_RX4_N		RX7_P		
BC29_RD6P	P29_ISG11_RX4_P		RX7_N		
BC29_RD2P	P29_ISG11_RX5_N		RX2_P		
BC29_RD2N	P29_ISG11_RX5_P		RX2_N		
BC29_RD4N	P29_ISG11_RX6_N		RX6_P		
BC29_RD4P	P29_ISG11_RX6_P		RX6_N		
BC29_RD5P	P29_ISG11_RX7_N		RX4_P		
BC29_RD5N	P29_ISG11_RX7_P		RX4_N		
BC28_TD4P	P30_ISG10_TX0_N		TX6_P		
BC28_TD4N	P30_ISG10_TX0_P		TX6_N		
BC28_TD7N	P30_ISG10_TX1_N		TX1_P		
BC28_TD7P	P30_ISG10_TX1_P		TX1_N		
BC28_TD2P	P30_ISG10_TX2_N		TX4_P		
BC28_TD2N	P30_ISG10_TX2_P	QSFP-DD30	TX4_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN39
BC28_TD3N	P30_ISG10_TX3_N		TX3_P		
BC28_TD3P	P30_ISG10_TX3_P		TX3_N		
BC28_TD6N	P30_ISG10_TX4_N		TX5_P		
BC28_TD6P	P30_ISG10_TX4_P		TX5_N		
BC28_TD3N	P30_ISG10_TX5_N		TX7_P		

BC28_TD3P	P30_ISG10_TX5_P		TX7_N		
BC28_TD5P	P30_ISG10_TX6_N		TX8_P		
BC28_TD5N	P30_ISG10_TX6_P		TX8_N		
BC28_TD0P	P30_ISG10_TX7_N		TX2_P		
BC28_TD0N	P30_ISG10_TX7_P		TX2_N		
BC28_RD2N	P30_ISG10_RX0_N		RX7_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC28_RD2P	P30_ISG10_RX0_P		RX7_P		
BC28_RD5P	P30_ISG10_RX1_N		RX8_P		
BC28_RD5N	P30_ISG10_RX1_P		RX8_N		
BC28_RD3N	P30_ISG10_RX2_N		RX3_P		
BC28_RD3P	P30_ISG10_RX2_P		RX3_N		
BC28_RD4P	P30_ISG10_RX3_N		RX2_P		
BC28_RD4N	P30_ISG10_RX3_P		RX2_N		
BC28_RD1N	P30_ISG10_RX4_N		RX4_P		
BC28_RD1P	P30_ISG10_RX4_P		RX4_N		
BC28_RD7P	P30_ISG10_RX5_N		RX6_P		
BC28_RD7N	P30_ISG10_RX5_P		RX6_N		
BC28_RD0N	P30_ISG10_RX6_N		RX1_N		
BC28_RD0P	P30_ISG10_RX6_P		RX1_P		
BC28_RD6N	P30_ISG10_RX7_N		RX5_P		
BC28_RD6P	P30_ISG10_RX7_P		RX5_N		
BC31_TD5P	P31_ISG9_TX0_N		TX5_N		
BC31_TD5N	P31_ISG9_TX0_P		TX5_P		
BC31_TD6P	P31_ISG9_TX1_N		TX4_P		
BC31_TD6N	P31_ISG9_TX1_P		TX4_N		
BC31_TD7N	P31_ISG9_TX2_N		TX2_P		
BC31_TD7P	P31_ISG9_TX2_P		TX2_N		
BC31_TD1P	P31_ISG9_TX3_N		TX8_P		
BC31_TD1N	P31_ISG9_TX3_P	QSFP-DD31	TX8_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN21
BC31_TD3N	P31_ISG9_TX4_N		TX1_N		
BC31_TD3P	P31_ISG9_TX4_P		TX1_P		
BC31_TD4P	P31_ISG9_TX5_N		TX6_P		
BC31_TD4N	P31_ISG9_TX5_P		TX6_N		
BC31_TD2P	P31_ISG9_TX6_N		TX3_N		
BC31_TD2N	P31_ISG9_TX6_P		TX3_P		
BC31_TD0N	P31_ISG9_TX7_N		TX7_P		

BC31_TD0P	P31_ISG9_TX7_P		TX7_N		
BC31_RD6N	P31_ISG9_RX0_N		RX5_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	
BC31_RD6P	P31_ISG9_RX0_P		RX5_P		
BC31_RD4P	P31_ISG9_RX1_N		RX2_P		
BC31_RD4N	P31_ISG9_RX1_P		RX2_N		
BC31_RD7P	P31_ISG9_RX2_N		RX1_N		
BC31_RD7N	P31_ISG9_RX2_P		RX1_P		
BC31_RD5P	P31_ISG9_RX3_N		RX6_N		
BC31_RD5N	P31_ISG9_RX3_P		RX6_P		
BC31_RD3P	P31_ISG9_RX4_N		RX4_P		
BC31_RD3N	P31_ISG9_RX4_P		RX4_N		
BC31_RD2N	P31_ISG9_RX5_N		RX8_P		
BC31_RD2P	P31_ISG9_RX5_P		RX8_N		
BC31_RD0N	P31_ISG9_RX6_N		RX3_P		
BC31_RD0P	P31_ISG9_RX6_P		RX3_N		
BC31_RD1P	P31_ISG9_RX7_N		RX7_P		
BC31_RD1N	P31_ISG9_RX7_P		RX7_N		
BC30_TD5N	P32_ISG8_TX0_N		TX2_N	QSFP-DD CHANNELS SWAPPED WITH IN THE QUAD	CONN40
BC30_TD5P	P32_ISG8_TX0_P		TX2_P		
BC30_TD6P	P32_ISG8_TX1_N		TX4_N		
BC30_TD6N	P32_ISG8_TX1_P		TX4_P		
BC30_TD7N	P32_ISG8_TX2_N		TX6_N		
BC30_TD7P	P32_ISG8_TX2_P		TX6_P		
BC30_TD0N	P32_ISG8_TX3_N		TX5_N		
BC30_TD0P	P32_ISG8_TX3_P		TX5_P		
BC30_TD4P	P32_ISG8_TX4_N		TX1_N		
BC30_TD4N	P32_ISG8_TX4_P	QSFP-DD32	TX1_P		
BC30_TD3P	P32_ISG8_TX5_N		TX3_N		
BC30_TD3N	P32_ISG8_TX5_P		TX3_P		
BC30_TD1N	P32_ISG8_TX6_N		TX7_P		
BC30_TD1P	P32_ISG8_TX6_P		TX7_N		
BC30_TD2P	P32_ISG8_TX7_N		TX8_P		
BC30_TD2N	P32_ISG8_TX7_P		TX8_N		
BC30_RD4N	P32_ISG8_RX0_N		RX3_P	QSFP-DD CHANNELS SWAPPED	
BC30_RD4P	P32_ISG8_RX0_P		RX3_N		
BC30_RD2P	P32_ISG8_RX1_N		RX5_P		

BC30_RD2N	P32_ISG8_RX1_P	RX5_N	WITH IN THE QUAD	
BC30_RD5N	P32_ISG8_RX2_N	RX7_N		
BC30_RD5P	P32_ISG8_RX2_P	RX7_P		
BC30_RD6N	P32_ISG8_RX3_N	RX8_P		
BC30_RD6P	P32_ISG8_RX3_P	RX8_N		
BC30_RD7N	P32_ISG8_RX4_N	RX6_N		
BC30_RD7P	P32_ISG8_RX4_P	RX6_P		
BC30_RD1P	P32_ISG8_RX5_N	RX4_N		
BC30_RD1N	P32_ISG8_RX5_P	RX4_P		
BC30_RD3P	P32_ISG8_RX6_N	RX1_N		
BC30_RD3N	P32_ISG8_RX6_P	RX1_P		
BC30_RD0N	P32_ISG8_RX7_N	RX2_N		
BC30_RD0P	P32_ISG8_RX7_P	RX2_P		

Table 4-1 Switch Port MAPPING TABLE

4.3. 400G / 100G Interface

AS7900-32X is PHY-less system, BCM56980 connects with QSFP-DD directly and the CPU controls the transceiver's I2C and status via CPLD(s).

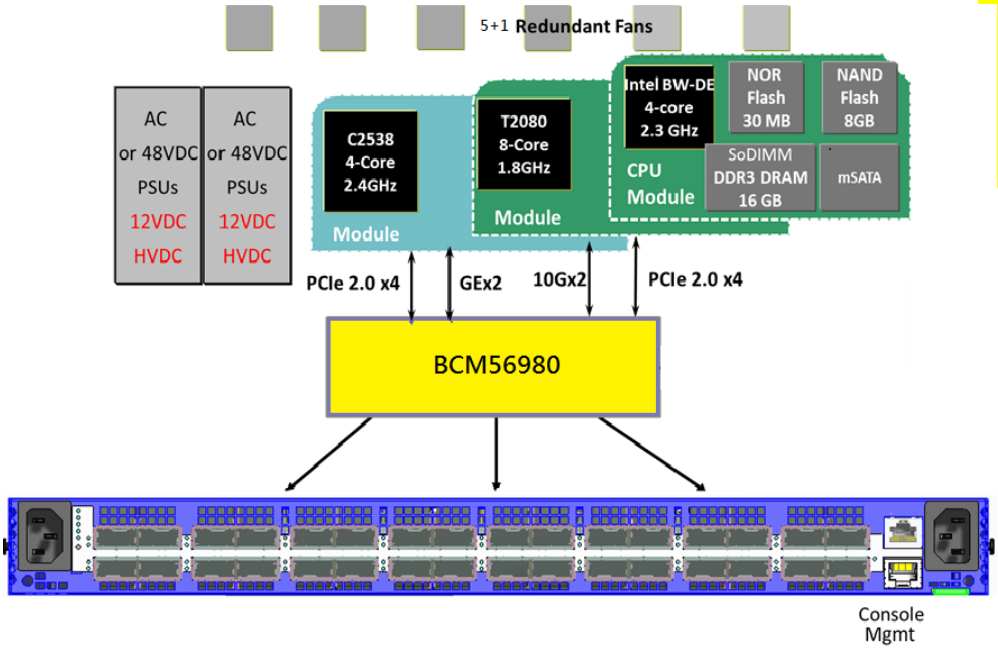


Figure 4-2 400G Interface Connection

4.4. LED interface

The BCM56980's three separate LED processors: LED-0, LED-1, LED-2, LED-3, LED-4,

- LED-0 provides port status for pipe 0, 1 (ports 1–64).
- LED-1 provides port status for pipe 2, 3 (ports 65–128).
- LED-2 provides port status for pipe 4, 5 (ports 129–192).
- LED-3 provides port status for pipe 6, 7 (ports 193–256).
- LED-4 provides port status for management ports (ports 257–259).

Port status information includes link status, transmit and receive activity, and speed settings.

4.4.1 LED timing diagrams

Figure 4-3 Single LED Refresh Cycle

4.5. QSFP-DD

The system has 32 QSFP-DD ports, QSFP-DD ports can support 400/100Gbps. The QSFP-DD ports support optical transceivers and DAC. The power class can support up to 14W.

5. Sub-system

5.1. Management PHY (BCM54616S)

The management port support 10/ 100/ 1000M Ethernet speed.

5.1.1. Configurations of PHY (BCM54616S)

Pin Number	Pin Name	Function Description
G7 G6 H6 G10	LED1 LED2 LED3 LED4	LED1 High >> Copper AN enable LED2 High >> Full-duplex LED3 High >> LED4 High >> AN at 10/100/1000BASE-T
F5 H5	MODE_SEL_0 MODE_SEL_1	MODE_SEL[1:0] * 01 RGMII (2.5V) 10 RGMII (HSTL1.8V) 11 RGMII (3.3V) 00 RGMII (3.3V)
H10 J0 J9 K10 K9	PHY_ADDR_0 PHY_ADDR_1 PHY_ADDR_2 PHY_ADDR_3 PHY_ADDR_4	ADDR = 00001

5.1.2. POR of PHY (BCM54616S)

The detailed power-on reset (POR) flow is as follows:

1. 3.3V up and Ref clock up
2. 3.3V enable MPS1484 to generate 2.5V
3. All powers are stable, POWR607 inform CPLD
4. CPLD receive the signal, CPLD assert Reset_N high

5.2. I2C

The CPU has one I2C channels for our application. The I2C used for system peripheral access include SODIMM, RTC and DC/DC. The I2C_0 and I2C_1 are for Mainboard function used.

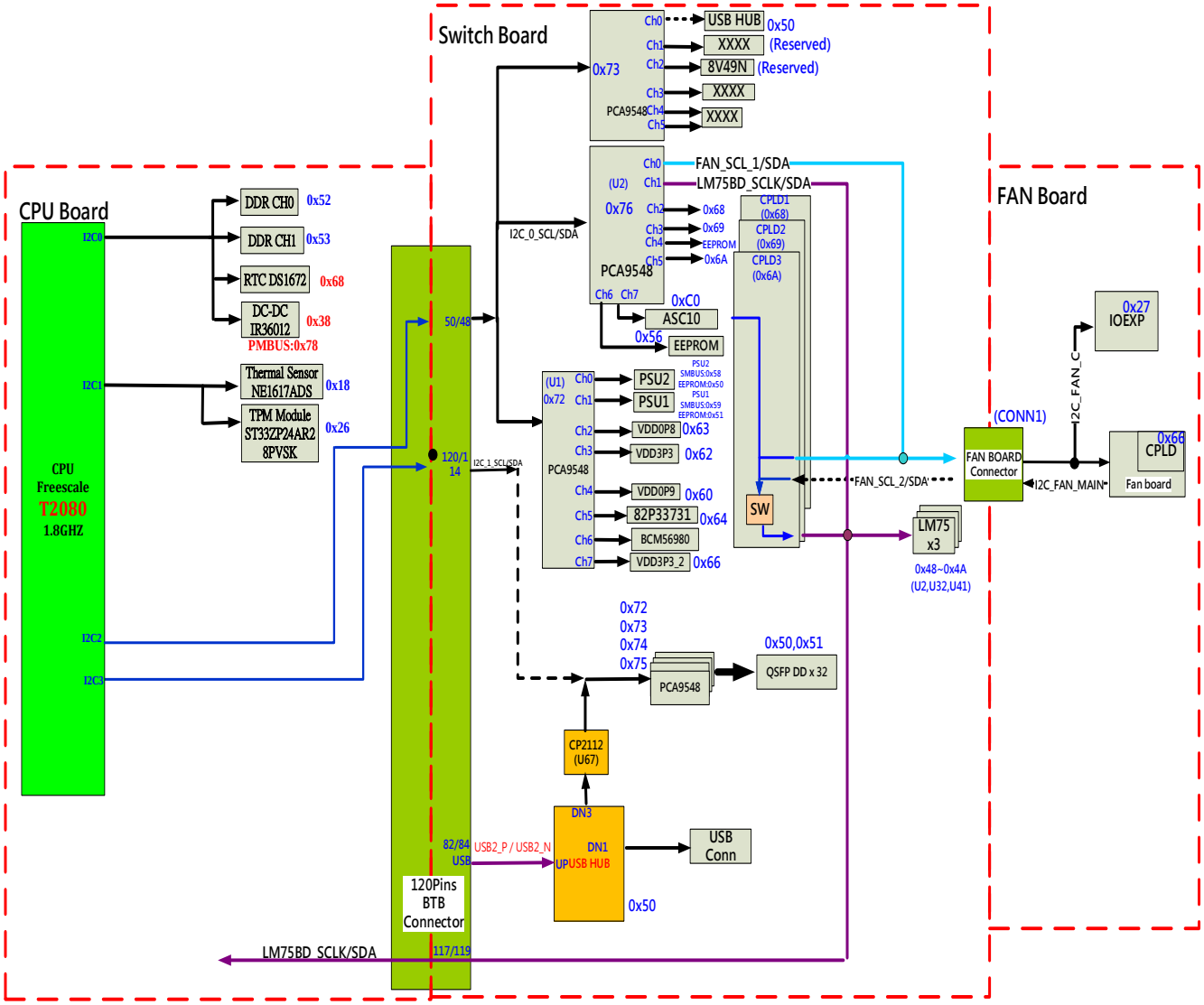


Figure 5-1 I2C Connection

	Channel	Device	Address
CPU	I2C_CH0	SODIMM SPD EEPROM	0x52
		SODIMM SPD EEPROM	0x53
		DS1672 (RTC)	0x68
		DC/DC IR36021	0X38
	I2C_CH1	NE1617EDS (Thermal)	0x18
		TPM module	0x13
	I2C_CH2	I2C switch (72)	0x72
		I2C switch (73)	0x73
		I2C switch (76)	0x76
	I2C_CH3	I2C switch (72)	0x72
		I2C switch (73)	0x73
		I2C switch (74)	0x74
		I2C switch (75)	0x75
I2C switch (72)	I2C_0_CH0	PWR module2	58 50
	I2C_0_CH1	PWR module1	59, 51
	I2C_0_CH2	TPS53641_VDD0P8-U33	0x63
	I2C_0_CH3	TPS53641_VDD3P3-U8	0x62
	I2C_0_CH4	ISL68127_VDD0P9-U4	0x60
	I2C_0_CH5	82P33731-U37	0x64
	I2C_0_CH6	BCM56980	
	I2C_0_CH7	TPS53641_VDD3P3_U6	66
I2C switch (73)	I2C_0_CH0	USB-Hub (Reserved)	0x50
	I2C_0_CH1	(Reserved)	
	I2C_0_CH2	8V49N (Reserved)	
I2C switch (76)	I2C_0_CH0	Fan	0x66
	I2C_0_CH1	LM75	48,49,4A
	I2C_0_CH2	CPLD1	0x68
	I2C_0_CH3	CPLD2	0x69
	I2C_0_CH4	EEPROM	
	I2C_0_CH5	CPLD3	0x6A

	I2C_0_CH6	EEPROM	0x56
	I2C_0_CH7	ASC_10	0xC0
I2C switch (72)	I2C_1_CH0	QSFP-DD Port 1	50, 51
	I2C_1_CH1	QSFP-DD Port 2	50, 51
	I2C_1_CH2	QSFP-DD Port 3	50, 51
	I2C_1_CH3	QSFP-DD Port 4	50, 51
	I2C_1_CH4	QSFP-DD Port 5	50, 51
	I2C_1_CH5	QSFP-DD Port 6	50, 51
	I2C_1_CH6	QSFP-DD Port 7	50, 51
	I2C_1_CH7	QSFP-DD Port 8	50, 51
I2C switch (73)	I2C_CH0	QSFP-DD Port 9	50, 51
	I2C_CH1	QSFP-DD Port 10	50, 51
	I2C_CH2	QSFP-DD Port 11	50, 51
	I2C_CH3	QSFP-DD Port 12	50, 51
	I2C_CH4	QSFP-DD Port 13	50, 51
	I2C_CH5	QSFP-DD Port 14	50, 51
	I2C_CH6	QSFP-DD Port 15	50, 51
	I2C_CH7	QSFP-DD Port 16	50, 51
I2C switch (74)	I2C_CH0	QSFP-DD Port 17	50, 51
	I2C_CH1	QSFP-DD Port 18	50, 51
	I2C_CH2	QSFP-DD Port 19	50, 51
	I2C_CH3	QSFP-DD Port 20	50, 51
	I2C_CH4	QSFP-DD Port 21	50, 51
	I2C_CH5	QSFP-DD Port 22	50, 51
	I2C_CH6	QSFP-DD Port 23	50, 51
	I2C_CH7	QSFP-DD Port 24	50, 51
I2C switch (75)	I2C_CH0	QSFP-DD Port 25	50, 51
	I2C_CH1	QSFP-DD Port 26	50, 51
	I2C_CH2	QSFP-DD Port 27	50, 51
	I2C_CH3	QSFP-DD Port 28	50, 51
	I2C_CH4	QSFP-DD Port 29	50, 51
	I2C_CH5	QSFP-DD Port 30	50, 51

	I2C_CH6	QSFP-DD Port 31	50, 51
	I2C_CH7	QSFP-DD Port 32	50, 51

Table 5- 1 I2C Address Table

5.3. UART

The UART port will be configured to enable UART1 only and support RJ45 type.

The console port interface conforms to the RJ45 electrical specification.

The console port is located on the front panel. The interface supports asynchronous mode with default eight data bits, one stop bit, and no parity. The unit will operate at the following baud rates:

- 9600, 19200, 38400, 57600, **115200 (Default)**

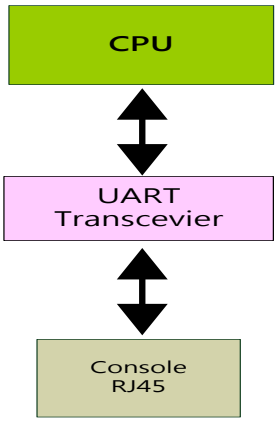


Figure 5-2 UART Connection

Pin number	Pin name	Pin number	Pin name
1	RTS	**2**	UART_TXD
3		**4**	
5	GND	**6**	UART_RxD
7		**8**	CTS

Table 5- 2 RS-232 Pin definition (RJ45)

CPU's UART		
Item	**Interface**	**Remark**
1	UART1	External RJ45 Console port

Table 5- 3 CPU UART Connection

5.4. USB

C2538 provides two USB ports. In this design we connect them for external type A USB connector and internal eUSB storage (USB to NAND Flash). The mapping table and connection are as below.

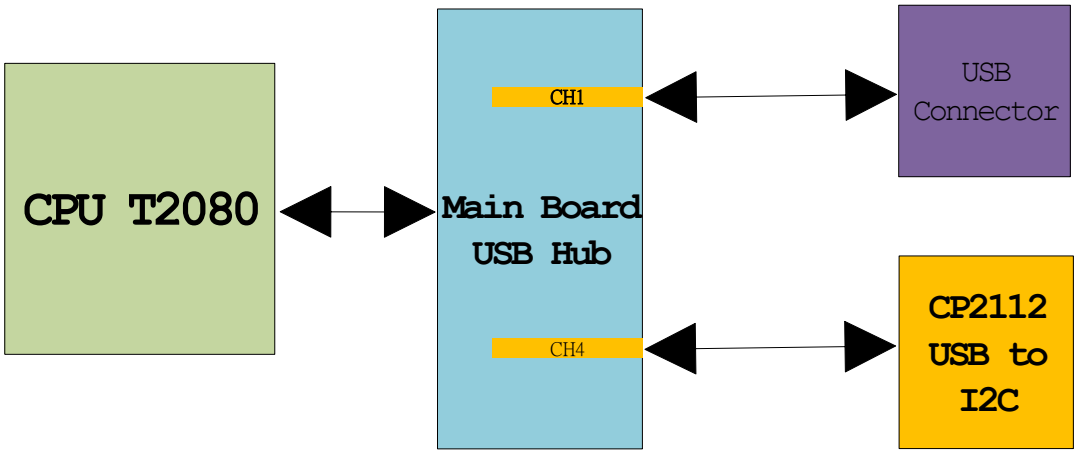


Figure 5-3 USB Connection

Pin Name of T2080	Function	Connection
USB1_UDM	USB1 data plus	Type A USB
USB1_UDP	USB1 data minus	
USB2_UDM	USB2 data plus	Do not install
USB2_UDP	USB2 data minus	

Table 5- 4 USB MAPPING TABLE

5.5. Interrupt

Pin Number	Pin Name	Function Description
U5.T48	CPLD2_INT_L	For CPLD interrupt
U5.T58	CPLD_INT_L	For CPLD interrupt

Table 5- 5 Interrupt MAPPING TABLE

CPLD1 in Switch board will collect all interrupts in Switch board from different devices, and then pass to CPU. Those devices are as below.

- MAC (BCM56980)
- CPLD2/3
- Mgmt Phy(BCM54616S)
- Thermal sensor(LM75)
- Fan
- IDT 8V89307
- PCIe

CPLD2/3 in Switch board will collect all interrupts from 32 * QSFP-DD Transceivers

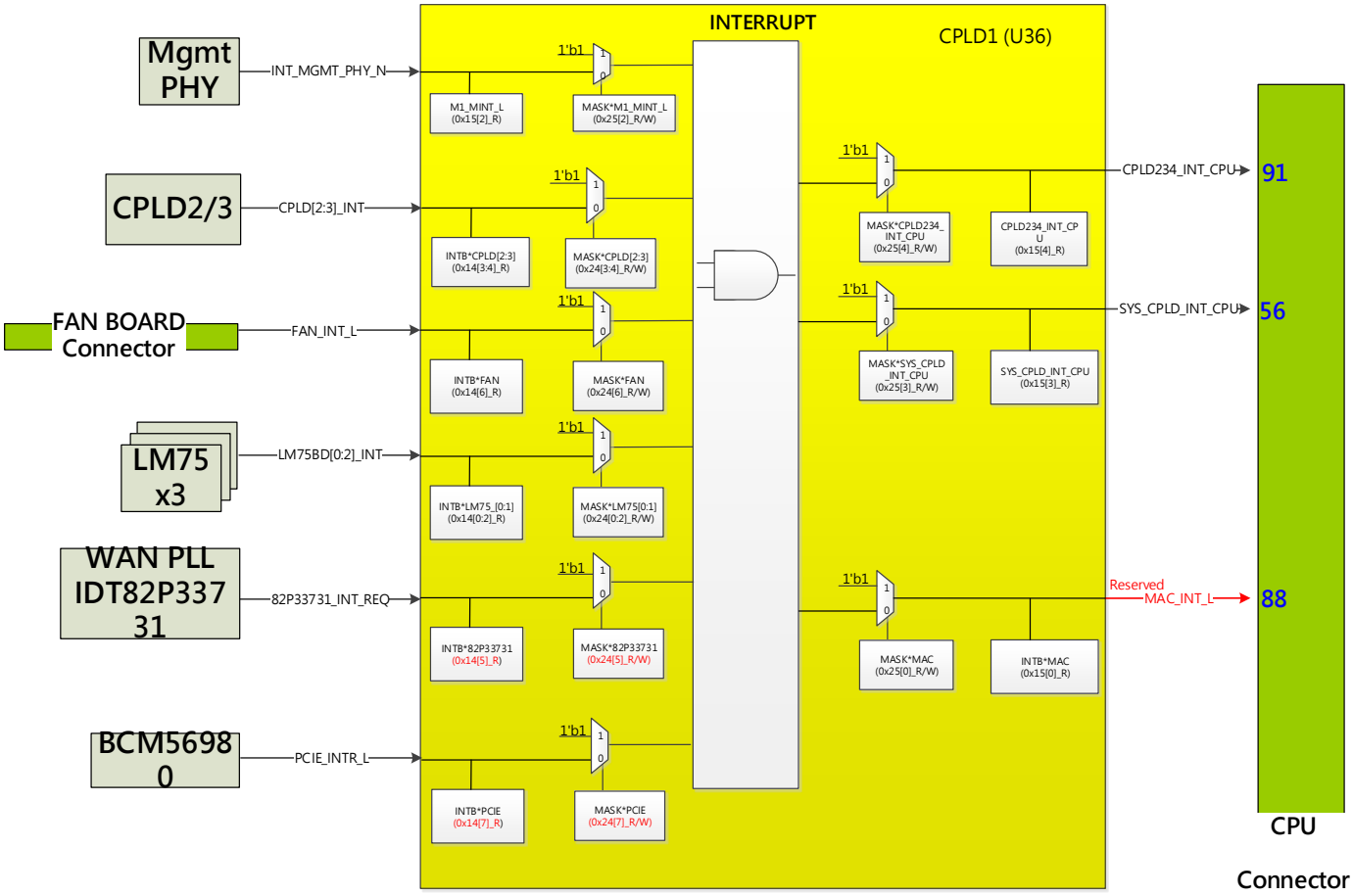


Figure 5-4 Interrupt Connection

5.6. JTAG

AS7900-32X has only one JTAG download chain for three CPLD with JTAG interface, it make the CPLD programing more quickly. The TCK and TMS pass to all devices by buffer. TDI and TDI are connecting directly.

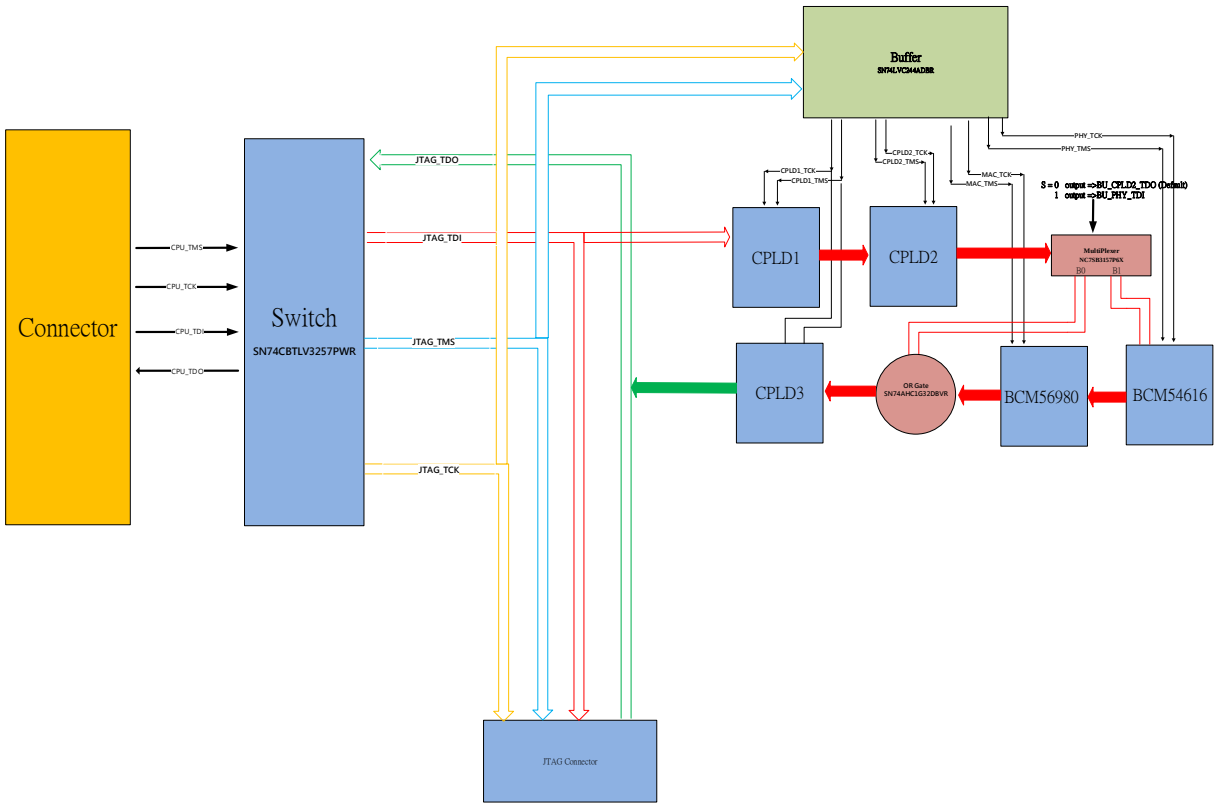


Figure 5-5 JTAG chain

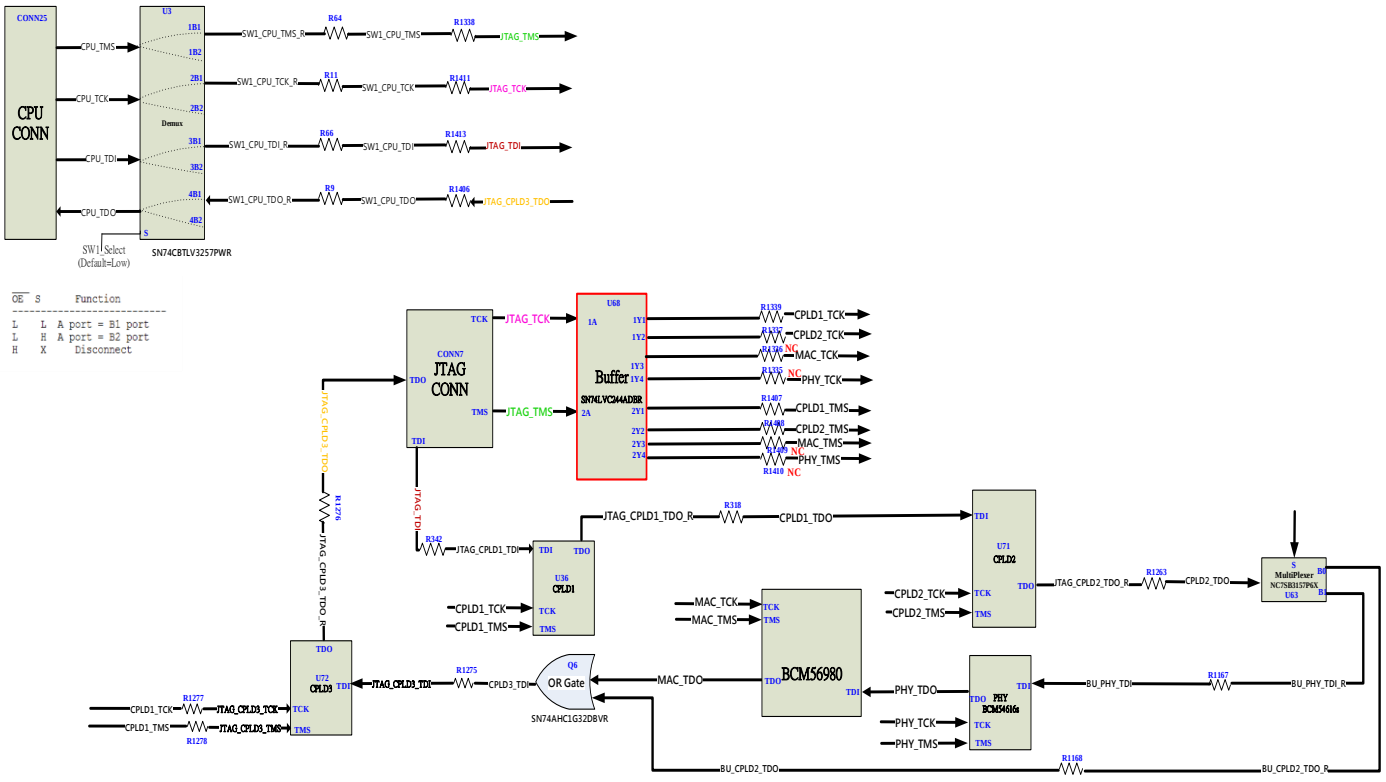


Figure 5-6 JTAG chain

5.7. Thermal system

5.7.1. Temperature sensor

There are three temperature sensors(U2,U32,U41) in AS7900-32X system, and the locations are as in the picture below. The CPU can access the sensor via I2C interface, and the sensor has the interrupt signal connect with CPLD for over-temp event application.

The temp sensor solution is “LIN LM75BD 2.8-5.5V TEMP MINOTOR SO8 LT/LF NXP”

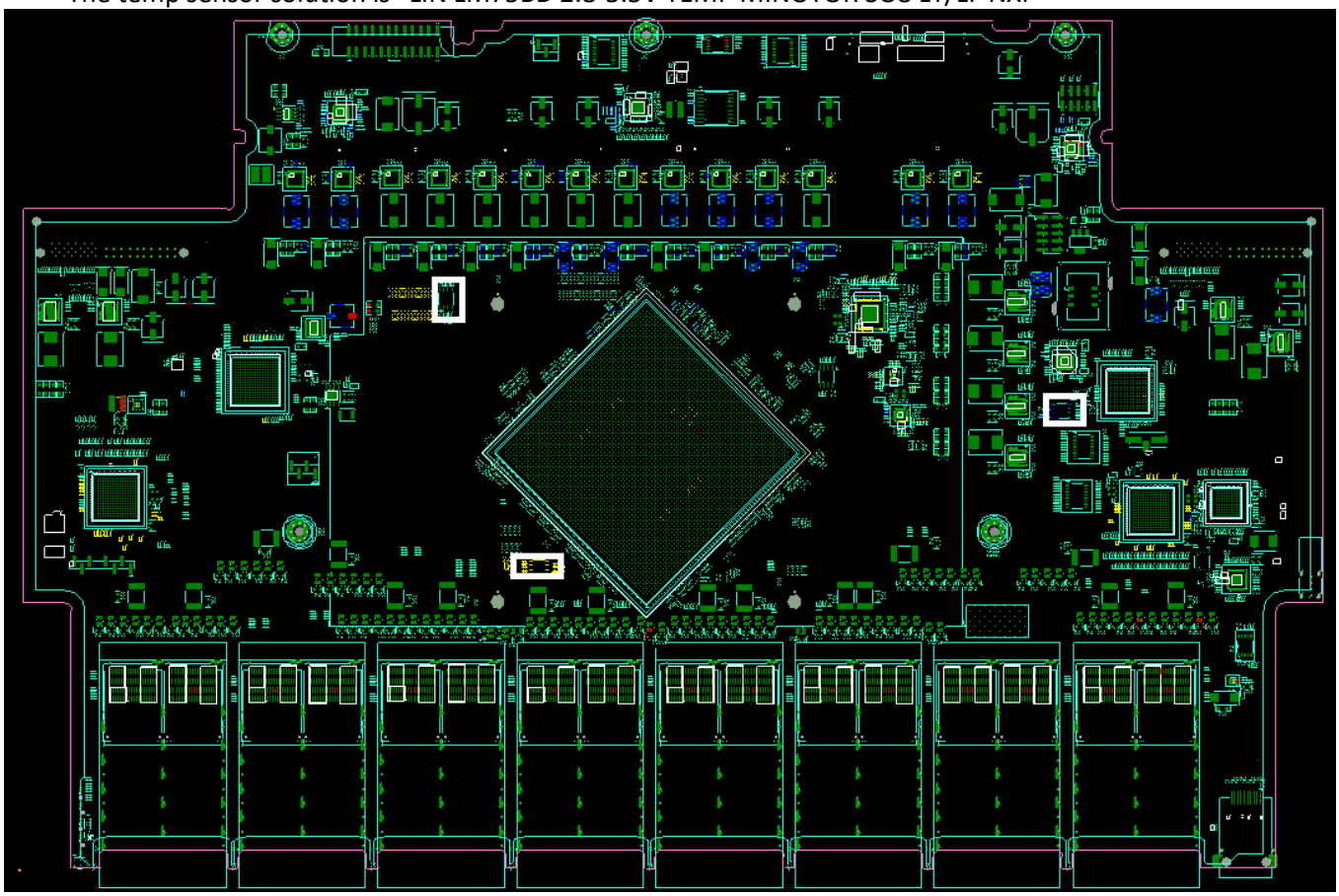


Figure 5-7 Switch board - Temp sensor location

Top

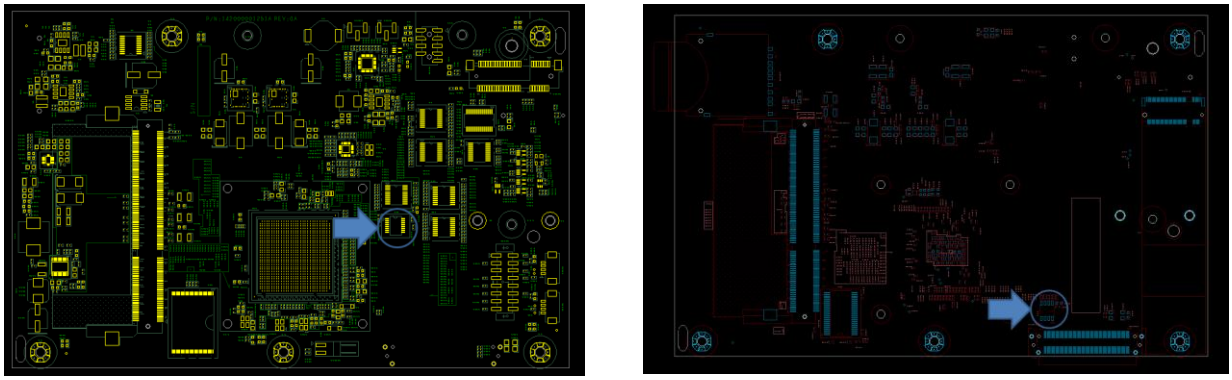


Figure 5-8 CPU board - Temp sensor location

5.7.2 Fan controller system

5.7.3 Fan PCB

The Fan PCB is 4 layers and provides the power, management and connectivity for the 5 system fan modules. The Fan PCB connects to the Main Switch PCB via a small cable assembly for power and a small cable assembly for management signals.

The Fan board has a CPLD to do the fan controller function. The CPLD on the Fan board can control the Fan's PWM signal for adjust Fan speed and count the Fan's Tach signal for Fan speed reporting. CPU can read the thermal sensor to get thermal information, and then adjust Fan speed to reduce system's thermal. The Fan's CPLD had included I2C thermal watchdog to avoid system shutdown. If the register count to zero, the Fan speed will be set to high speed.

5.7.4 Fan PCB Dimensions

	Inches	Millimeters
Length	9.54	242.5
Width	2.40	60.9

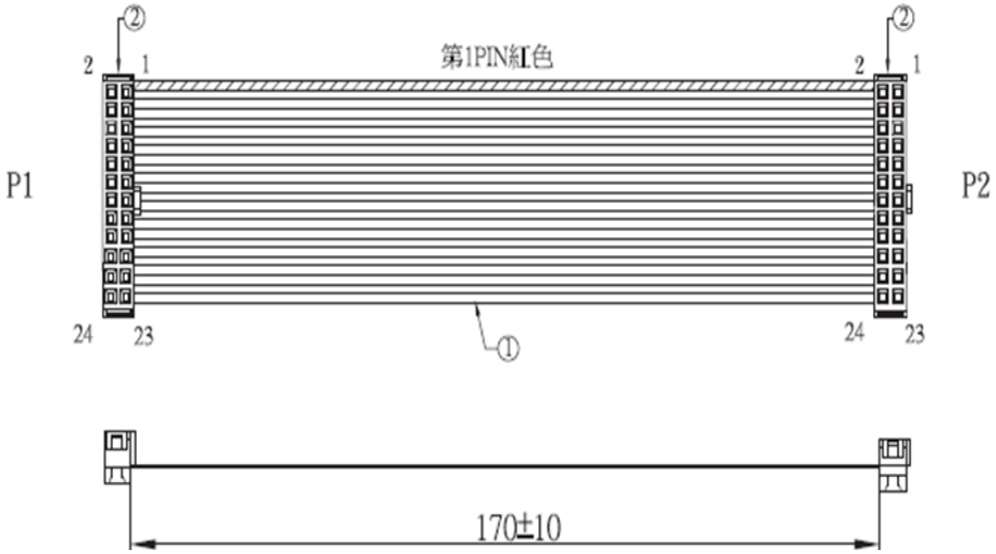
5.7.5 Fan PCB major components

Description	Manufacturer	Part Number
B2B Connector	DONG-WEI	BHE6T0-224S4
CPLD	Altera	5M1270ZF256C5N 3.3V

5.7.6 Fan PCB connector pinout

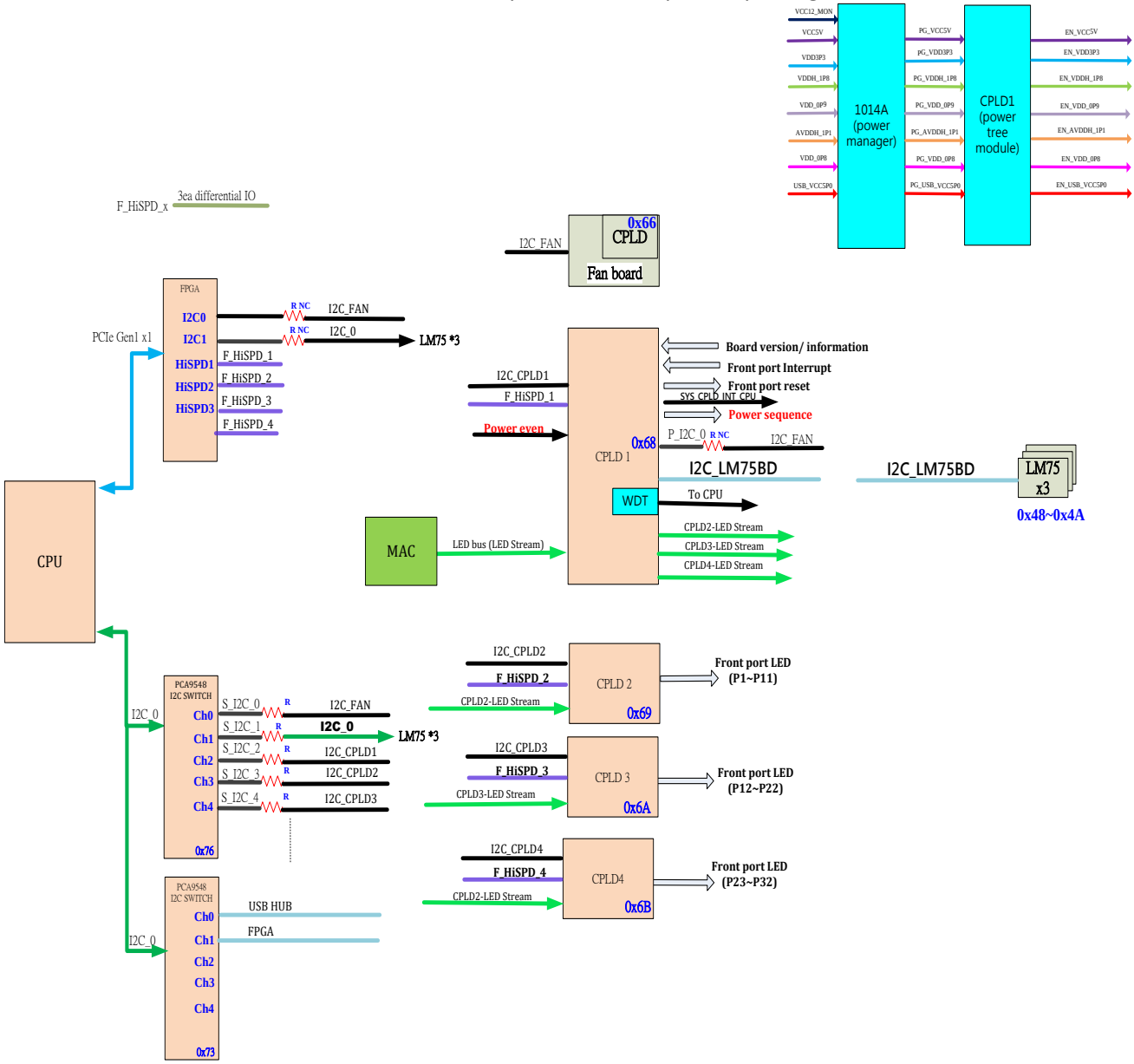
Name	Type	Net Name	Description
1	power	VCC12	12V Power
2	power	VCC12	12V Power
3	power	VCC12	12V Power
4	power	VCC12	12V Power
5	power	GND	12V/ 3.3V return
6	power	GND	12V/ 3.3V return
7	power	GND	12V/ 3.3V return
8	power	VDD3P3	3.3V Power
9	out	FAN_IDLE	Enable/ disable the Fan baord's I2C Master
10	in	FAN_INT_L	Fan board send intrupt
11	power	GND	12V/ 3.3V return
12	power	GND	12V/ 3.3V return
13	in	FAN_SCL_2	For Fan CPLD access switch board's thermal sensor
14	inout	FAN_SDA_1	For CPU to access Fan CPLD status
15	inout	FAN_SDA_2	For Fan CPLD access switch board's thermal sensor
16	out	FAN_SCL_1	For CPU to access Fan CPLD status
17	power	GND	12V/ 3.3V return
18	power	GND	12V/ 3.3V return
19	power	GND	12V/ 3.3V return
20	power	GND	12V/ 3.3V return
21	power	VCC12	12V Power
22	power	VCC12	12V Power
23	power	VCC12	12V Power
24	power	VCC12	12V Power

5.7.7 Fan Cable Pinout



5.8. CPLD

The Switch has three CPLDs for LED decoding, power module status, I2C switch, and System interrupt. Fan board has one CPLD for Fan direction, Speed control, Speed reporting…etc.



CPLD1 is LCMXO3LF-4300C-5BG324C

CPLD2/CPLD3/CPLD4 are LCMXO3L-1300C-5BG256C

CPLD Field upgrade information

The system support CPLD field upgraded function for main CPLD and Fan CPLD.

5.8.1.1. JTAG connection

- Main board
  - Main board CPLD have three CPLD devices; CPLD1, CPLD2 and CPLD3. The updater can update three CPLD devices in same time. CPU connects with CPLD's Jtag interface via CPU GPIO pin, and there has a JTAG chain in CPLD1, 2 and3.

- Fan board
  - Fan board has one CPLD device. The CPU connects with Fan CPLD JTAG interface via I2C expander IC. CPU use I2C expander to simulate JTAG signal for CPLD code update.

5.8.1.2. Upgrade procedure

In uboot, use the "run onie_rescue" command to enter ONIE.

LOADER=> run onie_rescue

Command for main board CPLD upgrade:

”TFTP_server_IP” : It is the IP address of TFTP server

”file_name.updater” : It is the file name of new CPLD image updater

ONIE: / # update_url tftp://”TFTP_server_IP”/”file_name.updater”

5.8.1.3. Operational mode

The real-time ISP feature present in the Max V family is used for upgrade CPLD code.

5.8.1.4. Power cycling requirements

The system needs a power cycle after finish CPLD code update. It will run original CPLD code before power cycle.

5.8.1.6 CPLD Programming tool

Lattice CPLD programming tools can be used to initially program the CPLDs. See below for additional information.

http://www.latticesemi.com/en/Support/Licensing.aspx#diamond

file:///C:/Users/Jeff/AppData/Local/Packages/Microsoft.MicrosoftEdge_8wekyb3d8bbwe/TempState/Downloads/ProgrammingCableUsersGuide.pdf

5.9. IDT 82P33731

5.9.1. Configurations of IDT 82P33731

Pin Number	Pin Name	Function Description
B11 C11	MPU_MODE1/ I2CM_SCL MPU_MODE0/ I2CM_SDA	During reset, these pins determine the default value of the MPU_SEL_CNFG[1:0] bits as follows: 00: I2C mode 01 ~ 10: Reserved 11: I2C master (EEPROM) mode I2CM_SCL: Serial Clock Line In I2C master mode, the serial clock is output on this pin. I2CM_SDA: Serial Data Input for I2C Master Mode In I2C master mode, this pin is used as the for the serial data.
K8	MS/SL	MS/SL: Master / Slave Selection This pin, together with the MS_SL_CTRL bit, controls whether the device is configured as the Master or as the Slave. The signal level on this pin is reflected by the MASTER_SLAVE bit.
H1 J1 J2	XO_FREQ0/ LOS0 XO_FREQ1/ LOS1 XO_FREQ2/ LOS2	XO_FREQ0 ~ XO_FREQ2: These pins set the oscillator frequency. XO_FREQ[2:0] Oscillator Frequency (MHz) 000 10.000 001 12.800 010 13.000 011 19.440 100 20.000 101 24.576 110 25.000 111 30.720 LOS0 ~ LOS2 - These pins are used to disqualify input clocks. See input clocks section for more details. After reset, this pin takes on the operation of LOS0-LOS2

Table 1. 82P33731 Configurations

5.9.2. POR of IDT 82P33731

The detailed power-on reset (POR) flow is as follows:

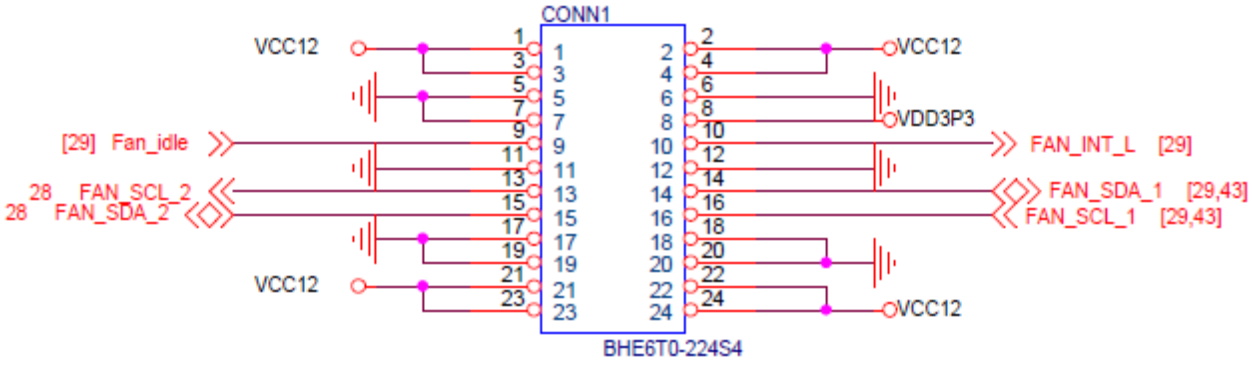
1. 3.3V up and Ref clock up
2. Then 3.3V enable AZ1117 to generate 1.8V
3. All power are stable, POWR1014 inform CPLD
4. CPLD receive the signal, CPLD assert Reset_N high

5.10 Connector

5.11 CPU Connector

ES7632BT R0C 120 Pin	CONNECTOR					ES7632BT R0C 120 Pin
		PIN #		PIN #		
LM75BD_SCLK	IN	119		120	-	GND
LM75BD_SDA	IN/OUT	117		118	OUT	CPU_XFI_EC_TX_0P
GND	-	115		116	OUT	CPU_XFI_EC_TX_0N
CPU_MPHY_SGMII_TX_0_S_P	OUT	113		114	-	GND
CPU_MPHY_SGMII_TX_0_S_N	OUT	111		112	-	GND
GND	-	109		110	IN	CPU_XFI_EC_RX_0P
MPHY_CPU_SGMII_RX_0_S_N	IN	107		108	IN	CPU_XFI_EC_RX_0N
MPHY_CPU_SGMII_RX_0_S_P	IN	105		106	-	GND
GND	-	103		104	-	GND
CPU_MPHY_MDC	OUT	101		102	OUT	CPU_XFI_EC_RX_2P
GND	-	99		100	OUT	CPU_XFI_EC_RX_2N
CPU_MPHY_MDIO	IN/OUT	97		98	-	GND
GND	-	95		96	-	GND
IP_UART0_SOUT	IN	93		94	IN	CPU_XFI_EC_TX_2P
CPLD23_INT_CPU	IN	91		92	IN	CPU_XFI_EC_TX_2N
1PPS_CPU	IN	89		90	-	GND
I2C_1_SCL	OUT	87		88	-	GND
CPU_PROCHOT	OUT	85		86	-	GND
Not Used	-	83		84	IN/OUT	USB2_N
I2C_1_SDA	IN/OUT	81		82	IN/OUT	USB2_P
UART1_CTS	IN	79		80	-	GND
CPU_TDI	IN	77		78	OUT	UCD9090_ALERT_L
UART1_TX	OUT	75		76	OUT	UART1_RTS
MAC_INT_L	IN	73		74	OUT	RESET_SYS_CPLD
GND	-	71		72	OUT	CPU_TMS
PCIE_OOB_TX_P	OUT	69		70	OUT	CPU_JTAG_RST
PCIE_OOB_TX_N	OUT	67		68	IN	P1014_RST
GND	-	65		66	OUT	CPU_TDO
UART1_RX	IN	63		64	OUT	CPU_TCK
GND	-	61		62	OUT	IP_UART0_SIN
PCIE_OOB_RX_P	IN	59		60	-	Not Used
PCIE_OOB_RX_N	IN	57		58	-	Not Used
GND	-	55		56	IN	SYS_CPLD_INT_CPU
GND	-	53		54	IN	USB1_PWRFAULT
CPU_PEX_PCIEA_TX_0_P	OUT	51		52	IN	Manu_RST
CPU_PEX_PCIEA_TX_0_N	OUT	49		50	OUT	I2C_0_SCL
GND	-	47		48	IN/OUT	I2C_0_SDA
GND	-	45		46	IN	RESET_LOCK
CPU_PEX_PCIEA_TX_1_N	OUT	43		44	OUT	CPU_THERMALTRIP
CPU_PEX_PCIEA_TX_1_P	OUT	41		42	OUT	USB1_VBUS
GND	-	39		40	-	GND
GND	-	37		38	-	GND
PEX_CPU_PCIEA_RX_0_N	IN	35		36	OUT	CPU_PEX_PCIEB_TX_0_P
PEX_CPU_PCIEA_RX_0_P	IN	33		34	OUT	CPU_PEX_PCIEB_TX_0_N
GND	-	31		32	-	GND
GND	-	29		30	-	GND
PEX_CPU_PCIEA_RX_1_N	IN	27		28	IN	PEX_CPU_PCIEB_RX_0_P
PEX_CPU_PCIEA_RX_1_P	IN	25		26	IN	PEX_CPU_PCIEB_RX_0_N
GND	-	23		24	-	GND
GND	-	21		22	-	GND
CPU_PEX_PCIEB_TX_1_N	OUT	19		20	IN	PEX_CPU_PCIEB_RX_1_P
CPU_PEX_PCIEB_TX_1_P	OUT	17		18	IN	PEX_CPU_PCIEB_RX_1_N
GND	-	15		16	-	GND
GND	-	13		14	-	GND
GND	-	11		12	-	GND
VCC12	-	9		10	-	VCC12
VCC12	-	7		8	-	VCC12
VCC5P0	-	5		6	-	VCC12
VCC5P0	-	3		4	-	VCC12
VCC5P0	-	1		2	-	VCC12

5.12 Connector for Fan board



6. Power Consumption

The total estimated power budget described in Table 2 is around ~1100 on this switchboard with CPU system.

All calculating data are based on the maximum power dissipation in the spec of components. The actual power draw of the system will be less than the maximum outlined in the table below.

TOR switch power consumption:

	Component	Upper Power		12V	12V	12V	3.3Vstb	12V	VDD3V3			12V			
		Description		(USB_VCC5P0)	(VCC5V)		(VDD1P2_PHY) : LDO 3.3Vstb=>1.2V/ 0.2A	VDD3P3	1.8V Analog (VDD_1P8)	VDD1P2	ROV, Core VDD (VDD_0P9) 0.88V~0.96V	(VDD_0P8)	Watt	Q'ty	Total Watt
			12	5	5	3.3	1.2	3.3	1.8	1.2	0.9	0.8			
CPU Board	CPU Module	Intel C2538	4.25										51.00	0	0.00
		Intel T2080	4.00										48.00	0	0.00
		Broadwell DE	7.67		0.50								94.48	1	94.48
Main Board	MAC	BCM56980													
	QSFP DD	400G transceiver						3.64					12.00	32	383.99
	BCM54616S	PHY				0.20	0.20						0.90	1	0.90
	CPLD1					0.16							0.53	1	0.53
	CPLD2~4							0.16					0.53	3	1.58
	USB	USB Device		1.00									5.00	1	5.00
	LEDs			0.010									0.05	389	19.45
	P1014A	Power Monitor				0.10						0.00	0.33	1	0.33
	TI Power (MOS)				0.0001	0.0001						0.00	0.00	12	0.01
	OCXO				0.10								0.50	2	1.00
Fan Board	FAN		2.80										33.60	6	201.60
	CPLD							0.10					0.33	1	0.33
	Others							1.00					3.30	1	3.30
	Sub-Power					0.20		0.67						1	
		Total Current	24.47	4.89	0.70	0.66	0.20	118.91	0.29	5.38	396.00	80.00			
		Efficiency 90%													

Table 6-1 Power Consumption Table

7. PSU

The system supports 4 kinds of power module.

AC power (Air direction : Front to back; red color panel)
AC power (Air direction : Back to front; blue color panel)
DC Power (Air direction : Front to back; red color panel)
DC input Power (Air direction : Front to back; blue color panel)

Those are for difference application; the fan direction is front to back or back to front, the AC/DC Power or DC/DC power.

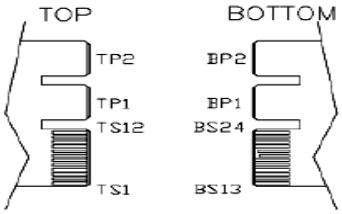
The AC/DC and DC/DC power are only different between power input; the output voltage SPEC is the same. The AC/DC power is 90~240Vac input, and DC/DC power is 36~72Vdc input. The power supply can support load sharing function.

PSU	Remarks	Vendor
131700000307A(FSH082-610G)	AFO	Acbel
131700000314A(FSH095-610G)	AFI	Acbel
131700000301A(YESM1300AM-2A01P10)	AFO	3Y
131700000328A(YESM1300AM-2R01P10)	AFI	3Y

7.1. Pinout

The power module output pin define is as below.

3.3. Pin assianment for DC output gold fingers



PIN NO.	CONDITION	PIN NO.	CONDITION
TS1	PDB_FAULT	BS13	+12VS+
TS2	PRESENT	BS14	+12VRS-
TS3	A0	BS15	12LS
TS4	PDB_ALERT	BS16	SMB_ALERT
TS5	AC-OK	BS17	SDA
TS6	Reserved	BS18	SCL
TS7	Reserved	BS19	PS-KILL
TS8	Reserved	BS20	PS_ON
TS9	Reserved	BS21	PW_OK
TS10	A2	BS22	A1
TS11	+5VSB	BS23	+5VSB
TS12	+5VSB	BS24	+5VSB
TP1	GND	BP1	+12V
TP2	GND	BP2	+12V
TOP		BOTTOM	

Figure 3: signal descriptions

7.2. Dimension

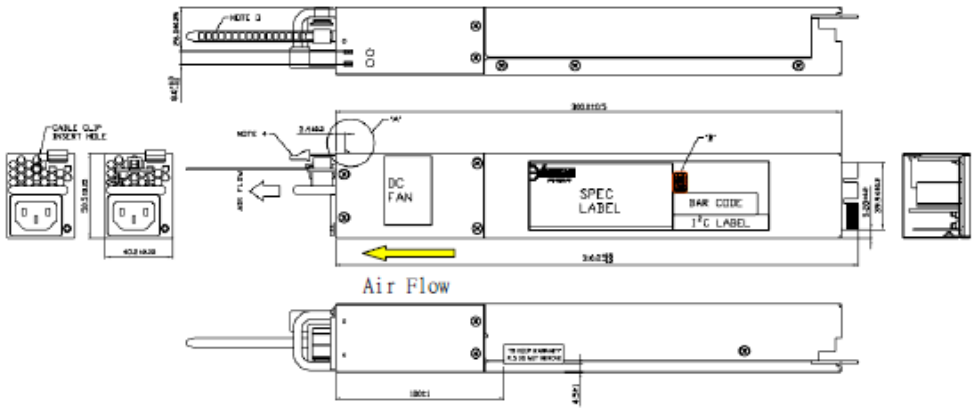
Nominal Dimensions

Height: 40mm

Width: 50.5mm

Depth: 310.2mm

The casing dimension is W 50.5 mm x L 310.2 mm x H 40 mm(including gold finger)



3.

Figure 2: Outline drawing

3.

Figure 7-1 PSU Dimension

7.3. Efficiency

The Efficiency should meet at least 80Plus Platinum rating, specified in the below table. The efficiency test condition should be 230VAC and with external fan power source or deduction of the power consumed by the fan at specified loading, according to 80Plus efficiency measurement specifications.

(80Plus Platinum) test at 230VAC with external fan instead of self fan module.

Input	10% load	20% load	50%load	100%load
230VAC	*	90%	94%	91%
115VAC	*	*	*	*

7.4. Power Supply Management Controller (PSMC)

The PSMC device in the power supply shall derive its power of the +5V or +3.3V on the system side of the Oring device and shall be grounded to return. It shall be compatible with SMBus specification 2.0 and PMBusTM Power System Management Protocol Specification Part I and Part II in Revision 1.1 or later. It shall be located at the address set by the A0 and A1 pins. Refer to the specification posted on www.ssiforum.org and www.pmbus.org website for details of the power supply monitoring interface requirements and refer to followed section of supported features. The below table reflect the power module addresses complying with the position in the power system.

PDB position and PSMC address	PM1 B0h/B1h	PM2 B2h/B3h
Pin A1/A0	0/0	0/1

PSMC Addressing

7.5. Power Supply Field Replacement Unit (FRU)

The power supply shall support electronic access of FRU information over an I2C bus. Five pins at the power supply connector are allocated for this. They are named SCL, SDA, A1, A0 and Write protect. SCL is serial clock. SDA is serial data. These two bidirectional signals from the basic communication lines over the I2C bus. A0and A1 are input address lines to the power supply. The backplane defines the state of these lines such that the address to the power supply is unique within the system. The resulting I2C address shall be per table below. The Write protection pin is to ensure that data will not accidentally overwritten.

The device used for this shall be powered from a 3.3V bias voltage derived from the 5VSB output . No pull-up resistors shall be on SCL or SDA inside the power supply.

EEPROM Addressing

PDB position and FRU address	PM1 A0h/A1h	PM2 A2h/A3h
Pin A1/A0	0/0	0/1

7.6. PSMC Sensors

Sensors shall be available to the PSMC for monitoring purpose. All Sensors shall continue to provide real time data as long as the PSMC device is powered. This means in standby and operation mode, while in standby the main output(s) of the power supply shall read zero Amps and Volts.

Sensor	Description
Vinput	Input Voltage
Iinput	Input Current
Pinput	Input Power
Voutput_main	Output Voltage main output
Ioutput_main	Output Current main output
Poutput_main	Output Power main output
Voutput_aux	Output Voltage auxiliary output
Ioutput_aux	Output Current auxiliary output
Poutput_aux	Output Power auxiliary output
Tcomp(TBD)	Component Temperature
Tenv	Environmental Temperature
RPMFan	Fan Speed reading
PDBfail	PDB fail protection

PSMC Sensor list

7.7. LEDs of Power Supply units

The power supply has Green/ Red led to show the power supply status.

The LED TYPE: YCG317-EGW(R+G) or equal.

Power supply status	Power supply LED color
No AC power to all PSU	OFF
Only +5V standby output on (AC OK)	1Hz Blinking Green
Power supply DC output ON and OK	Green
Power supply fail	Red
Fan fail	1Hz Blinking Red
Power supply warning	0.5Hz Blinking Red/Green *

NOTE: * Blinking frequency: (Red and Green on 0.5 Sec and off 0.5 Sec separately and sequentially in two seconds)

Figure 7-2 LEDs of Power Supply units

8. PCB

PCB information of stack-up, dimension and placement.

8.1. Stack-up

The Switch board PCB material is TU-933+ and it is the ultra-low loss material for High speed signal.

The PCB has 24 layers and power plane has 2oz for high current application.

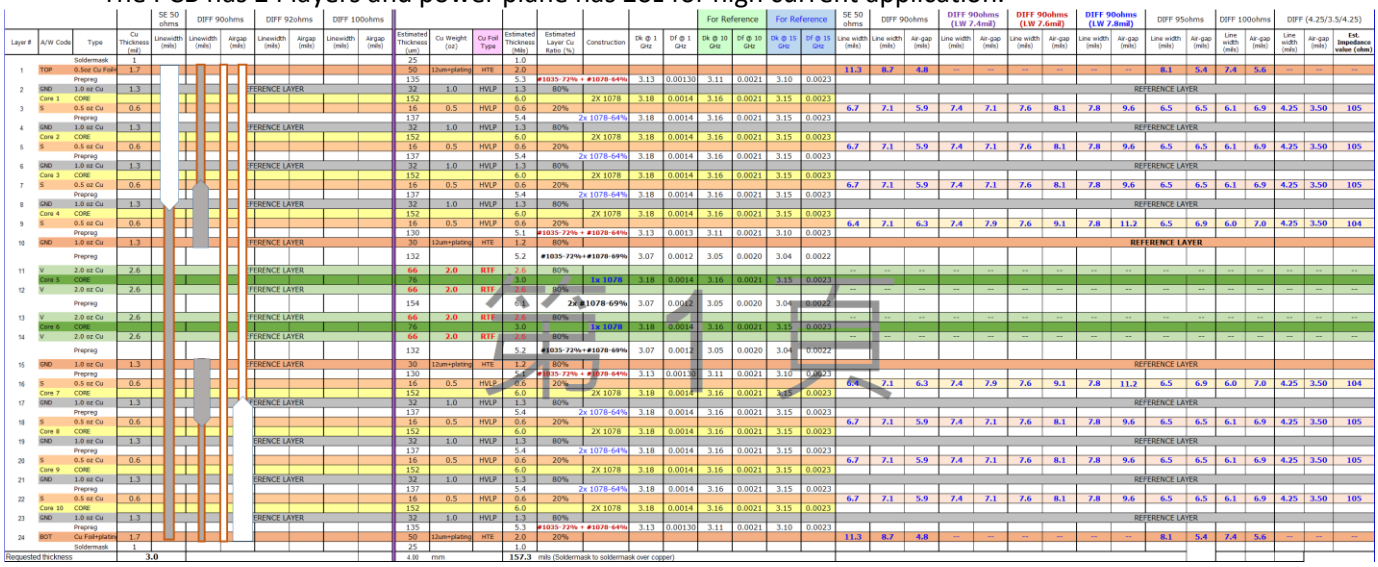


Figure 8-1 Switch board PCB Stackup

The CPU board PCB material is Tg150 and it is the low loss material for High speed signal. The PCB has 8 layers and power plane has 1oz for current application.

Date : 2015/1/7 09:08
P/N :
Layers : LAYER 8
Tg : TU 872
TU-872LK

Layer Name	Plane Description	Remain Copper (%)	Material	sheet	reduce after pressed	finish Thickness	tolerance	Er.	Single-end 50 Ω± 10% Impedance	Width	differential 85Ω± 10% Impedance	Width/Space	differential 90Ω± 10% Impedance	Width/Space	differential 100Ω± 10% Impedance	Width/Space	Ref.
	solder mask					0.5											
Layer1	Signal		Hoz Copper Foil+plating			1.7	min. 1.3		48.33	5	83.03	5.5/6.5	87.64	5/7	98.19	4/8	L02
	PREPREG		PREPREG	1		2.825	+/-1	3.45									
Layer2	POW/GND	86%	1oz		0.175	1.25											
	CORE		0.11	1		4	+/-1	3.65									
Layer3	Signal	50%	1oz		0.625	1.25			47.5	5	83.64	5.5/6.5	88.26	5/7	98.82	4/8	L02&L04
	PREPREG		PREPREG	2		7.6	+/-2	3.65									
Layer4	POW/GND	86%	1oz		0.175	1.25											
	CORE		1	1		36.87	+/-10%	3.8									
Layer5	POW/GND	86%	1oz		0.175	1.25											
	PREPREG		PREPREG	2		7.6	+/-2	3.65									
Layer6	Signal	50%	1oz		0.625	1.25			47.5	5	83.64	5.5/6.5	88.26	5/7	98.82	4/8	L05&L07
	CORE		0.11	1		4	+/-1	3.65									
Layer7	POW/GND	86%	1oz		0.175	1.25											
	PREPREG		PREPREG	1		2.825	+/-1	3.45									
LAYER 8	Signal		Hoz Copper Foil+plating			1.7	min. 1.3		48.33	5	83.03	5.5/6.5	87.64	5/7	98.19	4/8	L07
	solder mask					0.5											
Total Thickness= 1.97 mm					1.95	77.62											

unit : mil

Figure 8-2 CPU board PCB Stackup

8.2. Dimension

The Switch PCB dimension is 413 x 269 mm.

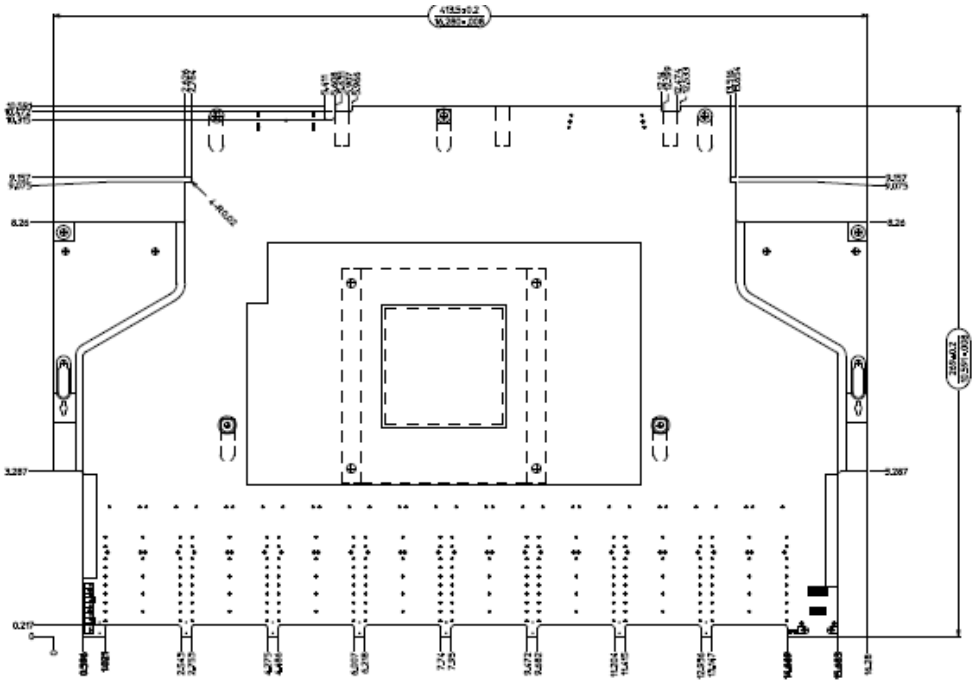


Figure 8-3 Switch board PCB Dimension

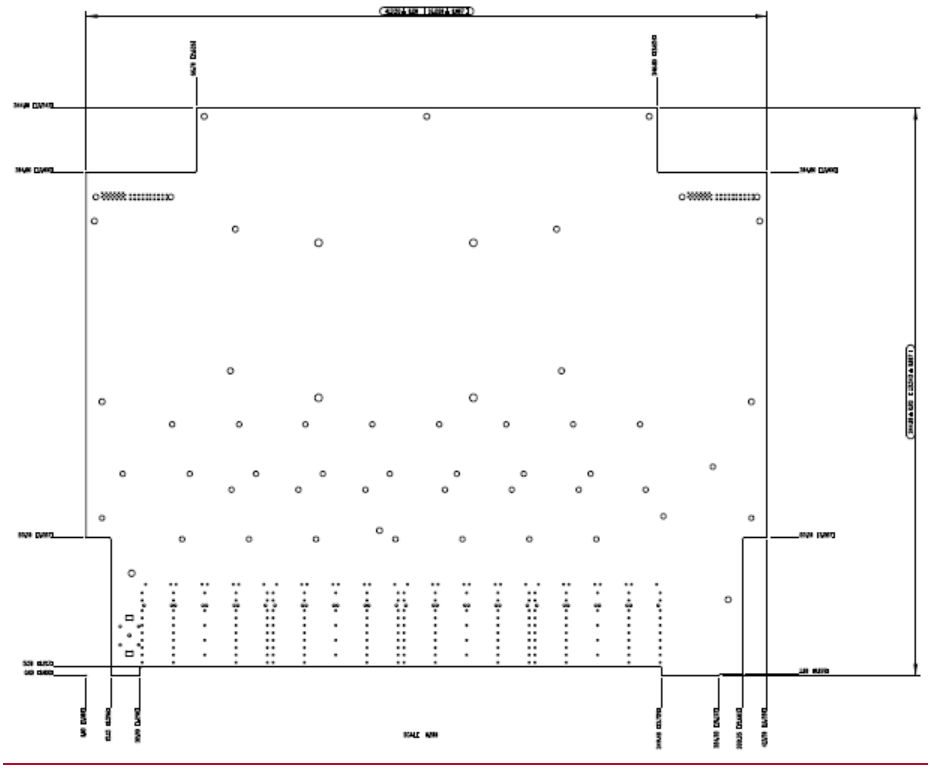
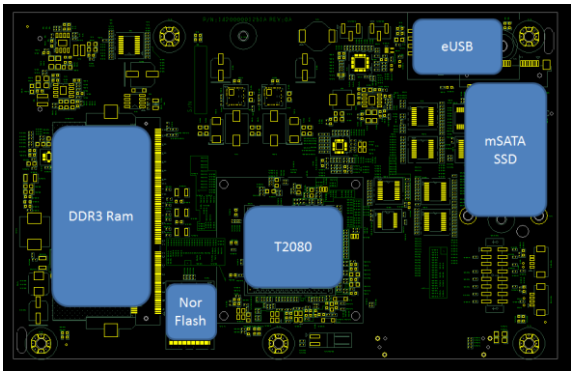


Figure 8-4 CPU board PCB Dimension

8.3. Placement

Top



Bottom

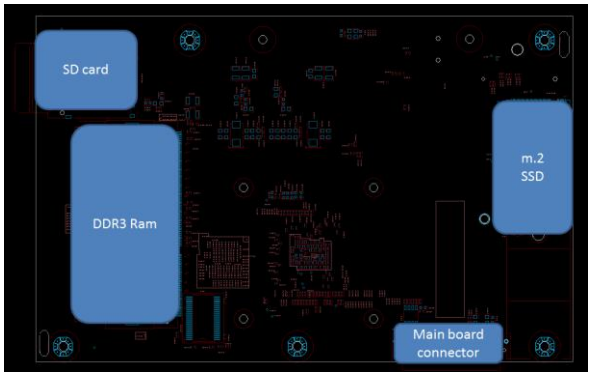
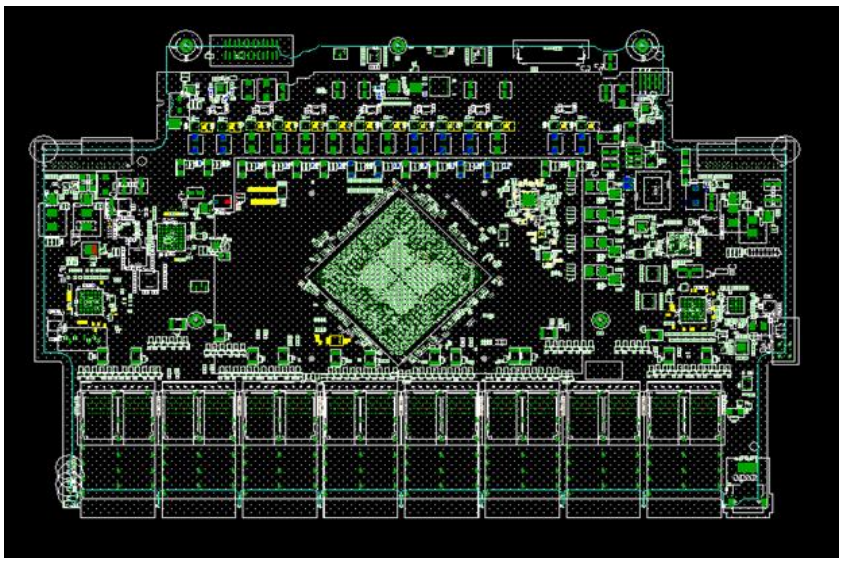


Figure 8-5 CPU board - PCB Placement

Top



Bottom

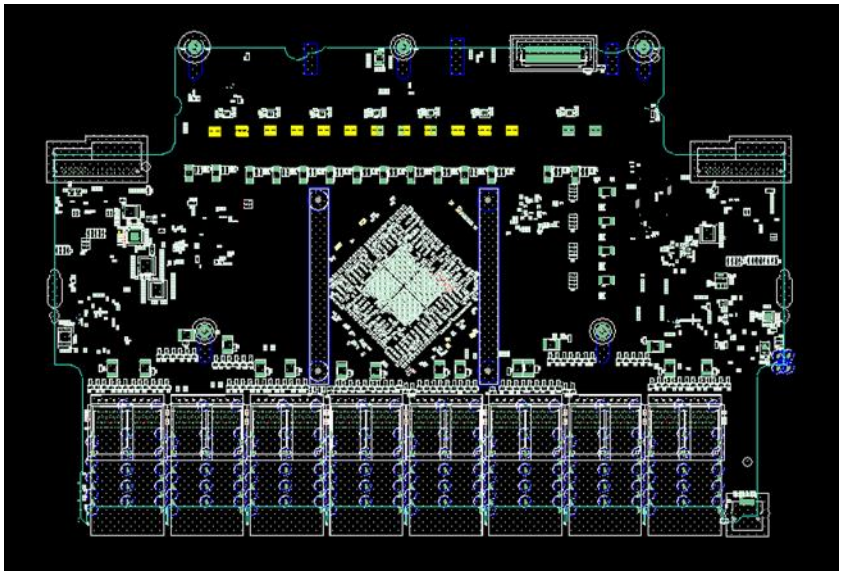
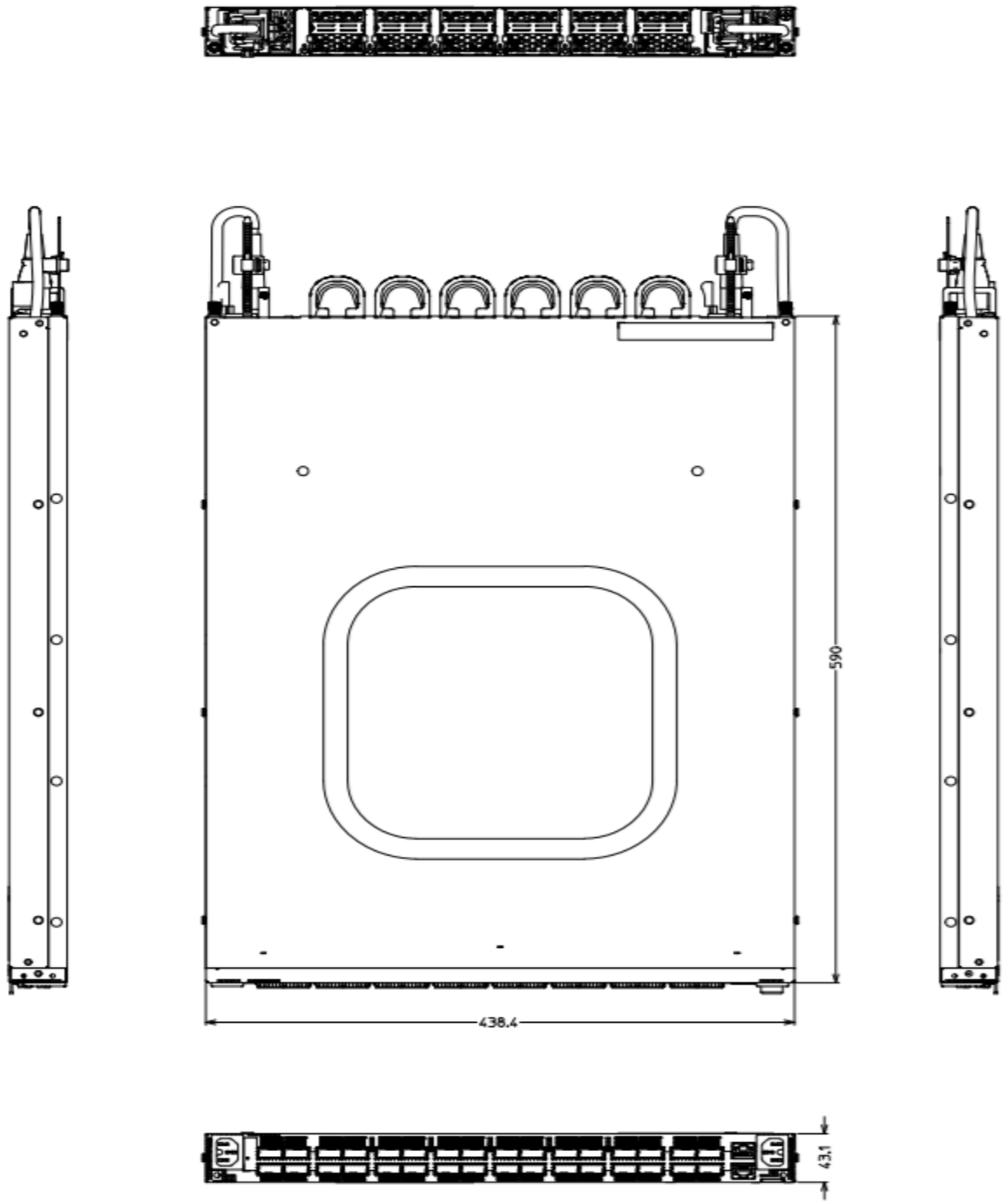


Figure 8-6 Switch board - PCB Placement

9. Mechanical



9.1. Dimension

Height: 43.25mm(maximum)

Width: 438.4mm

Depth: 515mm

9.2. Placement

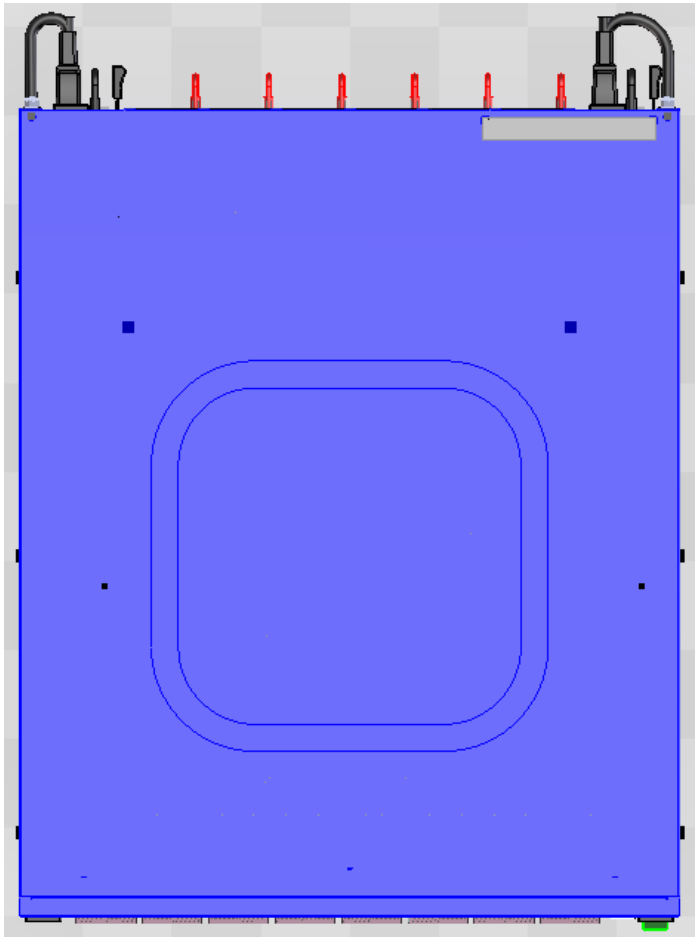


Figure 9-1 Mechanical Placement (Top)

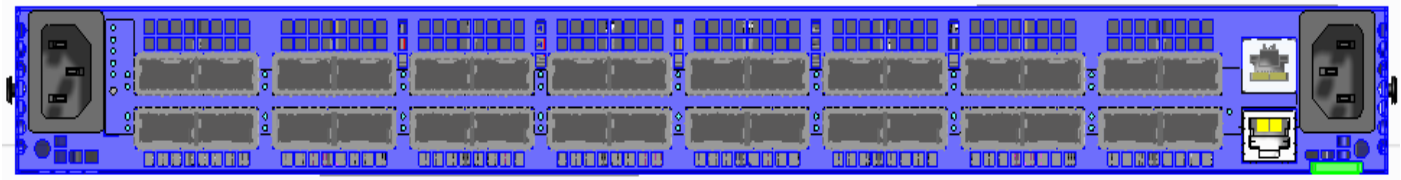


Figure 9-2 Mechanical Placement (Front)

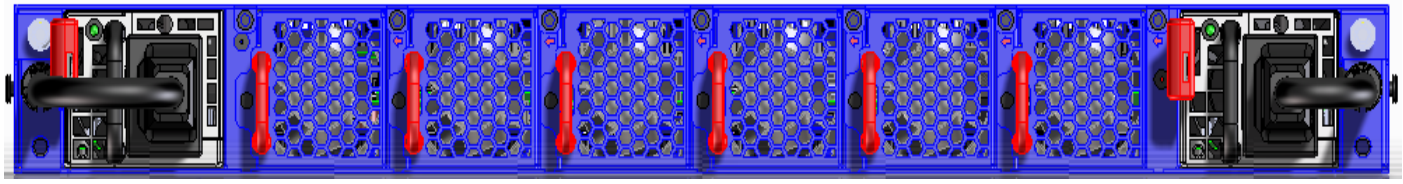


Figure 9-3 Mechanical Placement (Rear)

9.3. Cooling Method

9.3.1. Fan module

AS7900-32X system supports two kinds of Fan modules.

- Front to back Fan module with red color handle
- Back to Front Fan module with blue color handle

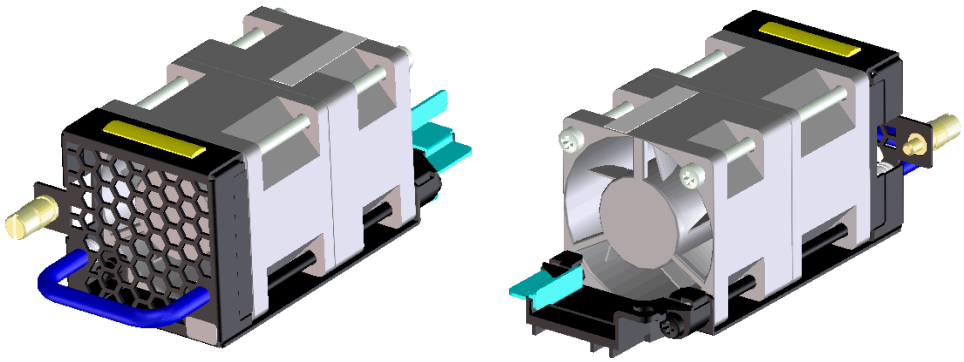


Figure 9-4 Back to front fan module

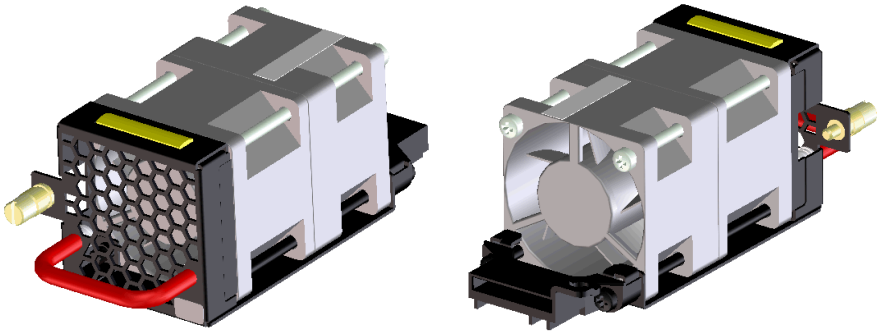


Figure 9-5 Front to Back fan module

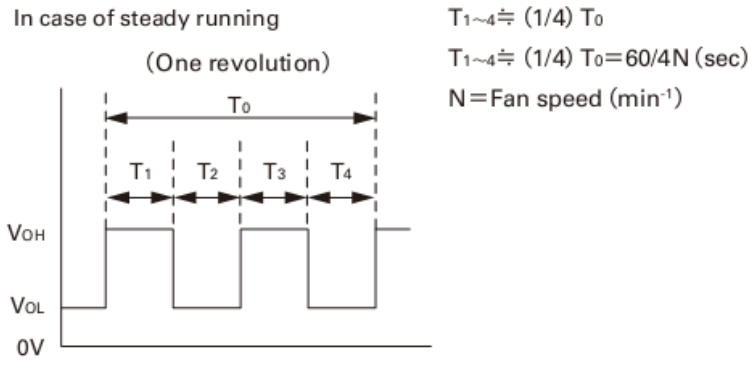
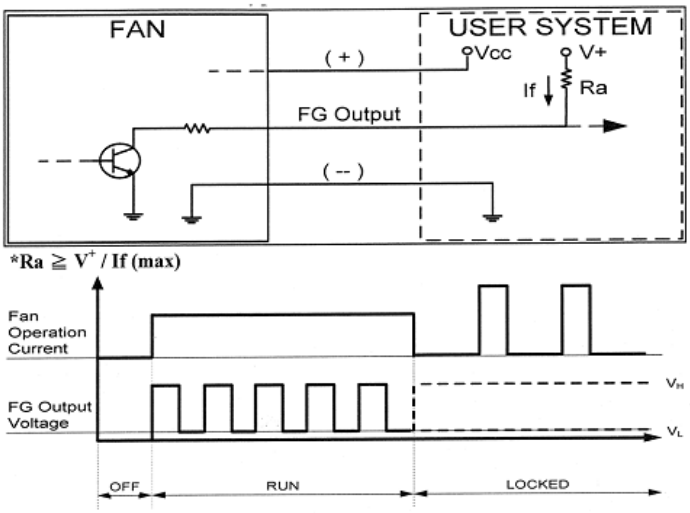


Figure 9-6 Fan Speed information



★Electrical Characteristics ：(at Ta = 25℃, V_{CC}=12V)

Parameter	Ratings			Unit
	min	typ.	max	
FG Supply Voltage(V+)	3	--	13.2	Voltage
FG Output Current (If)	--	--	5	mA
FG Output (VL)	0	--	0.5	Voltage
FG Output (VH)	--	V+	--	Voltage

Figure 9-7 Fan failed information

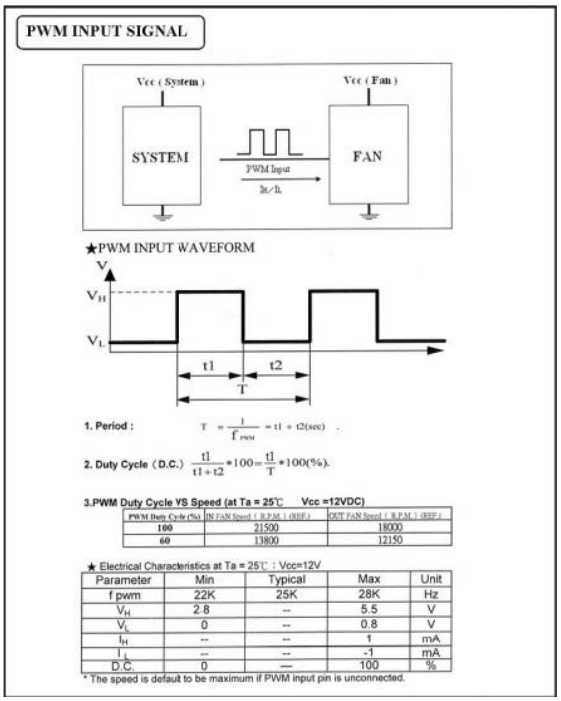


Figure 9-8 Fan PWM

Software Support

The AS7900-32X supports a base software package composed of the following components:

BIOS support

The AS7900-32X Supports AMI AptioV BIOS version A01 or greater with the x86 CPU module

U-Boot

The AS7800-64X Supports U-Boot version 1.4.0.2 or greater with the T2080 CPU module

ONIE

The AS7900-32X supports ONIE version 2014.08 or greater. See http://onie.org/

Open Network Linux

See http://opennetlinux.org/ for latest supported version

Specifications

Power Consumption

The total estimated system power consumption of the AS7900-32X is ~1100 Watts. This is based upon worst case power assumptions for traffic, optics used, and environmental conditions. Typical power consumption will be less.

Environmental

- 0 to 40 Degrees C operating range
- -40 to 40 Degrees C storage temperate range
- Humidity 5% to 95% non-condensing (operational and storage)
- Vibration – IEC 68-2-36, IEC 68-2-6
- Shock – IEC 68-2-29
- Acoustic Noise Level – Under 60dB in 40 degree C
- Altitude - 15,000 (4572 meters) tested operational altitude

Safety

- UL/ Canada
- CB (Issued by TUV/RH)
- China CCC

Electromagnetic Compatibility

- CE
- EN55022 Class A
- EN55024
- EN61000-3-2
- EN61000-3-3
- FCC Title 47, Part 15, Subpart B Class A
- VCCI Class A
- CCC

ROHS

Restriction of Hazardous Substances (6/6)

Compliance with Environmental procedure 020499-00 primarily focused on Restriction of Hazardous Substances (ROHS Directive 2002/95/EC) and Waste and Electrical and Electronic Equipment (WEEE