EDGECORE Networks Corporation

Edgecore AS7900-32X

Software Programming Guide

Revision 1.0

OPEN

Compute Project

Revision History

Revision	Date	Author	Description
1.0	3/16/2018	Jeff Catlin	Initial Release

Contents

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Description	**Manufacturer**	**Part Number**
T2080 CPU	Freescale	T2080NSN8TTB
SDRAM (8GB per channel)	UNIGEN	UG10U7211P8UU-BDE *2
USB to NAND Flash 8GB	ATP	AF8GSSGH-AC2
NOR Flash 128MB	MICRON	JS28F00AM29EWHA
Trusted Platform Module (TPM)	ST	ST33ZP24AR28PVSK
mSATA Connector	TE	1775838-2
M.2 connector	CONCRAFT	213BAAA32FA
SD Connector	CVILUX	CSD-09A001D
Switching Silicon	Broadcom	56980
10/100/1000 PHY	Broadcom	BCM54616S
Fans	AVC	DFPH0456B2UY006
CPLD (2)	Lattice	LCMXO3LF-1300C-5BG256C 2.5/3.3V
CPLD	Lattice	LCMXO3LF-4300C-5BG324C 2.5V/3.3V

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Scope

This document outlines the technical aspects of the Edgecore AS7900-32X Open Switch Platform that will aid in software development and/or porting software to the device .

Overview

This document describes the technical specifications of the AS7900-32X Leaf/Spine switch designed by Edgecore Networks Corporation. The AS7900-32X is a cost optimized switch design focused on Leaf/Spine deployments which support 400/100G. The AS7900-32X switch supports thirty-two QSFP-DD ports that each can operate at 10/25/40/50/100/200/400G modes of operation (different per port configurations supported based upon speed selected).

The AS7900-32X is a PHY-Less design with the QSFP28-DD connections directly attaching to the Serdes interfaces of the Broadcom 56980 switching silicon providing the lowest cost, latency, and power. The AS7900-32X supports traditional features found in Top of Rack / Leaf / Spine switches such as:

- Redundant field replaceable power supply and fan units
- Support for “Front to Back” or “Back to Front” air flow direction
- The AS7900-32X supports various Open Source CPU modules offered by Edgecore Networks which include the following:
    - Atom based C2538 based CPU module made publicly available through the OCP accepted AS7712-32X design

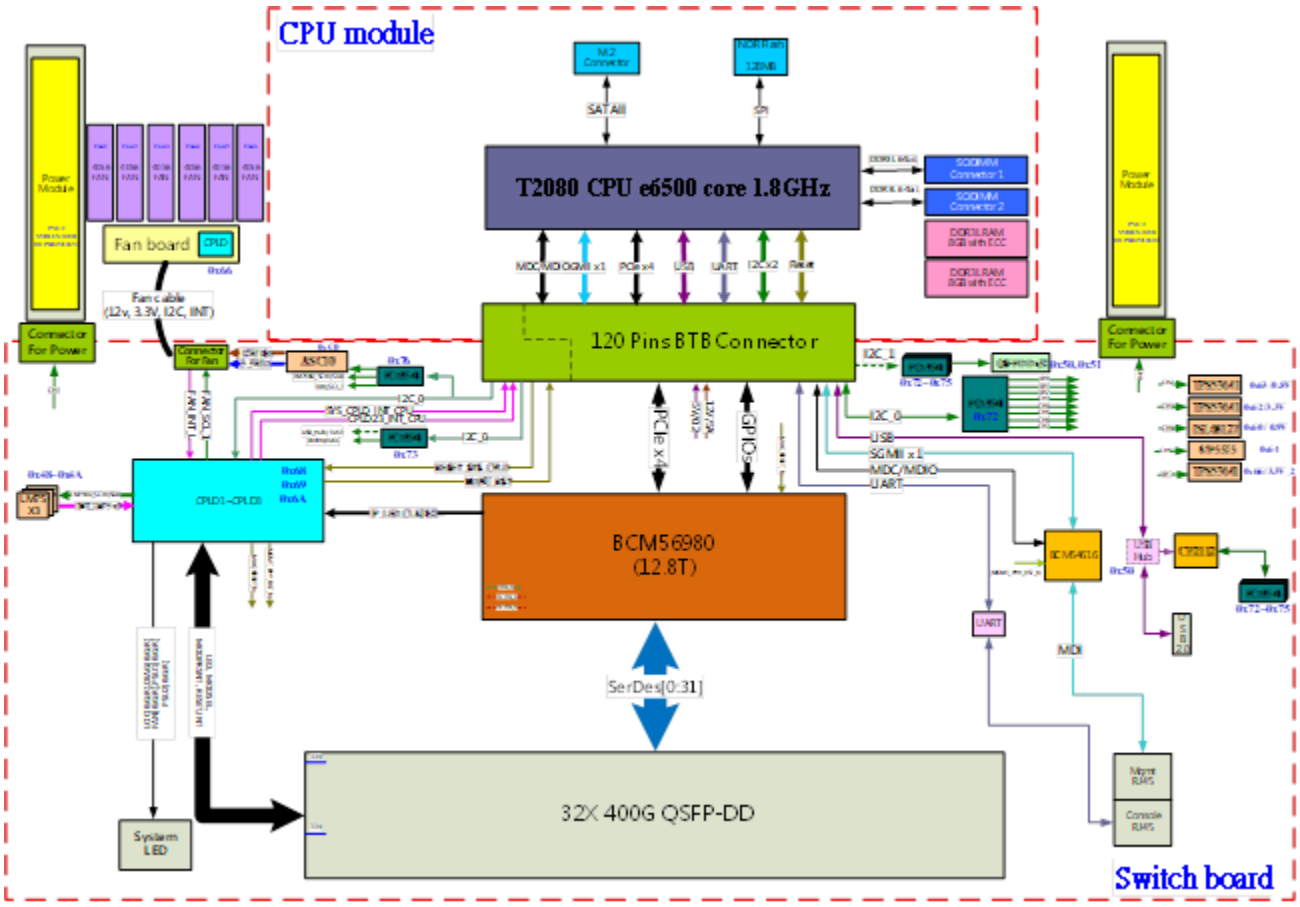
http://files.opencompute.org/oc/public.php?service=files&t=3d2271fd0e40a66725a747030487d571

    - Xeon based D-1518 based CPU module made publicly available through the OCP accepted AS7800-64X design

http://files.opencompute.org/oc/public.php?service=files&t=d2b4bfed8dfc024a1f2ece0db57118ee

    - Freescale T2080 based CPU module which is referenced in this specification

High Level Block Diagram



I2C Overview

The CPU has one I2C channels for our application.. The I2C used for system peripheral access include SODIMM, RTC and DC/DC. The I2C_0 and I2C_1 are for Mainboard function used.

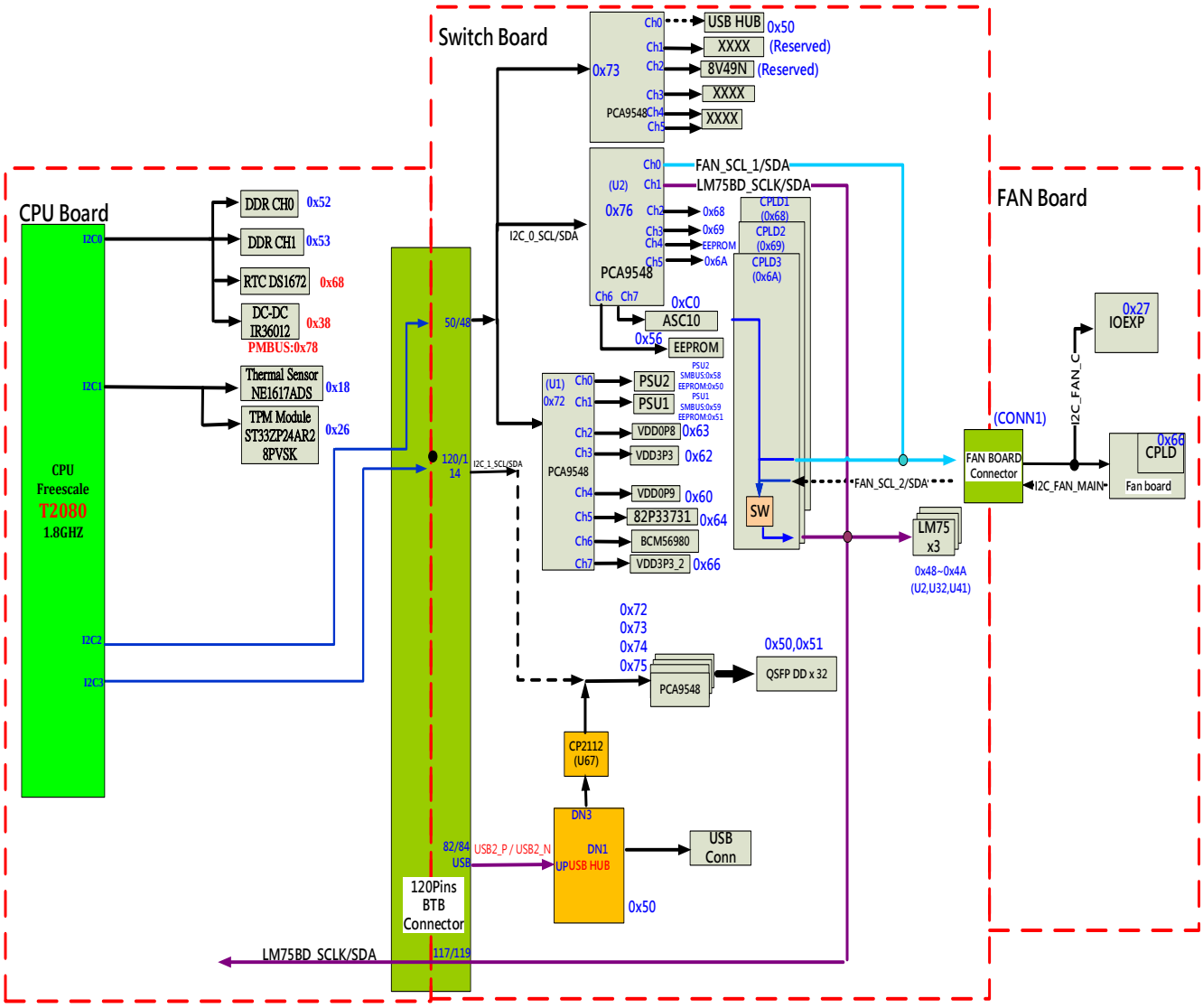


Figure 0-1 I2C Connection

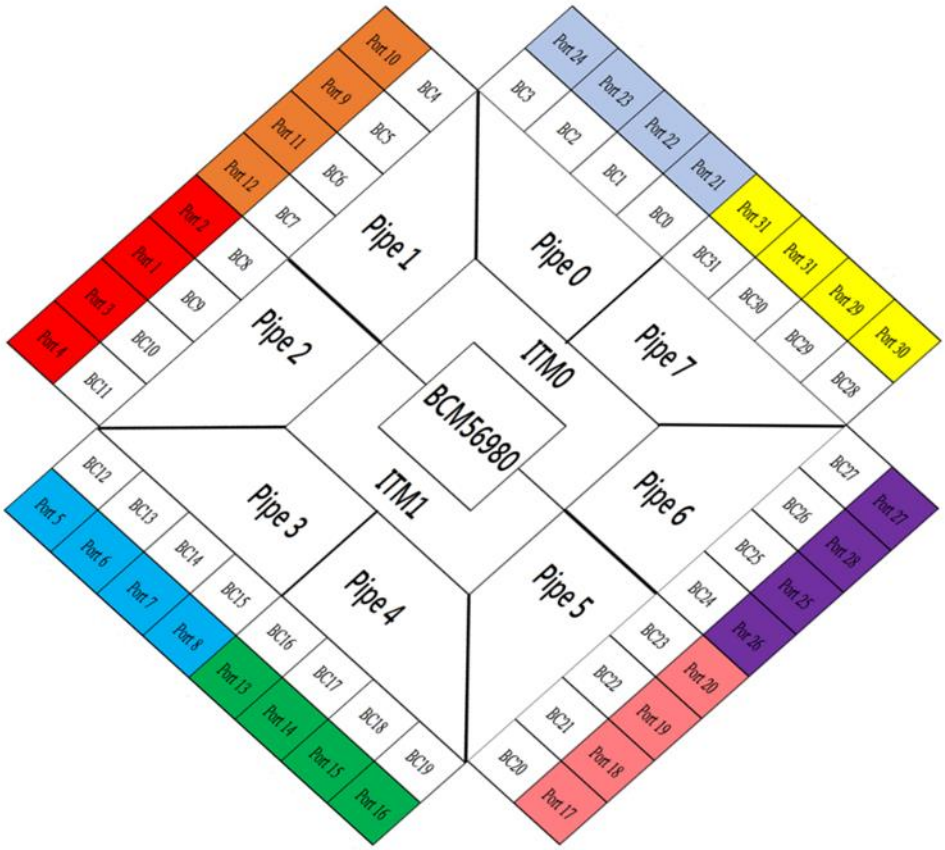
	Channel	Device	Address
CPU	I2C_CH0	SODIMM SPD EEPROM	0x52
		SODIMM SPD EEPROM	0x53
		DS1672 (RTC)	0x68
		DC/DC IR36021	0X38

	I2C_CH1	NE1617EDS (Thermal)	0x18
		TPM module	0x13
	I2C_CH2	I2C switch (72)	0x72
		I2C switch (73)	0x73
		I2C switch (76)	0x76
	I2C_CH3	I2C switch (72)	0x72
		I2C switch (73)	0x73
		I2C switch (74)	0x74
		I2C switch (75)	0x75
I2C switch (72)	I2C_0_CH0	PWR module2	58 50
	I2C_0_CH1	PWR module1	59, 51
	I2C_0_CH2	TPS53641_VDD0P8-U33	0x63
	I2C_0_CH3	TPS53641_VDD3P3-U8	0x62
	I2C_0_CH4	ISL68127_VDD0P9-U4	0x60
	I2C_0_CH5	82P33731-U37	0x64
	I2C_0_CH6	BCM56980	
	I2C_0_CH7	TPS53641_VDD3P3_U6	66
I2C switch (73)	I2C_0_CH0	USB-Hub (Reserved)	0x50
	I2C_0_CH1	(Reserved)	
	I2C_0_CH2	8V49N (Reserved)	
I2C switch (76)	I2C_0_CH0	Fan	0x66
	I2C_0_CH1	LM75	48,49,4A
	I2C_0_CH2	CPLD1	0x68
	I2C_0_CH3	CPLD2	0x69
	I2C_0_CH4	EEPROM	
	I2C_0_CH5	CPLD3	0x6A
	I2C_0_CH6	EEPROM	0x56
	I2C_0_CH7	ASC_10	0xC0
I2C switch (72)	I2C_1_CH0	QSFP-DD Port 1	50, 51
	I2C_1_CH1	QSFP-DD Port 2	50, 51
	I2C_1_CH2	QSFP-DD Port 3	50, 51

	I2C_1_CH3	QSFP-DD Port 4	50, 51
	I2C_1_CH4	QSFP-DD Port 5	50, 51
	I2C_1_CH5	QSFP-DD Port 6	50, 51
	I2C_1_CH6	QSFP-DD Port 7	50, 51
	I2C_1_CH7	QSFP-DD Port 8	50, 51
I2C switch (73)	I2C_CH0	QSFP-DD Port 9	50, 51
	I2C_CH1	QSFP-DD Port 10	50, 51
	I2C_CH2	QSFP-DD Port 11	50, 51
	I2C_CH3	QSFP-DD Port 12	50, 51
	I2C_CH4	QSFP-DD Port 13	50, 51
	I2C_CH5	QSFP-DD Port 14	50, 51
	I2C_CH6	QSFP-DD Port 15	50, 51
	I2C_CH7	QSFP-DD Port 16	50, 51
I2C switch (74)	I2C_CH0	QSFP-DD Port 17	50, 51
	I2C_CH1	QSFP-DD Port 18	50, 51
	I2C_CH2	QSFP-DD Port 19	50, 51
	I2C_CH3	QSFP-DD Port 20	50, 51
	I2C_CH4	QSFP-DD Port 21	50, 51
	I2C_CH5	QSFP-DD Port 22	50, 51
	I2C_CH6	QSFP-DD Port 23	50, 51
	I2C_CH7	QSFP-DD Port 24	50, 51
I2C switch (75)	I2C_CH0	QSFP-DD Port 25	50, 51
	I2C_CH1	QSFP-DD Port 26	50, 51
	I2C_CH2	QSFP-DD Port 27	50, 51
	I2C_CH3	QSFP-DD Port 28	50, 51
	I2C_CH4	QSFP-DD Port 29	50, 51
	I2C_CH5	QSFP-DD Port 30	50, 51
	I2C_CH6	QSFP-DD Port 31	50, 51
	I2C_CH7	QSFP-DD Port 32	50, 51

Table 5- 1 I2C Address Table

Port Mapping



Port 1	Port 3	Port 5	Port 7	Port 9	Port 11	Port 13	Port 15	Port 17	Port 19	Port 21	Port 23	Port 25	Port 27	Port 29	Port 31
BC9	BC10	BC12	BC14	BC5	BC6	BC16	BC18	BC20	BC22	BC0	BC2	BC25	BC27	BC29	BC30
BC8	BC11	BC13	BC15	BC4	BC7	BC17	BC19	BC21	BC23	BC1	BC3	BC24	BC26	BC28	BC31
Port 2	Port 4	Port 6	Port 8	Port 10	Port 12	Port 14	Port 16	Port 18	Port 20	Port 22	Port 24	Port 26	Port 28	Port 30	Port 32

1. CPLD overview

ES8632BT has four CPLD devices for decoding, Fan module status, reset system, power module status and System interrupt.

I2C address info:

*CPLD1:0x68
*CPLD2:0x69
*CPLD3:0x6A
*CPLD4:0x6B
*Fan_CPLD:0x66

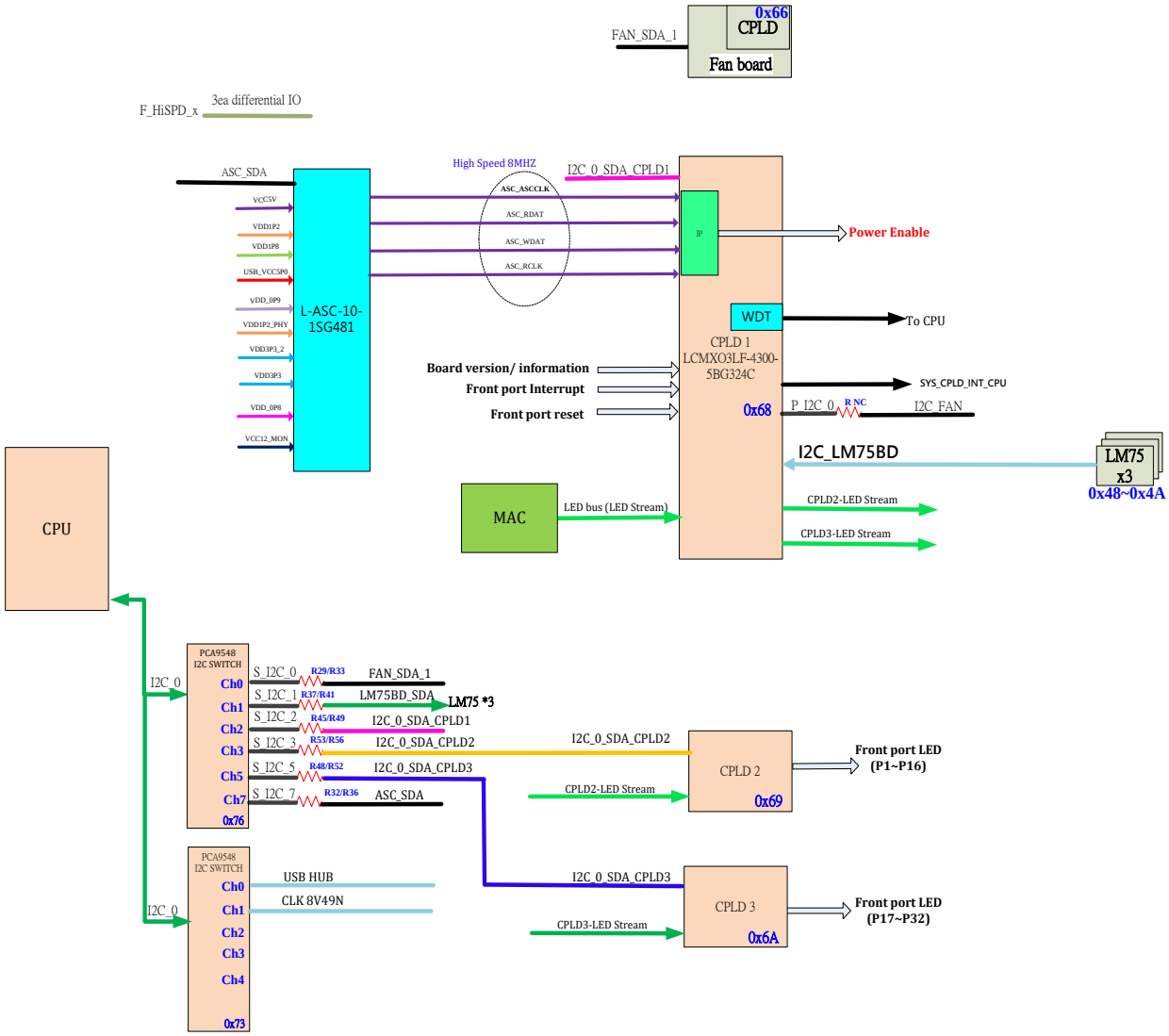


Figure 1-1 Block diagram

The CPLD on the CPU board is Altera MaxVEPM1270F256.The CPLD has registers to monitor the status of the fan module, thermal sensors and power module.

The CPLD also has the circuit of Watchdog and registers of CPLD code version and board ID.

1.1. CPLD 1 Architecture

1.1.1. Reset

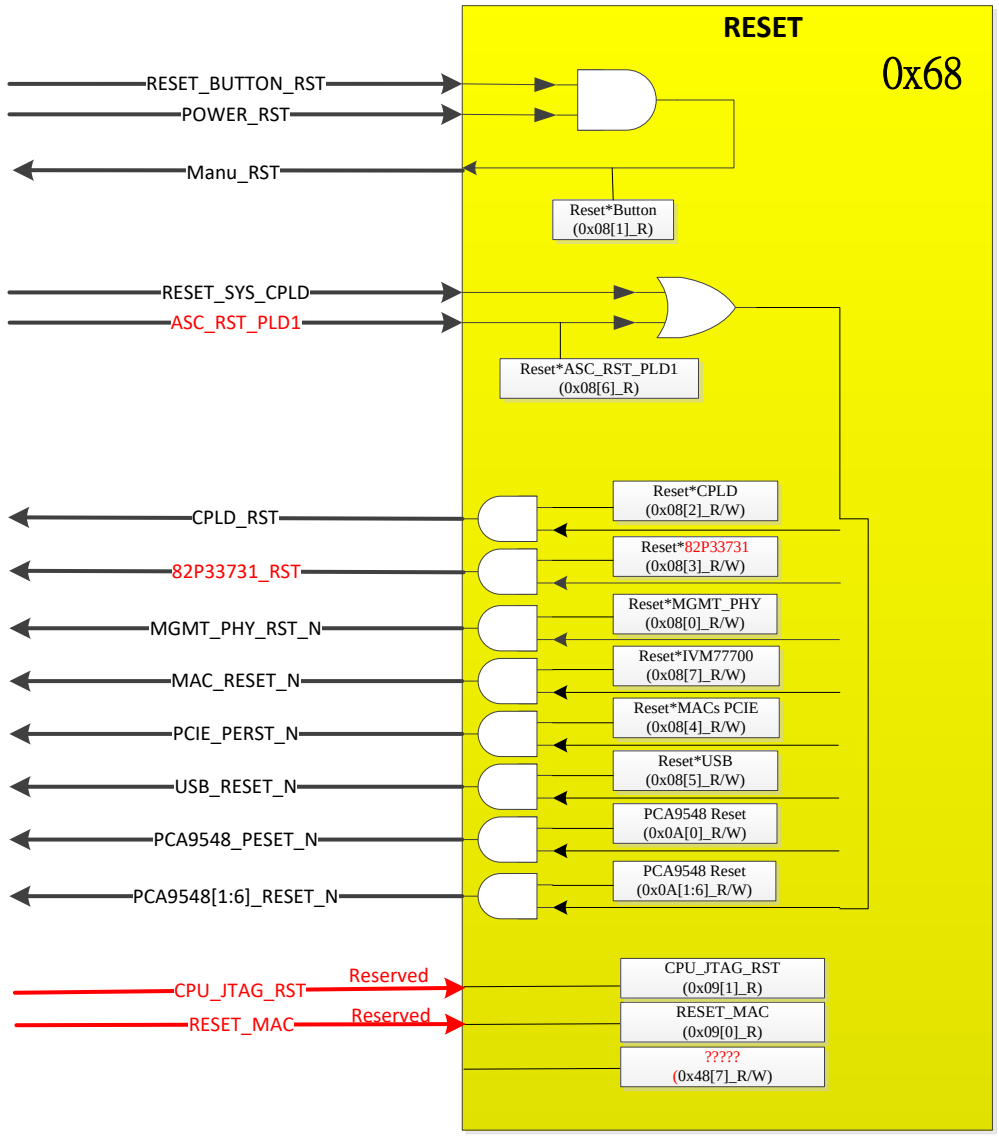


Figure 1-2 Reset function

The reset source is from “Power_RST” and Reset_button_RST, then the reset will be passing “MANU_RST” to CPU board. If CPU board is ready, CPU board will passing “RESET_SYS_CPLD” to CPLD and reset all device. There has a register can be used for reset chip individual.

There are two reserved signals, “Reset_MAC” and “CPU_JTAG_RST”.

1.1.2. MISC

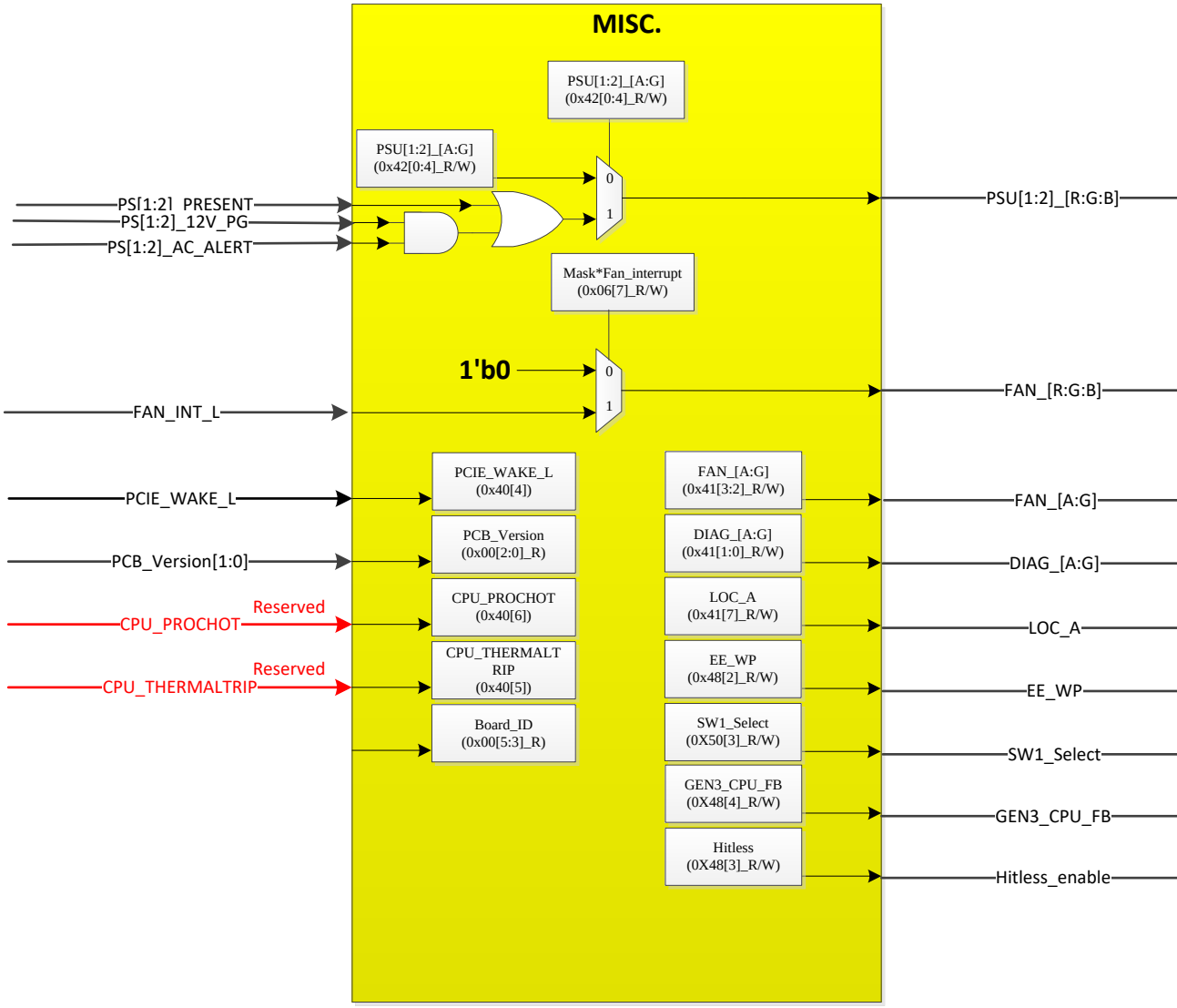


Figure 1-3 MISC function

The MISC include two signal groups, system LED and reserve signals.

The system LED include “PS[1:2]_[G:R]”,”Diag_[G:R]”, “FAN_[G:R]” and LOC_B. The interface need PWM system to do LED color adjust. The PWM system runs with 100k Hz, 8bits level. CPLD will control Fan and Power LED will enable right color by Fan and Power module status.

EE_WP driven the write protection pin of EEPROM to control Enable/ Disable write protection.

SW1_Select driven the selection pin of bus switch to switch CPLD’s JTAG interface and FPGA’s SPI mode.

CPLD has a register to record PCB version. And ID information. Those reserve signals connect to register for future use.

1.1.3. I2C Access

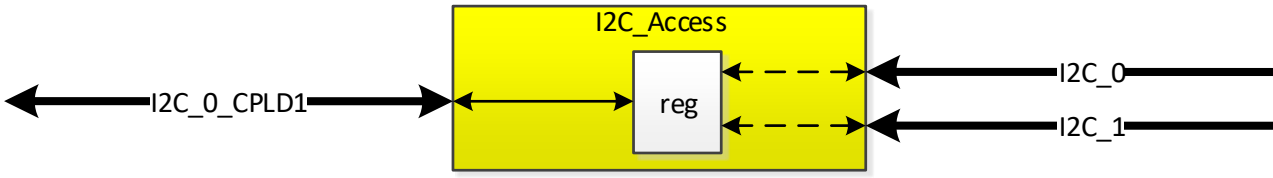


Figure 1-4 I2C function

I2C_0 (Net: I2C_0_SCL_CPLD1 ; I2C_0_SDA_CPLD1_R) is the CPLD control bus. From I2C_0, CPU can read/ write CPLD internal register

1.1.4. Interrupt

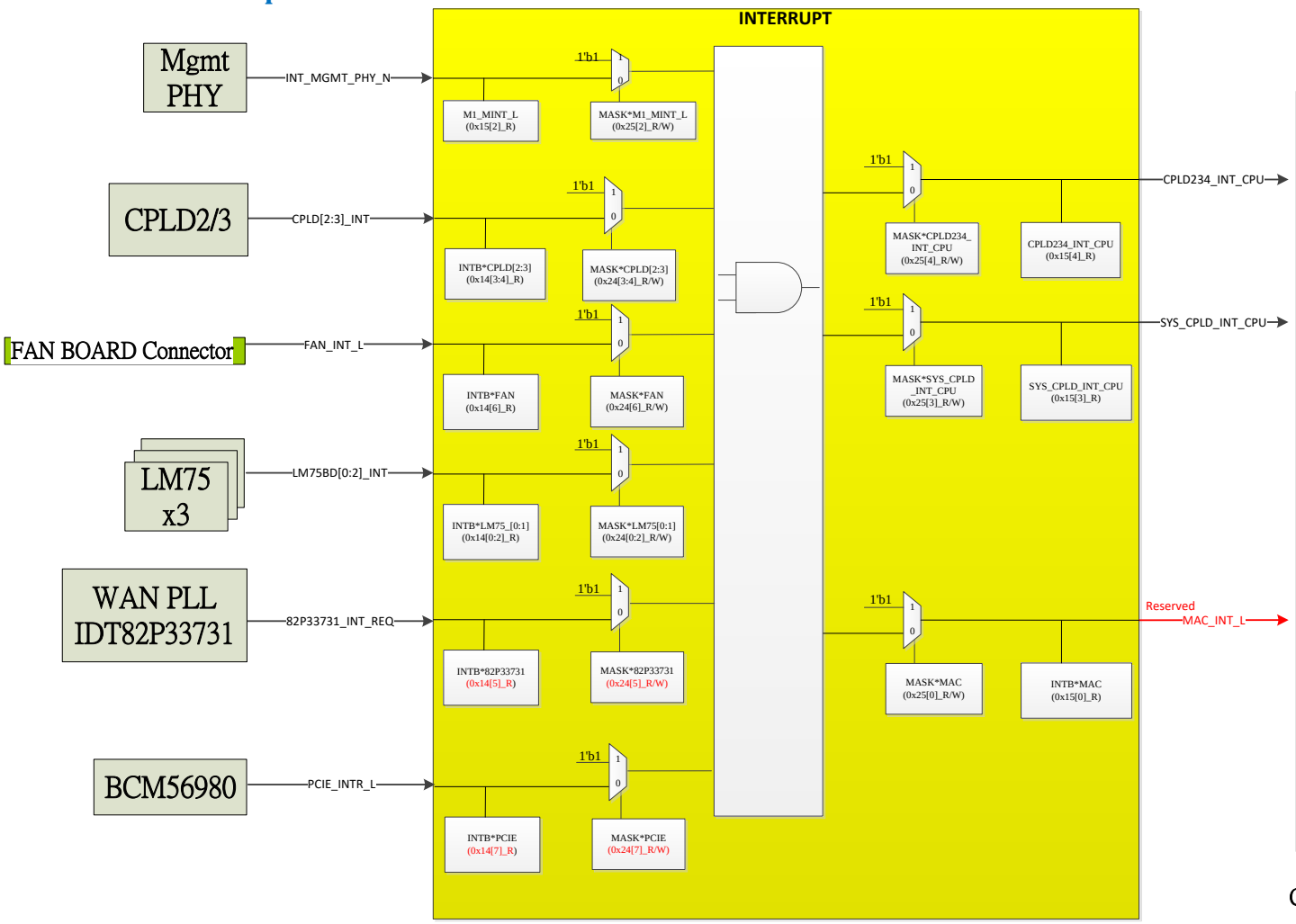


Figure 1-5 Interrupt function

If an interrupt occurs, CPLD1 inform CPU by “SYS_CPLD_INT_CPU”, CPLD2&3&4 inform CPU by “CPLD234_INT_CPU”. Register will record the interrupt status.

Mask register is for block the interrupt to CPU.

1.1.5. Clock

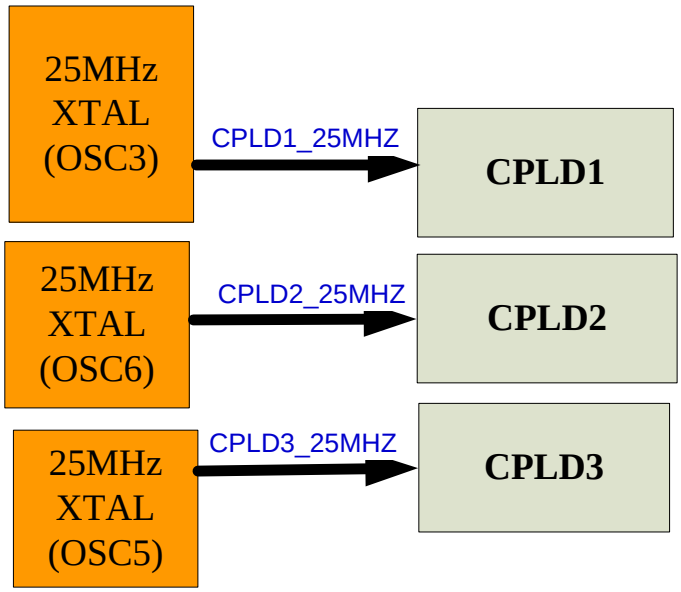


Figure 1-6 Clock OSC 25MHz

The CPLD reference clock is from 25MHz (Like : Net: CPLD1_25MHZ) . The 125MHz will transfer100KHz.

The 100 KHz is for LED PWM system block.

1.1.6. USB Over Current Protect

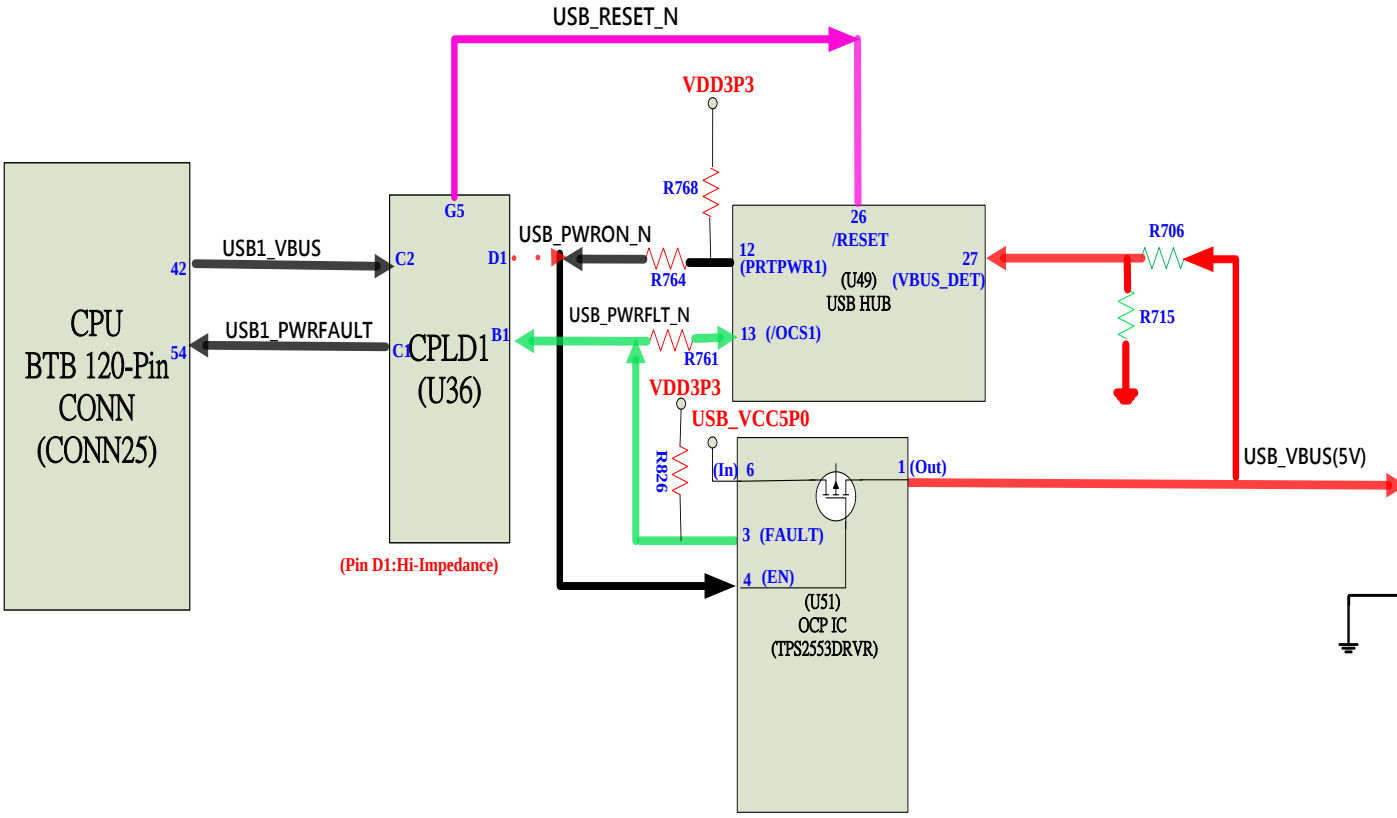


Figure 1-7 USB Block diagram

USB_PWRON_N is controlled by USB HUB, when detect USB_ PWRFLT_N down to low to protect the USB 5V over current. USB1_PWRFFAULT will send interrupt to CPU

CPU can enable and reset the USB by USB_enable (register 0x47[3]) and USB_RESET_N (0x08[5]). USB1_PWRFFAULT will return to H when CPU mask it by register USB_PWRFAULT_MASK (register 0x08[1]) or USB_RESET_N (0x08[5]) through I2C bus. USB1

1.1.7. Power Sequence

The most important function of the CPLD is to control the whole board power sequence based on the power sequence requirement of Innovium TERALYNX series.

CPLD would base on the power good signals from the VRs on the board and then drives the enable signals to enable the VRs.

The TPS53622A_FR_FAULT, TPS53622B_FR_FAULT, TPS53622C_FR_FAULT signals are used to indicate digital VRMs the high-side FETs short, over-voltage, over-temperature, and the input over-current conditions.

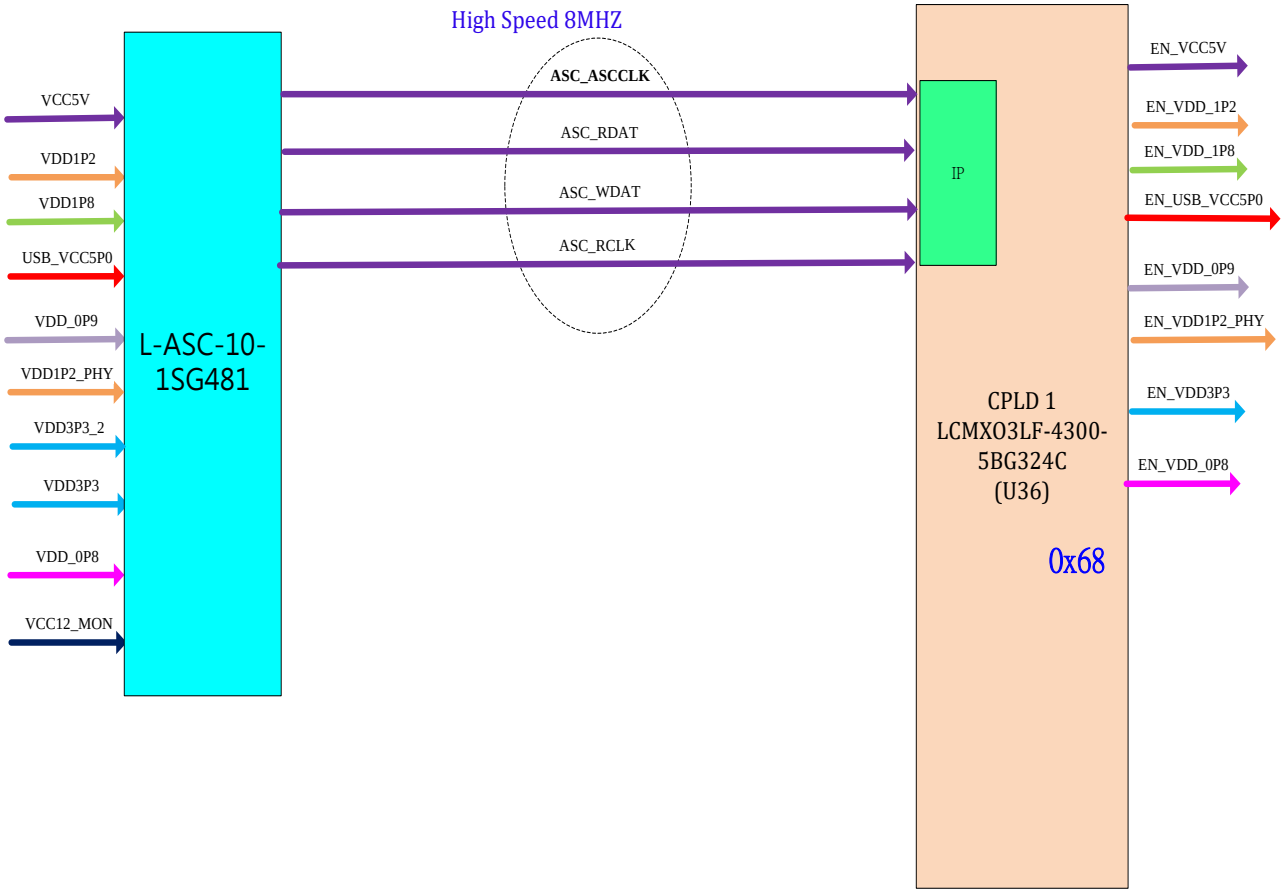
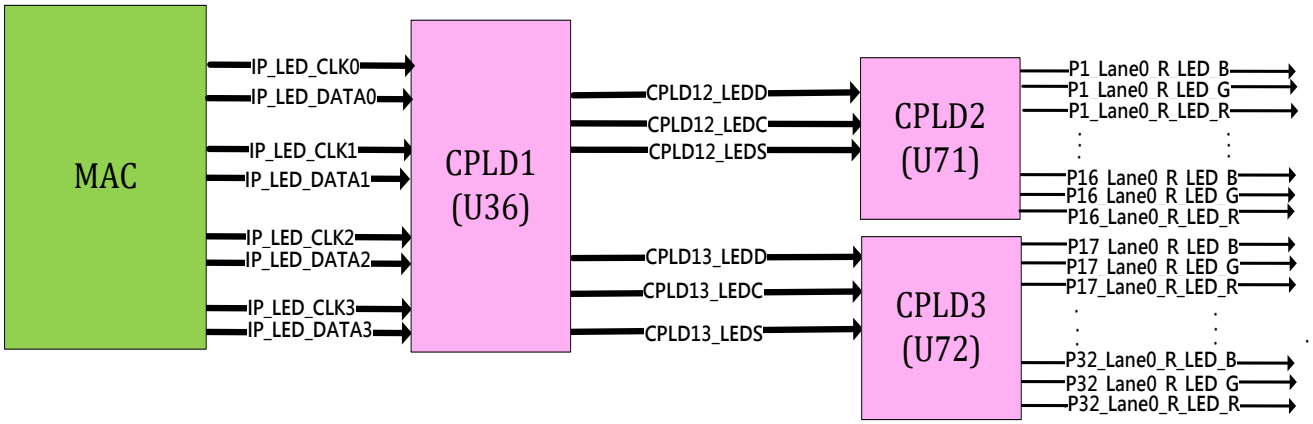
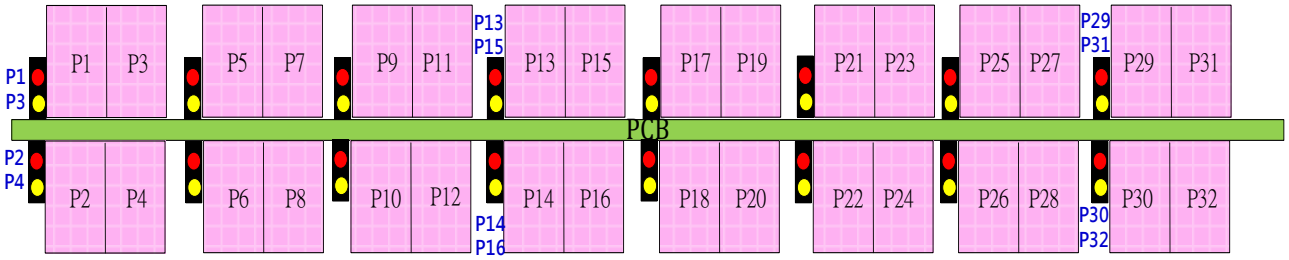


Figure 1-8 Power Sequence

1.1.8. LED Stream

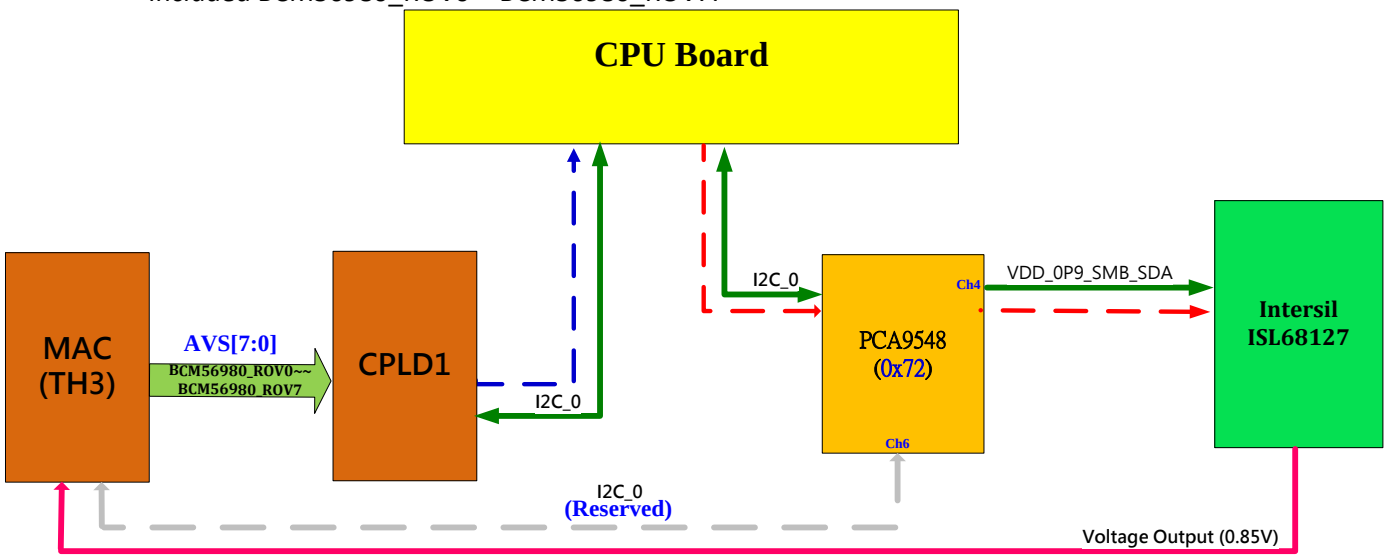




1.1.9. ROV Control

This ROV Control is design for the Core Voltage (0.85V) of MAC. There are 8 pins on the CPLD1.

Included BCM56980_ROV0~~BCM56980_ROV7.



The procedure for ROV control:

1. System power up, ISL68127 IC sets the default VDD voltage to be 0.85V nominal voltage;
2. When system software is up running, software will control CPU to READ, ROV registers of CPLD1 through I2C_0 Bus;
3. Software will WRITE to Register of ISL68127 IC through I2C (CPU -> PCA9548 -> ISL68127 IC) to set the operating voltage according the ROV value;

1.2. CPLD 2 / 3 Architecture

1.2.1. Front Port RGB LED

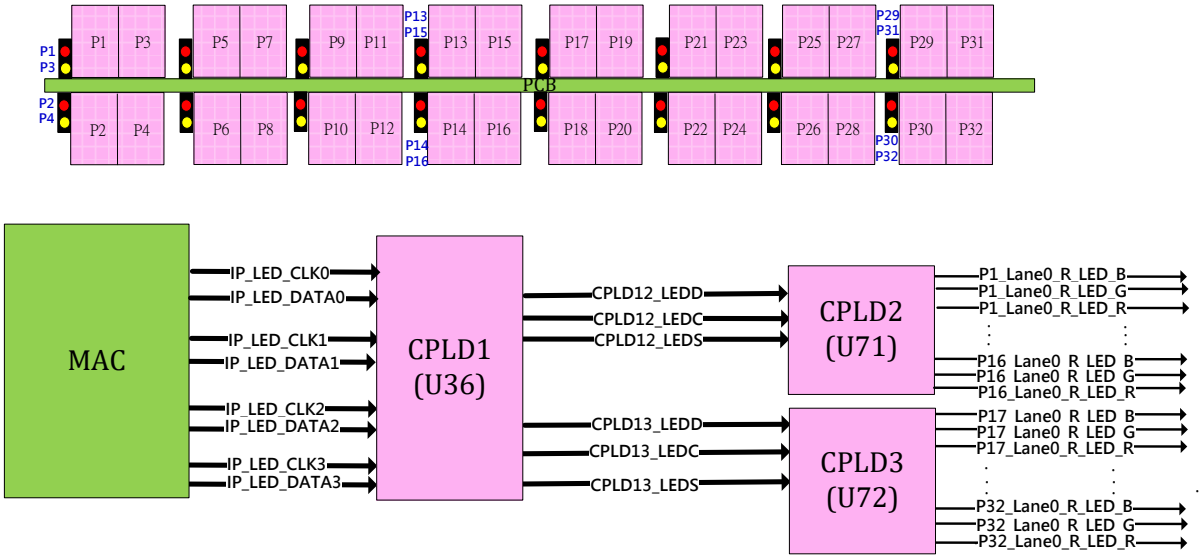


Figure 1-9 LED

The Front RGB LED need PWM system to do LED color adjust. The PWM system runs with 100 KHz, 8bits level. And show different LED color when the port link on 4x50G / 200G / 4x100G / 400G speed. The LED bus runs 5MHz serial bus and will indicate the port status is link or not.

1.2.2. MISC

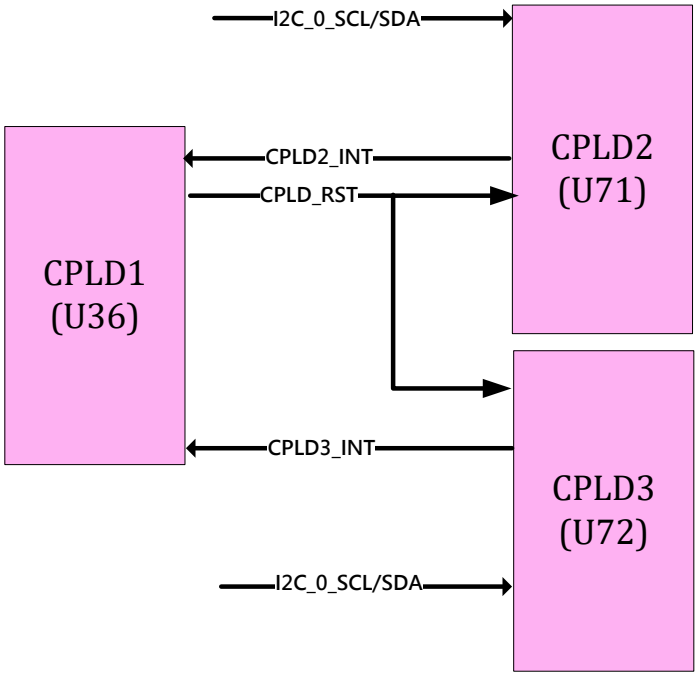


Figure 1-10 MISC

I2C_0 is the CPLD control bus. From I2C_0, CPU can read/ write CPLD internal register.
CPLD_RST will rest the CPLD2 to Default

1.2.3. Clock

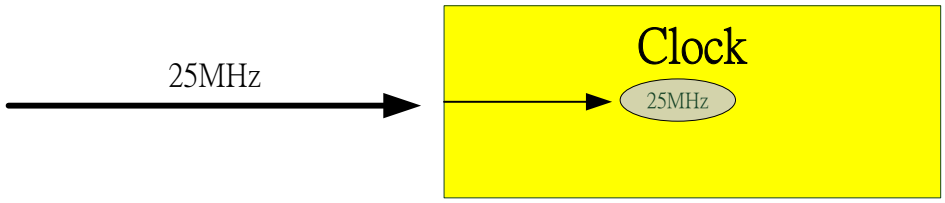


Figure 1-11 Clock OSC 25MHz

The CPLD reference clock is from 25MHz. The 125MHz will transfer100KHz.
The 100 KHz is for LED PWM system block.

1.3. Fan CPLD Architecture

1.3.1. Fan control/ LED

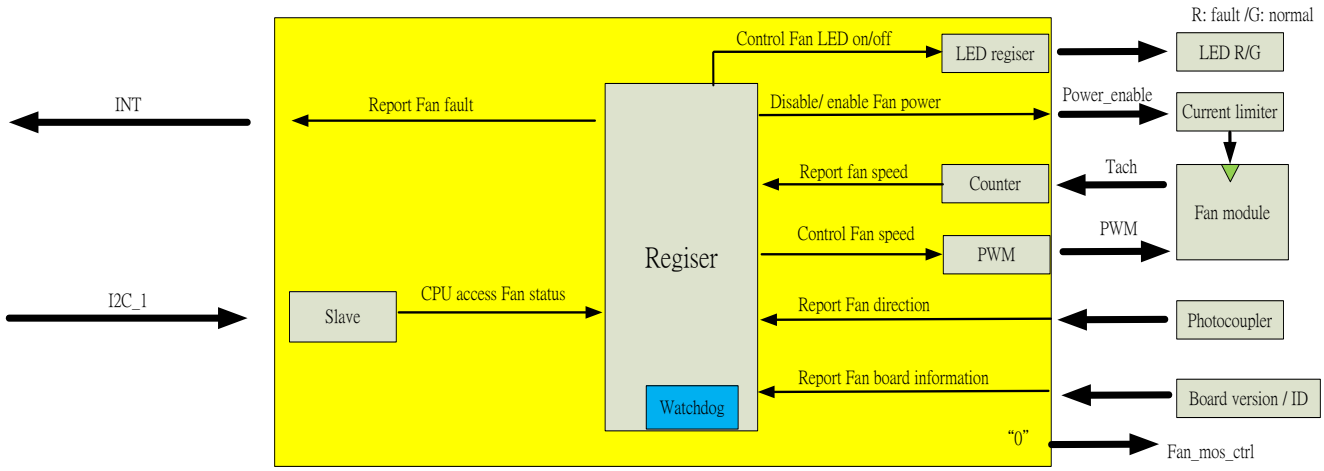


Figure 1-12 Fan CPLD block diagram

The CPU can access FAN CPLD via I2C interface to get the fan status.

The Fan CPLD has the register to control Fan PWM signal for fan speed control, and the counter for fan speed reporting. There has a fan power control to enable/ disable Fan power rail.

The CPLD will detect fan speed to check fan status if any issue. And CPLD will inform CPU by fan interrupt signal if there has fan fail occur or watchdog time out.

The fan LED will report the fan status via Red/ Green LED.

The watchdog timer is the thermal protection to avoid the CPU hang up. If watchdog timer count to zero, Fan CPLD will be pull-up the Fan speeds for system thermal protection.

1.3.2. Clock

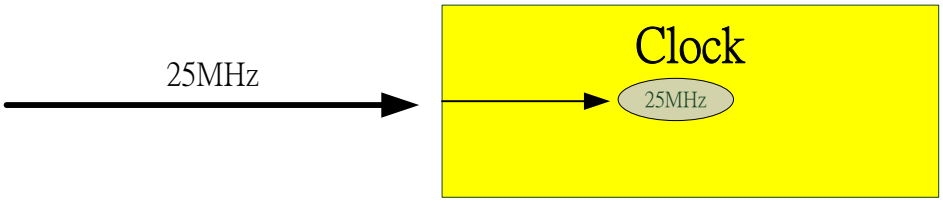


Figure 1-13 Clock OSC 25MHz

1.4. CPLD 1 Register

Address	Register	R/W	Default
0x00	Board Info	Read Only	
0x01	CPLD version	Read Only	
0x02	Power module status	Read Only	
0x04	System Reset-1 **(Reserved)**	Read& Write	0xFF
0x05	System Reset-2 **(Reserved)**	Read& Write	0xFF
0x06	System Reset-3 **(Reserved)**	Read& Write	0xFF
0x07	System Reset-4 **(Reserved)**	Read& Write	0xFF
0x08	System Reset-5	Read& Write	0xFF
0x09	System Reset-6	Read& Write	0x0F
0x0A	System Reset-7	Read& Write	0xFF
0x0B	System Reset Lock/ unlock	Read& Write	0x00
0x10	Interrupt Status-1 **(Reserved)**	Read Only	
0x11	Interrupt Status-2 **(Reserved)**	Read Only	
0x12	Interrupt Status-3 **(Reserved)**	Read Only	
0x13	Interrupt Status-4 **(Reserved)**	Read Only	
0x14	Interrupt Status-5	Read Only	
0x15	Interrupt Status-6	Read Only	
0x20	Interrupt Mask-1 **(Reserved)**	Read Only	0xFF
0x21	Interrupt Mask-2 **(Reserved)**	Read Only	0xFF
0x22	Interrupt Mask-3 **(Reserved)**	Read Only	0xFF
0x23	Interrupt Mask-4 **(Reserved)**	Read Only	0xFF
0x24	Interrupt Mask-5	Read Only	0x00

0x25	Interrupt Mask-6	Read Only	0x00
0x30	Module Present-1 **(Reserved)**	Read Only	
0x31	Module Present-2 **(Reserved)**	Read Only	
0x32	Module Present-3 **(Reserved)**	Read Only	
0x33	Module Present-4 **(Reserved)**	Read Only	
0x40	Recovery_CLK valid &1PPS Mask	Read& Write	0x50
0x41	System LED -1	Read& Write	0x12
0x42	System LED -2 **(PSU1/2 LED)**	Read& Write	0xFF
0x43	System LED -3 **(Reserved)**	Read& Write	0xFF
0x44	System LED -4 **(Reserved)**	Read& Write	0xFF
0x45	System LED -5 **(Reserved)**	Read& Write	0xFF
0x47	USB	Read& Write	0x0F
0x48	MISC	Read& Write	0xB0
0x49	FPGA control (Reserved)	Read& Write	0xFB
0x50	MISC2	Read& Write	
0x51	Power sequence	Read& Write	
0x52	Power sequence2	Read& Write	
0x53	Power marge	Read& Write	

Table 1-14 CPLD1 I/O Register Table

1.4.1. Offset 0x00 Board Info (Read Only)

Bit	Name	R/W	Default	Description
7:6	Reserved			
5:3	~~BOARD_ID[1:0]~~ (Reserved)	R		000: ~~ES8632BT (AS9716-32X)~~ 001: Reserved 010: Reserved 011: Reserved
2:0	PCB_VERSION[1:0]	R		000: R0A 001: R0B 010: R0C 011: R01

1.4.2. Offset 0x01 CPLD version (Read Only)

Bit	Name	R/W	Default	Description
7:0	CPLD_ver [7:0]	R		0000: CPLD version

1.4.3. Offset 0x02 BCM56980_ROV (Read Only)

Bit	Name	R/W	Default	Description
7:0	BCM56980_ROV [7:0]	R		BCM56980_ROV [7:0]

1.4.4. Offset 0x03 Power module status (Read Only)

Bit	Name	R/W	Default	Description
7:6	Reserved			
5:4	PS[1:2]_AC_ALERT	R		0: Fail 1: normal
3:2	PS[1:2]_12V_PG	R		0: Fail 1: normal
1:0	PS[1:2]_PRESENT	R		0: present 1:not present

[1]:PSU2 [0]: PSU1

1.4.5. Offset 0x04 System Reset-1 (Read & Write) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.6. Offset 0x05 System Reset-2 (Read & Write) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.7. Offset 0x06 System Reset-3 (Read & Write) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.8. Offset 0x07 System Reset-4 (Read & Write) (Reserved)

Bit	Name	R/W	Default	Description

7:0	Reserved			

1.4.9. Offset 0x08 System Reset-5 (Read & Write)

Bit	Name	R/W	Default	Description
7	Reset*IVM77700 (MAC_RESET_N)	R/W	1	1: IVM77700 is placed in normal operation state. 0: IVM77700 is placed in reset state.
6	Reset*ASC_RST_PLD1 (ASC_RST_PLD1)	R	1	1: DUT is placed in normal operation state. 0: DUT is placed in reset state.
5	Reset*USB_RESET (USB_RESET_N)	R/W	1	1: USB_RESET is placed in high. 0: USB_RESET is placed in Low.
4	Reset*MAC's PCIE (PCIE_PERST_L)	R/W	1	1: MAC's PCIE is placed in high. 0: MAC's PCIE is placed in Low.
3	Reset* 82P33731 (82P33731_RST)	R/W	1	1: 82P33731 is placed in normal operation state. 0: 82P33731 is placed in reset state.
2	Reset*CPLD (CPLD_RST)	R/W	1	1: CPLD is placed in normal operation state. 0: CPLD is placed in reset state
1	Reset*Button (Manu_RST)	R	1	1: DUT is placed in normal operation state. 0: DUT is placed in reset state.
0	Reset*MGMT_PHY (MGMT_PHY_RST_N)	R/W	1	1: MGMT_PHY is placed in normal operation state. 0: MGMT_PHY is placed in reset state.

0x08 will auto return to default after 500ms when set any bit to low

1.4.10. Offset 0x09 System Reset-6 (Read & Write)

Bit	Name	R/W	Default	Description
7	Reset*SPI Flash (QSPI_RST)	R/W	1	1: SPI Flash is placed in normal operation state. 0: SPI Flash is placed in reset state.
6:0				

0x09 will auto return to default after 500ms when set any bit to low

1.4.11. Offset 0x0A System Reset-7 (Read & Write)

Bit	Name	R/W	Default	Description
7	Reversed			
6	PCA9548_6_RESET_N (I2C_0; 0x73)	R/W	1	1: PCA9548 is placed in normal operation state. 0: PCA9548 is placed in reset state.
5	PCA9548_5_RESET_N (I2C_0, 0x76)	R/W	1	1: PCA9548 is placed in normal operation state. 0: PCA9548 is placed in reset state.
4	PCA9548_4_RESET_N (I2C_1; 0x75)	R/W	1	1: PCA9548 is placed in normal operation state. 0: PCA9548 is placed in reset state.

3	PCA9548_3_RESET_N (I2C_1; 0x74)	R/W	1	1: PCA9548 is placed in normal operation state. 0: PCA9548 is placed in reset state.
2	PCA9548_2_RESET_N (I2C_1; 0x73)	R/W	1	1: PCA9548 is placed in normal operation state. 0: PCA9548 is placed in reset state.
1	PCA9548_1_RESET_N (I2C_1; 0x72)	R/W	1	1: PCA9548 is placed in normal operation state. 0: PCA9548 is placed in reset state.
0	PCA9548_RESET_N (I2C_0; 0x72)	R/W	1	1: PCA9548 is placed in normal operation state. 0: PCA9548 is placed in reset state.

0x0a will auto return to default after 500ms when set any bit to low

1.4.12. Offset 0x0B System Reset Lock/ unlock (Read & Write)

Bit	Name	R/W	Default	Description
7:1	Reserved			
0	System Reset Lock	R/W	0	1: Lock system reset signal to be high. 0: System reset signal to be normal.

1.4.13. Offset 0x10 Interrupt Status-1 (Read Only) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.14. Offset 0x11 Interrupt Status-2 (Read Only) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.15. Offset 0x12 Interrupt Status-3 (Read Only) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.16. Offset 0x13 Interrupt Status-4 (Read Only) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.17. Offset 0x14 Interrupt Status-5 (Read Only)

Bit	Name	R/W	Default	Description
7	INTB*PCIE (PCIE_INTR_L)	R	1	1: No interrupt 0: There is INTR from PCIE of MAC
6	INTB*FAN (FAN_INT_L)	R	1	1: No interrupt: All 6 Fans ok 0: There is INTR from FAN: at least one of 6 Fans Fail.
5	INTB*Clock 82P33731 (82P3371_INT_REQ)	R	1	1: No interrupt 0: There is INTR from Clock Gen. 82P33731

4	INTB*CPLD3 (CPLD3_INT)	R	1	1: No interrupt 0: There is INTR from CPLD3
3	INTB*CPLD2 (CPLD2_INT)	R	1	1: No interrupt 0: There is INTR from CPLD2
2	INTB* LM75_2 (LM75BD21_INT)	R	1	1: No interrupt 0: There is INTR from LM75_2
1	INTB* LM75_1 (LM75BD1_INT)	R	1	1: No interrupt 0: There is INTR from LM75_1
0	INTB* LM75_0 (LM75BD0_INT)	R	1	1: No interrupt 0: There is INTR from LM75_0

1.4.18. Offset 0x15 Interrupt Status-6 (Read Only)

Bit	Name	R/W	Default	Description
7:5	Reserved		1	
4	CPLD234_INT_CPU	R	1	
3	SYS_CPLD_INT_CPU	R	1	
2	M1_MINT_L (INT_MGMT_PHY_N)	R	1	1: No interrupt 0: There is INTR from PHY (BCM54616S)
1	Reserved			
0	INTB*MAC (MAC_INT_L)	R	1	1: No interrupt 0: There is INTR from MAC

1.4.19. Offset 0x20 Interrupt Mask-1 (Read Only) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.20. Offset 0x21 Interrupt Mask-2 (Read Only) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.21. Offset 0x22 Interrupt Mask-3 (Read Only) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.22. Offset 0x23 Interrupt Mask-4 (Read Only) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.23. Offset 0x24 Interrupt Mask-5 (Read & Write)

Bit	Name	R/W	Default	Description

7	MASK*PCIE (PCIE_INTR_L)	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
6	MASK*FAN (FAN_INT_L)	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
5	MASK*82P33731 (82P33731_INT_REQ)	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
4	MASK*CPLD3 (CPLD3_INT)	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	MASK*CPLD2 (CPLD2_INT)	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	MASK*CPLD2 (CPLD4_INT)	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	MASK* LM75_1 (LM75BD1_INT)	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
0	MASK* LM75_0 (LM75BD0_INT)	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

1.4.24. Offset 0x25 Interrupt Mask-6 (Read & Write)

Bit	Name	R/W	Default	Description
7:5	Reserved			
4	MASK*CPLD234_INT_CPU (CPLD234_INT_CPU)	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
3	MASK*SYS_CPLD_INT_CPU (SYS_CPLD_INT_CPU)	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
2	MASK*M1_MINT_L (INT_MGMT_PHY_N)	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
1	Reserved			
0	MASK*MAC (MAC_INT_L)	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU

1.4.25. Offset 0x30 Module Present-1 (Read Only) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.26. Offset 0x31 Module Present-2 (Read Only) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.27. Offset 0x32 Module Present-3 (Read Only) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.28. Offset 0x33 Module Present-4 (Read Only) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.4.29. Offset 0x40 Recovery_CLKvalid & 1PPS Mask (Read & Write)

Bit	Name	R/W	Default	Description
7	Reserved			
6	CPU_THERMALTRIP_R	NA	NA	No use
5	CPU_PROCHOT_R	NA	NA	No use
4	PCIE_WAKE_L	R	1	
3	L1_RCVRD_CLK_VALID_backup (L1_RCVRD_CLK_VALID_bkup)	R		1:L1_RCVRD_CLK backup is VALID 0:L1_RCVRD_CLK backup is not VALID
2	L1_RCVRD_CLK_VALID	R		1:L1_RCVRD_CLK is VALID 0:L1_RCVRD_CLK is not VALID
1	Mask *1PPS_GPIO2 (1PPS_GPIO2_R)	R/W	0	1: CPLD blocks 1pps signal to1pps_GPIO2 0: CPLD passes 1pps signal to1pps_GPIO2
0	Mask *1PPS_CPU (1PPS_CPU_R)	R/W	0	1: CPLD blocks 1pps signal to CPU 0: CPLD passes 1pps signal to CPU

1.4.30. Offset 0x41 System LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7	LOC_A	R/W	1	1: LOC Blue LED off 0: LOC Blue LED on
6:4	Reversed			
3:2	FAN_A, FAN_G,	R/W	00	00: Release FAN LED control form S/W, FAN LED is lighted based on FAN hardware status signal. 01: Solid Amber by S/W, means FAN operates abnormally. 10: Solid Green by S/W, means FAN operates normally. 11: LED off by S/W
1	DIAG_A	R/W	1	1: Diag Red LED off 0: Diag Red LED on
0	DIAG_G	R/W	0	1: Diag Green LED off 0: Diag Green LED on

1.4.31. Offset 0x42 System LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:4	Reserved			
3	PSU2_A	R/W	0	00: Release PSU2 LED control from S/W. PSU2 LED is lighted based on PSU2 hardware status signals. 01: Solid Amber by S/W, means PSU present or the power is failed. 10: Solid Green by S/W. means PSU operates normally. 11: LED off by S/W.
2	PSU2_G	R/W	0	
1	PSU1_A	R/W	0	00: Release PSU1 LED control from S/W. PSU1 LED is lighted based on PSU1 hardware status signals. Green: This power is operation normally Amber: PWR present but no power on or power fault Off : Power supply not present 01: Solid Amber by S/W, means PSU present or the power is failed. 10: Solid Green by S/W. means PSU operates normally. 11: LED off by S/W.
0	PSU1_G	R/W	0	

1.4.32. Offset 0x43 System LED -3 (Read& Write) (Reserved)

Bit	Name	R/W	Default	Description
7:0	SYSLED_R_ PWM_[7:0]	R/W	0xFF	0: 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.4.33. Offset 0x44 System LED -4 (Read& Write) (Reserved)

Bit	Name	R/W	Default	Description
7:0	SYSLED_G_ PWM_[7:0]	R/W	0xFF	0: 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.4.34. Offset 0x45 System LED -5 (Read& Write) (Reserved)

Bit	Name	R/W	Default	Description
7:0	SYSLED_B_ PWM_[7:0]	R/W	0xFF	0: 0 %duty cycle

				01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.4.35. Offset 0x47 USB (Read & Write)

Bit	Name	R/W	Default	Description
7:4	Reserved			
3	USB enable	R/W	1	1: USB enable 0: USB disable
2	Reserved			
1	USB1_PWRFAULT_MASK	R/W	1	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU USB1_PWRFAULT interrupt Mask
0	USB_PWRFLT_N	R		1: No interrupt from 0: There is INTR from USB

*USB1_INT will occur when USB_PWRFLT_N active low and USB1_PWRFAULT_MASK set 0

1.4.36. Offset 0x48 MISC (Read & Write)

Bit	Name	R/W	Default	Description
7	Reserved			
6	Reserved			
5	MII_Mode_Sel (INTERF_SEL0)	R/W	0	0:SGMII 1:RGMII
4	GEN3_CPU_FB	R/W		(Reserved).
3	Hitless (Hitless_enable)	R/W		For field upgrade
2	EE_WP	R/W	0	1: Enable EEPROM's Write protection 0: Disable EEPROM's Write protection
1:0	PS[2:1]_ON	R/W	0	1: shutdown power supply 0: Enable power supply

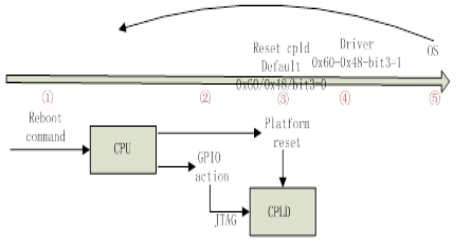
1.4.37. Offset 0x49 FPGA control (Read & Write) (Reserved)

Bit	Name	R/W	Default	Description
7	CONF_DONE_DIR	R/W	1	1: CONF_DONE Pin as input 0: CONF_DONE Pin as output
6	NCE_DIR	R/W	1	1: nCE Pin as input 0: nCE Pin as output
5	NCONFIG_DIR	R/W	1	1: nCONFIG Pin as input 0: nCONFIG Pin as output
4	NSTATUS_DIR	R/W	1	1: nSTATUS Pin as input 0: nSTATUS Pin as output

3	CONF_DONE	R/W	1	1: CONF_DONE driven high 0: CONF_DONE driven low
2	NCE	R/W	0	1: NCE driven high 0: NCE driven low
1	NCONFIG	R/W	1	1: NCONFIG driven high 0: NCONFIG driven low
0	NSTATUS	R/W	1	1: NSTATUS driven high 0: NSTATUS driven low

1.4.38. Offset 0x50 MISC-2 (Read & Write)

Bit	Name	R/W	Default	Description
7	5P49V590_CLK_SEL	R/W	0	Input clock select. Selects the active input reference source in manual switchover mode. 0 = XIN/REF, XOUT (default) 1 = CLKIN, CLKINB
6	MHOST1_BOOT_DEV	R/W	0	1: Tightly Coupled Memory or TCM in iProc (Default). 0: Boot ROM inside iProc (Reserved).
5	MHOST0_BOOT_DEV	R/W	1	1:mHost0 comes out of reset and begins executing code based on the setting of the BOOT_DEV [2:0] strap signals. 0:mHost0 is held in reset. NOTE: This signal must be pulled high.
4	Reserved			
3	SW1_Select	R/W	1	1: Select SPI mode of FPGA field upgrade 0: Select JTAG mode of CPLD field upgrade (SW Needs Set “1” before warm reset. (NOTE: When warm rest, CPU GPIO will send the unknow signal to CPLD JTAG, it will cause the CPLD jump into the reset mode. We need to set the SW1_SELECT as “1” (reg 0x48[3] of CPLD1) when power ON, or before warm reset to ensure the CPLD JTAG is clear.) (SW1_SELECT as “1” is hold till reboot finished and return to “0” when Platform reset occur). As the default setting to”1” SW needs use two .vme file to field upgrade. 1. Only System CPLD (Need to take care the initial reset when CPLD filed upgrade) 2. CPLD2, CPLD3… As the default setting to”0” When reboot, CPLD may be effected the

				unknow GPIO state when CPU be reset, the CPLD may jump into the reset state. (NOTE: When field upgrade SW1 Default needs to set to "0" (CPU=JTAG). Otherwise CPLD2/3 will be stuck when programing. Need to ask Lattice how to change the device sequence when program) 
2:0	BOOT_DEV[2:0]	R/W	0	3'b000: Load all necessary code from QSPI flash attached to IP_QSPI interface and begin execution. (others): Reserved. Note: It is a requirement that these signals are set to 3'b000.

- This register will not be reset, the value will return to Default only when re-power.

1.4.39. Offset 0x51 CP2112-1 (Read & Write)

Bit	Name	R/W	Default	Description
7:6	Reserved			
5	USB2112_BRDG_RST	R/W	1	1: normal 0: enable
4	GPIO.0_CLK (CP2112_CPLD_GPIO7)	R/W	0	In CLK mode, this pin outputs a clock signal whose frequency is configurable.
3	GPIO.0_RXT (CP2112_CPLD_GPIO1)	R/W	1	1: The pin is logic high when a transmission is not in progress.
2	GPIO.0_TXT (CP2112_CPLD_GPIO0)	R/W	1	1: The pin is logic high when a transmission is not in progress.
1:0	Reserved			

1.4.40. Offset 0x51 CP2112-2 (Read & Write)

Bit	Name	R/W	Default	Description
7	Reserved			
6	GPIO.6 (CP2112_CPLD_GPIO6)	R/W	0	user-configurable input or output.
5	GPIO.5 (CP2112_CPLD_GPIO5)	R/W	0	user-configurable input or output.
4	GPIO.4 (CP2112_CPLD_GPIO4)	R/W	0	user-configurable input or output.
3	GPIO.3 (CP2112_CPLD_GPIO3)	R/W	0	user-configurable input or output.
2	GPIO.2 (CP2112_CPLD_GPIO2)	R/W	0	user-configurable input or output.

1:0	Reserved			

1.5. CPLD 2 Register

Register	Offset	R/W	Default	Description
Reserved	0x00			
CPLD_VERSION	0x01	R		CPLD Version information
I2C_Select	0x02	R/W	0xFF	Select I2C bus for QSFP-DD Port 1 to Port 16
QSFP-DD_INT_1	0x10	R	0xFF	Interrupt status when a QSFP-DD is present or not. For QSFP-DD port 1 to port 8
QSFP-DD_INT_2	0x11	R	0xFF	Interrupt status when a QSFP-DD is present or not. For QSFP-DD port 9 to port 16
QSFP-DD_INT_MASK_1	0x18	R/W		
QSFP-DD_INT_MASK_2	0x19	R/W		
QSFP-DD_ MODPRSNT_N_1	0x20	R		QSFP-DD Present status for QSFP-DD port 1 to port 8
QSFP-DD_ MODPRSNT_N_2	0x21	R		QSFP-DD Present status for QSFP-DD port 9 to port 16
QSFP-DD_PRSNT_INT_1	0x24	R		
QSFP-DD_PRSNT_INT_2	0x25	R		
QSFP-DD_ PRSNT_MASK_1	0x28	R/W		
QSFP-DD_ PRSNT_MASK_2	0x29	R/W		
QSFP-DD_RESET_1	0x30	R/W		TX Reset status for QSFP-DD port 1 to port 8
QSFP-DD_RESET_2	0x31	R/W		TX Reset status for QSFP-DD port 9 to port 16
1x400G_RGB_LED-G	0X41	R/W		1x400G Green of RGB LED PWM
1x400G_RGB_ED-R	0X42	R/W		1x400G Red of RGB LED PWM
1x400G_RGB_LED-B	0X43	R/W		1x400G Blue of RGB LED PWM
1x200G_RGB_LED-G	0x44	R/W		1x200G Green of RGB LED PWM
1x200G_RGB_LED-R	0x45	R/W		1x200G Red of RGB LED PWM
1x200G_RGB_LED-B	0x46	R/W		1x200G Blue of RGB LED PWM
4x100G_RGB_LED-	0x47	R/W		4x100G Green of RGB LED PWM

G				
4x100G_RGB_LED-R	0x48	R/W		4x100G Red of RGB LED PWM
4x100G_RGB_LED-B	0x49	R/W		4x100G Blue of RGB LED PWM
4x50G_RGB_LED-G	0x51	R/W		4x50G Green of RGB LED PWM
4x50G_RGB_LED-R	0x52	R/W		4x50G Red of RGB LED PWM
4x50G_RGB_LED-B	0x53	R/W		4x50G Blue of RGB LED PWM
2x200G_RGB_LED-G	0x54	R/W		2x200G Green of RGB LED PWM
2x200G_RGB_LED-R	0x55	R/W		2x200G Red of RGB LED PWM
2x200G_RGB_LED-B	0x56	R/W		2x200G Blue of RGB LED PWM
8x50G_RGB_LED-G	0x57	R/W		8x50G Green of RGB LED PWM
8x50G_RGB_LED-R	0x58	R/W		8x50G Red of RGB LED PWM
8x50G_RGB_LED-B	0x59	R/W		8x50G Blue of RGB LED PWM
2x100G_RGB_LED-G	0x61	R/W		2x100G Green of RGB LED PWM
2x100G_RGB_LED-R	0x62	R/W		2x100G Red of RGB LED PWM
2x100G_RGB_LED-B	0x63	R/W		2x100G Blue of RGB LED PWM
8x25G_RGB_LED-G	0x64	R/W		8x25G Green of RGB LED PWM
8x25G_RGB_LED-R	0x65	R/W		8x25G Red of RGB LED PWM
8x25G_RGB_LED-B	0x66	R/W		8x25G Blue of RGB LED PWM
2x40G_RGB_LED-G	0x67	R/W		2x40G Green of RGB LED PWM
2x40G_RGB_LED-R	0x68	R/W		2x40G Red of RGB LED PWM
2x40G_RGB_LED-B	0x69	R/W		2x40G Blue of RGB LED PWM
8x10G_RGB_LED-G	0x71	R/W		8x10G Green of RGB LED PWM
8x10G_RGB_LED-R	0x72	R/W		8x10G Red of RGB LED PWM
8x10G_RGB_LED-	0x73	R/W		8x10G Blue of RGB LED PWM

B				

Table 1-15 CPLD2 I/O Register Table

1.5.1. Offset 0x00 Reserved

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.5.2. Offset 0x01 CPLD Version (Read Only)

Bit	Name	R/W	Default	Description
7:4	Reserved			
3:0	CPLD Version[3:0]	R		CPLD Version

1.5.3. Offset 0x02 I2C_Select (Read & Write) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			
	I2C_Select[3:0]			I2C_Select Bit0 00000: Select I2C bus for QSFP-DD Port 1 00001: Select I2C bus for QSFP-DD Port 2 …….. FF: No select I2C bus

1.5.4. Offset 0x10 QSFP-DD_INT_1 (Read Only)

Bit	Name	R/W	Default	Description
7:0	QSFP-DD_INT_ Port[8:1]			QSFP-DD_INT_ Port 1 to Port 8 0: Generates an interrupt when a QSFP-DD is present for QSFP-DD Port 1: No interrupt

Note: Register will clear the interrupt automatically after reading.

1.5.5. Offset 0x11 QSFP-DD_INT_2 (Read Only)

Bit	Name	R/W	Default	Description
7:2	Reserved			
2:0	QSFP-DD_INT_ Port[16:9]			QSFP-DD_INT_ Port 9 to Port 16 0: Generates an interrupt when a QSFP-DD is present for QSFP-DD Port 1: No interrupt

Note: Register will clear the interrupt automatically after reading.

1.5.6. Offset 0x18 QSFP-DD_Mask INT_1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	QSFP-DD_MSK INT_ Port[8:1]			

1.5.7. Offset 0x19 QSFP-DD_Mask INT_2 (Read & Write)

Bit	Name	R/W	Default	Description
7:2	Reserved			
2:0	QSFP-DD_MSK INT_ Port[16:9]			

1.5.8. Offset 0x20 QSFP-DD_MODPRSNT_1 (Read Only)

Bit	Name	R/W	Default	Description
7:0	QSFP-DD_MODPRSNT_N Port[8:1]			EX: P32_MODPRSNT_N QSFP-DD Present signal for Port 1 to Port 8 0: There is a QSFP-DD XCVR installed. 1: QSFP-DD port has been uninstalled

1.5.9. Offset 0x21 QSFP-DD_MODPRSNT_2 (Read Only)

Bit	Name	R/W	Default	Description
7:3	Reserved			
2:0	QSFP-DD_MODPRSNT_N Port[16:9]			EX: P32_MODPRSNT_N QSFP-DD Present signal for Port 9 to Port 16 0: There is a QSFP-DD XCVR installed. 1: QSFP-DD port has been uninstalled

1.5.10. Offset 0x24 QSFP-DD_PRSNT_INT_1 (Read Only)

Bit	Name	R/W	Default	Description
7:0	QSFP-DD_PRSNT_INT Port[8:1]			

Note: Register will clear the interrupt automatically after reading.

1.5.11. Offset 0x25 QSFP-DD_PRSNT_INT_2 (Read Only)

Bit	Name	R/W	Default	Description
7:3	Reserved			
2:0	QSFP-DD_PRSNT_INT Port[16:9]			

Note: Register will clear the interrupt automatically after reading.

1.5.12. Offset 0x28 QSFP-DD_PRSNT_MASK_1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	QSFP-DD_PRSNT_Mask Port[8:1]			

1.5.13. Offset 0x29 QSFP-DD_PRSNT_MASK_2 (Read & Write)

Bit	Name	R/W	Default	Description
7:3	Reserved			
2:0	QSFP-DD_PRSNT_Mask Port[16:9]			

1.5.14. Offset 0x30 QSFP-DD_RESET_1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	QSFP-DD Reset Port[8:1]			EX: P11_RESET_N QSFP-DD Reset status for Port 1 to Port 8 0: QSFP-DD is placed in reset state. 1: QSFP-DD is placed in normal operation state.

1.5.15. Offset 0x31 QSFP-DD_RESET_2 (Read & Write)

Bit	Name	R/W	Default	Description
7:3	Reserved			
2:0	QSFP-DD Reset Port[16:9]			EX: P11_RESET_N QSFP-DD Reset status for Port 9 to Port 16 0: QSFP-DD is placed in reset state. 1: QSFP-DD is placed in normal operation state.

1.5.16. Offset 0x41 400G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	400G_G_ PWM_[7:0]	R/W	0xFF	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.17. Offset 0x42 400G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	400G_R_ PWM_[7:0]	R/W	0xFF	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.18. Offset 0x43 400G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	400G_B_ PWM_[7:0]	R/W	0x00	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.19. Offset 0x44 1x200G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	1x200G_G_ PWM_[7:0]	R/W	0x00	0 : 0 %duty cycle 01: 1/255 % duty cycle

				02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.20. Offset 0x45 1x200G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	1x200G_R_ PWM_[7:0]	R/W	0x00	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.21. Offset 0x46 1x200G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	1x200G_B_ PWM_[7:0]	R/W	0xFF	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.22. Offset 0x47 4x100G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	4x100G_G_ PWM_[7:0]	R/W	0x80	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.23. Offset 0x48 4x100G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	4x100G_R_ PWM_[7:0]	R/W	0x00	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle

				…… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.24. Offset 0x49 4x100G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	4x100G_B_ PWM_[7:0]	R/W	0xFF	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.25. Offset 0x51 4x50G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	4x50G_G_ PWM_[7:0]	R/W	0xFF	00 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.26. Offset 0x52 4x50G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	4x50G_R_ PWM_[7:0]	R/W	0x00	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.27. Offset 0x53 4x50G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	4x50G_B_ PWM_[7:0]	R/W	0xFF	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle ……

				FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.28. Offset 0x54 2x200G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x200G_G_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle良率 …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.29. Offset 0x55 2x200G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x200G_R_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.30. Offset 0x56 2x200G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x200G_B_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.31. Offset 0x57 8x50G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x50G_G_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle良率 …… FE: 254/255 % duty cycle

				FF: 255/255 % duty cycle

1.5.32. Offset 0x58 8x50G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x50G_R_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.33. Offset 0x59 8x50G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x50G_B_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.34. Offset 0x61 2x100G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x100G_G_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle良率 …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.35. Offset 0x62 2x100G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x100G_R_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.36. Offset 0x63 2x100G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x100G_B_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.37. Offset 0x64 8x25G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x25G_G_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle良率 …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.38. Offset 0x65 8x25G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x25G_R_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.39. Offset 0x66 8x25G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x25G_B_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.40. Offset 0x67 2x40G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x40G _G_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle良率 …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.41. Offset 0x68 2x40G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x40G_R_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.42. Offset 0x69 2x40G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x40G_B_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.43. Offset 0x71 8x10G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x10G_G_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle良率 …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.44. Offset 0x72 8x10G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description

7:0	8x10G_R_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.5.45. Offset 0x73 8x10G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x10G_B_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6. **CPLD 3** Register

Register	Offset	R/W	Default	Description
Reserved	0x00			
CPLD_VERSION	0x01	R		CPLD Version information
I2C_Select	0x02			
QSFP-DD_INT_1	0x10	R		Interrupt status when a QSFP-DD is present or not. For QSFP-DD port 17 to port 24
QSFP-DD_INT_2	0x11	R		Interrupt status when a QSFP-DD is present or not. For QSFP-DD port 250 to port 32
QSFP-DD_INT_MASK_1	0x18	R/W		
QSFP-DD_INT_MASK_2	0x19	R/W		
QSFP-DD_MODPRSNT_N_1	0x20	R		QSFP-DD Present status for QSFP-DD port 17 to port 24
QSFP-DD_MODPRSNT_N_2	0x21	R		QSFP-DD Present status for QSFP-DD port 25 to port 32
QSFP-DD_PRSNT_INT_1	0x24	R		
QSFP-DD_PRSNT_INT_2	0x25	R		
QSFP-DD_PRSNT_MASK_1	0x28	R/W		
QSFP-DD_PRSNT_MASK_2	0x29	R/W		
QSFP-DD_RESET_1	0x30	R/W		TX Reset status for QSFP-DD port 17 to port 24
QSFP-DD_RESET_2	0x31	R/W		TX Reset status for QSFP-DD port 25 to port 32
1x400G_RGB_LED-G	0X41	R/W		1x400G Green of RGB LED PWM
1x400G_RGB_ED-R	0X42	R/W		1x400G Red of RGB LED PWM
1x400G_RGB_LED-B	0X43	R/W		1x400G Blue of RGB LED PWM
1x200G_RGB_LED-G	0x44	R/W		1x200G Green of RGB LED PWM
1x200G_RGB_LED-R	0x45	R/W		1x200G Red of RGB LED PWM
1x200G_RGB_LED-	0x46	R/W		1x200G Blue of RGB LED PWM

B				
4x100G_RGB_LED-G	0x47	R/W		4x100G Green of RGB LED PWM
4x100G_RGB_LED-R	0x48	R/W		4x100G Red of RGB LED PWM
4x100G_RGB_LED-B	0x49	R/W		4x100G Blue of RGB LED PWM
4x50G_RGB_LED-G	0x51	R/W		4x50G Green of RGB LED PWM
4x50G_RGB_LED-R	0x52	R/W		4x50G Red of RGB LED PWM
4x50G_RGB_LED-B	0x53	R/W		4x50G Blue of RGB LED PWM
2x200G_RGB_LED-G	0x54	R/W		2x200G Green of RGB LED PWM
2x200G_RGB_LED-R	0x55	R/W		2x200G Red of RGB LED PWM
2x200G_RGB_LED-B	0x56	R/W		2x200G Blue of RGB LED PWM
8x50G_RGB_LED-G	0x57	R/W		8x50G Green of RGB LED PWM
8x50G_RGB_LED-R	0x58	R/W		8x50G Red of RGB LED PWM
8x50G_RGB_LED-B	0x59	R/W		8x50G Blue of RGB LED PWM
2x100G_RGB_LED-G	0x61	R/W		2x100G Green of RGB LED PWM
2x100G_RGB_LED-R	0x62	R/W		2x100G Red of RGB LED PWM
2x100G_RGB_LED-B	0x63	R/W		2x100G Blue of RGB LED PWM
8x25G_RGB_LED-G	0x64	R/W		8x25G Green of RGB LED PWM
8x25G_RGB_LED-R	0x65	R/W		8x25G Red of RGB LED PWM
8x25G_RGB_LED-B	0x66	R/W		8x25G Blue of RGB LED PWM
2x40G_RGB_LED-G	0x67	R/W		2x40G Green of RGB LED PWM
2x40G_RGB_LED-R	0x68	R/W		2x40G Red of RGB LED PWM
2x40G_RGB_LED-B	0x69	R/W		2x40G Blue of RGB LED PWM
8x10G_RGB_LED-G	0x71	R/W		8x10G Green of RGB LED PWM
8x10G_RGB_LED-	0x72	R/W		8x10G Red of RGB LED PWM

R				
8x10G_RGB_LED-B	0x73	R/W		8x10G Blue of RGB LED PWM

Table 1-16 CPLD3 I/O Register Table

1.6.1. Offset 0x00 Reserved

Bit	Name	R/W	Default	Description
7:0	Reserved			

1.6.2. Offset 0x01 CPLD Version (Read Only)

Bit	Name	R/W	Default	Description
7:4	Reserved			
3:0	CPLD Version[3:0]	R		CPLD Version

1.6.3. Offset 0x02 I2C_Select (Read & Write) (Reserved)

Bit	Name	R/W	Default	Description
7:0	Reserved			
	I2C_Select[3:0]			I2C_Select Bit0 00000: Select I2C bus for QSFP-DD Port 1 00001: Select I2C bus for QSFP-DD Port 2 …… FF: No select I2C bus

1.6.4. Offset 0x10 QSFP-DD_INT_1 (Read Only)

Bit	Name	R/W	Default	Description
7:0	QSFP-DD_INT_ Port[24:17]			QSFP-DD_INT_ Port 17 to Port 24 0: Generates an interrupt when a QSFP-DD is present for QSFP-DD Port 1: No interrupt

Note: Register will clear the interrupt automatically after reading.

1.6.5. Offset 0x11 QSFP-DD_INT_2 (Read Only)

Bit	Name	R/W	Default	Description
7:0	QSFP-DD_INT_ Port[32:25]			QSFP-DD_INT_ Port 25 to Port 32 0: Generates an interrupt when a QSFP-DD is present for QSFP-DD Port 1: No interrupt

Note: Register will clear the interrupt automatically after reading.

1.6.6. Offset 0x18 QSFP-DD_INT_MASK_1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	QSFP-DD_MSK INT_ Port[24:17]			

1.6.7. Offset 0x19 QSFP-DD_INT_MASK_2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	QSFP-DD_MSK INT_ Port[32:25]			

1.6.8. Offset 0x20 QSFP-DD_MODPRSNT_1 (Read Only)

Bit	Name	R/W	Default	Description

7:0	QSFP-DD_MODPRSNT_N Port[24:17]			EX: P32_MODPRSNT_N QSFP-DD Present signal for Port 17 to Port 24 0: There is a QSFP-DD XCVR installed. 1: QSFP-DD port has been uninstalled

1.6.9. Offset 0x21 QSFP-DD_MODPRSNT_2 (Read Only)

Bit	Name	R/W	Default	Description
7:3	Reserved			
2:0	QSFP-DD_MODPRSNT_N Port[32:25]			EX: P32_MODPRSNT_N QSFP-DD Present signal for Port 25 to Port 32 0: There is a QSFP-DD XCVR installed. 1: QSFP-DD port has been uninstalled

1.6.10. Offset 0x24 QSFP-DD_PRSNT_INT_1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	QSFP-DD_PRSNT_INT Port[24:17]			

Note: Register will clear the interrupt automatically after reading.

1.6.11. Offset 0x25 QSFP-DD_PRSNT_INT_2 (Read & Write)

Bit	Name	R/W	Default	Description
7:3	Reserved			
2:0	QSFP-DD_PRSNT_INT Port[32:25]			

Note: Register will clear the interrupt automatically after reading.

1.6.12. Offset 0x28 QSFP-DD_PRSNT_MASK_1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	QSFP-DD_PRSNT_Mask Port[24:17]			

1.6.13. Offset 0x29 QSFP-DD_PRSNT_MASK_2 (Read & Write)

Bit	Name	R/W	Default	Description
7:3	Reserved			
2:0	QSFP-DD_PRSNT_Mask Port[32:25]			

1.6.14. Offset 0x30 QSFP-DD_RESET_1 (Read Only)

Bit	Name	R/W	Default	Description
7:0	QSFP-DD Reset Port[24:17]			EX: P11_RESET_N QSFP-DD Reset status for Port 17 to Port 24 0: QSFP-DD is placed in reset state. 1: QSFP-DD is placed in normal operation state.

1.6.15. Offset 0x31 QSFP-DD_RESET_2 (Read Only)

Bit	Name	R/W	Default	Description
7:0	QSFP-DD Reset			EX: P11_RESET_N

	Port[32:25]			QSFP-DD Reset status for Port 25 to Port 32 0: QSFP-DD is placed in reset state. 1: QSFP-DD is placed in normal operation state.

1.6.16. Offset 0x41 400G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	400G_G_ PWM_[7:0]	R/W	0xFF	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.17. Offset 0x42 400G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	400G_R_ PWM_[7:0]	R/W	0xFF	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.18. Offset 0x43 400G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	400G_B_ PWM_[7:0]	R/W	0x00	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.19. Offset 0x44 1x200G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	1x200G_G_ PWM_[7:0]	R/W	0x00	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle

				FF: 255/255 % duty cycle

1.6.20. Offset 0x45 1x200G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	1x200G_R_ PWM_[7:0]	R/W	0x00	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.21. Offset 0x46 1x200G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	1x200G_B_ PWM_[7:0]	R/W	0x00	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.22. Offset 0x47 4x100G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	4x100G_G_ PWM_[7:0]	R/W	0x80	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.23. Offset 0x48 4x100G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	4x100G_R_ PWM_[7:0]	R/W	0x00	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.24. Offset 0x49 4x100G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	4x100G_B_ PWM_[7:0]	R/W	0xFF	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.25. Offset 0x51 4x50G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	4x50G_G_ PWM_[7:0]	R/W	0xFF	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle良率 …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.26. Offset 0x52 4x50G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	4x50G_R_ PWM_[7:0]	R/W	0x00	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.27. Offset 0x53 4x50G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	4x50G_B_ PWM_[7:0]	R/W	0xFF	0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.28. Offset 0x54 2x200G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x200G_G_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle良率 …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.29. Offset 0x55 2x200G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x200G_R_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.30. Offset 0x56 2x200G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x200G_B_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.31. Offset 0x57 8x50G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x50G_G_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle良率 …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.32. Offset 0x58 8x50G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description

7:0	8x50G_R_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.33. Offset 0x59 8x50G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x50G_B_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.34. Offset 0x61 2x100G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x100G_G_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle良率 …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.35. Offset 0x62 2x100G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x100G_R_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.36. Offset 0x63 2x100G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x100G_B_ PWM_[7:0]	R/W		0 : 0 %duty cycle

				01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.37. Offset 0x64 8x25G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x25G_G_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle良率 …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.38. Offset 0x65 8x25G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x25G_R_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.39. Offset 0x66 8x25G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x25G_B_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.40. Offset 0x67 2x40G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x40G _G_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle

				02: 2 / 255% duty cycle良率 …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.41. Offset 0x68 2x40G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x40G_R_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.42. Offset 0x69 2x40G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	2x40G_B_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.43. Offset 0x71 8x10G RGB LED -1 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x10G_G_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle良率 …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.44. Offset 0x72 8x10G RGB LED -2 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x10G_R_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle

				…… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.6.45. Offset 0x73 8x10G RGB LED -3 (Read & Write)

Bit	Name	R/W	Default	Description
7:0	8x10G_B_ PWM_[7:0]	R/W		0 : 0 %duty cycle 01: 1/255 % duty cycle 02: 2 / 255% duty cycle …… FE: 254/255 % duty cycle FF: 255/255 % duty cycle

1.7. Fan board Register

Address	Register	R/W	Default
0x00	Board Info	Read Only	0x03
0x01	CPLD version	Read Only	
0x04	Fan CPLD Reset	Read& Write	0x80
0x05	Interrupt Status	Read Only	0x80
0x06	Interrupt Mask	Read Only	0x00
0x0F	Fan Module Present	Read Only	0x3F
0x10	Fan Module Direction	Read Only	0x3F
0x11	Fan Module PWM	Read& Write	0x04
0x12	Front Fan1 Module Speed	Read Only	
0x13	Front Fan2 Module Speed	Read Only	
0x14	Front Fan3 Module Speed	Read Only	
0x15	Front Fan4 Module Speed	Read Only	
0x16	Front Fan5 Module Speed	Read Only	
0x17	Front Fan6 Module Speed	Read Only	
0x1C	LED Display-1	Read& Write	0x00
0x1D	LED Display-2	Read& Write	0x00
0x22	Rear Fan1 Module Speed	Read Only	
0x23	Rear Fan2 Module Speed	Read Only	
0x24	Rear Fan3 Module Speed	Read Only	
0x25	Rear Fan4 Module Speed	Read Only	
0x26	Rear Fan5 Module Speed	Read Only	
0x27	Rear Fan6 Module Speed	Read Only	
0x30	Fan Module Power enable	Read& Write	0x3F
0x31	Watchdog timer	Read& Write	0x06
0x32	Watchdog Maximum PWM value	Read& Write	0x0F
0x33	Watchdog disable	Read& Write	0x01

Table 1-17 Fan board CPLD I/O Register Table

1.7.1. Offset 0x00 Board Info (Read Only)

Bit	Name	R/W	Default	Description
7:5	Version_ID[2:0]	R	000	000: R0A 001: R0B 100: R01 Others: Reserved
4:2	Reserved			
1:0	Board_ID[1:0]	R	11	00: Reserved 01: ZZ project 10: Reserved 11: AO project

1.7.2. Offset 0x01 CPLD version (Read Only)

Bit	Name	R/W	Default	Description
7:0	CPLD_ver[7:0]	R	0x00	CPLD version

1.7.3. Offset 0x04 Fan CPLD Reset (Read & Write)

Bit	Name	R/W	Default	Description
7	Reset_CPLD	R/W	1	1: CPLD is placed in normal operation state. 0: CPLD is placed in reset state.
6:0	Reserved			

1.7.4. Offset 0x05 Interrupt Status (Read Only)

Bit	Name	R/W	Default	Description
7	Alarm_INTB_CPU	R	1	1: No interrupt 0: There is INTR toCPU
6:0	Reserved			

1.7.5. Offset 0x06 Interrupt Mask (Read Only)

Bit	Name	R/W	Default	Description
7	MASK*Fan_interrupt	R/W	0	1: CPLD blocks incoming the interrupt 0: CPLD passes the interrupt to CPU
6:0	Reserved			

1.7.6. Offset 0x0F Fan Module Present (Read Only)

Bit	Name	R/W	Default	Description
7:6	Reserved			
5	Fan_present6	R	1	1: Fan6 isn't inserted 0: Fan6 is inserted
4	Fan_present5	R	1	1: Fan5 isn't inserted 0: Fan5 is inserted
3	Fan_present4	R	1	1: Fan4 isn't inserted 0: Fan4 is inserted
2	Fan_present3	R	1	1: Fan3 isn't inserted 0: Fan3 is inserted
1	Fan_present2	R	1	1: Fan2 isn't inserted 0: Fan2 is inserted
0	Fan_present1	R	1	1: Fan1 isn't inserted 0: Fan1 is inserted

1.7.7. Offset 0x10 Fan Module Direction (Read Only)

Bit	Name	R/W	Default	Description

7:6	Reserved			
5	Fan_DIR6	R	1	1: The air flow of Fan6 is “front to back” 0: The air flow of Fan6 is “back to front”
4	Fan_DIR5	R	1	1: The air flow of Fan5 is “front to back” 0: The air flow of Fan5 is “back to front”
3	Fan_DIR4	R	1	1: The air flow of Fan4 s “front to back” 0: The air flow of Fan4 is “back to front”
2	Fan_DIR3	R	1	1: The air flow of Fan3 is “front to back” 0: The air flow of Fan3 is “back to front”
1	Fan_DIR2	R	1	1: The air flow of Fan2 is “front to back” 0: The air flow of Fan2 is “back to front”
0	Fan_DIR1	R	1	1: The air flow of Fan1 is “front to back” 0: The air flow of Fan1 is “back to front”

1.7.8. Offset 0x11 Fan Module PWM (Read & Write)

Bit	Name	R/W	Default	Description
7:4	Reserved	N/A	N/A	
3:0	Fan PWM [3:0]	R/W	0100	The value of this field will be forced to 4 if a value less than 4 is written. 0100 : 5 x 6.25% = 31.5% duty cycle 0101 : 6 x 6.25% = 37.5% duty cycle 0110: 7 x 6.25% = 43.75% duty cycle …… 1110: 15 x 6.25% = 93.75% duty cycle 1111: 16 x 6.25% = 100% duty cycle

1.7.9. Offset 0x12 Front Fan1 Module Speed (Read Only)

Bit	Name	R/W	Default	Description
7:0	Front_Fan1_Tach	R		0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇨ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.7.10. Offset 0x13 Front Fan2 Module Speed(Read Only)

Bit	Name	R/W	Default	Description
7:0	Front_Fan2_Tach	R		0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇨ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.7.11. Offset 0x14 Front Fan3 Module Speed (Read Only)

Bit	Name	R/W	Default	Description
7:0	Front_Fan3_Tach	R		0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇨ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.7.12. Offset 0x15 Front Fan4 Module Speed (Read Only)

Bit	Name	R/W	Default	Description
7:0	Front_Fan4_Tach	R		0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇨ Fan speed (RPM) = Reg_value * 100 EX: register value : 80

				The RPM value is 80*100 = 8000

1.7.13. Offset 0x16 Front Fan5 Module Speed (Read Only)

Bit	Name	R/W	Default	Description
7:0	Front_Fan5_Tach	R		0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇨ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.7.14. Offset 0x17 Front Fan6 Module Speed (Read Only)

Bit	Name	R/W	Default	Description
7:0	Front_Fan6_Tach	R		0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇨ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.7.15. Offset 0x1C LED Display-1 (Read & Write)

Bit	Name	R/W	Default	Description
7	PWM1 for LED_Fan5_R	R/W	0	1: Fan1 _LED is Red 0: off
6	PWM1 for LED_Fan5_G	R/W	0	1: Fan1 _LED is Green 0: off
5	PWM2 for LED_Fan4_R	R/W	0	1: Fan2 _LED is Red 0: off
4	PWM2 for LED_Fan4_G	R/W	0	1: Fan2 _LED is Green 0: off
3	PWM3 for LED_Fan3_R	R/W	0	1: Fan3 _LED is Red 0: off
2	PWM3 for LED_Fan3_G	R/W	0	1: Fan3 _LED is Green 0: off
1	PWM4 for LED_Fan2_R	R/W	0	1: Fan4 _LED is Red 0: off
0	PWM4 for LED_Fan2_G	R/W	0	1: Fan4 _LED is Green 0: off

1.7.16. Offset 0x1D LED Display-2 (Read & Write)

Bit	Name	R/W	Default	Description
7:4	Reserved			
3	PWM5 for LED_Fan1_R	R/W	0	1: Fan5 _LED is Red 0: off
2	PWM5 for LED_Fan1_G	R/W	0	1: Fan5 _LED is Green 0: off
1	PWM6 for LED_Fan6_R	R/W	0	1: Fan6 _LED is Red 0: off
0	PWM6 for LED_Fan6_G	R/W	0	1: Fan6 _LED is Green 0: off

1.7.17. Offset 0x22 Rear Fan1 Module Speed (Read Only)

Bit	Name	R/W	Default	Description
7:0	Rear_Fan1_Tach	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇨ Fan speed (RPM) = Reg_value * 100 EX: register value : 80

				The RPM value is 80*100 = 8000

1.7.18. Offset 0x23 Rear Fan2 Module Speed (Read Only)

Bit	Name	R/W	Default	Description
7:0	Rear_Fan2_Tach	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇨ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.7.19. Offset 0x24 Rear Fan3 Module Speed (Read Only)

Bit	Name	R/W	Default	Description
7:0	Rear_Fan3_Tach	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇨ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.7.20. Offset 0x25 Rear Fan4 Module Speed (Read Only)

Bit	Name	R/W	Default	Description
7:0	Rear_Fan4_Tach	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇨ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.7.21. Offset 0x26 Rear Fan5 Module Speed (Read Only)

Bit	Name	R/W	Default	Description
7:0	Rear_Fan5_Tach	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇨ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.7.22. Offset 0x27 Rear Fan6 Module Speed (Read Only)

Bit	Name	R/W	Default	Description
7:0	Rear_Fan6_Tach	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms ⇨ Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

1.7.23. Offset 0x30 Fan Module Power enable (Read & Write)

Bit	Name	R/W	Default	Description
7:6	Reserved			
5	Fan_Power6	R/W	1	1: Enable the fan Power 0: Disable the fan power
4	Fan_Power 5	R/W	1	1: Enable the fan Power 0: Disable the fan power
3	Fan_Power 4	R/W	1	1: Enable the fan Power 0: Disable the fan power
2	Fan_Power 3	R/W	1	1: Enable the fan Power 0: Disable the fan power
1	Fan_Power 2	R/W	1	1: Enable the fan Power

				0: Disable the fan power
0	Fan_Power 1	R/W	1	1: Enable the fan Power 0: Disable the fan power

1.7.24. Offset 0x31 Watchdog timer (Read & Write)

Bit	Name	R/W	Default	Description
7:0	Watchdog timer	R/W	0x06	A countdown timer with 1 second resolution. Default is 6 sec.

1.7.25. Offset 0x32 Watchdog Maximum PWM value (Read& Write)

Bit	Name	R/W	Default	Description
7:4	Reserved			
3:0	Watchdog Maximum PWM value	R/W	1111	This register's contents will be copied to the PWM register when the watchdog timer expires (WD == 0) The value of this field will be forced to 4 if a value less than 4 is written. 0100 : 5 x 6.25% = 31.5% duty cycle 0101 : 6 x 6.25% = 37.5% duty cycle 0110: 7 x 6.25% = 43.75% duty cycle …… 1110: 15 x 6.25% = 93.75% duty cycle 1111: 16 x 6.25% = 100% duty cycle

1.7.26. Offset 0x33 Watchdog disable (Read& Write)

Bit	Name	R/W	Default	Description
7:1	Reserved			
0	Watchdog disable	R/W	1	1: Enable the watchdog timer 0: Disable the watchdog timer

1.7.27. Offset 0x42 Fan LED (Read& Write)

Bit	Name	R/W	Default	Description
7	LED_Debug_mode	R/W	0	1:LED debug mode on 0:LED debug mode off
6:0	Reserved			

1.8. CPLD pin-out list

1.8.1. CPLD1 pin-out list

Pin Number	Pin Name	Net name	I/O	Active	Description
B12	PT21A	1PPS_CPU_R	O		1PPS_CPU to CPU Board
N15	PR18B	5P49V590_CLK_SEL	O		(Reserved), default=Low
P3	PL18B	82P33731_INT_REQ_CPLD_R	I	Low	Interrupt from 82P33731
P2	PL18C	82P33731_RST_CPLD_R	O	Low	CPLD1 issue RESET to 82P33731
A10	PT19A	ASC_ALERT_L		Low	
T12	PB23D	ASC_ASCCLK	I		
T14	PB26C	ASC_GPIO5_RV			
N12	PB26D	ASC_GPIO6_RV			
U15	PB27A	ASC_GPIO7_RV			
E10	PT22C	ASC_IN1	O	Low	CPLD1 issues RESET to ASC
R12	PB24C	ASC_RCLK			
U13	PB24A	ASC_RDAT			
L2	PL14B	ASC_RST_PLD1	I	Low	ASC issues RESET to CPLD1
D1	PL4D	ASC_RST_PLD1_CPU	O	Low	CPLD1 issues RESET to CPU after CPLD1 receives ASC_RST_PLD1
E9	PT20C/SCL/PCLKT0_0	ASC_SCL_CPLD1_R			
D10	PT20D/SDA/PCLKC0_0	ASC_SDA_CPLD1_R			
V14	PB24B	ASC_WDAT			
L18	PR15C	BCM56980_ROV0	I		ROV [0:7] to adjust Core Voltage (0.85V)
M18	PR15D	BCM56980_ROV1	I		ROV [0:7] to adjust Core Voltage (0.85V)
M17	PR16A	BCM56980_ROV2	I		ROV [0:7] to adjust Core Voltage (0.85V)
N18	PR16B	BCM56980_ROV3	I		ROV [0:7] to adjust Core Voltage (0.85V)
L14	PR16C	BCM56980_ROV4	I		ROV [0:7] to adjust Core Voltage (0.85V)
N17	PR16D	BCM56980_ROV5	I		ROV [0:7] to adjust Core Voltage (0.85V)
M15	PR17A	BCM56980_ROV6	I		ROV [0:7] to adjust Core Voltage (0.85V)
P18	PR17B	BCM56980_ROV7	I		ROV [0:7] to adjust Core Voltage (0.85V)
L4	PL15A	BOOT_DEV0_R			
M2	PL15B	BOOT_DEV1_R			
M1	PL15C	BOOT_DEV2_R			
P13	PB30C	BTB_CONN_RVS1_R			
K15	PR10B/PCLKC1_0	CP2112_CPLD_GPIO0			CP2112 setup function pin
K14	PR10C	CP2112_CPLD_GPIO1			CP2112 setup function pin
J18	PR10D	CP2112_CPLD_GPIO2			CP2112 setup function pin
K16	PR13A	CP2112_CPLD_GPIO3			CP2112 setup function pin
K12	PR13C	CP2112_CPLD_GPIO4			CP2112 setup function pin
K13	PR13D	CP2112_CPLD_GPIO5			CP2112 setup function pin
K18	PR14A	CP2112_CPLD_GPIO6			CP2112 setup function pin
K17	PR13B	CP2112_CPLD_GPIO7			CP2112 setup function pin
D5	PT11C	CPLD_RST	O	Low	CPLD1 generates RESET to CPLD2/CPLD3
E15	PR3A/R_GPLLT_IN	CPLD1_25MHZ	I		25MHZ Clock In
E14	PT28D/DONE	CPLD1_DONE			

C16	PT28C/INITN	CPLD1_INITN			
D11	PT23C/JTAGENB	CPLD1_JTAGENB			N/A
D12	PT23D/PROGRAMN	CPLD1_PROGRAMN			N/A
V11	PB21A	CPLD12_LEDC	O		Clock of LED stream to CPLD2
T11	PB20D	CPLD12_LEDD	O		Data of LED stream to CPLD2
V12	PB21B	CPLD12_LEDS	O		LED stream to CPLD2
T15	PB29A	CPLD13_LEDC	O		Clock of LED stream to CPLD3
R14	PB27D	CPLD13_LEDD	O		Data of LED stream to CPLD3
T16	PB29B	CPLD13_LEDS	O		LED stream to CPLD3
E1	PL5B	CPLD2_INT	I	Low	CPLD2 generates Interrupt to CPLD1
E2	PL5A	CPLD234_INT_CPU	O		CPLD1 generates Interrupt to CPU board
H5	PL5D	CPLD3_INT	I		CPLD3 generates Interupt to CPLD1
A4	PT12A	CPU_JTAG_RST			
E8	PT18C	CPU_PROCHOT_R	I		
C11	PT21B	CPU_THERMALTRIP_R	I		
P5	PB4C	DIAG_B	O	Low	LED:System self-diagnostic test
R6	PB4D	DIAG_G	O	Low	LED: System self-diagnostic test successfully completed.
R5	PB6C	DIAG_R	O	Low	LED:System self-diagnostic test
B10	PT19B	EE_WP	O	High	Enable EEPROM write-protected 1: enable write-protected 0: disable write-protected.
T17	PR20D	EN_USB_VCC5P0_R	O	High	Enanle the Power IC for USB_VCC5P0
T18	PR19B	EN_VCC5V_R	O	High	Enanle the Power IC for VCC5V
R16	PR20C	EN_VDD_0P8_R	O	High	Enanle the Power IC for VDD_0P8
P15	PR20A	EN_VDD_0P9_R	O	High	Enanle the Power IC for VDD_0P9
U18	PR20B	EN_VDD_1P2_R	O	High	Enanle the Power IC for VDD1P2
N14	PR19D	EN_VDD_1P8_R	O	High	Enanle the Power IC for VDD1P8
P16	PR19A	EN_VDD1P2_PHY_R	O	High	Enanle the Power IC for VDD1P2_PHY
R17	PR19C	EN_VDD3P3_R	O	High	Enanle the Power IC for VDD3P3
N7	PB7C	FAN_B	O	Low	PWM mechanism of FAN LED on the front panel to show FAN status
P7	PB7D	FAN_G	O	Low	PWM mechanism of FAN LED on the front panel to show FAN status
H1	PL8B	FAN_IDLE	O		
G2	PL7A	FAN_INT_L	I	Low	FAN interrupt from FAN Board
V4	PB6B	FAN_R	O	Low	PWM mechanism of FAN LED on the front panel to show FAN status
F4	PL3B/L_GPLLC_FB	FAN_SCL_1_R			FAN I2C Clock 1: connected to FAN board & CPU Board
F5	PL3D	FAN_SCL_2_R			FAN I2C Clock 2: connected to FAN board.
E3	PL3C	FAN_SDA_1_R			FAN I2C DATA 1
D2	PL4A/L_GPLLT_IN	FAN_SDA_2_R			FAN I2C DATA 2
P14	PB30D	HITLESS_ENABLE_R			(Reserved)
N11	PB21C	HVO2_CPLD			
F10	PT21D	I2C_0_SCL_CPLD1_R	I		CPU to CPLD1 I2C Clock
A11	PT22A	I2C_0_SDA_CPLD1_R	I/O		CPU to/from CPLD1 I2C Data.
P6	PB3D	I2C_1_SCL_CPLDSYS			

T3	PB4A/CSSPIN	I2C_1_SDA_CPLDSYS			
F3	PL4C	INT_MGMT_PHY_N	I	Low	BCM54616S issue Interrupt to CPLD1
P12	PB27C	INTERF_SEL0			
E18	PR7A	IP_LED_CLK0	I		Clock 0 of LED Stream connected to MAC
H16	PR7C	IP_LED_CLK1	I		Clock 1 of LED Stream connected to MAC
J15	PR8A	IP_LED_CLK2	I		Clock 2 of LED Stream connected to MAC
J13	PR8C	IP_LED_CLK3	I		Clock 3 of LED Stream connected to MAC
G17	PR7B	IP_LED_DATA0	I		Data 0 of LED Stream connected to MAC
F18	PR7D	IP_LED_DATA1	I		Data 1 of LED Stream connected to MAC
H17	PR8B	IP_LED_DATA2	I		Data 2 of LED Stream connected to MAC
G18	PR8D	IP_LED_DATA3	I		Data 3 of LED Stream connected to MAC
B1	PL2A	LM75BD_SCLK_R	O		Clock of I2C Bus connected to three LM75
C2	PL2B	LM75BD_SDA_R	I/O		Data of I2C Bus connected to three LM75
H3	PL7C	LM75BD0_INT	I		Device 0 of LM75 (0x48) issues Interrupt to CPLD1
H4	PL7D	LM75BD1_INT	I		Device 1 of LM75 (0x49) issues Interrupt to CPLD1
H2	PL8A	LM75BD2_INT	I		Device 2 of LM75 (0x4A) issues Interrupt to CPLD1
U5	PB7B	LOC_B	O	Low	PWM mechanism of LOC LED : Flashing by remote management command, Assists the technician in finding the right device for service in the rsck.
V3	PB6A	LOC_G	O	Low	PWM mechanism of LOC LED : Flashing by remote management command, Assists the technician in finding the right device for service in the rsck.
U4	PB4B	LOC_R	O	Low	PWM mechanism of LOC LED : Flashing by remote management command, Assists the technician in finding the right device for service in the rsck.
G3	PL6B/PCLKC5_0	MAC_INT_L	I	Low	MAC issues Interrupt to CPLD1
P4	PL20C	MAC_RESET_N	O	Low	CPLD1 issues RESET to MAC
B4	PT11B	MANU_RST	O	Low	CPLD1 issues RESET to CPU Board.
G5	PL4B/L_GPLLC_IN	MGMT_PHY_RST_N	O	Low	CPLD1 issues RESET to PHY (BCM54616S)
N1	PL16A	MHOST0_BOOT_DEV_R			
N2	PL16B	MHOST1_BOOT_DEV_R			
B6	PT13A	PCA9548_1_RESET_N	O	Low	CPLD1 issues RESET to PCA9548 (U62) for Port 1~8
C3	PT10A	PCA9548_2_RESET_N	O	Low	CPLD1 issues RESET to PCA9548 (U65) for Port 9~16
C4	PT10B	PCA9548_3_RESET_N	O	Low	CPLD1 issues RESET to PCA9548 (U46) for Port 17~24.
F7	PT10C	PCA9548_4_RESET_N	O	Low	CPLD1 issues RESET to PCA9548 (U43) for Port 25~32
E6	PT10D	PCA9548_5_RESET_N	O	Low	CPLD1 issues RESET to PCA9548 (U2) for FAN, LM75 ,EEPROM, CPLDs, ASC
A3	PT11A	PCA9548_6_RESET_N	O	Low	CPLD1 issues RESET to PCA9548 (U60) for USB Hub

D6	PT12D	PCA9548_RESET_N	O	Low	CPLD1 issues RESET to PCA9548 (U1) for PSUs, MAC, Power Rails, 33731,
D3	PL2C	PCB_VERSION1	I		PCB Version [1:2]
J1	PL8D	PCB_VERSION2	I		PCB Version [1:2]
T2	PL20A	PCIE_INTR_L_R	I	Low	MAC issues Interrupt to CPLD1 via PCIe interface.
N5	PL20B	PCIE_PERST_L	O	Low	CPLD1 issues RESET to MAC via PCIe interface.
U1	PL19D	PCIE_WAKE_L_R	I	Low	MAC issue WAKE to CPLD1 via PCIe
K3	PL10B	POWER_RST	I	Low	Power Supervisor (POWER1014A) issues RESET to CPLD1
T8	PB13A/PCLKT2_0	PS1_12V_PG	I		PSU1, 12V Power Good.
R8	PB12D	PS1_AC_ALERT	I		PSU1 AC Alert
T9	PB13B/PCLKC2_0	PS1_PDB_ALERT	I		PSU1 PS_ON (Reserved)
U7	PB12C	PS1_PRESENT	I		PSU1 Present
V8	PB15A	PS2_12V_PG	I		PSU2, 12V Power Good.
P9	PB13D	PS2_AC_ALERT	I		PSU2 AC Alert
U9	PB15B	PS2_PDB_ALERT	I		PSU2 PS_ON (Reserved)
R9	PB13C	PS2_PRESENT	I		PSU2 Present
T6	PB9A/MCLK/CCLK	PSU1_B	O	Low	Blue PWM LED for PSU1 Status
R7	PB9D	PSU1_G	O	Low	Green PWM LED for PSU1 Status
N8	PB9C	PSU1_R	O	Low	Red PWM LED for PSU1 Status
U6	PB9B/SO/SPISO	PSU2_B	O	Low	Blue PWM LED for PSU2 Status
T5	PB7A	PSU2_G	O	Low	Green PWM LED for PSU2 Status
T4	PB6D	PSU2_R	O	Low	Red PWM LED for PSU2 Status
B7	PT14B	QSPI_RST	O	Low	Reset for SPI Flash (U5) of PCIe Gen 3
A5	PT12B	RESET_BUTTON_RST	I	Low	SW1 (RESET button) issues RESET to CPLD1
H6	PL8C	RESET_MAC	I	Low	CPU Board issues REST_MAC to CPLD1 (Reserved)
C5	PT12C	RESET_SYS_CPLD	I	Low	CPU Board issues RESET_SYS_CPLD to reset CPLD and all devices.
G14	PR3D	SW1_SELECT	O		SW1_SELECT deiven the selection pin of bus switch to switch CPLD's JTAG interface and FPGA's SPI Mode. 1: Slect SPI mode of FPGA. 0: CPLD interface of JTAG mode.
G4	PL6A/PCLKT5_0	SYS_CPLD_INT_CPU	O	Low	CPLD1 issues Interrup to CPU
C15	PT26B	TRIM_SW_OE	O	Low	set Trimmer function Enable
N9	PB15C	USB_PWRFLT_N	I	Low	USB Power Fault : USB OCP issues Fault to CPLD and USB HUB
V9	PB18A	USB_PWRON_N	O	Low	to Power Enable USB OCP
N10	PB15D	USB_RESET_N	O	Low	CPLD1 issue RESET to USB HUB.
T10	PB18C	USB1_PWRFAULT	O	Low	CPLD1 issues this signal to CPU Board to show USB Power Fault.
U10	PB18B	USB1_VBUS	I	Low	CPU issues it to CPLD1 to Enable/Disable USB 1: Enable USB. 0: Disable USB.
H18	PR10A/PCLKT1_0	USB2112_BRDG_RST	O	Low	CPLD1 issues RESET to USB Bridge U67 (CP2112)

Table 1-18 CPLD1 Pin-out Table

1.8.2. CPLD2 pin-out list

Pin Number	Pin Name	Net Name	I/O	Active	Description
H5	PL9C/PL13C/PL15C	CPLD_RST	O	Low	CPLD1 to CPLD2/CPLD3 Reset
K14	PR10A/PR14A/PR17A	CPLD12_LEDC	I		Clock of LED stream from CPLD1
K16	PR9B/PR13B/PR16B DQS1N	CPLD12_LEDD	I		Data of LED stream from CPLD1
K15	PR10B/PR14B/PR17B	CPLD12_LEDS	I		LED stream from CPLD1
D16	PR2A/PR3A/PR3A || R_GPLLT_IN**	CPLD2_25MHZ	I		25MHZ Clock Input
C13	PT24D/PT28D/PT36D || DONE	CPLD2_DONE			
A13	PT24C/PT28C/PT36C || INITN	CPLD2_INITN			
K2	PL10B/PL14B/PL17B	CPLD2_INT	O	Low	CPLD2 issues Interrupt to CPLD1
C10	PT20C/PT23C/PT27C || JTAGENB	CPLD2_JTAGENB			
B10	PT20D/PT23D/PT27D || PROGRAMN	CPLD2_PROGRAMN			
J2	PL9A/PL13A/PL15A	I2C_0_SCL_CPLD2	I		I2C Clock from CPU Board via PCA9548
K1	PL9B/PL13B/PL15B	I2C_0_SDA_CPLD2_R	I/O		I2C Data from/to CPU Board via PCA9548
A7	PT16C/PT15C/PT17C || TCK	JTAG_CPLD2_TCK			
A6	PT12D/PT13D/PT14D || TDI	JTAG_CPLD2_TDI			
C6	PT12C/PT13C/PT14C || TDO	JTAG_CPLD2_TDO_R			
B8	PT16D/PT15D/PT17D || TMS	JTAG_CPLD2_TMS			
T8	PB12B/PB15B/PB18B	P1_INT	I	Low	Interrupt from Port 1
C4	PT9A*/PT9A*/PT9A*	P1_LANE0_R_LED_B	O	Low	Blue LED for Port 1
B5	PT9B*/PT9B*/PT9B*	P1_LANE0_R_LED_G	O	Low	Green LED for Port 1
A5	PT11A*/PT11A*/PT11A*	P1_LANE0_R_LED_R	O	Low	Red LED for Port 1
R8	PB11B/PB13B/PB16B || PCLKC2_0	P1_MODPRSNT_N	I	Low	Module of Port 1 is presented
P8	PB12A/PB15A/PB18A	P1_RESET_N	O	Low	CPLD2 issues RESET to Port 1
P16	PR13D/PR18D/PR23D	P10_INT	I	Low	Interrupt from Port 10
J11	PR10C/PR14C/PR17C	P10_LANE0_R_LED_B	O	Low	Blue LED for Port 10
K11	PR12C/PR16C/PR21C	P10_LANE0_R_LED_G	O	Low	Green LED for Port 10
N15	PR13C/PR18C/PR23C	P10_LANE0_R_LED_R	O	Low	Red LED for Port 10
F4	PL3C/PL6C/PL6C	P10_MODPRSNT_N	I	Low	Module of Port 10 is presented
A15	PT24B*/PT28B*/PT36B*	P10_RESET_N	O	Low	CPLD2 issues RESET to Port 10
C12	PT23A*/PT27A*/PT35A*	P11_INT	I	Low	Interrupt from Port 11
L12	PR10D/PR14D/PR17D	P11_LANE0_R_LED_B	O	Low	Blue LED for Port 11
L13	PR12D/PR16D/PR21D	P11_LANE0_R_LED_G	O	Low	Green LED for Port 11
D11	PT21D/PT24D/PT32B*	P11_LANE0_R_LED_R	O	Low	Red LED for Port 11

P15	PR14C/PR20C/PR25C	P11_MODPRSNT_N	I	Low	Module of Port 11 is presented
R16	PR14D/PR20D/PR25D	P11_RESET_N	O	Low	CPLD2 issues RESET to Port 11
L10	PB18D/PB21D/PB26D	P12_INT	I	Low	Interrupt from Port 12
F9	PT19C/PT22A*/PT26A*	P12_LANE0_R_LED_B	O	Low	Blue LED for Port 12
E11	PT19D/PT22B*/PT26B*	P12_LANE0_R_LED_G	O	Low	Green LED for Port 12
E10	PT20B*/PT23B*/PT27B*	P12_LANE0_R_LED_R	O	Low	Red LED for Port 12
R10	PB19B/PB23B/PB29B	P12_MODPRSNT_N	I	Low	Module of Port 12 is presented
T11	PB21A/PB24A/PB31A	P12_RESET_N	O	Low	CPLD2 issues RESET to Port 12
N9	PB16D/PB18B/PB21B	P13_INT	I	Low	Interrupt from Port 13
E7	PT12B*/PT13B*/PT14B*	P13_LANE0_R_LED_B	O	Low	Blue LED for Port 13
C7	PT13B*/PT14B*/PT15B*	P13_LANE0_R_LED_G	O	Low	Green LED for Port 13
B7	PT13A*/PT14A*/PT15A*	P13_LANE0_R_LED_R	O	Low	Red LED for Port 13
M9	PB18C/PB21C/PB26C	P13_MODPRSNT_N	I	Low	Module of Port 13 is presented
M8	PB16C/PB18A/PB21A	P13_RESET_N	O	Low	CPLD2 issues RESET to Port 13
N11	PB21D/PB24D/PB31D	P14_INT	I	Low	Interrupt from Port 14
B13	PT22C/PT26A*/PT34A*	P14_LANE0_R_LED_B	O	Low	Blue LED for Port 14
F10	PT21C/PT24C/PT32A*	P14_LANE0_R_LED_G	O	Low	Green LED for Port 14
B12	PT23B*/PT27B*/PT35B*	P14_LANE0_R_LED_R	O	Low	Red LED for Port 14
P11	PB21B/PB24B/PB31B	P14_MODPRSNT_N	I	Low	Module of Port 14 is presented
M10	PB21C/PB24C/PB31C	P14_RESET_N	O	Low	CPLD2 issues RESET to Port 14
R9	PB18A/PB21A/PB26A	P15_INT	I	Low	Interrupt from Port 15
B11	PT22A*/PT25A*/PT33A*	P15_LANE0_R_LED_B	O	Low	Blue LED for Port 15
A12	PT22B*/PT25B*/PT33B*	P15_LANE0_R_LED_G	O	Low	Green LED for Port 15
A14	PT22D/PT26B*/PT34B*	P15_LANE0_R_LED_R	O	Low	Red LED for Port 15
T14	PB22D/PB26B/PB34B	P15_MODPRSNT_N	I	Low	Module of Port 15 is presented
R13	PB22C/PB26A/PB34A	P15_RESET_N	O	Low	CPLD2 issues RESET to Port 15
T12	PB22B/PB27B/PB35B	P16_INT	I	Low	Interrupt from Port 16
A11	PT21A*/PT24A*/PT28A*	P16_LANE0_R_LED_B	O	Low	Blue LED for Port 16
D10	PT20A*/PT23A*/PT27A*	P16_LANE0_R_LED_G	O	Low	Green LED for Port 16
C11	PT21B*/PT24B*/PT28B*	P16_LANE0_R_LED_R	O	Low	Red LED for Port 16

T10	PB18B/PB21B/PB26B	P16_MODPRSNT_N	I	Low	Module of Port 16 is presented
R11	PB22A/PB27A/PB35A	P16_RESET_N	O	Low	CPLD2 issues RESET to Port 16
P12	PB24A/PB29A/PB37A	P2_INT	I	Low	Interrupt from Port 2
C15	PR1C/PR2C/PR2C	P2_LANE0_R_LED_B	O	Low	Blue LED for Port 2
B16	PR1D/PR2D/PR2D	P2_LANE0_R_LED_G	O	Low	Green LED for Port 2
D15	PR2D/PR4D/PR4D	P2_LANE0_R_LED_R	O	Low	Red LED for Port 2
N8	PB12C/PB15C/PB18C	P2_MODPRSNT_N	I	Low	Module of Port 2 is presented
L9	PB12D/PB15D/PB18D	P2_RESET_N	O	Low	CPLD2 issues RESET to Port 2
R14	PB25D/PB30D/PB38D	P3_INT	I	Low	Interrupt from Port 3
F13	PR3C/PR5C/PR6C	P3_LANE0_R_LED_B	O	Low	Blue LED for Port 3
G12	PR3D/PR5D/PR6D	P3_LANE0_R_LED_G	O	Low	Green LED for Port 3
G13	PR4D/PR6D/PR7D	P3_LANE0_R_LED_R	O	Low	Red LED for Port 3
P13	PB25B/PB30B/PB38B || SI/SISPI	P3_MODPRSNT_N	I	Low	Module of Port 3 is presented
T15	PB25C/PB30C/PB38C	P3_RESET_N	O	Low	CPLD2 issues RESET to Port 3
M2	PL14A/PL20A/PL25A	P4_INT	I	Low	Interrupt from Port 4
F8	PT18A*/PT20A*/PT22A*	P4_LANE0_R_LED_B	O	Low	Blue LED for Port 4
D9	PT18B*/PT20B*/PT22B*	P4_LANE0_R_LED_G	O	Low	Green LED for Port 4
C9	PT18D/PT20D/PT22D || SDA/PCLKC0_0	P4_LANE0_R_LED_R	O	Low	Red LED for Port 4
M3	PL13A/PL19A/PL24A	P4_MODPRSNT_N	I	Low	Module of Port 4 is presented
N1	PL13B/PL19B/PL24B	P4_RESET_N	O	Low	CPLD2 issues RESET to Port 4
C2	PL1D/PL2D/PL2D	P5_INT	I	Low	Interrupt from Port 5
B3	PT9C/PT9C/PT9C	P5_LANE0_R_LED_B	O	Low	Blue LED for Port 5
A4	PT10A*/PT10A*/PT10A*	P5_LANE0_R_LED_G	O	Low	Green LED for Port 5
C5	PT10B*/PT10B*/PT10B*	P5_LANE0_R_LED_R	O	Low	Red LED for Port 5
N3	PL14B/PL20B/PL25B	P5_MODPRSNT_N	I	Low	Module of Port 5 is presented
B1	PL1C/PL2C/PL2C	P5_RESET_N	O	Low	CPLD2 issues RESET to Port 5
G5	PL4C/PL7C/PL7C	P6_INT	I	Low	Interrupt from Port 6
G11	PR5C/PR8C/PR10C	P6_LANE0_R_LED_B	O	Low	Blue LED for Port 6
H12	PR5D/PR8D/PR10D	P6_LANE0_R_LED_G	O	Low	Green LED for Port 6
J12	PR6D/PR9D/PR11D	P6_LANE0_R_LED_R	O	Low	Red LED for Port 6
B14	PT24A*/PT28A*/PT36A*	P6_MODPRSNT_N	I	Low	Module of Port 6 is presented
G6	PL3D/PL6D/PL6D	P6_RESET_N	O	Low	CPLD2 issues RESET to Port 6
G3	PL5B/PL8B/PL9B	P7_INT	I	Low	Interrupt from Port 7

J16	PR7C/PR10C/PR15A	P7_LANE0_R_LED_B	O	Low	Blue LED for Port 7
J14	PR7D/PR10D/PR15B	P7_LANE0_R_LED_G	O	Low	Green LED for Port 7
J13	PR9D/PR13D/PR16D	P7_LANE0_R_LED_R	O	Low	Red LED for Port 7
J5	PL10C/PL14C/PL16C	P7_MODPRSNT_N	I	Low	Module of Port 7 is presented
G2	PL5A/PL8A/PL9A	P7_RESET_N	O	Low	CPLD2 issues RESET to Port 7
J4	PL9D/PL13D/PL15D	P8_INT	I	Low	Interrupt from Port 8
A9	PT18C/PT20C/PT22C || SCL/PCLKT0_0	P8_LANE0_R_LED_B	O	Low	Blue LED for Port 8
B9	PT19A*/PT21A*/PT25A*	P8_LANE0_R_LED_G	O	Low	Green LED for Port 8
A10	PT19B*/PT21B*/PT25B*	P8_LANE0_R_LED_R	O	Low	Red LED for Port 8
G4	PL4D/PL7D/PL7D	P8_MODPRSNT_N	I	Low	Module of Port 8 is presented
H6	PL5D/PL8D/PL9D	P8_RESET_N	O	Low	CPLD2 issues RESET to Port 8
K3	PL10A/PL14A/PL17A	P9_INT	I	Low	Interrupt from Port 9
B6	PT11B*/PT11B*/PT11B*	P9_LANE0_R_LED_B	O	Low	Blue LED for Port 9
A3	PT11C/PT12A*/PT12A*	P9_LANE0_R_LED_G	O	Low	Green LED for Port 9
D6	PT12A*/PT13A*/PT14A*	P9_LANE0_R_LED_R	O	Low	Red LED for Port 9
F5	PL5C/PL8C/PL9C	P9_MODPRSNT_N	I	Low	Module of Port 9 is presented
K6	PL10D/PL14D/PL16D	P9_RESET_N	O	Low	CPLD2 issues RESET to Port 9

Table 1-19 CPLD2 Pin-out Table

1.8.3. CPLD3 pin-out list

Pin Number	Pin Name	Net Name	I/O	Active	Description
J5	PL10C/PL14C/PL16C	CPLD_RST	O	Low	CPLD1 to CPLD2/CPLD3 Reset
H2	PL6B/PL9B/PL10B	CPLD13_LEDC	I		Clock of LED stream from CPLD1
G1	PL6A/PL9A/PL10A	CPLD13_LEDD	I		Data of LED stream from CPLD1
H4	PL6C/PL9C/PL10C	CPLD13_LEDS	I		LED stream from CPLD1
E3	PL2B/PL4B/PL4B || L_GPLLC_IN	CPLD3_25MHZ	O	Low	25MHZ Clock Input
C13	PT24D/PT28D/PT36D || DONE	CPLD3_DONE			
A13	PT24C/PT28C/PT36C || INITN	CPLD3_INITN			
K6	PL10D/PL14D/PL16D	CPLD3_INT	O	Low	CPLD3 issues Interrupt to CPLD1
C10	PT20C/PT23C/PT27C || JTAGENB	CPLD3_JAGENB			
B10	PT20D/PT23D/PT27D || PROGRAMN	CPLD3_PPROGRAMN			
K3	PL10A/PL14A/PL17A	I2C_0_SCL_CPLD3	I		I2C Clock from CPU Board via PCA9548
K2	PL10B/PL14B/PL17B	I2C_0_SDA_CPLD3	I/O		I2C Data from/to CPU Board via PCA9548
A7	PT16C/PT15C/PT17C || TCK	JTAG_CPLD3_TCK			
A6	PT12D/PT13D/PT14D || TDI	JTAG_CPLD3_TDI			
C6	PT12C/PT13C/PT14C || TDO	JTAG_CPLD3_TDO_R			
B8	PT16D/PT15D/PT17D || TMS	JTAG_CPLD3_TMS			
K16	PR9B/PR13B/PR16B DQS1N	P17_INT	I	Low	Interrupt from Port 17
R5	PB5A/PB4A/PB6A || CSSPIN	P17_LANE0_R_LED_B	O	Low	Blue LED for Port 17
P5	PB5B/PB4B/PB6B	P17_LANE0_R_LED_G	O	Low	Green LED for Port 17
T3	PB6C/PB6A/PB7A	P17_LANE0_R_LED_R	O	Low	Red LED for Port 17
L16	PR11A/PR15A/PR18A	P17_MODPRSNT_N	I	Low	Module of Port 17 is presented
J2	PL9A/PL13A/PL15A	P17_RESET_N	O	Low	CPLD3 issues RESET to Port 17
H16	PR7B/PR10B/PR12B || PCLKC1_0	P18_INT	I	Low	Interrupt from Port 18
P10	PB19A/PB23A/PB29A	P18_LANE0_R_LED_B	O	Low	Blue LED for Port 18
R10	PB19B/PB23B/PB29B	P18_LANE0_R_LED_G	O	Low	Green LED for Port 18
T11	PB21A/PB24A/PB31A	P18_LANE0_R_LED_R	O	Low	Red LED for Port 18
H15	PR6B/PR9B/PR11B DQS0N	P18_MODPRSNT_N	I	Low	Module of Port 18 is presented
K15	PR10B/PR14B/PR17B	P18_RESET_N	O	Low	CPLD3 issues RESET to Port 18
B16	PR1D/PR2D/PR2D	P19_INT	I	Low	Interrupt from Port 19
P11	PB21B/PB24B/PB31B	P19_LANE0_R_LED_B	O	Low	Blue LED for Port 19
M10	PB21C/PB24C/PB31C	P19_LANE0_R_LED_G	O	Low	Green LED for Port 19
N11	PB21D/PB24D/PB31D	P19_LANE0_R_LED_R	O	Low	Red LED for Port 19
J15	PR9A/PR13A/PR16A DQS1	P19_MODPRSNT_N	I	Low	Module of Port 19 is presented
K14	PR10A/PR14A/PR17A	P19_RESET_N	O	Low	CPLD3 issues RESET to Port 19
F12	PR4C/PR6C/PR7C	P20_INT	I	Low	Interrupt from Port 20
H12	PR5D/PR8D/PR10D	P20_LANE0_R_LED_B	O	Low	Blue LED for Port 20
H13	PR6C/PR9C/PR11C	P20_LANE0_R_LED_G	O	Low	Green LED for Port 20
J16	PR7C/PR10C/PR15A	P20_LANE0_R_LED_R	O	Low	Red LED for Port 20
C16	PR2C/PR4C/PR4C	P20_MODPRSNT_N	I	Low	Module of Port 20 is presented
D15	PR2D/PR4D/PR4D	P20_RESET_N	O	Low	CPLD3 issues RESET to Port 20
G12	PR3D/PR5D/PR6D	P21_INT	I	Low	Interrupt from Port 21
T5	PB6A/PB7A/PB9A	P21_LANE0_R_LED_B	O	Low	Blue LED for Port 21
R6	PB6B/PB7B/PB9B	P21_LANE0_R_LED_G	O	Low	Green LED for Port 21
N6	PB8C/PB9C/PB10A	P21_LANE0_R_LED_R	O	Low	Red LED for Port 21

G13	PR4D/PR6D/PR7D	P21_MODPRSNT_N	I	Low	Module of Port 21 is presented
F13	PR3C/PR5C/PR6C	P21_RESET_N	O	Low	CPLD3 issues RESET to Port 21
H14	PR7A/PR10A/PR12A || PCLKT1_0	P22_INT	I	Low	Interrupt from Port 22
N7	PB9D/PB10D/PB13D	P22_LANE0_R_LED_B	O	Low	Blue LED for Port 22
M6	PB11C/PB12A/PB15A	P22_LANE0_R_LED_G	O	Low	Green LED for Port 22
L8	PB11D/PB12B/PB15B	P22_LANE0_R_LED_R	O	Low	Red LED for Port 22
H5	PL9C/PL13C/PL15C	P22_MODPRSNT_N	I	Low	Module of Port 22 is presented
J4	PL9D/PL13D/PL15D	P22_RESET_N	O	Low	CPLD3 issues RESET to Port 22
D16	PR2A/PR3A/PR3A || R_GPLLT_IN**	P23_INT	I	Low	Interrupt from Port 23
R13	PB22C/PB26A/PB34A	P23_LANE0_R_LED_B	O	Low	Blue LED for Port 23
T14	PB22D/PB26B/PB34B	P23_LANE0_R_LED_G	O	Low	Green LED for Port 23
T12	PB22B/PB27B/PB35B	P23_LANE0_R_LED_R	O	Low	Red LED for Port 23
D14	PR1A/PR2A/PR2A || R_GPLLT_FB**	P23_MODPRSNT_N	I	Low	Module of Port 23 is presented
E15	PR1B/PR2B/PR2B || R_GPLLC_FB**	P23_RESET_N	O	Low	CPLD3 issues RESET to Port 23
F15	PR3B/PR5B/PR5B	P24_INT	I	Low	Interrupt from Port 24
J13	PR9D/PR13D/PR16D	P24_LANE0_R_LED_B	O	Low	Blue LED for Port 24
J11	PR10C/PR14C/PR17C	P24_LANE0_R_LED_G	O	Low	Green LED for Port 24
K11	PR12C/PR16C/PR21C	P24_LANE0_R_LED_R	O	Low	Red LED for Port 24
E14	PR2B/PR3B/PR3B || R_GPLLC_IN**	P24_MODPRSNT_N	I	Low	Module of Port 24 is presented
E16	PR3A/PR5A/PR5A	P24_RESET_N	O	Low	CPLD3 issues RESET to Port 24
G15	PR5A/PR8A/PR9A	P25_INT	I	Low	Interrupt from Port 25
L7	PB8D/PB9D/PB10B	P25_LANE0_R_LED_B	O	Low	Blue LED for Port 25
P6	PB8A/PB9A/PB12A || MCLK/CCLK	P25_LANE0_R_LED_G	O	Low	Green LED for Port 25
T6	PB8B/PB9B/PB12B || SO/SPISO	P25_LANE0_R_LED_R	O	Low	Red LED for Port 25
F14	PR4A/PR6A/PR7A	P25_MODPRSNT_N	I	Low	Module of Port 25 is presented
F16	PR4B/PR6B/PR7B	P25_RESET_N	O	Low	CPLD3 issues RESET to Port 25
J3	PL7D/PL10D/PL12B || PCLKC4_0	P26_INT	I	Low	Interrupt from Port 26
R11	PB22A/PB27A/PB35A	P26_LANE0_R_LED_B	O	Low	Blue LED for Port 26
P12	PB24A/PB29A/PB37A	P26_LANE0_R_LED_G	O	Low	Green LED for Port 26
T13	PB24B/PB29B/PB37B	P26_LANE0_R_LED_R	O	Low	Red LED for Port 26
G14	PR5B/PR8B/PR9B	P26_MODPRSNT_N	I	Low	Module of Port 26 is presented
G16	PR6A/PR9A/PR11A DQS0	P26_RESET_N	O	Low	CPLD3 issues RESET to Port 26
H1	PL7B/PL10B/PL11B	P27_INT	I	Low	Interrupt from Port 27
T7	PB11A/PB13A/PB16A || PCLKT2_0	P27_LANE0_R_LED_B	O	Low	Blue LED for Port 27
R8	PB11B/PB13B/PB16B || PCLKC2_0	P27_LANE0_R_LED_G	O	Low	Green LED for Port 27
P8	PB12A/PB15A/PB18A	P27_LANE0_R_LED_R	O	Low	Red LED for Port 27
L15	PR12A/PR16A/PR21A	P27_MODPRSNT_N	I	Low	Module of Port 27 is presented
H3	PL7A/PL10A/PL11A	P27_RESET_N	O	Low	CPLD3 issues RESET to Port 27
T9	PB16A/PB20A/PB23A || PCLKT2_1	P28_INT	I	Low	Interrupt from Port 28
P16	PR13D/PR18D/PR23D	P28_LANE0_R_LED_B	O	Low	Blue LED for Port 28
P15	PR14C/PR20C/PR25C	P28_LANE0_R_LED_G	O	Low	Green LED for Port 28
R16	PR14D/PR20D/PR25D	P28_LANE0_R_LED_R	O	Low	Red LED for Port 28
M8	PB16C/PB18A/PB21A	P28_MODPRSNT_N	I	Low	Module of Port 28 is presented
N9	PB16D/PB18B/PB21B	P28_RESET_N	O	Low	CPLD3 issues RESET to Port 28
T10	PB18B/PB21B/PB26B	P29_INT	I	Low	Interrupt from Port 29
R7	PB9A/PB10A/PB13A	P29_LANE0_R_LED_B	O	Low	Blue LED for Port 29
P7	PB9B/PB10B/PB13B	P29_LANE0_R_LED_G	O	Low	Green LED for Port 29
M7	PB9C/PB10C/PB13C	P29_LANE0_R_LED_R	O	Low	Red LED for Port 29

P9	PB16B/PB20B/PB23B || PCLKC2_1	P29_MODPRSNT_N	I	Low	Module of Port 29 is presented
R9	PB18A/PB21A/PB26A	P29_RESET_N	O	Low	CPLD3 issues RESET to Port 29
N10	PB19C/PB23C/PB28A	P30_INT	I	Low	Interrupt from Port 30
K4	PL11C/PL16C/PL19C	P30_LANE0_R_LED_B	O	Low	Blue LED for Port 30
L5	PL11D/PL16D/PL19D	P30_LANE0_R_LED_G	O	Low	Green LED for Port 30
T15	PB25C/PB30C/PB38C	P30_LANE0_R_LED_R	O	Low	Red LED for Port 30
M9	PB18C/PB21C/PB26C	P30_MODPRSNT_N	I	Low	Module of Port 30 is presented
L10	PB18D/PB21D/PB26D	P30_RESET_N	O	Low	CPLD3 issues RESET to Port 30
T4	PB3B/PB3B/PB4B	P31_INT	I	Low	Interrupt from Port 31
R14	PB25D/PB30D/PB38D	P31_LANE0_R_LED_B	O	Low	Blue LED for Port 31
T8	PB12B/PB15B/PB18B	P31_LANE0_R_LED_G	O	Low	Green LED for Port31
N8	PB12C/PB15C/PB18C	P31_LANE0_R_LED_R	O	Low	Red LED for Port 31
M11	PB19D/PB23D/PB28B	P31_MODPRSNT_N	I	Low	Module of Port 31 is presented
P4	PB3A/PB3A/PB4A	P31_RESET_N	O	Low	CPLD3 issues RESET to Port 32
K13	PR11C/PR15C/PR19C	P32_INT	I	Low	Interrupt from Port 32
B5	PT9B*/PT9B*/PT9B*	P32_LANE0_R_LED_B	O	Low	Blue LED for Port 32
C4	PT9A*/PT9A*/PT9A*	P32_LANE0_R_LED_G	O	Low	Green LED for Port 32
A4	PT10A*/PT10A*/PT10A*	P32_LANE0_R_LED_R	O	Low	Red LED for Port 32
L14	PR11B/PR15B/PR18B	P32_MODPRSNT_N	I	Low	Module of Port 32 is presented
K12	PR11D/PR15D/PR19D	P32_RESET_N	O	Low	CPLD3 issues RESET to Port 32

Table 1-20 CPLD3 Pin-out Table

1.8.4. Fan CPLD pin-out list

Pin	Net name	IN/ OUT
T8	VERSION_ID_3	IN
T7	VERSION_ID_2	IN
T6	VERSION_ID_1	IN
A11	I2C_master_enable	IN
A5	FAN_SDA_2_R	IN/ OUT
M1	FAN_SDA_1_R	IN/ OUT
A4	FAN_SCL_2_R	OUT
N1	FAN_SCL_1	IN
A8	FAN_PWM_6	OUT
B13	FAN_PWM_5	OUT
B16	FAN_PWM_4	OUT
H13	FAN_PWM_3	OUT
M14	FAN_PWM_2	OUT
M13	FAN_PWM_1	OUT
B5	FAN_LED_R_6	OUT
N11	FAN_LED_R_5	OUT
P10	FAN_LED_R_4	OUT
M16	FAN_LED_R_3	OUT
A13	FAN_LED_R_2	OUT
A10	FAN_LED_R_1	OUT
C7	FAN_LED_G_6	OUT
L12	FAN_LED_G_5	OUT
M11	FAN_LED_G_4	OUT
L16	FAN_LED_G_3	OUT
C13	FAN_LED_G_2	OUT
C10	FAN_LED_G_1	OUT
A6	FAN_INTERRUPT	OUT
A2	FAN_IDLE	IN
B7	FAN_DIRECTION_6	IN
D11	FAN_DIRECTION_5	IN
C14	FAN_DIRECTION_4	IN
H14	FAN_DIRECTION_3	IN
K13	FAN_DIRECTION_2	IN
N13	FAN_DIRECTION_1	IN
B9	FAN6R_SENSOR	IN

C8	FAN6_SENSOR	IN
C12	FAN5R_SENSOR	IN
E12	FAN5_SENSOR	IN
C15	FAN4R_SENSOR	IN
A15	FAN4_SENSOR	IN
K14	FAN3R_SENSOR	IN
J13	FAN3_SENSOR	IN
P14	FAN2R_SENSOR	IN
L13	FAN2_SENSOR	IN
P12	FAN1R_SENSOR	IN
R13	FAN1_SENSOR	IN
E6	EN_FAN6	OUT
E11	EN_FAN5	OUT
E10	EN_FAN4	OUT
D9	EN_FAN3	OUT
D8	EN_FAN2	OUT
D7	EN_FAN1	OUT
T5	BOARD_ID_2	IN
T4	BOARD_ID_1	IN

Table 1-21 Fan board CPLD Pin-out Table