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Compute Project



**OCP U.S. SUMMIT 2017**

Santa Clara, CA



# A Novel, Scalable, Energy Proportional Architecture for 48V to PoL Direct Conversion

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OPEN HARDWARE.

OPEN SOFTWARE.

OPEN FUTURE.



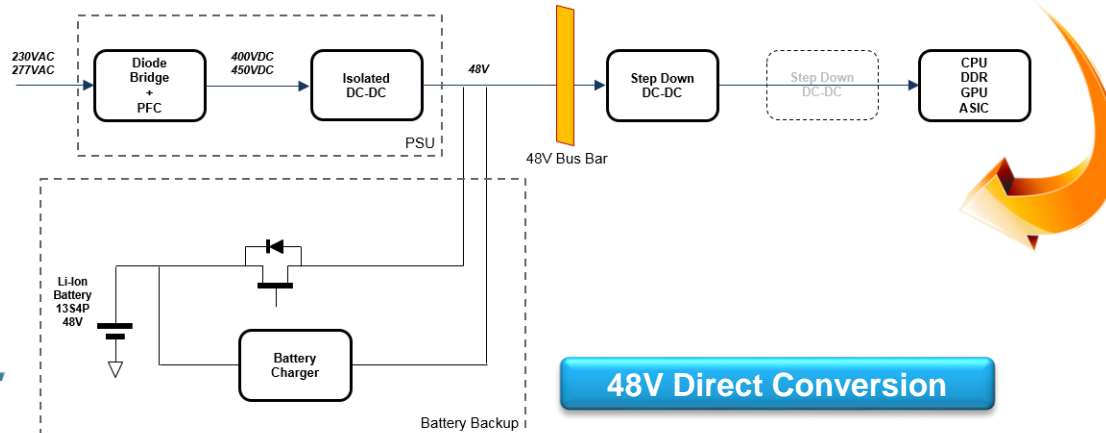
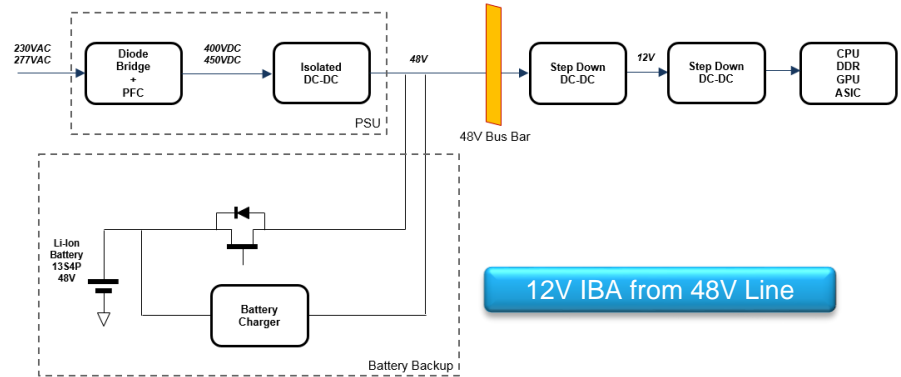
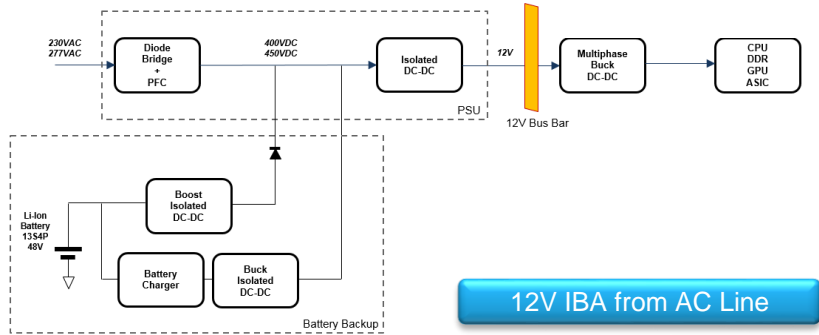
# Data Center Power Challenges

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- **Data Center Energy Consumption** *(US Department of Energy Study)*
  - US data centers consumed about 70 billion kilowatt-hours of electricity in 2014
  - Total US data center energy consumption to grow by 4 percent between now and 2020
  - Efficiency improvements played an enormous role in taming the growth rate of the data center industry's energy consumption.
  - If stayed at efficiency levels of 2010, data centers would have consumed close to 40 billion kWh more than they did in 2014
- **Higher Power Needed by Silicon Key Components**
  - CPU power demand going above 240W
  - GPU and Networking ASICs power demand above 350W
  - DDR power increase due to faster memory and higher number of DIMMs
- **More Efficient Data Center and Power Architectures are Needed**

# Power Distribution Overview

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## 48V Direct Conversion Advantages

48V distribution current is  $1/4^{\text{th}}$  compared to 12V with **distribution losses** reduced to  $1/16^{\text{th}}$

Better conversion **efficiency** (downstream and upstream)

High Power **Boost** converter not required

Simpler distributed BBS **maximizing** server density

Leverage of existing **Telecom** infrastructure



# Direct Conversion Challenges Addressed

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**Direct Conversion  
From 54V to  
CPU/DDR/ASIC**

**Intel VR13 Fully  
Compliant  
(No Waiver)**

**Fully Isolated  
Architecture**

**Scalable  
Architecture**

**High and Flat  
Efficiency Curve**

**Phase Shedding  
and Pulse Skipping**

**400V Input Ready**

15+ Years  
Multiphase  
DCDC

CPU VR  
Digital Core

Scalability  
IPs

PMBus  
AVS1.3

HV Digital  
Direct  
Conversion

High  
Efficiency  
DC/DC

BCD  
Technology

New Product  
Ideas

Product  
Concept

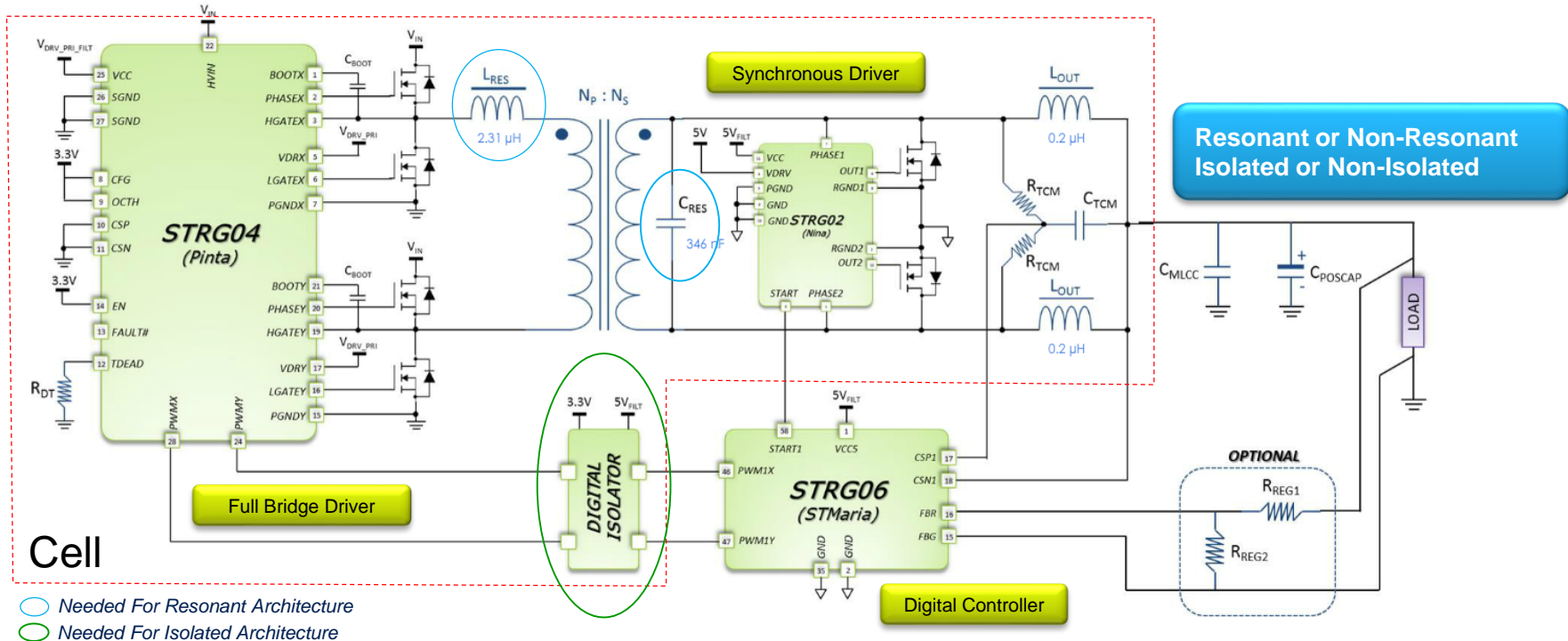
New IPs  
Development

New  
Architecture



# New Architecture: Resonant Current Doubler

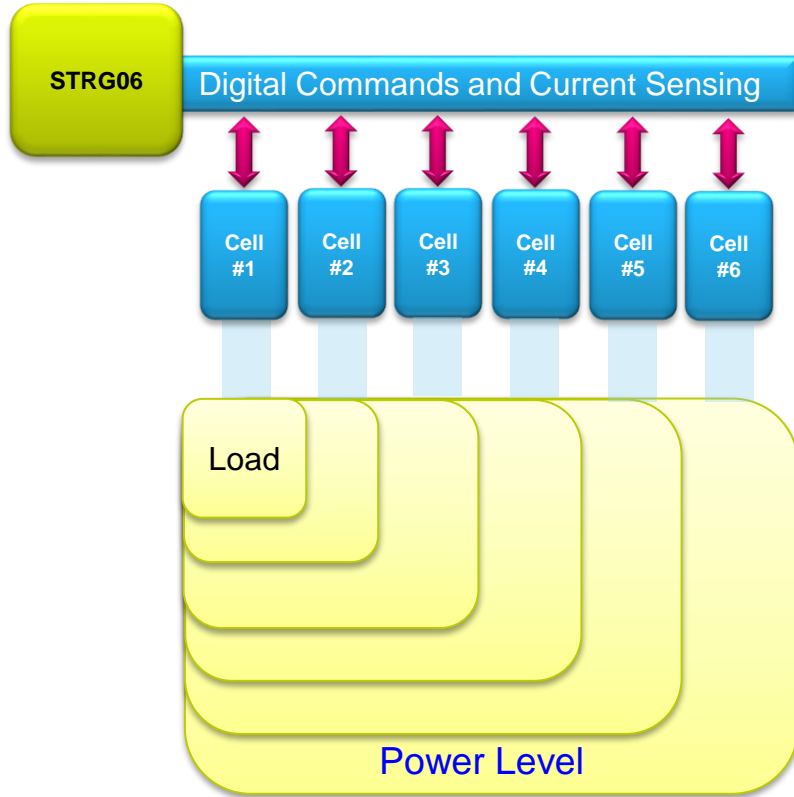
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**STRG06** Multiphase Resonant Constant On Time Digital Controller 6 interleaved Cells (automatically turned on/off by load request) with PMBUS

**STRG04** 100V Full Bridge Driver with programmable predictive control for zero voltage operations in constant phase shift control

**STRG02** Single wire controlled Synchronous Rectifier able to zero voltage and zero current operations



## More Power → More Cells

- Design Only One Cell to Design a Flexible System
- Support up to 6 Cells
- Automatic Interleaving Among Cells
- Automatic Cell Turn on/off Management
- Active Current Balancing Among Cells
- Pulse Skipping Mode When in Single Cell

100W



One Cell

600W

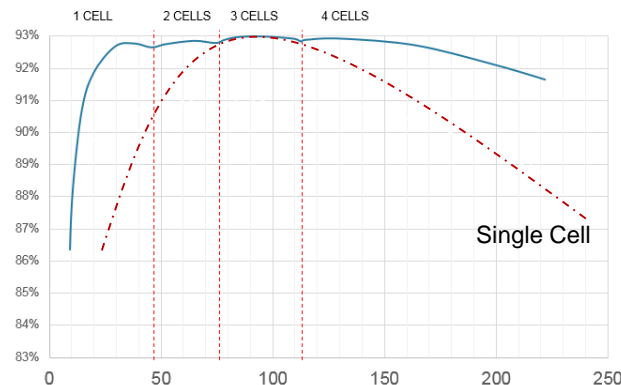
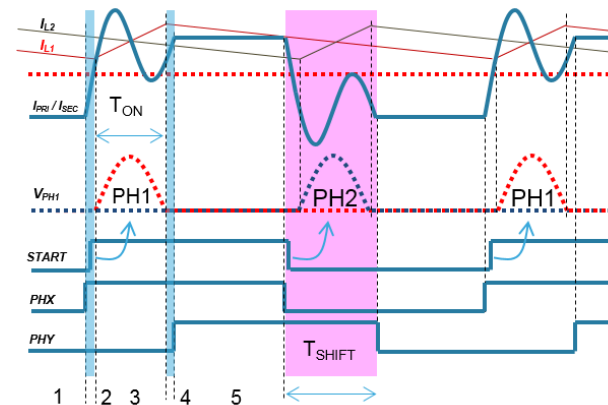


Multiple Cell

# Architecture Key Advantages

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- Fully Isolated, Resonant or Non-Resonant Direct Conversion
  - $54V \rightarrow V_{CORE}(1.xV), V_{DDR}(1.2V), V_{SOC}(0.8V), V_{IBC}(12V, 5V, 3.3V)$
- Maximum Efficiency Across Full Load Range
  - ZVS and ZCS under any working conditions
  - Energy Proportional Management → Dynamic Cell Management, Pulse Skipping
  - No Heat Sink Required
  - OpEx savings enhances system and datacenter performance/watt
- Scalable and Flexible
  - Converter Cells are paralleled and interleaved
  - System scalability according to the load power demand
  - Variable Frequency in CCM and DCM
  - Instantaneous turn-on of resonant converters when load increases
  - Resonant or Non-Resonant Mode of Operations
- Any Digital Load (CPU, GPU, DDR, ASICs)
  - High Bandwidth to sustain CPUs' load transient
  - Easy to design and to compensate like a Buck converter
  - Up and down reference transitions → Sink mode operations
  - Minimized noise content for closer proximity to Digital Loads
- High Power Density and Telemetry (PMBus™, AVS1.3)





- This Architecture Natively Supports Full Isolation
  - Controller at secondary side for direct interaction with SVI/PMBus signals from Load
  - Controller directly manages remote sense functions
  - Primary side is driven through digital isolator (when isolation is needed)
- Electrical Isolation provided by the transformer
  - No direct connection of the 48V, or -48V, input line to the load
- Safety Isolation
  - Required above 60VDC
  - 400V Input ready topology
- Optional Feature
  - If Isolation is not Required Digital Isolator can be Removed

# eColumbus Design Tool

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The specifications view

## eDesignSuite

### Converter Specifications

Input: 40 V - 60 V (54 V nom.)  
Output: 1 V (0.8 V - 1.2 V) - 84 W  
1 cell - 70 A  
No load fsw: 380 kHz  
Lout delta current 10.5 A  
Max. Ta: 50 °C

Change Specifications...

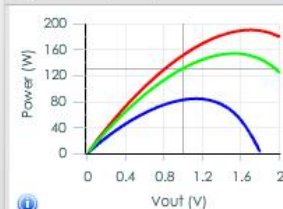
### Actuals

@Vin: 54 V Vout: 1 V Iout: 70 A

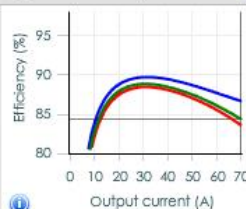
Tshift: 0.561  $\mu$ s  
Tstart: 128 ns  
Tdt: 68 ns  
fsw: 405.42 kHz

### Design Refinements

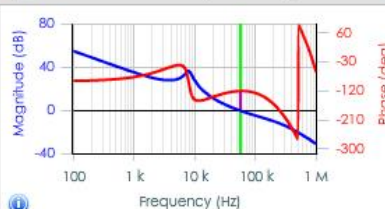
Cell Capability: 131.07 W



$\eta$  Cell Efficiency: 0.84 %



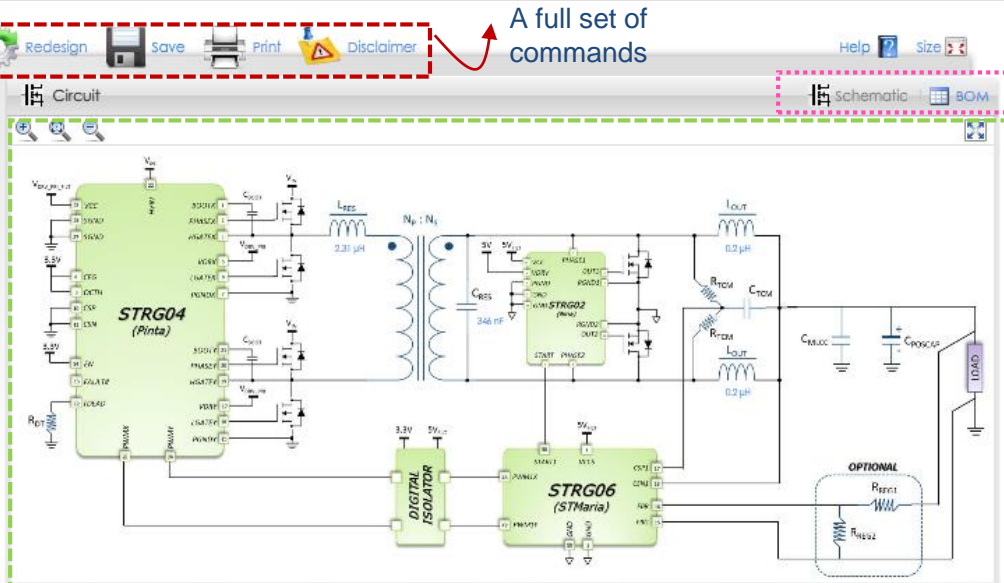
Bode: fc = 54.98 kHz - phase margin = 60 °



Cell Losses: 12.9 W - 15.6 %

Sec. Rectification	7.05 W - 54.45%
Ires	2.38 W - 18.37%
Lout	1.41 W - 10.86%
Transformer	811 mW - 6.27%
ICs biasing	500 mW - 3.86%
Full Bridge	485 mW - 3.75%
Cres	315 mW - 2.44%

The actual view



A full set of commands

A fully interactive BOM

A fully annotated and interactive schematic

A full set of analysis diagrams

# Developments Tools

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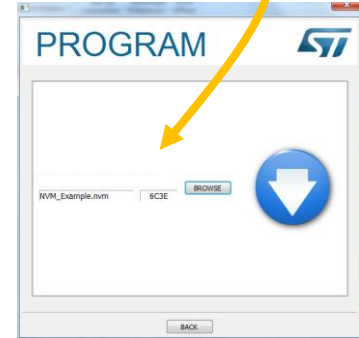
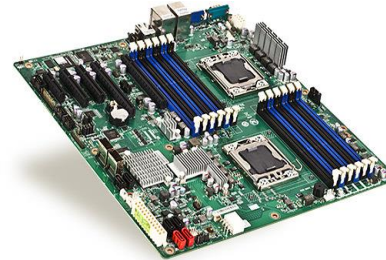
*A complete set of software tools, HW programmers and Technical Collaterals are available to support custom application designs*

- **NVM Flasher Tool (2<sup>nd</sup>)**

- Allows Programming STRG06 on board in a few simple steps
- Totally safe process since it is impossible altering the parameters by this tool

- **POWER MASTER Tool (1<sup>st</sup>)**

- Device & Application Configuration definition
  - Security: different rights for different operators
- NVM file (Non Volatile Memory) generation

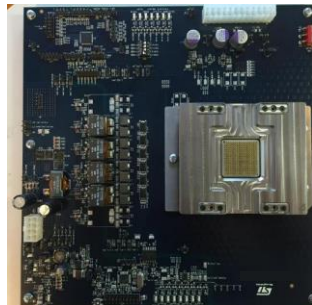


- **Technical documentation available (3<sup>rd</sup>)**

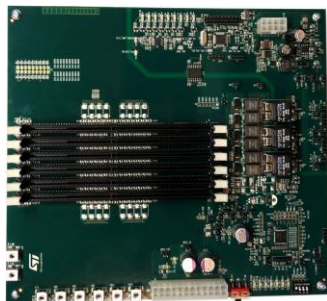
- Detailed command sequence to support writing the NVM file by PMBUS on board in production line

# Reference Designs

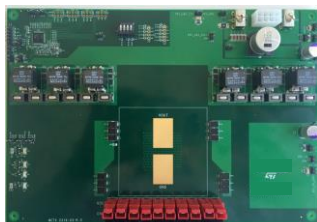
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54V → 1.8V Intel VR13



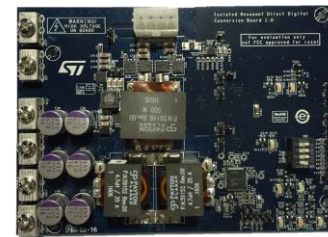
54V → 1.2V DDR



54V → 0.9V ASIC

Conversion Type	Application	Output Current and Power	Number of Cells
54V → 1.8V	Intel VR13 CPU	165W TDC 360W Peak	4
54V → 1.2V	VDDQ DDR3/4	120A - 150W	2
54V → 0.9V	ASIC Core	300A - 270W	6
54V → 12V	Point of Load	42A - 500W	1
54V → 1V	Point of Load	80A - 80W	1
54V → 3.3V	Point of Load	46A - 150W	1

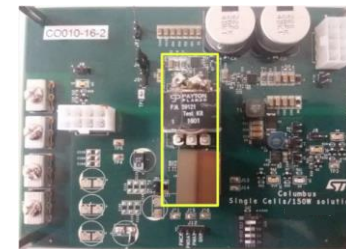
Same Scalable Topology for Different Point of Load  
Ideal for Power Modules Applications



54V → 12V POL



54V → 1V POL



54V → 3.3V POL 1/8<sup>th</sup> Brick

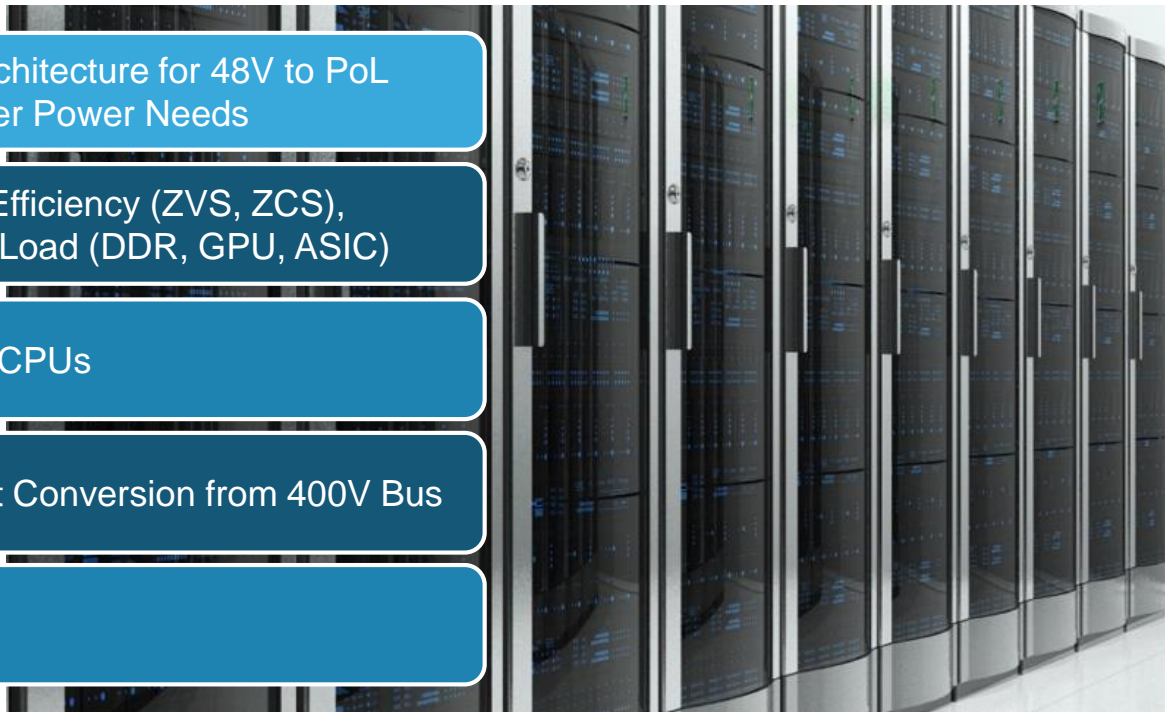
Innovative Resonant Current Doubler Architecture for 48V to PoL  
Direct Conversion Addressing Data Center Power Needs

Fully Isolated, Scalable, Maximized Flat Efficiency (ZVS, ZCS),  
Energy Proportional Able to Support Any Load (DDR, GPU, ASIC)

Fully Compliant to Intel and Other Brand CPUs

Flexible Architecture Extendable to Direct Conversion from 400V Bus

Available in Mass Production Since 2016







# 48V direct conversion to CPU, memory or ASIC

High efficiency (ZVS, ZCS). Fully isolated, scalable  
and energy proportional



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