Mono Lake M/B

PCB REV: E
PCBA REV: C3A
FAB: 5
SCH Rev: V3
LAST UPDATE: 2016/02/19

COVER PAGE

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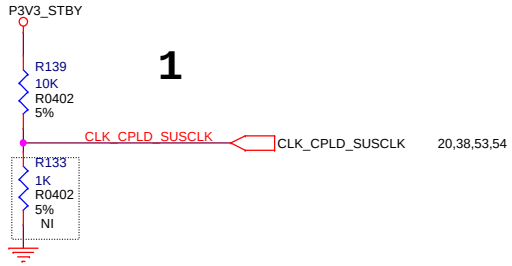
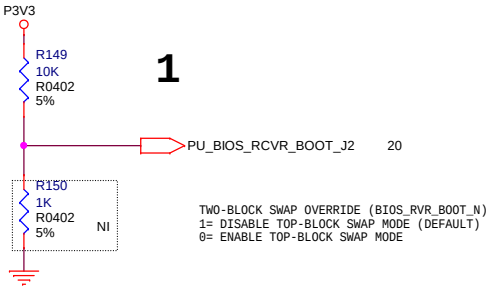
GPIO62



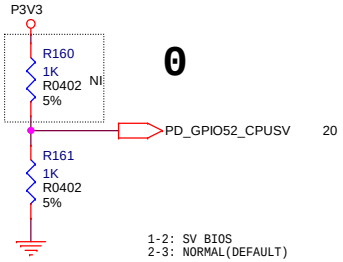
PLL ON-DIE VOLTAGE REGULATOR ENABLE.
ENABLED WHEN SAMPLED HIGH (DEFAULT).
DISABLED WHEN SAMPLED LOW.
WEAK INTERNAL PU (15K-40K).

TOP_BLOCK_SWAP



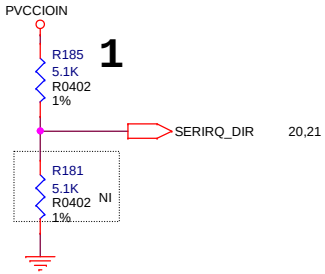
TWO-BLOCK SWAP OVERRIDE (BIOS_RVR_BOOT_N)
1= DISABLE TOP-BLOCK SWAP MODE (DEFAULT)
0= ENABLE TOP-BLOCK SWAP MODE

GP52_GSXSLOAD

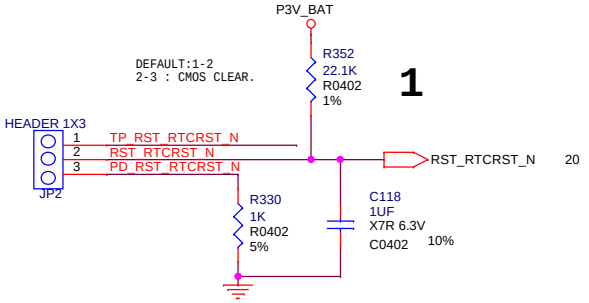


1-2: SV BIOS
2-3: NORMAL(DEFAULT)

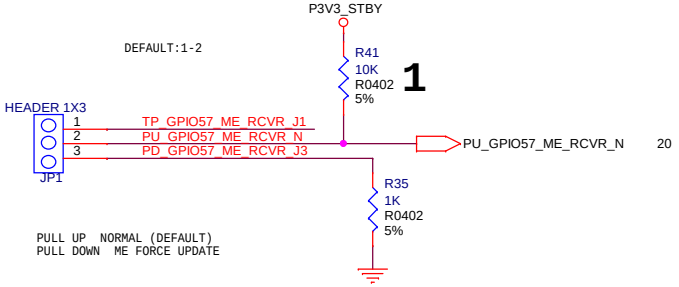
SERIRQ_DIR



CMOS CLEAR

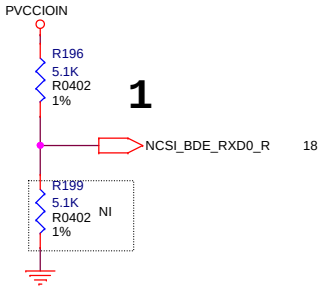


ME_RCVR

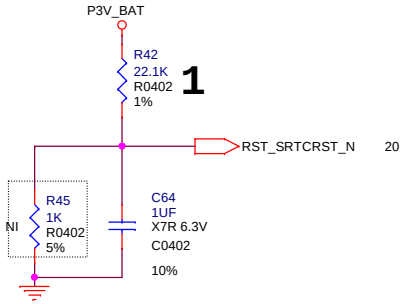


PULL UP NORMAL (DEFAULT)
PULL DOWN ME FORCE UPDATE

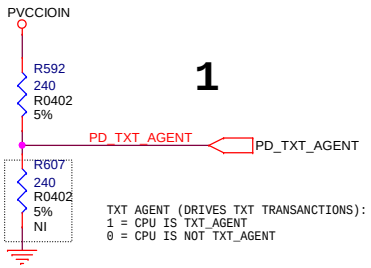
NCSI_RXD_0



CLEAR TPM REGISTERS

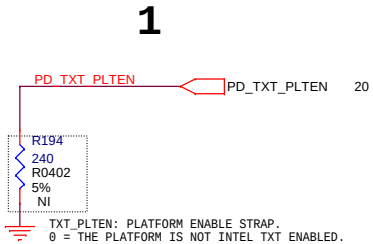


TXT_AGENT



TXT AGENT (DRIVES TXT TRANSANCTIONS):
1 = CPU IS TXT_AGENT
0 = CPU IS NOT TXT_AGENT

TXT_PLTEN



TXT_PLTEN: PLATFORM ENABLE STRAP.
0 = THE PLATFORM IS NOT INTEL TXT ENABLED.
1 = DEFAULT. THE PLATFORM IS INTEL TXT ENABLED.

Pull-up : METAL KEY
Pull-down : UNIQUE KEY
FOR PC BASED FUSED UNITS THE DEFAULT WILL BE pull-down.
NCSI_RXD_0 NOW HAS pull-up AS THE DEFAULT.

BDE STRAPPING 1

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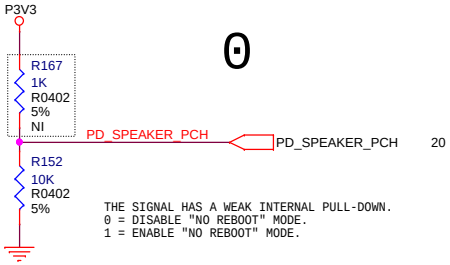
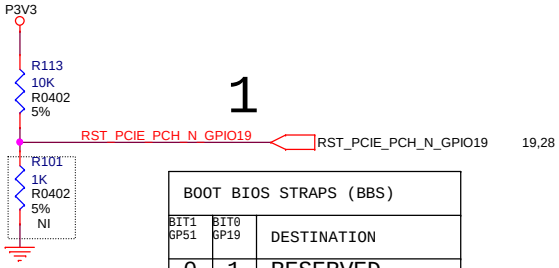
SPKR

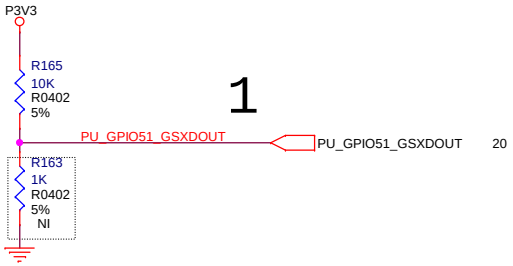


GPIO19

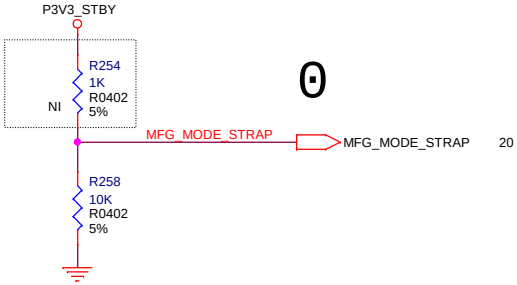


BOOT BIOS STRAPS (BBS)		
BIT1 GP51	BIT0 GP19	DESTINATION
0	1	RESERVED
1	0	RESERVED
1	1	SPI <DEFAULT>
0	0	RESERVED

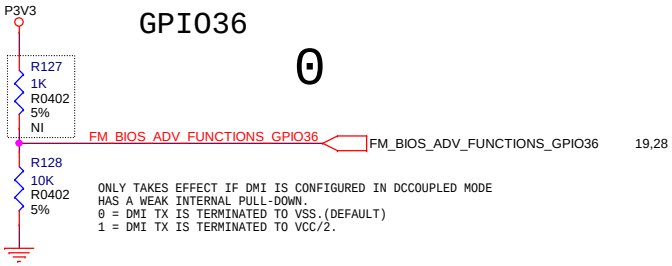
GPIO51



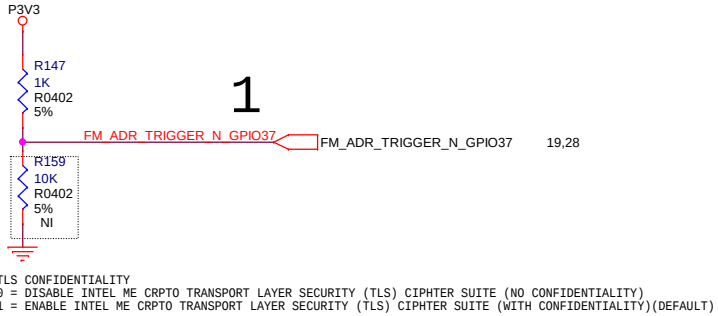
MFG_MODE_STRAP



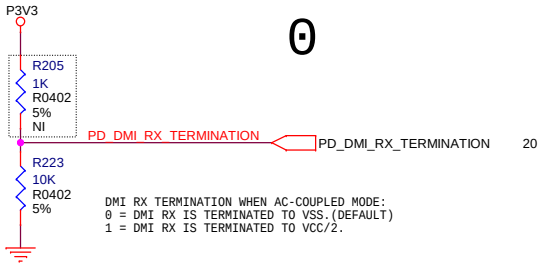
BIOS_ADV_FUNCTIONS GPIO36



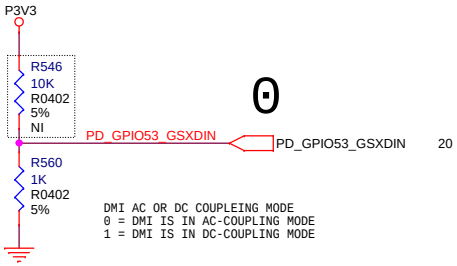
GPIO37



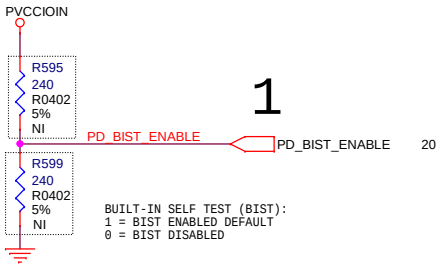
GPIO33



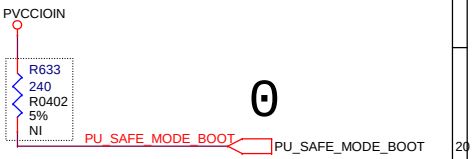
GP53_GSXDIN



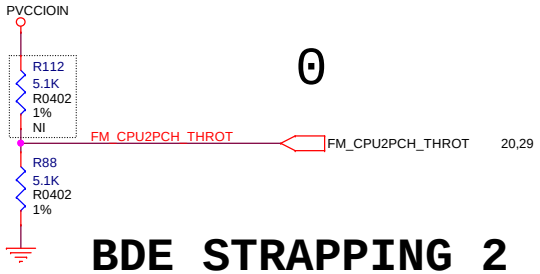
BIST_ENABLE



SAFE_MODE_BOOT



CPU2PCH_THROT



BDE STRAPPING 2

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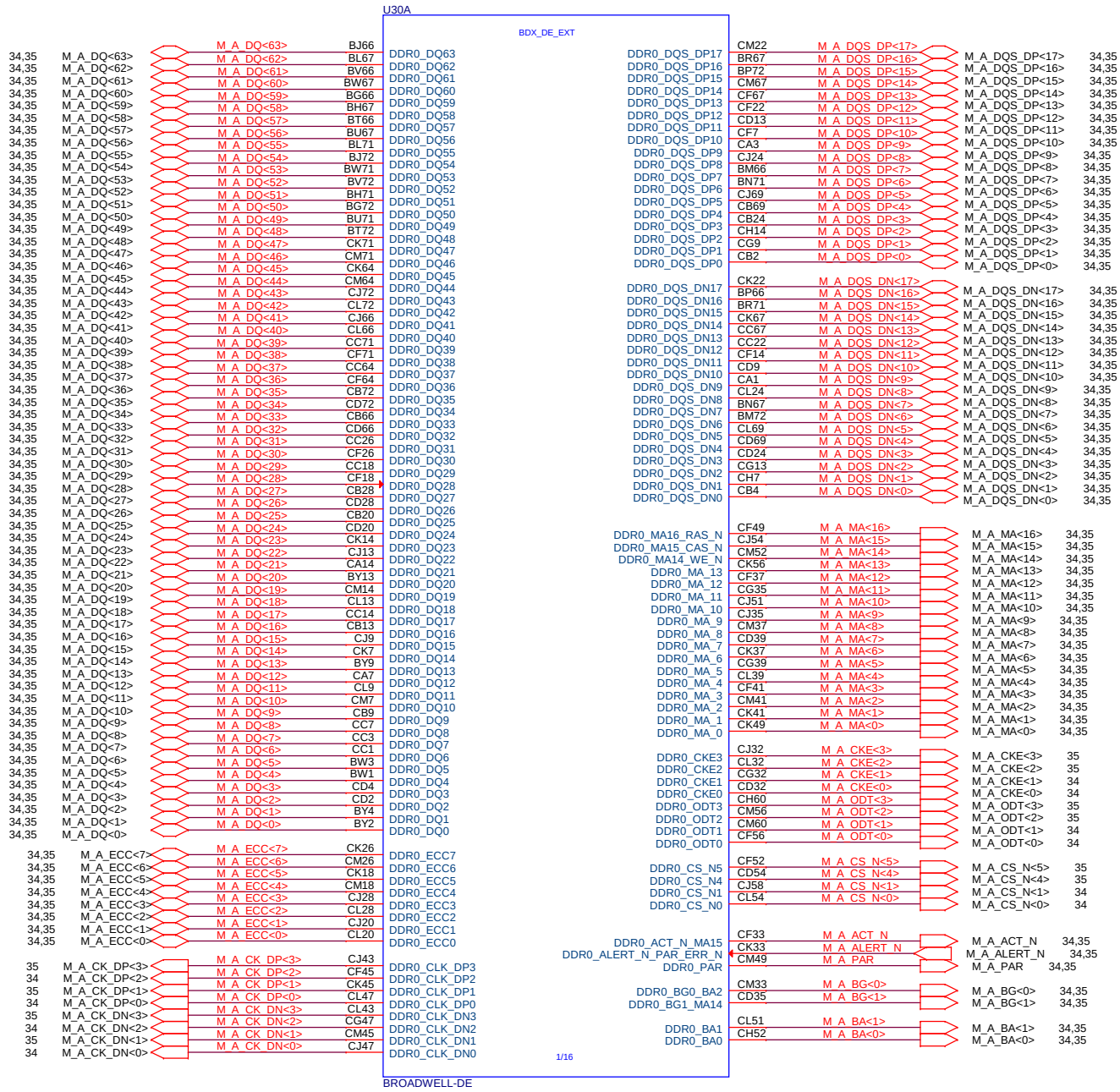

BDX-DE DDR4 CHANNEL A

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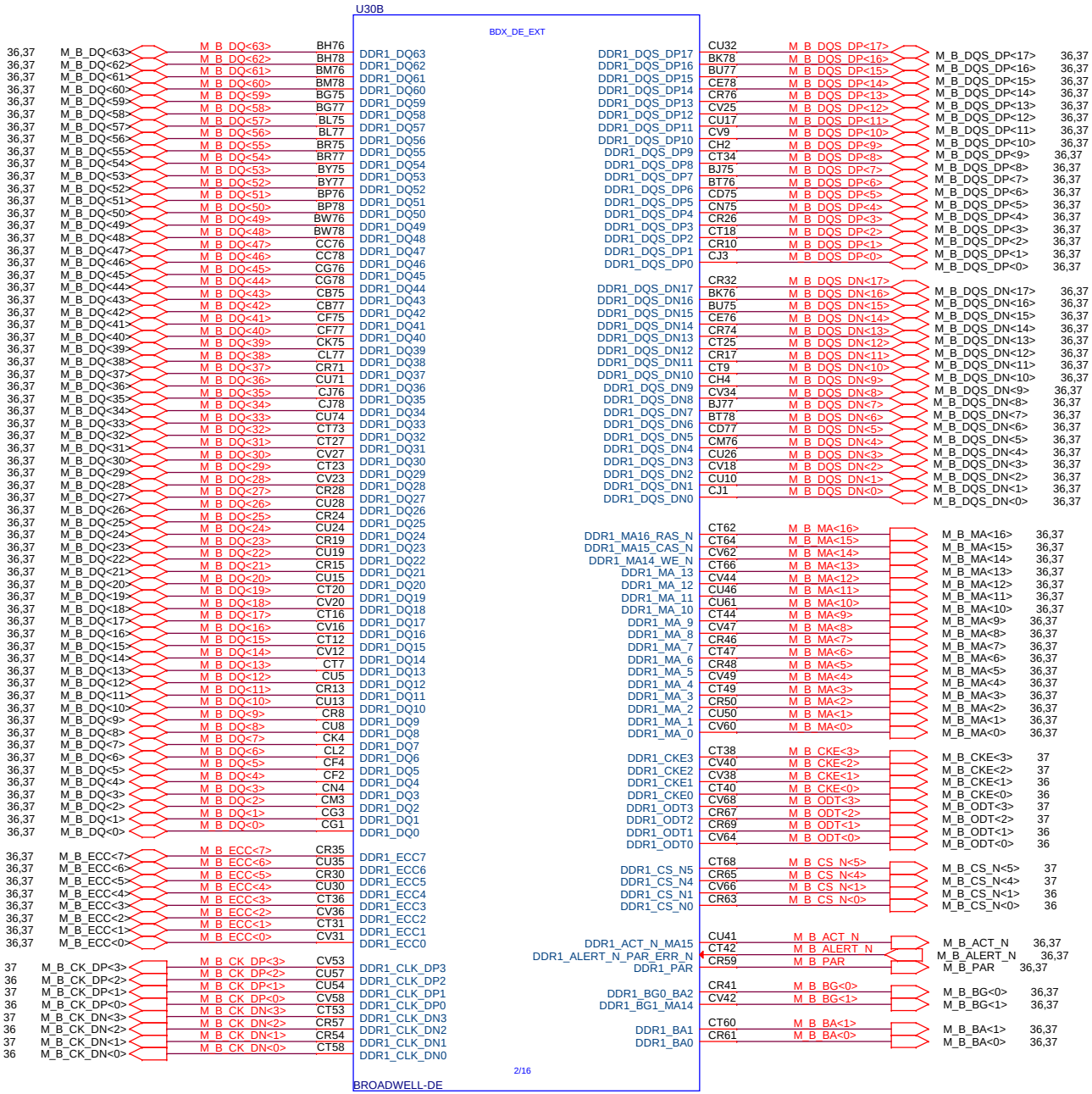

BDX-DE DDR4 CHANNEL B

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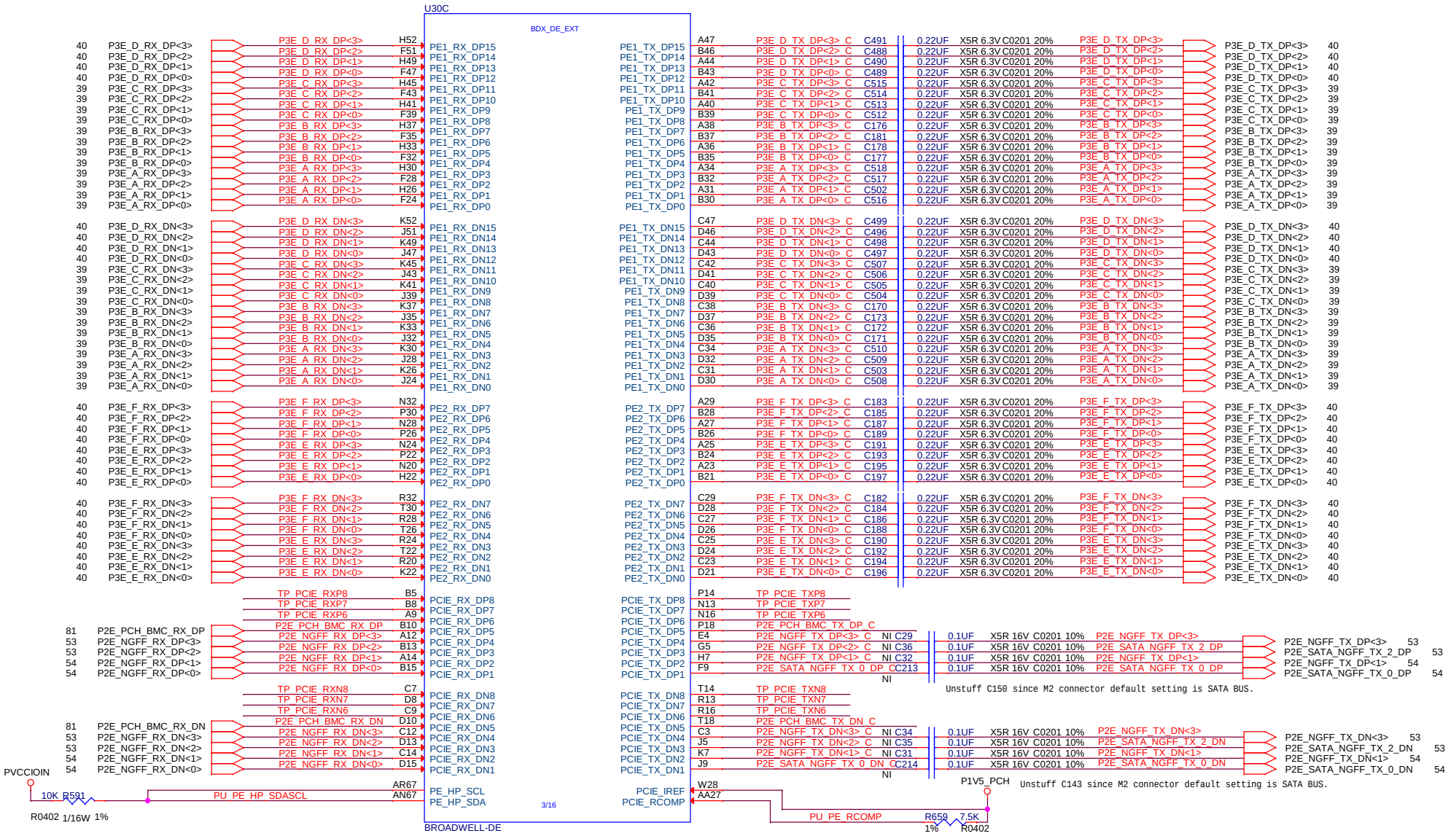

BDX-DE PCIE CPU/PCH

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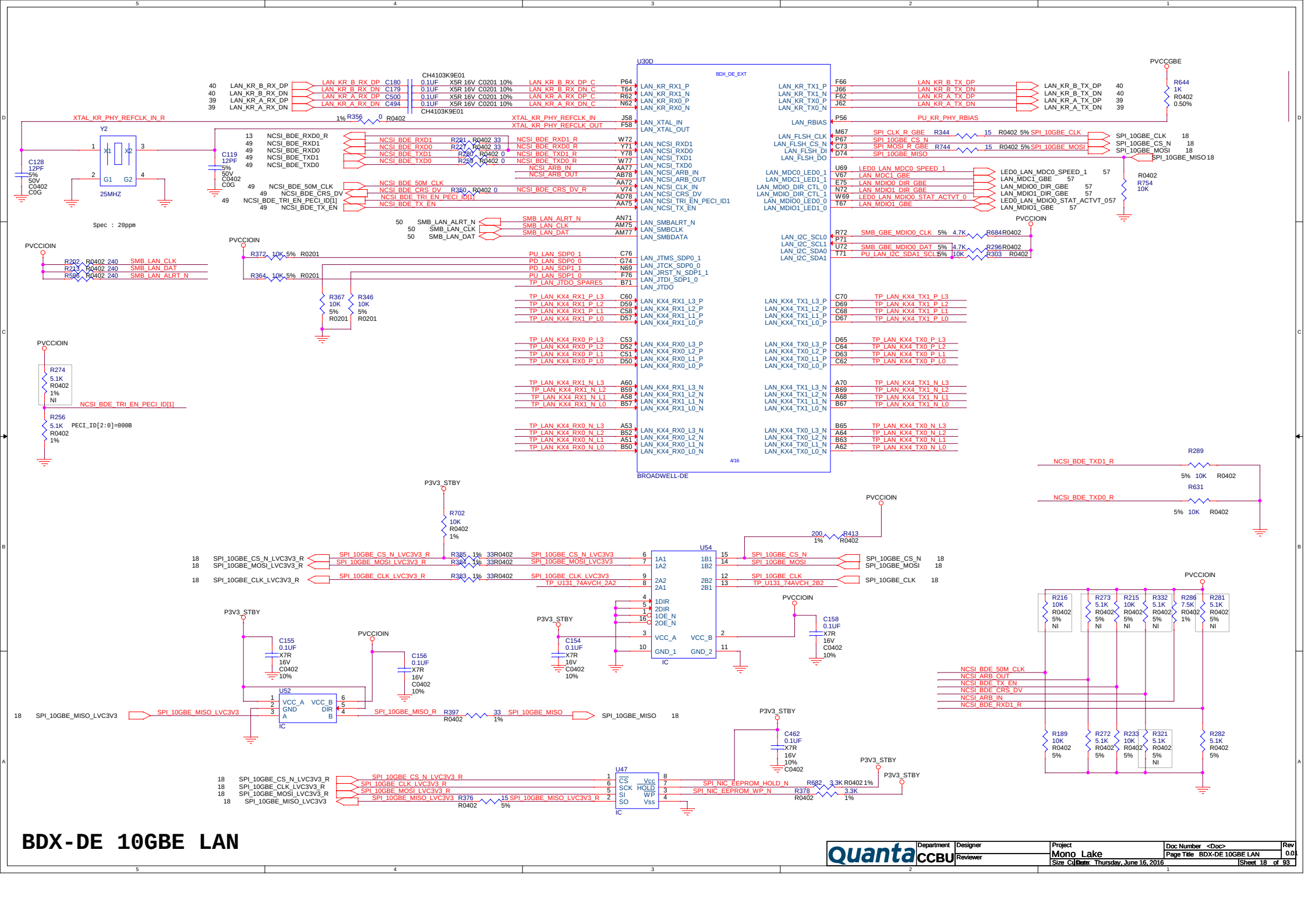
U30D
BDX_DE_EXT
BROADWELL-DE
4/16
CH4103K9E01
Y2
25MHZ
Spec : 20ppm
XTAL_KR_PHY_REFCLK_IN_R
LAN_KR_B_RX_DP
LAN_KR_B_RX_DN
LAN_KR_A_RX_DP
LAN_KR_A_RX_DN
LAN_KR_B_TX_DP
LAN_KR_B_TX_DN
LAN_KR_A_TX_DP
LAN_KR_A_TX_DN
PU_KR_PHY_RBIAS
NCSI_BDE_RXD0_R
NCSI_BDE_RXD1
NCSI_BDE_RXD0
NCSI_BDE_TXD1
NCSI_BDE_TXD0
NCSI_BDE_50M_CLK
NCSI_BDE_CRS_DV
NCSI_BDE_TRI_EN_PECI_ID[1]
NCSI_BDE_TX_EN
SMB_LAN_ALRT_N
SMB_LAN_CLK
SMB_LAN_DAT
SPI_10GBE_CLK
SPI_10GBE_CS_N
SPI_10GBE_MOSI
SPI_10GBE_MISO
LED0_LAN_MDC0_SPEED_1
LAN_MDC1_GBE
LAN_MDIO0_DIR_GBE
LAN_MDIO1_DIR_GBE
LED0_LAN_MDIO0_STAT_ACTVT_0
LAN_MDIO1_GBE
SMB_GBE_MDIO0_CLK
SMB_GBE_MDIO0_DAT
PU_LAN_I2C_SDA1_SCL1
PVCCIOIN
PVCCGBE
P3V3_STBY
IC
U52
U54
U47
NCSI_BDE_TRI_EN_PECI_ID[1]
PECI_ID[2:0]=000B
SPI_10GBE_CS_N_LVC3V3
SPI_10GBE_MOSI_LVC3V3
SPI_10GBE_CLK_LVC3V3
SPI_10GBE_MISO_LVC3V3
TP_U131_74AVCH_2A2
TP_U131_74AVCH_2B2
SPI_NIC_EEPROM_HOLD_N
SPI_NIC_EEPROM_WP_N
NCSI_BDE_TXD1_R
NCSI_BDE_TXD0_R
NCSI_ARB_OUT
NCSI_ARB_IN
NCSI_BDE_RXD1_R
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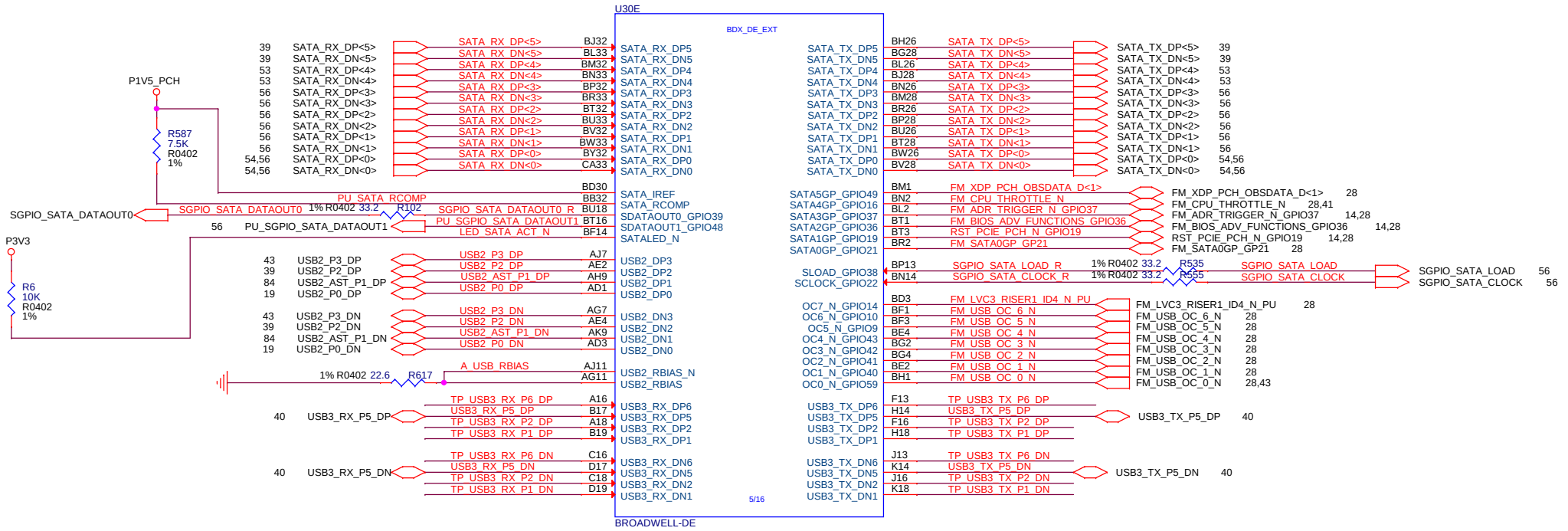

BDX-DE SATA, USB2, USB3

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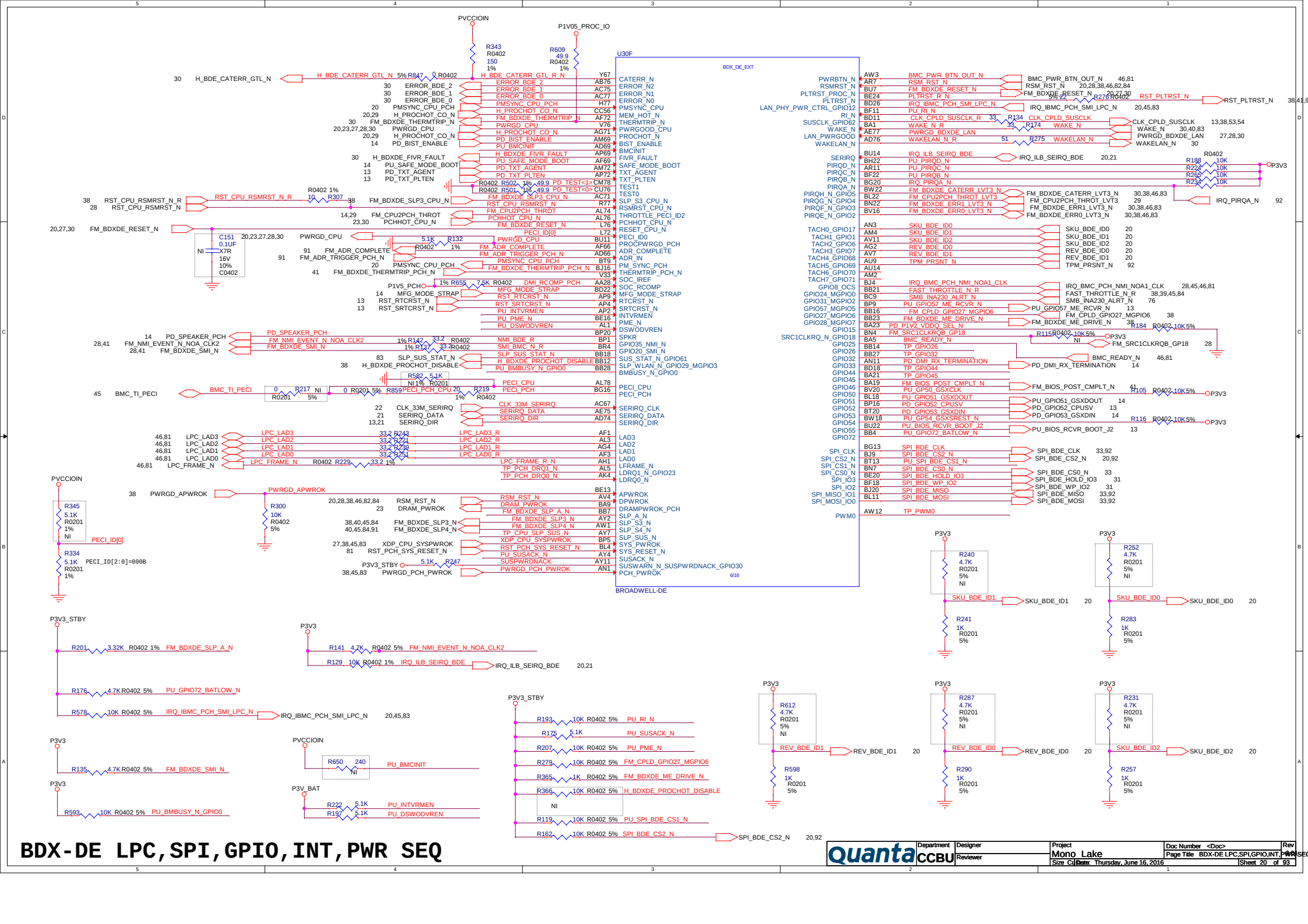
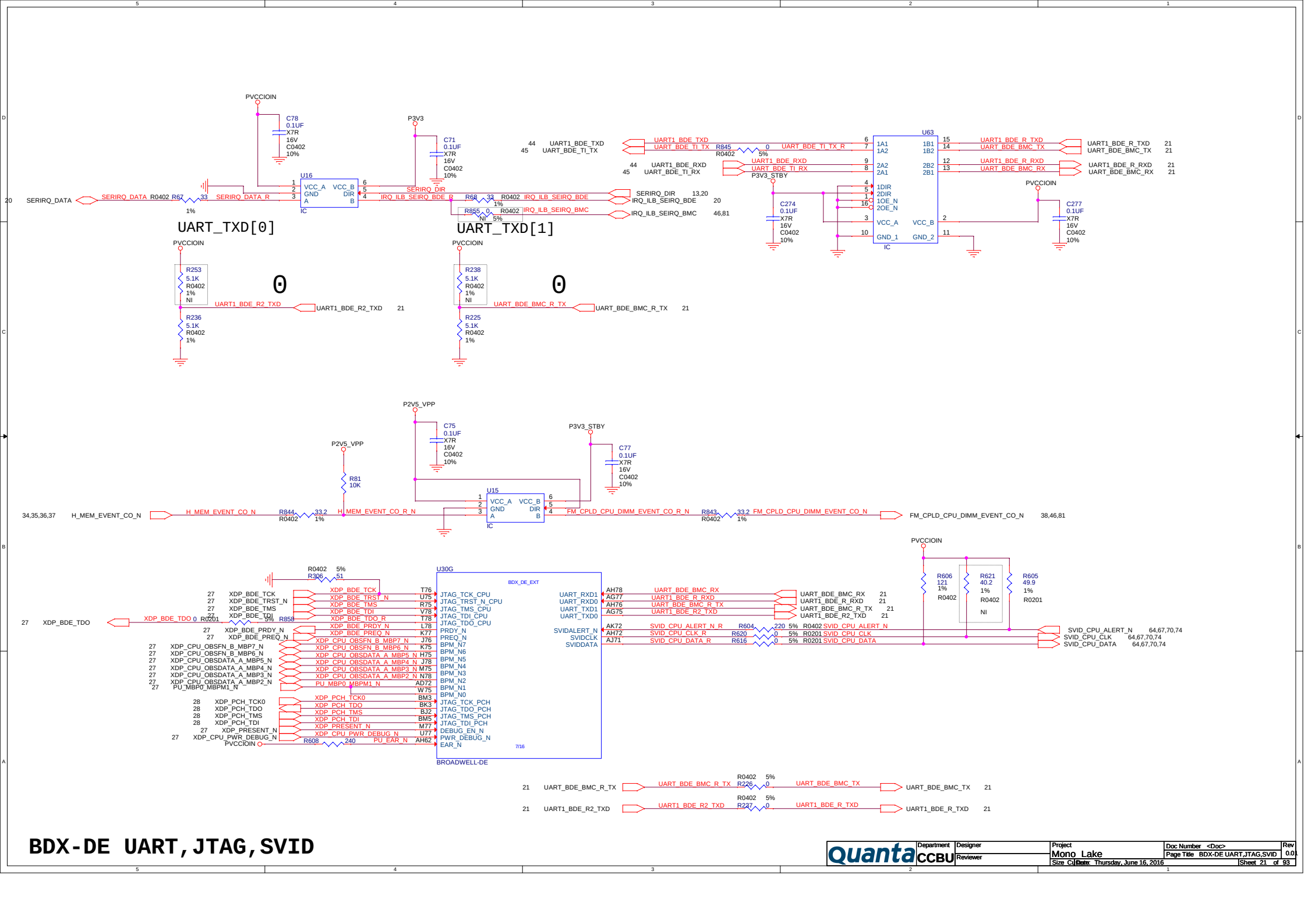


BDX-DE LPC,SPI,GPIO,INT,PWR SEQ



BDX-DE UART,JTAG,SVID

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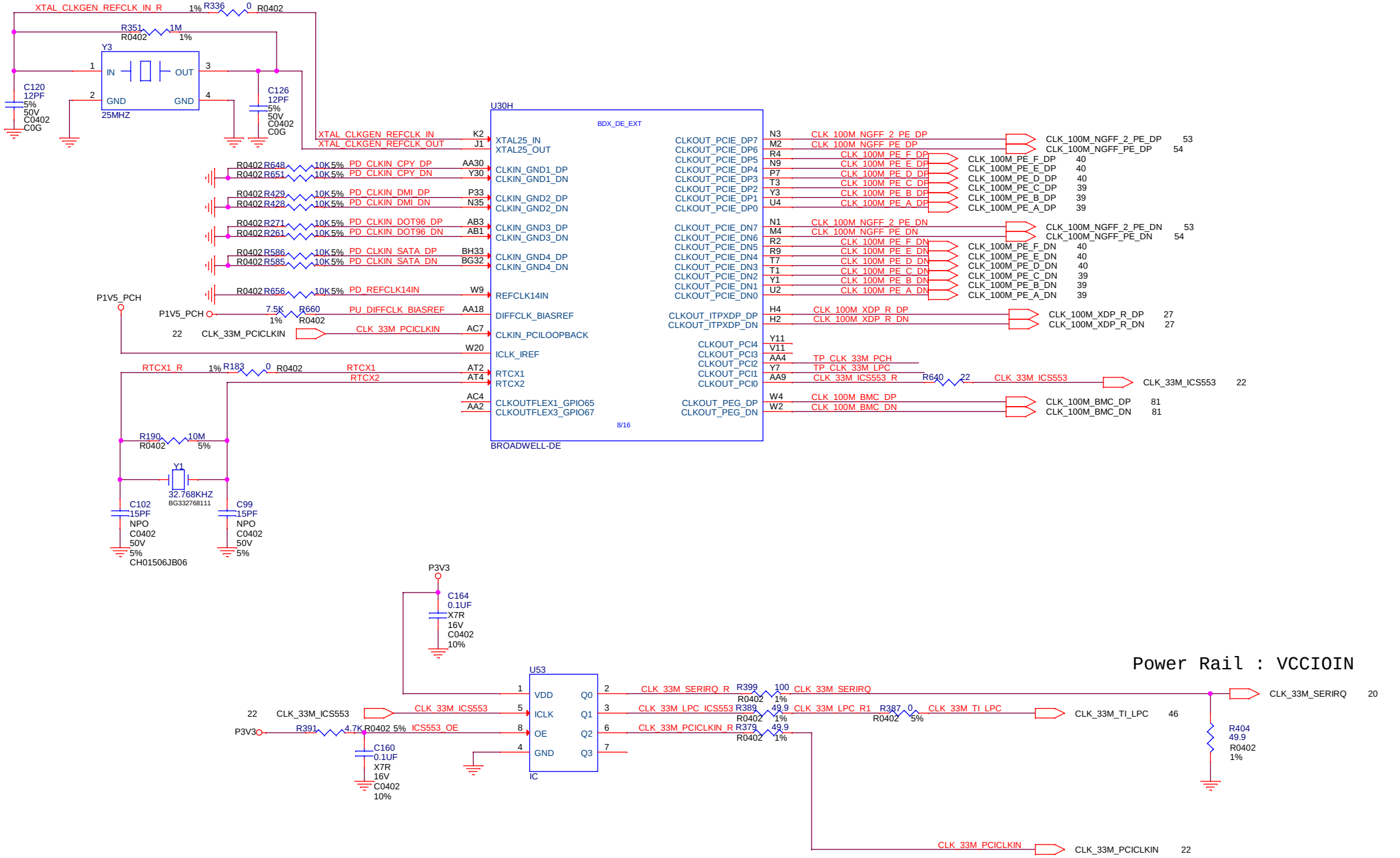

BDX-DE CLK

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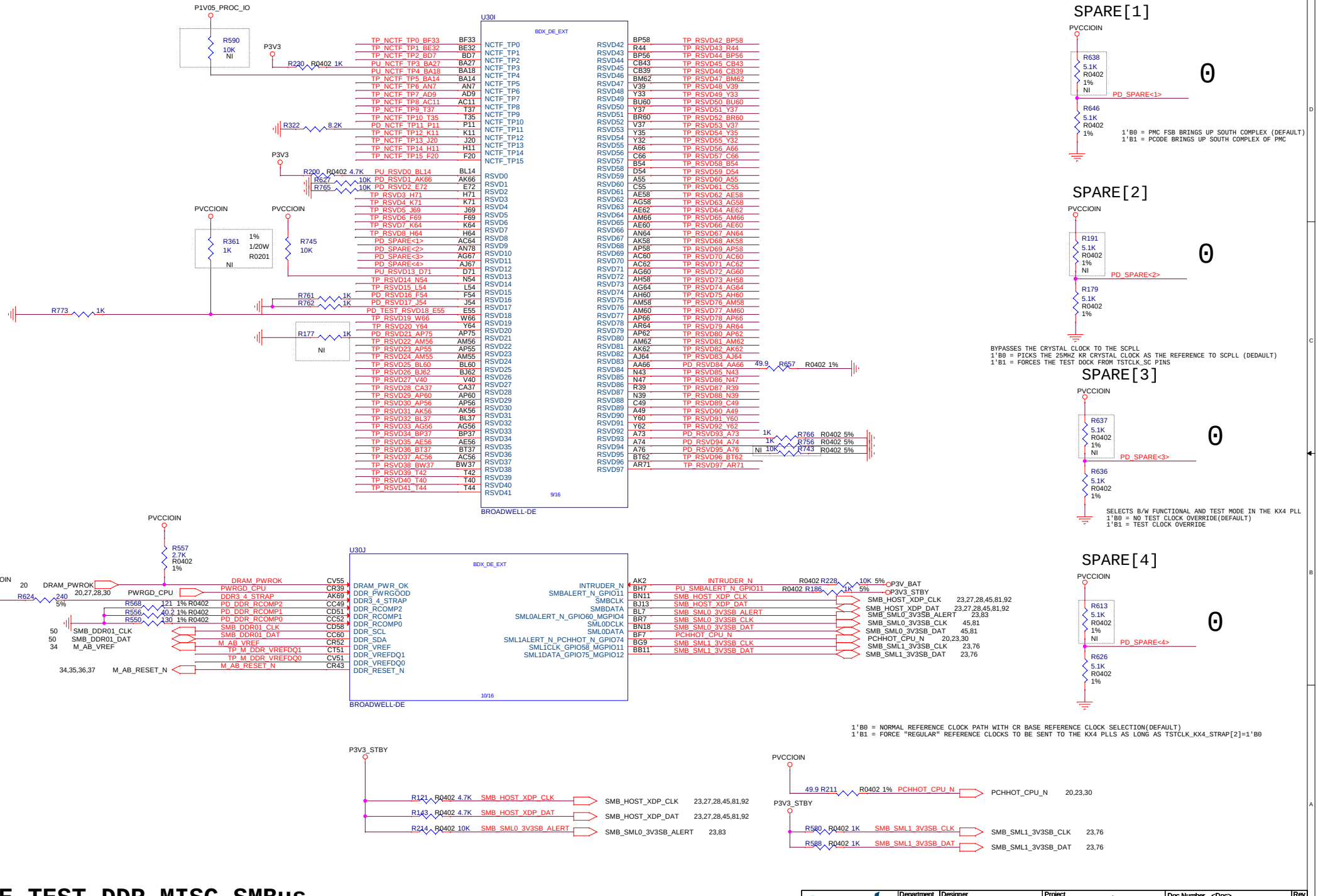

BDX-DE TEST,DDR MISC,SMBus

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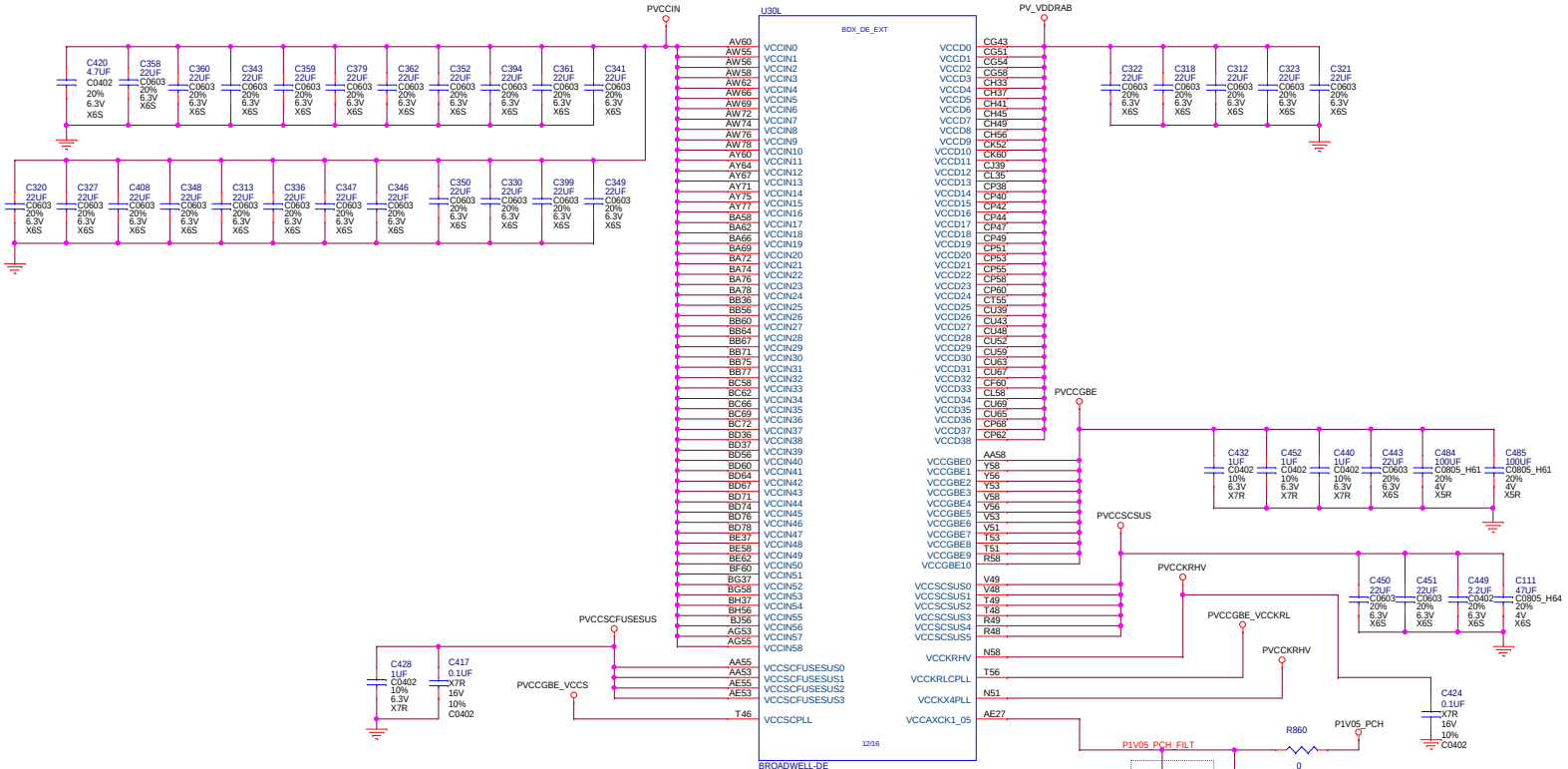

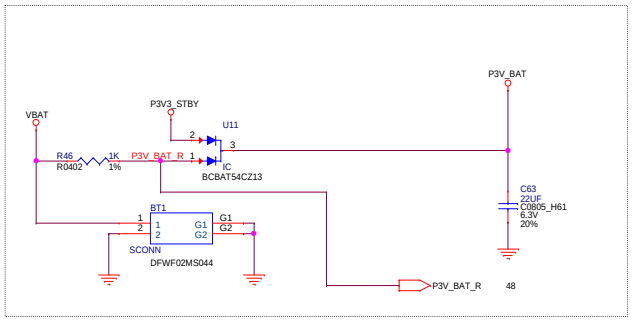

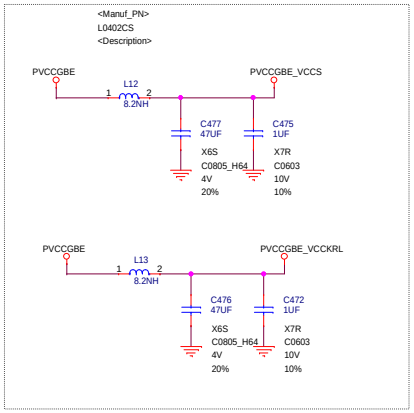

BDX-DE POWER<1>

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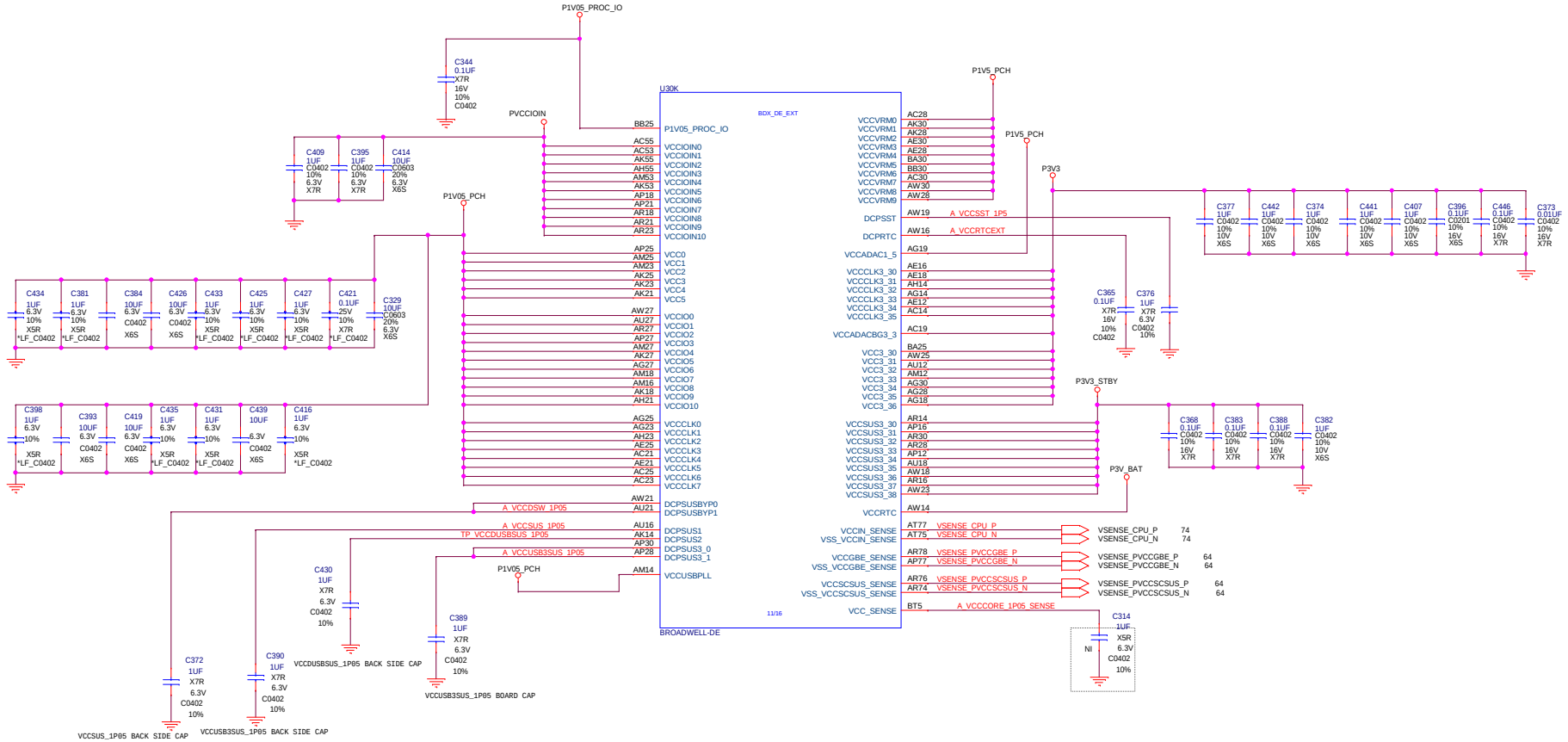

BDX-DE POWER<2>

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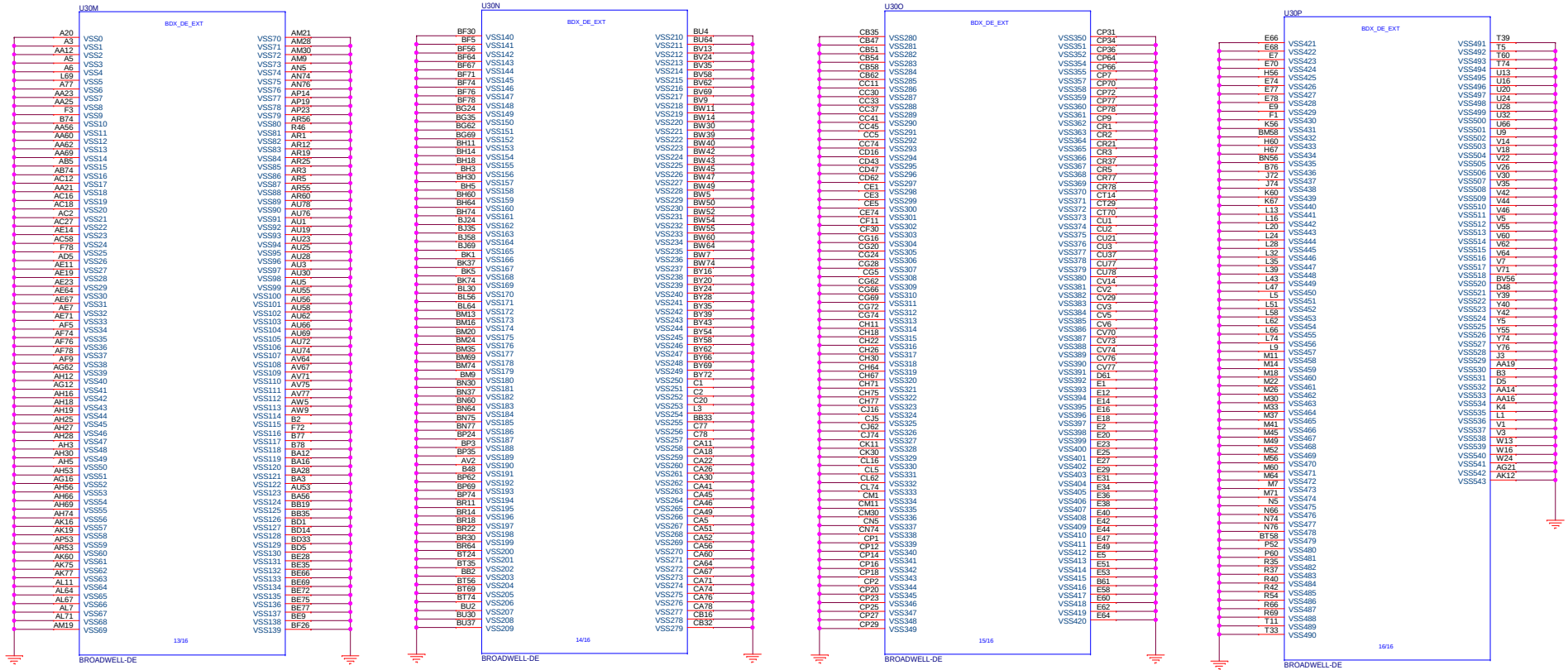

BDX-DE GND

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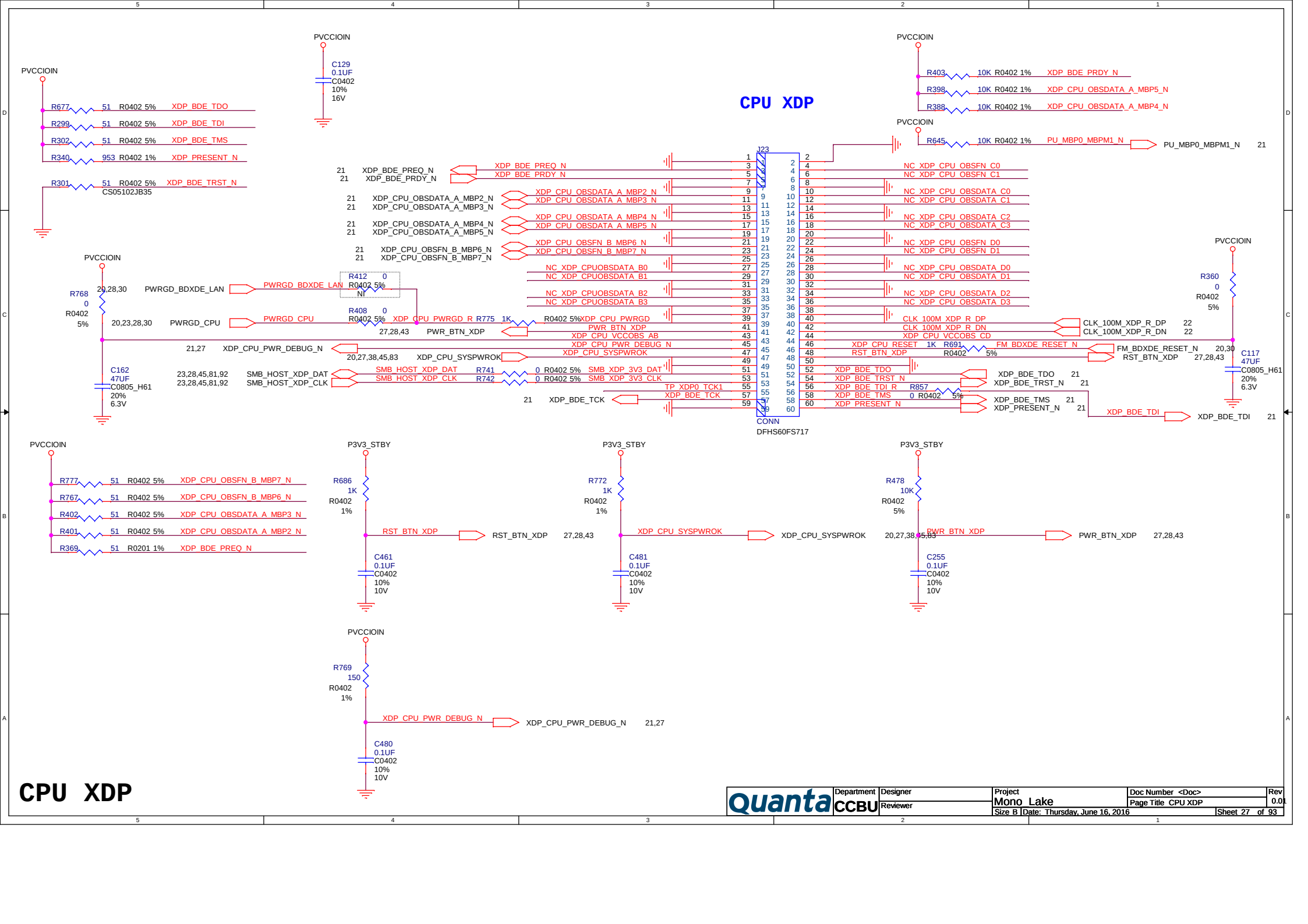
CPU XDP
PVCCIOIN
C129 0.1UF C0402 10% 16V
R677 51 R0402 5% XDP_BDE_TDO
R299 51 R0402 5% XDP_BDE_TDI
R302 51 R0402 5% XDP_BDE_TMS
R340 953 R0402 1% XDP_PRESENT_N
R301 51 R0402 5% XDP_BDE_TRST_N
CS05102JB35
R403 10K R0402 1% XDP_BDE_PRDY_N
R398 10K R0402 1% XDP_CPU_OBSDATA_A_MBP5_N
R388 10K R0402 1% XDP_CPU_OBSDATA_A_MBP4_N
R645 10K R0402 1% PU_MBP0_MBPM1_N
PU_MBP0_MBPM1_N 21
J23
CONN
DFHS60FS717
XDP_BDE_PREQ_N
XDP_BDE_PRDY_N
XDP_CPU_OBSDATA_A_MBP2_N
XDP_CPU_OBSDATA_A_MBP3_N
XDP_CPU_OBSDATA_A_MBP4_N
XDP_CPU_OBSDATA_A_MBP5_N
XDP_CPU_OBSFN_B_MBP6_N
XDP_CPU_OBSFN_B_MBP7_N
NC_XDP_CPUOBSDATA_B0
NC_XDP_CPUOBSDATA_B1
NC_XDP_CPUOBSDATA_B2
NC_XDP_CPUOBSDATA_B3
NC_XDP_CPU_OBSFN_C0
NC_XDP_CPU_OBSFN_C1
NC_XDP_CPU_OBSDATA_C0
NC_XDP_CPU_OBSDATA_C1
NC_XDP_CPU_OBSDATA_C2
NC_XDP_CPU_OBSDATA_C3
NC_XDP_CPU_OBSFN_D0
NC_XDP_CPU_OBSFN_D1
NC_XDP_CPU_OBSDATA_D0
NC_XDP_CPU_OBSDATA_D1
NC_XDP_CPU_OBSDATA_D2
NC_XDP_CPU_OBSDATA_D3
CLK_100M_XDP_R_DP
CLK_100M_XDP_R_DN
XDP_CPU_VCCOBS_CD
XDP_CPU_VCCOBS_AB
XDP_CPU_PWRGD
PWR_BTN_XDP
XDP_CPU_PWR_DEBUG_N
XDP_CPU_SYSPWROK
XDP_CPU_RESET
RST_BTN_XDP
FM_BDXDE_RESET_N
SMB_XDP_3V3_DAT
SMB_XDP_3V3_CLK
XDP_BDE_TDO
XDP_BDE_TRST_N
XDP_BDE_TDI_R
XDP_BDE_TMS
XDP_PRESENT_N
TP_XDP0_TCK1
XDP_BDE_TCK
PWRGD_BDXDE_LAN
PWRGD_CPU
SMB_HOST_XDP_DAT
SMB_HOST_XDP_CLK
R768 0 R0402 5%
R412 0 R0402 5% NI
R408 0 R0402 5%
R775 1K R0402 5%
R691 1K R0402 5%
R741 0 R0402 5%
R742 0 R0402 5%
R857 0 R0402 5%
R360 0 R0402 5%
C162 47UF C0805_H61 20% 6.3V
C117 47UF C0805_H61 20% 6.3V
R777 51 R0402 5% XDP_CPU_OBSFN_B_MBP7_N
R767 51 R0402 5% XDP_CPU_OBSFN_B_MBP6_N
R402 51 R0402 5% XDP_CPU_OBSDATA_A_MBP3_N
R401 51 R0402 5% XDP_CPU_OBSDATA_A_MBP2_N
R369 51 R0201 1% XDP_BDE_PREQ_N
P3V3_STBY
R686 1K R0402 1%
R772 1K R0402 1%
R478 10K R0402 5%
C461 0.1UF C0402 10% 10V
C481 0.1UF C0402 10% 10V
C255 0.1UF C0402 10% 10V
R769 150 R0402 1%
C480 0.1UF C0402 10% 10V
CPU XDP
Quanta
Department CCBU
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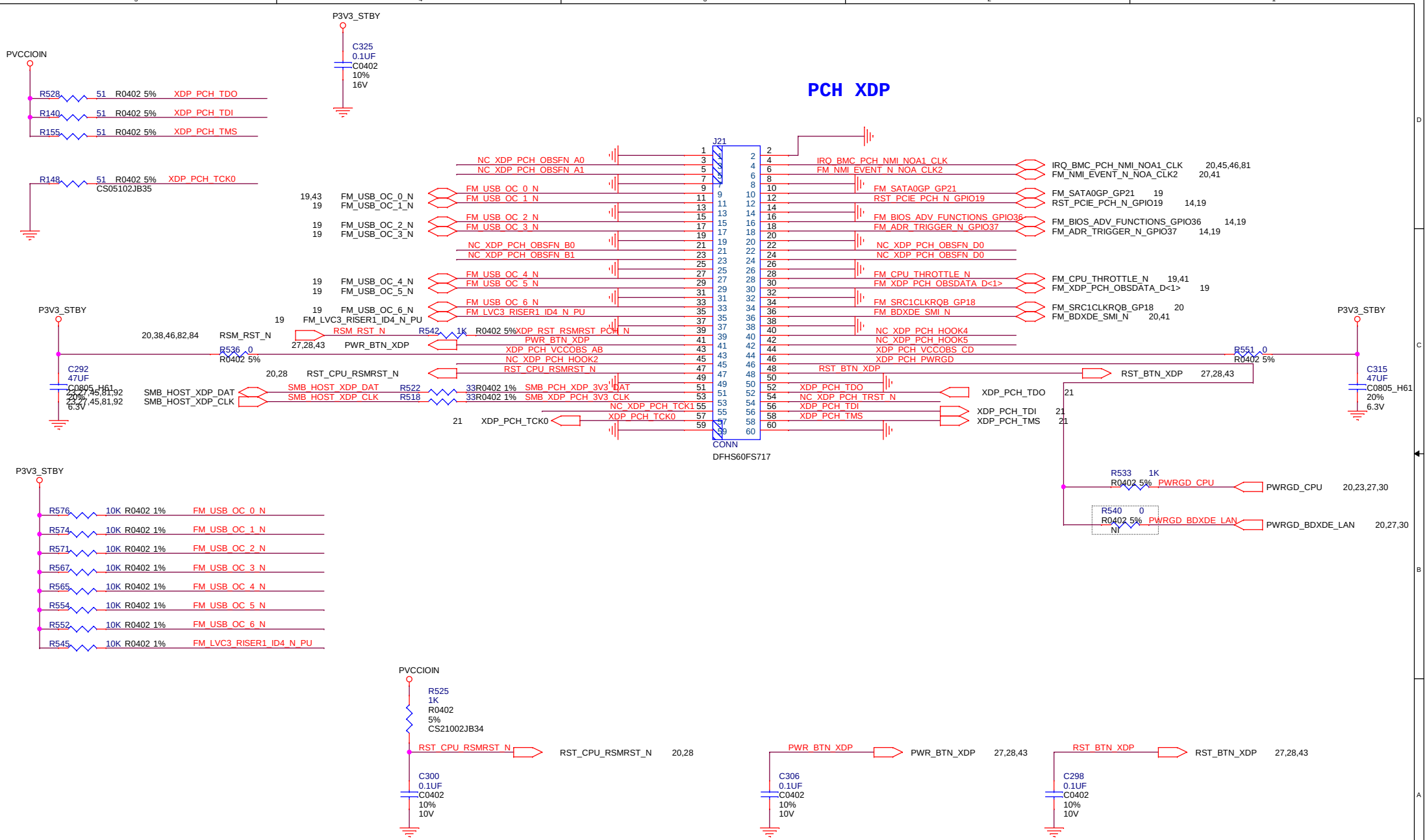
PCH XDP
P3V3_STBY
PVCCIOIN
C325
0.1UF
C0402
10%
16V
R528 51 R0402 5% XDP_PCH_TDO
R140 51 R0402 5% XDP_PCH_TDI
R155 51 R0402 5% XDP_PCH_TMS
R148 51 R0402 5% XDP_PCH_TCK0
CS05102JB35
J21
CONN
DFHS60FS717
NC_XDP_PCH_OBSFN_A0
NC_XDP_PCH_OBSFN_A1
FM_USB_OC_0_N
FM_USB_OC_1_N
FM_USB_OC_2_N
FM_USB_OC_3_N
NC_XDP_PCH_OBSFN_B0
NC_XDP_PCH_OBSFN_B1
FM_USB_OC_4_N
FM_USB_OC_5_N
FM_USB_OC_6_N
FM_LVC3_RISER1_ID4_N_PU
RSM_RST_N
PWR_BTN_XDP
XDP_PCH_VCCOBS_AB
NC_XDP_PCH_HOOK2
RST_CPU_RSMRST_N
SMB_HOST_XDP_DAT
SMB_HOST_XDP_CLK
SMB_PCH_XDP_3V3_DAT
SMB_XDP_PCH_3V3_CLK
NC_XDP_PCH_TCK1
XDP_PCH_TCK0
XDP_RST_RSMRST_PCH_N
IRQ_BMC_PCH_NMI_NOA1_CLK
FM_NMI_EVENT_N_NOA_CLK2
FM_SATA0GP_GP21
RST_PCIE_PCH_N_GPIO19
FM_BIOS_ADV_FUNCTIONS_GPIO36
FM_ADR_TRIGGER_N_GPIO37
NC_XDP_PCH_OBSFN_D0
FM_CPU_THROTTLE_N
FM_XDP_PCH_OBSDATA_D<1>
FM_SRC1CLKRQB_GP18
FM_BDXDE_SMI_N
NC_XDP_PCH_HOOK4
NC_XDP_PCH_HOOK5
XDP_PCH_VCCOBS_CD
XDP_PCH_PWRGD
RST_BTN_XDP
XDP_PCH_TDO
NC_XDP_PCH_TRST_N
XDP_PCH_TDI
XDP_PCH_TMS
R536 0 R0402 5%
R542 1K R0402 5%
R522 33R0402 1%
R518 33R0402 1%
R551 0 R0402 5%
C292 47UF C0805_H61 20% 6.3V
C315 47UF C0805_H61 20% 6.3V
R533 1K R0402 5% PWRGD_CPU
R540 0 R0402 5% PWRGD_BDXDE_LAN NI
R576 10K R0402 1% FM_USB_OC_0_N
R574 10K R0402 1% FM_USB_OC_1_N
R571 10K R0402 1% FM_USB_OC_2_N
R567 10K R0402 1% FM_USB_OC_3_N
R565 10K R0402 1% FM_USB_OC_4_N
R554 10K R0402 1% FM_USB_OC_5_N
R552 10K R0402 1% FM_USB_OC_6_N
R545 10K R0402 1% FM_LVC3_RISER1_ID4_N_PU
R525 1K R0402 5% CS21002JB34
C300 0.1UF C0402 10% 10V
C306 0.1UF C0402 10% 10V
C298 0.1UF C0402 10% 10V
PWRGD_CPU
PWRGD_BDXDE_LAN
PCH XDP
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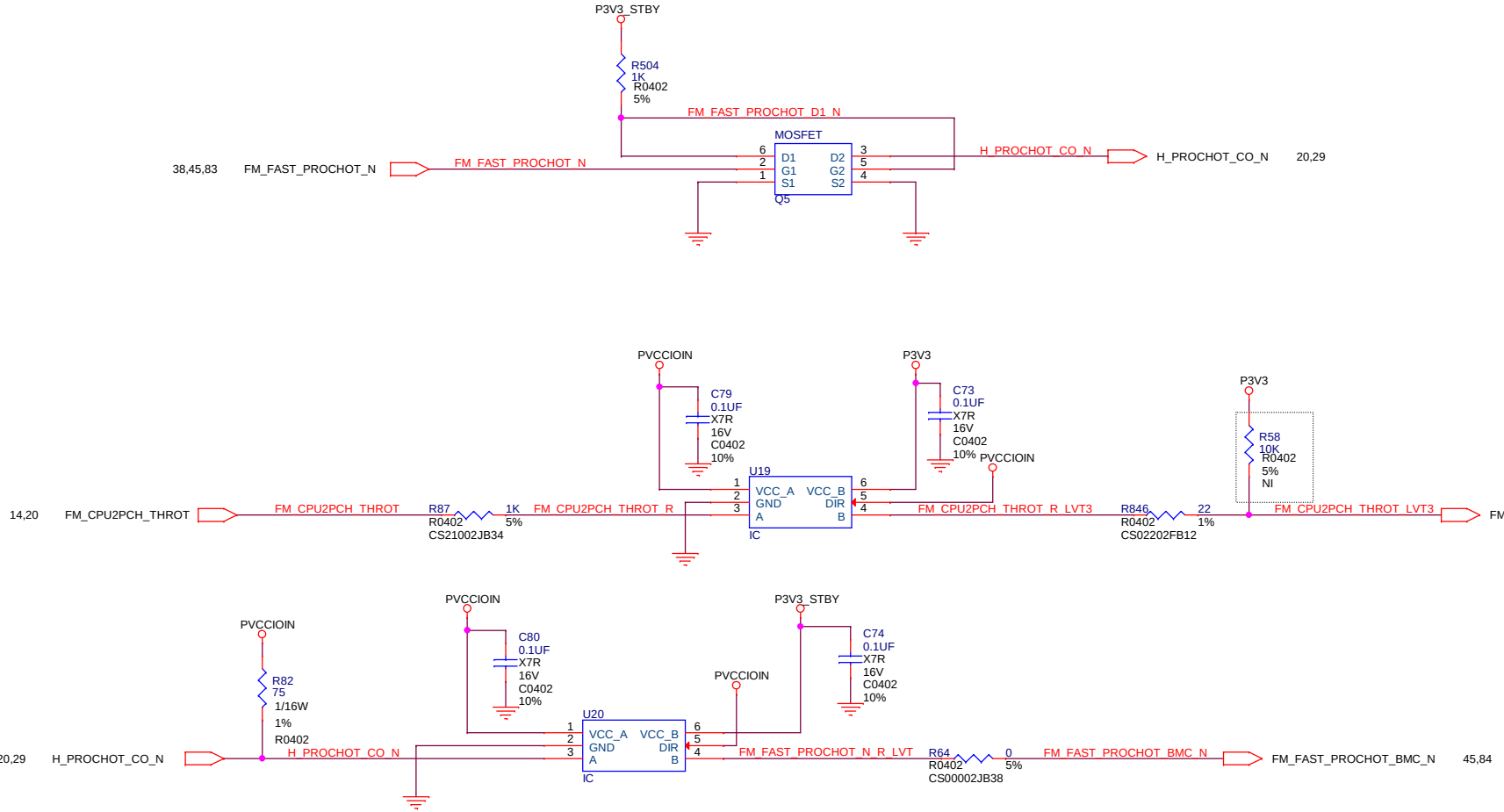

ERROR CNTL 1

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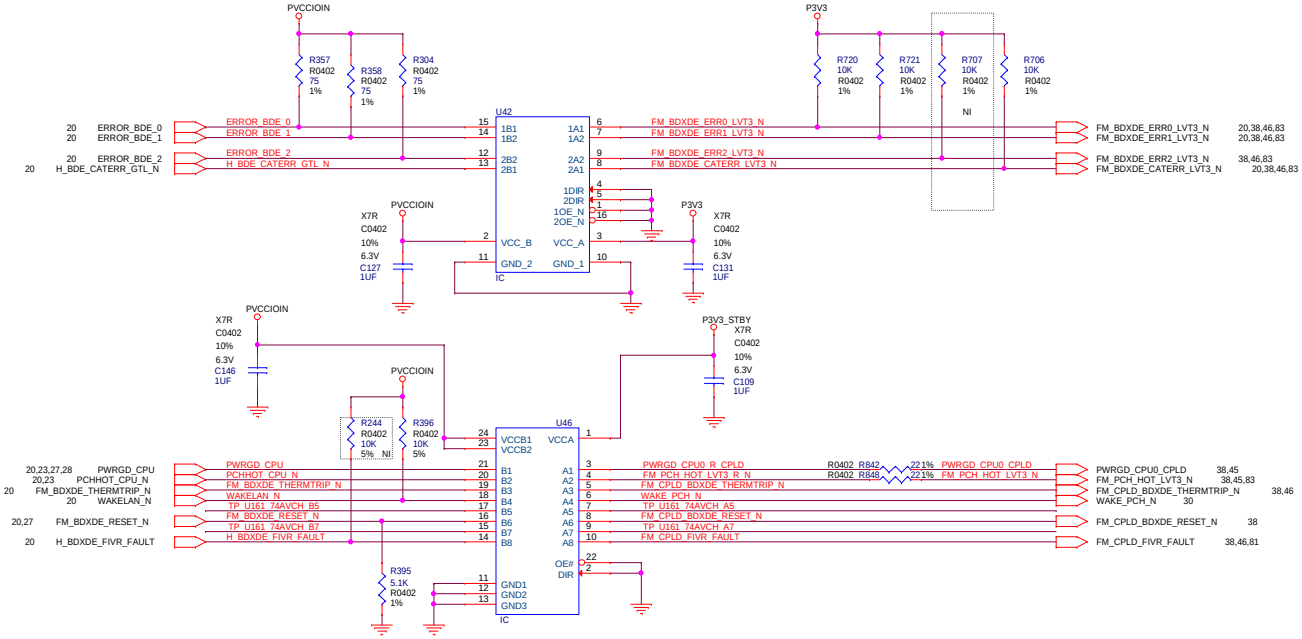
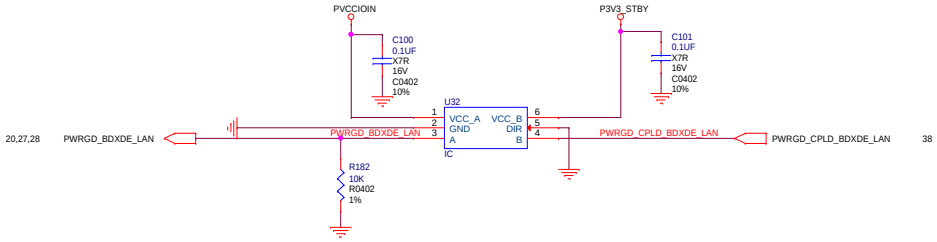
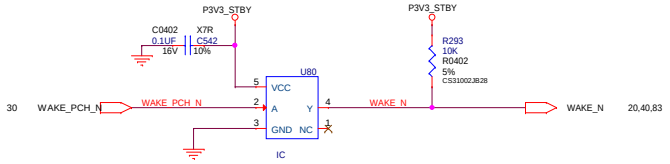
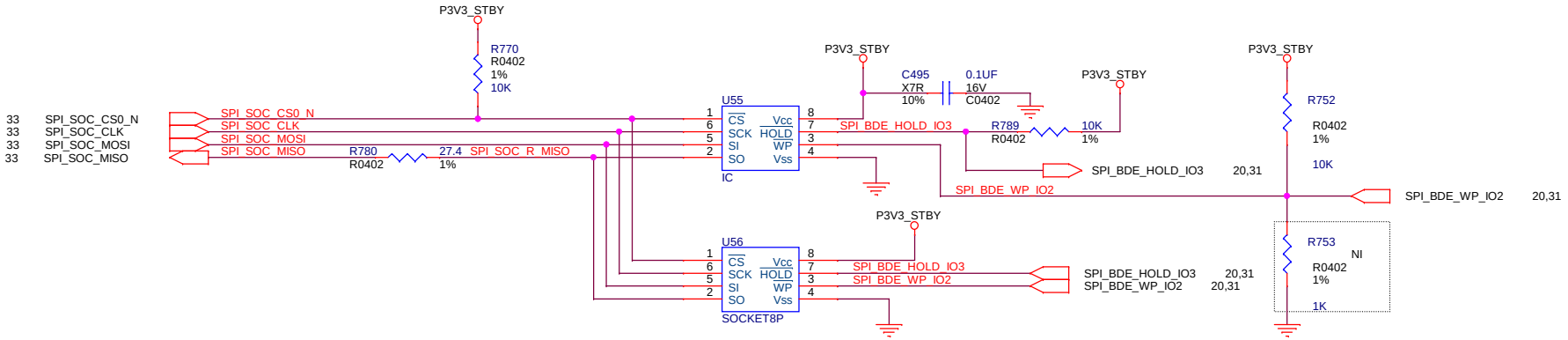






ERROR CNTL 2

Quanta	Department CCBU	Designer	Project Mono_Lake	Doc Number <Doc>	Rev 0.01
		Reviewer		Page Title ERROR CNTL 2	
			Size C Date: Thursday, June 16, 2016	Sheet 30 of 93	



CPU SPI

Quanta	Department CCBU	Designer	Project Mono_Lake	Doc Number <Doc>	Rev 0.01
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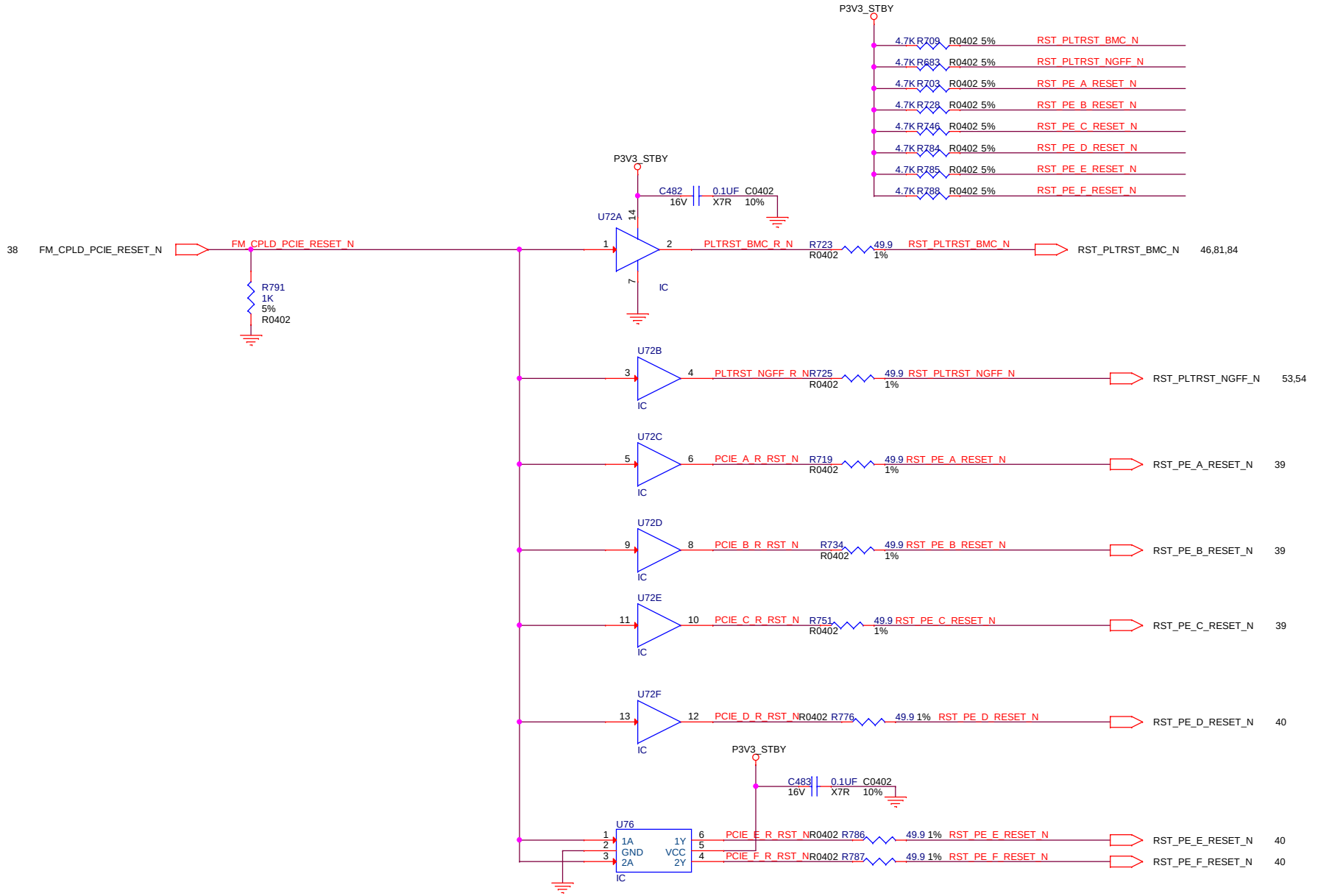

PLTRST_BUFFER

Quanta	Department CCBU	Designer	Project Mono_Lake	Doc Number <Doc>	Rev 0.01
		Reviewer		Page Title PLTRST_BUFFER	
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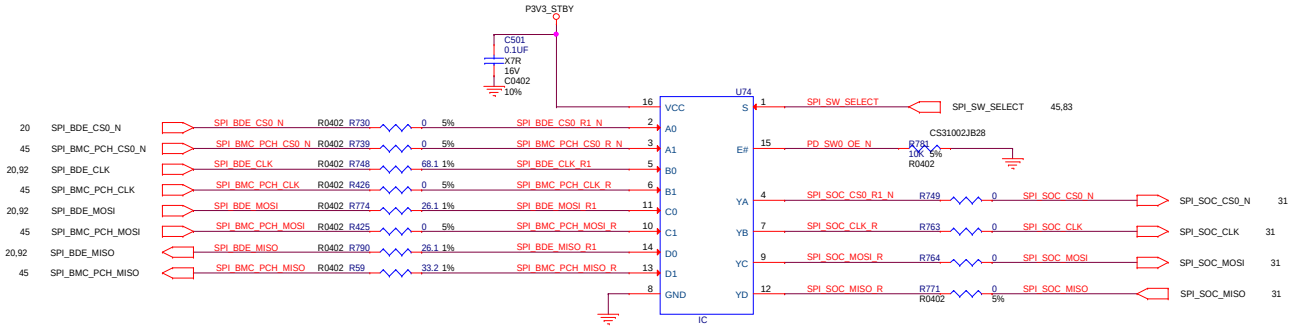

SPI MUX

Quanta	Department CCBU	Designer	Project Mono_Lake	Doc Number <Doc>	Rev 0.01
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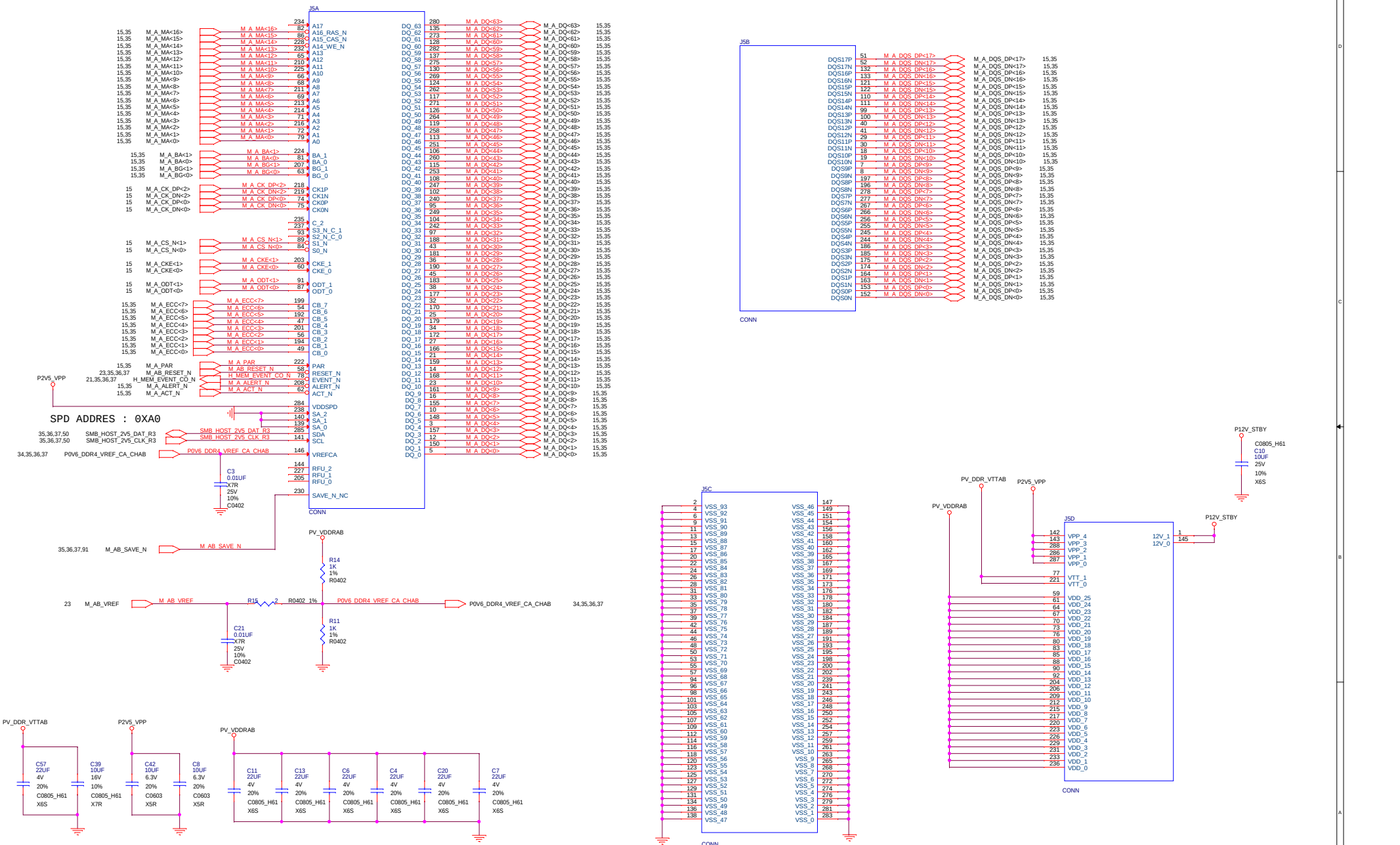

DDR4 RDIMM CHA_1

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		Reviewer	Page Title: DDR4 RDIMM CHA_1	
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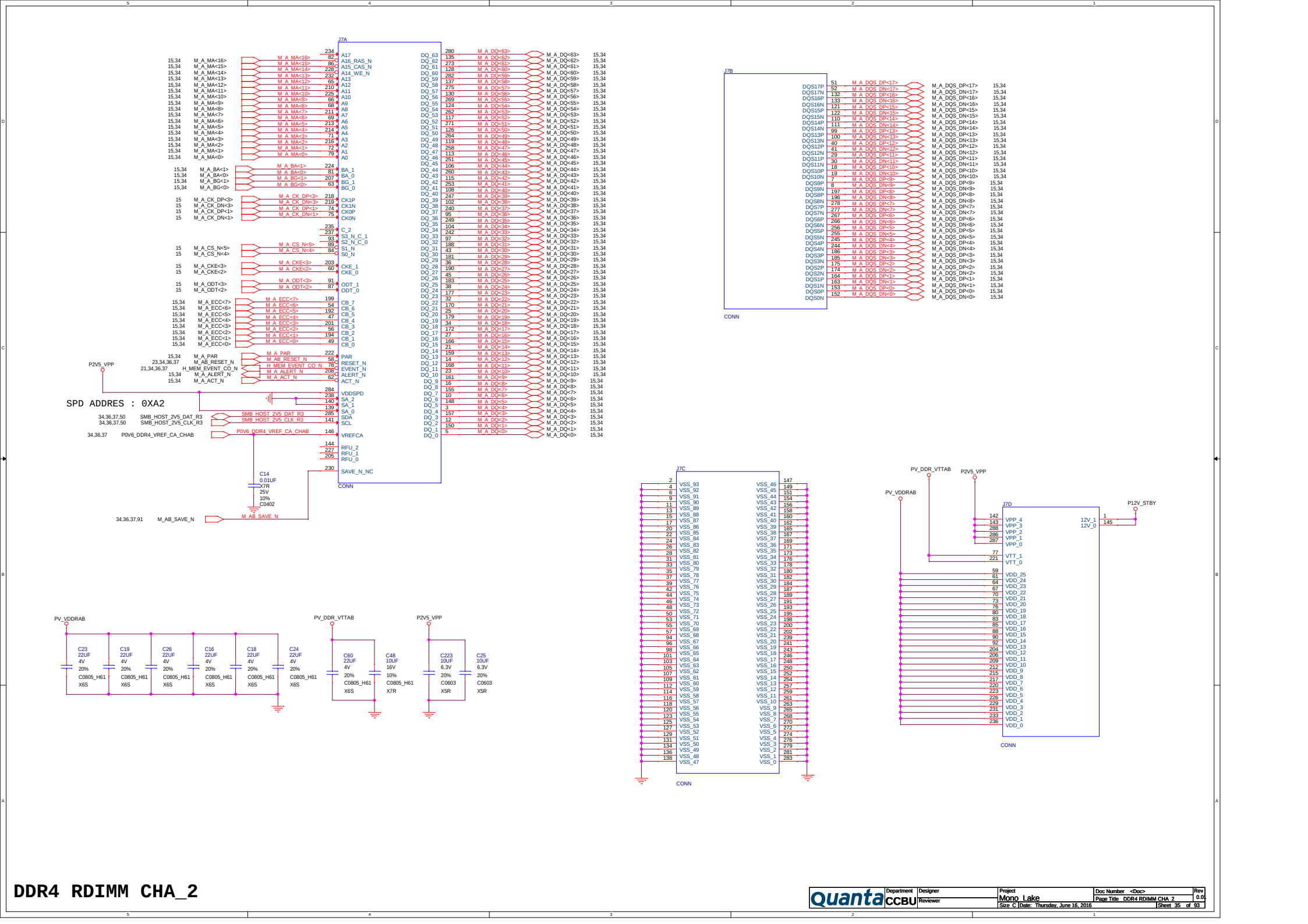
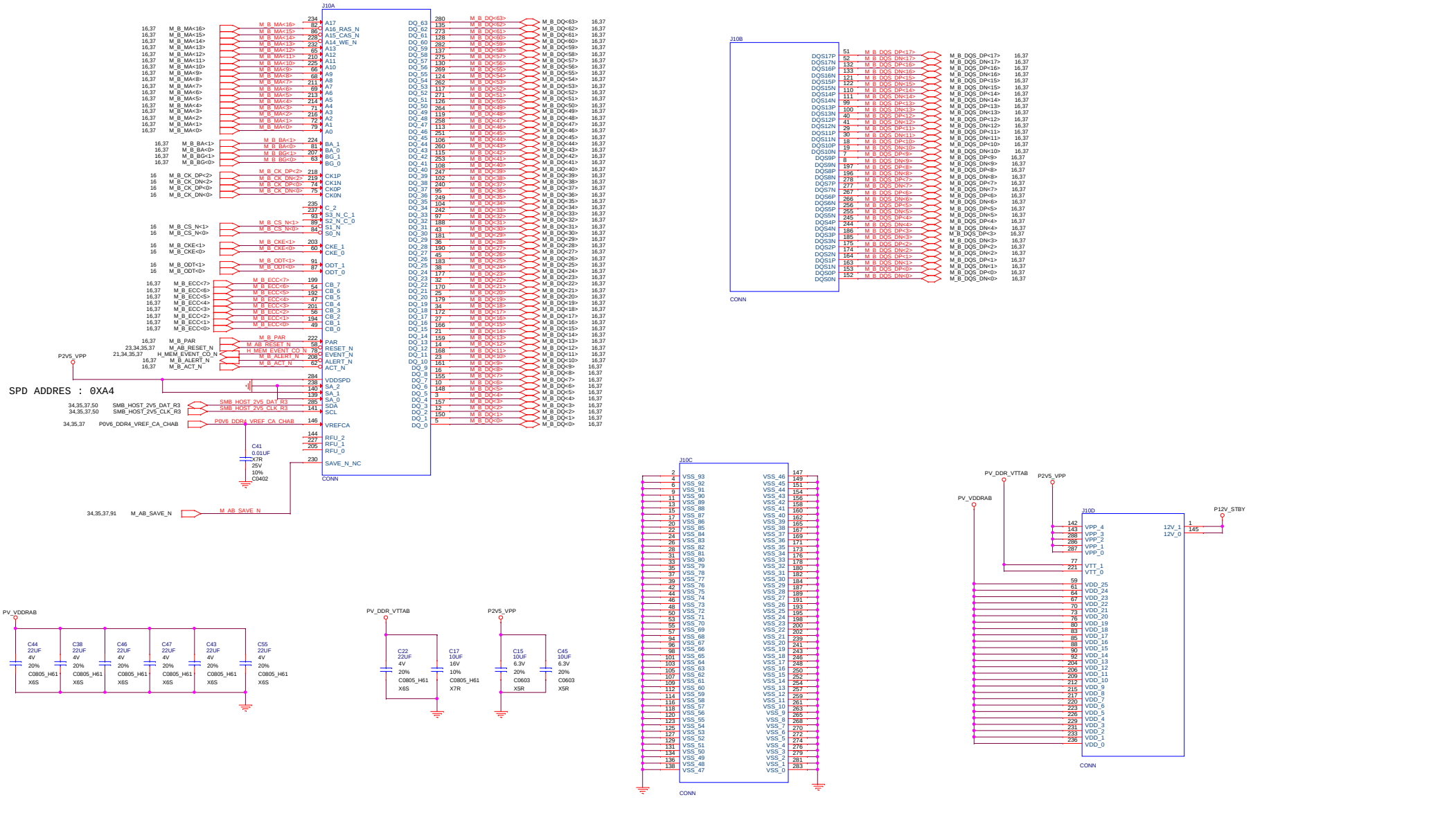


DDR4 RDIMM CHA_2

Quanta	Department: CCBU	Designer	Project: Mono_Lake	Doc Number: <Doc> Rev: 0.0
		Reviewer	Page Title: DDR4 RDIMM CHA_2	
			Size: C Date: Thursday, June 16, 2016	Sheet 35 of 93



DDR4 RDIMM CHB_1

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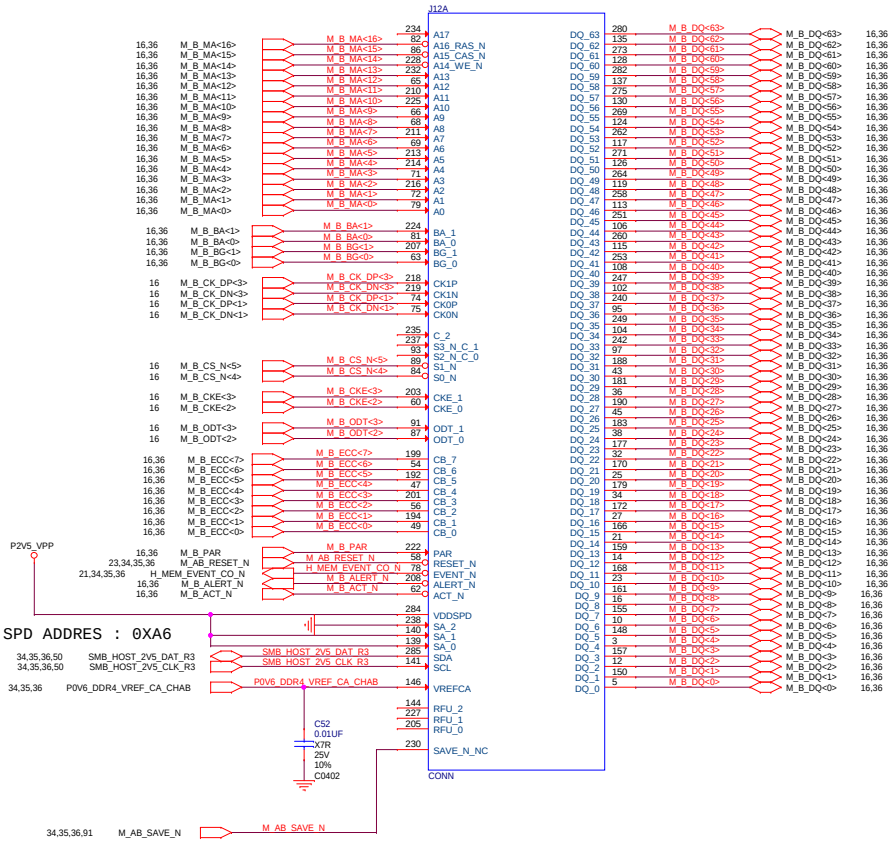

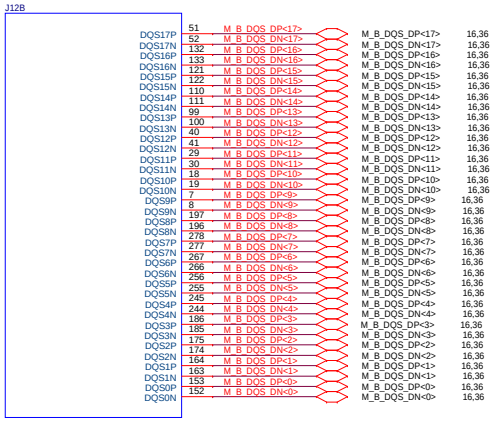

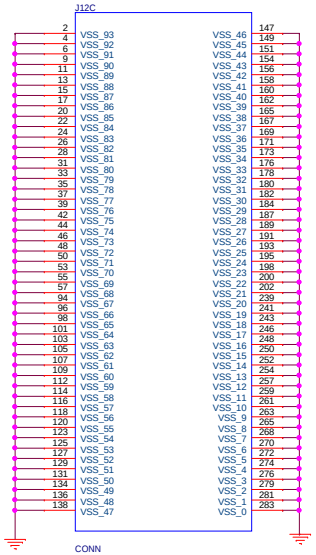

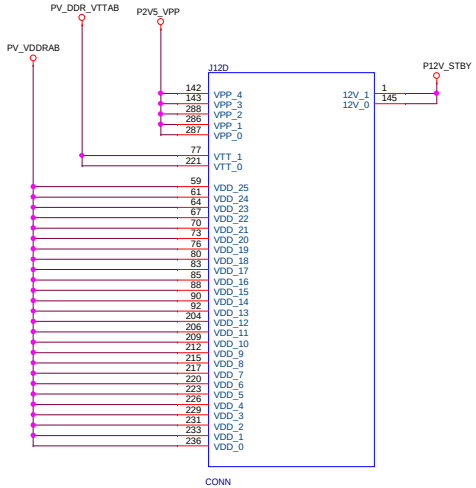

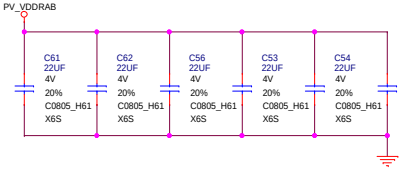

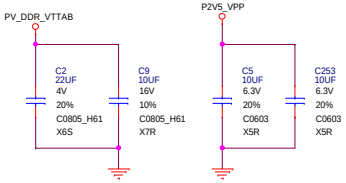

DDR4 RDIMM CHB_2

Quanta	Department: CCBU	Designer	Project: Mono Lake	Doc Number: <Doc> Rev: 0.0
		Reviewer	Page Title: DDR4 RDIMM CHB_2	
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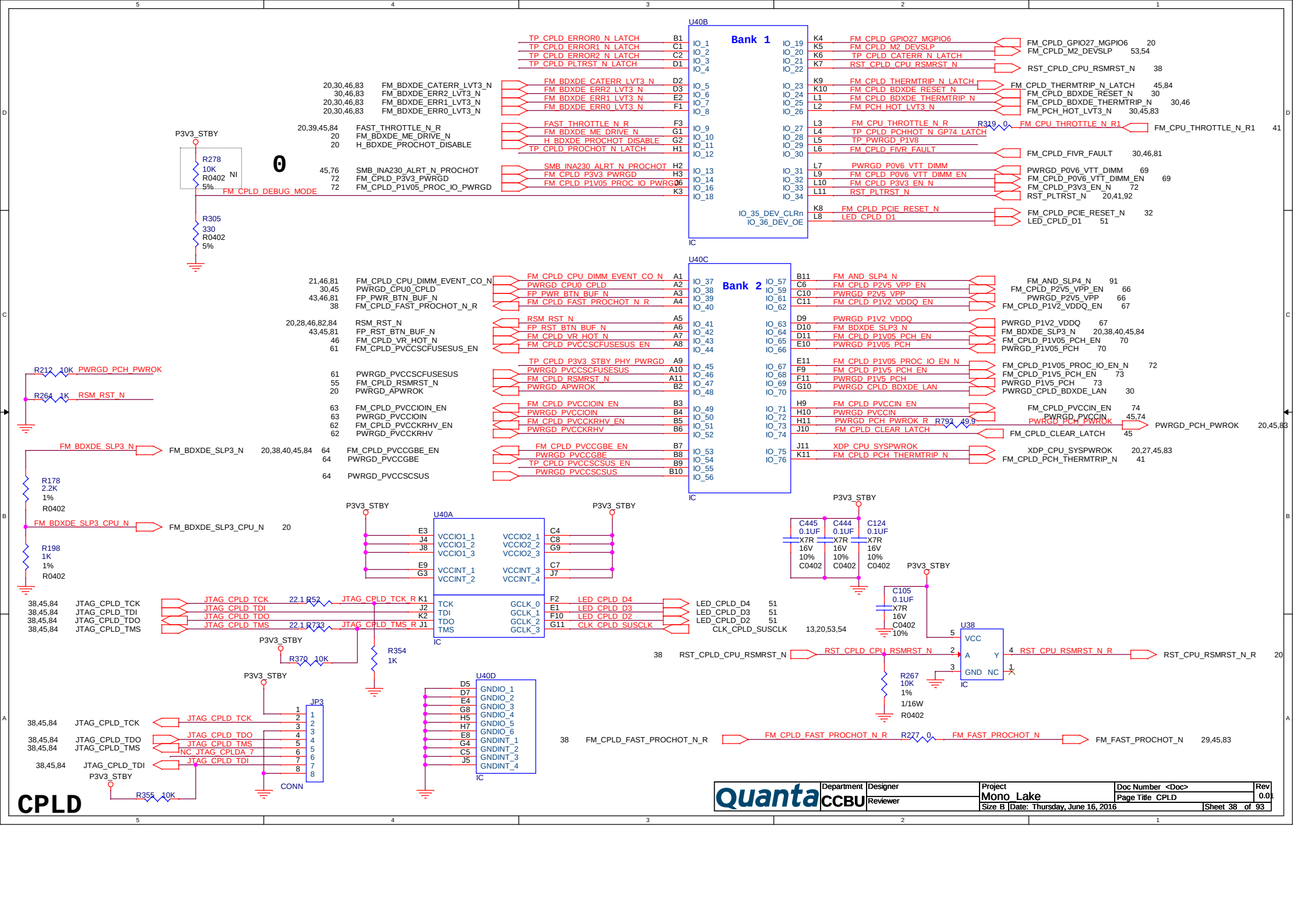
U40B
Bank 1
TP_CPLD_ERROR0_N_LATCH
TP_CPLD_ERROR1_N_LATCH
TP_CPLD_ERROR2_N_LATCH
TP_CPLD_PLTRST_N_LATCH
FM_BDXDE_CATERR_LVT3_N
FM_BDXDE_ERR2_LVT3_N
FM_BDXDE_ERR1_LVT3_N
FM_BDXDE_ERR0_LVT3_N
FAST_THROTTLE_N_R
FM_BDXDE_ME_DRIVE_N
H_BDXDE_PROCHOT_DISABLE
TP_CPLD_PROCHOT_N_LATCH
SMB_INA230_ALRT_N_PROCHOT
FM_CPLD_P3V3_PWRGD
FM_CPLD_P1V05_PROC_IO_PWRGD
FM_CPLD_GPIO27_MGPIO6
FM_CPLD_M2_DEVSLP
TP_CPLD_CATERR_N_LATCH
RST_CPLD_CPU_RSMRST_N
FM_CPLD_THERMTRIP_N_LATCH
FM_CPLD_BDXDE_RESET_N
FM_CPLD_BDXDE_THERMTRIP_N
FM_PCH_HOT_LVT3_N
FM_CPU_THROTTLE_N_R
TP_CPLD_PCHHOT_N_GP74_LATCH
TP_PWRGD_P1V8
FM_CPLD_FIVR_FAULT
PWRGD_P0V6_VTT_DIMM
FM_CPLD_P0V6_VTT_DIMM_EN
FM_CPLD_P3V3_EN_N
RST_PLTRST_N
FM_CPLD_PCIE_RESET_N
LED_CPLD_D1
IO_35_DEV_CLRn
IO_36_DEV_OE
IC
P3V3_STBY
R278
10K
R0402
NI
5%
0
FM_CPLD_DEBUG_MODE
R305
330
R0402
5%
R319 0
FM_CPU_THROTTLE_N_R1
U40C
Bank 2
FM_CPLD_CPU_DIMM_EVENT_CO_N
PWRGD_CPU0_CPLD
FP_PWR_BTN_BUF_N
FM_CPLD_FAST_PROCHOT_N_R
RSM_RST_N
FP_RST_BTN_BUF_N
FM_CPLD_VR_HOT_N
FM_CPLD_PVCCSCFUSESUS_EN
TP_CPLD_P3V3_STBY_PHY_PWRGD
PWRGD_PVCCSCFUSESUS
FM_CPLD_RSMRST_N
PWRGD_APWROK
FM_CPLD_PVCCIOIN_EN
PWRGD_PVCCIOIN
FM_CPLD_PVCCKRHV_EN
PWRGD_PVCCKRHV
FM_CPLD_PVCCGBE_EN
PWRGD_PVCCGBE
TP_CPLD_PVCCSCSUS_EN
PWRGD_PVCCSCSUS
FM_AND_SLP4_N
FM_CPLD_P2V5_VPP_EN
PWRGD_P2V5_VPP
FM_CPLD_P1V2_VDDQ_EN
PWRGD_P1V2_VDDQ
FM_BDXDE_SLP3_N
FM_CPLD_P1V05_PCH_EN
PWRGD_P1V05_PCH
FM_CPLD_P1V05_PROC_IO_EN_N
FM_CPLD_P1V5_PCH_EN
PWRGD_CPLD_BDXDE_LAN
FM_CPLD_PVCCIN_EN
PWRGD_PVCCIN
PWRGD_PCH_PWROK
R793 49.9
FM_CPLD_CLEAR_LATCH
XDP_CPU_SYSPWROK
FM_CPLD_PCH_THERMTRIP_N
IC
R212 10K PWRGD_PCH_PWROK
R264 1K RSM_RST_N
FM_BDXDE_SLP3_N
R178
2.2K
1%
R0402
FM_BDXDE_SLP3_CPU_N
R198
1K
1%
R0402
U40A
VCCIO1_1
VCCIO1_2
VCCIO1_3
VCCINT_1
VCCINT_2
VCCIO2_1
VCCIO2_2
VCCIO2_3
VCCINT_3
VCCINT_4
TCK
TDI
TDO
TMS
GCLK_0
GCLK_1
GCLK_2
GCLK_3
JTAG_CPLD_TCK
JTAG_CPLD_TDI
JTAG_CPLD_TDO
JTAG_CPLD_TMS
JTAG_CPLD_TCK_R
JTAG_CPLD_TMS_R
22.1 R52
22.1 R733
LED_CPLD_D4
LED_CPLD_D3
LED_CPLD_D2
CLK_CPLD_SUSCLK
C445 0.1UF X7R 16V 10% C0402
C444 0.1UF X7R 16V 10% C0402
C124 0.1UF X7R 16V 10% C0402
C105 0.1UF X7R 16V 10% C0402
U38
VCC
A
Y
GND
NC
RST_CPLD_CPU_RSMRST_N
RST_CPU_RSMRST_N_R
R267 10K 1% 1/16W R0402
R370 10K
R354 1K
JP3
CONN
U40D
GNDIO_1
GNDIO_2
GNDIO_3
GNDIO_4
GNDIO_5
GNDIO_6
GNDINT_1
GNDINT_2
GNDINT_3
GNDINT_4
R355 10K
FM_CPLD_FAST_PROCHOT_N_R
R277 0
FM_FAST_PROCHOT_N
CPLD
Quanta
Department CCBU
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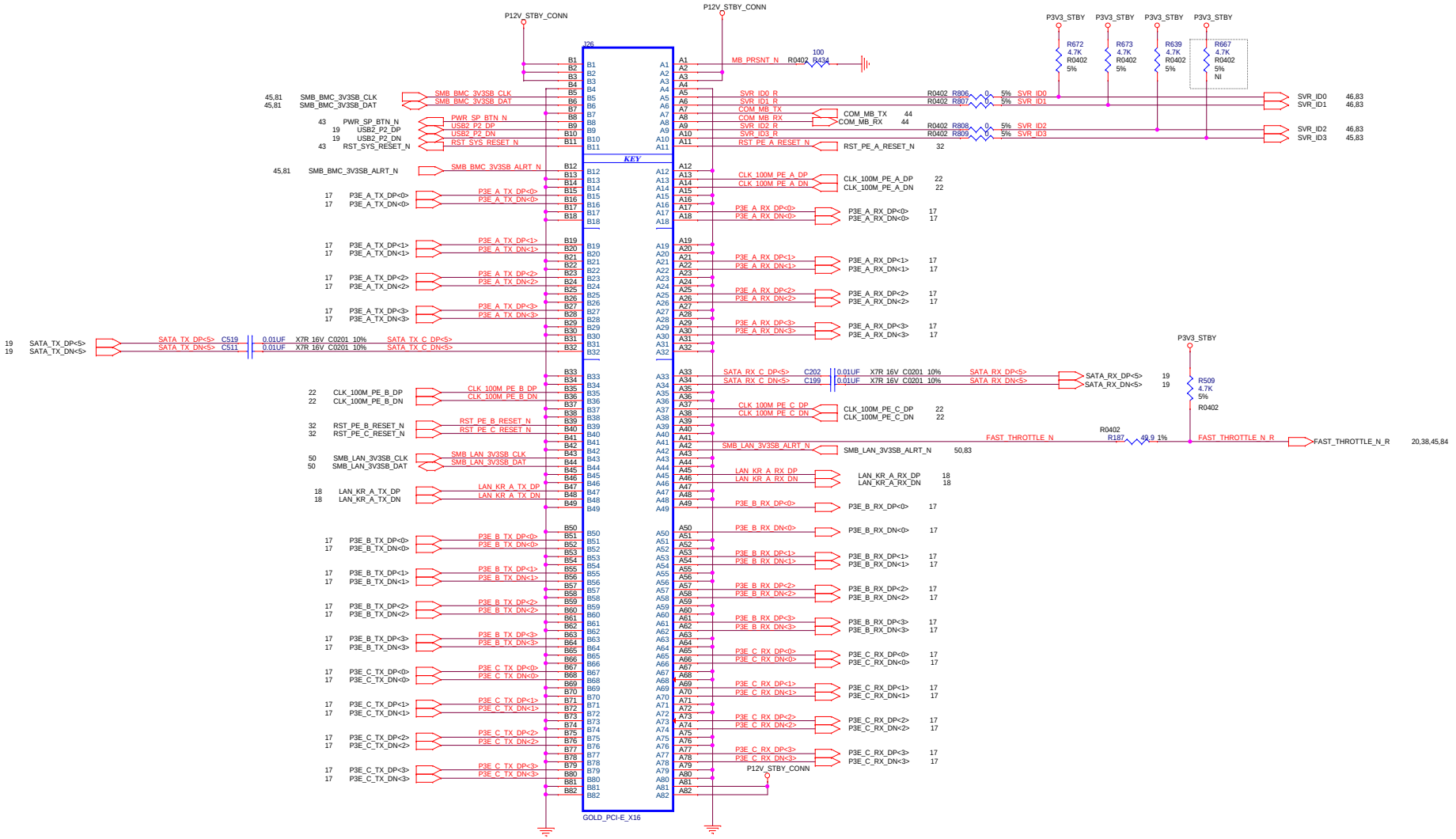

GOLD_FINGER_PRIMARY

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		Reviewer	Page Title GOLD_FINGER_PRIMARY	
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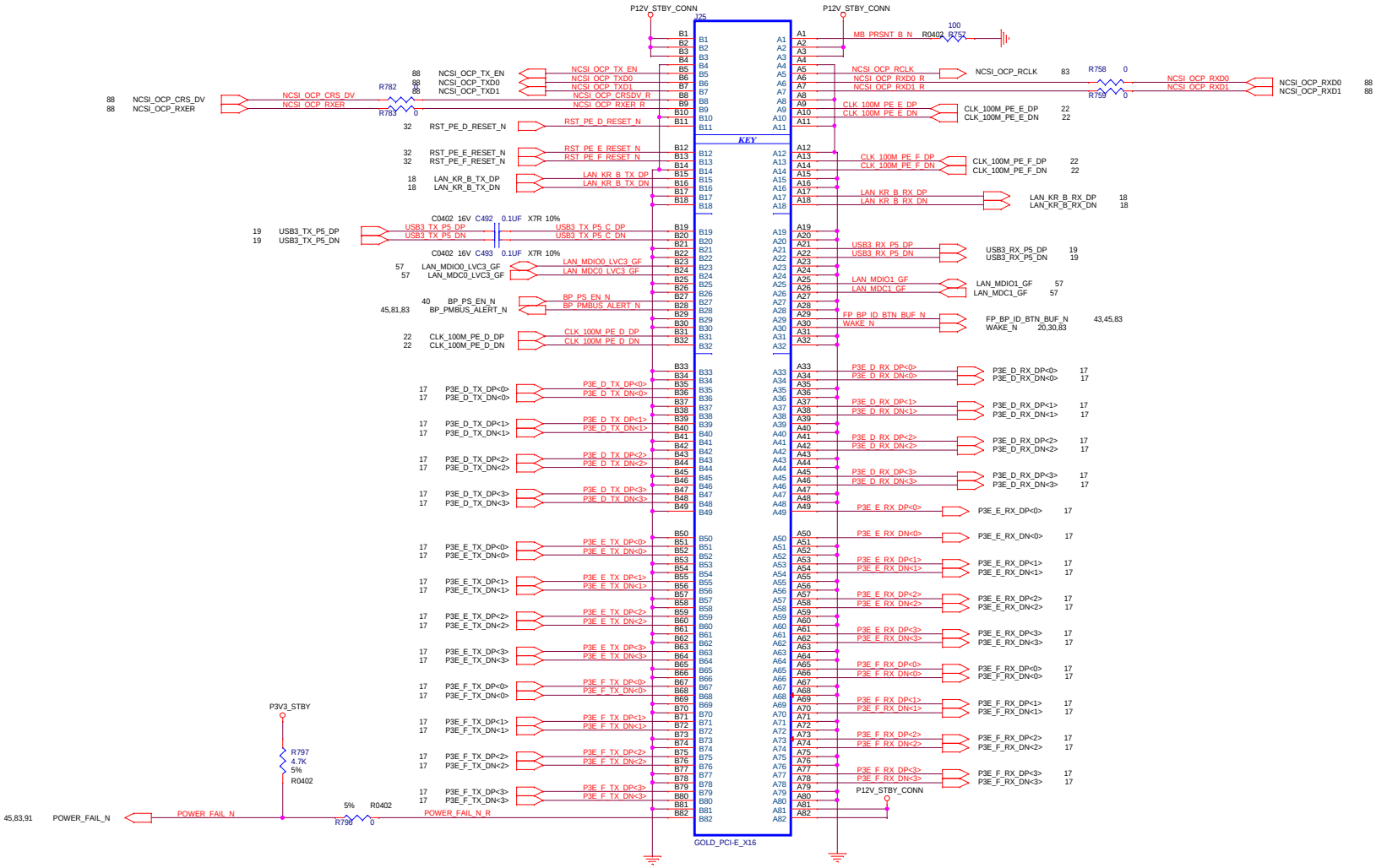

GOLD_FINGER_EXTENSION

Quanta	Department: CCBU	Designer:	Project: Mono_Lake	Doc Number: <Doc> Rev: 0.01
		Reviewer:		Page Title: GOLD_FINGER_EXTENSION
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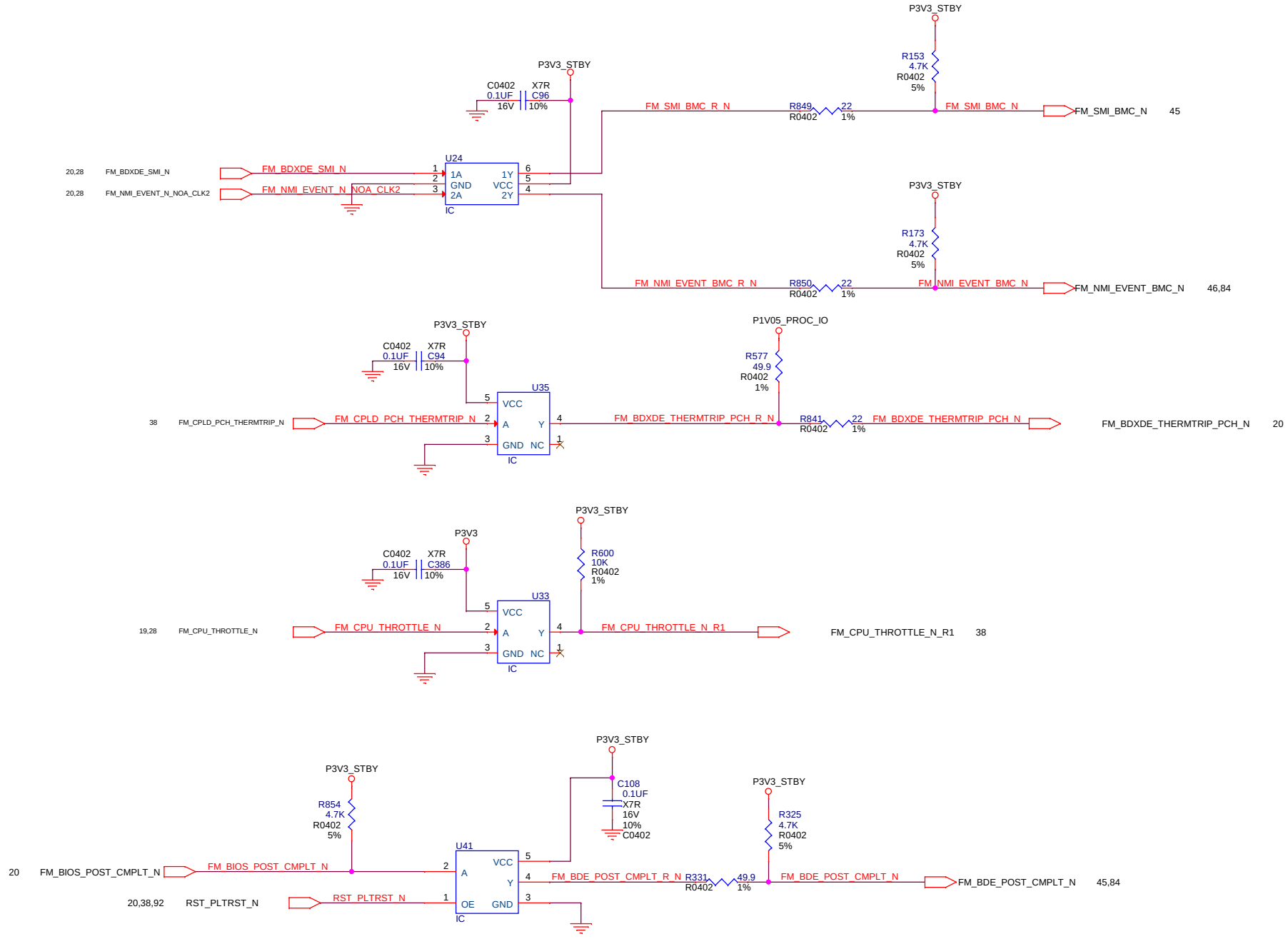

LEVEL_SHIFT

Quanta	Department CCBU	Designer	Project Mono_Lake	Doc Number <Doc>	Rev 0.01
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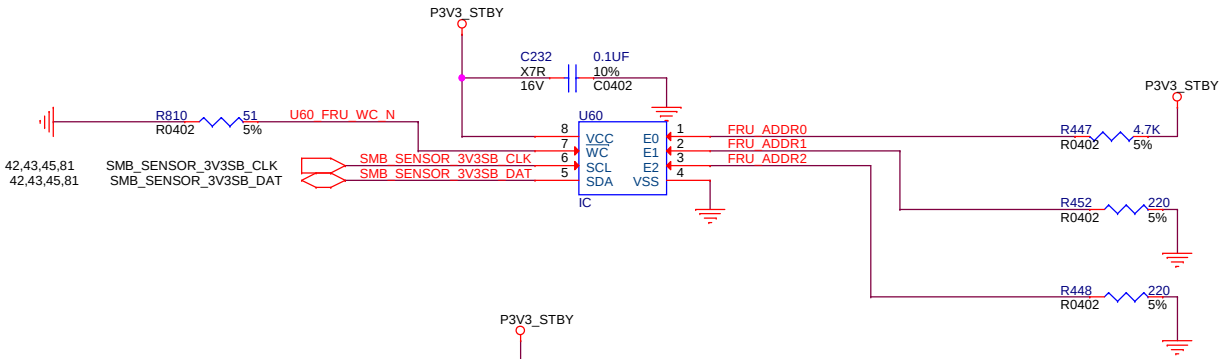
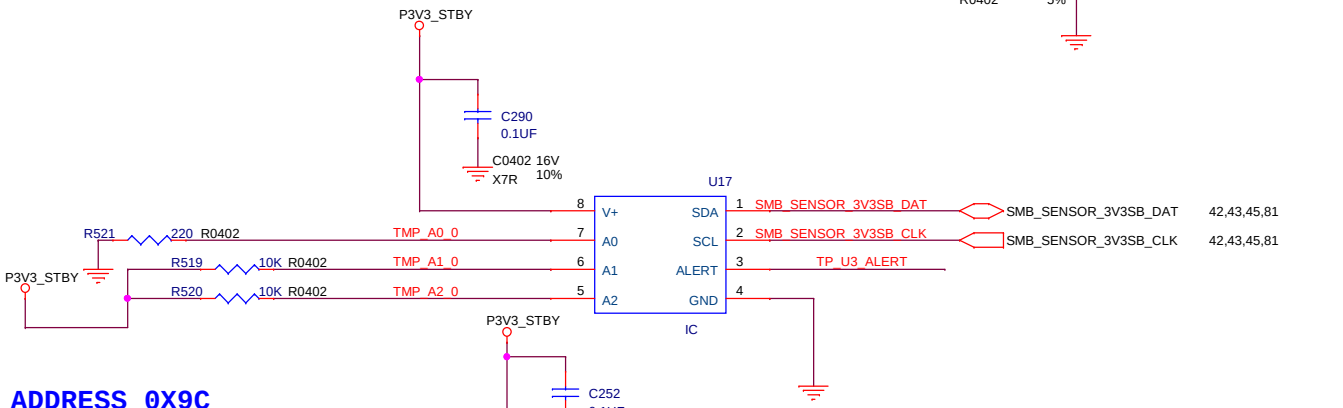
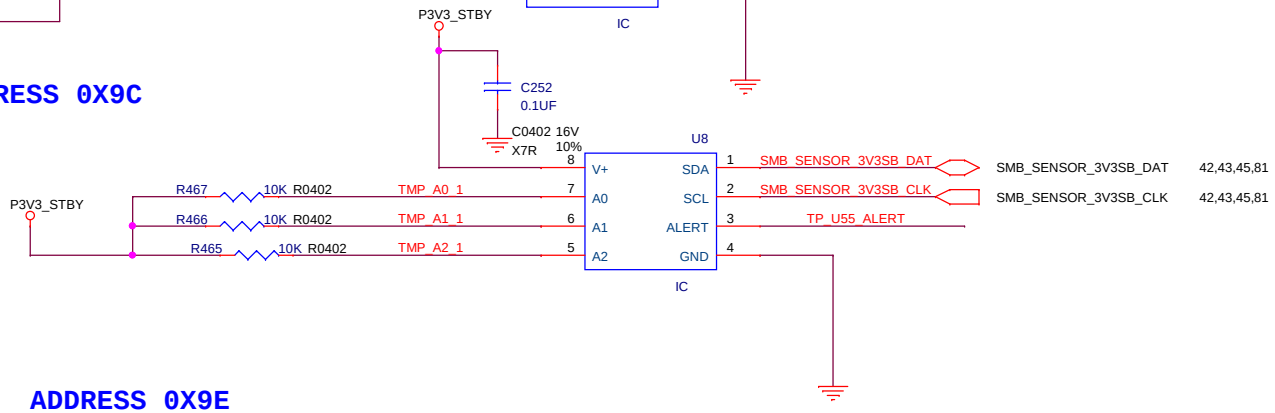
SMBus (8-bit) Address:0xA2

FRU





ADDRESS 0X9C



ADDRESS 0X9E

SYS_SENSOR

Quanta	Department CCBU	Designer	Project Mono_Lake	Doc Number <Doc>	Rev 0.01
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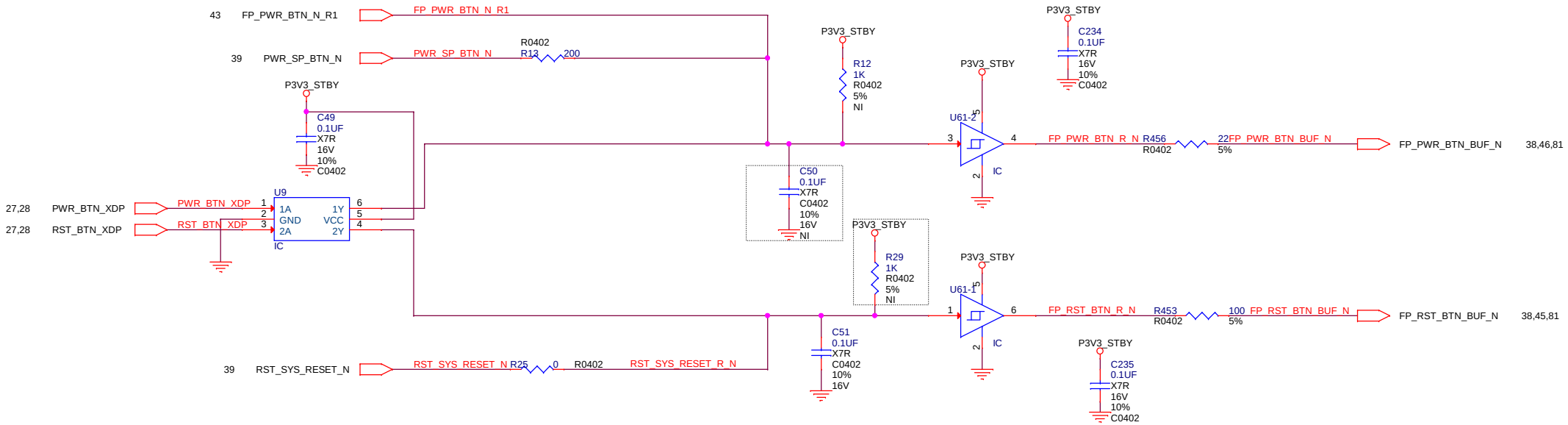

Front panel connector

Quanta	Department CCBU	Designer	Project Mono_Lake	Doc Number <Doc>	Rev 0.01
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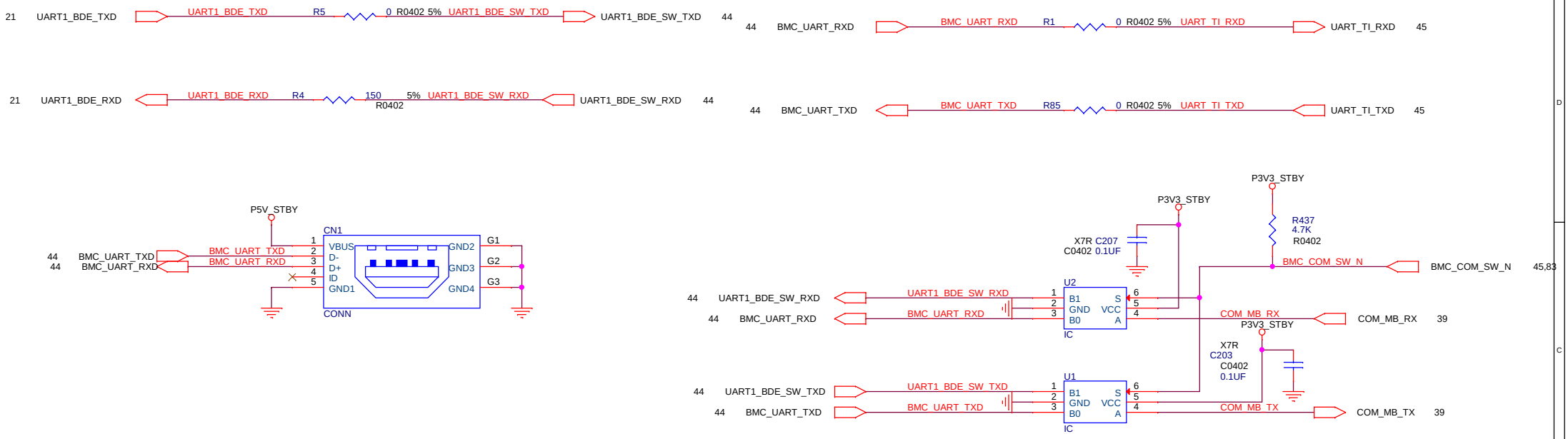

Debug UART

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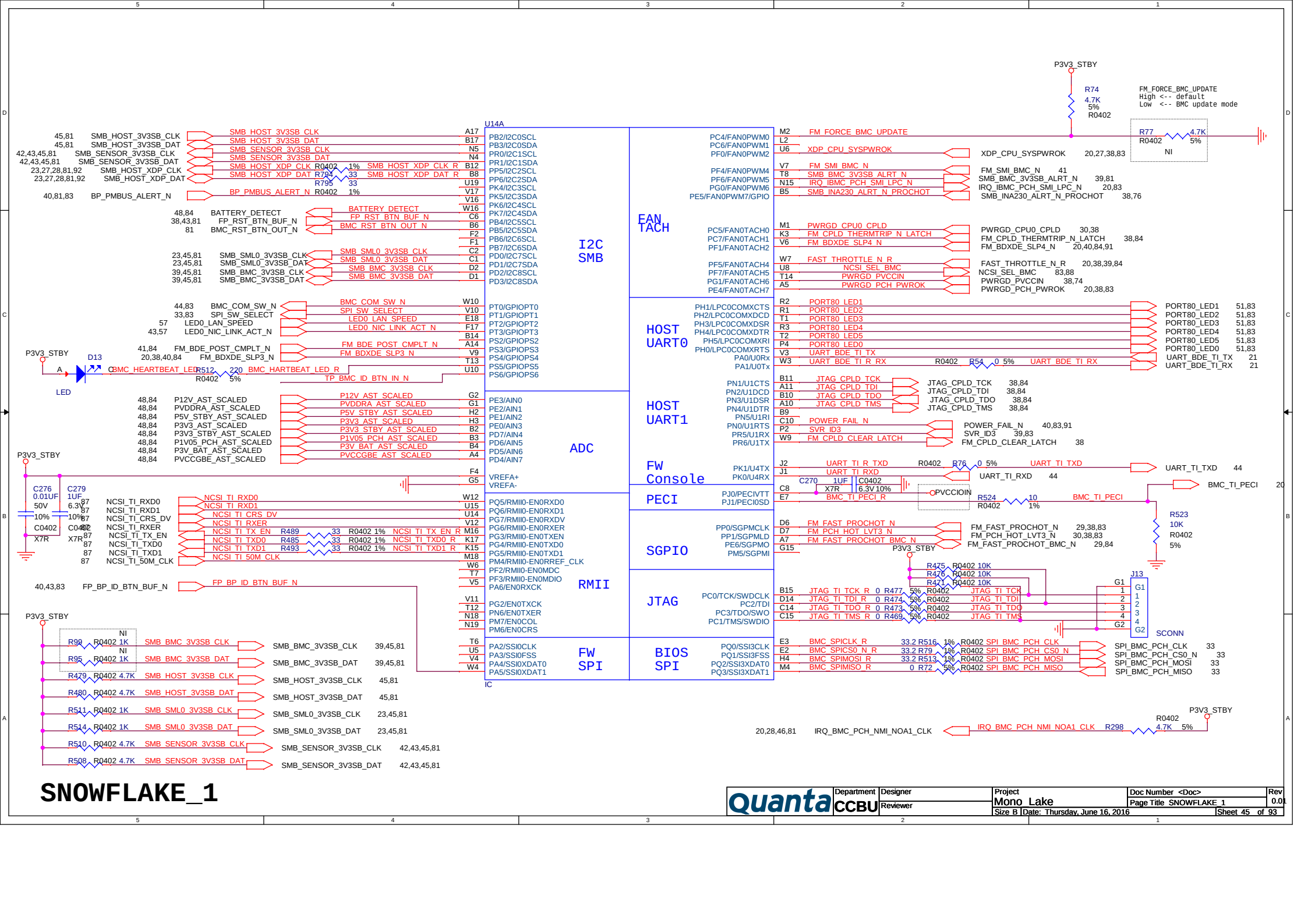
U14A
I2C SMB
FAN TACH
HOST UART0
HOST UART1
FW Console
PECI
SGPIO
JTAG
BIOS SPI
ADC
RMII
FW SPI
IC
P3V3_STBY
SMB_HOST_3V3SB_CLK
SMB_HOST_3V3SB_DAT
SMB_SENSOR_3V3SB_CLK
SMB_SENSOR_3V3SB_DAT
SMB_HOST_XDP_CLK
SMB_HOST_XDP_DAT
BP_PMBUS_ALERT_N
BATTERY_DETECT
FP_RST_BTN_BUF_N
BMC_RST_BTN_OUT_N
SMB_SML0_3V3SB_CLK
SMB_SML0_3V3SB_DAT
SMB_BMC_3V3SB_CLK
SMB_BMC_3V3SB_DAT
BMC_COM_SW_N
SPI_SW_SELECT
LED0_LAN_SPEED
LED0_NIC_LINK_ACT_N
FM_BDE_POST_CMPLT_N
FM_BDXDE_SLP3_N
BMC_HEARTBEAT_LED
TP_BMC_ID_BTN_IN_N
P12V_AST_SCALED
PVDDRA_AST_SCALED
P5V_STBY_AST_SCALED
P3V3_AST_SCALED
P3V3_STBY_AST_SCALED
P1V05_PCH_AST_SCALED
P3V_BAT_AST_SCALED
PVCCGBE_AST_SCALED
NCSI_TI_RXD0
NCSI_TI_RXD1
NCSI_TI_CRS_DV
NCSI_TI_RXER
NCSI_TI_TX_EN
NCSI_TI_TXD0
NCSI_TI_TXD1
NCSI_TI_50M_CLK
FP_BP_ID_BTN_BUF_N
FM_FORCE_BMC_UPDATE
XDP_CPU_SYSPWROK
FM_SMI_BMC_N
SMB_BMC_3V3SB_ALRT_N
IRQ_IBMC_PCH_SMI_LPC_N
SMB_INA230_ALRT_N_PROCHOT
PWRGD_CPU0_CPLD
FM_CPLD_THERMTRIP_N_LATCH
FM_BDXDE_SLP4_N
FAST_THROTTLE_N_R
NCSI_SEL_BMC
PWRGD_PVCCIN
PWRGD_PCH_PWROK
PORT80_LED1
PORT80_LED2
PORT80_LED3
PORT80_LED4
PORT80_LED5
PORT80_LED0
UART_BDE_TI_TX
UART_BDE_TI_RX
JTAG_CPLD_TCK
JTAG_CPLD_TDI
JTAG_CPLD_TDO
JTAG_CPLD_TMS
POWER_FAIL_N
SVR_ID3
FM_CPLD_CLEAR_LATCH
UART_TI_R_TXD
UART_TI_RXD
BMC_TI_PECI
PVCCIOIN
FM_FAST_PROCHOT_N
FM_PCH_HOT_LVT3_N
FM_FAST_PROCHOT_BMC_N
JTAG_TI_TCK_R
JTAG_TI_TDI_R
JTAG_TI_TDO_R
JTAG_TI_TMS_R
SCONN
BMC_SPICLK_R
BMC_SPICS0_N_R
BMC_SPIMOSI_R
BMC_SPIMISO_R
SPI_BMC_PCH_CLK
SPI_BMC_PCH_CS0_N
SPI_BMC_PCH_MOSI
SPI_BMC_PCH_MISO
IRQ_BMC_PCH_NMI_NOA1_CLK
SNOWFLAKE_1
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Designer
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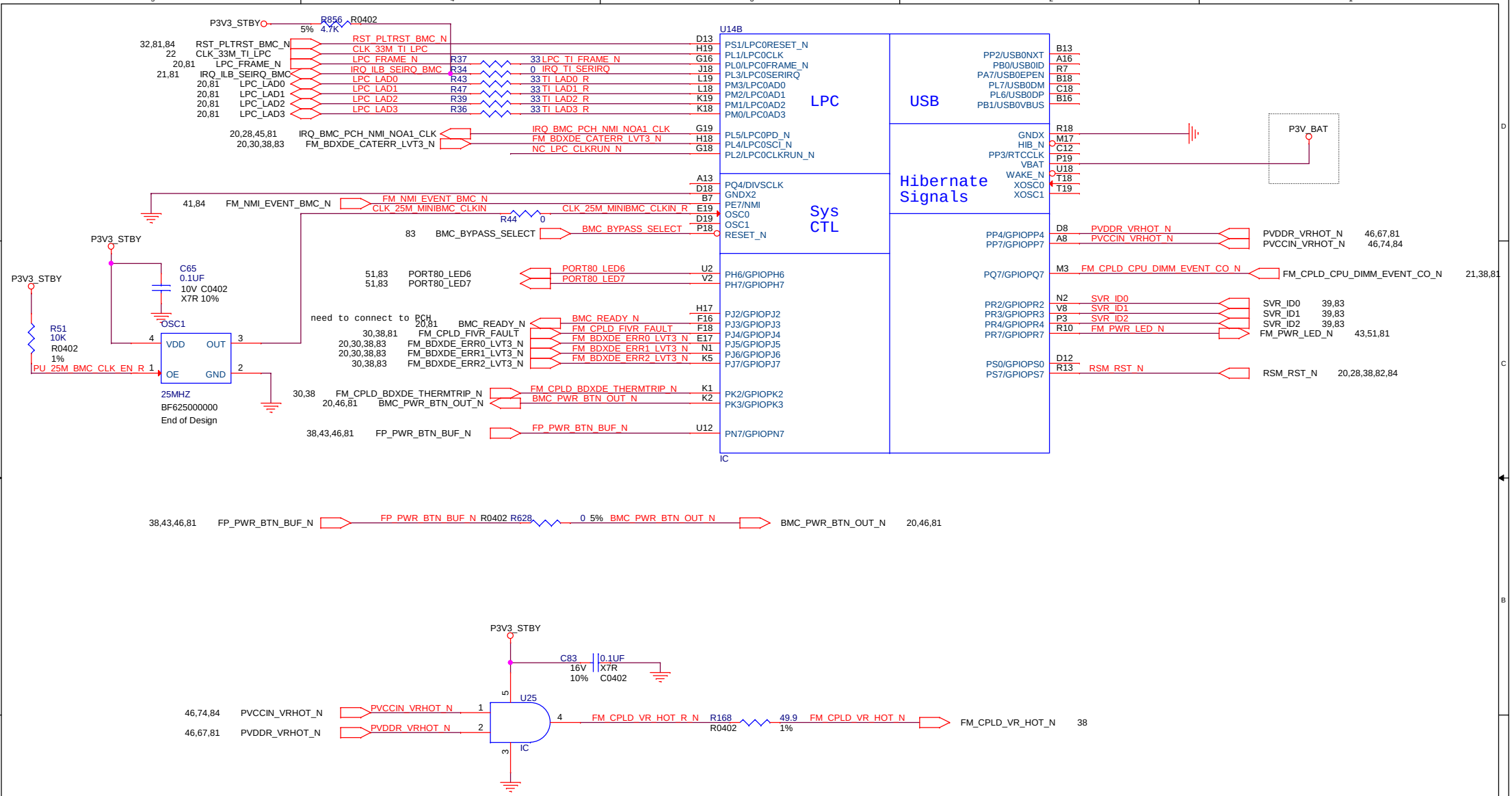

SNOWFLAKE_2

Quanta	Department CCBU	Designer	Project Mono_Lake	Doc Number <Doc> Rev 0.01
		Reviewer		Page Title SNOWFLAKE_2
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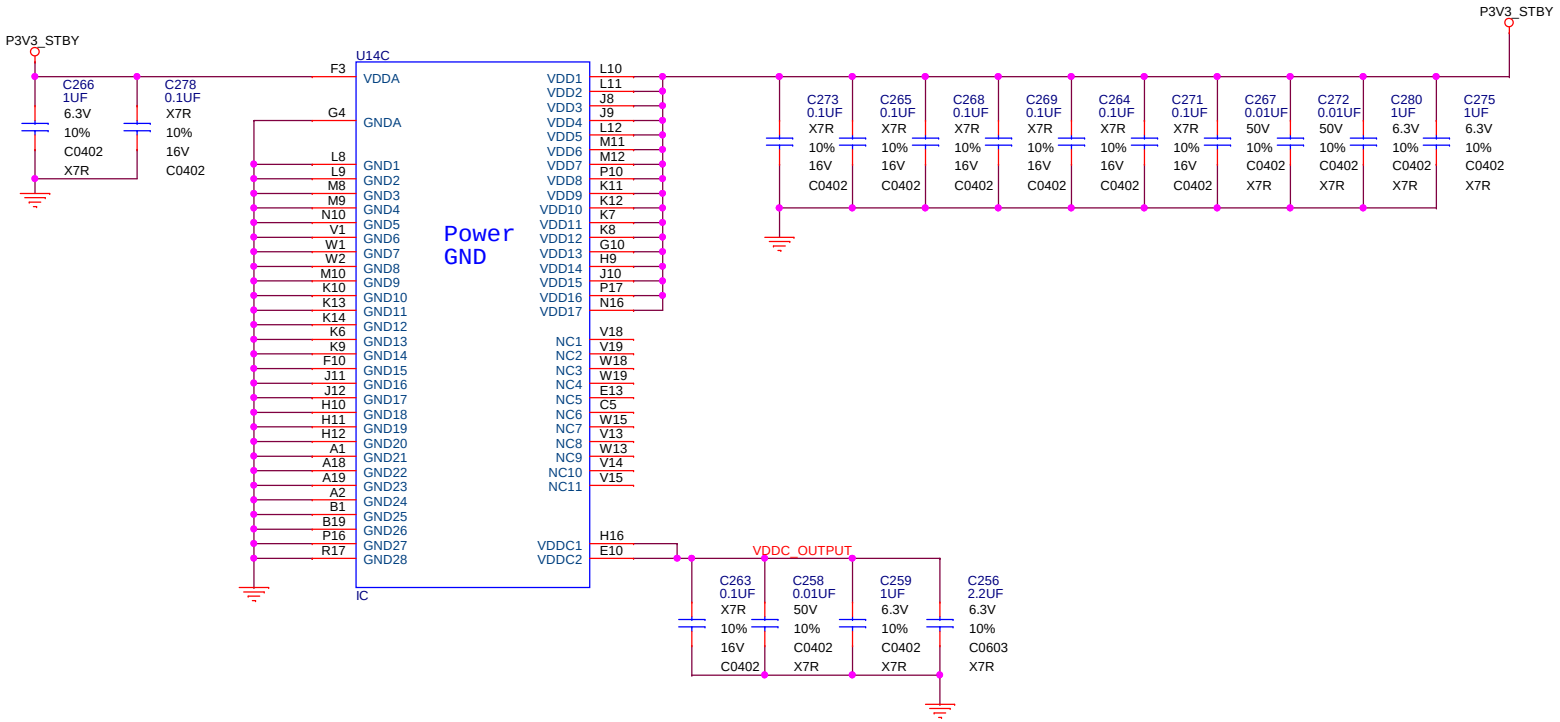
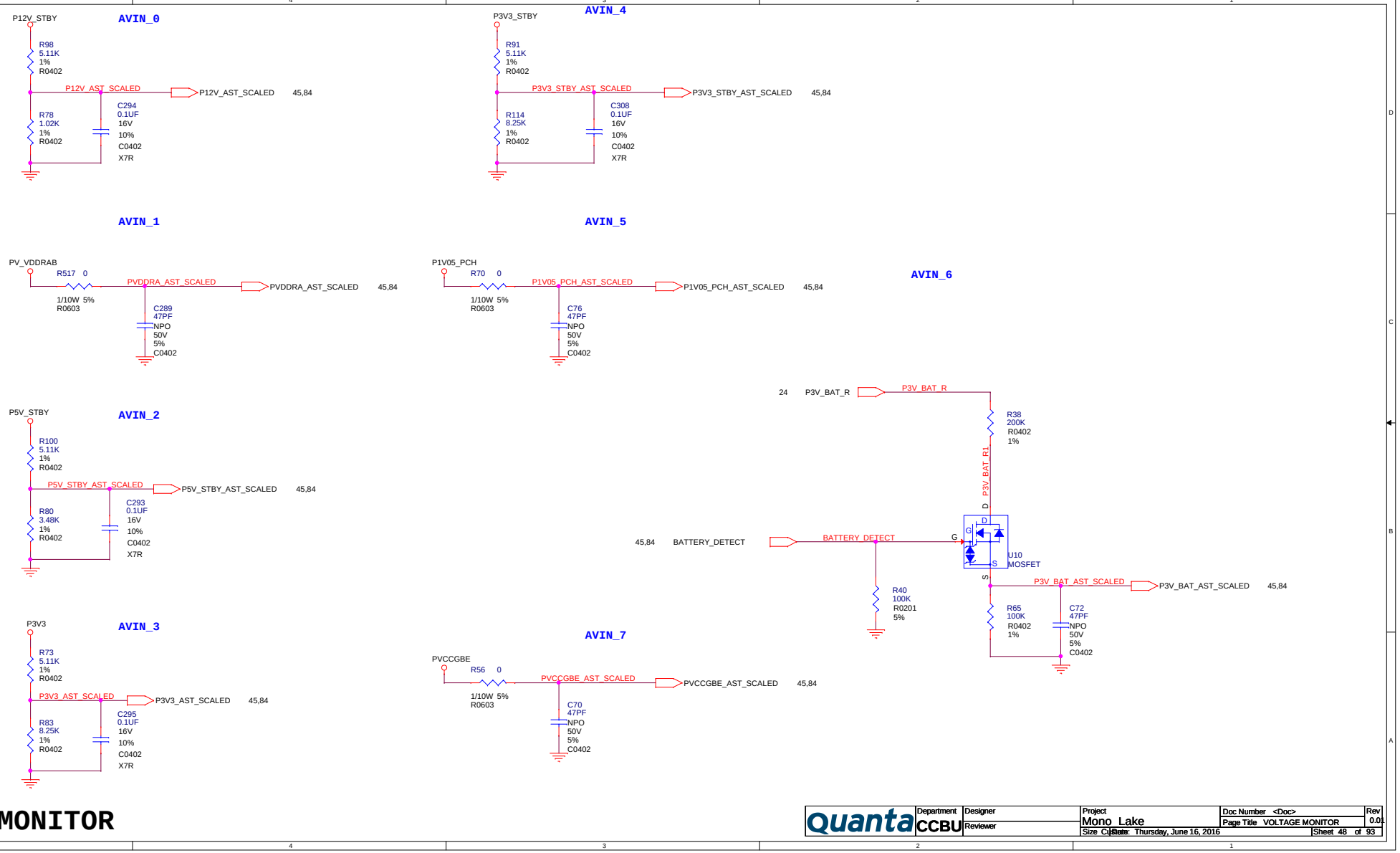


SNOWFLAKE_3

Quanta	Department CCBU	Designer	Project Mono_Lake	Doc Number <Doc>	Rev 0.01
		Reviewer		Page Title SNOWFLAKE_3	
			Size B Date: Thursday, June 16, 2016		Sheet 47 of 93



VOLTAGE MONITOR

Quanta	Department CCBU	Designer	Project Mono_Lake	Doc Number <Doc>	Rev 0.01
		Reviewer		Page Title VOLTAGE MONITOR	
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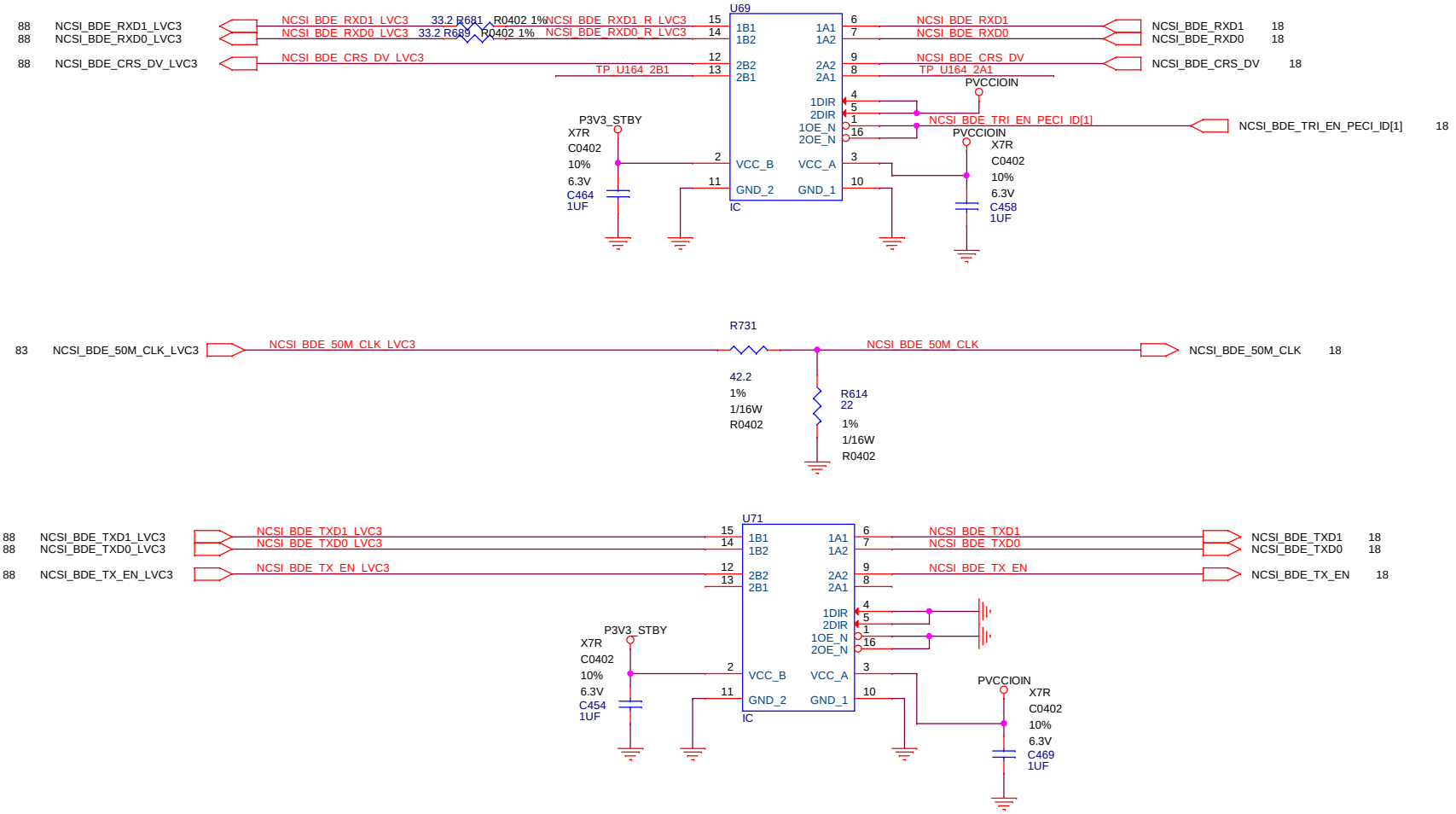

NCSI LEVEL SHIFT

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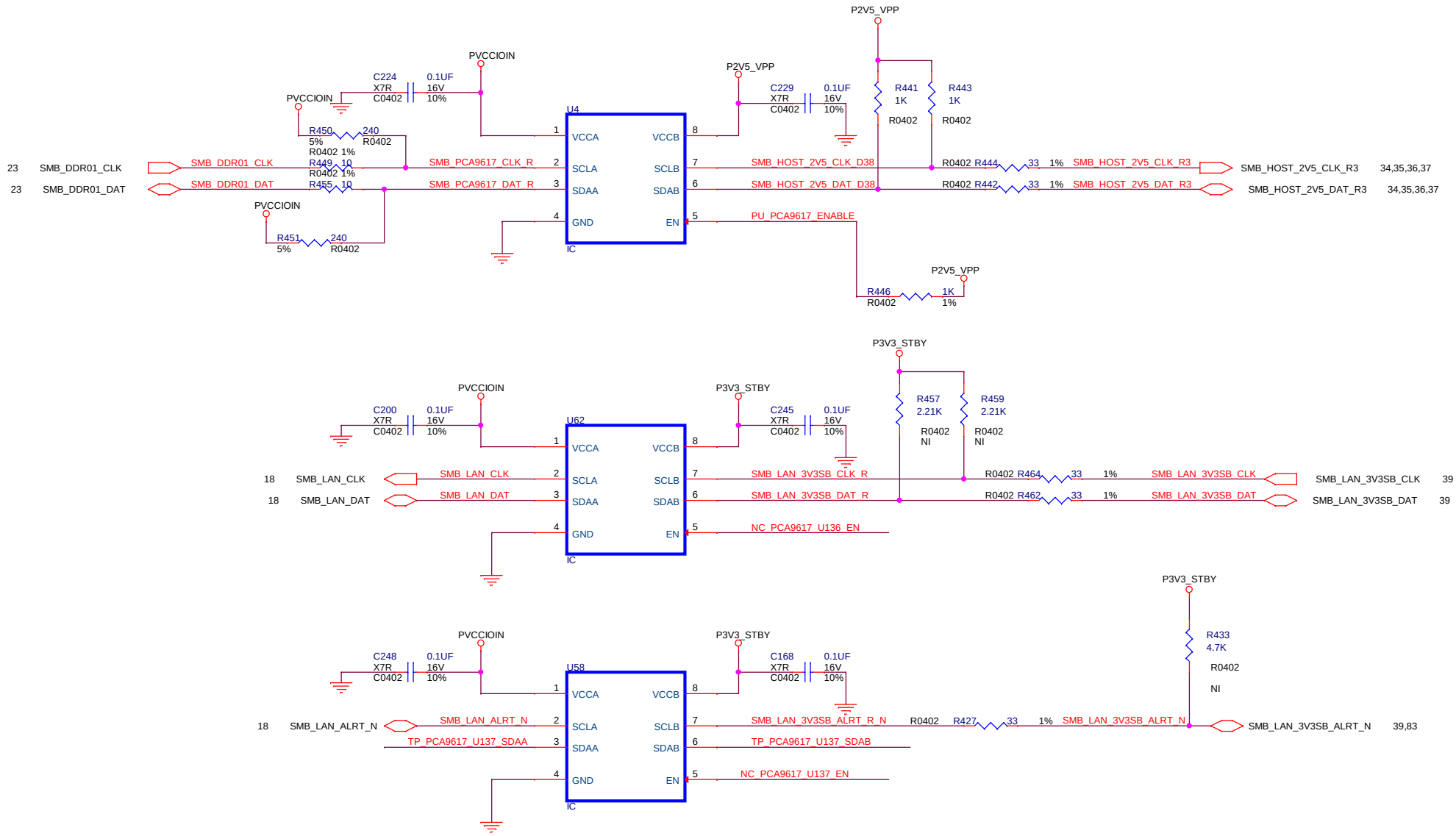
		Reviewer		Page Title NCSI LEVEL SHIFT	
			Size B	Date: Thursday, June 16, 2016	Sheet 49 of 93



SMBUS ISOLATOR

Quanta	Department CCBU	Designer	Project Mono_Lake	Doc Number <Doc>	Rev 0.01
		Reviewer		Page Title SMBUS ISOLATOR	
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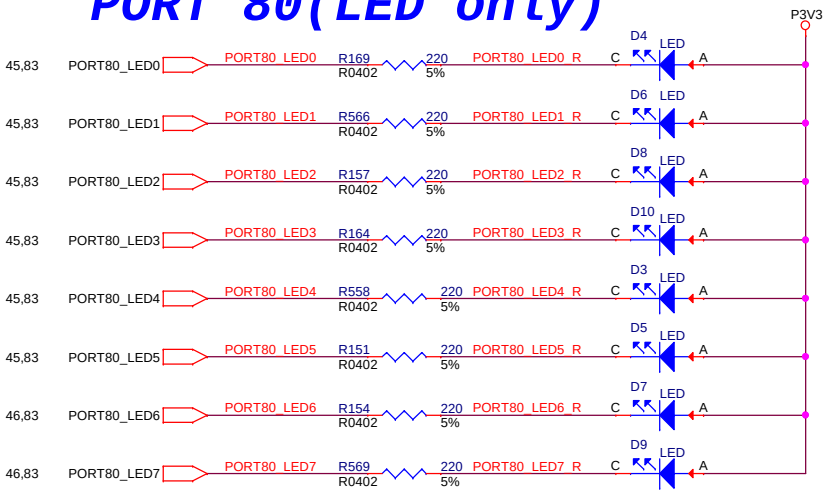
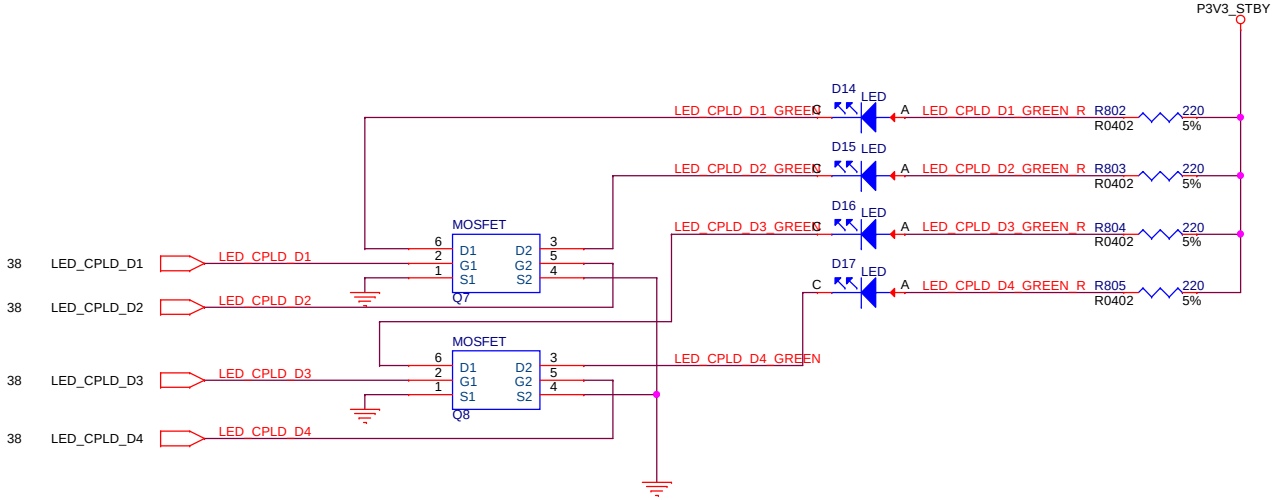
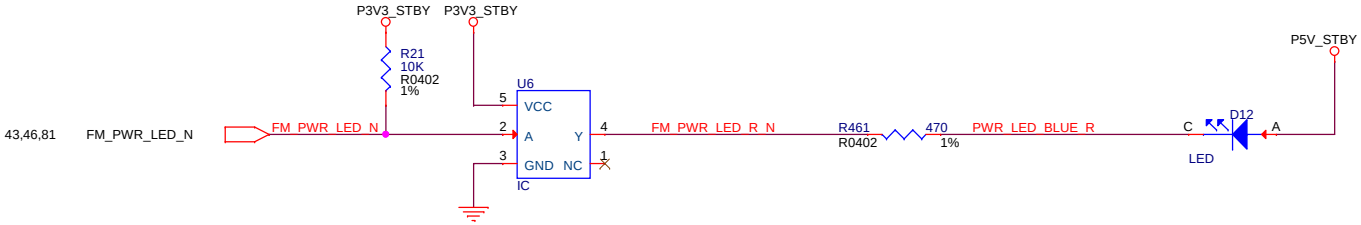
PORT 80(LED only)





POWER LED (BLUE)



PWR/ PORT 80 LED

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		Reviewer	Page Title PWR/ PORT 80 LED	
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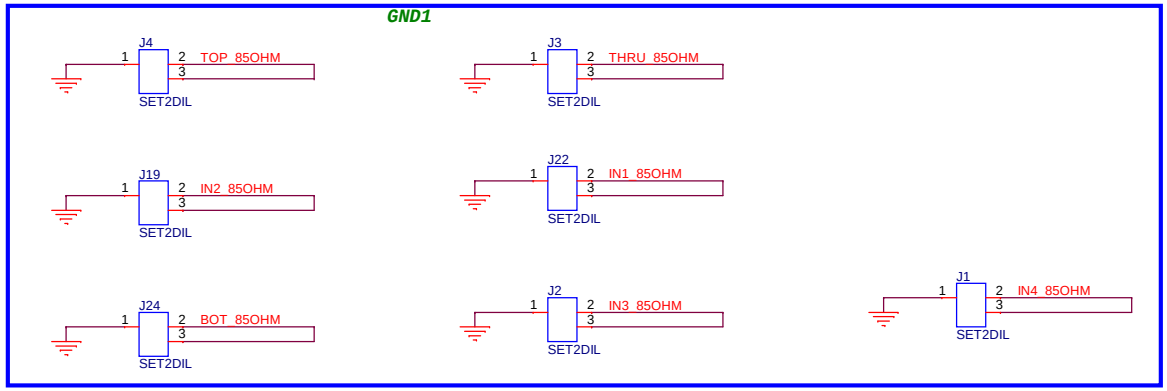
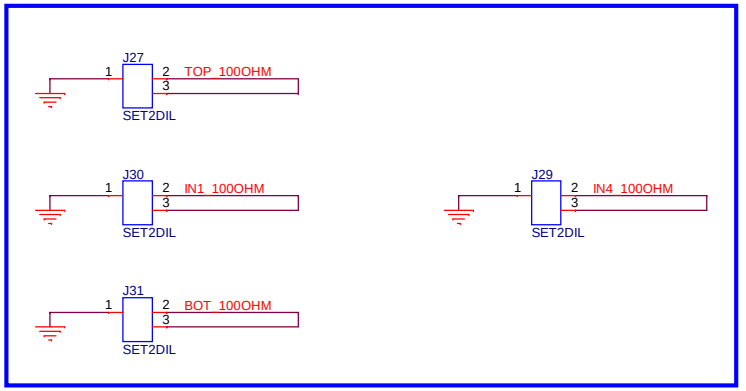
SET2DEL



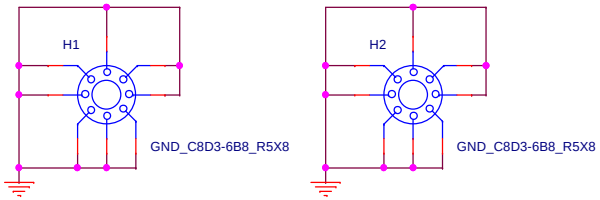


Screw Hole

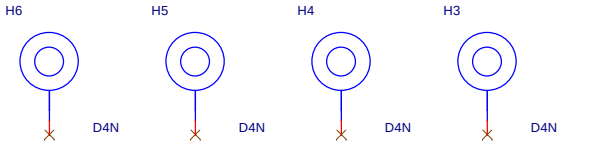
H7
HOLE_C6D3-4B6_NPB

For TPM module

1 TP_M2_LATCH EBF20010010
1 TP_HEAT_SINK1 FBF20016010
1 TP_CPU_BACKPLANE FBF20015010
1 TP_SCREW_1 MS06065I010
1 TP_SCREW_2 MS06065I010
1 TP_BATTERY_CABLE AHL03003058
1 TP_BIOS_LABEL AP0SERVER05
1 TP_JUMPER_1 DEJP0050103
1 TP_JUMPER_2 DEJP0050103
1 TP_SCREW_3 MS30040I009



GRIP



1 EBMF1007010

CE Logo

DM1
DUMMY_SYMBOL
CE_LOGO_5.8X5.08

NGFF HOLE

H9
HOLE3_C7D4-8B7_P4-6_NPB

SCREW/TP

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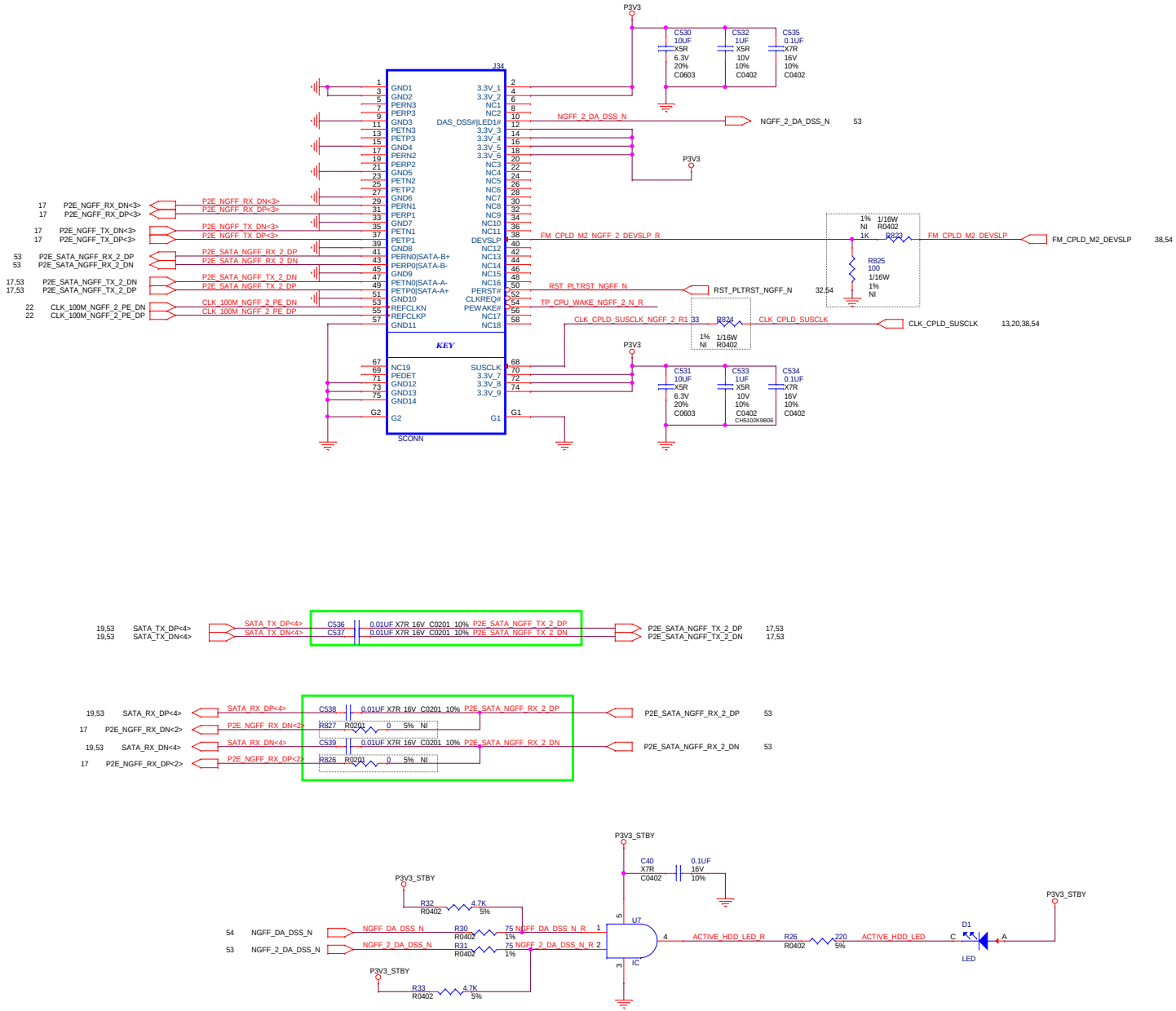

The 2nd M.2 CONN

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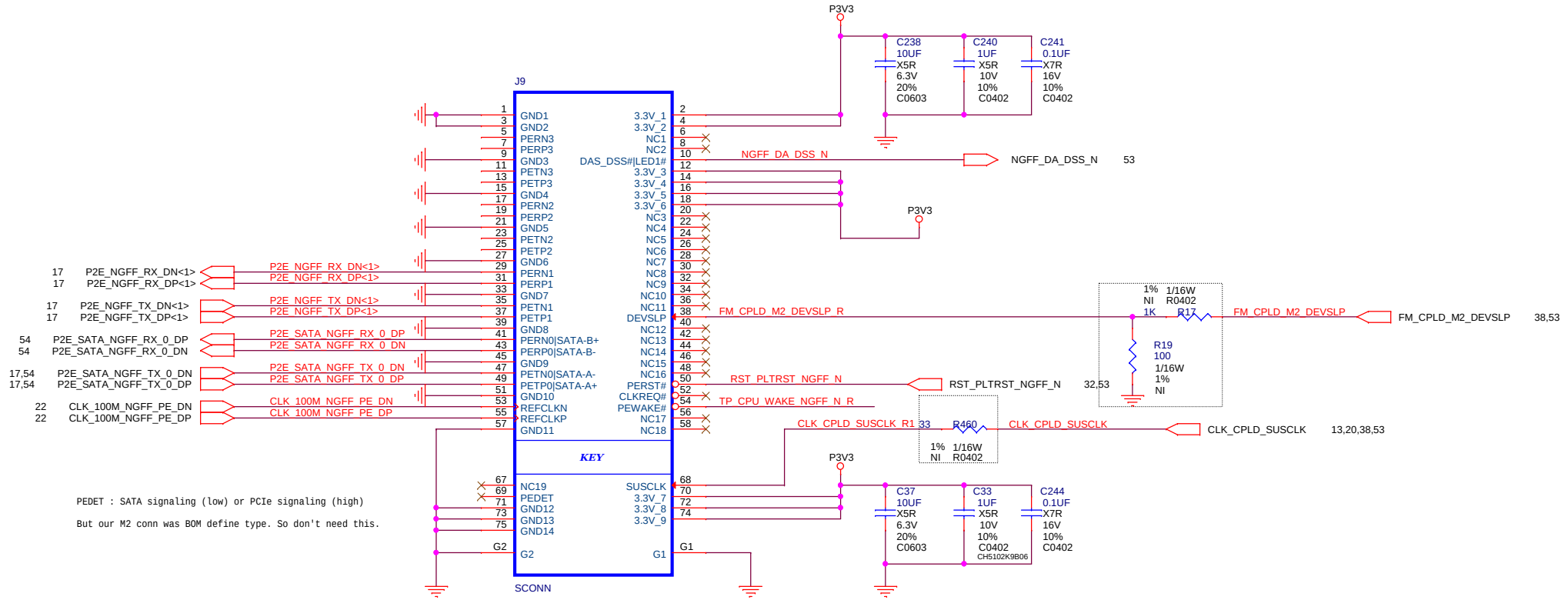

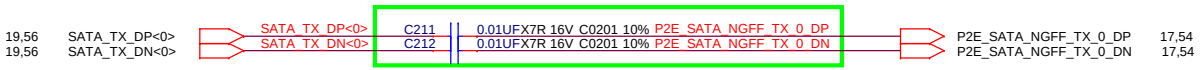

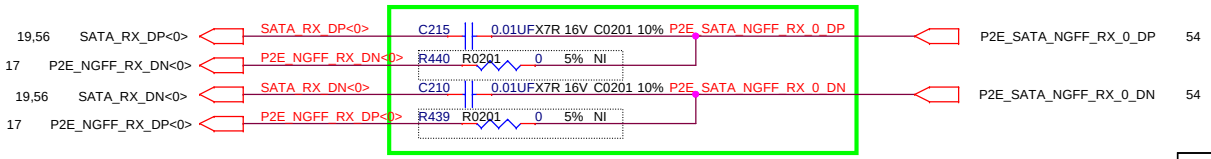

The 1st M.2 CONN

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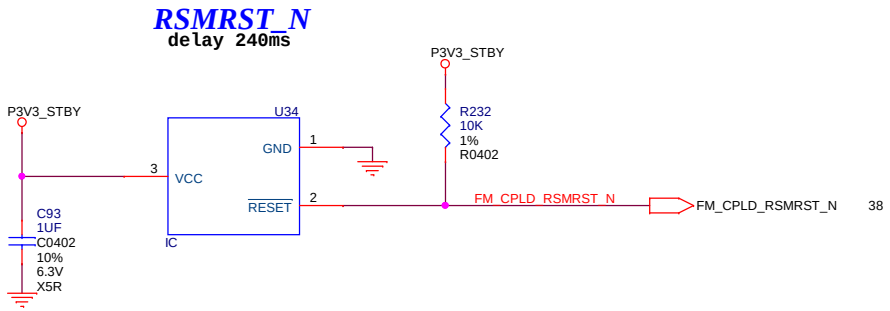
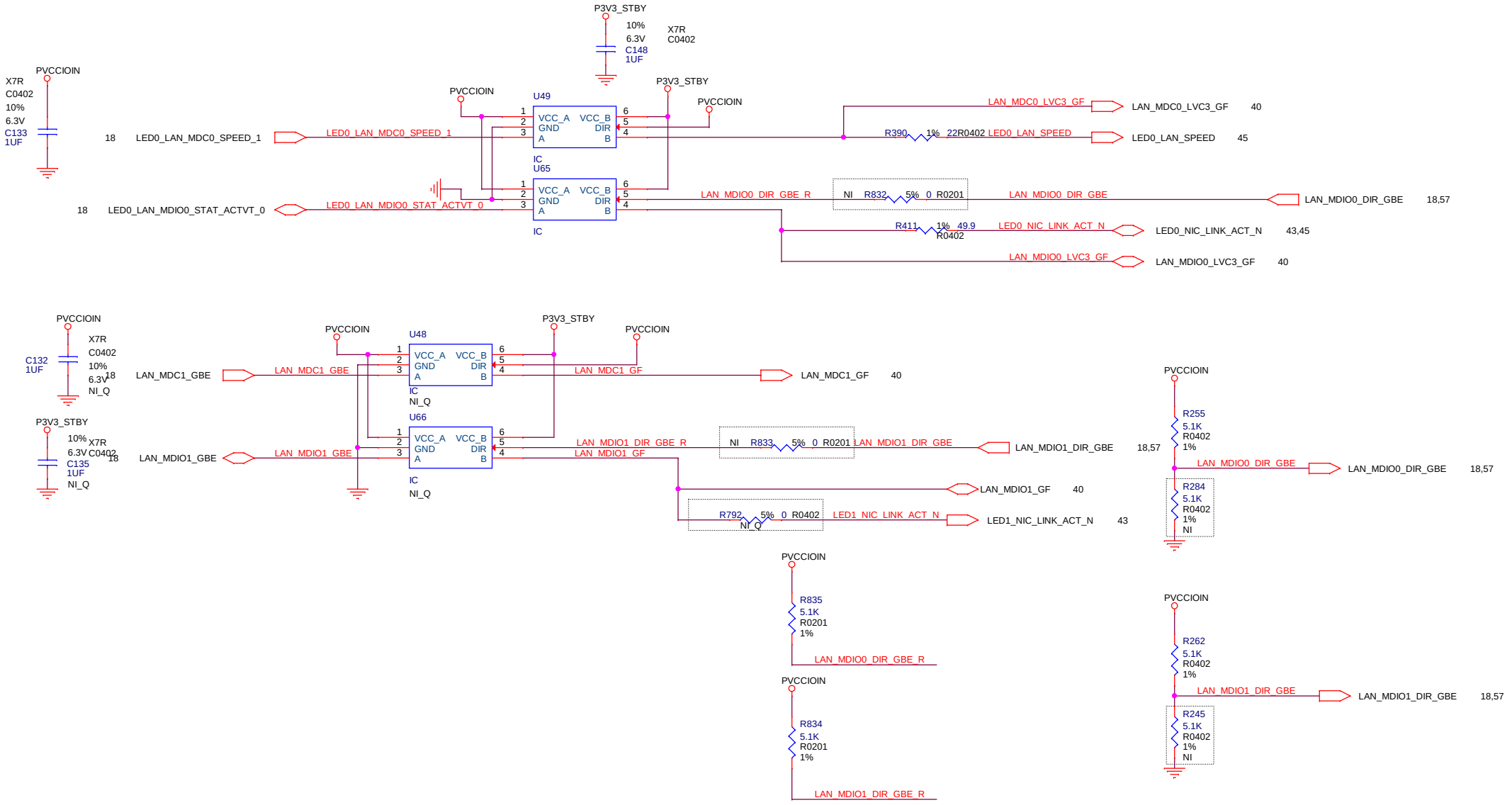


RSMRST

Quanta	Department CCBU	Designer	Project Mono_Lake	Doc Number <Doc>	Rev 0.01
		Reviewer		Page Title RSMRST	
			Size B Date: Thursday, June 16, 2016		Sheet 55 of 93



MDC/MDIO

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BLANK

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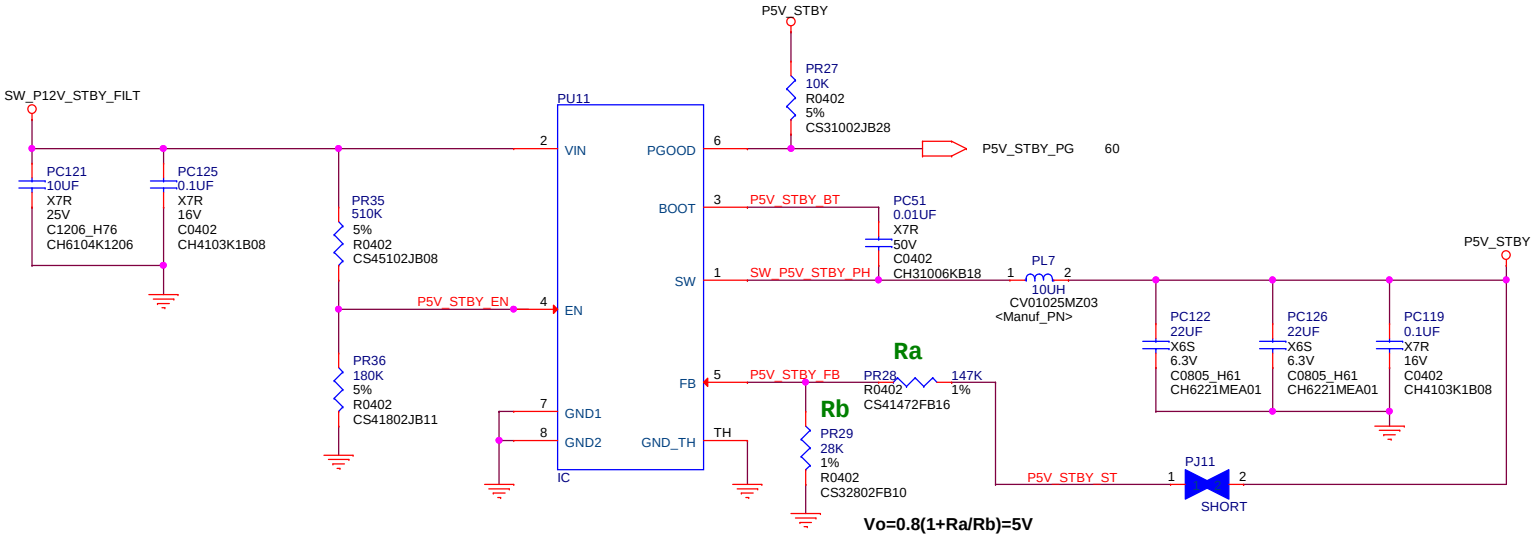
P5V_STBY Design specification

Output Voltage = 5V±5%
Output Ripple & Noise < 30mV
Transient Tolerance = 500mV
TDC = 0.15A
Max current =0.15A
Over-Current Protection(IC rating) = 1.5A
Slew Rate = 2.5A/us
Work Frequency = 800kHZ
Efficiency > 90% @TDC



P5V_STBY

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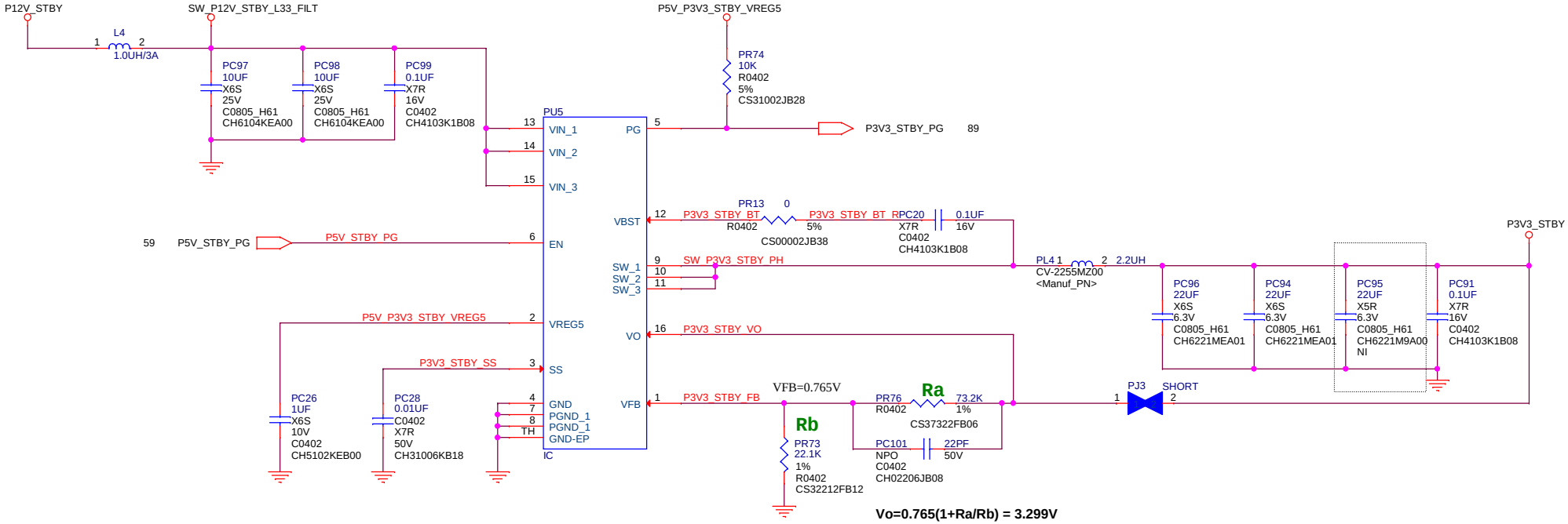
P3V3_STBY Design specification

Output Voltage = 3.3±5%
Output Ripple & Noise < 30mV
Transient Tolerance = 330mV
TDC = 5.16A
Max current = 5.16A
Over-Current Protection(IC rating) = 6.1A
Slew Rate = 2.5A/us
Work Frequency = 650kHZ
Efficiency > 90% @TDC



P3V3_STBY

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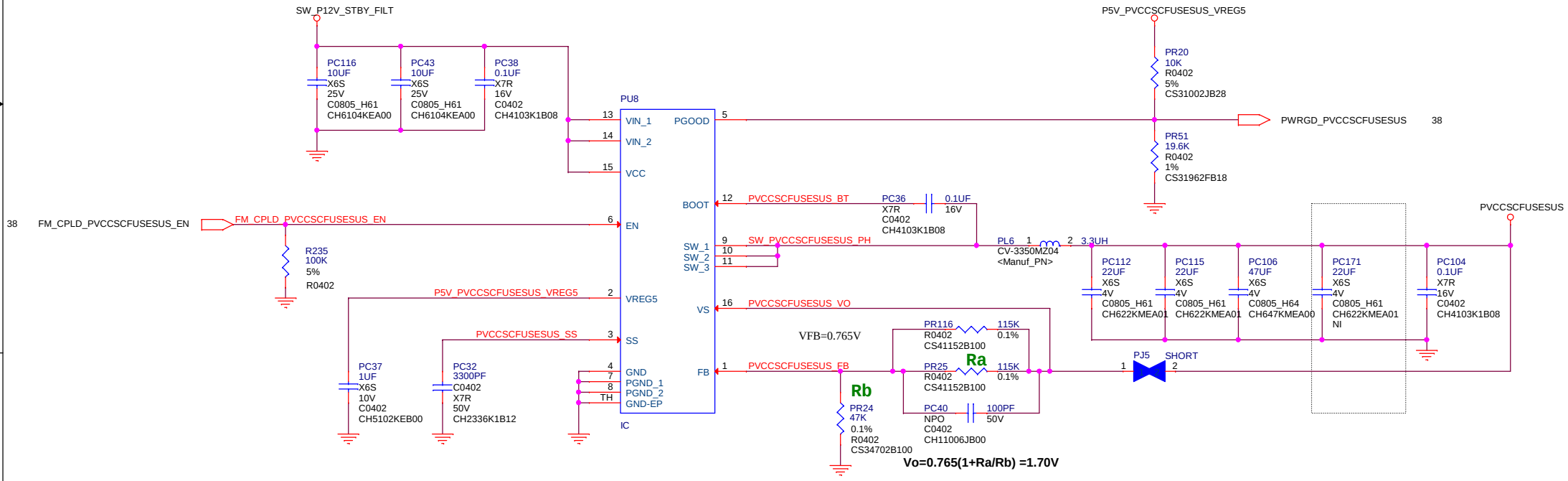
PVCCSCFUSESUS Design specification

Output Voltage = 1.7V
DC (+/- pk) < 2%
Ripple (+/- pk) < 10mV
Total TOL (+/-) < 5%
TDC = 1.3A
Max current =2A
Over-Current Protection(IC rating) =4A
Slew Rate = 0.5 A/us
load step = 1A pk
Work Frequency = 650kHZ
Efficiency > 85% @TDC



PVCCSCFUSESUS

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		Reviewer		Page Title PVCCSCFUSESUS	
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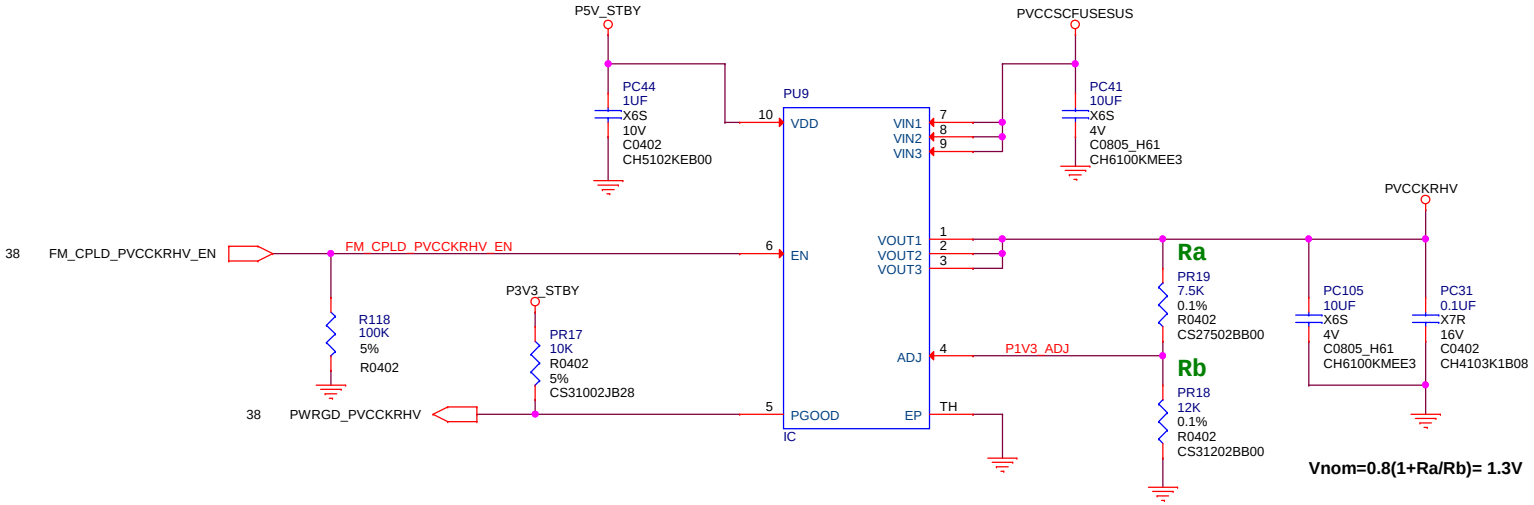
PVCCKRHV Design specification

Output Voltage = 1.3V
DC (+/- pk) < 2.1%
Ripple (+/- pk) < 4mV
Total TOL (+/-) < 4%
TDC = 0.25A
Max current =0.5A
Slew Rate = 11 A/us
load step = 0.15A pk
PD = (1.7V - 1.3V) * 0.25A = 0.1W



PVCCKRHV

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		Reviewer		Page Title PVCCKRHV	
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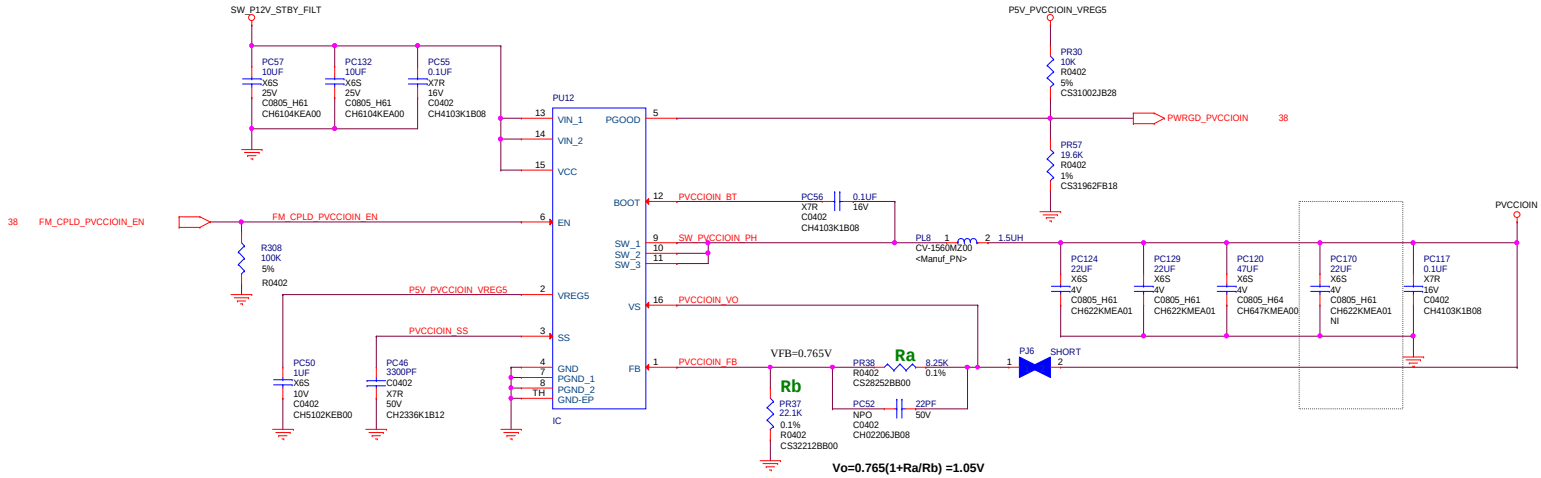
PVCCIOIN Design specification

Output Voltage = 1.05V
DC (+/- pk) < 2.1%
Ripple (+/- pk) < 1%
Total TOL (+/-) < 5%/52.5mV
TDC = 1.7A
Max current =2A
Over-Current Protection(IC rating) =4A
Slew Rate = 0.3 A/us
Load step = 0.3A pk
Work Frequency = 650kHZ
Efficiency > 85% @TDC



PVCCIOIN

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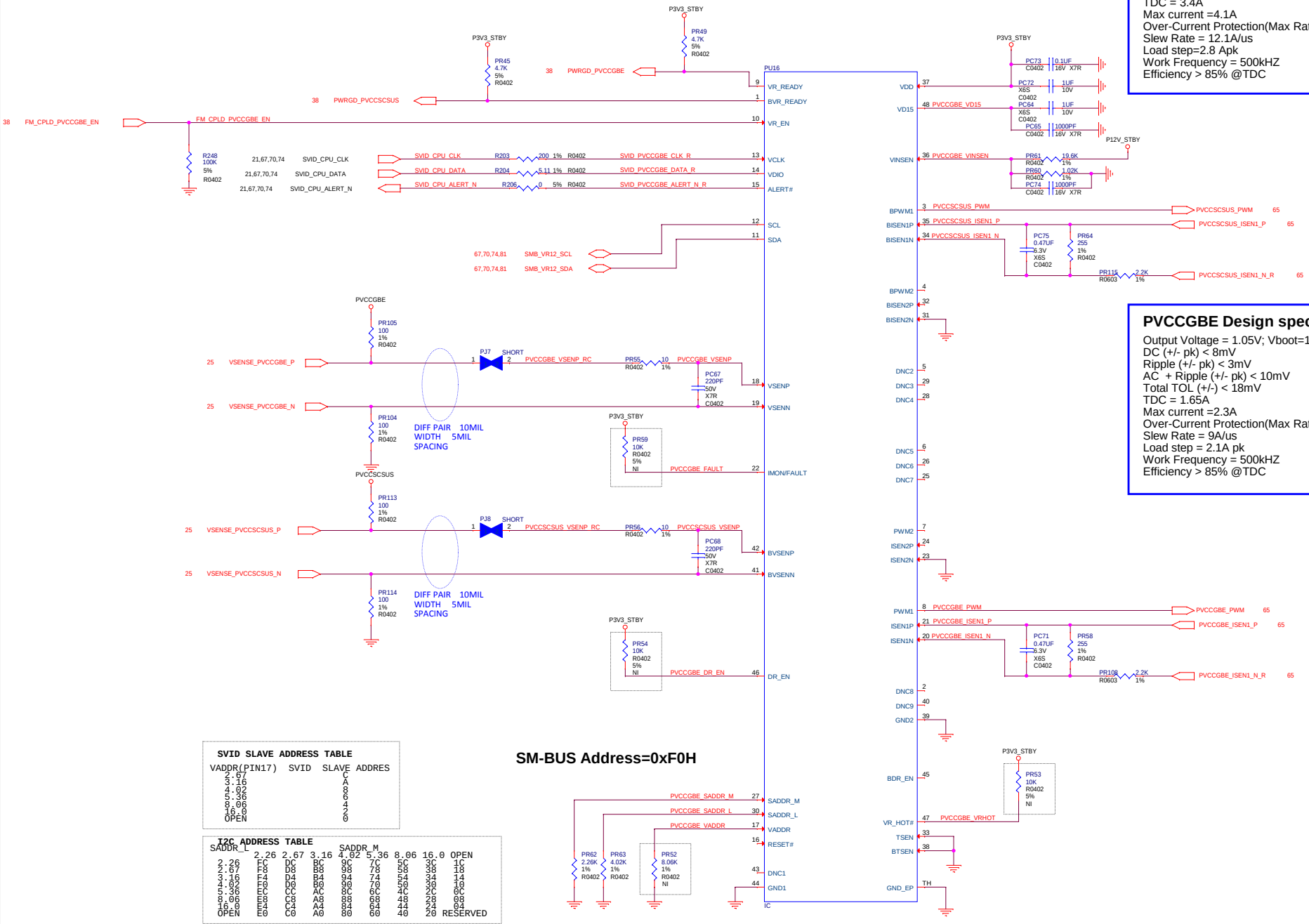
PVCCSCSUS Design specification

Output Voltage = Typ 1.05V; Vboot=1.05V
DC (+/- pk) < 8mV
Ripple (+/- pk) < 4mV
Total TOL (+/-) = 5%
TDC = 3.4A
Max current =4.1A
Over-Current Protection(Max Rating × 1.5) =4.65A
Slew Rate = 12.1A/us
Load step=2.8 Apk
Work Frequency = 500kHZ
Efficiency > 85% @TDC

PVCCGBE Design specification

Output Voltage = 1.05V; Vboot=1.05V
DC (+/- pk) < 8mV
Ripple (+/- pk) < 3mV
AC + Ripple (+/- pk) < 10mV
Total TOL (+/-) < 18mV
TDC = 1.65A
Max current =2.3A
Over-Current Protection(Max Rating × 1.5) =3.45A
Slew Rate = 9A/us
Load step = 2.1A pk
Work Frequency = 500kHZ
Efficiency > 85% @TDC



SVID SLAVE ADDRESS TABLE

VADDR(PIN17)	SVID	SLAVE ADDRES
2.67		C
3.16		A
4.02		8
5.36		6
8.06		4
16.0		2
OPEN		0

I2C ADDRESS TABLE

SADDR_L \ SADDR_M	2.26	2.67	3.16	4.02	5.36	8.06	16.0	OPEN
2.26	FC	DC	BC	9C	7C	5C	3C	1C
2.67	F8	D8	B8	98	78	58	38	18
3.16	F4	D4	B4	94	74	54	34	14
4.02	F0	D0	B0	90	70	50	30	10
5.36	EC	CC	AC	8C	6C	4C	2C	0C
8.06	E8	C8	A8	88	68	48	28	08
16.0	E4	C4	A4	84	64	44	24	04
OPEN	E0	C0	A0	80	60	40	20	RESERVED

SM-BUS Address=0xF0H

PVCCGBE & PVCCSCSUS

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		Reviewer	Page Title PVCCGBE& PVCCSCSUS		
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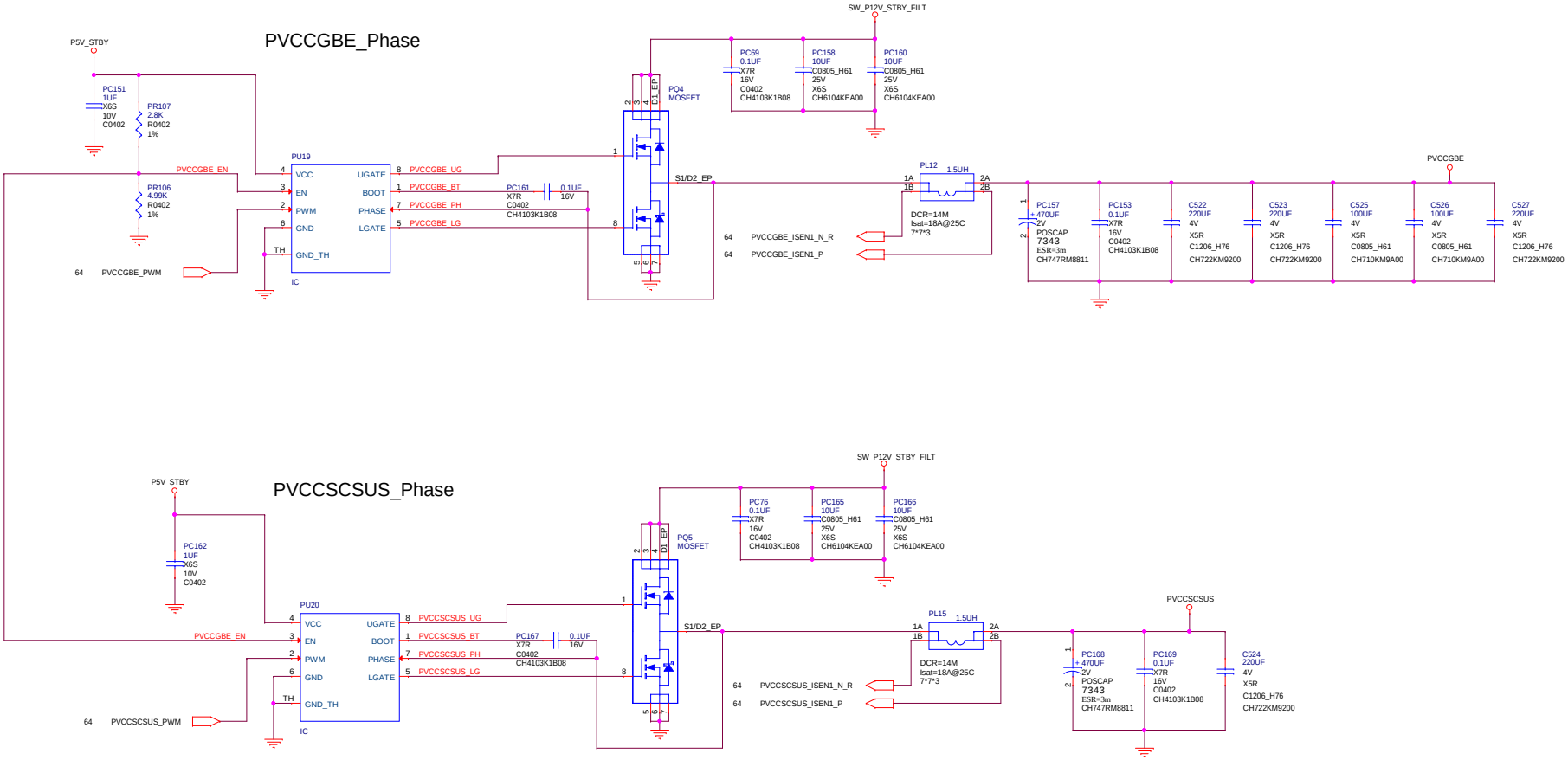

PVCCGBE & PVCCSCSUS PHASE

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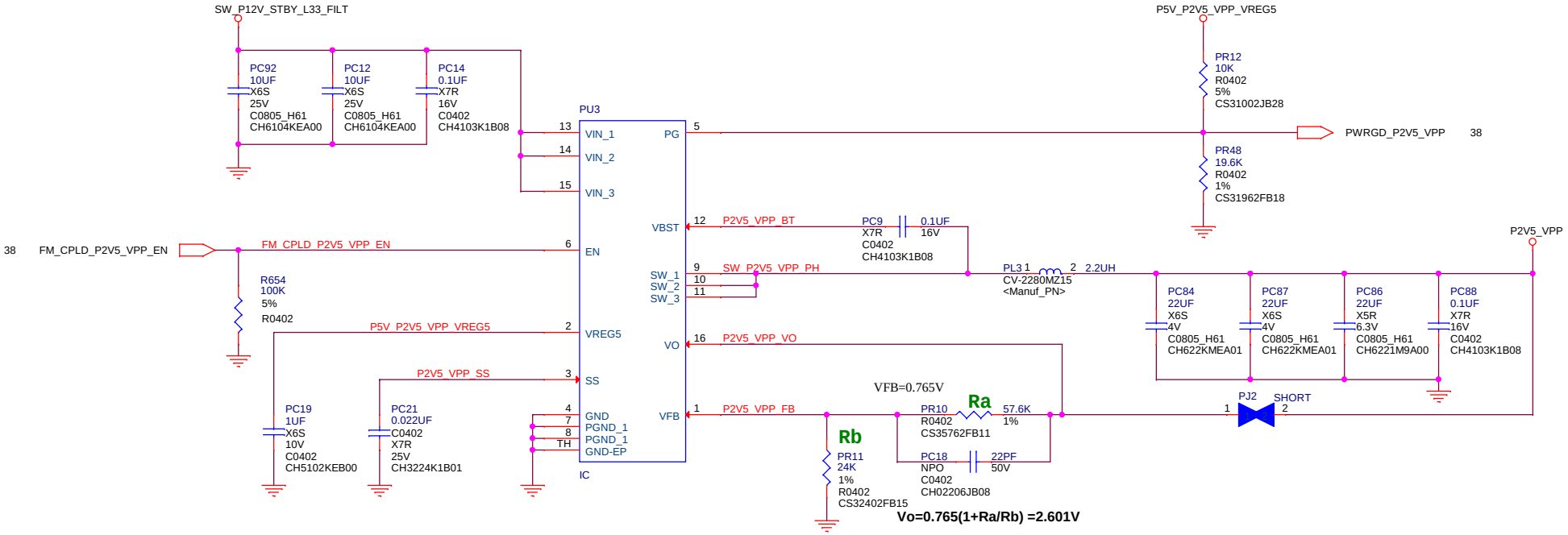
P2V5_VPP Design specification

Output Voltage = 2.6V
DC (+/- pk) < 75mV
Ripple (+/- pk) < 25mV
Total TOL (+/-) < 250mV / -90mV (2.750V/2.410V)
TDC = 4.26A
Max current =4.26A
Over-Current Protection(IC rating) =6.1A
Slew Rate = 13.74 A/us
Load step (0.15A-3.6A) = 3.45A pk
Work Frequency = 650kHZ
Efficiency > 90% @TDC



P2V5_VPP

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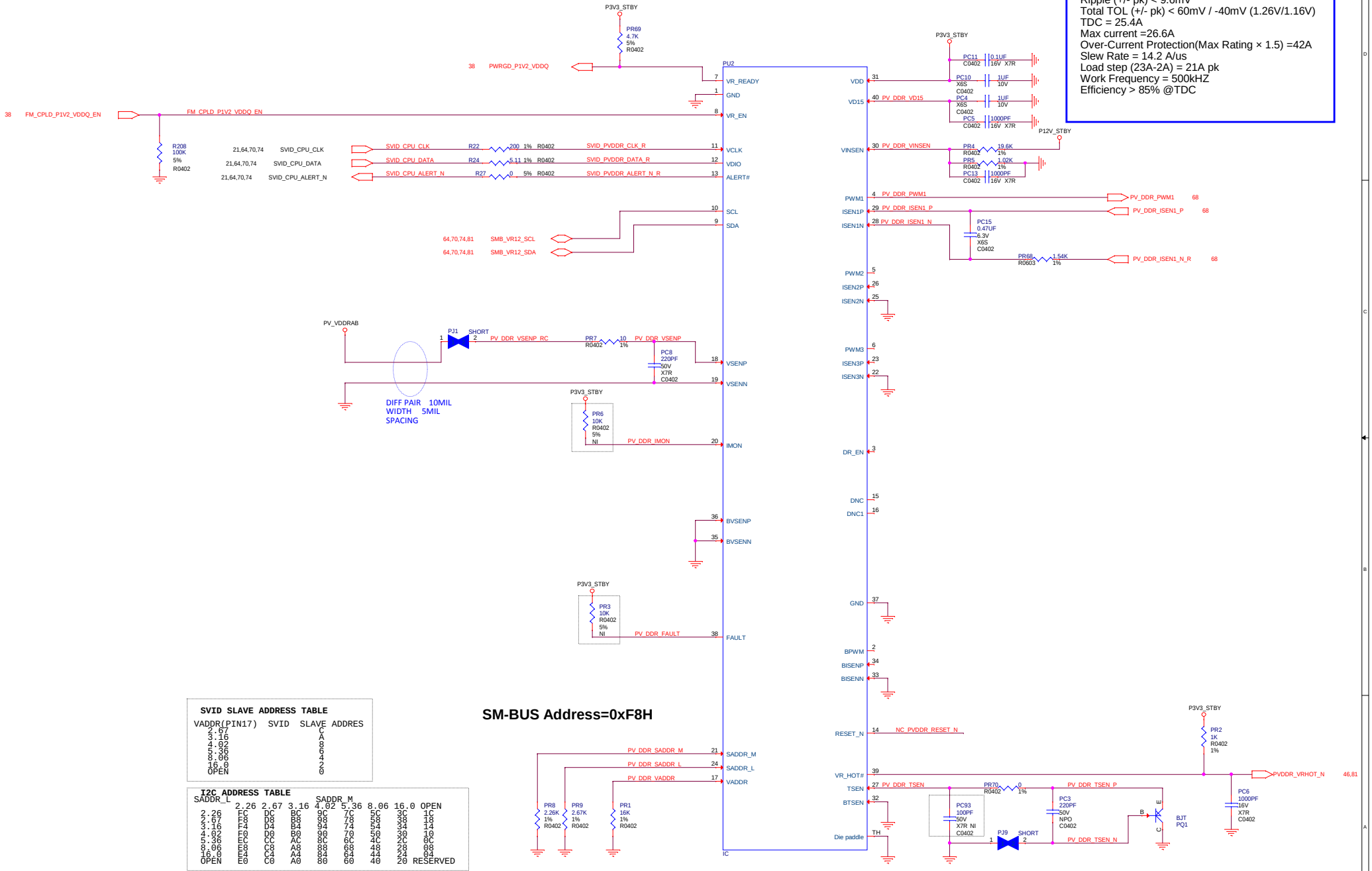
PV_VDDRAB Design specification

Output Voltage = 1.215V
DC (+/- pk) < 8mV; Vboot=1.2V
Ripple (+/- pk) < 9.6mV
Total TOL (+/- pk) < 60mV / -40mV (1.26V/1.16V)
TDC = 25.4A
Max current =26.6A
Over-Current Protection(Max Rating × 1.5) =42A
Slew Rate = 14.2 A/us
Load step (23A-2A) = 21A pk
Work Frequency = 500kHZ
Efficiency > 85% @TDC



SVID SLAVE ADDRESS TABLE

VADDR(PIN17)	SVID	SLAVE ADDRES
2.67		C
3.16		A
4.02		8
5.36		6
8.06		4
16.0		2
OPEN		0

I2C ADDRESS TABLE

SADDR_L \ SADDR_M	2.26	2.67	3.16	4.02	5.36	8.06	16.0	OPEN
2.26	FC	DC	BC	9C	7C	5C	3C	1C
2.67	F8	D8	B8	98	78	58	38	18
3.16	F4	D4	B4	94	74	54	34	14
4.02	F0	D0	B0	90	70	50	30	10
5.36	EC	CC	AC	8C	6C	4C	2C	0C
8.06	E8	C8	A8	88	68	48	28	08
16.0	E4	C4	A4	84	64	44	24	04
OPEN	E0	C0	A0	80	60	40	20	RESERVED

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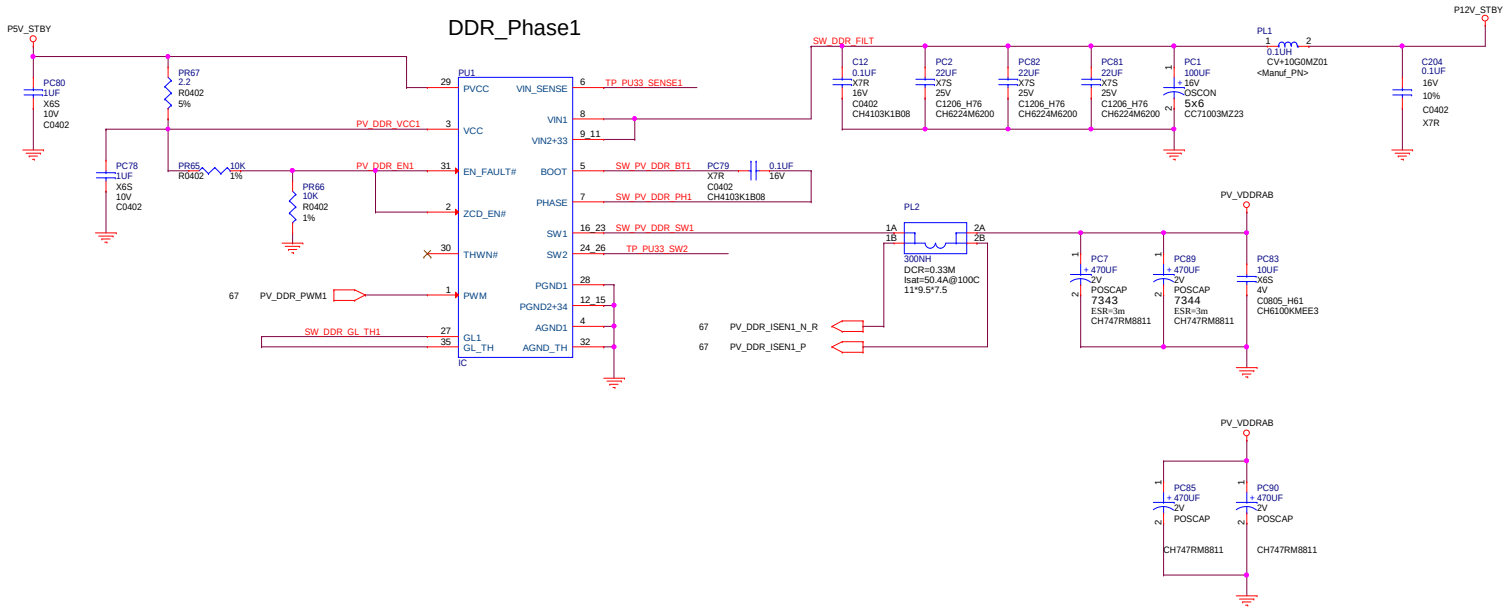
PV_VDDRAB



PV_VDDRAB_PHASE

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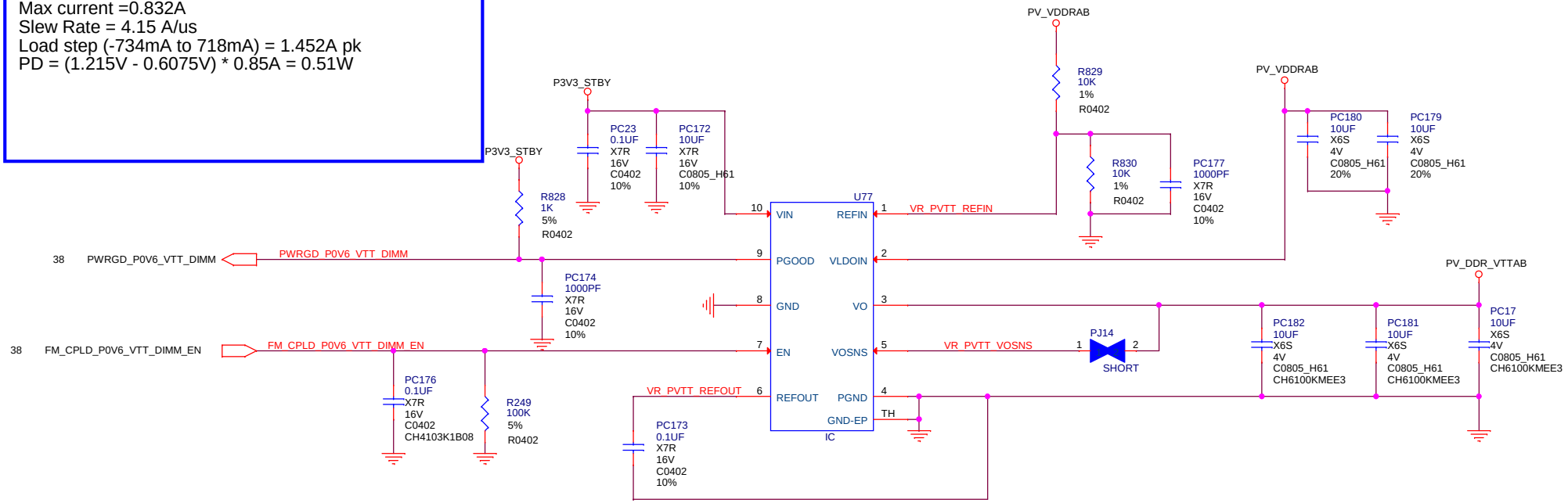
PV_DDR_VTT_AB Design specification

Output Voltage = 0.608V
DC (+/- pk) < 15mV
Total TOL (+/-) < +51mV / -45mV (0.651V/0.555V)
TDC = 0.832A
Max current =0.832A
Slew Rate = 4.15 A/us
Load step (-734mA to 718mA) = 1.452A pk
PD = (1.215V - 0.6075V) * 0.85A = 0.51W



PV_DDR_VTTAB

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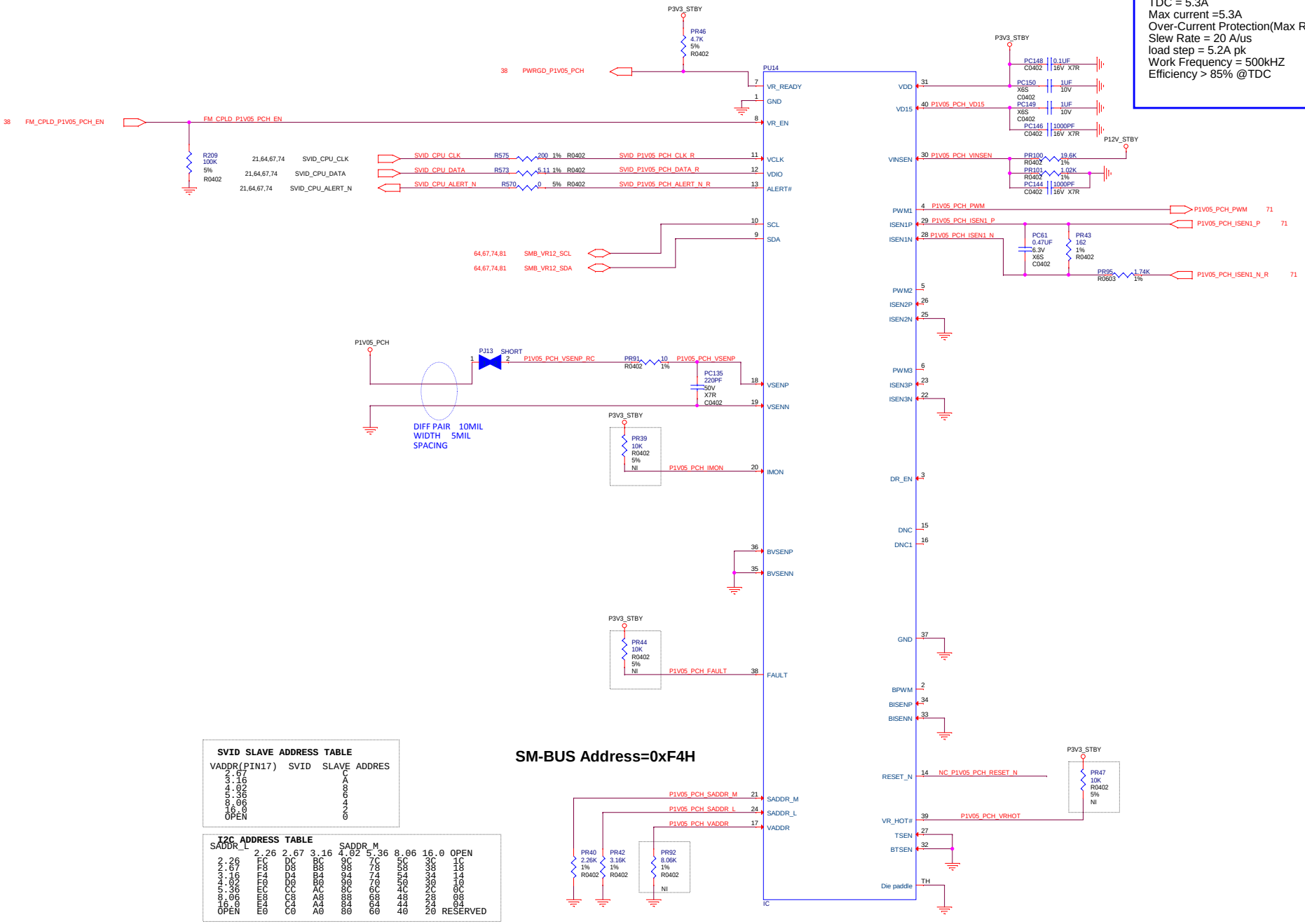
P1V05_PCH Design specification

Output Voltage = 1.05V
DC (+/- pk) < 8mV
Ripple (+/- pk) < 6mV
Total TOL (+/-) < 5%/52.5mV
TDC = 5.3A
Max current =5.3A
Over-Current Protection(Max Rating × 1.5) =7.95A
Slew Rate = 20 A/us
load step = 5.2A pk
Work Frequency = 500kHZ
Efficiency > 85% @TDC



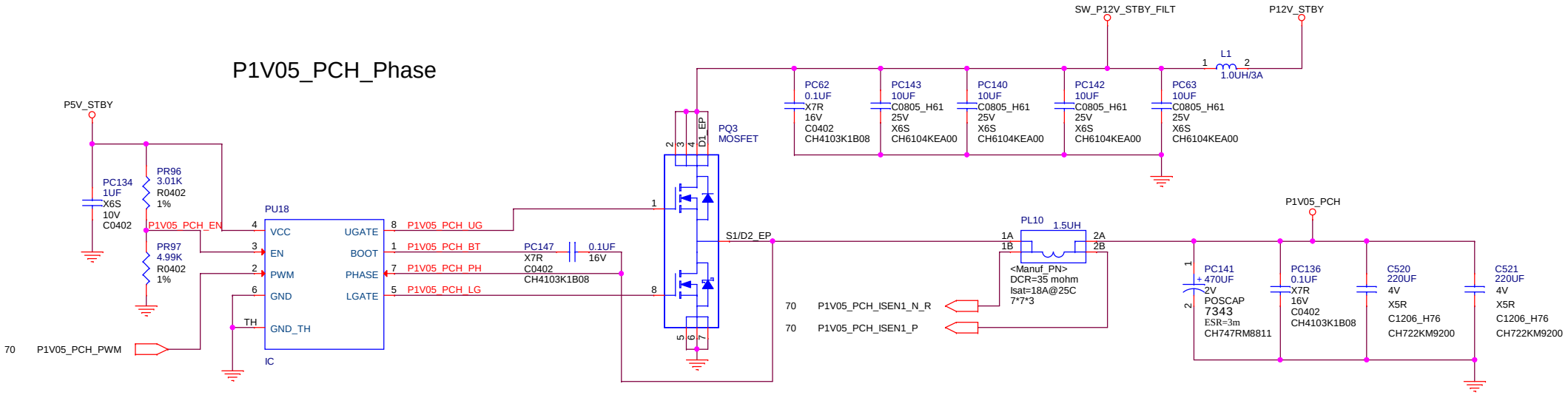
SVID SLAVE ADDRESS TABLE

VADDR(PIN17)	SVID	SLAVE ADDRES
2.67		C
3.16		A
4.02		8
5.36		6
8.06		4
16.0		2
OPEN		0

I2C ADDRESS TABLE

SADDR_L \ SADDR_M	2.26	2.67	3.16	4.02	5.36	8.06	16.0	OPEN
2.26	FC	DC	BC	9C	7C	5C	3C	1C
2.67	F8	D8	B8	98	78	58	38	18
3.16	F4	D4	B4	94	74	54	34	14
4.02	F0	D0	B0	90	70	50	30	10
5.36	EC	CC	AC	8C	6C	4C	2C	0C
8.06	E8	C8	A8	88	68	48	28	08
16.0	E4	C4	A4	84	64	44	24	04
OPEN	E0	C0	A0	80	60	40	20	RESERVED

P1V05_PCH



P1V05_PCH PHASE

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P1V05_PROC_IO & P3V3 SWITCH

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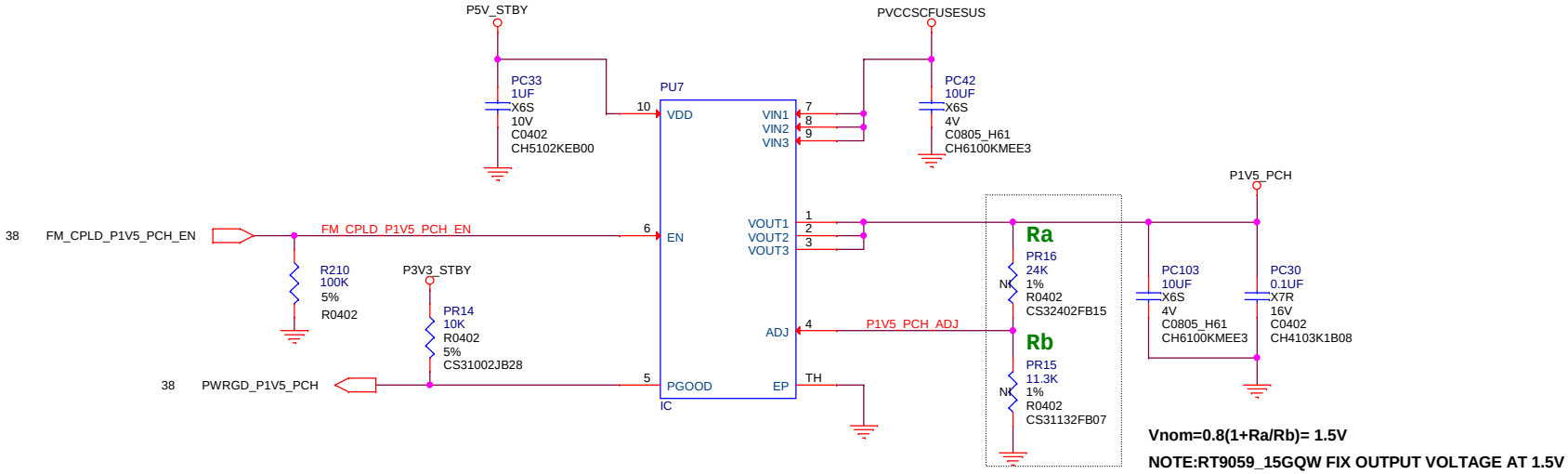
P1V5_PCH Design specification

Output Voltage = 1.5V
DC (+/- pk) < 3%
Ripple (+/- pk) < 1%
AC + ripple (+/- pk) < 2%
Total TOL (+/-) < 5%
TDC = 0.2A
Max current =0.3A
Slew Rate = 1 A/us
Load step = 0.03A pk
PD = (1.7V - 1.5V) * 0.2A = 0.04W



P1V5_PCH

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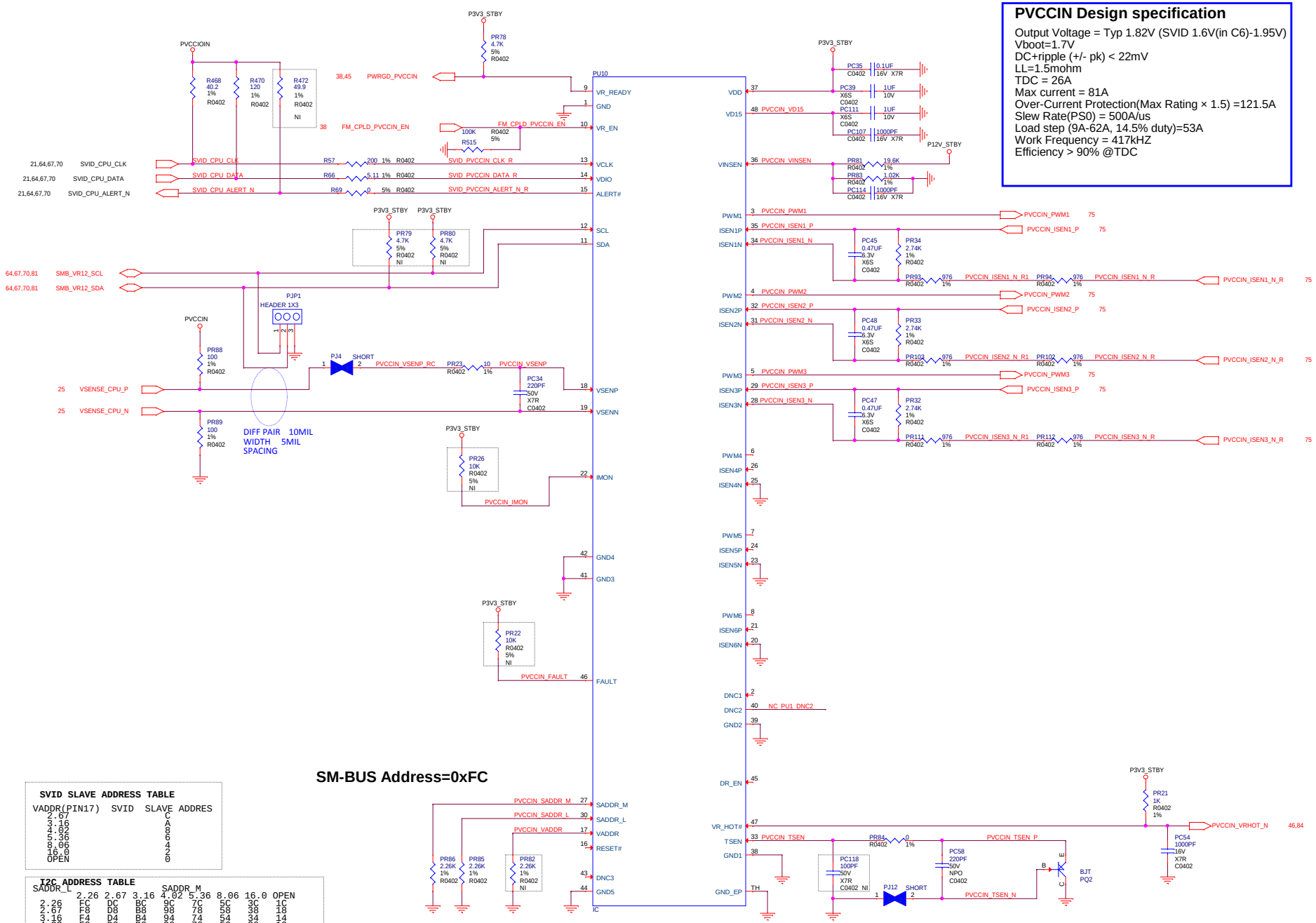

PVCCIN Design specification

Output Voltage = Typ 1.82V (SVID 1.6V(in C6)-1.95V)
Vboot=1.7V
DC+ripple (+/- pk) < 22mV
LL=1.5mohm
TDC = 26A
Max current = 81A
Over-Current Protection(Max Rating × 1.5) =121.5A
Slew Rate(PS0) = 500A/us
Load step (9A-62A, 14.5% duty)=53A
Work Frequency = 417kHZ
Efficiency > 90% @TDC

SVID SLAVE ADDRESS TABLE

VADDR(PIN17)	SVID	SLAVE ADDRES
2.67		C
3.16		A
4.02		8
5.36		6
8.06		4
16.0		2
OPEN		0

I2C ADDRESS TABLE

SADDR_L	2.26	2.67	3.16	4.02	5.36	8.06	16.0	OPEN
SADDR_M								
2.26	FC	DC	BC	9C	7C	5C	3C	1C
2.67	F8	D8	B8	98	78	58	38	18
3.16	F4	D4	B4	94	74	54	34	14
4.02	F0	D0	B0	90	70	50	30	10
5.36	EC	CC	AC	8C	6C	4C	2C	0C
8.06	E8	C8	A8	88	68	48	28	08
16.0	E4	C4	A4	84	64	44	24	04
OPEN	E0	C0	A0	80	60	40	20	RESERVED

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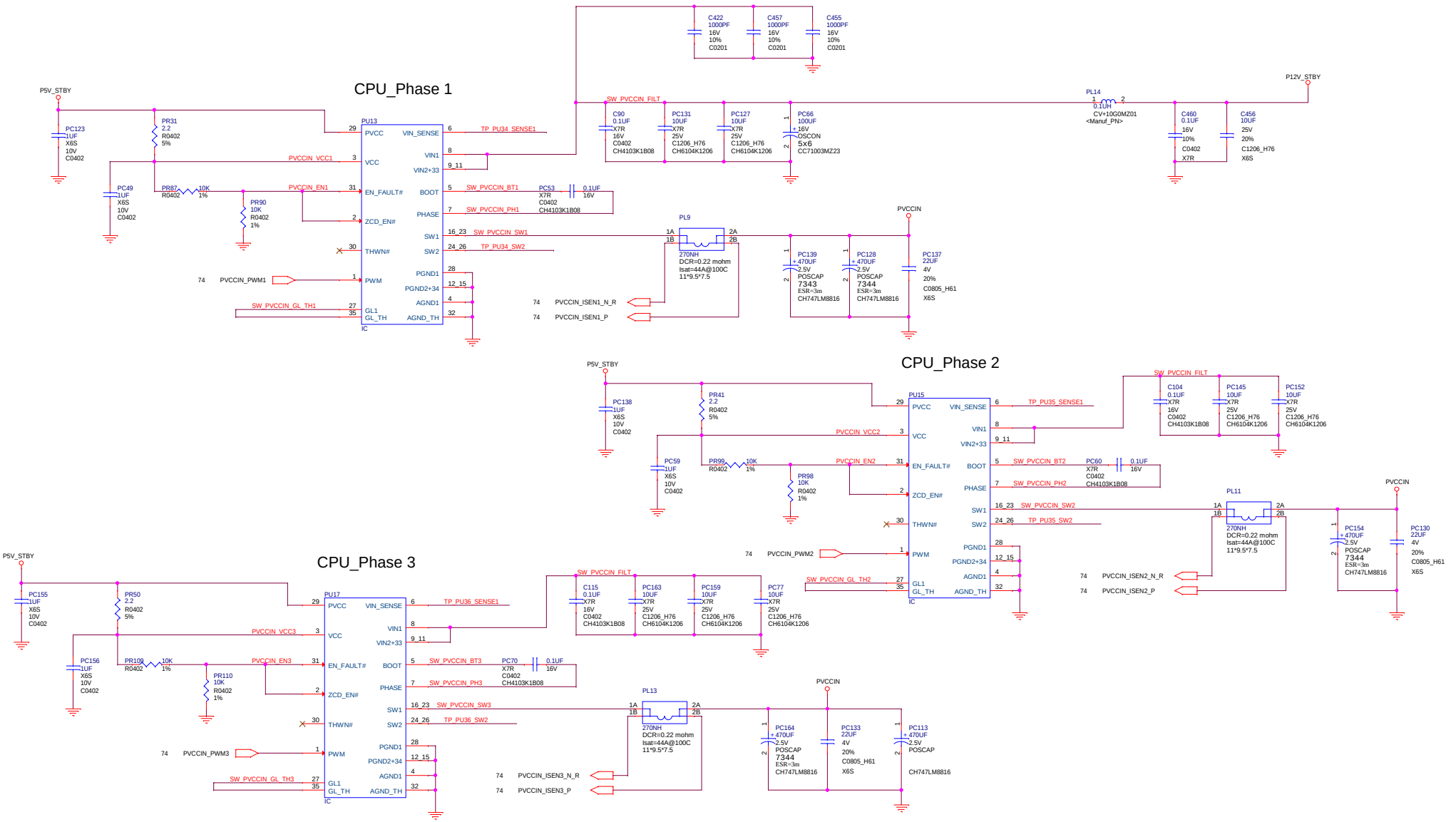
PVCCIN


CPU_Phase 1
CPU_Phase 2
CPU_Phase 3
P5V_STBY
P12V_STBY
PVCCIN
PU13
PU15
PU17
PL9
PL11
PL13
PL14
PVCCIN_VCC1
PVCCIN_VCC2
PVCCIN_VCC3
PVCCIN_EN1
PVCCIN_EN2
PVCCIN_EN3
PVCCIN_PWM1
PVCCIN_PWM2
PVCCIN_PWM3
SW_PVCCIN_FILT
SW_PVCCIN_BT1
SW_PVCCIN_PH1
SW_PVCCIN_SW1
SW_PVCCIN_GL_TH1
SW_PVCCIN_BT2
SW_PVCCIN_PH2
SW_PVCCIN_SW2
SW_PVCCIN_GL_TH2
SW_PVCCIN_BT3
SW_PVCCIN_PH3
SW_PVCCIN_SW3
SW_PVCCIN_GL_TH3
TP_PU34_SENSE1
TP_PU34_SW2
TP_PU35_SENSE1
TP_PU35_SW2
TP_PU36_SENSE1
TP_PU36_SW2
PVCCIN_ISEN1_N_R
PVCCIN_ISEN1_P
PVCCIN_ISEN2_N_R
PVCCIN_ISEN2_P
PVCCIN_ISEN3_N_R
PVCCIN_ISEN3_P
270NH
DCR=0.22 mohm
Isat=44A@100C
11*9.5*7.5
PROPRIETARY NOTE
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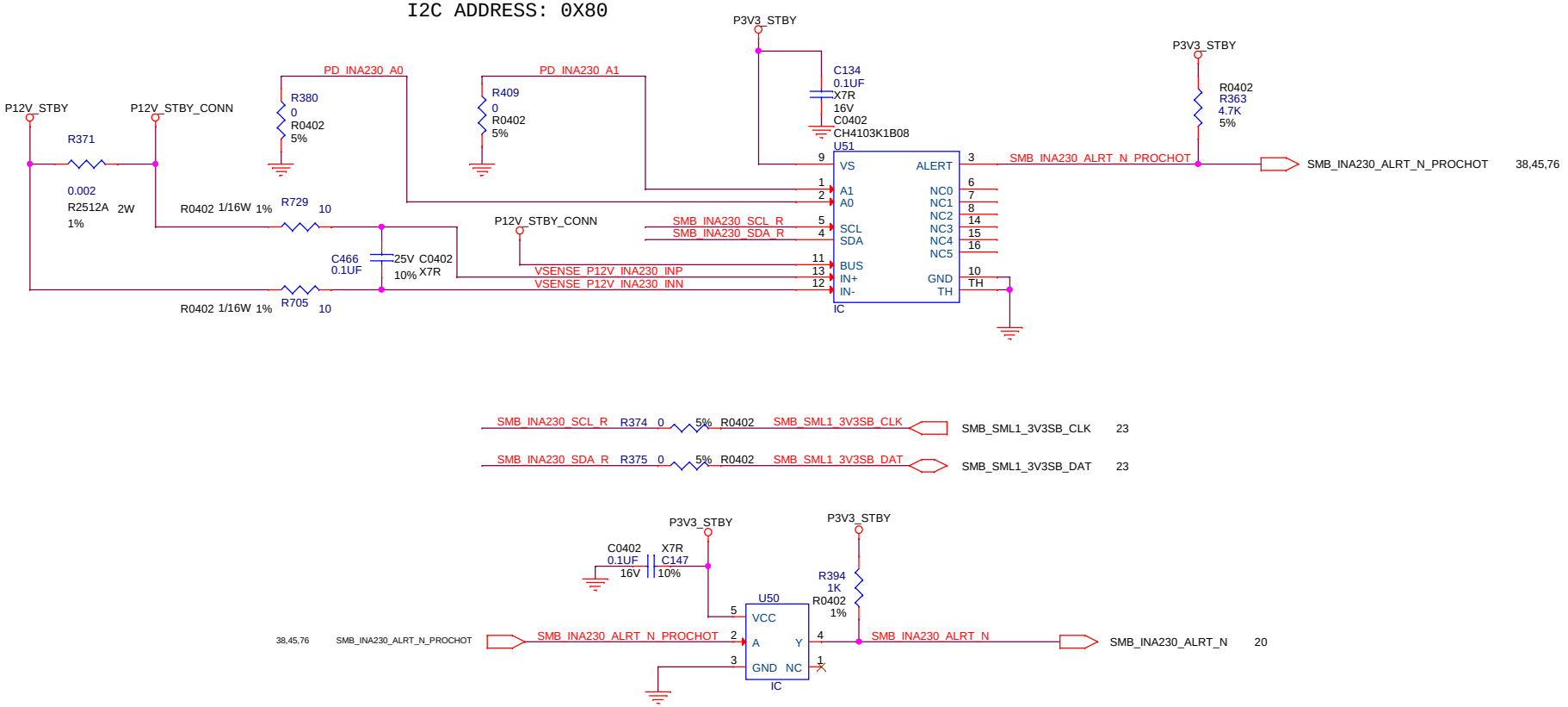

Power sensing

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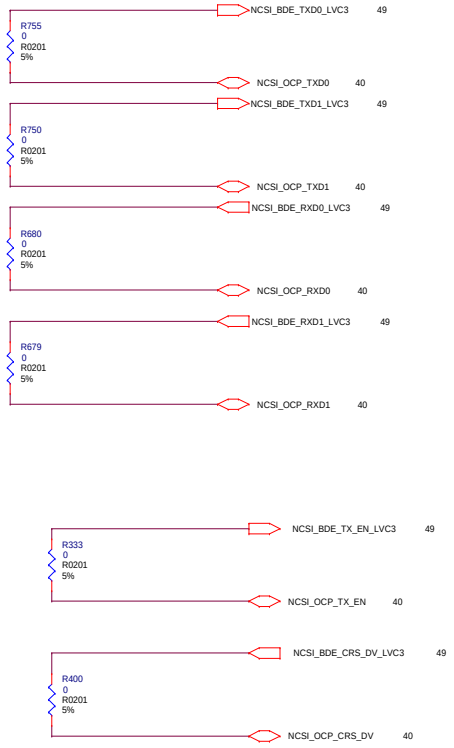

NCSI MUX

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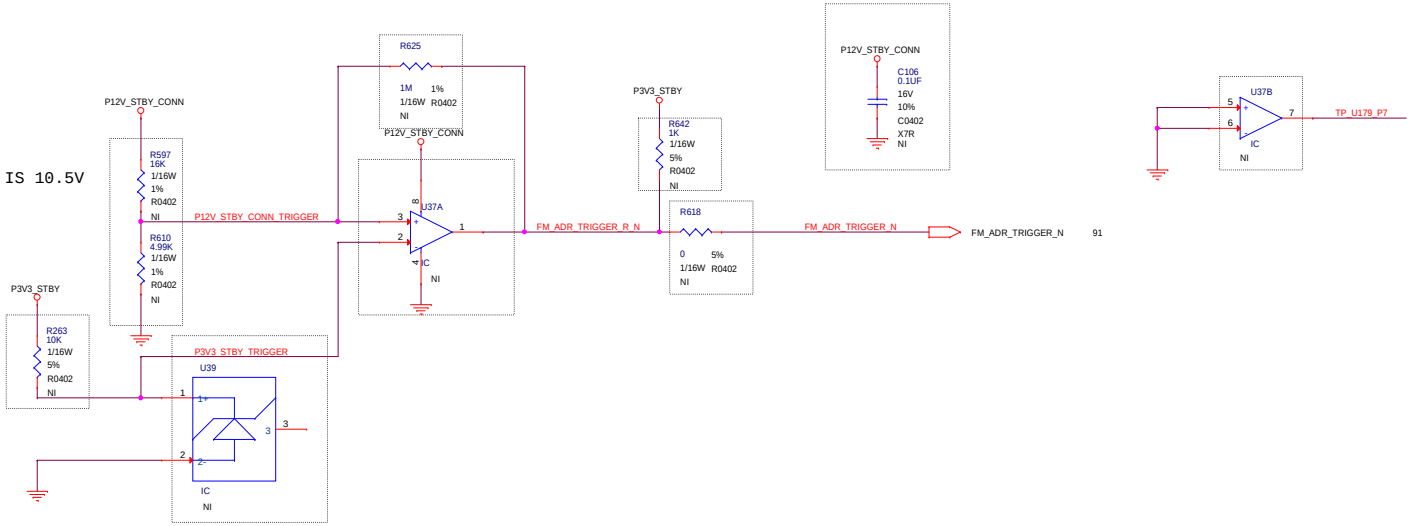
P12V_STBY_CONN TRIP POINT IS 10.5V

10.5*(R1/R1+R2)=3.3



ADR FUNCTION

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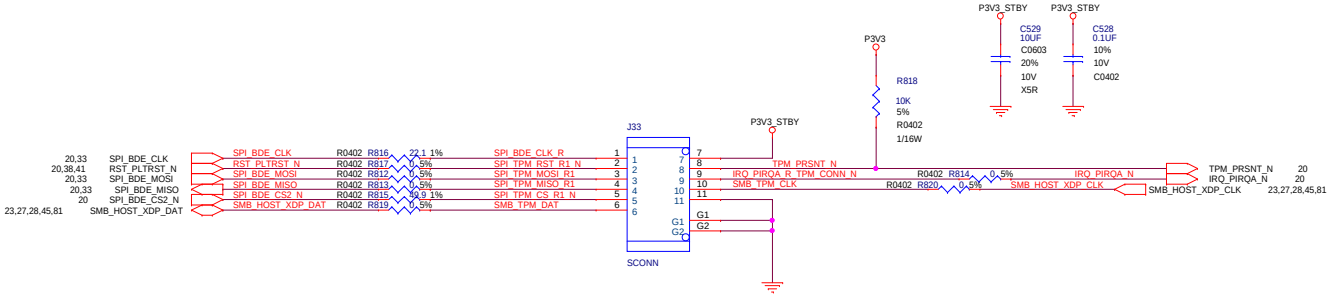

TPM

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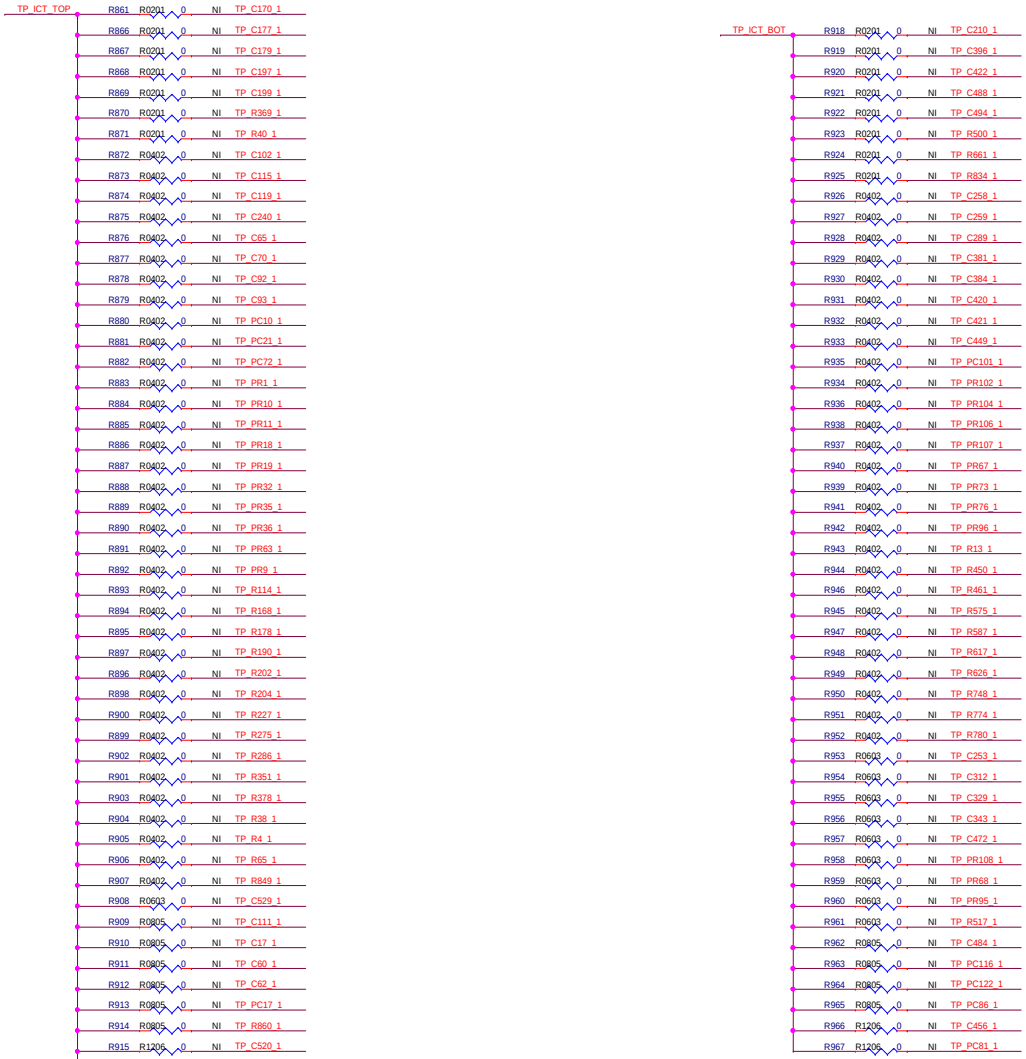

TP RESERVE FOR ICT

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