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Silicon to Software™

EDA for Multi-die System Integration in a Package

Exploration ➔ Design ➔ Optimization ➔ Validation ➔ Analysis ➔ Signoff

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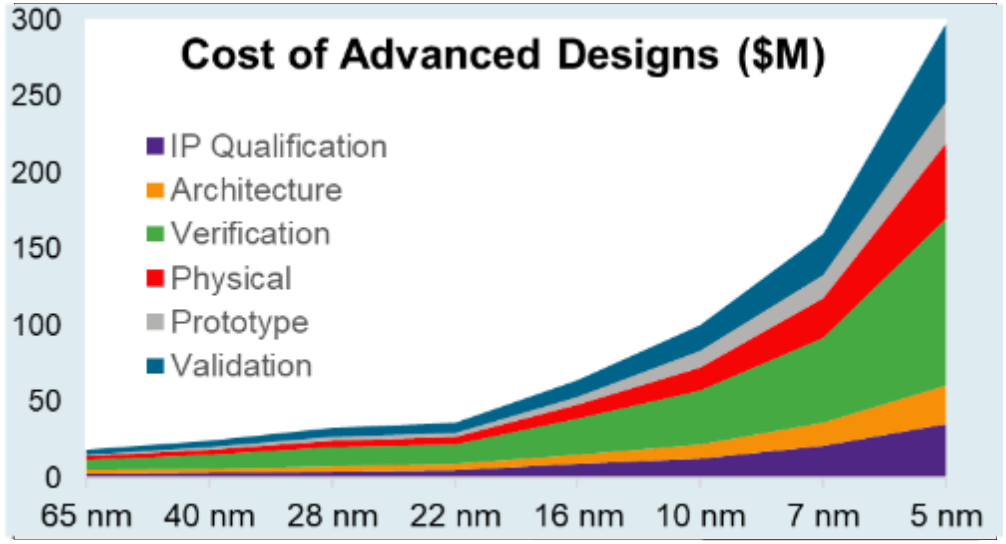
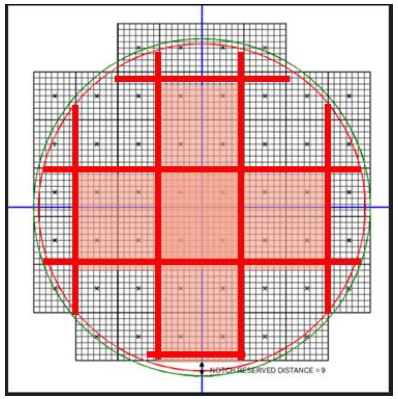
Multi-Die Advanced Packaging

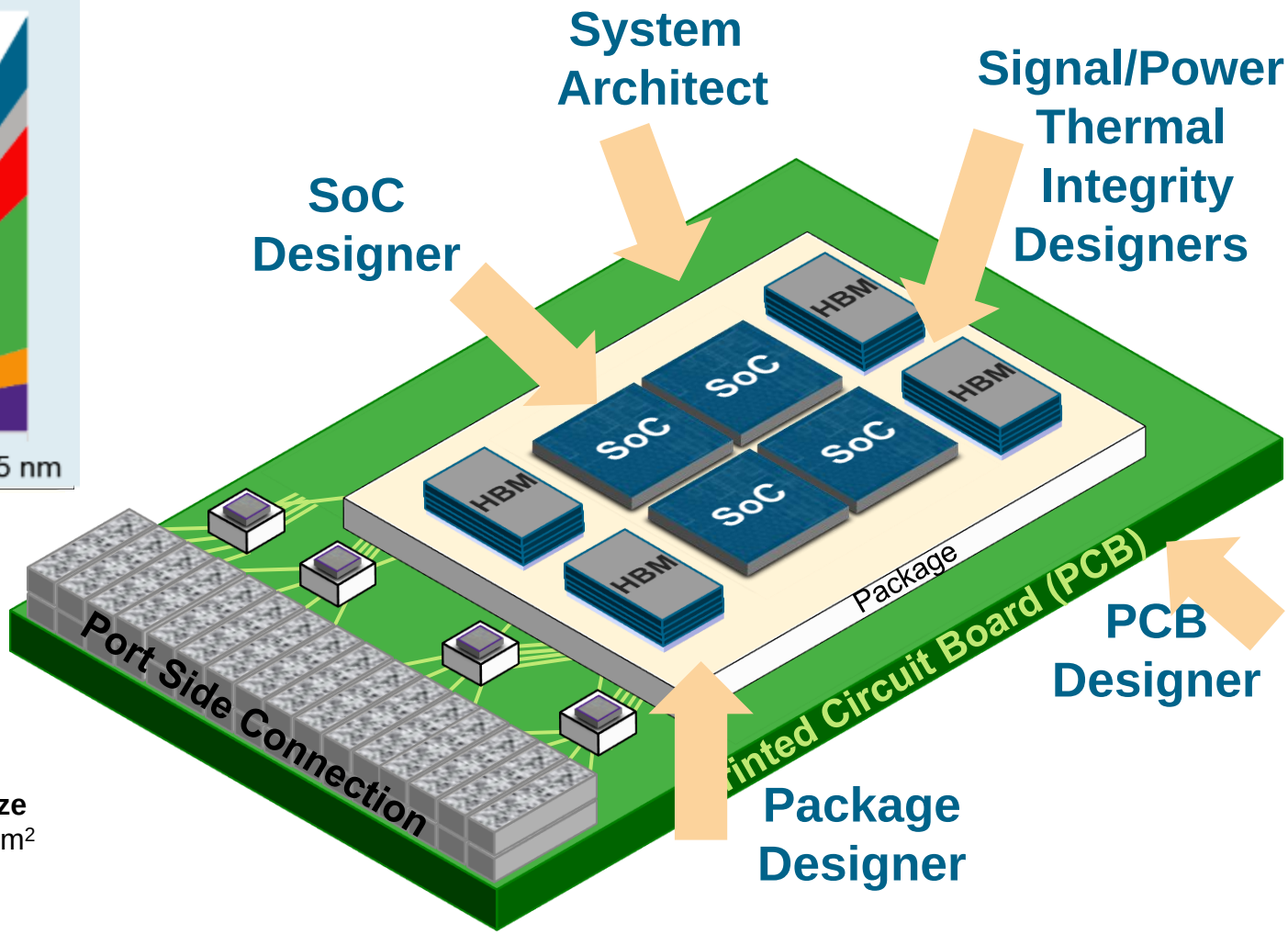
Bandwidth, Performance, Power, Latency, and Development Cycle



Source: Design Activities and Strategic Implications, IBS 2019

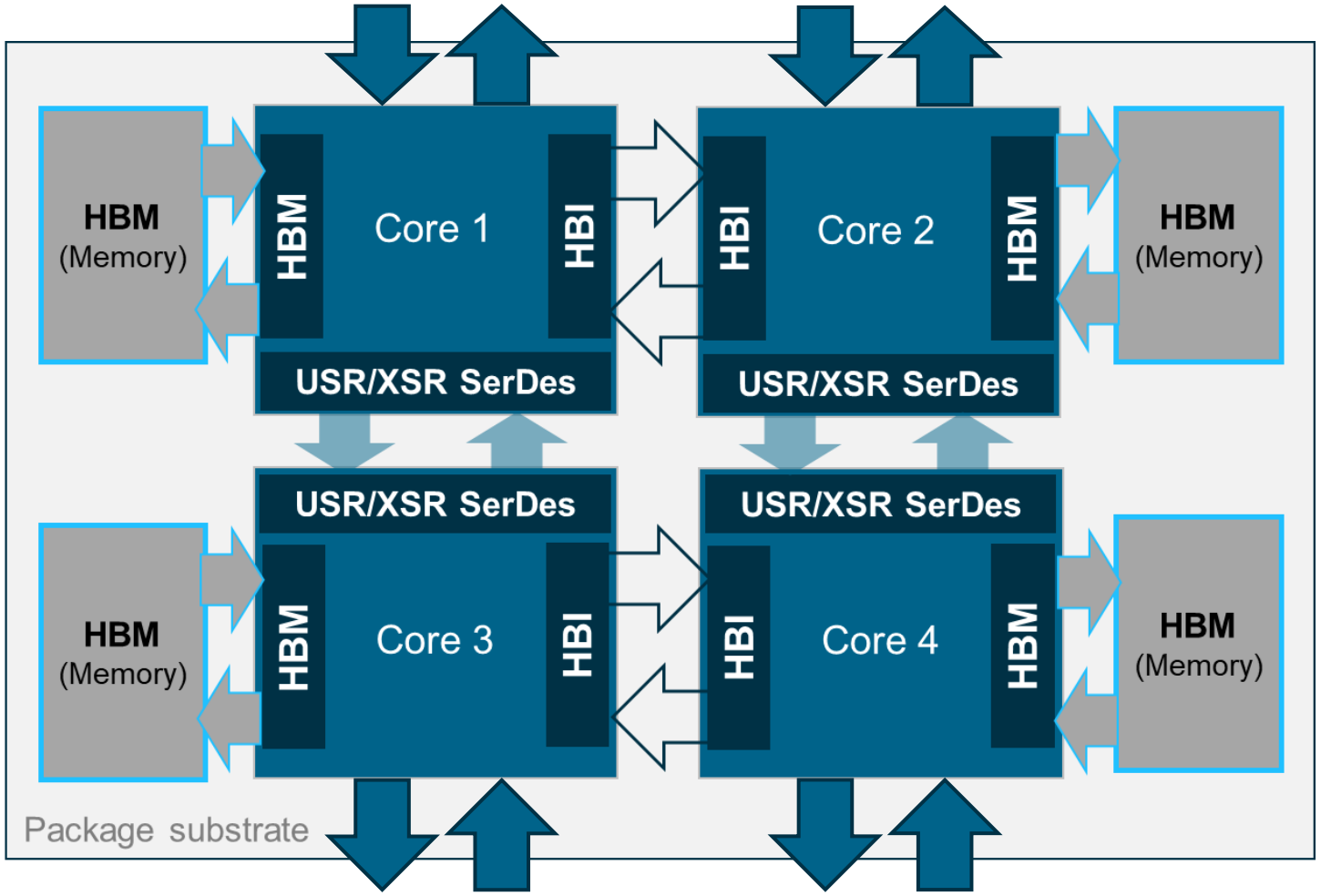


Wafer and reticle size
Max. Stepper ~800 mm^2
(not to scale)



Example Die-to-Die Physical Interfaces (PHYs)

High Bandwidth Memory/Interconnect (HBM/HBI), Ultra/Extra Short Reach (USR/XSR)



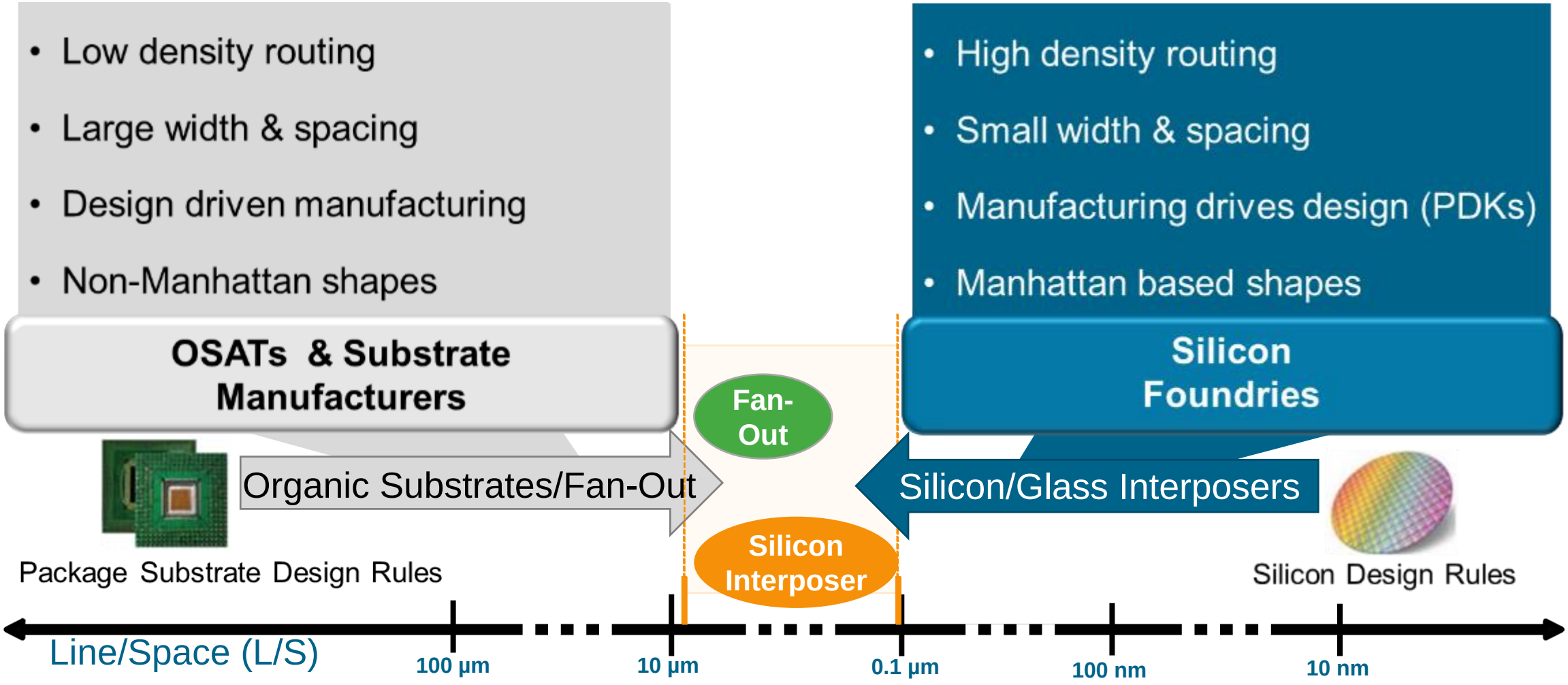
Die-to-Die Interface

Die-to-Die PHY Options in Advanced Process Nodes

Parallel vs. Serial Interfaces

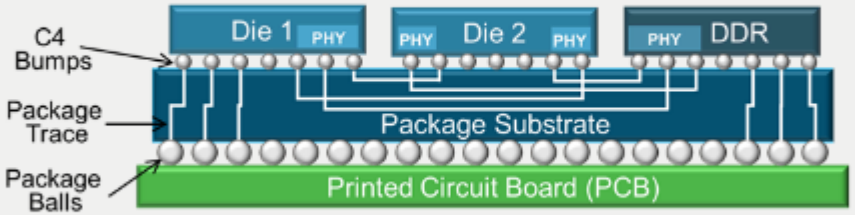
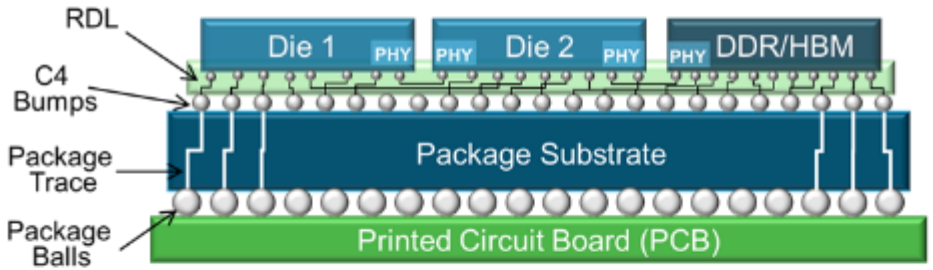
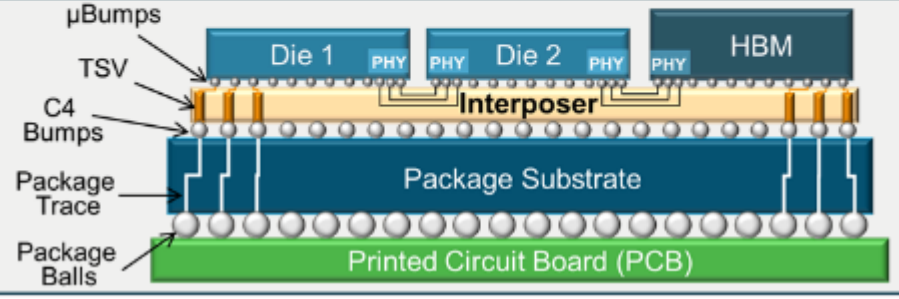
	Parallel Interface		Serial Interface (SerDes)
	Non-Memory	**Memory**	
Standards & Specifications	DARPA, OCP-ODSA AIB, HBI, BoW	JEDEC HBM2, HBM2E HBM3	IEEE 802.3, PCI-SIG, OIF 1G - 56G & 112G URS/XSR
Data Rate per Lane (Gbps)	1 to 2 → 2 to 4 → 4 to 6	2.4 → 3.2 to 3.6 → 6.4	1.25 to 112
I/O number per link	30 to 2000+	1024	2 pairs (4) ✓
Latency	Low ✓	Low ✓	High
Interconnect reach	Short	Short	Long ✓
Interconnect medium type need	High density routing (Silicon Interposer)		Low resistance (High Density Fan-Out)

IC Packaging “Adjacency” Rapidly Morphing into Core EDA



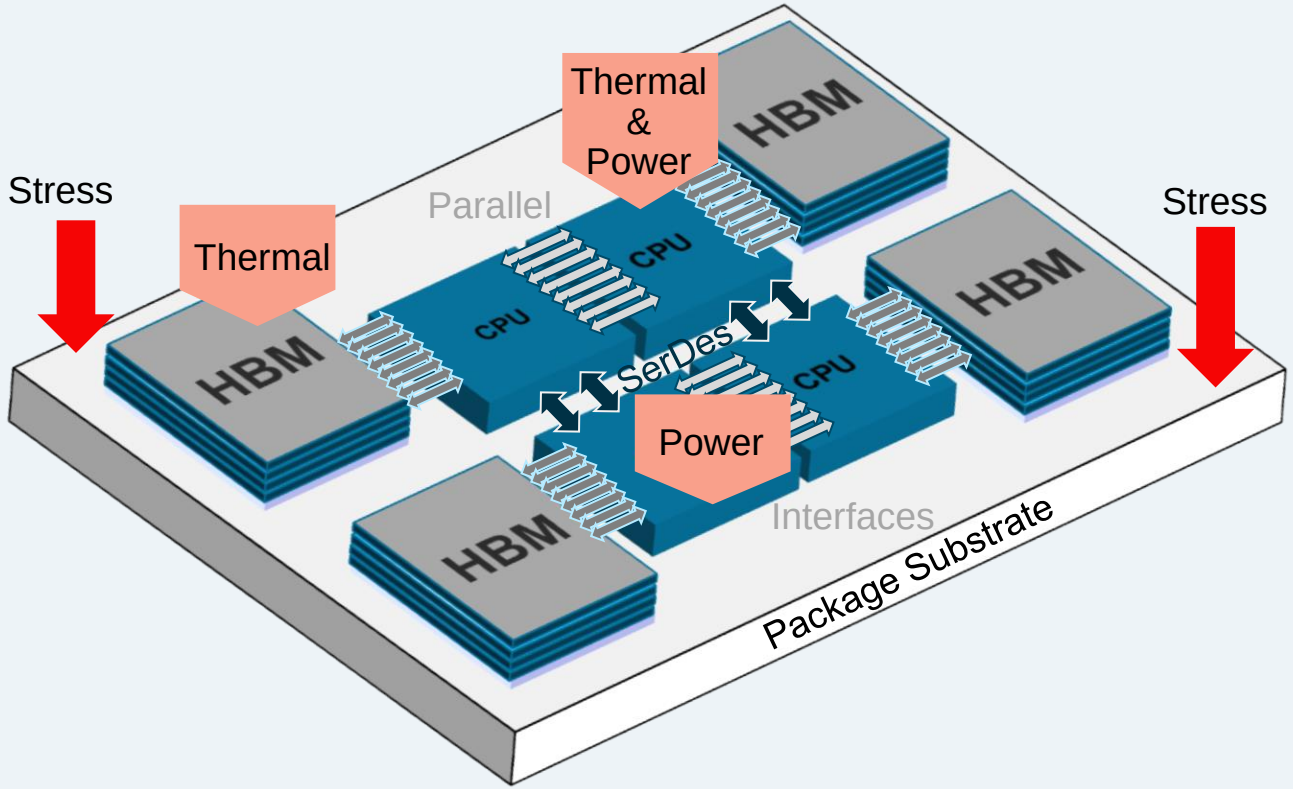
Advanced Packaging Technologies

Interconnect Density, Trace Length, Performance, Size and Cost

		Routing Density w/s	Trace length	Trace loss	Size	Cost
	Multi-Chip-Module (**MCM**) Organic built-up	Low > 8 µm width & spacing	Long ✓	Low ✓	Large Large	Low to Med. ✓
	Wafer level **Fan-Out** Re-distribution layer (RDL)	Med. to High ≥ 2 µm ✓	Med. to Long ✓	Med. to Low ✓	Medium > 2x reticle	Med. to Low ✓
	Silicon /Glass **Interposer** Through silicon Via (TSV)	High ~ 0.4 µm ✓	Short	High	Small 2x reticle	High

2.5D/3DIC Design Challenges

Signal Quality, Power, Thermal & Mechanical Stress



- Signal integrity
- Power integrity
- Thermal integrity
- Mechanical stress
- Complex physical verification and analysis

Chip-Package Co-Design for an Optimal Solution!

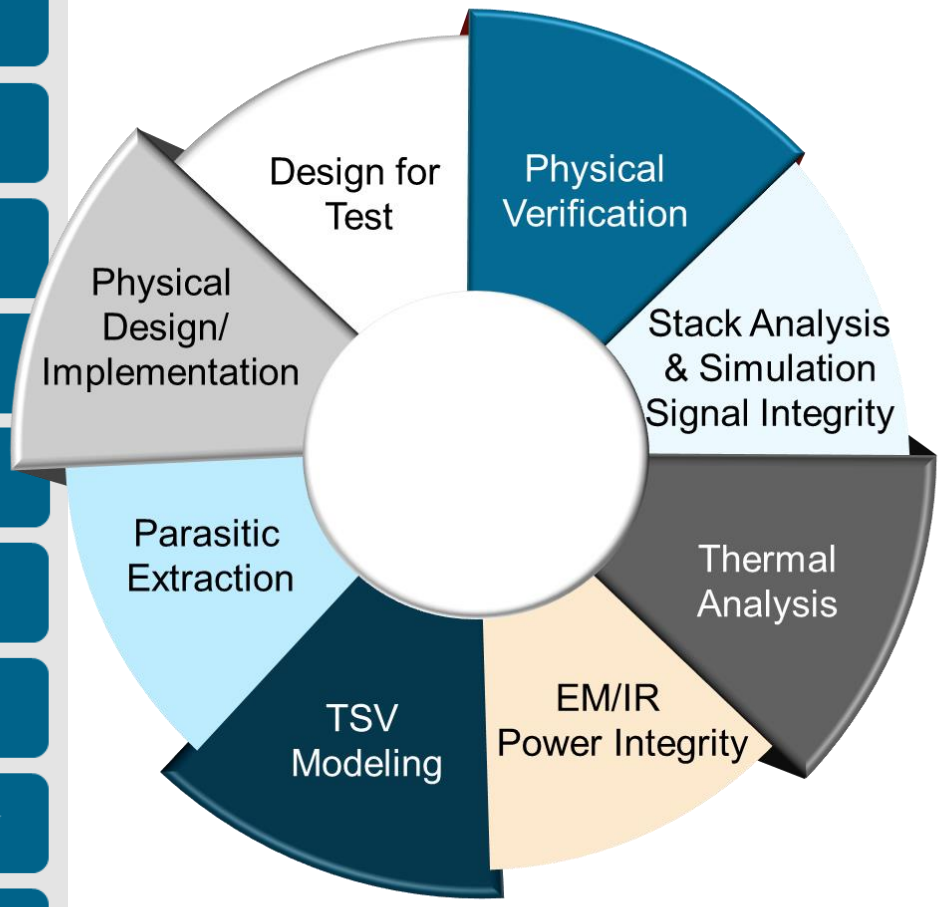
Multi-Die Package Design EDA Tools Today

Existing Limitations and Challenges	Multi-Die Integration Solution

• Disjointed solutions with multiple point tools,
  • Limited cross-discipline collaboration support
  • Each with own interfaces and use models
  • Large feedback loops for convergence
  • Lack of automation
  • Separate use models
  • Database size limitations
 	
• Power/signal/thermal noise optimization starts too late in the design cycle
 	
• Multiple point tools each w/ separate capability and scripts. Lack support for early exploration and end to end validation
	• A unified platform that enables cross-discipline co-design & co-optimization
	  • Unified GUI interface, 3D & 2D view
	  • DRC-aware environment
	  • Automation (routing/shielding, bump placement, …)
	  • Common data model, enabling scalability in capacity and performance
	
	• Power/signal/thermal noise aware design optimization from early exploration to design signoff (die to PCB)
	
	• SoC-scale integrated platform from early architectural exploration, to design/implementation, validation, to signoff

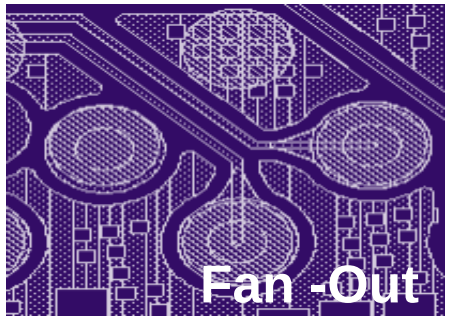
Ideal Multi-Die Design Platform for a System in a Package

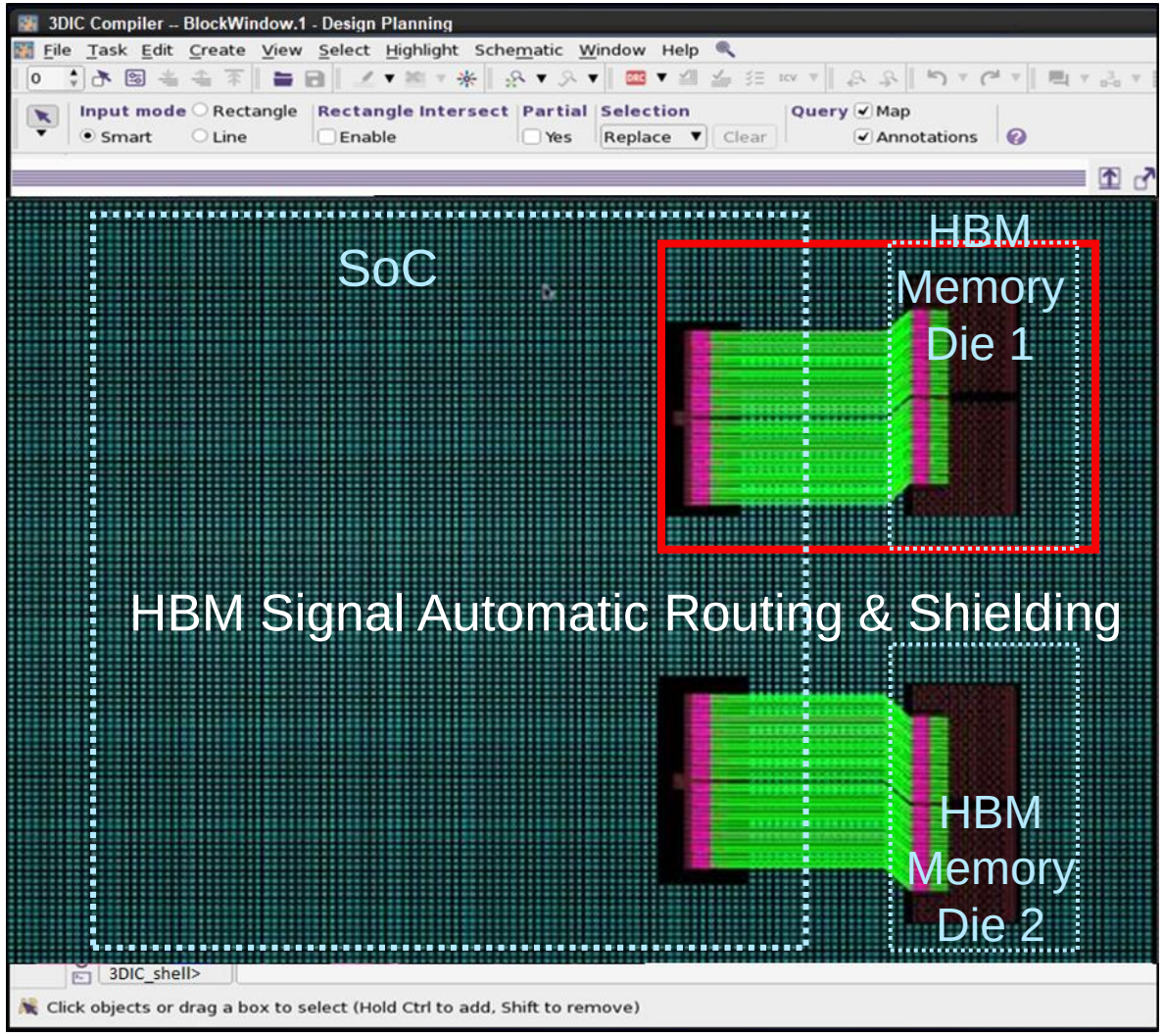
- Exploration
- Floorplanning
- Routing & Shielding
- Test
- Extraction
- Signal Integrity
- Power Integrity
- Thermal Integrity
- Physical Verification

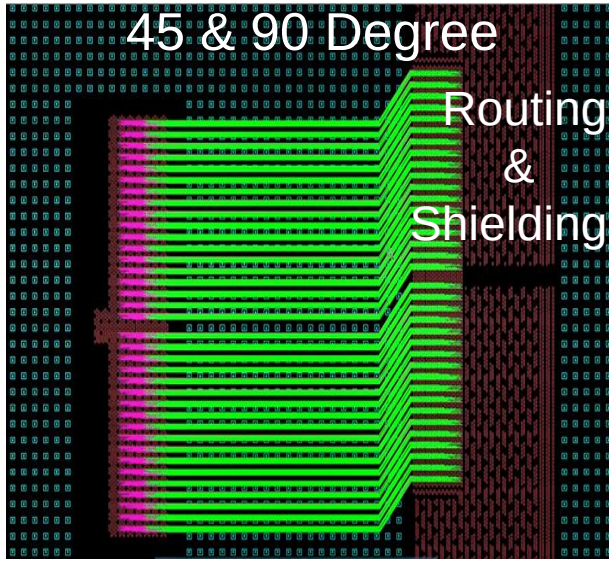


Auto-Routing & Auto-Shielding

Fan-Out routing
(any-angle, teardrops & oblong shapes, degassing hole)





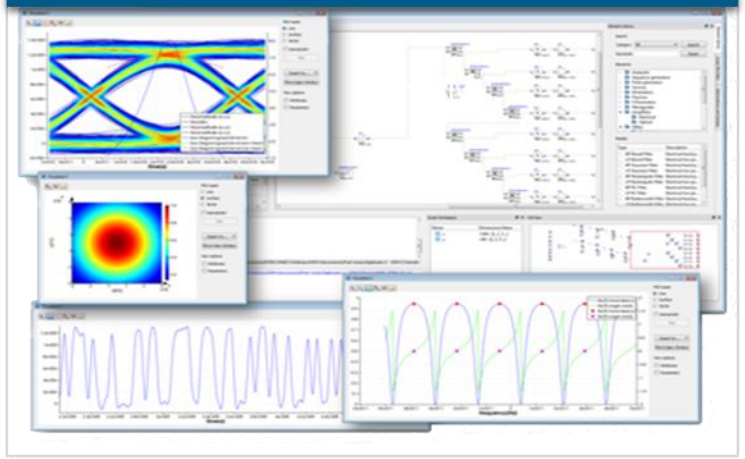


Si Interposer

Multi-Die System Integration – Analysis & Validation

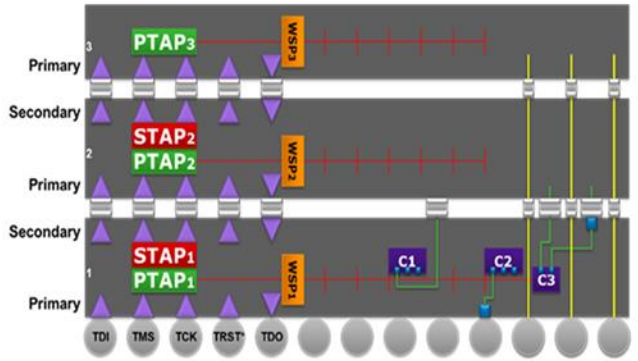
Signal Integrity, Power Integrity, Thermal/Mechanical Integrity, DFT Rule Check→ **Signoff**

Extraction & Signal Integrity

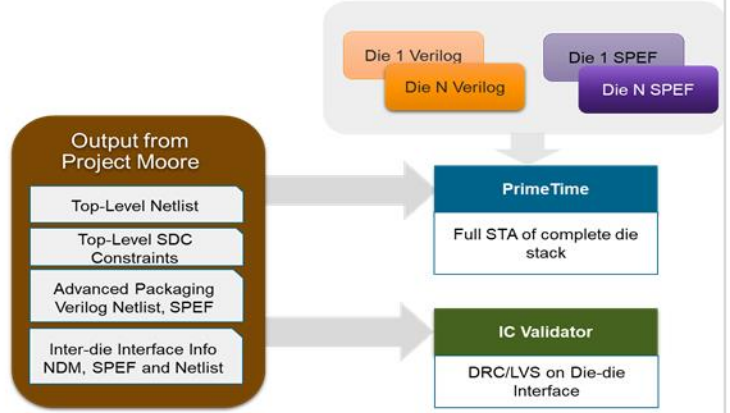


DFT Rule Check

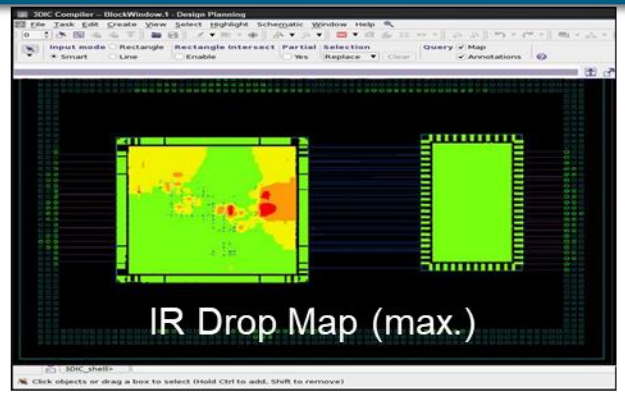
Logical and physical connectivity check



Sign-Off (STA, DRC/VS)

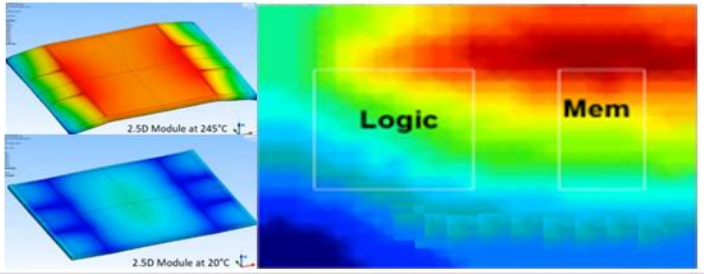


EM/IR & Power Analysis

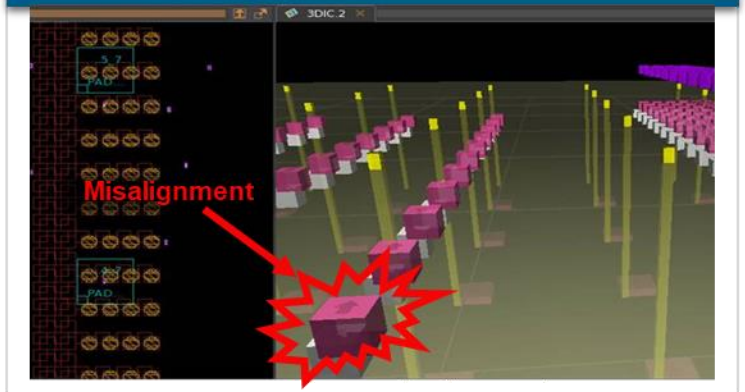


Thermal & Mechanical Analysis

Thermal hotspot detection & correction
Temperature aware resistance, EM, IR



Physical Verification



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