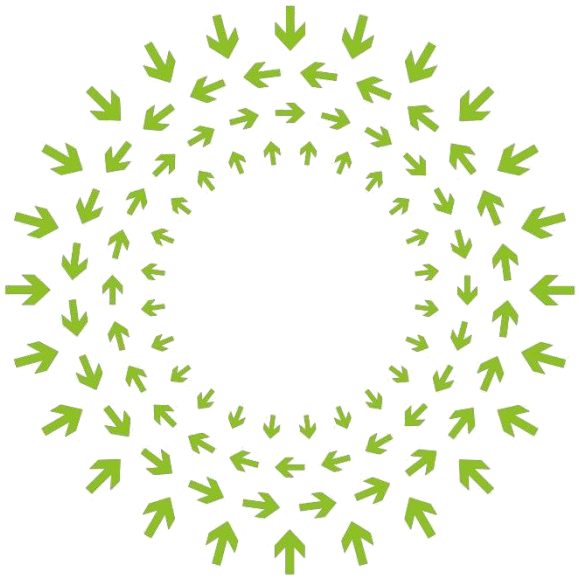


OPEN

Compute Project

Inspur Server Total Design Scheme

Crane Mountain

Rev 0.1

Author:

Inspur Crane Mountain Team

1. Revision History

Version	Date	Description
0.1	4/15/2019	Initial Release

Note: Because the product version upgrade or other reasons, the contents of this document will not be updated on a regular basis. Unless otherwise agreed, this document used only as a guide, in this document, all statements, information and advice does not constitute any express or implied guarantees.

2. Scope

This specification describes Intel Motherboard v4.0 design and design requirement to integrate Intel Motherboard v4.0 into Open Rack V2.

3. Contents

目录

4. Overview

4.1 Overview

Crane Mountain is based on Intel® Cascade Lake-SP CPU architecture. The motherboard supports up to 48 DIMMs. Crane Mountain is designed in the Q1 of 2019. It is update of Sky Lake-SP CPU architecture.

4.2 Product Overview

Crane Mountain is a completely independent research and development of server products. Based on Intel® Cascade Lake-SP CPU architecture, using Lewisburg chipset. Support four mainstream Intel Xeon Cascade Lake-SP 82xx/62xx/52xx series processors. Support 48 DIMMs DDR4 memory, the biggest support to 2933 MHZ. Supports 24pcs 2.5 -inch SATA disk or 6 blocks of 2.5 inch NVMe hard disk, and supports SATA/PCIE M. 2. PCI Express support expansion slot X24 . Supports OCP MEZZ connecter A, B and C, extended SATA * 4 and second block PCIE M. 2 disk. Structure, storage, PCI extension, power supply, fan and other parts modular design. Centralized power supply design, to realize saving energy and reducing consumption.

4.3 Product standard

CPU	
CPU type	Supports four Intel® Cascade Lake-SP 82xx/62xx/52xx series processors (TDP 205W)
Connecter	Four Socket-P0 slots
Chipset	

Chipset type	PCH LBG-2
RAM	
RAM type	DDR4 ECC RDIMM/LRDIMM/3DS LRDIMM
RAM slot quantity	48
RAM total capacity	Total capacity 6144GB（single 128GB）
I/O Connecter	
USB	Two rear USB 3.0 ports, one on board USB 3.0 port
VGA	One rear VGA
UID	One ID pilot lamp inlay
Network card	
Network card controller	Support OCP MEZZ connecter A, B and C.
Manager chipset	
Manager chipset	Integrated one independent 1000 Mbps network interface, specifically for remote management of IPMI.
PCI Express slot	The motherboard supports three PCI Express 3.0 x24 slots
HDD	
HDD type	Support up to 24 2.5-inch SAS/SATA HDDs, or 18 2.5 inch SAS/SATA HDDs and 6 NVMe SSDs
Power supply	
PSU spec	The whole system adopts three specifications of PSU, the power is 800/1300/1600W, and the maximum configuration is 2 power supplies. According to the system configuration, the appropriate PSU and PSU redundancy modes are selected to support 1+1 redundancy under certain configuration conditions.
Input power	The main specifications is 1600W PSU

	AC-- 90-264V,NOM-- 100-240V DC-- 190-310V, NOM-- 240V
Environmental Requirements	
Altitude (Motherboard)	1500m (operational) or 12192m(non - operational)
Altitude (Full system)	1500m (operational) or 12192m(non - operational)
Operating and storage relative humidity (Full system)	10% to 90% (non-condensing)
Operating temperature rang (Motherboard)	-5℃ to +45℃ ; Note: It is suggested to power on to work after standing for 1 hour in the data center, after long time transportation.
Operating temperature range(Full system)	-5℃ to +35℃; Note: It is suggested to power on to work after standing for 1 hour in the data center, after long time transportation.
Storage temperature range (Motherboard)	-40℃ to +70℃
Storage temperature range(Full system)	-40℃ to +70℃
Transportation temperature range(Motherboard)	-40℃ to +70℃ (short-term storage)
Transportation temperature range(Full system)	-40℃ to +70℃ (short-term storage)

5. Physical Specifications

5.1 Block Diagram

Figure 5-1 illustrates the functional block diagram of the Motherboard.

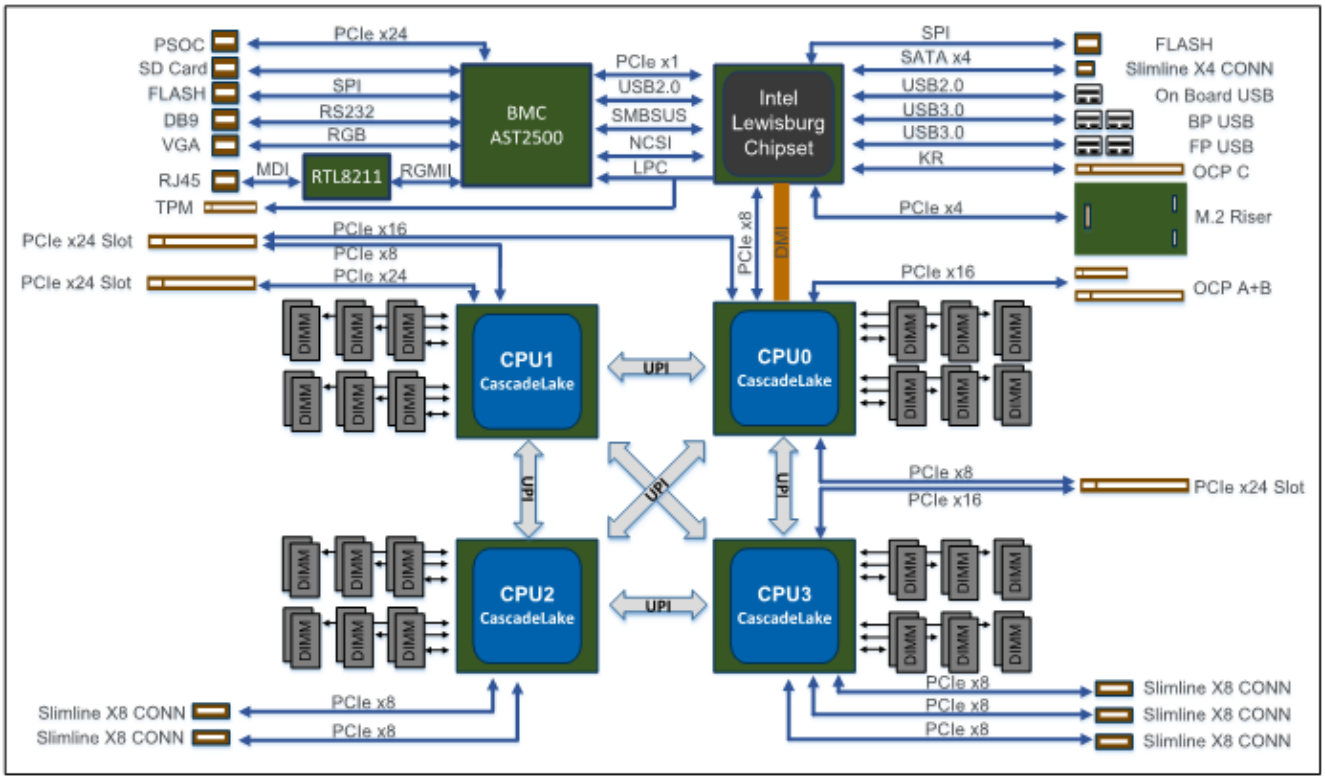


Figure 5-1 Block Diagram

5.2 Placement and Form Factor

Board form factor is 16.7 inch by 24 inch (16.7”x24”). And Figure 5-2 illustrates board placement. The placement is meant to show key components ’relative positions, while exact dimension and position information would be exchanged by DXF format for layout and 3D model for mechanical.

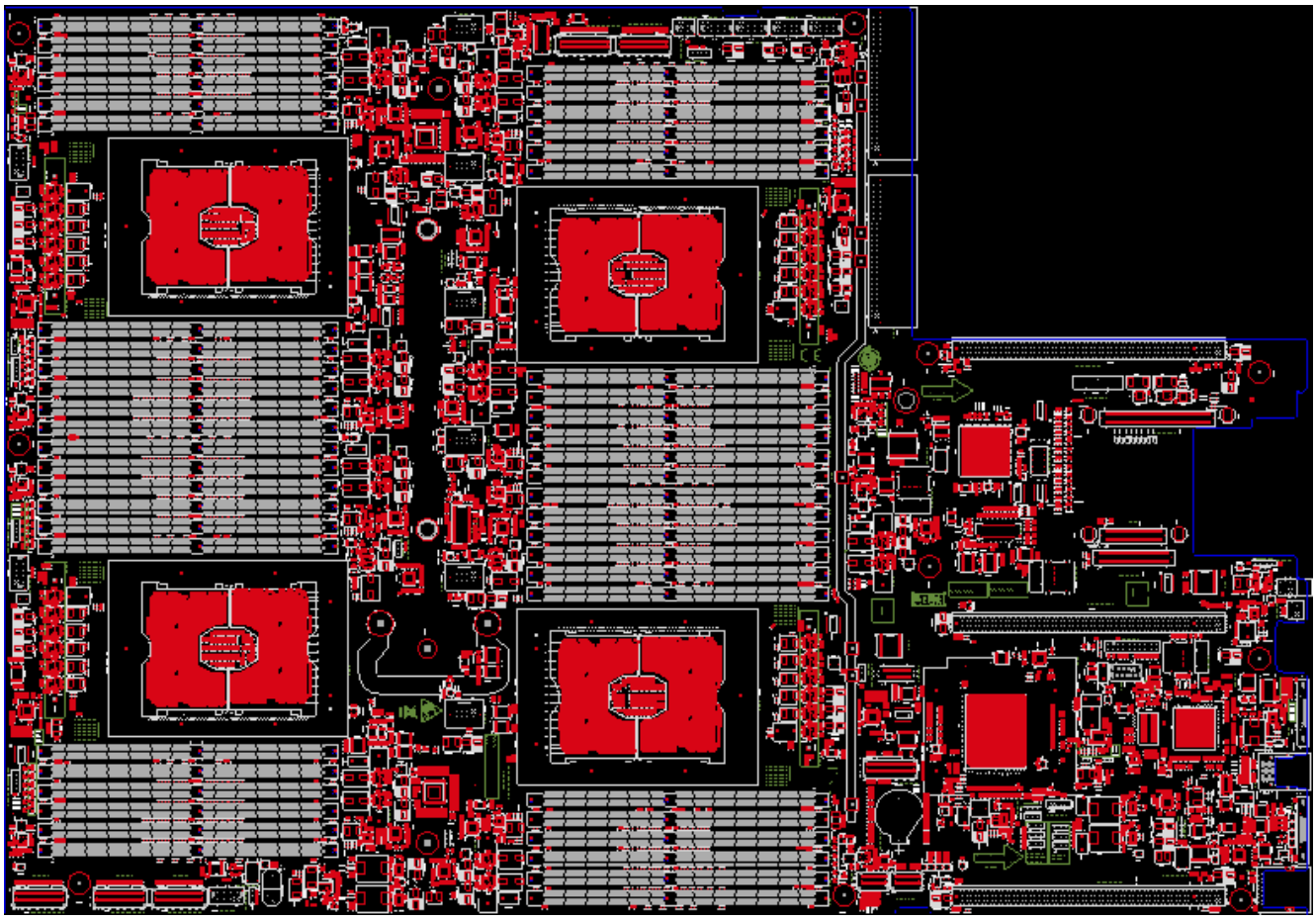


Figure 5-2 Placement

5.3 CPU and Memory

5.3.1 CPU

The motherboard supports all Intel® Cascade Lake -SP processors with TDP up to 205W.

- Support four Cascade Lake-SP processors up to 205W TDP.
- Three full-width Intel UPI links up to 10.4 GT/s/direction for Cascade Lake-SP processor.
- Up to 28 cores per CPU (up to 56 threads with Hyper-Threading Technology).
- Single Processor mode and Two-CPU mode are both supported

5.3.2 DIMM

The motherboard has DIMM subsystem designed as below:

- DDR4 direct attach memory support on CPU0, CPU1, CPU2 and CPU3.
- 6x channels DDR4 registered memory interface on each CPU

- 2x DDR4 slots on each Chanel (total 48x DIMMs)
- Support DDR4 speeds up to 2933MT/s 1DCP, 2666MT/s 2DCP
- Support RDIMMs, LRDIMMs , or 3DS LRDIMMs
- Support SR, DR, QR and 8R DIMMs
- Up to maximum 6144 GB with 128 GB DRAM DIMM
- Follow updated JEDEC DDR4 specification with 288 pin DIMM socket
- Memory support matrix for DDR4 is as Table 5-1

2 Slots Per Channel	
1 DIMM Per Channel	2 DIMM per Channel
2933 MT/s	2666 MT/s

Table 5-1

5.3.3 DCPMM

Board and system design support Intel® Optane™ DC persistent memory with 128G, 256G and 512G. Max, 24 DCPMMs with ADR function.

5.4 PCH

The motherboard uses Intel® Lewisburg chipset, which supports following features:

- 2x rear USB3.0 ports, 1x on board USB3.0 port;
- 1x slimline x4 connector use for SATA 0-3;
- 1x slimline x8 connector use for M.2 Riser Board(PCIe X4 Colay with SATA);
- LPC interface, mux with BMC to enable BMC the capability to perform BIOS upgrade and Recovery
- LPC and SPI interface for TPM header
- SMBUS interface (master & slave)
- Intel® Server Platform Services (SPS) 4.0 Firmware with Intel® Node Manager
- PECI access to CPU
- SMLink0 connect to BMC
- Intel® Manageability Engine (ME) obtain HSC PMBus related information directly.
- Intel® ME SMLink1 connects to Hot swap controller PMBus interface by default.
- BMC connected to HSC PMBus, so it masters HSC PMBus related feature flexibly.

- Temperature sensors reading from BMC
- PCH SKUs
- Board design shall support all PCH SKUs in terms of power delivery and thermal design.

5.5 PCIe Usage

PCIe lanes are configured according to Figure 5-3 and Table 5-2:

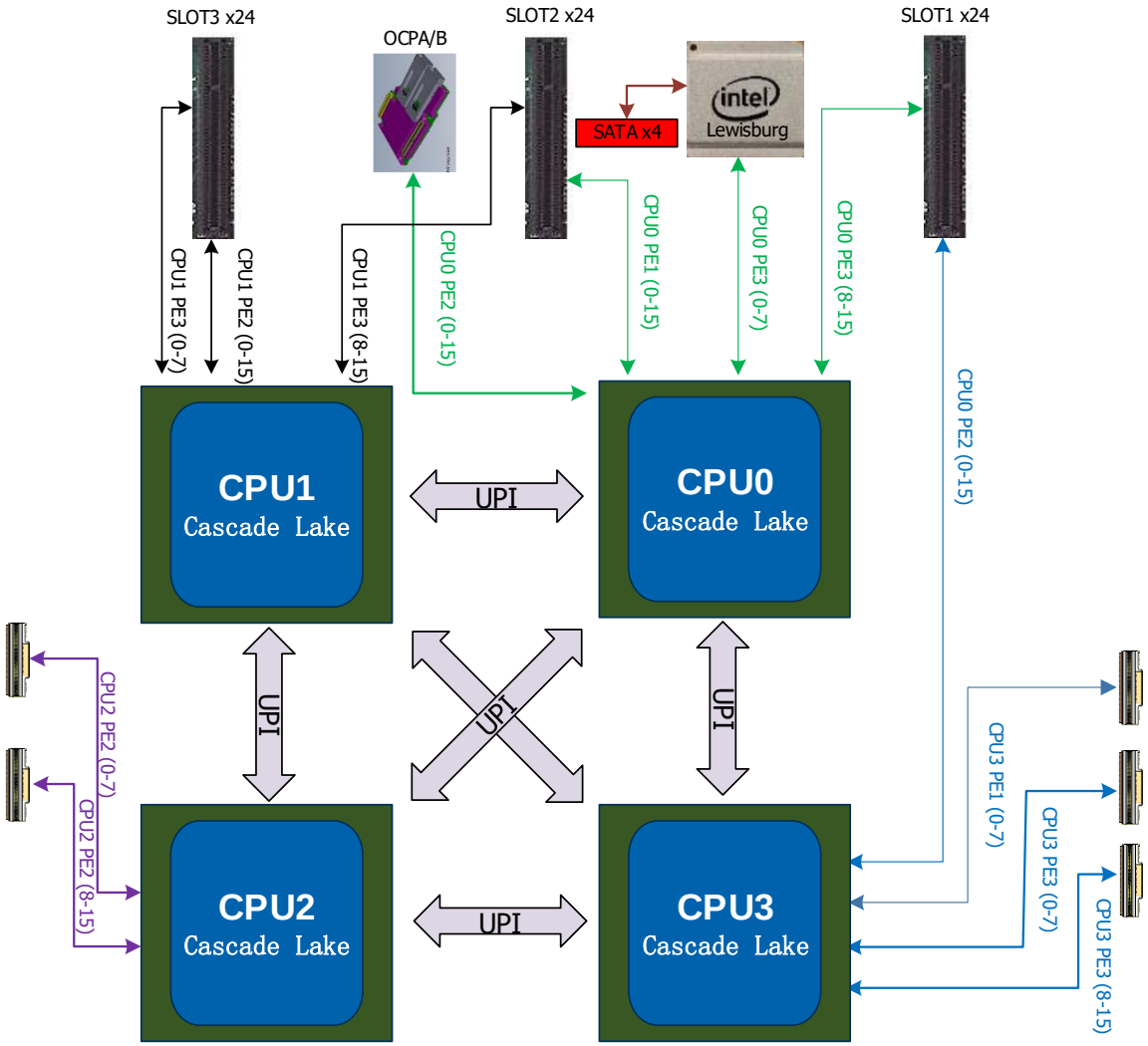


Figure 5-3 PCIe Usage

PCIE Resource Configuration			
CPU0	PE1(Lane0-15)	x16	PCIe Slot2
	PE2(Lane0-15)	2 x8	OCP A/B
	PE3(Lane0-7)	x8	PCH for QAT
	PE3(Lane8-15)	x8	PCIe Slot 1
CPU1	PE2(Lane0-15)	x16	PCIe Slot 3
	PE3(Lane0-7)	x8	PCIe Slot 3
	PE3(Lane8-15)	x8	PCIe Slot 2
CPU2	PE2(Lane0-15)	2 x8	2 x8 Slimline for riser card/GPU
CPU3	PE1(Lane0-7)	x8	x8 Slimline for NVMe
	PE2(Lane0-15)	x16	PCIe Slot 1
	PE3(Lane0-7)	x8	x8 Slimline for NVMe
	PE3(Lane8-15)	x8	x8 Slimline for NVMe

Table 5-2

5.6 MB PCB Stack Up

	Subclass Name	Type	Material	Thickness (MIL)
1		SURFACE	AIR	
2	TOP	CONDUCTOR	COPPER	1.6
3		DIELECTRIC	FR-4	2.705
4	GND02	PLANE	COPPER	1.3
5		DIELECTRIC	FR-4	3
6	ART03	CONDUCTOR	COPPER	1.3
7		DIELECTRIC	FR-4	11.5
8	ART04	CONDUCTOR	COPPER	1.3
9		DIELECTRIC	FR-4	3
10	GND05	PLANE	COPPER	1.3
11		DIELECTRIC	FR-4	3.58
12	ART06	CONDUCTOR	COPPER	1.3
13		DIELECTRIC	FR-4	10
14	POWER07	PLANE	COPPER0.5OZ	2.4
15		DIELECTRIC	FR-4	5
16	POWER08	PLANE	COPPER0.5OZ	2.4
17		DIELECTRIC	FR-4	10
18	ART09	CONDUCTOR	COPPER	1.3
19		DIELECTRIC	FR-4	3.58
20	GND10	PLANE	COPPER	1.3
21		DIELECTRIC	FR-4	3
22	ART11	CONDUCTOR	COPPER	1.3
23		DIELECTRIC	FR-4	11.5
24	ART12	CONDUCTOR	COPPER	1.3
25		DIELECTRIC	FR-4	3
26	GND13	PLANE	COPPER	1.3
27		DIELECTRIC	FR-4	2.705
28	BOTTOM	CONDUCTOR	COPPER	1.6
29		SURFACE	AIR	

Figure 5-4 stack up

6. I/O System

This section describes the motherboard I/O system.

6.1 PCIe x24 Slot

The motherboard has three PCIe x24 slots used by four kinds of PCIe riser cards.

The PCIe lanes to these three PCIe x24 slots are from CPU0, CPU1, and CPU3.

Figure 6-1 illustrates the source of all the three PCIe x24 slots.

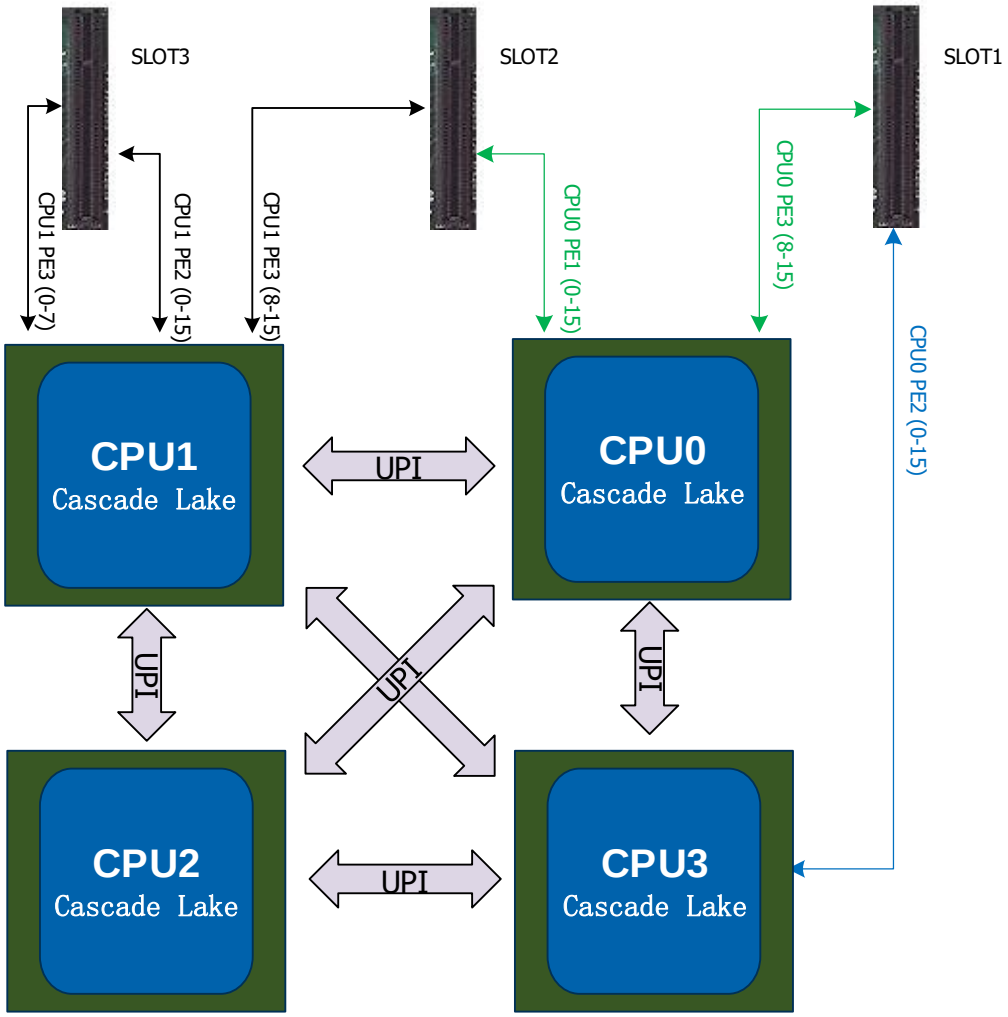
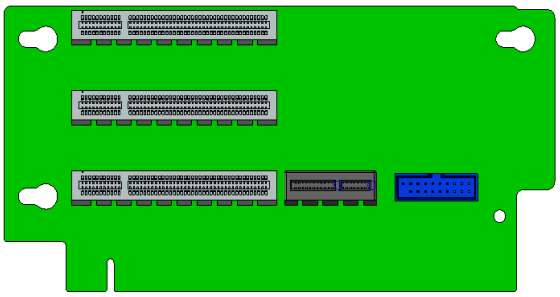


Figure 6-1 PCIe x24 slot

6.2 Riser Card Type

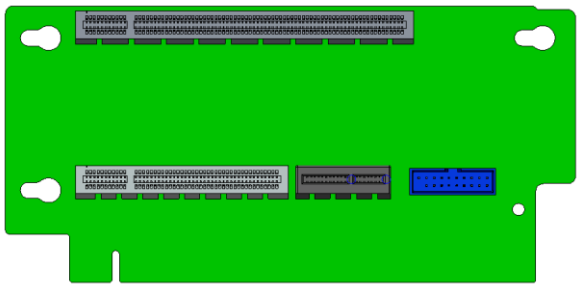
There are four kinds of PCIe riser cards as follow.

6.2.1 3 x8 PCIe riser card 0



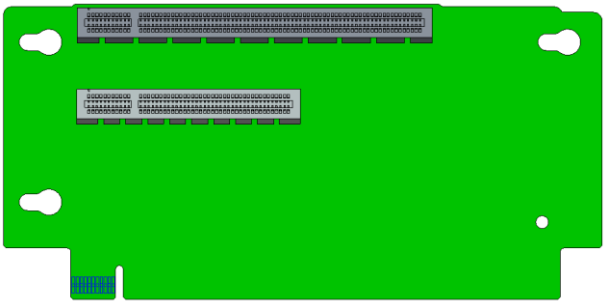
This riser card can support three standard PCIe x8 add-in cards, and it can be used on the PCIe x24 slot 1 and slot 2 of the motherboard.

6.2.2 x16 & x8 PCIe riser card 1



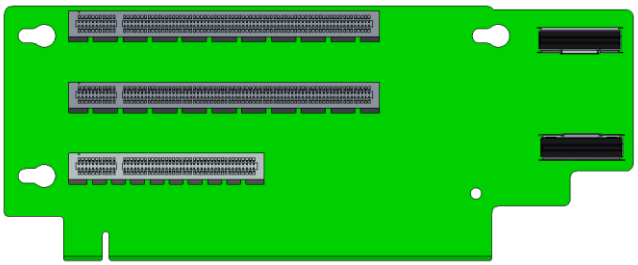
This riser card can support one standard PCIe x8 as well as one PCIe x16 add-in cards, and it can be used on the PCIe x24 slot 1 and slot 2 of the motherboard.

6.2.3 x16 & x8 PCIe riser card 2



This riser card can support one standard PCIe x8 as well as one PCIe x16 add-in cards, and it can be only used on the PCIe x24 slot 3 of the motherboard, according to the setting in BIOS.

6.2.4 2 x16 & x8 PCIe riser card 3



This riser card can support one standard PCIe x8 as well as two PCIe x16 add-in cards, and it can be only used on the PCIe x24 slot 2 of the motherboard, according to the setting in BIOS.

The CPU2's x16 PCIe through two slimline cable connected to Card3. The system has 4 x16 PCIe and they are come from different processor.

6.3 DIMM Slot

Total 48 DIMMs, DIMM 1 are Black, DIMM0 are White.

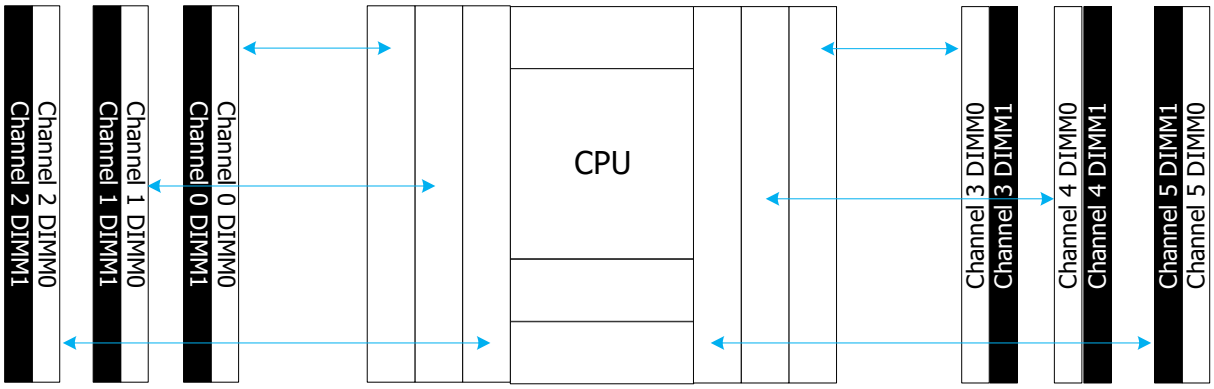


Figure 6-2 DIMM Topology

6.4 PCIe Mezzanine Card

The motherboard support OCP A/C Mezz cards. OCP A card has both Connector A and Connector B, support max PCIe 16x Mezz card.

Connector Pin definition follow the *OCP Mezzanine Card 2.0 rev1.0*

6.5 Network

6.5.1 Data network

Use Single or Dual Port OCP Mezz cards.

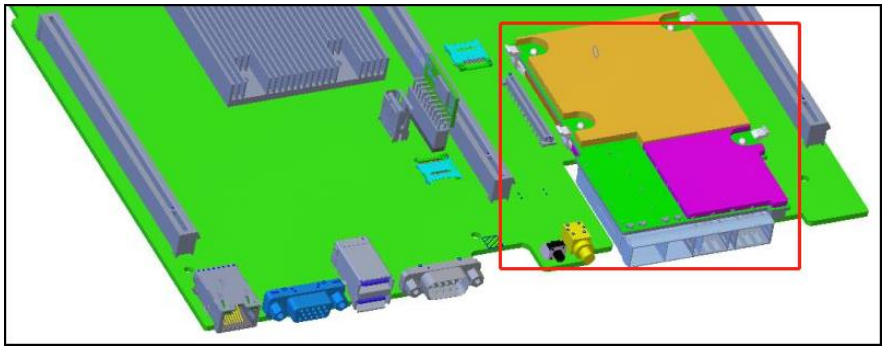
6.5.2 Management network

The motherboard has two options of management network interface for BMC's

connection. Management network shares data network's physical interface. Management connection was independent from data traffic, and OS/driver condition.

a) One dedicated RJ45 port for Board management, driven by BMC through RMII/NC-SI.

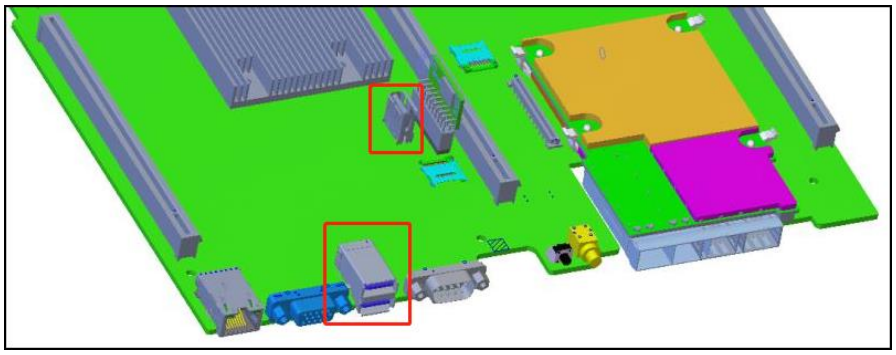
b) One OCP A shared-NIC, driven by BMC through NCSI



6.6 USB

The motherboard has one double ports external USB2.0/3.0 connector located in the rear edge of Motherboard, one single port USB2.0/3.0 connector on the motherboard. BIOS should support following devices on USB ports available on Motherboard:

- USB Keyboard and mouse
- USB flash drive (bootable)
- USB hard drive (bootable)
- USB optical drive (bootable)



6.7 SATA/SAS/NVME

The motherboard can support as many as 24x 2.5" hard disks, combining with three 8-port HDD Backplanes.

6.7.1 4x SATA

The motherboard has Intel® Lewisburg PCH on board, which has a SATA controller that is support 8x SATA 3.0 ports. Four of these ports are connected to a Slimline x4 connector through PCB transmission line, the other end through a cable connected to an Oculink X4 connector on the HDD Backplane.

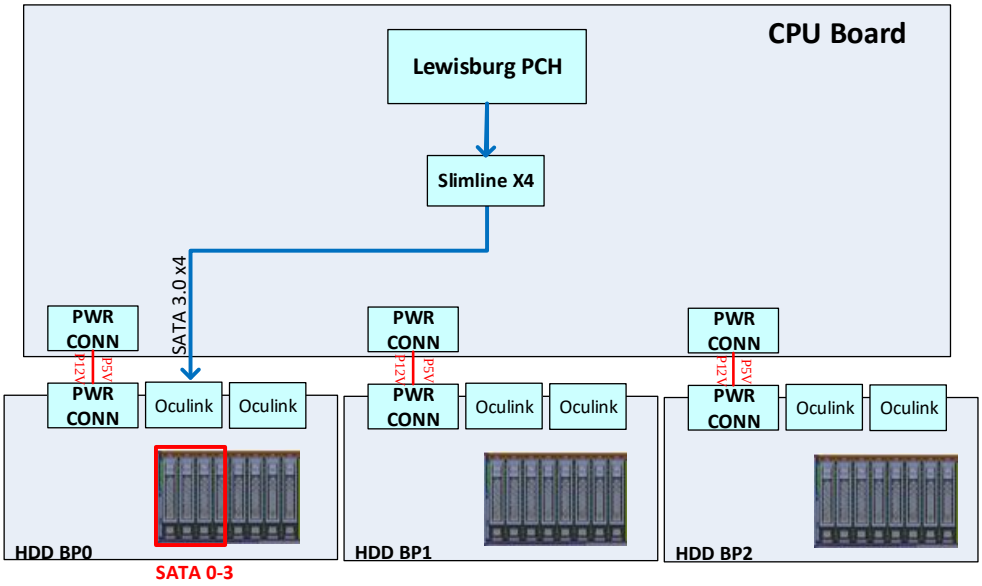


Figure 6-3 4x SATA Topology

6.7.2 24x SAS

Combining with a RAID Card and an SAS Expander Card, the Mother board can support as many as 24 SAS hard disks.

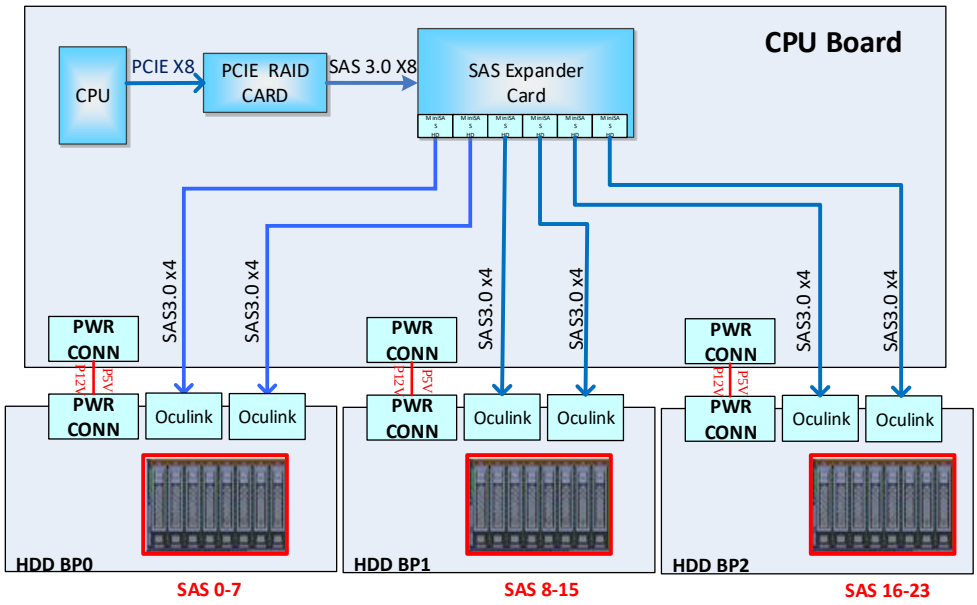


Figure 6-4 24x SAS Topology

6.7.3 6x NVMe

Using three Slimline x8 cables, the Motherboard can support 6 NVMe hard disks.

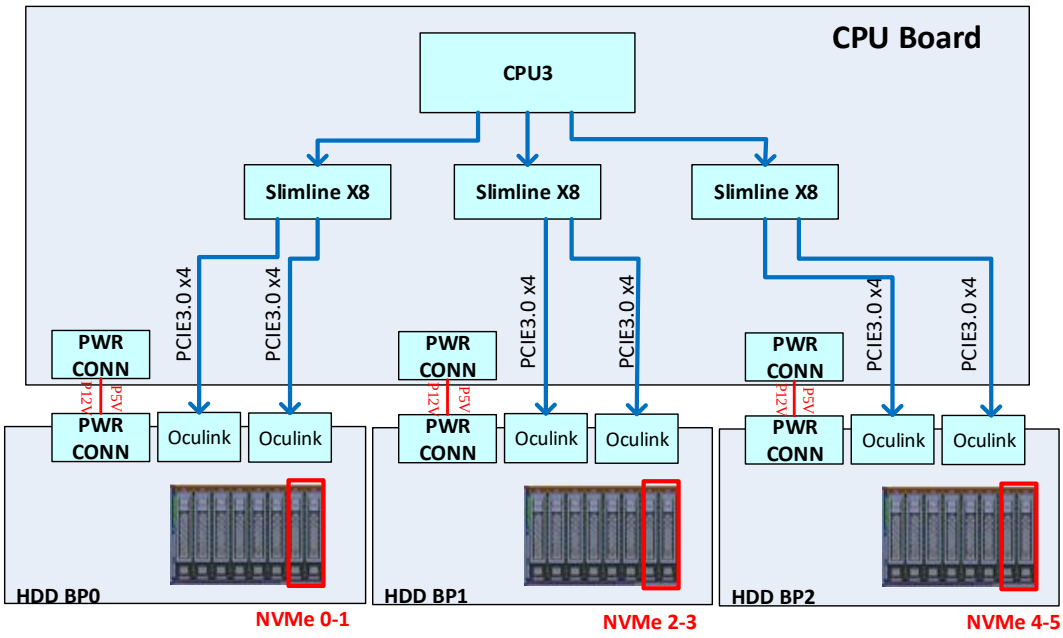


Figure 6-5 6x NVMe Topology

6.8 M.2

Combining with a carrier board, the motherboard supports 2x PCIe/ SATA M.2 devices. The Intel® Lewisburg PCH has 8 PCI express ports muxed with SATA, and four of them are connected through PCB transmission line towards a Slimline x8 connector on the

motherboard, the other end is connected to anther Slimline x8 connector on the M.2 carrier board through a cable.

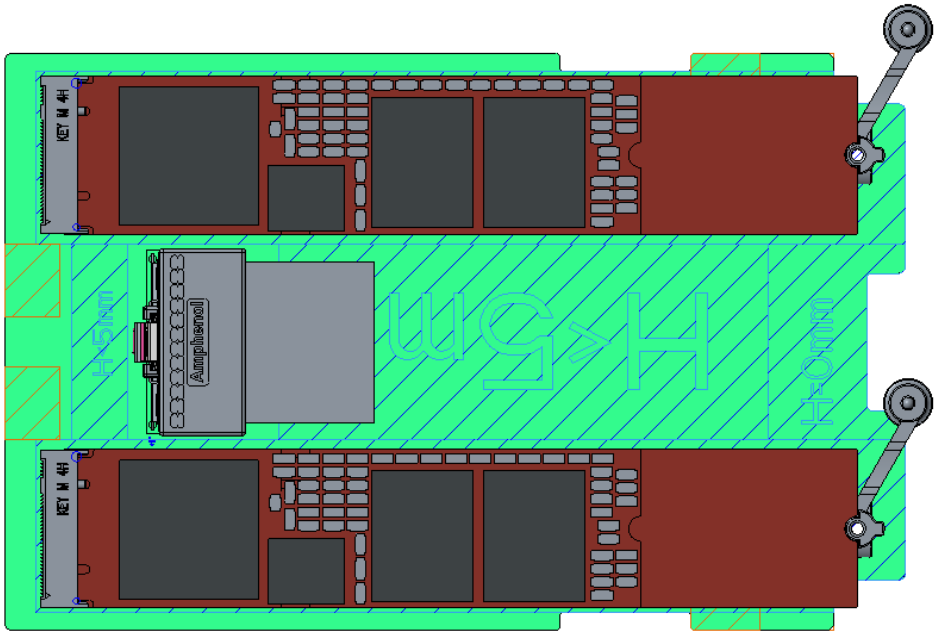


Figure 6-6 M.2 Carrier Board

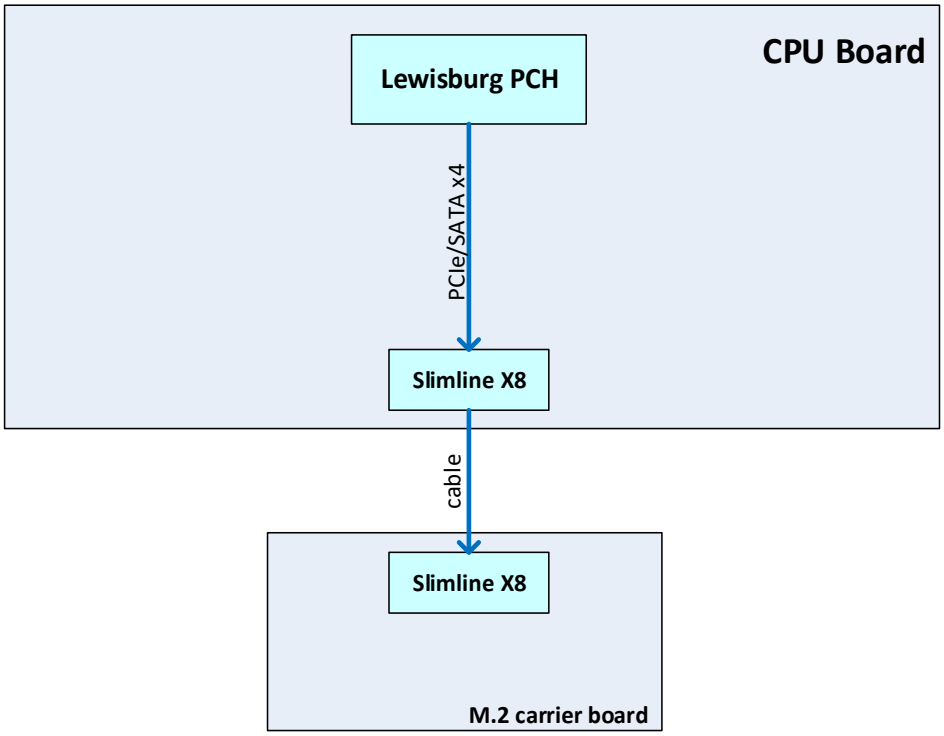


Figure 6-7 M.2 Topology

6.9 Fan

The motherboard holds 6x system FAN connectors. Each FAN has 8 pins, which includes two DC power pins, two GND pins, two TACH pins, one PRESENT pin and one PWM pin. They are used to support dual rotor FAN that shares PWM control signal and PRESENT signal but has separate TACH signal. FAN connector pin definition is listed in Table 6-1, and FAN connector diagram is shown in Figure 6-1. Rated voltage of FAN is 12 VDC, and rated current is 5000 mA/Max, 5750 mA.

Pin	Definition
1	INFAN 12 VDC
2	OUTFAN 12 VDC
3	INFAN GND
4	OUTFAN GND
5	INFAN TACH
6	OUTFAN TACH
7	JUMP TO PIN 3
8	INFAN & OUTFAN PWM

Table 6-1

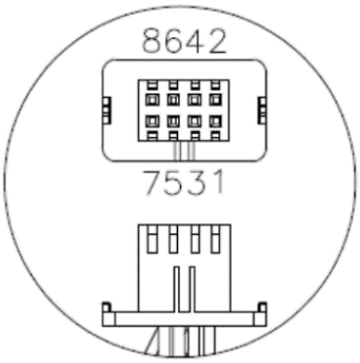


Figure 6-8 FAN connector

6.10 LED

► DIMM offline diagnosis LED: Yellow, LED1-LED48

--Indicating DIMM error, one-to-one match with 48 DIMMs;

--Turn ON, after SW7 is pressed if corresponding DIMM error occurs

►FAN status LED, Red/Green, LED49-LED52 and LED54-LED55

--Indicating FAN status, one-to-one match with 6 FANs;

--When FAN error occurs, Red. When FAN works normally, Green

► BMC FAULT LED: RED, LED53

--When BMC error occurs, Turn ON.

► CPU CATERR LED: RED, LED64

--When CPU CATERR occurs, Turn ON.

► CPU ERR2 LED: RED, LED66

--When CPU ERR2 occurs, Turn ON.

► PCH PWROK LED: Green, LED71

--When PCH core well power rails are powered and stable, Turn ON.

► SYS PWROK LED: Green, LED72

--When System Power is OK, Turn ON.

► BMC Heart Beat LED: Green, LED63

--When BMC is active, blinking.

► PSOC Version LED: Green, LED401-LED403

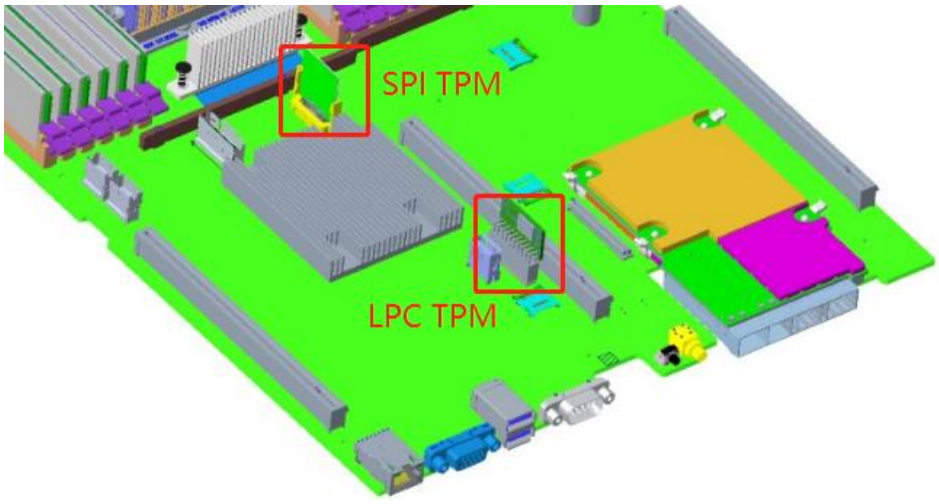
-- Indicating PSOC Version.

► CPLD Version LED: Green, LED59-LED60 and LED73-LED74

-- Indicating CPLD Version.

6.11 TPM

The Motherboard supports one TPM connector with SPI interface, one TPM connector with LPC interface.



6.12 Header

Signal	Description	Location	Default
FM_MFG_MODE	1-2:Enable Manufacture Mode 2-3:Disable Manufacture Mode	J70	Default 2-3
HDA_SDO	1-2:Disable Flash Override 2-3:Enable Flash Override	J72	Default 1-2

FM_ME_RECOVER_N	1-2:Normal 2-3:ME Force Update	J88	Default 1-2
RST_RTCRST_N	1-2:Normal Operation 2-3:Clear CMOS	J89	Default 1-2
FM_PASSWORD_CLEAR_N	1-2:Normal Operation 2-3:Clear Password	J103	Default 1-2
FM_BIOS_TOP_SWAP_SPKR	1-2:Normal Operation and Top Swap Disable 2-3:Recover BIOS and Top Swap Enable	J120	Default 1-2
SMB_HOST_STBY_LVC3_SCL/SDA	For ME Debug	J86	----
SMB_SMLINK2_STBY_LVC3_SCL/SDA	System Management Link 2 SCL/Data	J113	----
INTRUDER_N	Intruder Detect	J57	----
SMBUS6_CPU1_VR_SDA/SCL	SMBUS For CPU1 PVCCIN & PVCCSA VR	J115	----
SMBUS6_CPU2_VR_SDA/SCL	SMBUS For CPU2 PVCCIN & PVCCSA VR	J49	----
SMBUS6_CPU3_VR_SDA/SCL	SMBUS For CPU3 PVCCIN & PVCCSA VR	J65	----
SMBUS6_CPU4_VR_SDA/SCL	SMBUS For CPU4 PVCCIN & PVCCSA VR	J114	----
P5V_HDD_SDA/SCL	SMBUS For P5V_HDD VR	J52	----
P3V3_SDA/SCL	SMBUS For P3V3 VR	J66	----

7. Motherboard Power system

7.1 Open Power budget

Rail	Voltage(V)		CPUn(205W)	DIMM	AEP	Lewisburg-T	NVME SSD	SAS HDD	SYS_Fan	M.2	USB	BMC	PCIE(25W)	CRT	PCIE GPU(300W)	OCPA/B	CPLD	BIOS	CK420	DB1900	TPM	USB2244	Total (A)
IC QTY	IC Qty		4	24	24	1	6	18	6	2	5	1	4	1	4	1	1	1	1	2	1	1	
PVCCIN_CPUn	SVID	1.80	228.00																				912.00
PVCCSA_CPUn	SVID	0.85	16.00																				64.00
PVCCIO_CPUn	SVID	1.00	21.00																				84.00
PVDDQ_XXX	SVID	1.20	17.50	12.00	2.68																		708.00
PVTT_XXX	0.60	0.60		0.30	0.01																		7.20
PVPP_XXX	2.50	2.50	1.20	1.50	0.20																		64.80
P12V_NVDIMM_XXX	12.00	12.00																					
P5V_STBY	5.00	5.00												0.50		2.40							2.90
P3V3_STBY	3.30	3.30	0.08			1.10	0.02					0.40	0.375		0.375	1.60	1.00	0.043			0.05		7.63
P2V5_STBY	2.50	2.50										0.10											0.10
P1V8_STBY	1.80	1.80				1.00						0.10											1.10
P1V2_STBY	1.20	1.20										0.60											0.60
P1V15_STBY	1.15	1.15										0.80											0.80
PVNN_STBY_PCH	SVID	1.00				20.50																	20.50
P1V05_STBY_PCH	1.05	1.05				15.00																	15.00
P12V	12.00	12.00			1.40		2.50	1.50	6.00				2.10		24.25								217.00
P12V_STBY	12.00	12.00														2.40							2.40
P5V	5.00	5.00						1.50			1.00												41.00
P3V3	3.30	3.30								2.50			3.00		3.00	6.40			0.40	0.45		0.20	36.90
Power (max)			205.00	18.33	20.52	29.00	25.00	25.50	72.00	8.25	5.00	3.39	25.00	2.50	300.00	67.20	3.30	0.14	1.32	1.49	0.17	0.66	
			820.00	439.92	492.53	29.00	150.00	459.00	432.00	16.50	25.00	3.39	100.00	2.50	1200.00	67.20	3.30	0.14	1.32	2.97	0.17	0.66	4245.59

Table 7-1 System Power Budget

7.2 Power Simple Topology

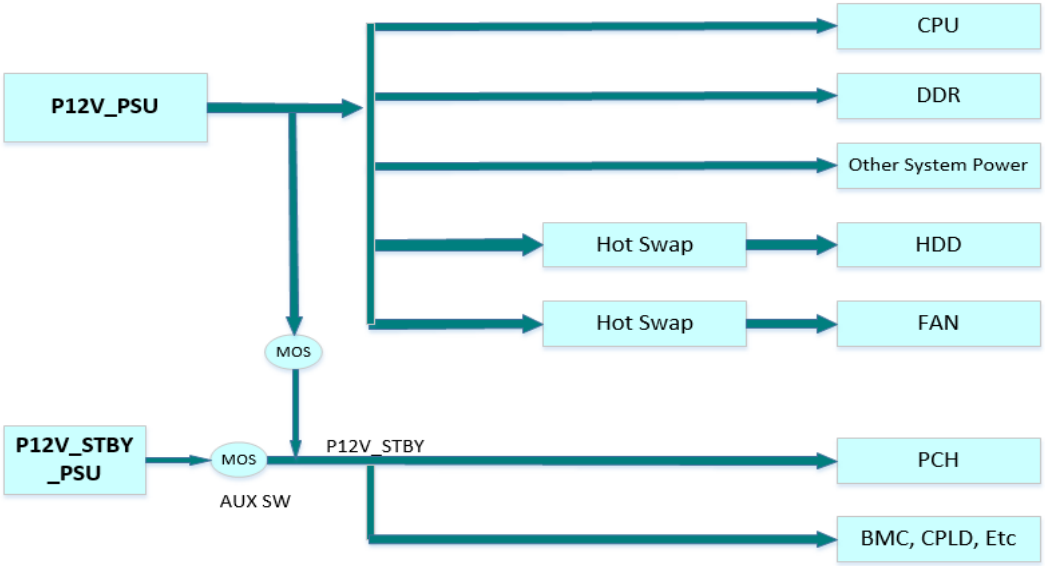


Figure 7-1 power topology

7.3 Input voltage Level

The nominal input voltage delivered by the power supply is 12.2VDC nominal at light loading with a range of 11.4V to 12.6V.

Output Voltage	Vmin	Vnom	Vmax
+12V	+11.80V	+12.20V	+12.6V

Table 7-2 PSU Output Characteristics

7.4 DC-DC Power Design

7.4.1 CPU VR

CPU VR follow latest VR13 SPEC. Using the minimum number of total phases to support the maximum CPU power. CPU VR have auto phase dropping feature, and run at optimized phase count among 1, 2, 3,…, and maximum phase count. CPU VR support all Power States to allow the VRM to operate at its peak efficiency at light loading.

7.4.2 DIMM VR

DIMM VR support auto phase dropping for high efficiency across loading. DIMM VR compliant to latest VR13 specification.

7.4.3 Detail design

Power Rail	VOUT	VIN	VR Type	VR QTY /BRD	VR Controller IC and FET	SMBus Address
PVCCIN_CPU1 PVCCIN_CPU2 PVCCIN_CPU3 PVCCIN_CPU4	SVID	P12V_PSU	Switcher	4	Infineon PXM1610C+6Phase TDA21470；5Phase for PVCCIN_CPU; 1Phase for PVCCSA	CPU1:0X48 CPU2:0X48 CPU3:0X48 CPU4:0X48 With I2C SW
PVCCSA_CPU1 PVCCSA_CPU2 PVCCSA_CPU3 PVCCSA_CPU4	SVID	P12V_PSU	Switcher	4		
PVCCIO_CPU1 PVCCIO_CPU2 PVCCIO_CPU3 PVCCIO_CPU4	SVID	P12V_PSU	Switcher	4	Infineon PXE1110C+1Phase TDA21470	CPU1:0X50 CPU2:0X50 CPU3:0X50 CPU4:0X50 With I2C SW
PVDDQ_ABC PVDDQ_DEF PVDDQ_GHJ PVDDQ_KLM PVDDQ_NPQ PVDDQ_RST PVDDQ_UVW PVDDQ_XYZ	1.2V	P12V_PSU	Switcher	8	Infineon PXM1310C+2Phase TDA21470	PVDDQ_ABC:0XC0 PVDDQ_DEF:0XE4 PVDDQ_GHJ:0XC0 PVDDQ_KLM:0XE4 PVDDQ_NPQ:0XC0 PVDDQ_RST:0XE4 PVDDQ_UVW:0XC0 PVDDQ_XYZ:0XE4
PVTT_ABC PVTT_DEF PVTT_GHJ PVTT_KLM PVTT_NPQ PVTT_RST PVTT_UVW PVTT_XYZ	0.6V	P12V_PSU	Switcher	8	IR3897MTRPBF	
PVPP_ABC PVPP_DEF PVPP_GHJ PVPP_KLM PVPP_NPQ PVPP_RST PVPP_UVW PVPP_XYZ	2.5V	P12V_PSU	Switcher	8	TPS53515RVER	

PVNN_STBY_PCH	0.85V 0.9V 0.95V or 1.0V	P12V_STBY	Switcher	1	IR38263MTRPBF	PVNN:0X80
P1V05_STBY_PCH	1.05V	P12V_STBY	Switcher	1	TPS53353DQPR	
P1V8_STBY	1.8V	P12V_STBY	Switcher	1	MPQ8632GLE-6-Z	
P3V3_STBY	3.3V	P12V_STBY	Switcher	1	TPS53515RVER	
P2V5_STBY	2.5V	P3V3_STBY	LDO	1	TPS74801DRCR	
P1V2_STBY	1.2V	P2V5_STBY	LDO	1	TPS74801DRCR	
P1V15_STBY	1.15V	P12V_STBY	Switcher	1	MPQ8636GLE-4-Z	
P5V_STBY	5.0V	P12V_STBY	Switcher	1	MPQ8632GLE-6-Z	
P12V_FAN	12V	P12V_PSU	Hot Swap	1	VT505BFQX	P12V_FAN:0X82
P12V_HDD	12V	P12V_PSU	Hot Swap	1	VT505BFQX	P12V_HDD:0X8A
P5V_HDD	5.0V	P12V_PSU	Switcher	1	PV3205+2PHASE MP86945	P5V_HDD:0X46
P3V3	12V	P12V_PSU	Switcher	1	PV3205+2PHASE MP86945	P3V3:0X86
P5V	5.0V	P12V_PSU	Switcher	1	TPS53513RVER	

8. BIOS

8.1 BIOS Description

8.1.1 BIOS Chip

The BIOS chip uses PCH's SPI interface through BMC controlled MUX.

Item	Description
Code Base Vendor	AMI AptioV
BIOS Image Size	16MB
ROM Image Size	32MB

8.1.2 BIOS Source Code

BIOS Code based on AMI Purley LightningRidge CRB code, using Intel EDKII software architecture.

8.2 BIOS Features

8.2.1 BIOS Supported Specifications

- Multiprocessor Specification, Version 1.4.
- PCI BIOS Specification, Version 2.1.
- PCI-to-PCI Bridge Architecture Specification, Version 1.2.
- PCI Express Base Specification Version 4.0
- PCI Local Bus Specification Version 3.0
- PCI Firmware Specification Version 3.2
- Advanced Configuration and Power Interface Specification 5.0 or later
- System Management BIOS (SMBIOS) Specification 3.2.0 or later
- Plug and Play BIOS Specification, Revision 1.0A
- PC System Design Guide 2001 - Any conflict occurs between Windows Logo Program System and Device Requirements and, follows Windows Logo Program System and Device Requirements.
- Serial ATA Specification 3.0 or later
- AHCI Specification 1.3
- EDD (BIOS Enhanced Disk Drive) Specification V3.0 Revision 0.8
- Bootable CD-ROM Format Specification, Version 1.0
- TCG EFI Platform Specification
- Functionality and Interface Specification of Cryptographic Support Platform for Trusted Computing (Chinese TCM)
- UEFI Specification 2.3.1 or later
- UEFI PI Specification 1.7 or later
- UEFI SCT 2.3
- NIST 800-147 BIOS Protection Guidelines
- NIST 800-147B BIOS Protection Guidelines for Server
- Intelligent Platform Management Interface Specification V2.0

8.2.2 BIOS Error Handle

The BIOS should support reporting the following POST or error SEL log to BMC and standard RAS feature. From the SEL log, the user may know the specific location of device that the error happens with. And the system could be more reliable with the RAS feature.

- BIOS support IPMI SEL Log
- BIOS support machine check error
- BIOS support DDR4 command/Address parity check
- BIOS support memory mirroring
- BIOS support memory demand/patrol scrubbing
- BIOS support memory rank/multi rank sparing
- BIOS support Intel QPI Clock Fail over
- BIOS support PCI Express Advanced Error Reporting
- BIOS support PCI Express Enhanced Root Port Error Reporting
- BIOS support EMCA gen 2

8.2.3 BIOS Setup Screen

BIOS setup options are included but not limited to the following options:

- BIOS setup support modifying active core numbers

  The BIOS setup shall display the total core numbers and the active core numbers of every CPU. And the user shall be allowed to disable any number of cores supported.

- BIOS setup support enable/disable HT

  Hyper Thread option shall be enabled by default. Only one thread is active if HT is disabled.

- BIOS setup support enable/disable VT-X/VT-D/SR-IOV

  These items shall be enabled if virtualization function is need and could be disabled if not.

- BIOS setup support displaying the L1/L2/L3 cache of CPU

The L1/L2/L3 cache size of CPU should be displayed on the main page of BIOS Setup.

- BIOS setup support enable/disable Turbo Boost

  Turbo Mode opportunistically, and automatically, allows processor cores to run faster than the marked frequency if the physical processor is operating below power, temperature and current specification limits. Turbo Mode can be enabled or disabled by the BIOS and it will increase the performance of workloads.

- BIOS setup support enable/disable P-state (EIST)

  Enhanced Intel Speed Step Technology support shall be controlled by the BIOS. EIST, which offers the capability to support a multitude of processor performance states, allows the processor to dynamically adjust frequency and voltage based on power versus performance needs. EIST should be enabled by default.

- BIOS setup support enable/disable C-state

  Multiple low power idle states (C0/C1/C1E/C6) should be typically implemented by the BIOS. Enable C state could minimize the idle power consumption of the processor. C state may be set disabled by default for the system performance.

- BIOS setup support enable/disable PCIE ASPM

  ASPM operation may be controlled by the BIOS. Optimal power consumption could be obtained if ASPM is enabled, however, some instances of performance impact can be observed.

- BIOS setup support enable/disable PXE boot

  The BIOS should support UEFI and Legacy PXE boot by default and they may be disabled under BIOS setup. PXE will be booted directly if F12 is pressed during the POST process.

- BIOS setup support performance/efficient/custom

  The BIOS is set to performance mode by default. The user may change to efficient mode for power saving or to custom mode under BIOS setup if they want.

8.2.4 SMBIOS

The BIOS shall provide support for the System Management BIOS (SMBIOS) Reference Specification, Version 3.2.0 or later. The BIOS shall implement the following SMBIOS tables:

Type	Structure
0	BIOS Information
1	System Information
2	Base Board Information
3	System Enclosure or Chassis
4	Processor Information
7	Cache Information
8	Port Connector Information
9	System Slots
11	OEM Strings
13	BIOS Language Information
16	Physical Memory Array
17	Memory Device
19	Memory Array Mapped Address
38	IPMI Device Information
39	System Power Supply
41	Onboard Devices Extended Information
127	End-of-Table

8.2.5 Boot

- BIOS Support SAS, SATA and PXE boot.

  The BIOS shall support booting to SAS device, SATA disk or PXE boot option.

- BIOS Support Changing boot priority

  Boot priority shall be changed under BIOS setup and boot option shall be allowed to be disabled or enabled.

- BIOS support modifying BOOT sequence via IPMI commands:

  The sequence of boot option shall be adjusted with IPMI raw or chassis command. This change should be one-time or persistent.

- BIOS support Boot Retry :

  Enable: If there is no bootable device found, BIOS should keep loop searching for bootable device.

  Disable: If there is no bootable device found, BIOS will stop boot and show" Reboot and Select proper Boot device or Insert Boot Media in selected Boot device and press a key".

  BIOS shall support UEFI and legacy boot mode options, and UEFI and legacy boot mode shall have independent boot loop.

8.2.6 BIOS Update

- BIOS support USB Storage Device Recovery

  The BIOS may supporting recovery via a USB storage with a BIOS image in it when the BIOS of the system is corrupted with incomplete functionality.

- BIOS support Update BIOS Image through BMC

  The BIOS shall support being flashed via BMC Web GUI. There may be two upgrade modes, "BIOS+ME" and "BIOS only". And there should be a checkbox of "Keep BIOS Setup Option" for users, so they can choose whether the NVRAM should be cleared.

- BIOS support Update BIOS in UEFI Shell, Windows OS & Linux OS

  The BIOS shall support for flashing BIOS under UEFI Shell, Windows and Linux with AMI AFU tools. And with different parameters, BIOS region, ME region or other region could be flashed separately.

9. BMC

BMC is an independent system of host server system. This independent system has its own processor and memory; The host system can be managed by BMC system even if host hardware or OS hang or went down.

9.1 Main Feature

- Support IPMI 2.0, IPMI Interface include KCS, LAN, IPMB
- Management Protocol,IPMI2.0, HTTPS, SNMP, Smash CLI
- Web GUI
- Redfish
- Management Network Interface, Dedicated/NCSI
- Console Redirection(KVM) and Virtual Media
- Serial Over Lan(SOL)
- Diagnostic Logs, System Event Log (SEL), Blackbox Log, Audit Log
- Hardware watchdog timer, Fans will full speed when BMC no response in 4 mins
- Intel® Intelligent Power Node Manager 4.0 support
- Event Alert, SNMP Trap(v1/v2c/v3), Email Alert and Syslog
- Dual BMC firmware image support
- Storage, Monitor RAID Controller/HDD/Virtual HDD
- Firmware update, BMC/BIOS/CPLD
- Device State Monitor and Diagnostic

9.2 Integrated BMC Hardware

ASPEED AST2500 Baseboard Management Controller, at the center of the server management subsystem is the ASPEED AST2500 integrated Baseboard Management Controller. This device provides support for many platform functions including system video capabilities, legacy Super I/O functions, hardware monitoring functions, and incorporates an ARM1176JZF-S 32-bit RISC CPU microcontroller to host an IPMI 2.0 compliant server management firmware stack.

The following functionality is integrated into the component:

- Baseboard Management Controller (BMC) with peripherals
- Server class Super I/O (SIO)
- Graphics controller
- Remote KVM redirection, USB media redirection, and HW Encryption

The eSPI/LPC interface to the host is used for SIO and BMC communication. The eSPI/LPC Bus interface provides IPMI Compliant KCS and BT interfaces.

The PCI Express interface is mainly used for the graphics controller interface to communicate with the host. The graphics controller is a VGA-compliant controller with 2D hardware acceleration and full bus master support. The graphics controller can support up to 1920x1200 resolution at high refresh rates. The PCI Express interface is also used for BMC messaging to other system devices using MCTP protocol.

The USB 2.0 Hub interface is used for remote keyboard and mouse, and remote storage support. BMC supports various storage devices such as CDROM, DVDROM, CDROM (ISO image), floppy

and USB flash disk. Any of the storage devices can be used as a boot device and the host can boot from this remote media via redirection over the USB interface.

For the main capabilities of the BMC AST2500.BMC provide the 10/100/1000M local RJ45 management connector through RTL8211FD and enable the communication between BMC and OCP A/PCH with NCSI BUS.

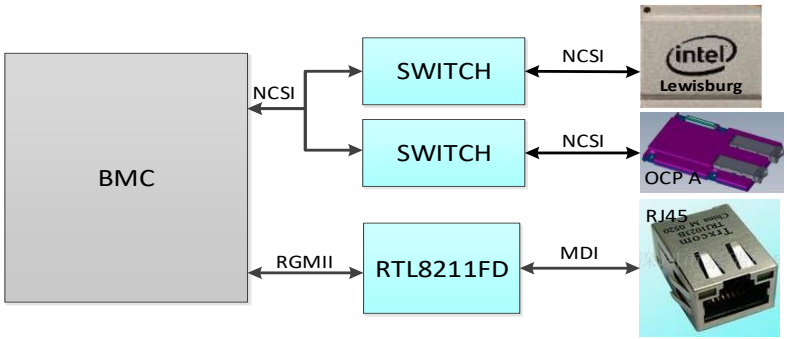


Figure 8-1 BMC managerial network topology

10. Thermal Design Requirements

To meet thermal reliability requirement, the thermal and cooling solution should dissipate heat from the components when system operating at its maximum thermal power. The thermal solution should be found by setting a high power target for initial design in order to avoid redesign of cooling solution; however, the final thermal solution of the system should be most optimized and energy efficient under data center environmental conditions with the lowest capital and operating costs. Thermal solution should not allow any overheating issue for any components in system.

10.1 Data Center Environmental Conditions

The thermal design needs to satisfy the data center operational conditions as described below.

10.1.1 Altitude

Data centers could be located up to 1500 meters above sea level.

10.1.2 Cold-Aisle temperature

Data centers will generally maintain cold aisle temperatures between 18°C and 30°C (65°F to 85°F). The mean temperature in the cold aisle is 24°C with 3°C standard

deviation. The cold aisle temperature in a data center may fluctuate minutely depending to the outside air temperature of data center. Every component in system must be cooled and maintained below its maximum spec temperature in any of cold aisle temperature in a data center.

10.1.3 R.H

Most data centers will maintain the relative humidity to be between 20% and 80%. In the thermal design, the environmental condition changes due to the high altitude may not be considered when the thermal design can meet the requirement with maximum relative humidity, 80%.

10.2 Server operational condition

10.2.1 Inlet Temperature

The inlet air temperature will vary. The normal config can working in the temperature range -5°C ~+35°C. The temperature of all components are not allowed beyond the thermal specification over the validation range 0°C ~+35°C.

10.2.2 Fan Redundancy

The server fans at N+1 redundancy should be sufficient for cooling server components to temperatures below their maximum spec to prevent server shut down or to prevent either CPU or memory throttling.

10.2.3 Thermal Margin

The thermal margin is the difference between the maximum theoretical safe temperature and the actual temperature. The board design operates at an inlet temperature of 35°C (95°F) outside of the system with a minimum 2% thermal margin for every component on the card. Otherwise, the thermal margin for every component in the system is at least 7% for inlet temperature up to 30°C.

10.3 Thermal kit requirements

10.3.1 Heat Sink

The heat sink design should choose to be most optimized design with lowest cost. The heat sink design should be reliable and the most energy efficient design that satisfies all the conditions described above.

For normal config, system use 2U heatsink 4PCS; For GPU config, system use 2U heatsink 2PCS and 1U heatsink 2PCS.

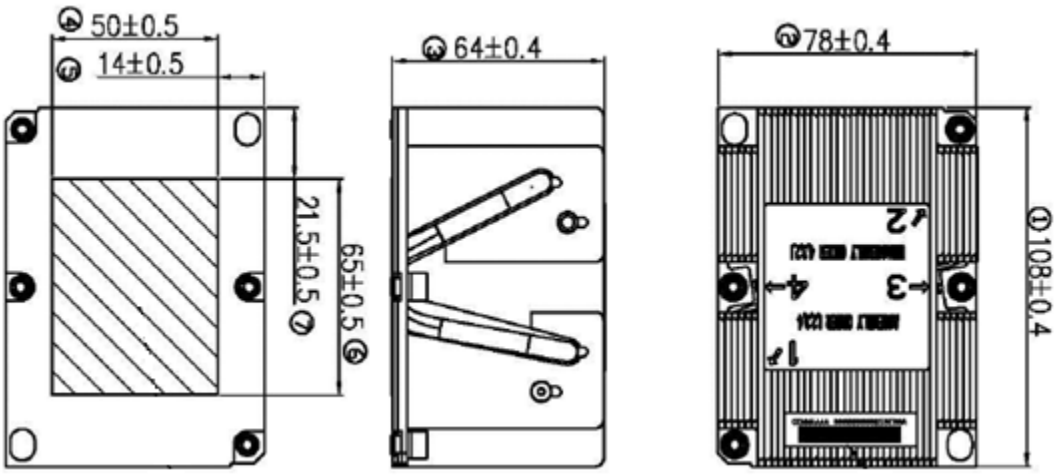


Figure 10-1 2U heatsink

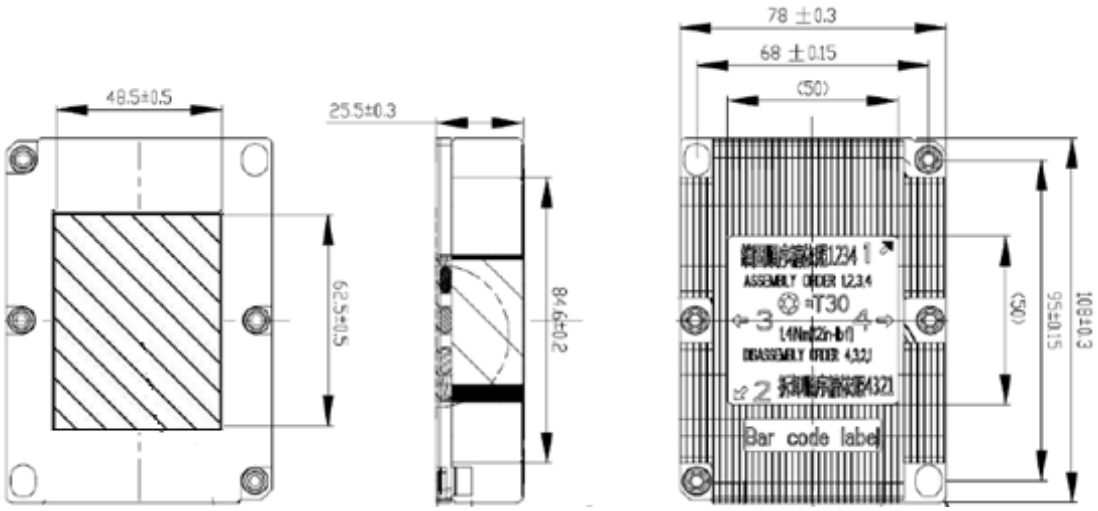


Figure 10-2 1U heatsink

10.3.2 System Fan

The system fan must be highly power-efficient with dual bearing. The propagation of vibration cause by fan rotation should be minimized and limited. The frame size of fan is 60x60x56mm and the quantity of fan is 6PCS. The power supply for fan should use 2 pin P12V to avoid current over spec.

10.3.3 Air-Duct

The air duct needs to be part of the motherboard tray cover, and must be most energy

efficient design. The air-duct design should be simple and easily serviceable. For different config, system can change the air-duct to meet. Using highly green material or reusable material for the air duct is preferred.

10.3.4 Thermal sensor

The maximum allowable tolerance of thermal sensors in the motherboard is ±3°C. Using higher accuracy sensor is preferred.

11. Environmental and Regulations

11.1 Motherboard high altitude

11.1.1 Operational at 1500 meters above sea level

11.1.2 Non-Operational at 12192 meters above sea level

11.2 Motherboard relative humidity

11.2.1 Operating and Storage relative humidity: 10% to 90% (non-condensing)

11.3 Motherboard Temperature

11.3.1 operating temperature range: -5℃to +45℃

11.3.2 Storage temperature range: -40℃ to +70℃

11.3.3 Transportation temperature range: -40℃to +70℃(short-term storage)

11.4 Full system high altitude

11.4.1 Operational at 1500 meters above sea level

11.4.2 Non-Operational at 12192 meters above sea level

11.5 Full system relative humidity

11.5.1 Operating and Storage relative humidity: 10% to 90% (non-condensing)

11.6 Full system Temperature

11.6.1 operating temperature range: -5℃ to +35℃

11.6.2 Storage temperature range: -40℃ to +70℃

11.6.3 Transportation temperature range: -40℃ to +70℃ (short-term storage)

11.7 Full system Vibration & Shock

11.7.1 Operating Vibration:

0.2g acceleration, 5 to 500 Hz, 15minutes per each of the three axes, Transportation temperature range: -40℃to +70℃ (short-term storage)

11.7.2 Non-Operating Vibration:

2.2g acceleration, 5 to 500 Hz, 10minutes per each of the three axes

11.7.3 Operating Shock: 2g, half-sine 11mS, 100 shocks per each of the three axes.

11.7.4 Non-Operating Shock: 25g, 2 shocks per face

12. Mechanical

12.1 External Chassis

2U Rack mount sever in 19-inch rack frame. Chassis form factor: 780mm(D)*435mm(W)*87mm(H)

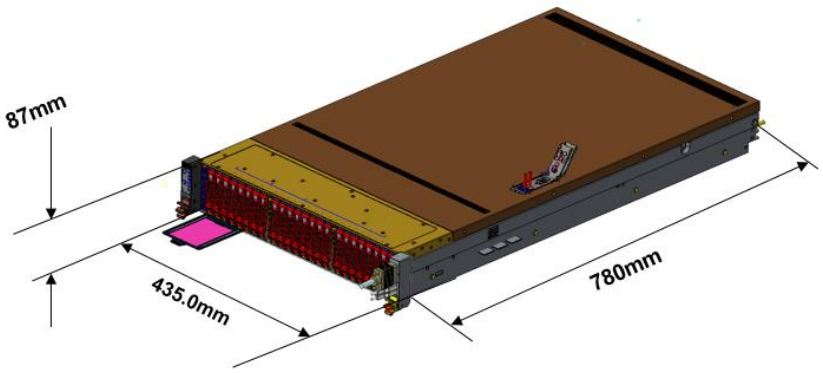


Figure12-1: Chassis Form-Factor

12.2 HDD Carrier

2.5’’ HDD Carrier should be hot-plug.

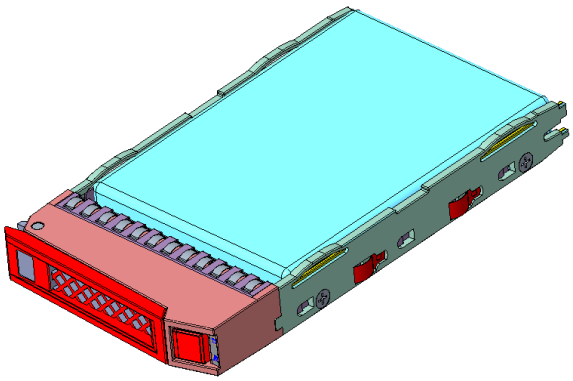


Figure12-2: 2.5’’ Hot-plug HDD Carrier

12.3 Fan Module

Fan module should be hot-plug and convenient for disassembly and assembly.

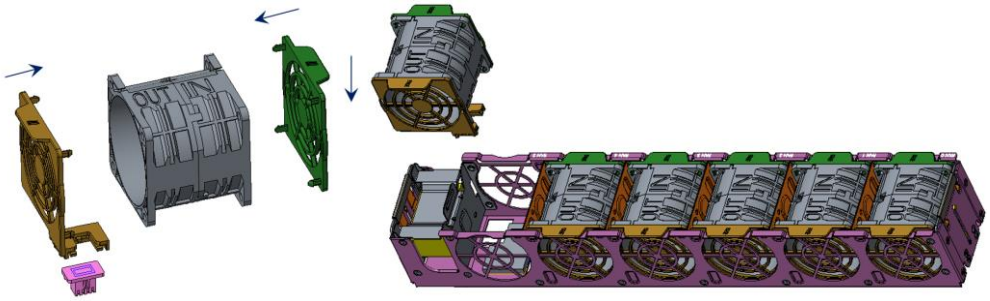


Figure12-3: Fan Module

12.4 PCIE Module

PCIe related designs should follow PCIe specification.
The PCIe needs to be assembled to the PCIe bracket first, and then assembled into the chassis. The PCIe card should be fixed in a relatively simply. Tool-less design is preferred.

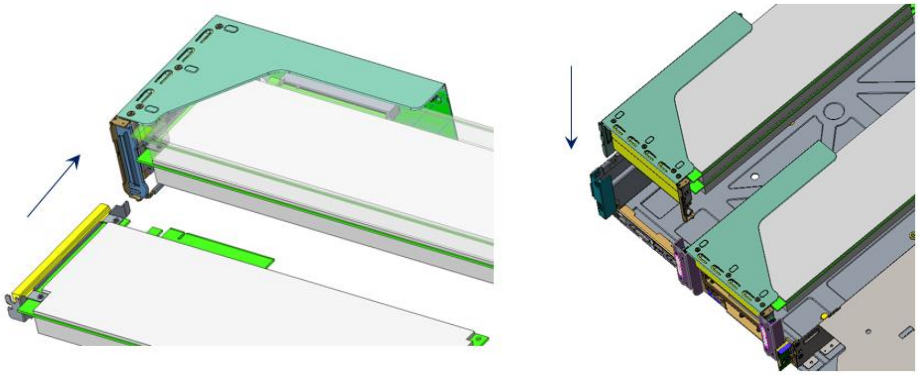


Figure12-4: PCIe Module

12.5 Front View

Up to 24 2.5’’ HDD (3x8) is supported.

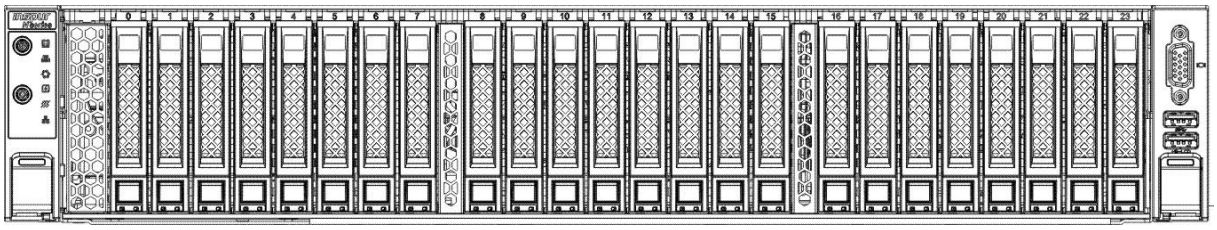


Figure12-5: Front View

12.6 Rear View

8PCIe or 4GPU is supported.

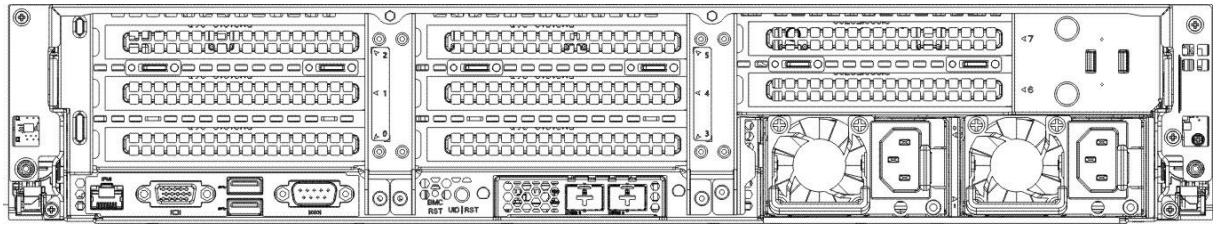


Figure12-6: Rear View-8PCIe

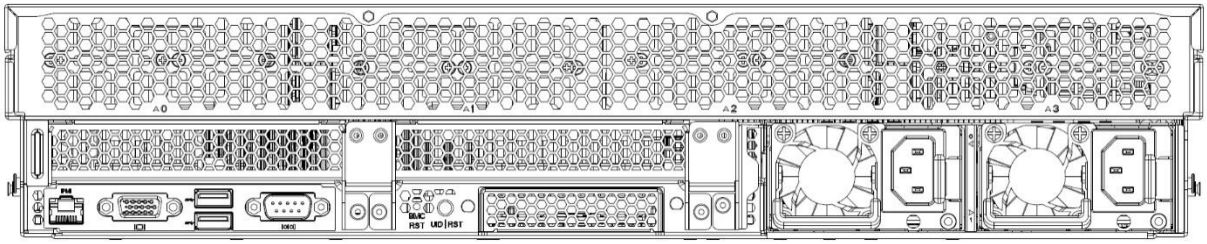


Figure12-7: Rear View-4GPU

13. Labels and Markings

13.1 Labels

The motherboard shall include the labels such as adhesive and silk screen labels on the component side of the motherboard.

13.2 Markings

The motherboard shall include the markings such as adhesive and silk screen markings in accordance with required international certification.

The Crane Mountain shall include the following labels on the component side of the motherboard. The labels shall not be placed in a way that may cause them to disrupt the functionality or the air flow path of system.

Open top panel stickers	Adhesive label	Yes
Component description stickers (rear panel view、motherboard view……)	Adhesive label	Yes
Host nameplate label	Adhesive label	Yes
Carton configuration label	Adhesive label	Yes
The serial number label	Adhesive label	Yes
Certification label (FCC)	Adhesive label	Yes
Remove the protective film label	Adhesive label	Yes
More power supply label	Adhesive label	Yes

14. Deliverables