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ODSA PoC Software development outline

ODSA: Seeds of future silicon innovation

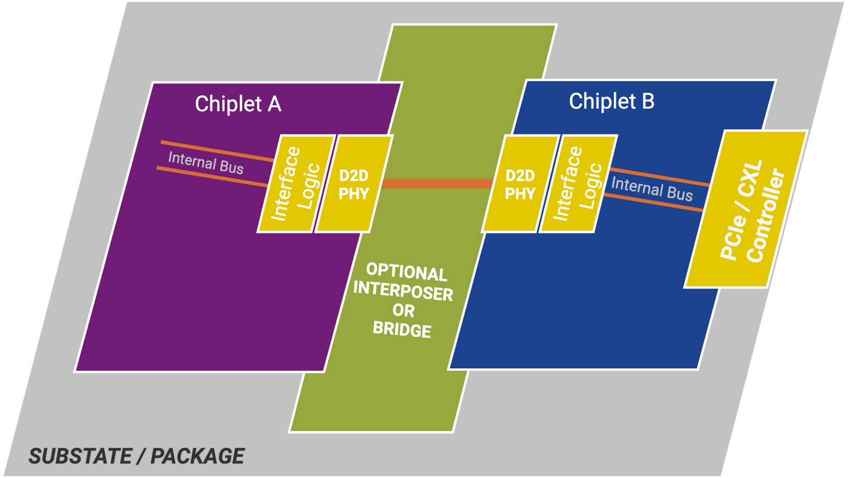
Sharing contributions from ODSA PoC team by Purush Gupta L B

Agenda

- What is PoC?
- PoC Hardware overview
- Software stack for PoC
- Applications being targeted / Use Case
- Long term roadmap
- Call to Action

Background

An open platform to foster inter-chip integration

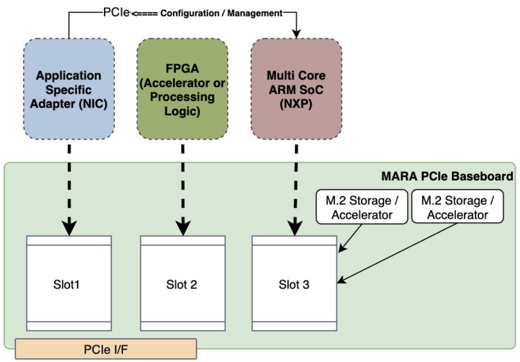


Multiple chiplets need to operate as single functional unit

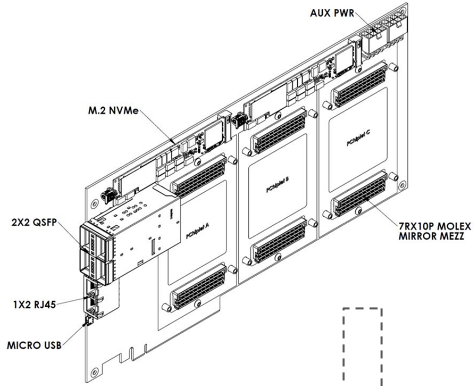
- Open Domain Specific Architecture is an new open definition for Programmable devices optimized for specific applications or class of applications and made of modular pChiplet [collection of die in a single package]

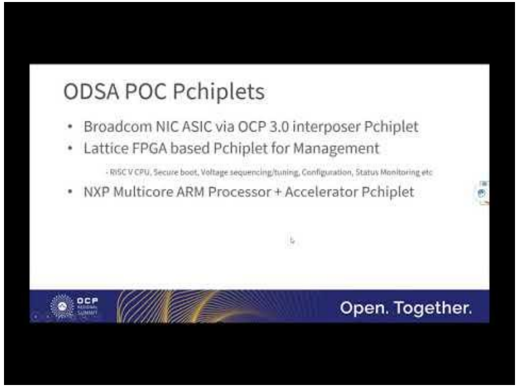
- Goal for ODSA to apply these highly integrated, multi functional devices to meet the demands of high-intensity workloads in the data center/edge/enterprise application – e.g. machine learning, video processing, accelerator, etc

Proof-Of-Concept Hardware



PCIe
<==== Configuration / Management
Application Specific Adapter (NIC)
FPGA (Accelerator or Processing Logic)
Multi Core ARM SoC (NXP)
MARA PCIe Baseboard
M.2 Storage / Accelerator
M.2 Storage / Accelerator
Slot1
Slot 2
Slot 3
PCIe I/F





ODSA POC Pchiplets

- Broadcom NIC ASIC via OCP 3.0 interposer Pchiplet
- Lattice FPGA based Pchiplet for Management
  - RISC V CPU, Secure boot, Voltage sequencing/tuning, Configuration, Status Monitoring etc
- NXP Multicore ARM Processor + Accelerator Pchiplet

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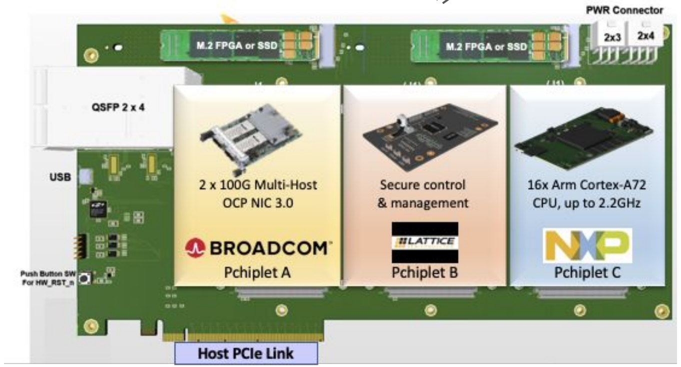
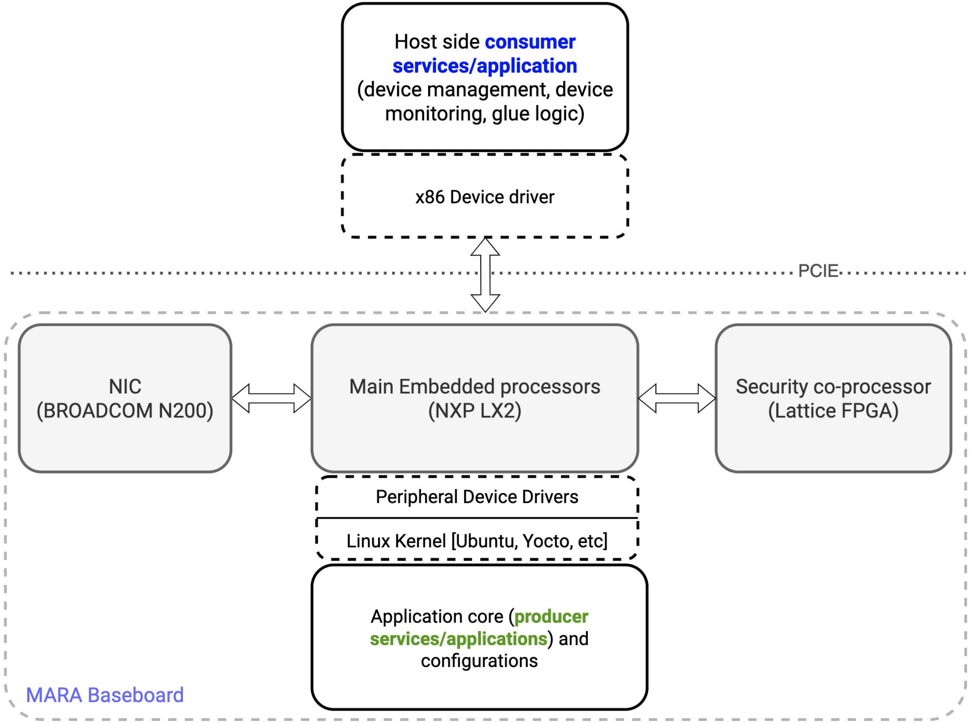


Proof-Of-Concept Software Stack


Host side consumer services/application (device management, device monitoring, glue logic)
x86 Device driver
PCIE
NIC (BROADCOM N200)
Main Embedded processors (NXP LX2)
Security co-processor (Lattice FPGA)
Peripheral Device Drivers
Linux Kernel [Ubuntu, Yocto, etc]
Application core (producer services/applications) and configurations
MARA Baseboard

- **Kernel/Bootloader** for the embedded processor
- **Peripheral Device Drivers:** The main SOC needs to communicate and interact with various IP subsystems part of other PChiplets
- **Host Device Drivers:** The Platform host device drivers interface needs to be lightweight and should available for most devices.
- **Application:** In the end applications make or break the platform and test the capabilities of the frameworks. Fortunately we have identified quite a few that can highlight the unique capabilities

Proof-Of-Concept Applications/Use-cases

Use-cases	Demo highlight
Network traffic management	Demonstrate ability to pipe traffic directed to x86 to the NXP-LX2 and potentially scan for malicious packets
FTP (Data Transfer Node: DoE Content Distribution	Build an dedicated FTP client/appliance that can be used to stage/accelerate the traffic between two network connections
Computational Storage + OVS Offload	Demonstrate a computational storage controller
NVMe + RoCE Demonstrator	Demonstrate a NVMeOF Target controller
HCI Controller	Demonstrate encapsulation of the storage and networking components to host system in a direct attached or network attached configuration.

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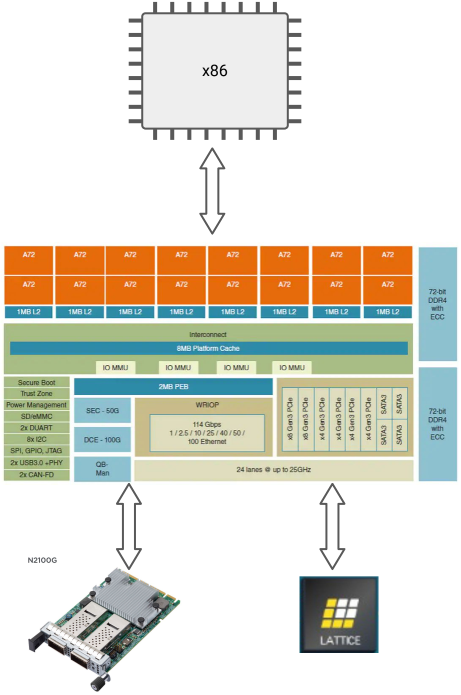
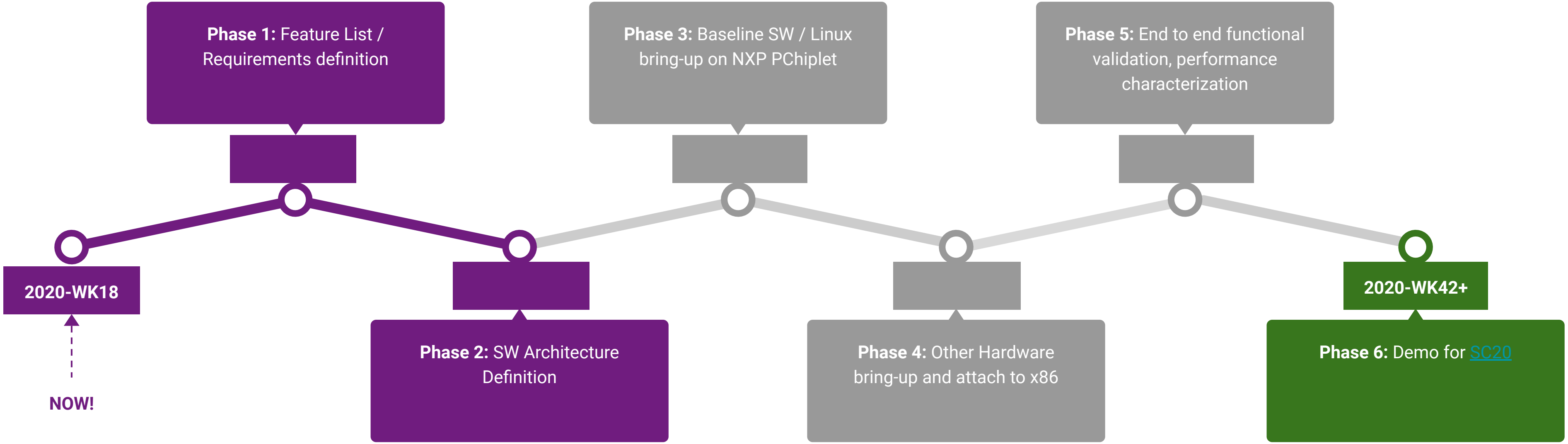
Proof-Of-Concept Bring up plan



Credit:
(1) NXP refer to source
(2) Broadcom refer to source
(3) Lattice refer to source

1. **Kernel / Bootloader**
   a. Start with NXP LX2 open source Layerscape SDK (LSDK)
   b. Update the DTS
   c. Configure the bootloader, Kernel with appropriate modules and enable trusted firmware
2. **Peripheral Device Drivers**
   a. Review the portability of the drivers for the peer adapters so they can enumerate under ARM (NXP LX2)
   b. Exercise the interfaces to validate the functionality
3. **Host Device Drivers**
   a. Review enumeration of the devices on the x86 host
4. **Application**
   a. Review the libraries required to stitch the application

Proof-Of-Concept SW Milestones



2020-WK18

NOW!

Phase 1: Feature List / Requirements definition

Phase 2: SW Architecture Definition

Phase 3: Baseline SW / Linux bring-up on NXP PChiplet

Phase 4: Other Hardware bring-up and attach to x86

Phase 5: End to end functional validation, performance characterization

Phase 6: Demo for SC20

2020-WK42+

* Tentative proposal based on volunteers availability/commitments. We need help on every stage of this project!

Call for action

TEAMWORK
"Great things are done by a series of small things brought together."
Vincent Van Gogh

- Looking for teams and individuals who are passionate about new HW, FW and SW concepts and participate in paradigm shifts on how Silicon is integrated and deployed.
- In need of Kernel, device-driver, hardware debug folks with lots of curiosity, eagerness to help
- We welcome varied experiences, perspectives and vision to make this a reality! Please join and spread the word.