

Revision History		Date
0.1	X00 start.	Sep. 20, 2015
1.1	PCB Part Number : 2976927201 Add EMI solution, page 86~89	Feb. 1, 2016

Page Descriptions
01-01_History
01-02_Block Diagram
01-03_Power Consumption
01-04_I2C Tree
01-05_PWR [5V & 2V5 & 3V3A]
01-06_PWR [MAC AVS-1]
01-07_PWR [MAC AVS-2]
01-08_PWR [3V3 & 1V8]_1
01-09_PWR [3V3 & 1V8]_2
01-10_PWR [PHY 1V0 & MAC 1V]_1
01-11_PWR [PHY 1V0 & MAC 1V]_2
01-12_PWR [PHY 1V0A]_3
01-13_PWR [PHY 1V0A]_4
01-14_PWR [CT 1V9]_1
01-15_PWR [CT 1V9]_2
01-16_12V PWR CONN & HOT SWAP
01-17_CLK [25M_156.25M]
01-18_CLK [PHY_156.25M]
01-19_MasterCPLD- LCMXO2-1200
01-20_BCM56864 [MISC_WC28-31]
01-21_BCM56864 [WC0-27]
01-22_BCM56864 [PWR1]
01-23_BCM56864 [PWR2]
01-24_BCM56864 [PWR3]
01-25_BCM56864 [GND]
01-26_Block_PHY 1-6 [L]
01-27_Block_PHY 7-12 [R]
01-28_PHY MISC
01-29_Block_10G RJ-45 [P1-P24]
01-30_Block_10G RJ-45 [P25-P48]
01-31_Block_QSFP+ [P1-P6]
01-32_Port LED decode
01-33_USB& Thermal
01-34_FAN CONN/MGMT/ResetButton
01-35_CPU-Board-IF Connector
01-36_10GBT_LED Array
01-37_QSFP+_LED Array
02-01_BCM84858_PHY_A
02-02_BCM84858_PHY_B
02-03_BCM84858_PHY_C
02-04_BCM84858_PHY_D
03-01_10GBT_RJ-45_2x6
04-01_QSFP CAGE 2x3

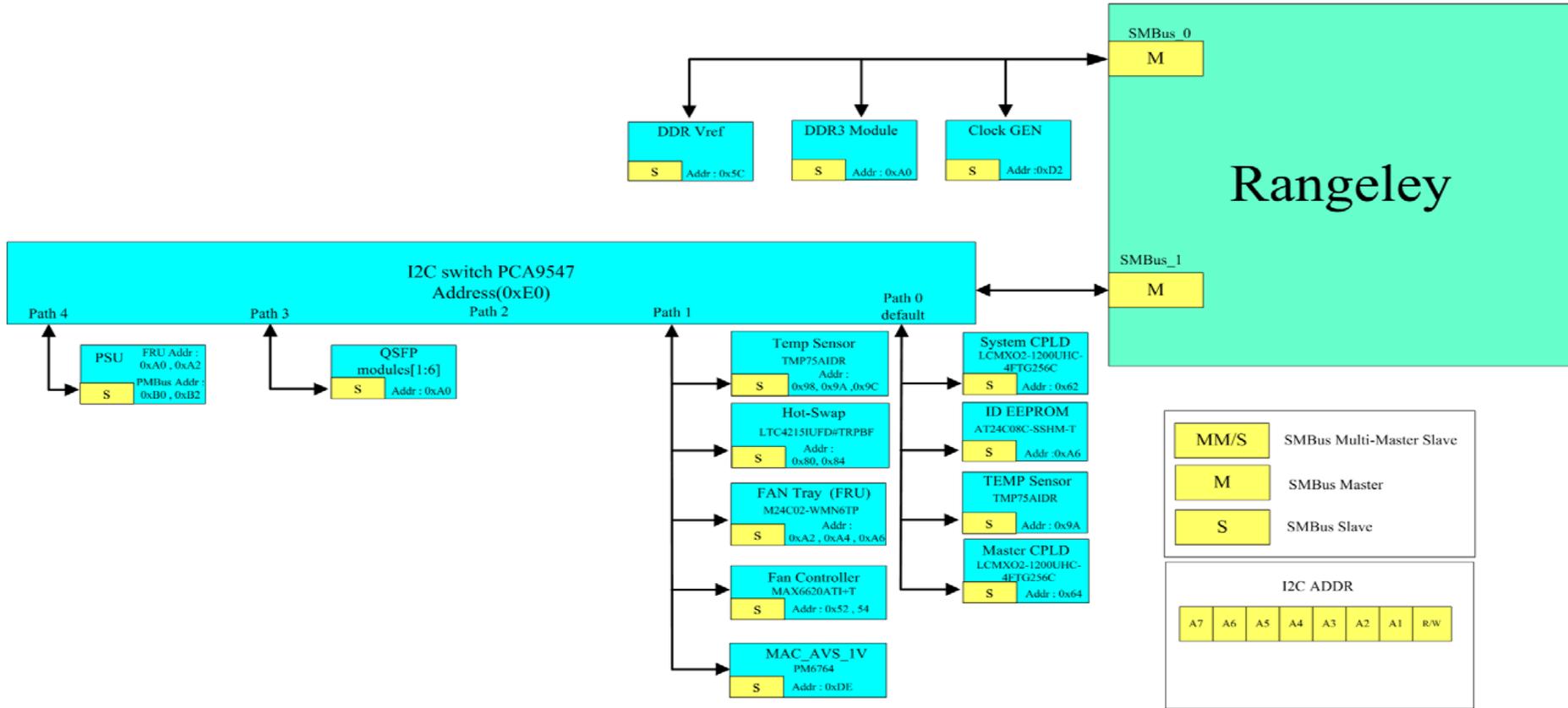
- Note:**
- 1.All of resistors are 5%, 0603 SMD except other specified description.
 - 2.All of capacitors are 50V except other specified description.
 - 3.All of aluminous capacitors are 105 degree C except other specified description.
 4. # for LOW active signals(name#)

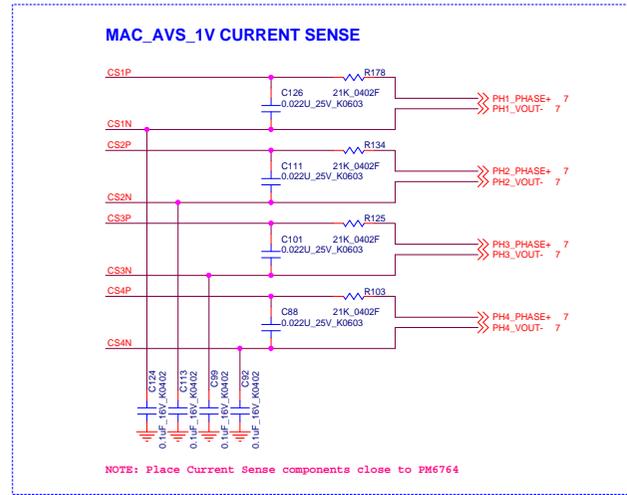
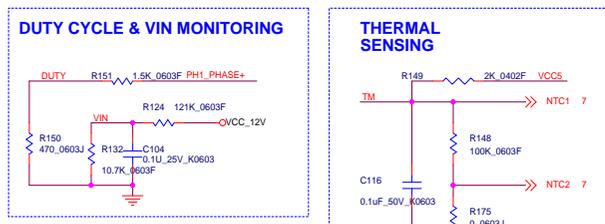
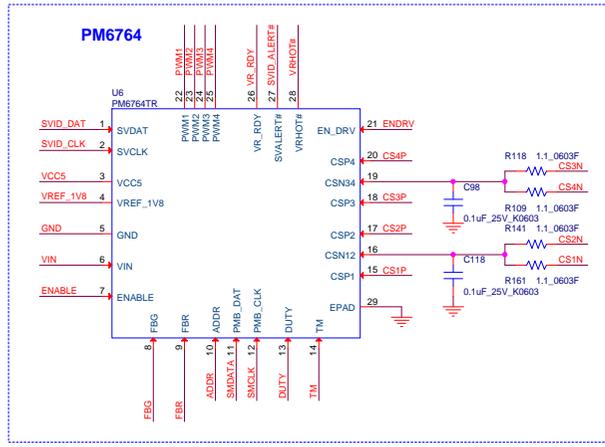
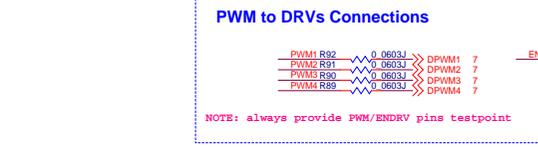
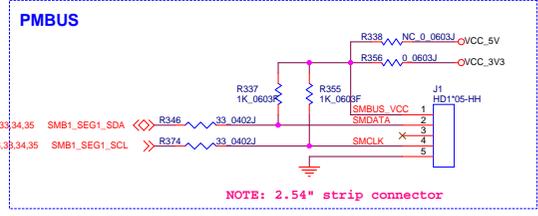
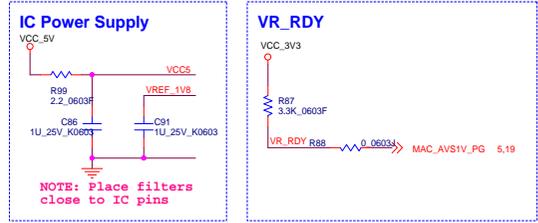
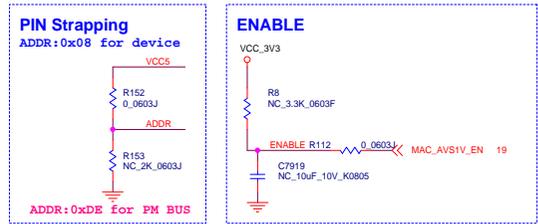
SCHEMATICS OF	FILE NAME	DRAWN	DESIGNED	CHECKED	APPROVED

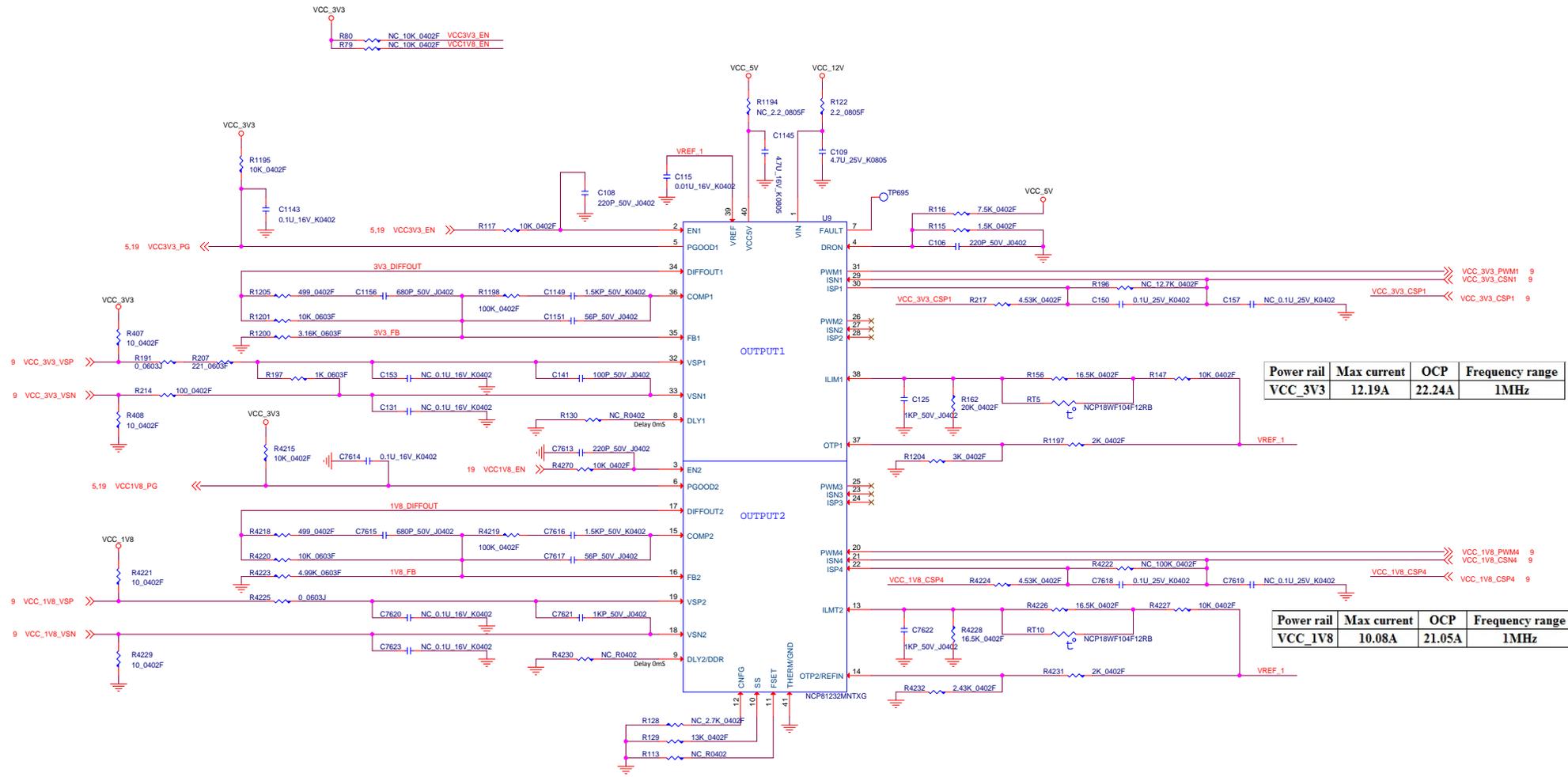
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File		01-01_History	
Size	Document Number	Rev	
C	1ADSS-0XXXXX	1.1	
Date:	Tuesday, September 13, 2016	Sheet	1 of 80







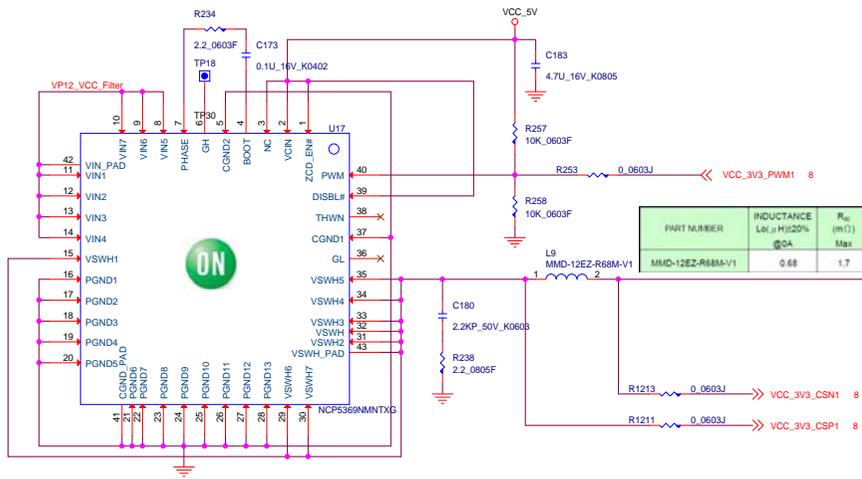
Power rail	Max current	OCp	Frequency range
VCC_3V3	12.19A	22.24A	1MHz

Power rail	Max current	OCp	Frequency range
VCC_1V8	10.08A	21.05A	1MHz

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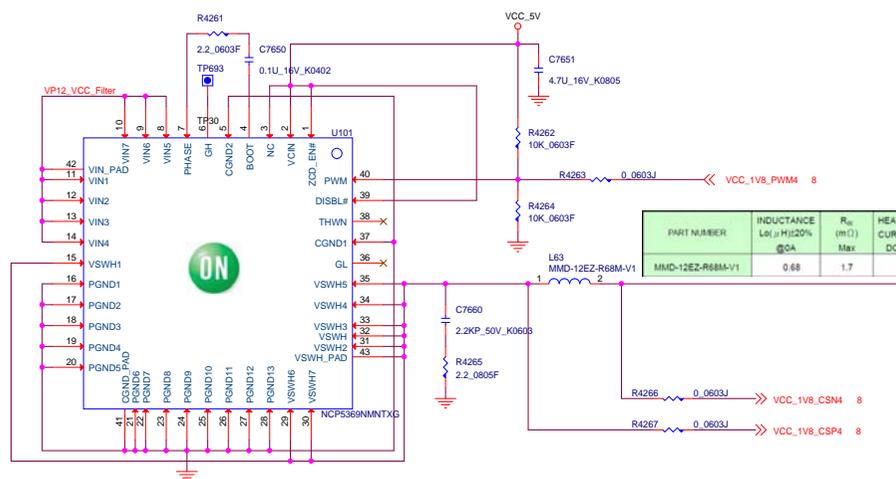
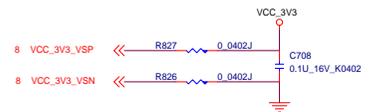
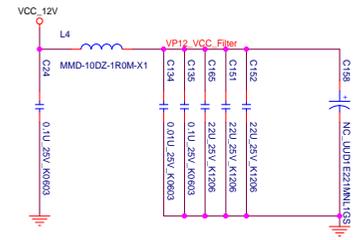
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File	01-08_PWR [3V3 & 1V8]_1		
Size	Document Number		Rev
C	1ADSS-0XXXX		1.1
Date:	Tuesday, September 13, 2016	Sheet	8 of 80



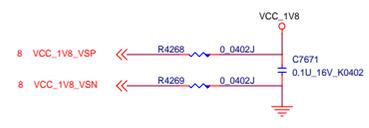
PART NUMBER	INDUCTANCE L ₅ (μH) ±20% @0A	R _{DC} (mΩ) Max	HEAT RATING CURRENT I _{DC} (A) DC AMPS ¹	SATURATION CURRENT I _{sat} (A) DC AMPS
MMD-12EZ-R68M-V1	0.68	1.7	34	54

Power rail	Max current	OCF	Frequency range
VCC_3V3	12.19A	22.24A	1MHz



PART NUMBER	INDUCTANCE L ₆₃ (μH) ±20% @0A	R _{DC} (mΩ) Max	HEAT RATING CURRENT I _{DC} (A) DC AMPS ¹	SATURATION CURRENT I _{sat} (A) DC AMPS
MMD-12EZ-R68M-V1	0.68	1.7	34	54

Power rail	Max current	OCF	Frequency range
VCC_1V8	10.08A	21.05A	1MHz

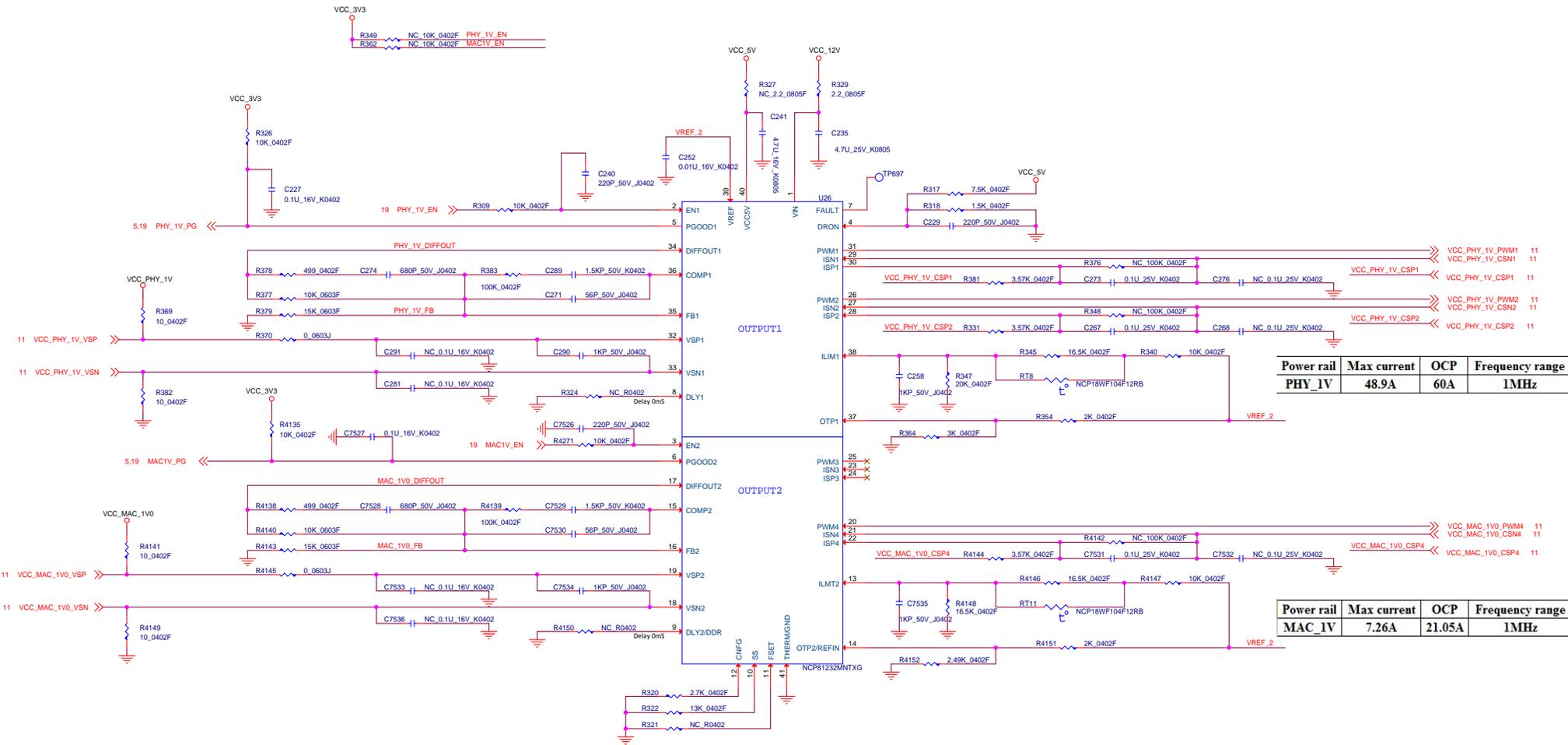


65VPS20R
CAP AL 3P 6.3V 820uF M 10*10.3 5HD TP

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File	01-09_PWR [3V3 & 1V8] 2	
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Date:	Tuesday, September 13, 2016	Sheet 8 of 80



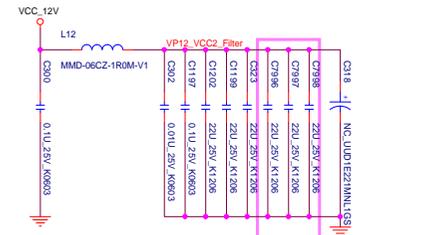
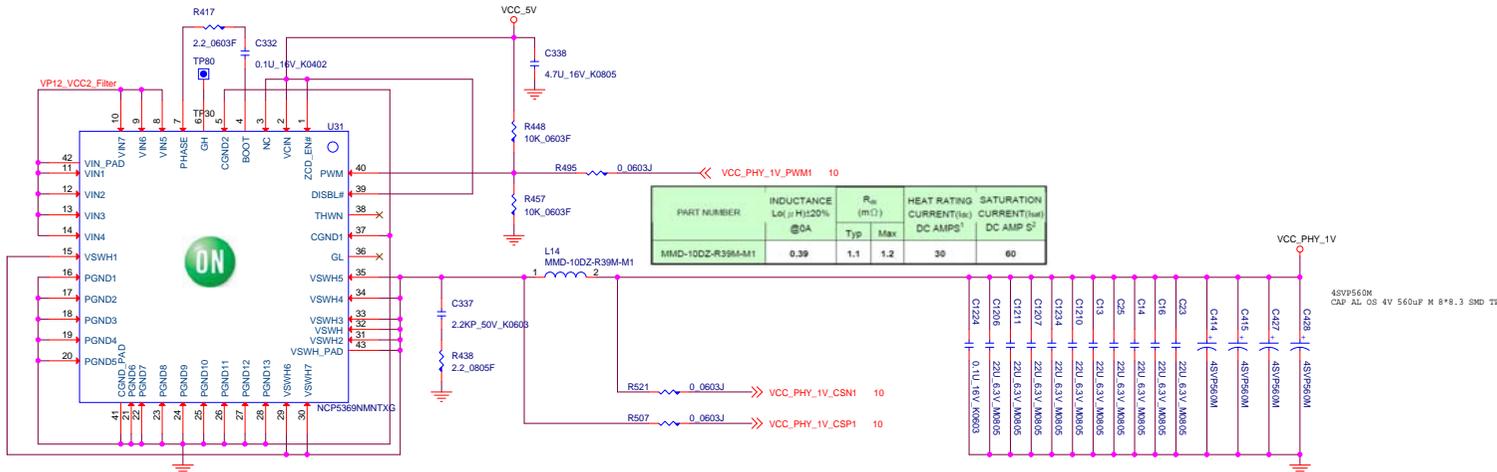
Power rail	Max current	OCF	Frequency range
PHY_1V	48.9A	60A	1MHz

Power rail	Max current	OCF	Frequency range
MAC_1V	7.26A	21.05A	1MHz

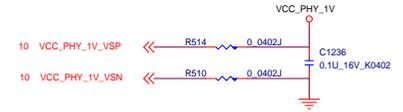
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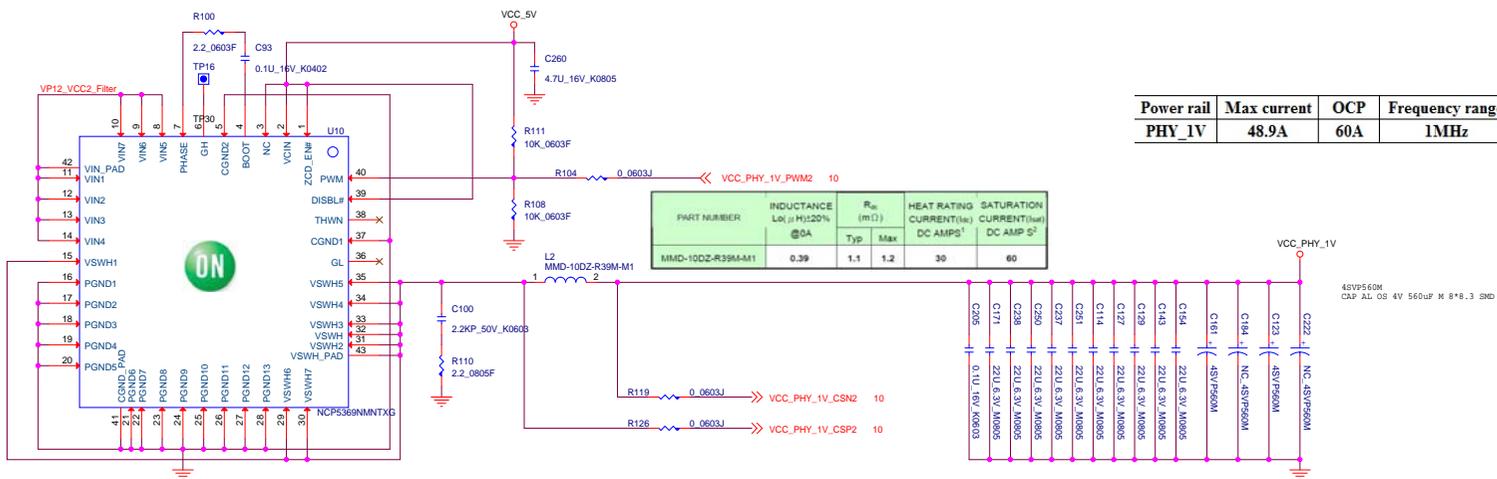
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01-10_PWR [PHY 1V0 & MAC 1V]_1			
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Date:	Tuesday, September 13, 2016	Sheet	10 of 80



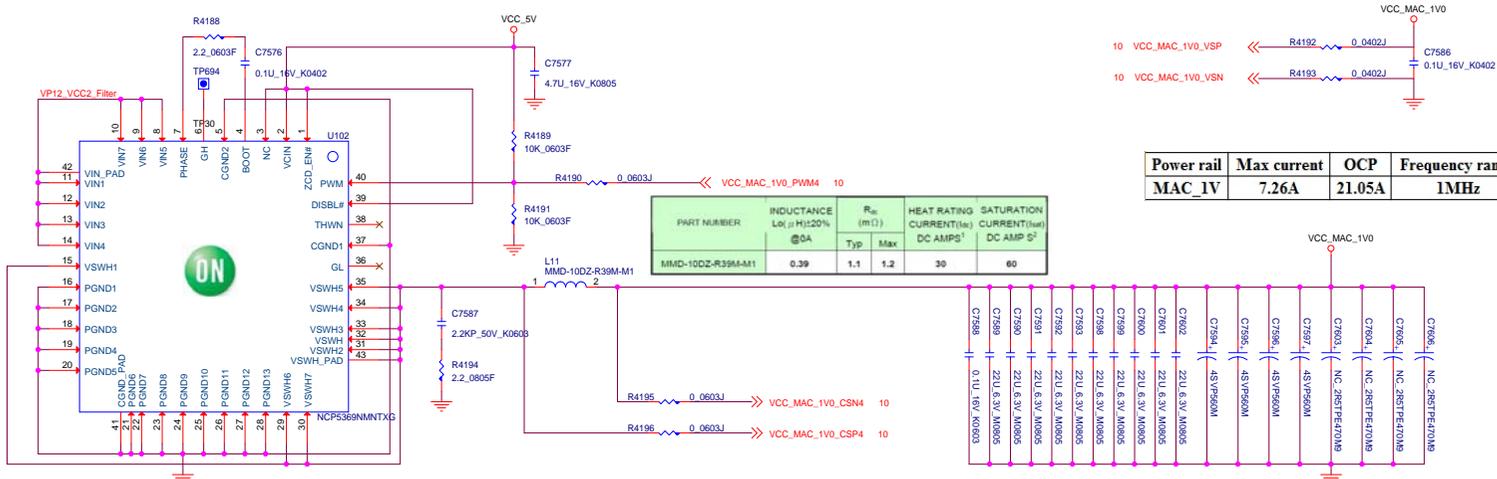
Add the C7996,C7997,C7998 to reduce the noise.20150108



Power rail	Max current	OCF	Frequency range
PHY_IV	48.9A	60A	1MHz



Power rail	Max current	OCF	Frequency range
PHY_IV	48.9A	60A	1MHz



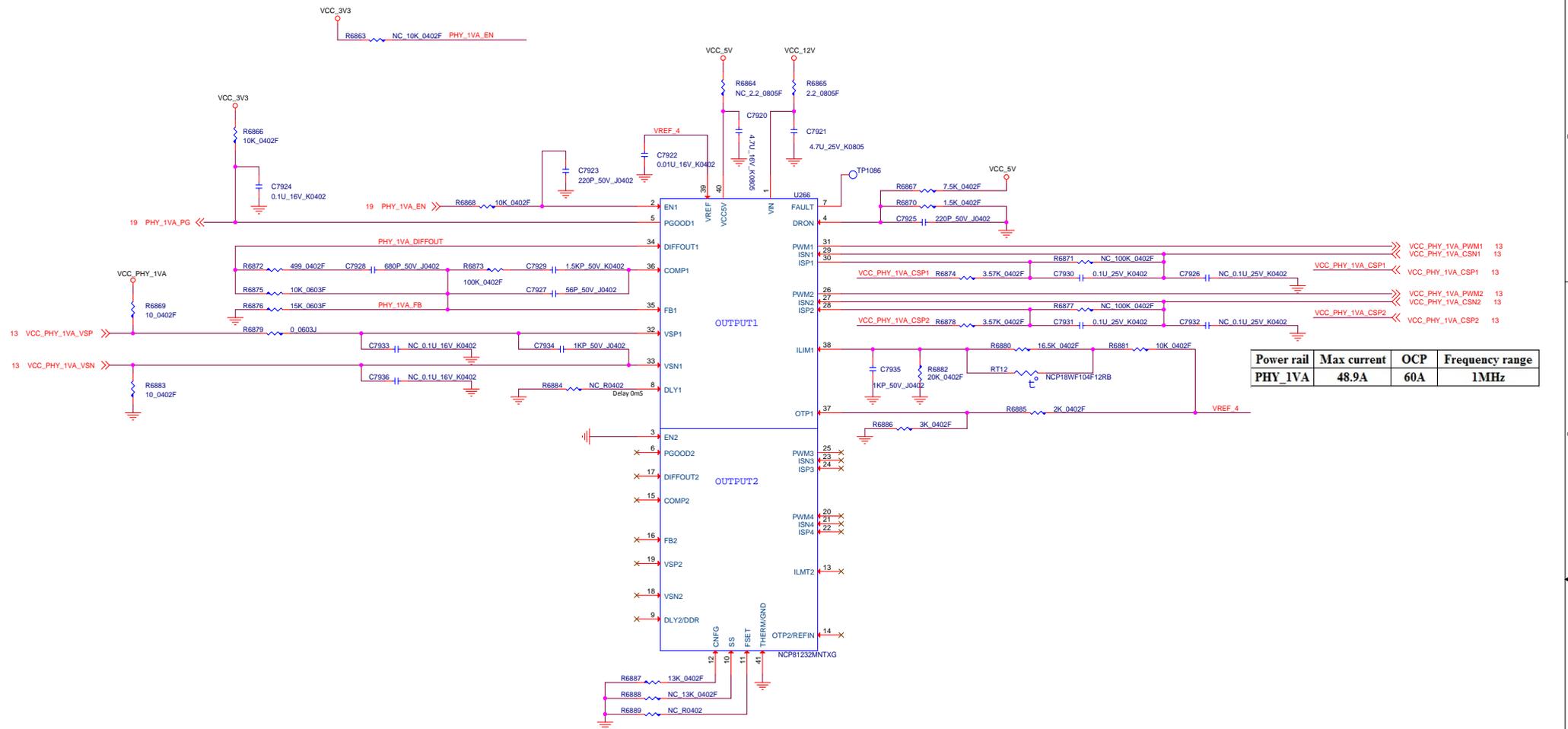
Power rail	Max current	OCF	Frequency range
MAC_IV	7.26A	21.05A	1MHz



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Date:	Tuesday, September 13, 2016	Sheet 11 of 80

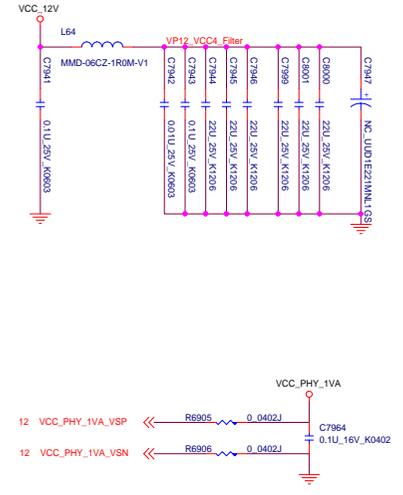
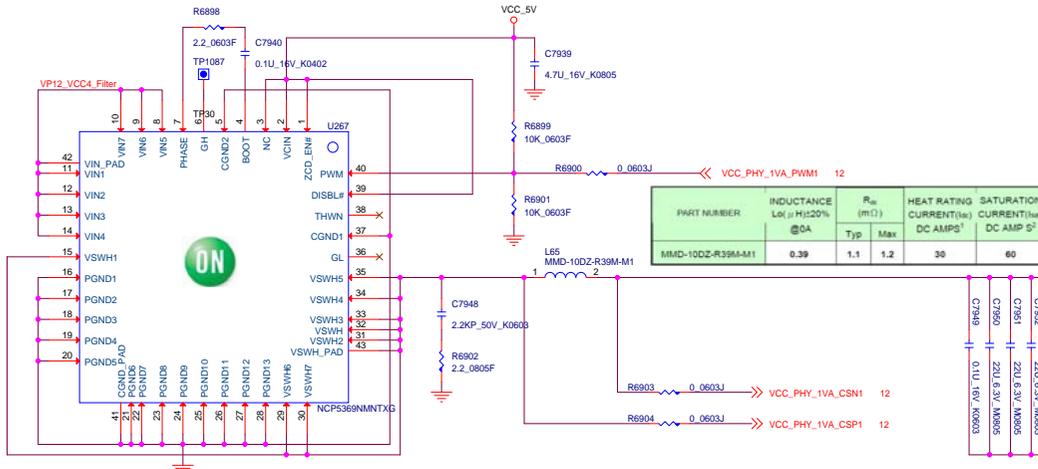


Power rail	Max current	OCp	Frequency range
PHY_1VA	48.9A	60A	1MHz

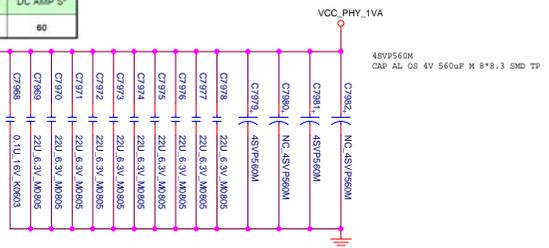
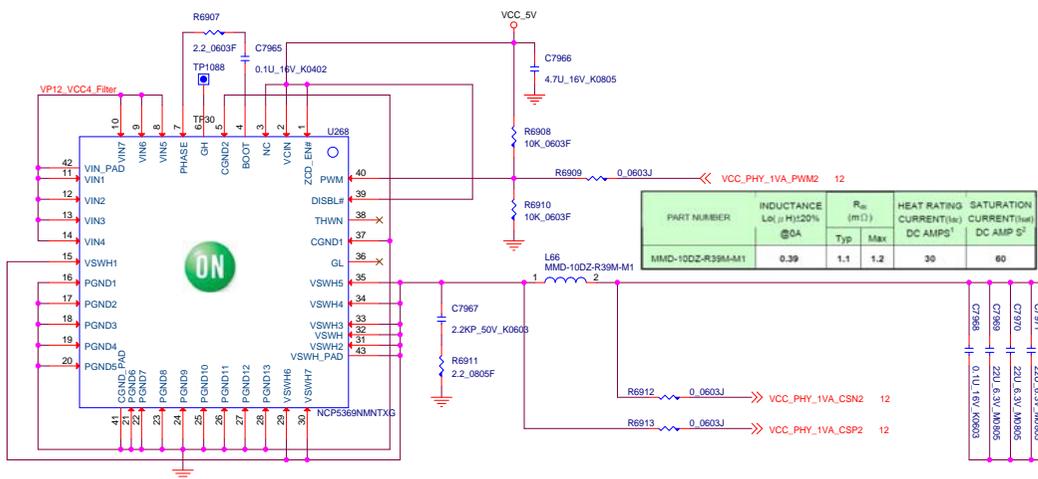
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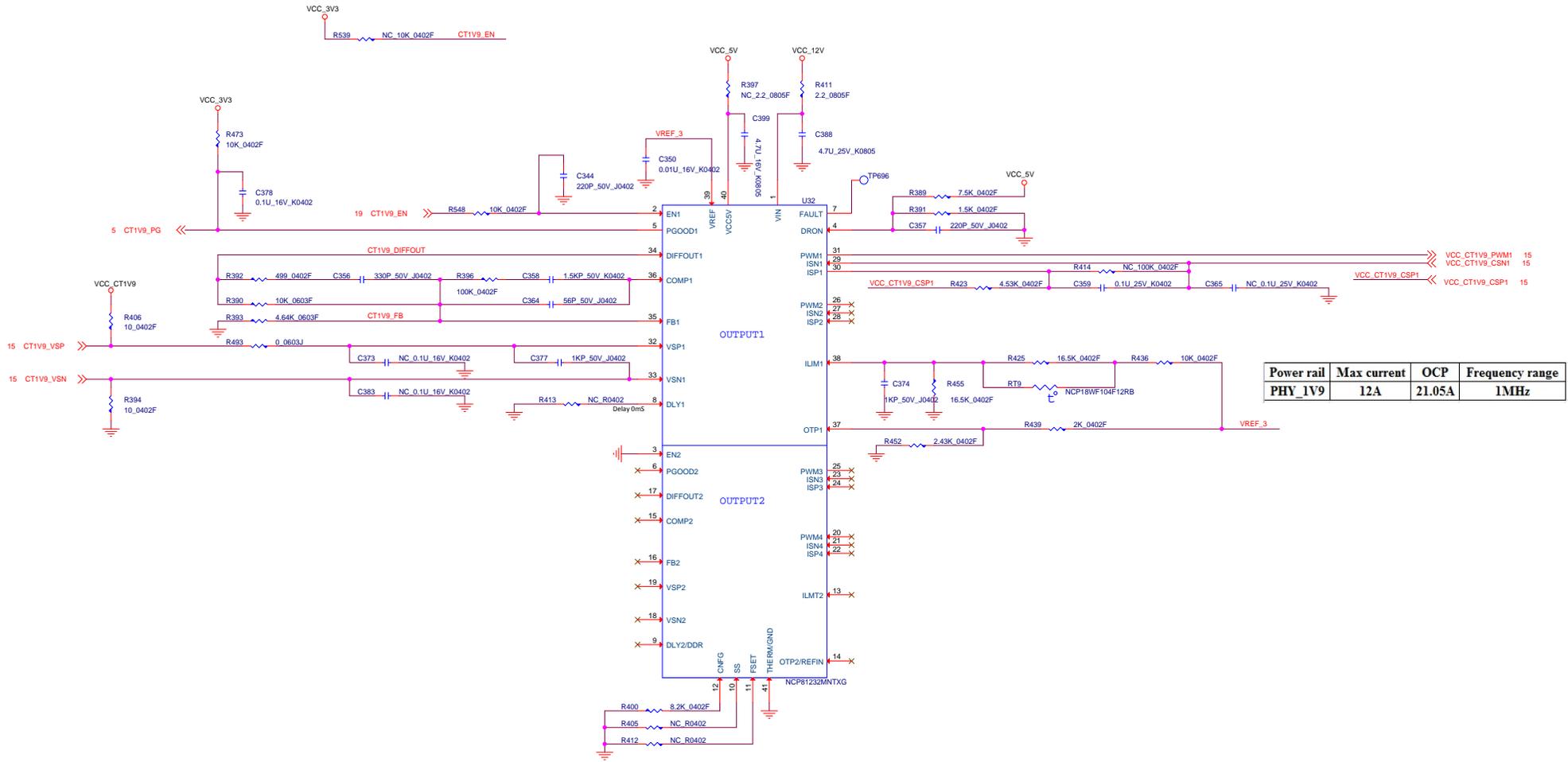
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File		01-12_PWR [PHY 1V0A]_3	
Size	Document Number		
C	1ADSS-0XXXXX	Rev	1.1
Date:	Tuesday, September 13, 2016	Sheet	12 of 80



Power rail	Max current	OCF	Frequency range
PHY_1VA	48.9A	60A	1MHz





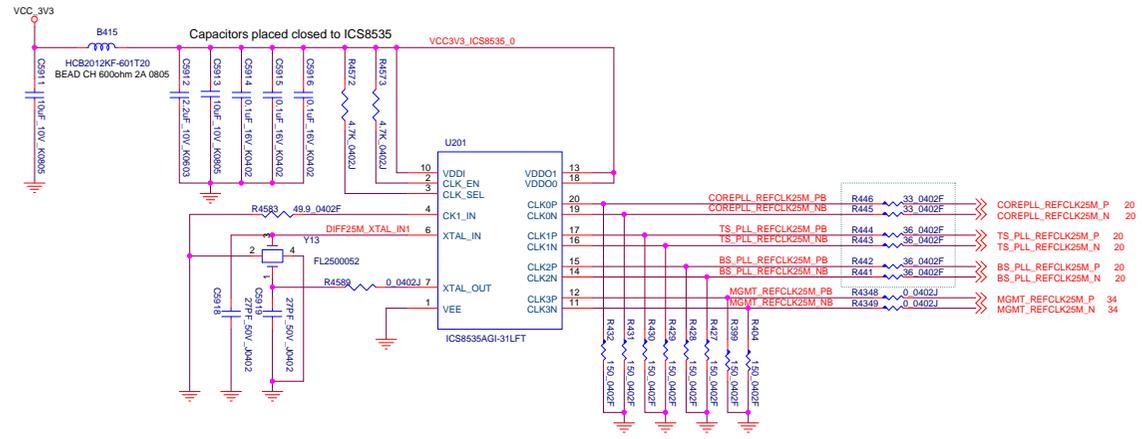
Power rail	Max current	OCp	Frequency range
PHY_1V9	12A	21.05A	1MHz

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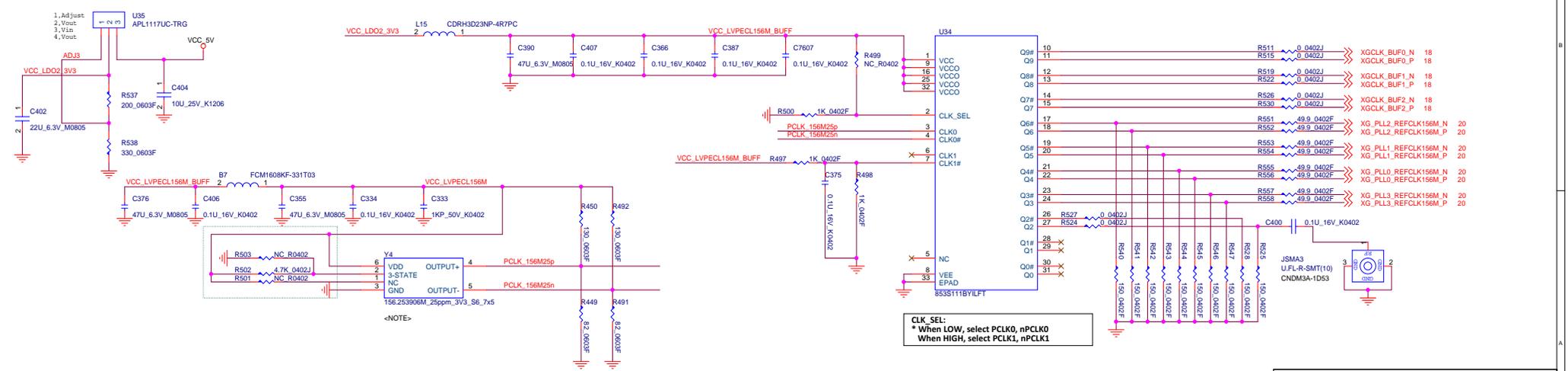
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File	01-12_PWR [CT 1V9]_1		
Size	Document Number		Rev
C	1ADSS-0XXXXX		1.1
Date:	Tuesday, September 13, 2016	Sheet	14 of 80

25MHz Differential Clock for BCM56850 Core Clock



156.25MHz Differential Clock for BCM56850

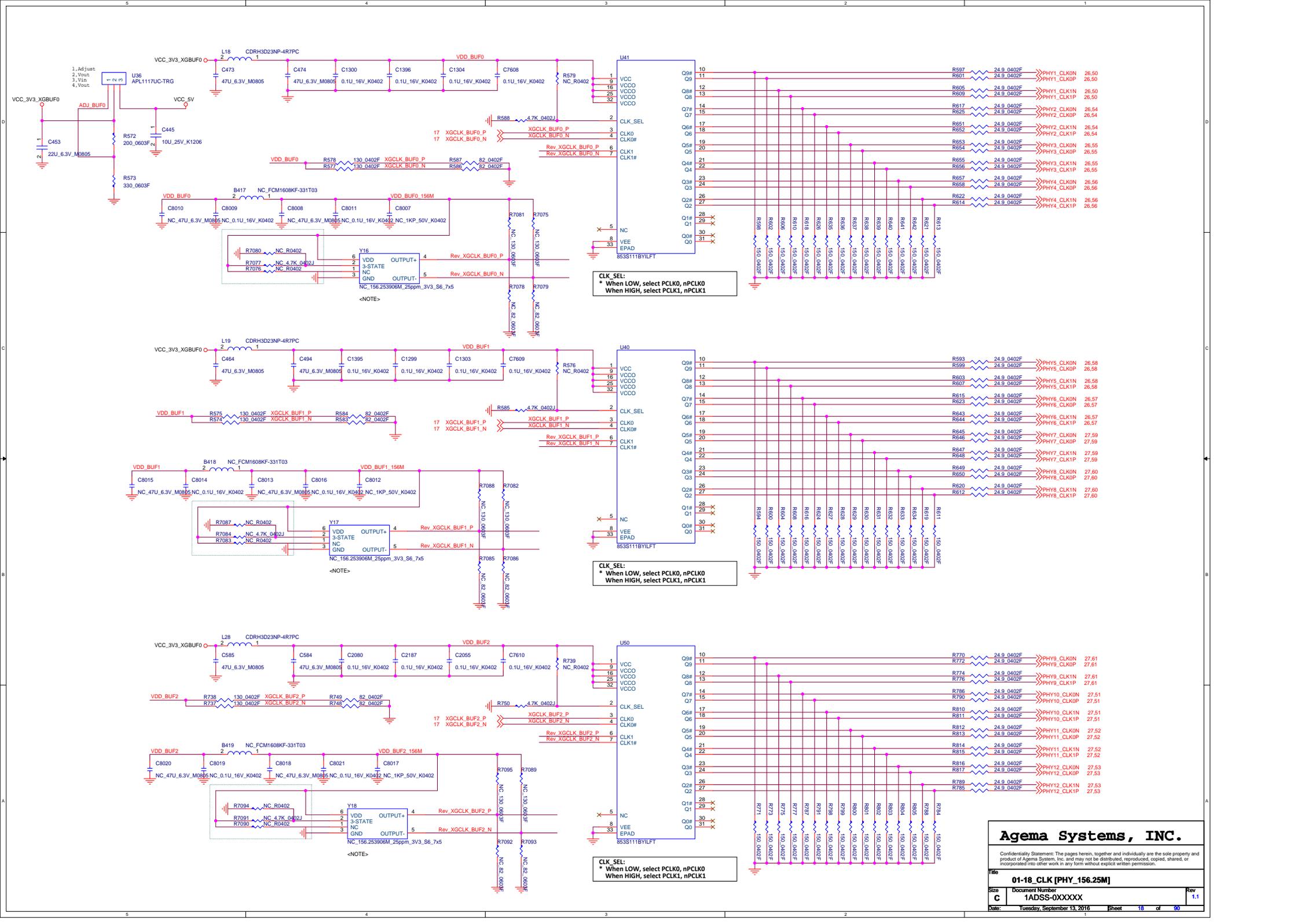


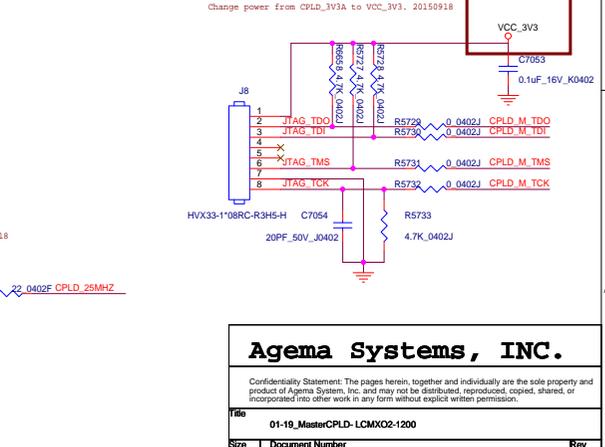
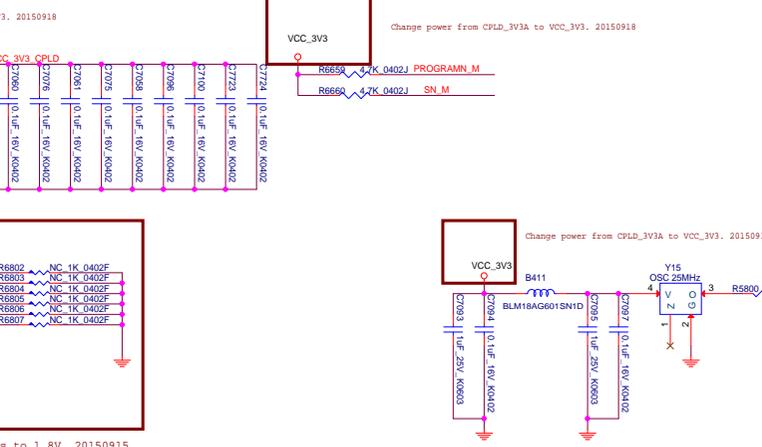
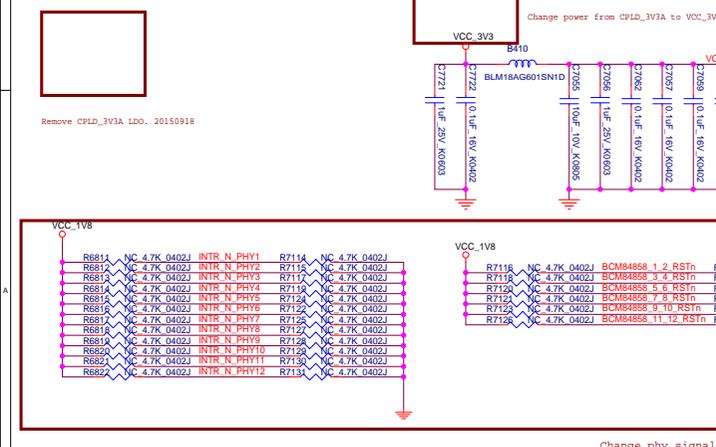
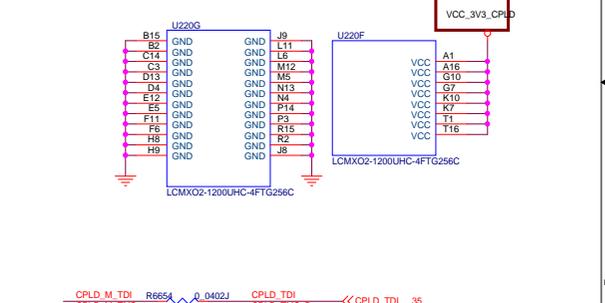
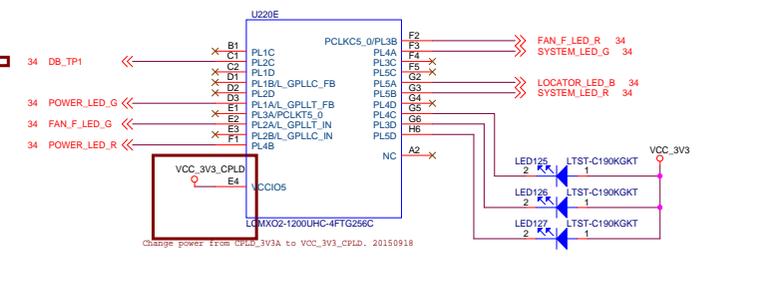
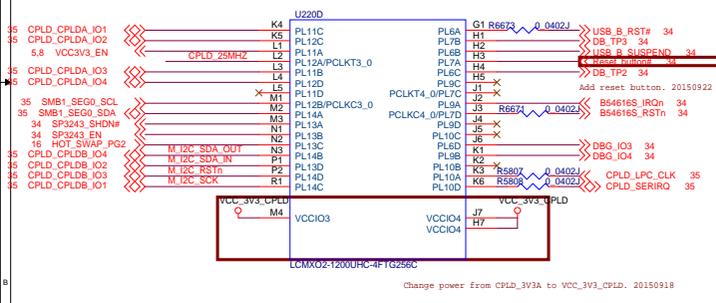
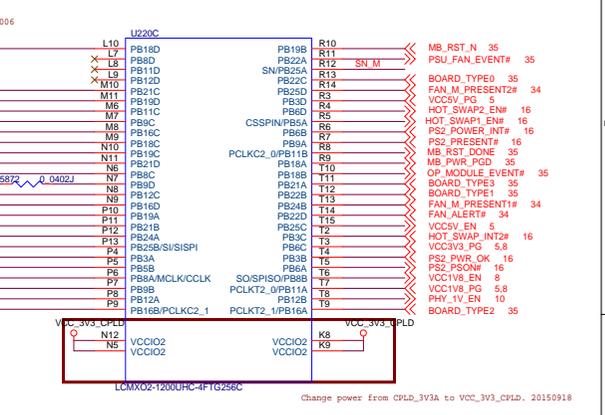
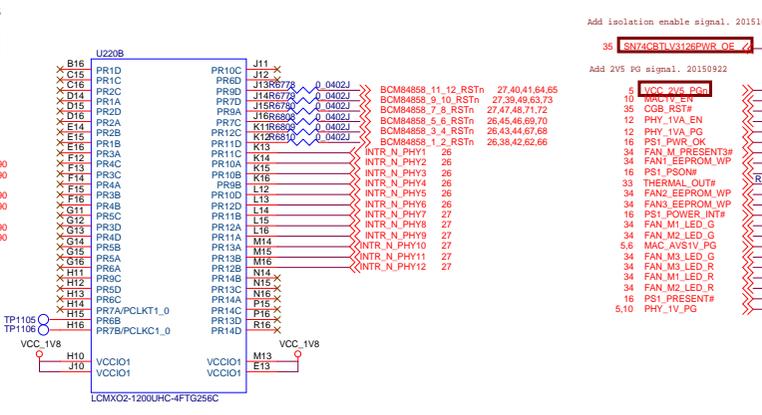
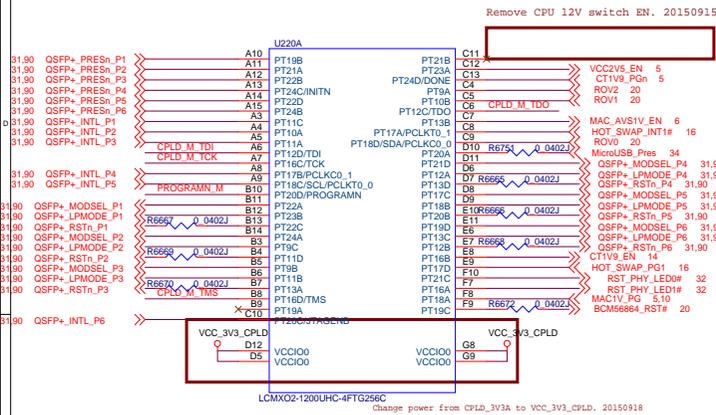
CLK_SEL:
 * When LOW, select PCLK0, nPCLK0
 When HIGH, select PCLK1, nPCLK1

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File		01-17_CLK [25M_156.25M]	
Size	Document Number		
C	1ADSS-0XXXXX	Sheet	17 of 80
Date:	Tuesday, September 13, 2016	Rev	1.1





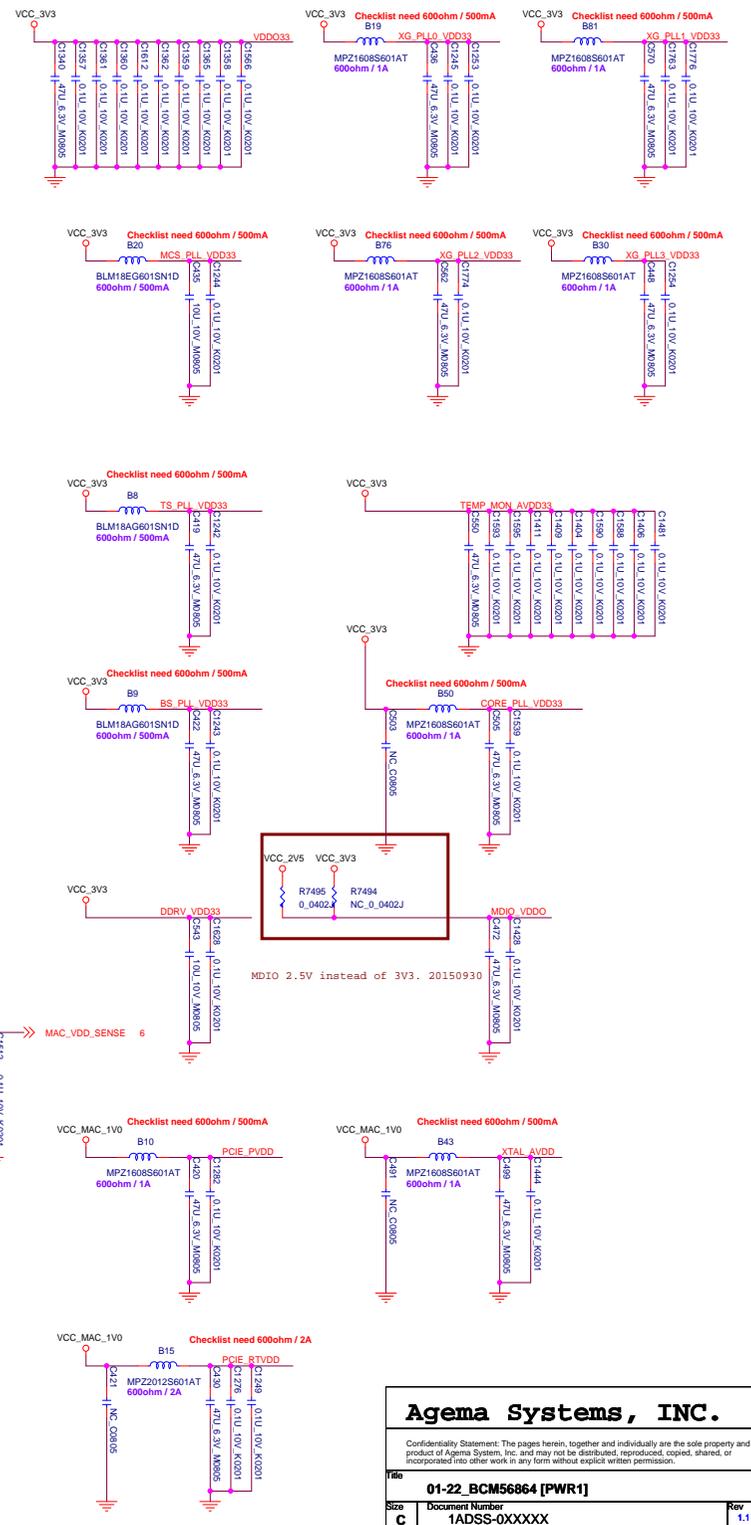
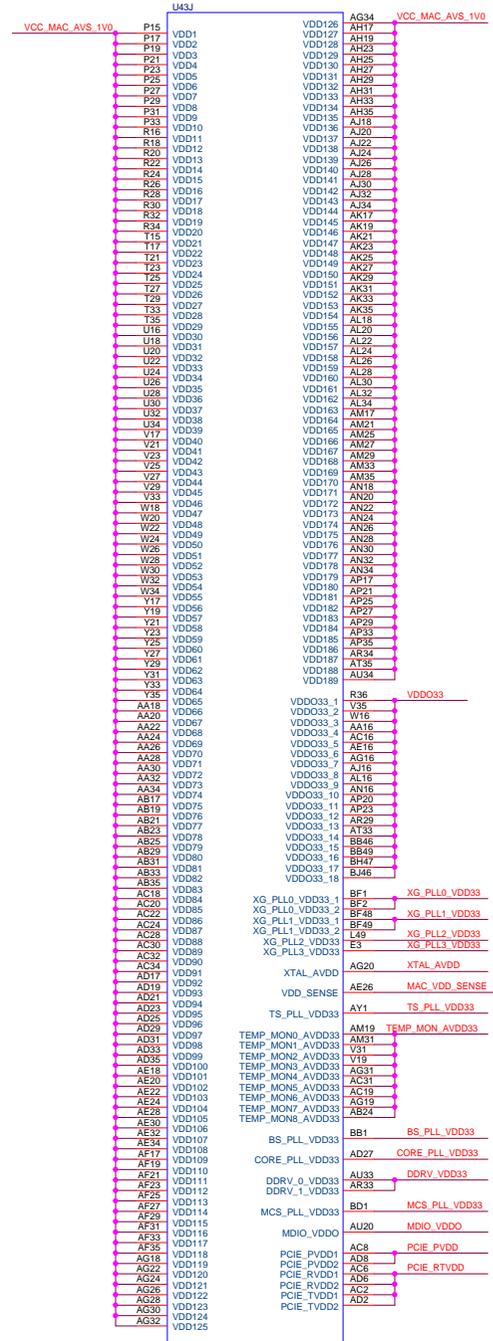
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Size: C Document Number: 1ADSS-0XXXXX Rev: 1.1

Date: Tuesday, September 13, 2016 Sheet: 19 of 80

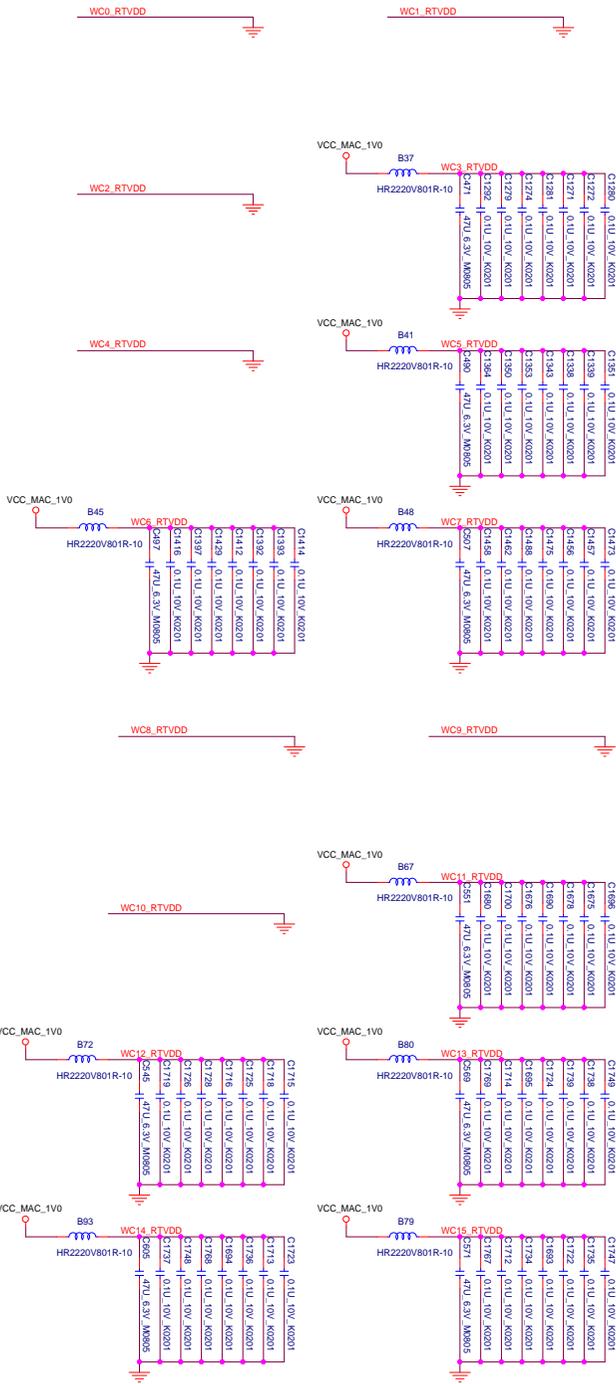
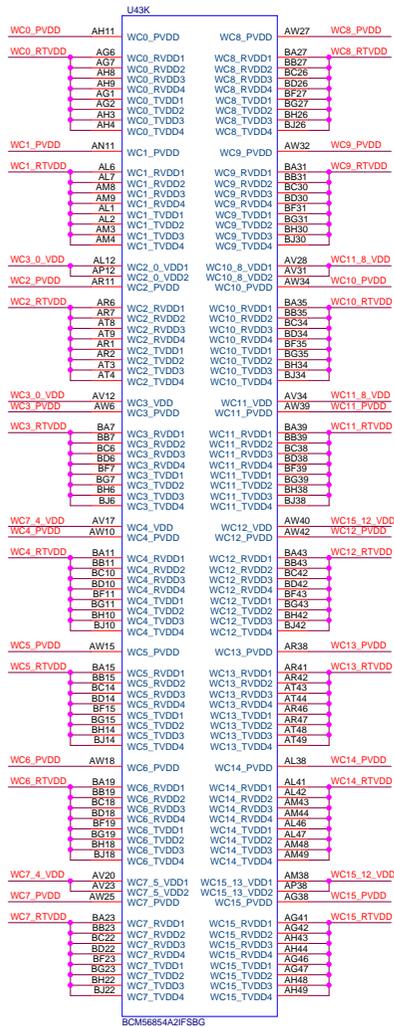


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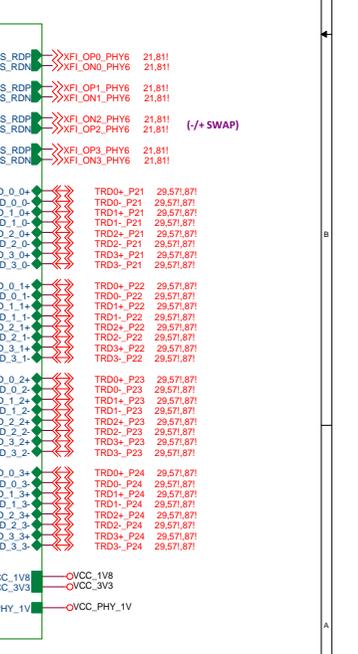
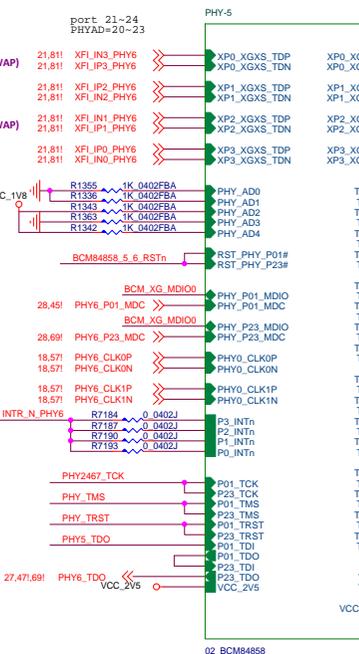
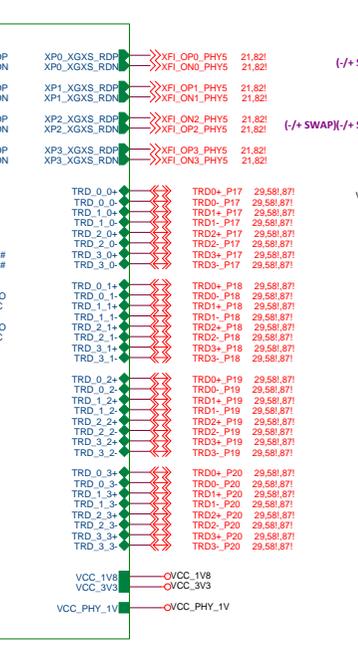
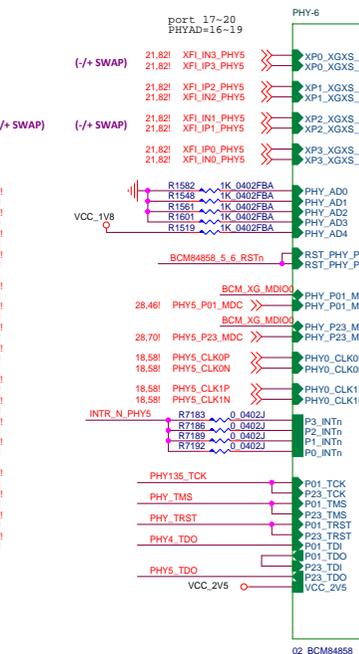
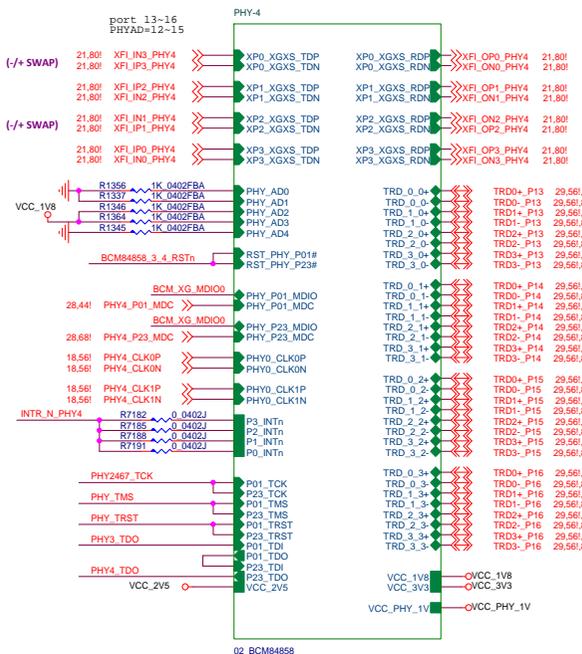
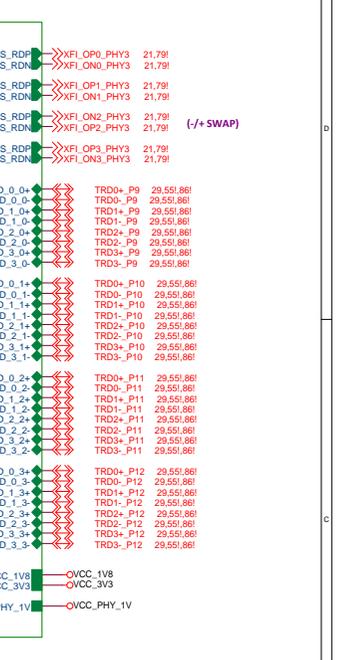
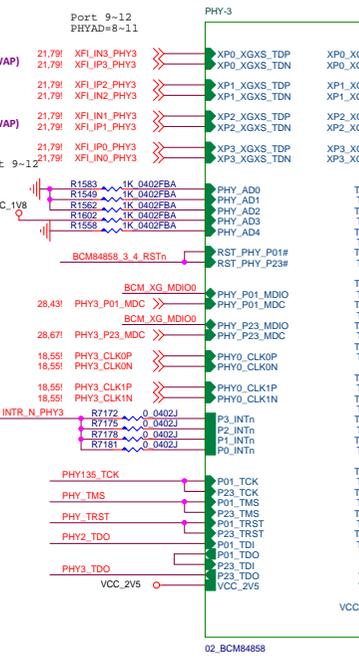
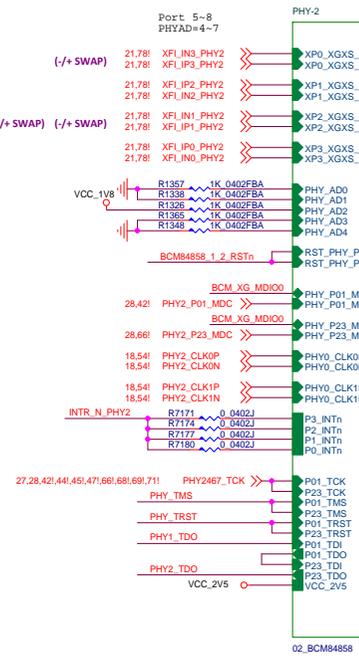
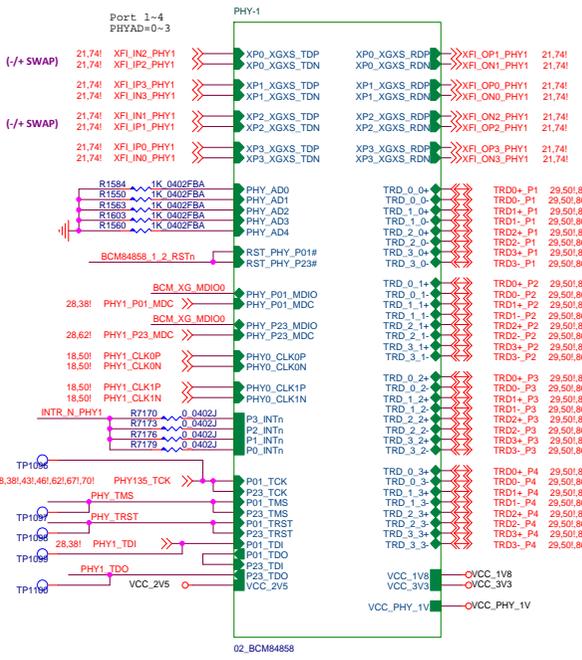
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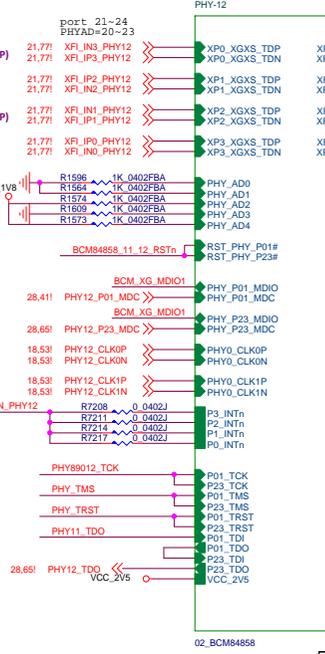
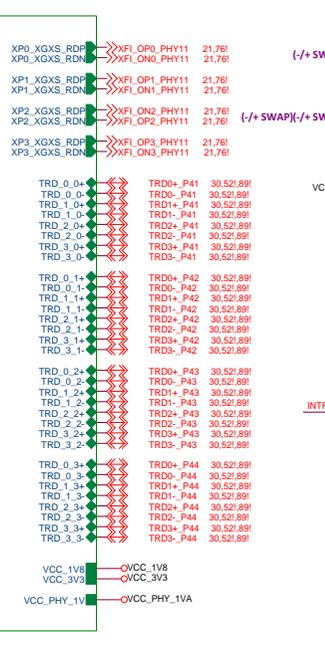
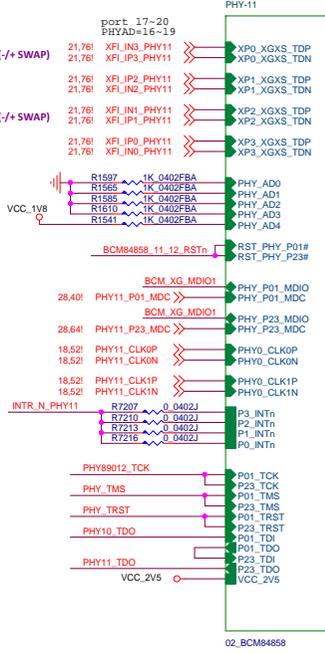
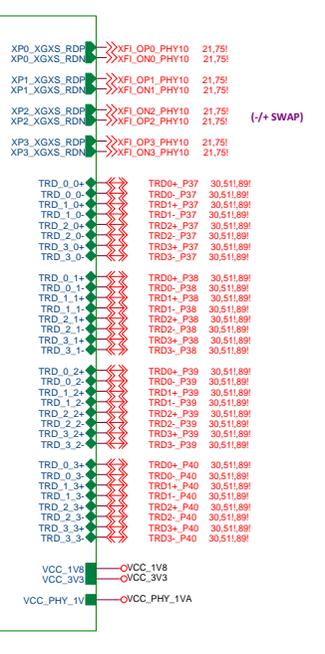
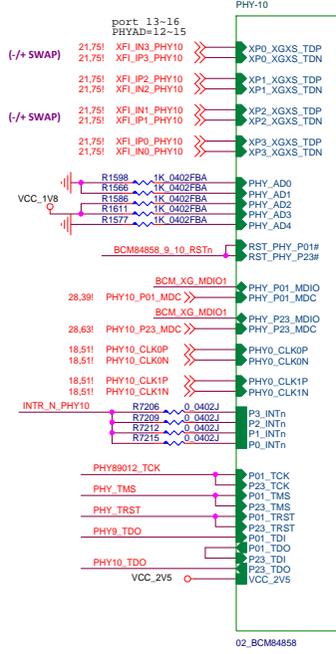
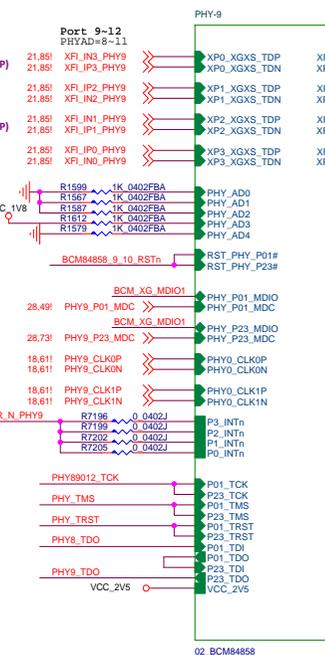
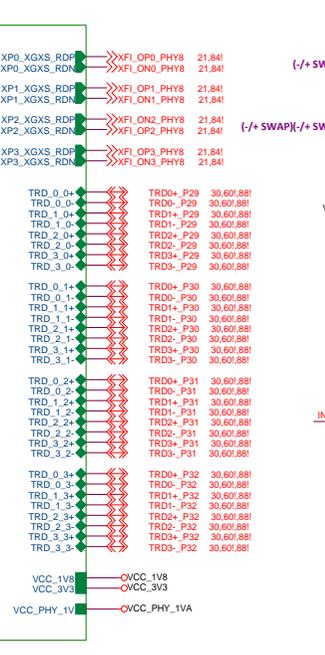
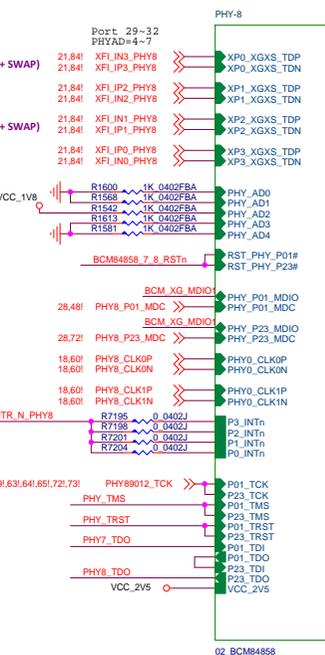
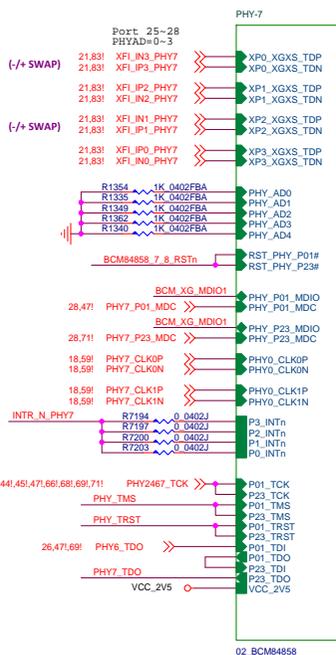
File		01-22_BCM56864 [PWR1]	
Size	Document Number	1ADSS-0XXXX	
C	Rev	1.1	
Date:	Tuesday, September 13, 2016	Sheet	22 of 80

Broadcom Ball out v3.1: Correct I/O type from GND to PWR for WC11_VDD pin.



U43E				U43F				U43G				U43H				U43I			
A2	E43			K29	R12			AE1	AP8			AY14	BE21			P16	AD28		
AGND1	AGND101	E44		AGND201	AGND301	R13		AGND401	AGND501	APP		AGND601	AGND701	BE22		AGND801	AGND901	AD29	
AGND2	AGND102	E45		AGND202	AGND302	R14		AGND402	AGND502	AP9		AGND602	AGND702	BE23		AGND802	AGND902	AD30	
AGND3	AGND103	E46		AGND203	AGND303	R40		AGND403	AGND503	AP11		AGND603	AGND703	BE24		AGND803	AGND903	AD31	
AGND4	AGND104	E47		AGND204	AGND304	R40		AGND404	AGND504	AP40		AGND604	AGND704	BE25		AGND804	AGND904	AD32	
AGND5	AGND105	E48		AGND205	AGND305	R46		AGND405	AGND505	AP46		AGND605	AGND705	BE26		AGND805	AGND905	AD33	
AGND6	AGND106	F1		AGND206	AGND306	T10		AGND406	AGND506	AP44		AGND606	AGND706	BE27		AGND806	AGND906	AD34	
AGND7	AGND107	F2		AGND207	AGND307	T11		AGND407	AGND507	AP45		AGND607	AGND707	BE28		AGND807	AGND907	AD35	
AGND8	AGND108	F3		AGND208	AGND308	T12		AGND408	AGND508	AP42		AGND608	AGND708	BE29		AGND808	AGND908	AD36	
AGND9	AGND109	F4		AGND209	AGND309	T38		AGND409	AGND509	AP49		AGND609	AGND709	BE30		AGND809	AGND909	AD37	
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INTR_N_PHY8	INTR_N_PHY8			
INTR_N_PHY9	INTR_N_PHY9	19,471,481,711,721	BCM84858_7_8_RSTn	
INTR_N_PHY10	INTR_N_PHY10	19,301,491,631,731	BCM84858_9_10_RSTn	
INTR_N_PHY11	INTR_N_PHY11	19,401,641,651	BCM84858_11_12_RSTn	
INTR_N_PHY12	INTR_N_PHY12			
INTR_N_PHY13	INTR_N_PHY13	20,28,391,391,401,411,421,431,441,451,461,471,481,491,631,641,651,661,671,681,691,701,711,721,731		
INTR_N_PHY14	INTR_N_PHY14			
INTR_N_PHY15	INTR_N_PHY15			
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INTR_N_PHY17	INTR_N_PHY17			
INTR_N_PHY18	INTR_N_PHY18			

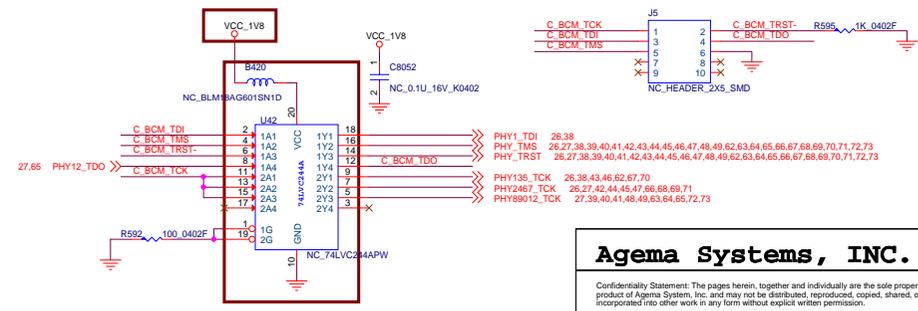
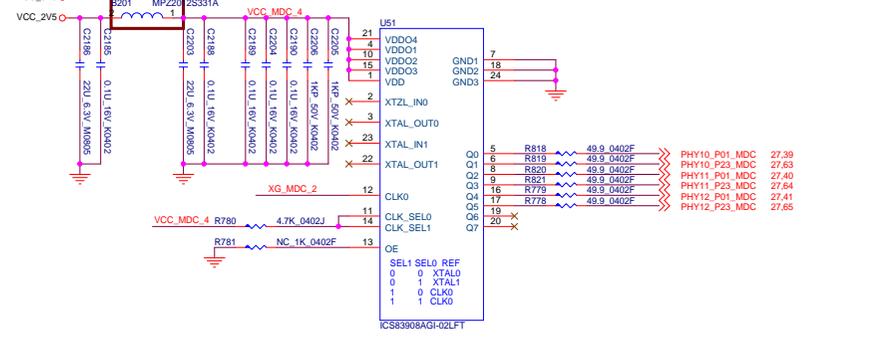
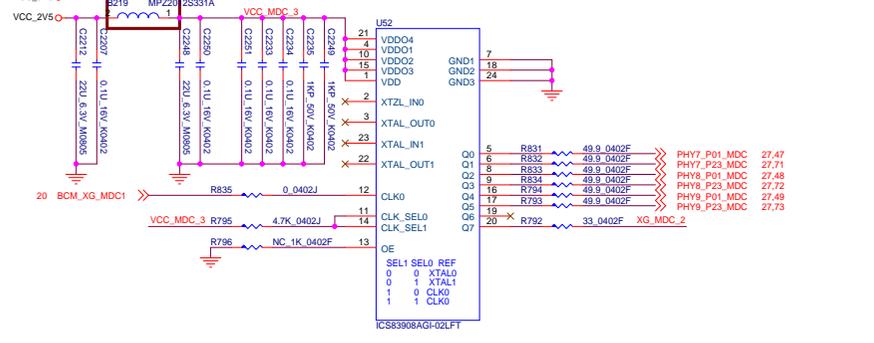
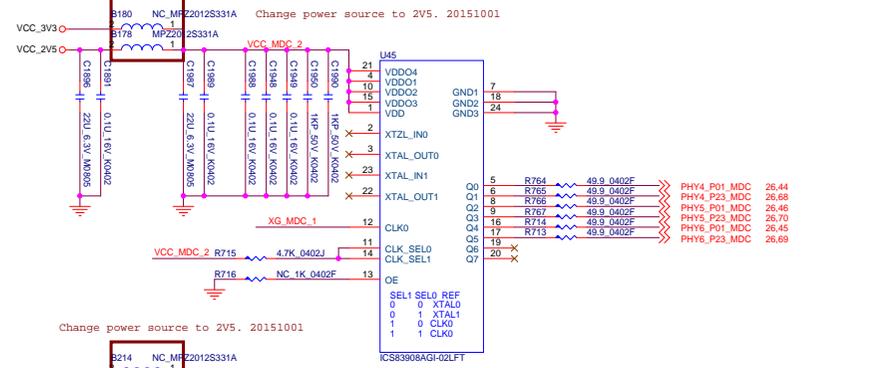
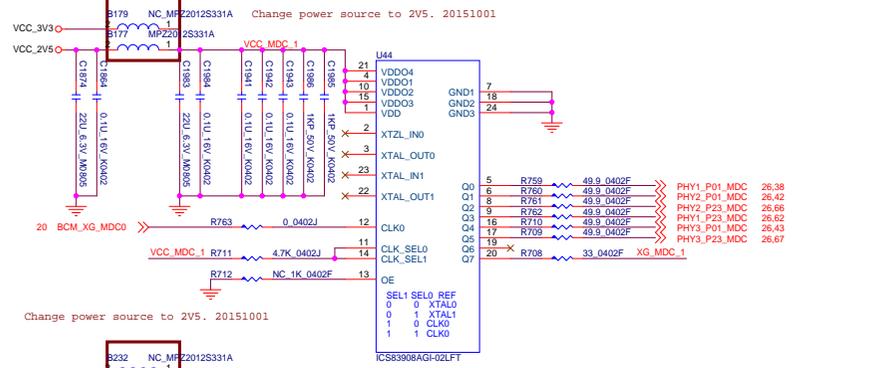
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Size: Document Number **1ADSS-0XXXX**

Date: **Tuesday, September 13, 2016** Sheet **27** of **80**



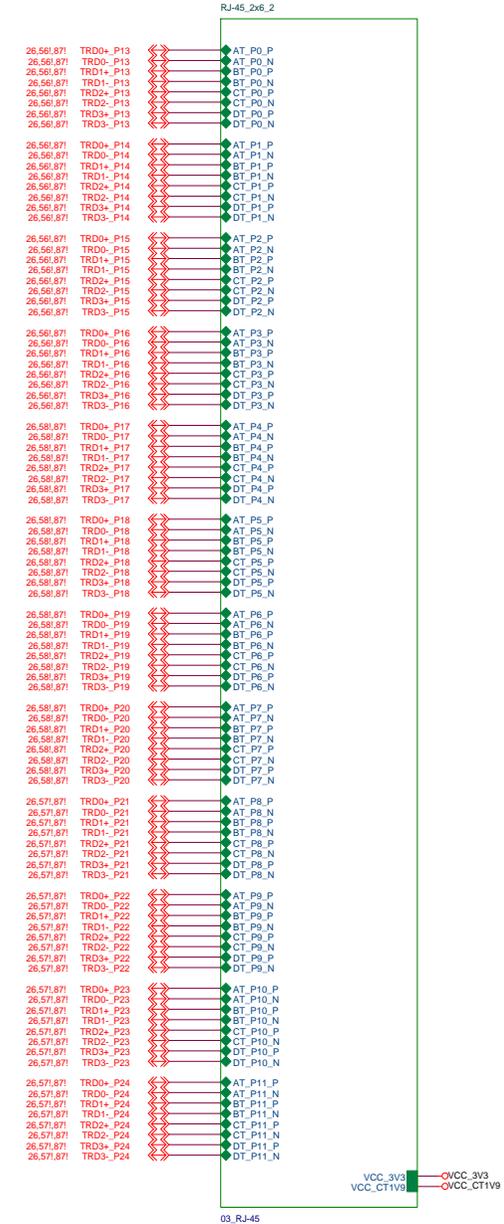
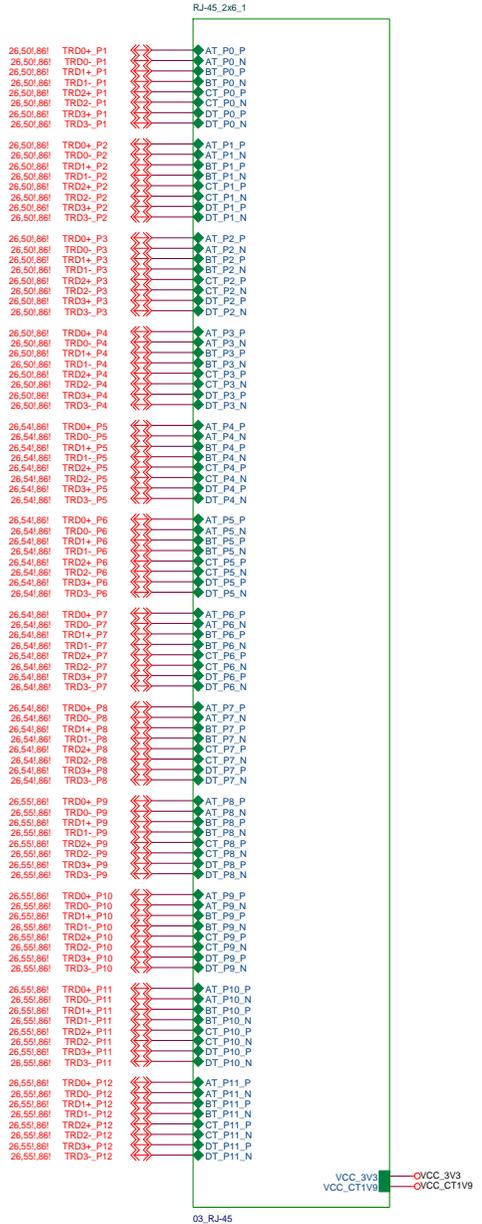
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Date:	Tuesday, September 13, 2016	Sheet 28 of 80

P1~P12

P13~P24



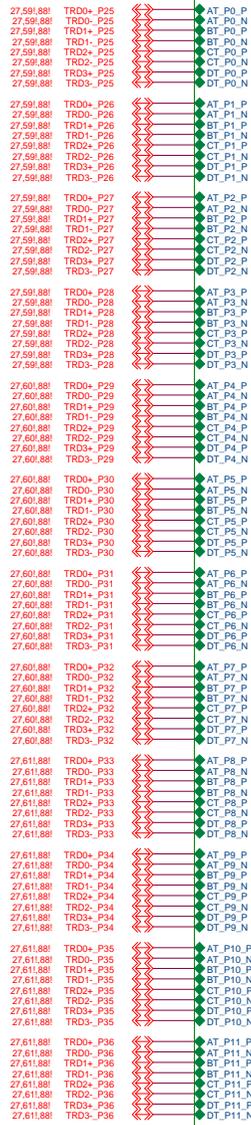
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Date:	Tuesday, September 13, 2016	Sheet	29 of 80

P25~P36

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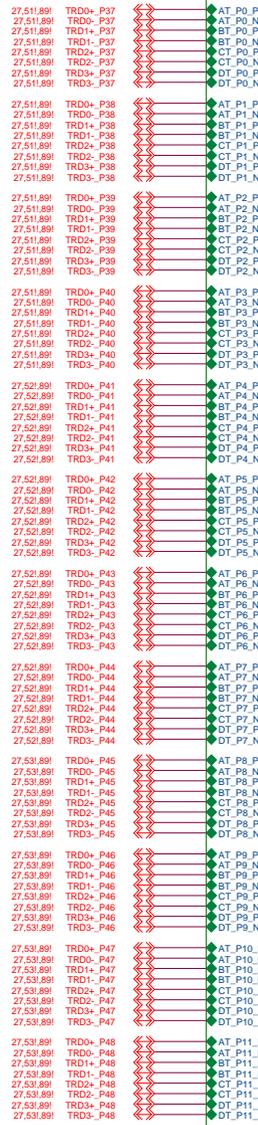


VCC_3V3
VCC_CT1V8

03_RJ-45

P37~P48

RJ-45_2x6_4



VCC_3V3
VCC_CT1V8

03_RJ-45

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Date:	Tuesday, September 13, 2016	Sheet	30 of 80

OSFP_CAGE1



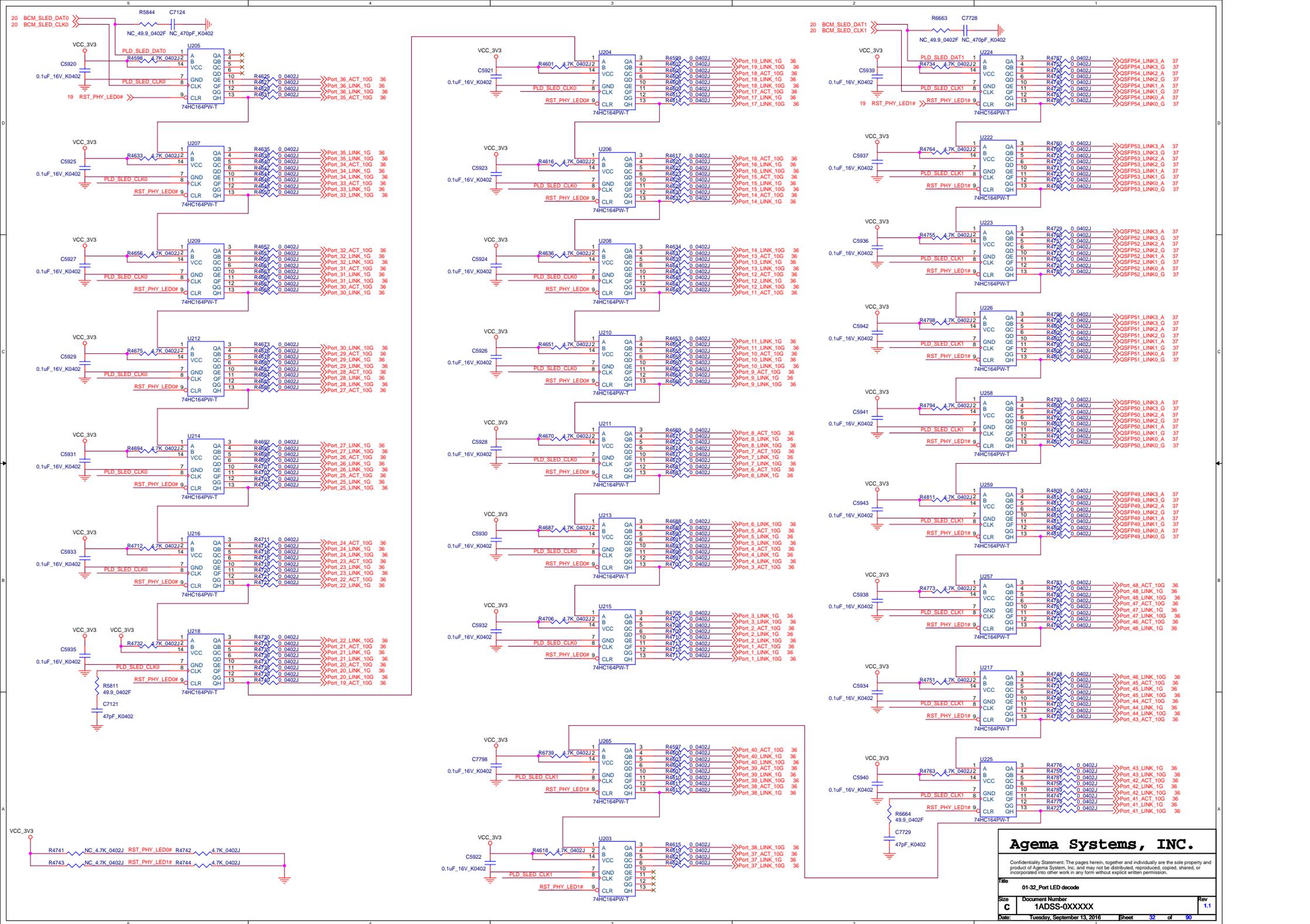
Swap the P/N trace to avoid backdrill impact. 20151001

04_QSFP_CAGE_2x3

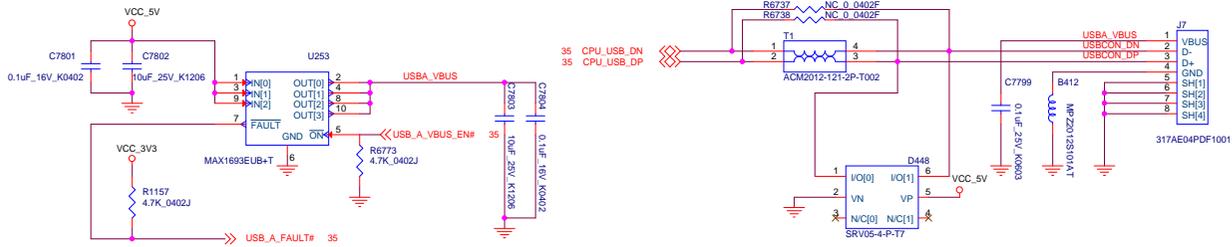
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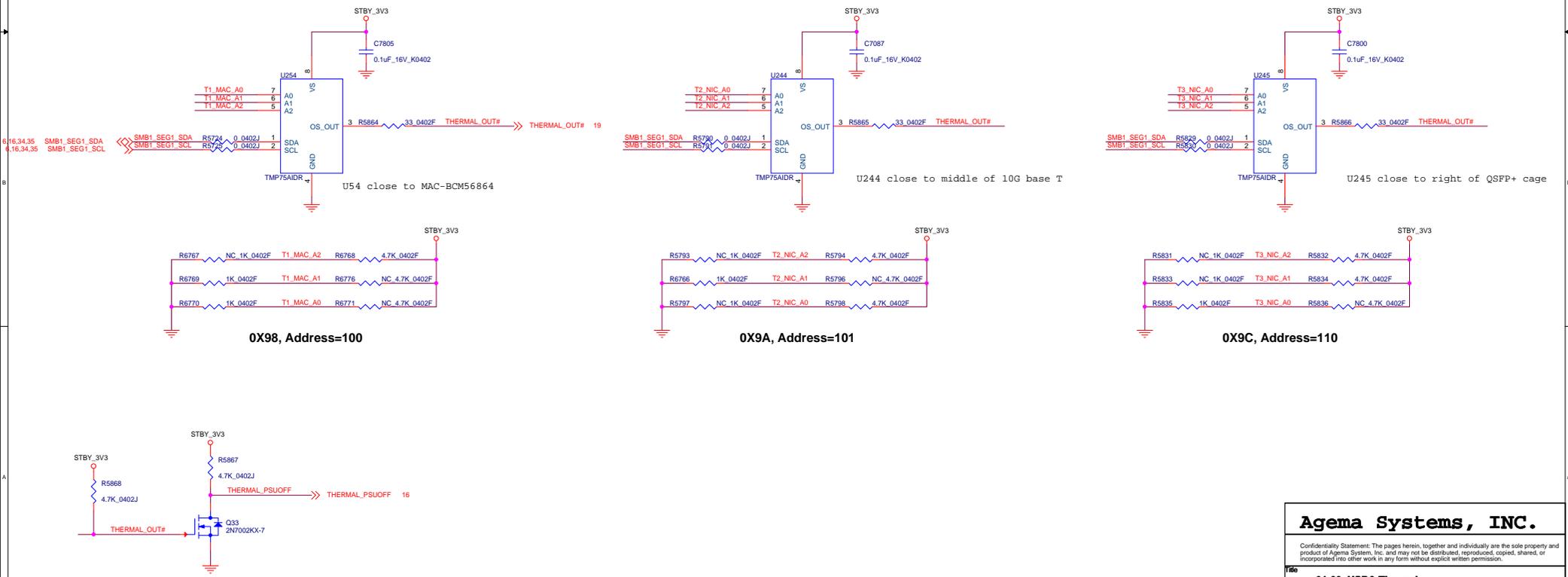
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Date:	Tuesday, September 13, 2016	Sheet	31 of 80



USB_A Device



Thermal Sensor

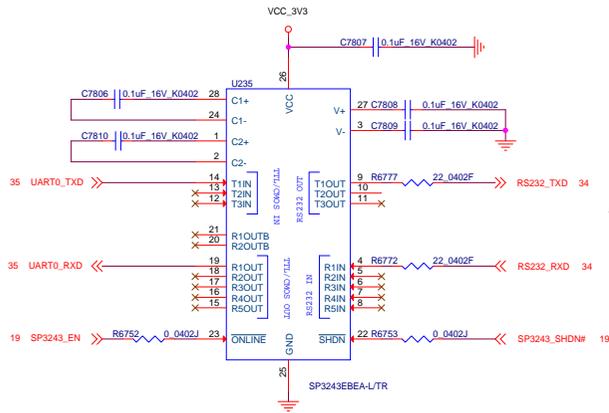


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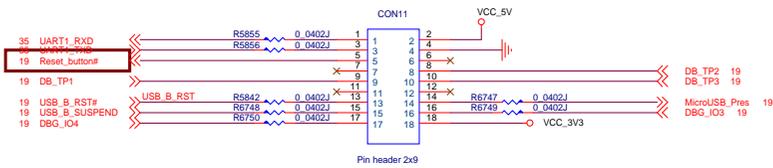
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C			Rev 1.1
Date:	Tuesday, September 13, 2016	Sheet	33 of 80

UART Interface

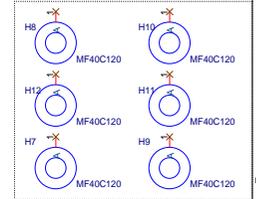


Add reset button signal. 20150915

7-Segment digit LED Connector

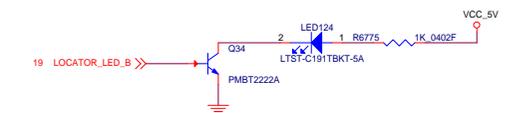
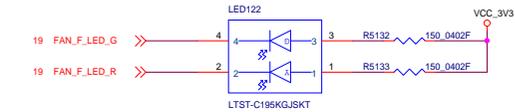
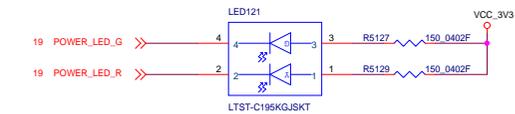
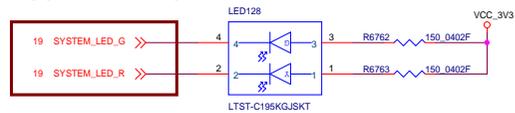


FOR SMT

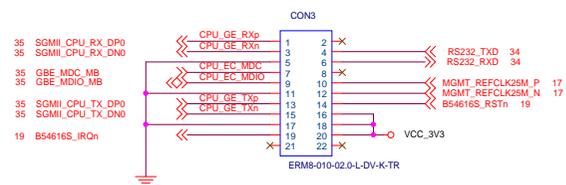


LED Indicator

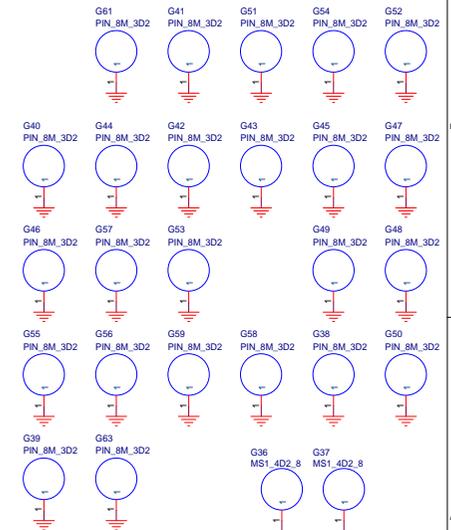
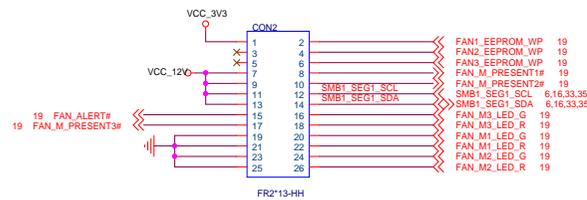
Change pin name from health to system. 20151002



MGMT Board Connector



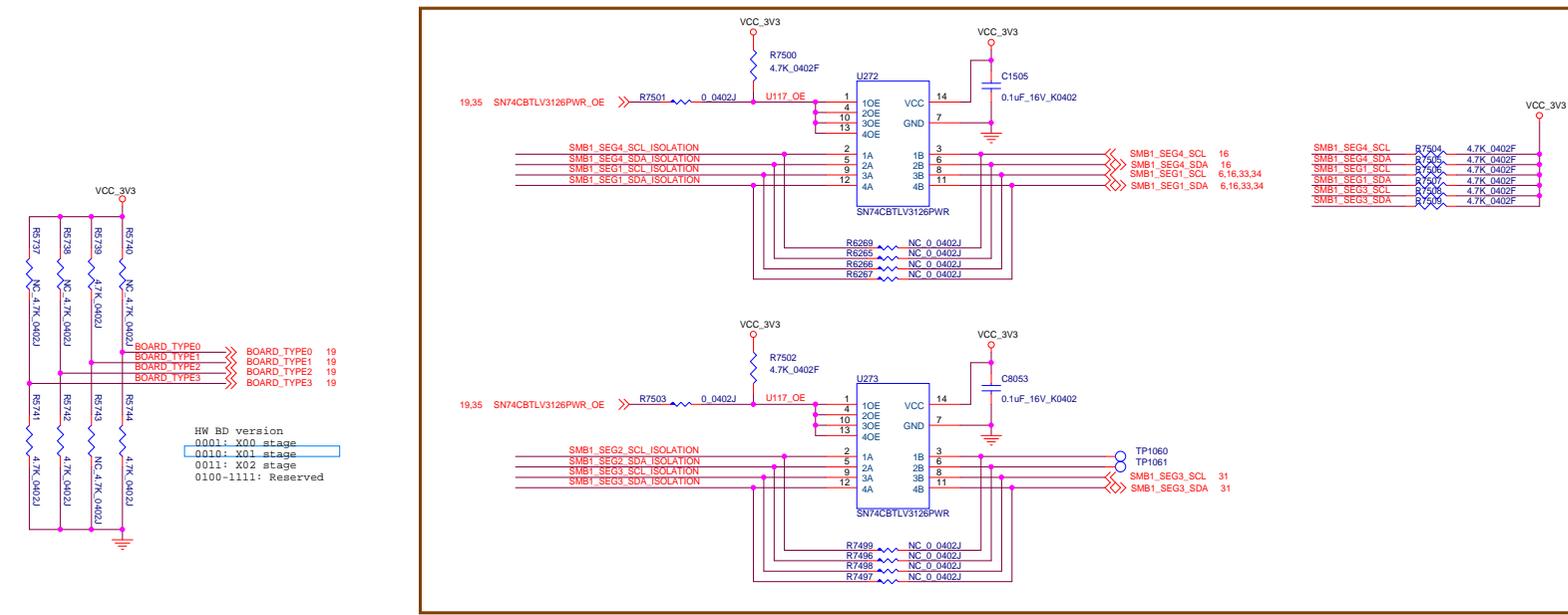
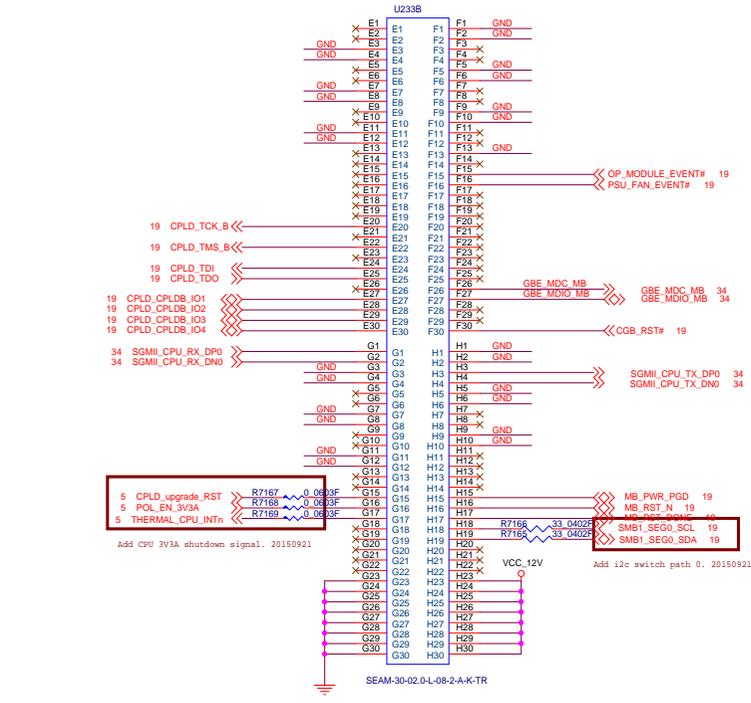
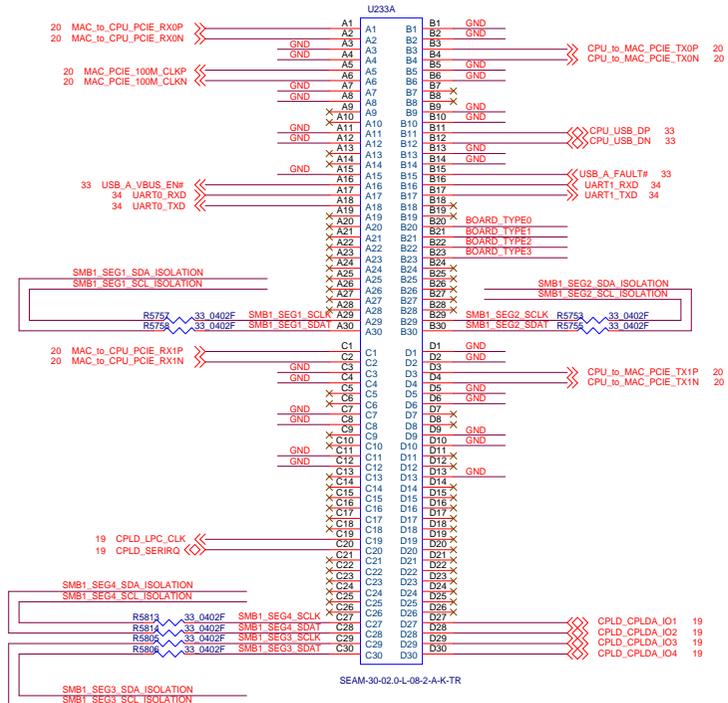
FAN Board Connector



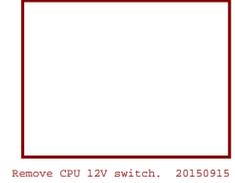
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File	01-34_FAN CONN/MGMT7-LED	
Size	Document Number	Rev
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Date:	Tuesday, September 13, 2016	Sheet 34 of 80



Add U272,U273 to isolate cross voltage domain. 20151006

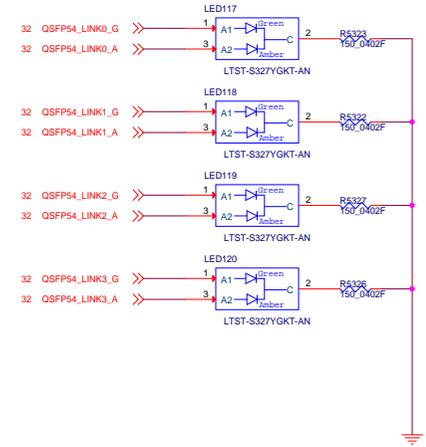
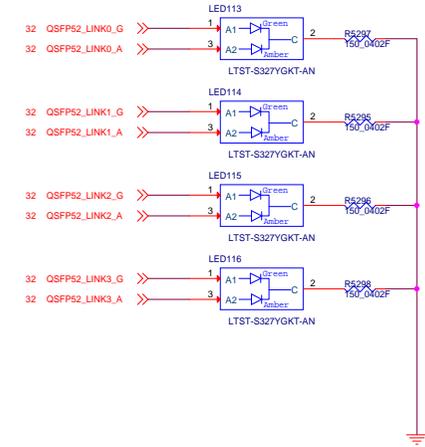
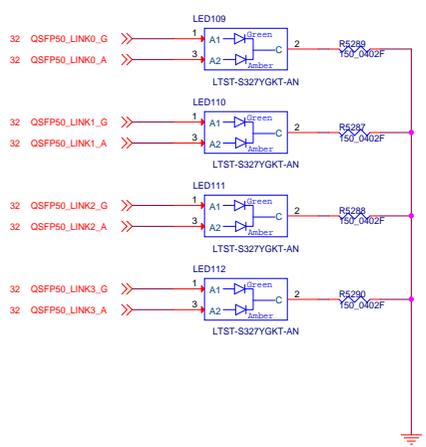
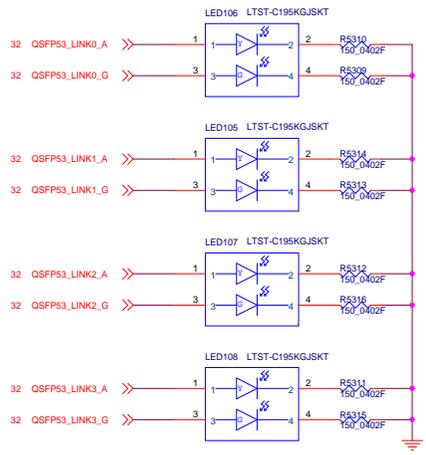
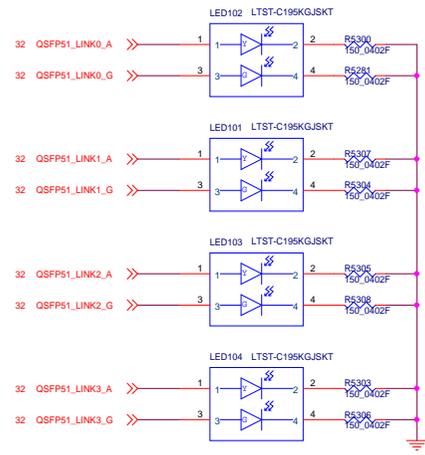
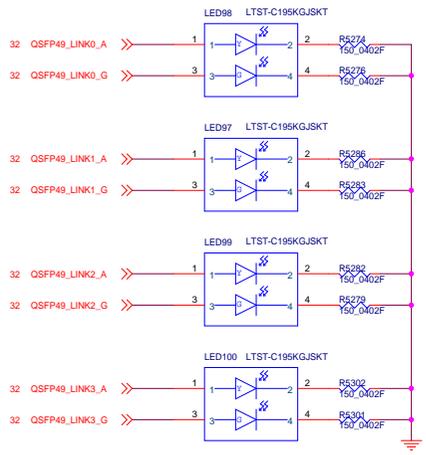


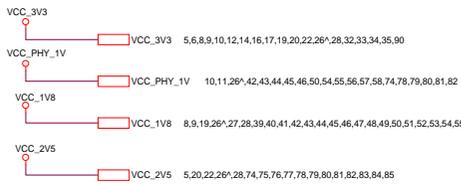


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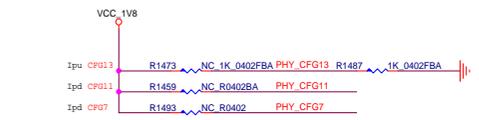
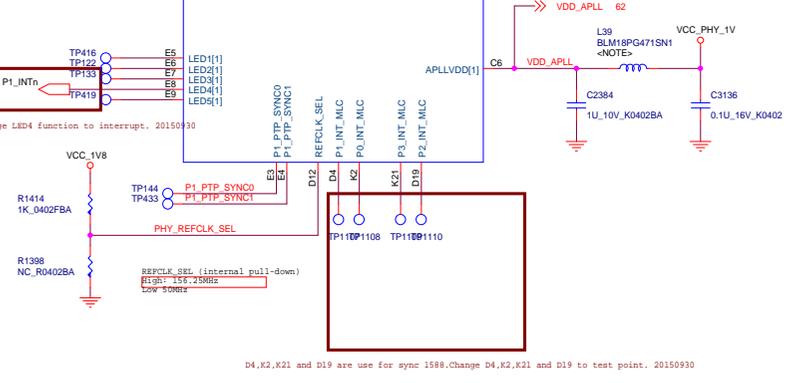
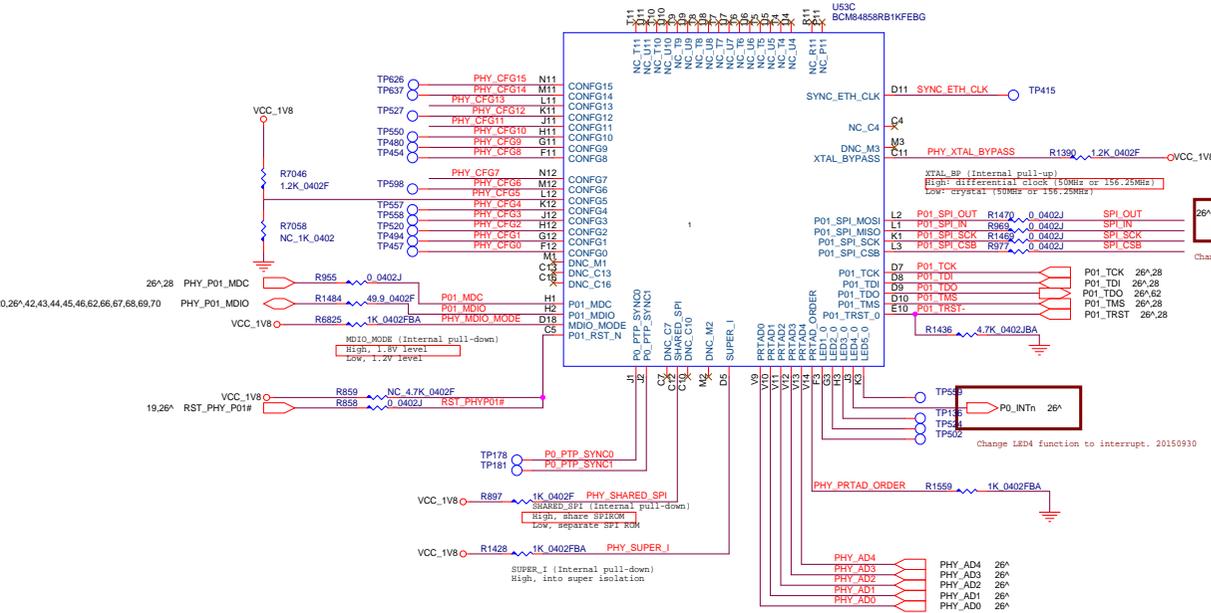
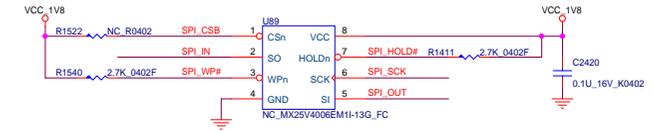
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File		01-36_108BT_LED Array	
Size	Document Number	1ADSS-0XXXX	
C			Rev 1.1
Date:	Tuesday, September 13, 2016	Sheet	36 of 80





SPI EEPROM



Config[7]: 10GBT core power down

High: Power down 10GBT core
Low: Power-up 10GBT core

Config[11]: LED control

High: Under user control
Low: LED 1, 2, 3, 5 are predefined as configured. LED 4 under user control.

Config[12]:

High: Firmware forces 1G fiber
Low: Firmware forces sets speed of device interfaces to 10G

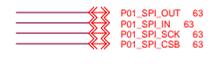
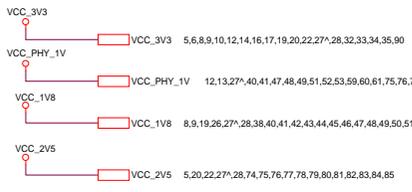
Config[13]: SPIROM

High: Load FW from SPIROM
Low: Load FW from MDIO interface

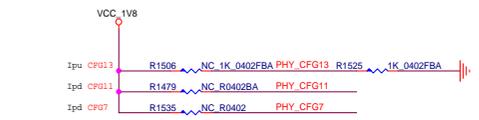
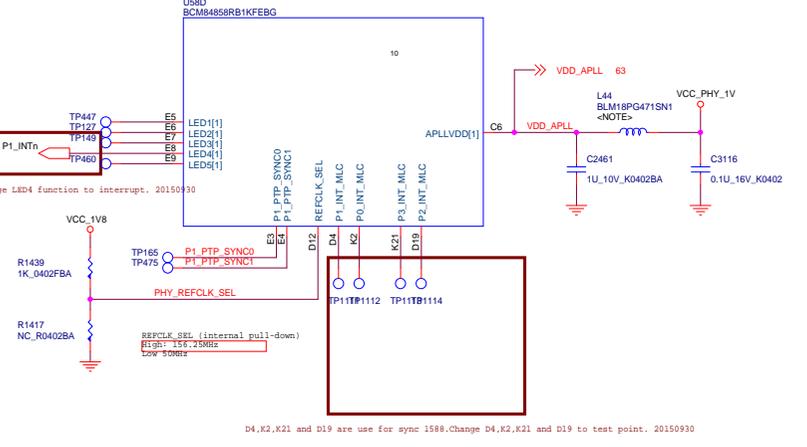
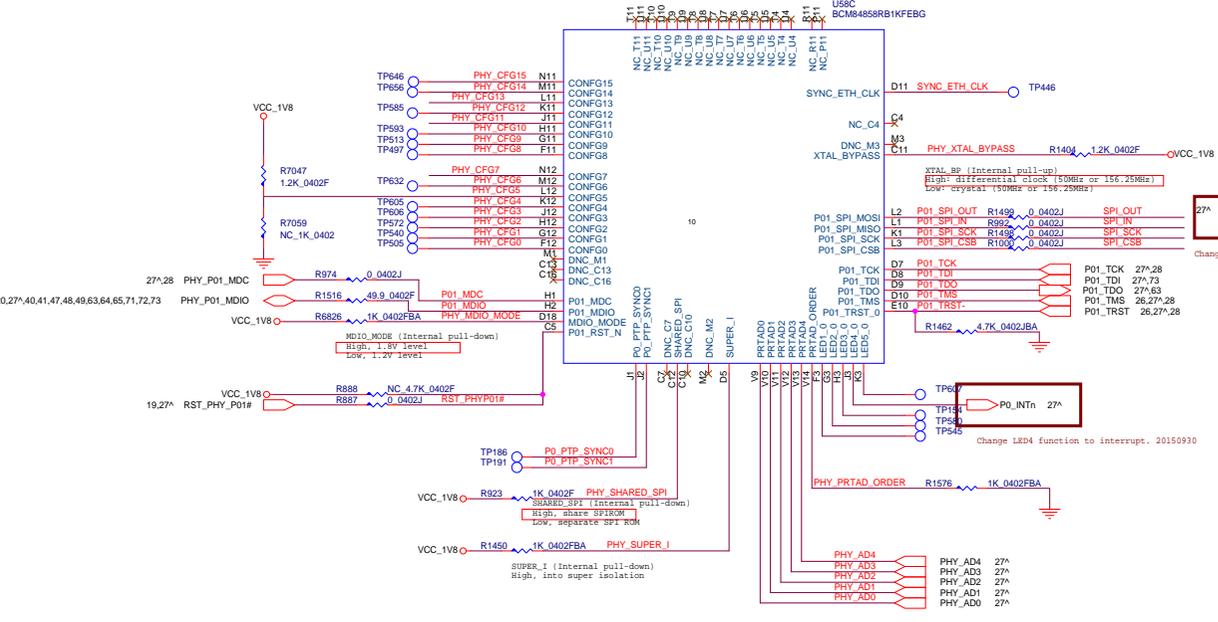
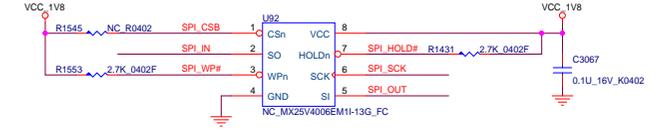
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File		02-01_BCM84848_PHY_A	
Size	Document Number	1ADSS-0XXXXX	
C			Rev 1.1
Date:	Tuesday, September 13, 2016	Sheet	38 of 80



SPI EEPROM

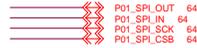
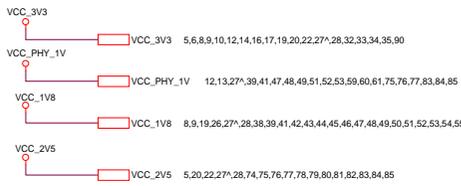


- Config[7]: 10GBT core power down**
 High: Power down 10GBT core
 Low: Power-up 10GBT core
- Config[11]: LED control**
 High: Under user control
 Low: LED 1, 2, 3, 5 are predefined as configured. LED 4 under user control.
- Config[12]:**
 High: Firmware forces 1G fiber
 Low: Firmware forces sets speed of device interfaces to 10G
- Config[13]: SPIROM**
 High: Load FW from SPIROM
 Low: Load FW from MDIO interface

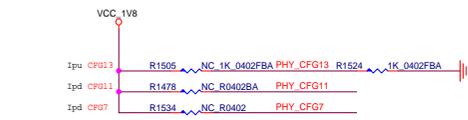
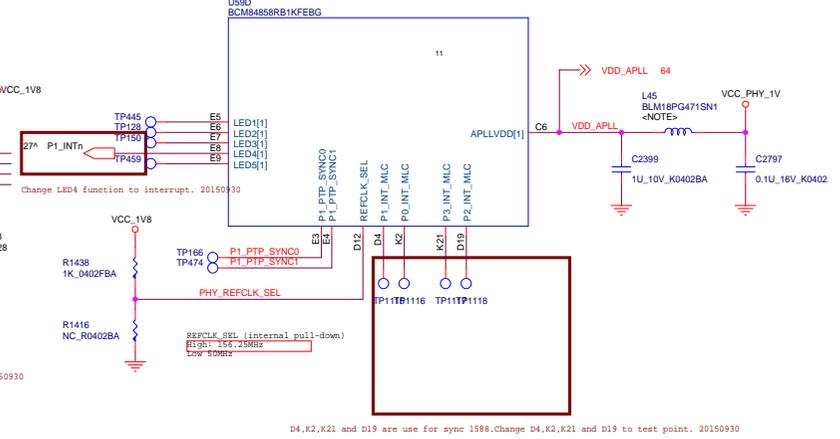
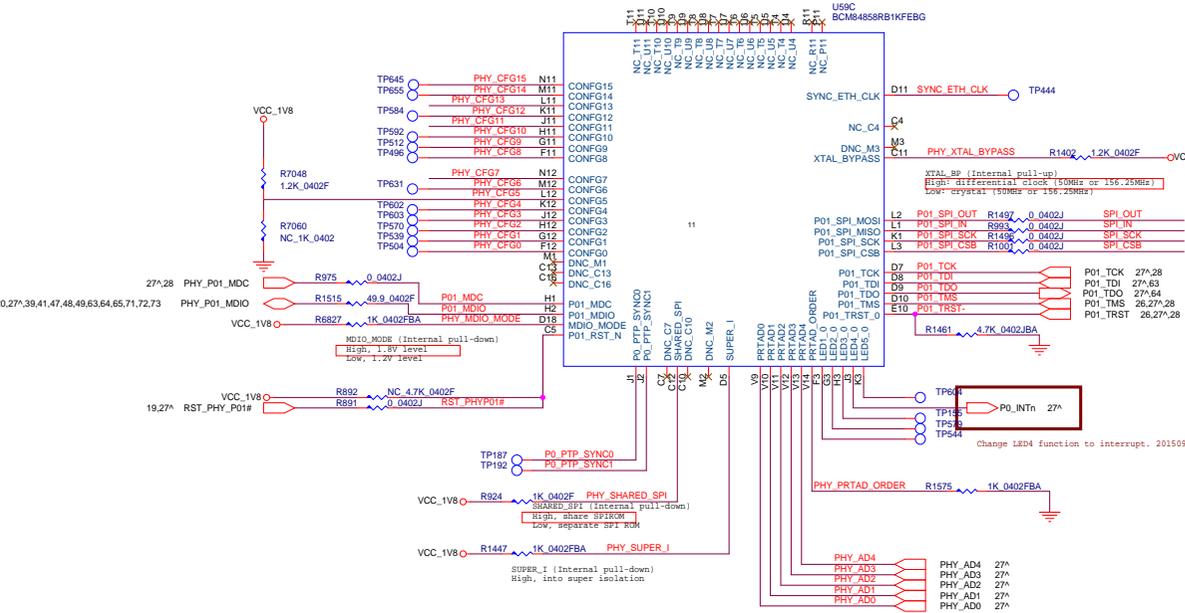
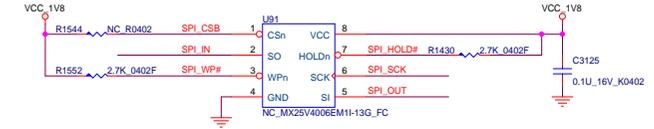
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File		02-01_BCM84848_PHY_A	
Size	Document Number		
C	1ADSS-0XXXXX	Rev	1.1
Date:	Tuesday, September 13, 2016	Sheet	39 of 80



SPI EEPROM

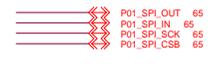
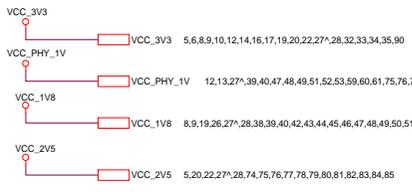


- Config[7]: 10GBT core power down**
 High: Power down 10GBT core
 Low: Power-up 10GBT core
- Config[11]: LED control**
 High: Under user control
 Low: LED 1, 2, 3, 5 are predefined as configured. LED 4 under user control.
- Config[12]:**
 High: Firmware forces 1G fiber
 Low: Firmware forces sets speed of device interfaces to 10G
- Config[13]: SPIROM**
 High: Load FW from SPIROM
 Low: Load FW from MDIO interface

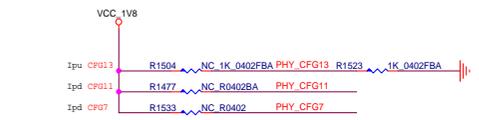
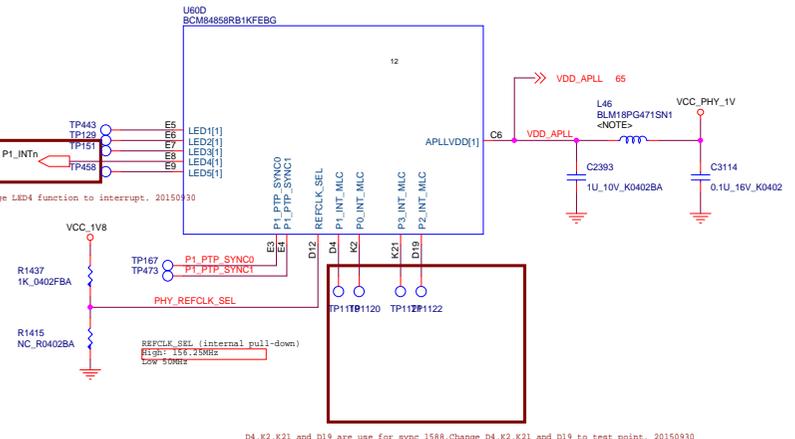
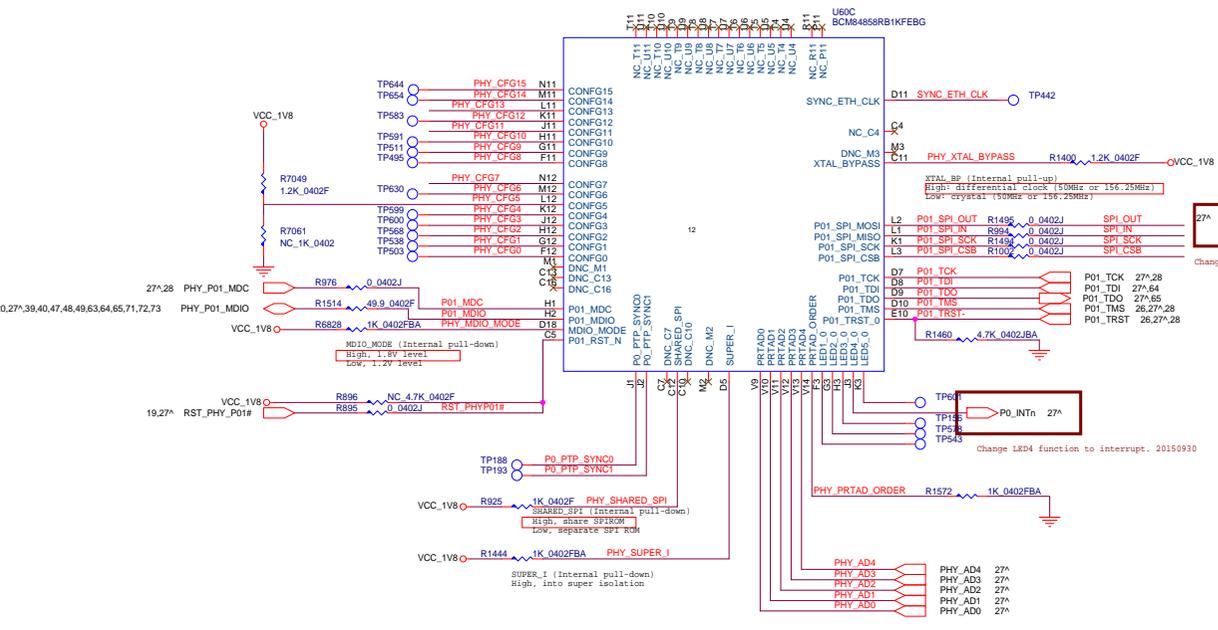
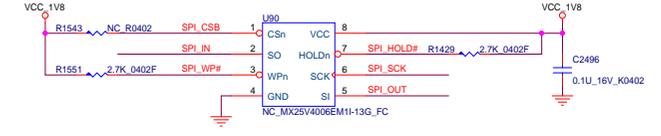
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File	02-01_BCM84848_PHY_A	
Size	Document Number	Rev
C	1ADSS-0XXXXX	1.1
Date:	Tuesday, September 13, 2016	Sheet 40 of 80



SPI EEPROM

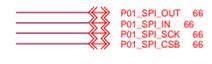
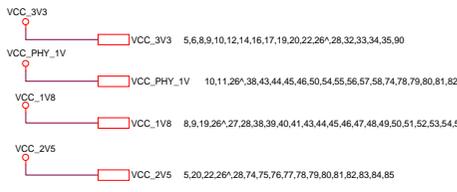


- Config[7]: 10GBT core power down**
 High: Power down 10GBT core
 Low: Power-up 10GBT core
- Config[11]: LED control**
 High: Under user control
 Low: LED 1, 2, 3, 5 are predefined as configured. LED 4 under user control.
- Config[12]:**
 High: Firmware forces 1G fiber
 Low: Firmware forces sets speed of device interfaces to 10G
- Config[13]: SPIROM**
 High: Load FW from SPIROM
 Low: Load FW from MDIO interface

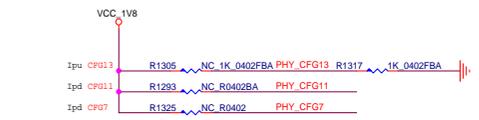
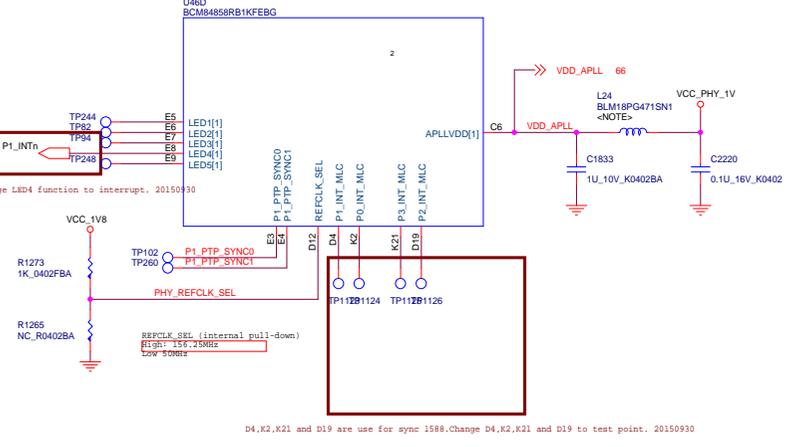
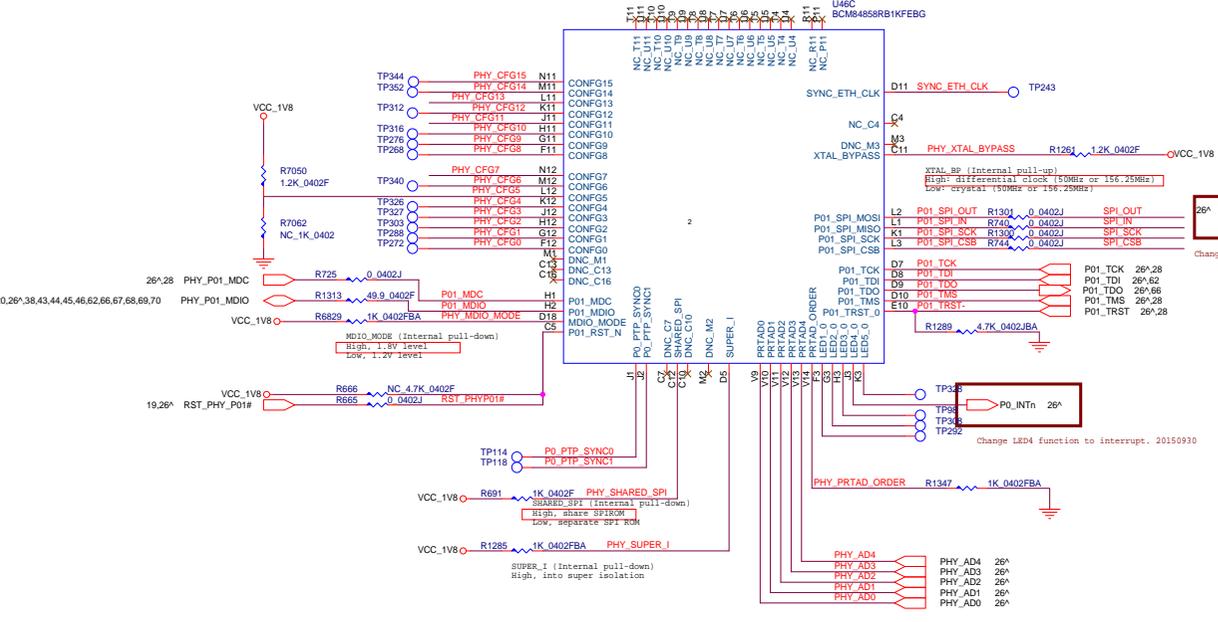
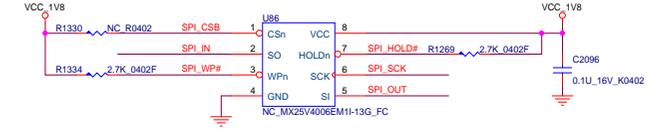
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File		02-01_BCM84848_PHY_A	
Size	Document Number	1ADSS-0XXXXX	
C			Rev 1.1
Date:	Tuesday, September 13, 2016	Sheet	41 of 80



SPI EEPROM

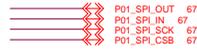
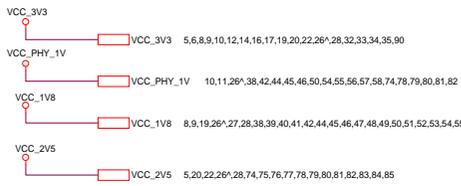


- Config[7]: 10GBT core power down**
 High: Power down 10GBT core
 Low: Power-up 10GBT core
- Config[11]: LED control**
 High: Under user control
 Low: LED 1, 2, 3, 5 are predefined as configured. LED 4 under user control.
- Config[12]:**
 High: Firmware forces 1G fiber
 Low: Firmware forces sets speed of device interfaces to 10G
- Config[13]: SPIROM**
 High: Load FW from SPIROM
 Low: Load FW from MDIO interface

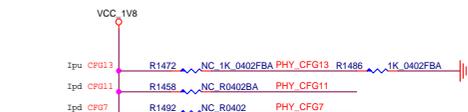
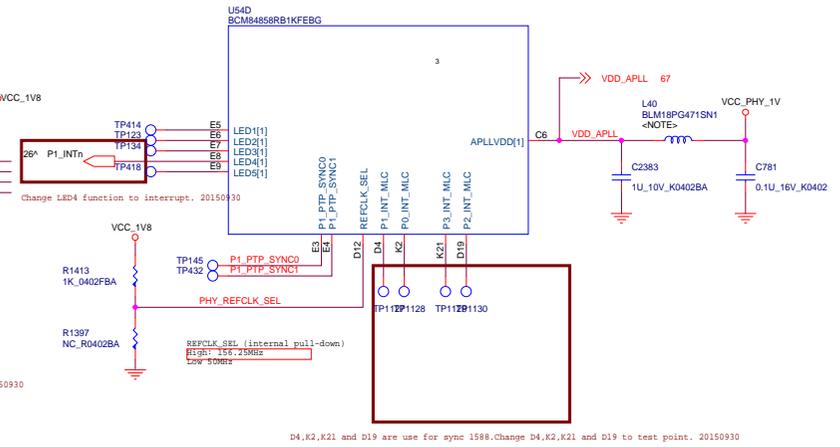
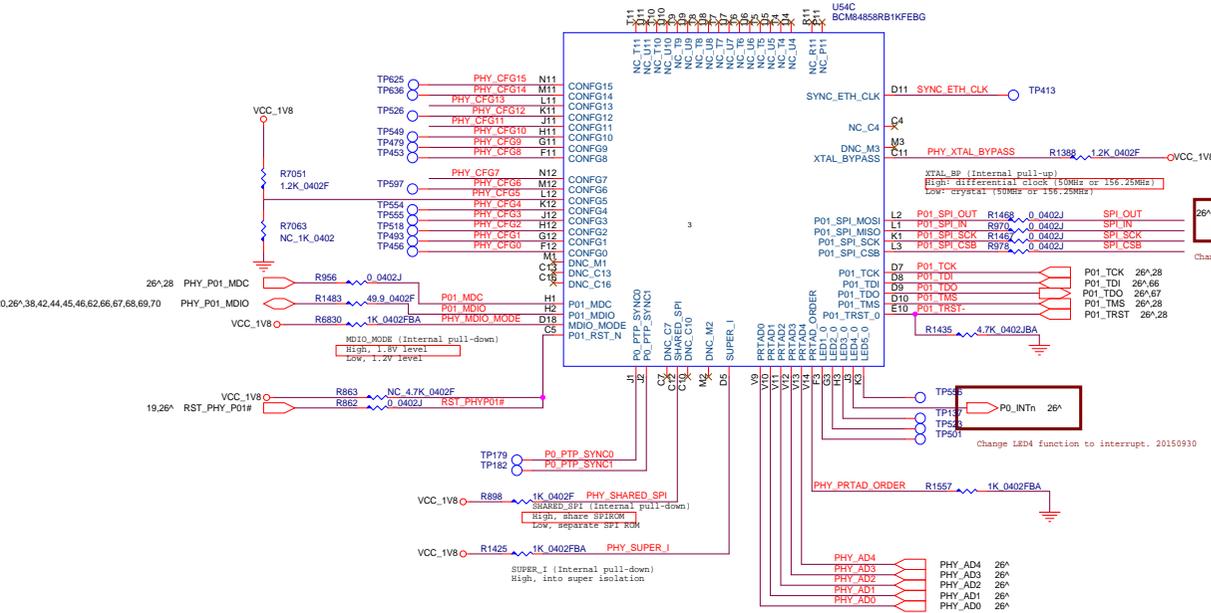
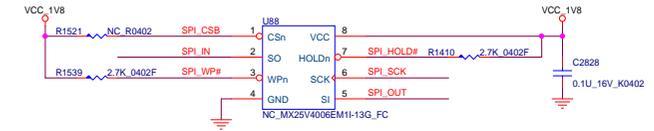
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File		02-01_BCM84848_PHY_A	
Size	Document Number		
C	1ADSS-0XXXXX	Rev	1.1
Date:	Tuesday, September 13, 2016	Sheet	42 of 80



SPI EEPROM



Config[7]: 10GBT core power down

High: Power down 10GBT core
 Low: Power-up 10GBT core

Config[11]: LED control

High: Under user control
 Low: LED 1, 2, 3, 5 are predefined as configured. LED 4 under user control.

Config[12]:

High: Firmware forces 1G fiber
 Low: Firmware forces sets speed of device interfaces to 10G

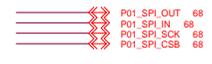
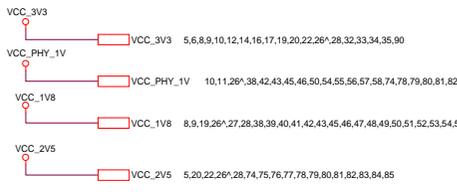
Config[13]: SPIROM

High: Load FW from SPIROM
 Low: Load FW from MDIO interface

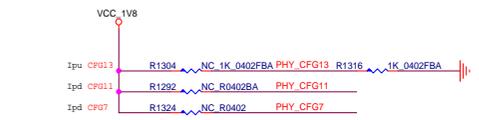
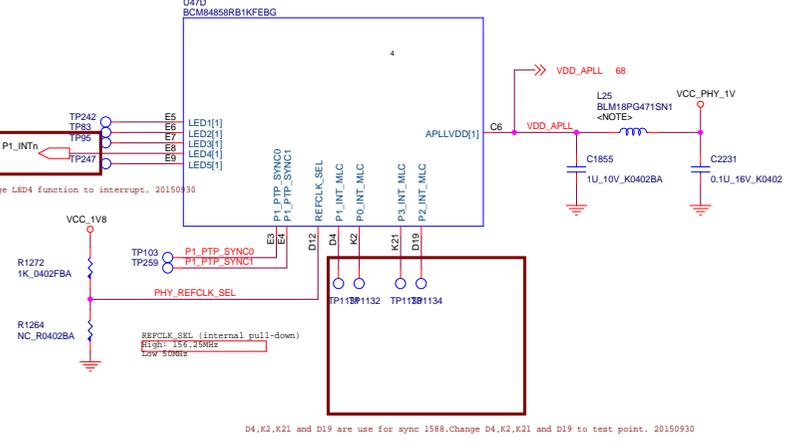
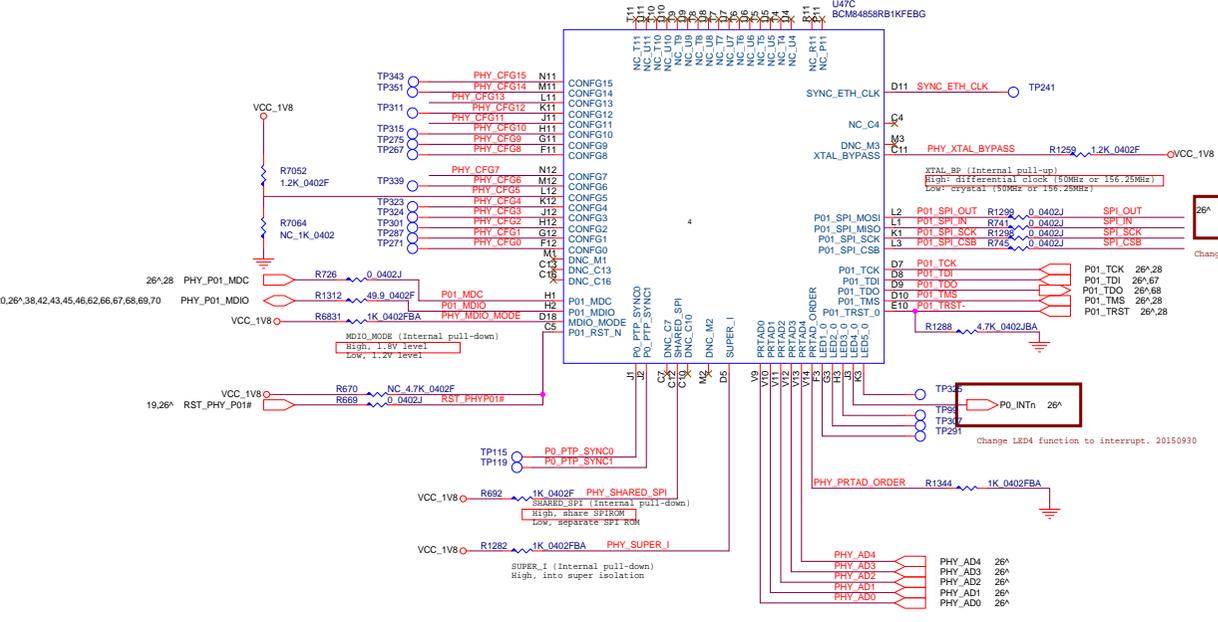
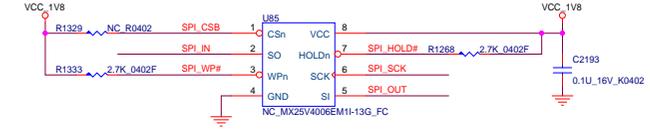
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File		
02-01_BCM84848_PHY_A		
Size	Document Number	Rev
C	1ADSS-0XXXXX	1.1
Date:	Tuesday, September 13, 2016	Sheet 43 of 80



SPI EEPROM

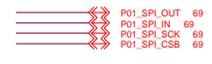
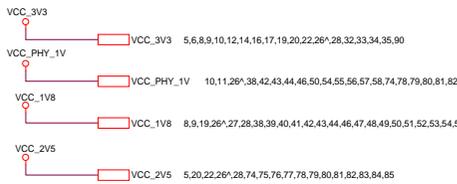


- Config[7]: 10GBT core power down
 - High: Power down 10GBT core
 - Low: Power-up 10GBT core
- Config[11]: LED control
 - High: Under user control
 - Low: LED 1, 2, 3, 5 are predefined as configured. LED 4 under user control.
- Config[12]:
 - High: Firmware forces 1G fiber
 - Low: Firmware forces sets speed of device interfaces to 10G
- Config[13]: SPIROM
 - High: Load FW from SPIROM
 - Low: Load FW from MDIO interface

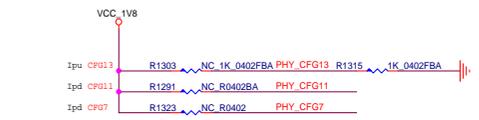
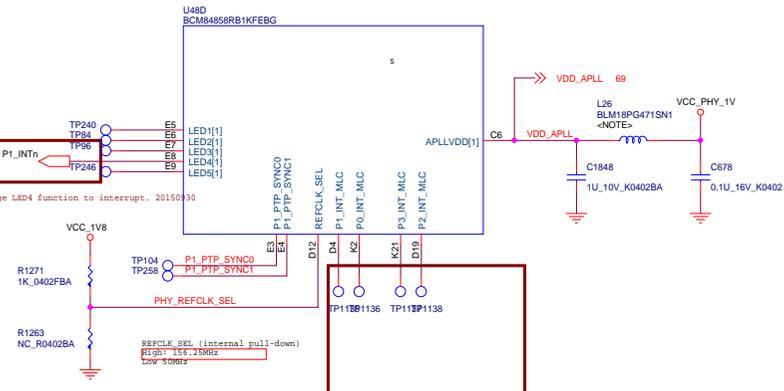
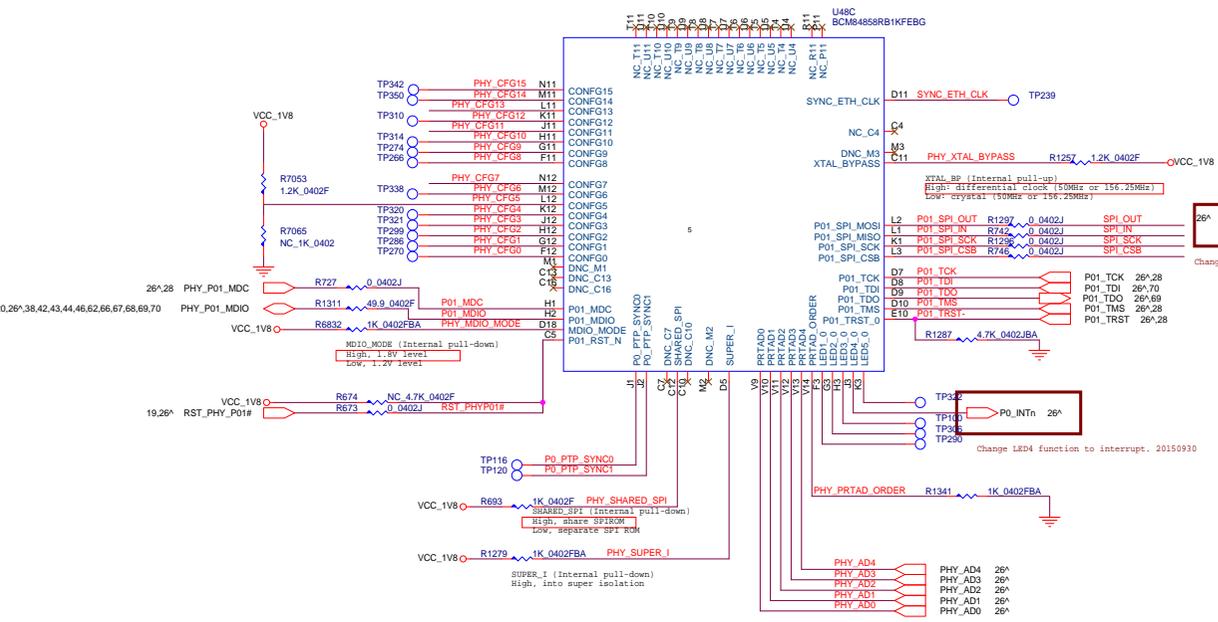
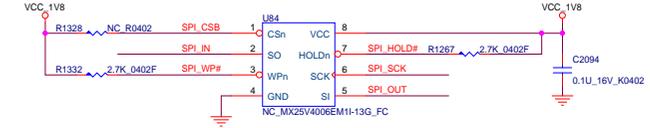
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File	02-01_BCM84848_PHY_A		
Size	Document Number		Rev
C	1ADSS-0XXXXX		1.1
Date:	Tuesday, September 13, 2016	Sheet	44 of 80



SPI EEPROM

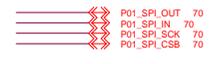
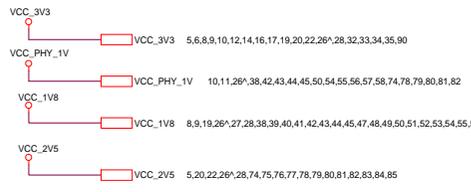


- Config[7]: 10GBT core power down**
High: Power down 10GBT core
Low: Power-up 10GBT core
- Config[11]: LED control**
High: Under user control
Low: LED 1, 2, 3, 5 are predefined as configured. LED 4 under user control.
- Config[12]:**
High: Firmware forces 1G fiber
Low: Firmware forces sets speed of device interfaces to 10G
- Config[13]: SPIROM**
High: Load FW from SPIROM
Low: Load FW from MDIO interface

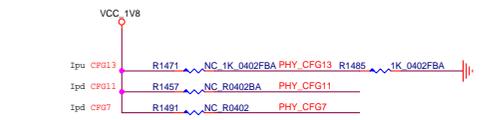
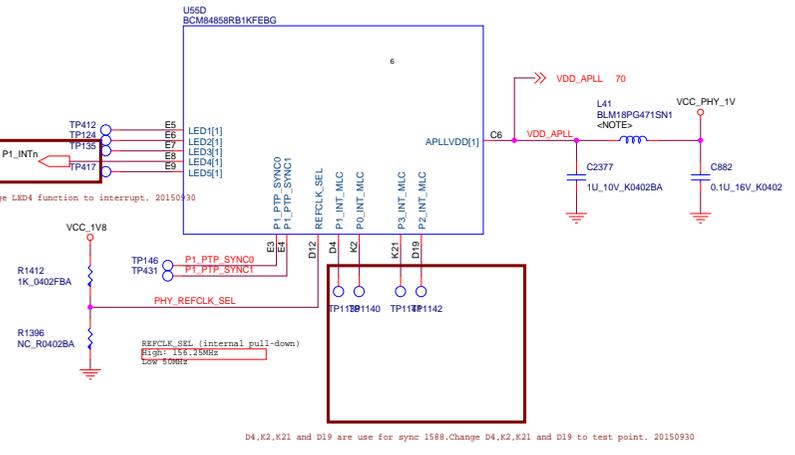
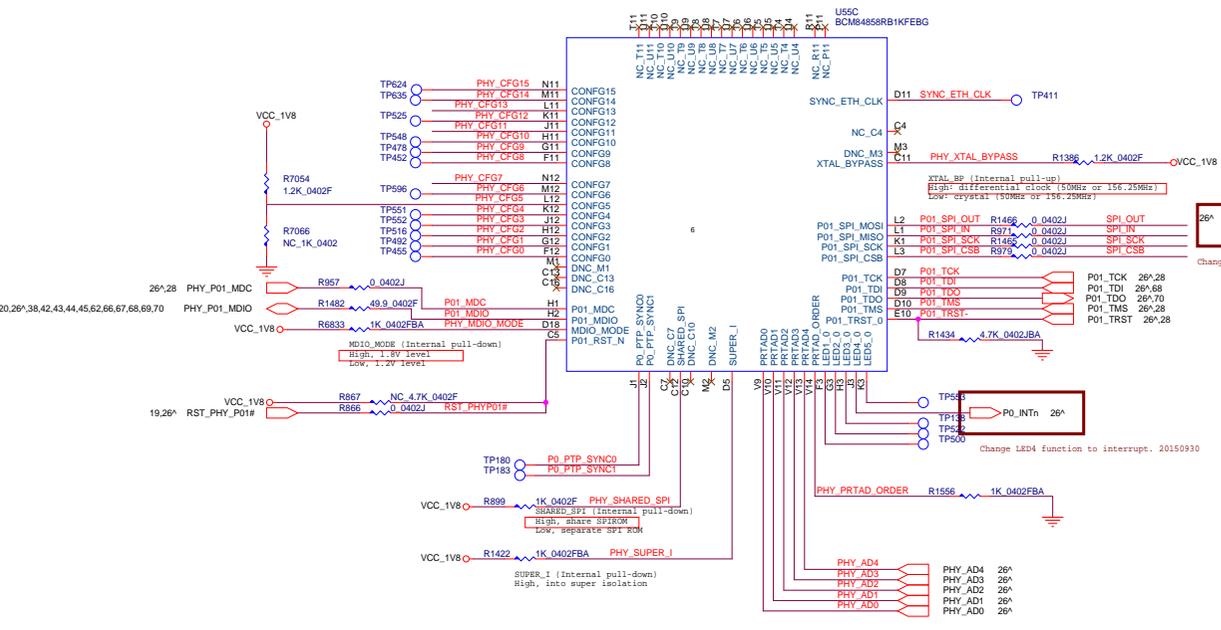
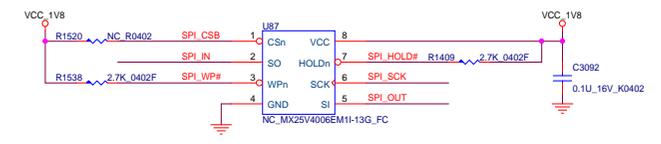
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File		02-01_BCM84848_PHY_A	
Size	Document Number		
C	1ADSS-0XXXXX	Rev	1.1
Date:	Tuesday, September 13, 2016	Sheet	45 of 80



SPI EEPROM

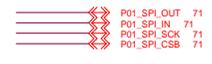
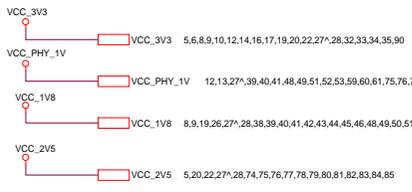


- Config[7]: 10GBT core power down**
 High: Power down 10GBT core
 Low: Power-up 10GBT core
- Config[11]: LED control**
 High: Under user control
 Low: LED 1, 2, 3, 5 are predefined as configured. LED 4 under user control.
- Config[12]:**
 High: Firmware forces 1G fiber
 Low: Firmware forces sets speed of device interfaces to 10G
- Config[13]: SPIROM**
 High: Load FW from SPIROM
 Low: Load FW from MDIO interface

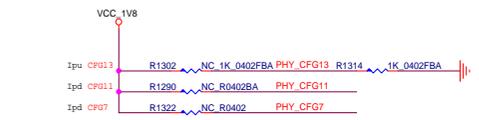
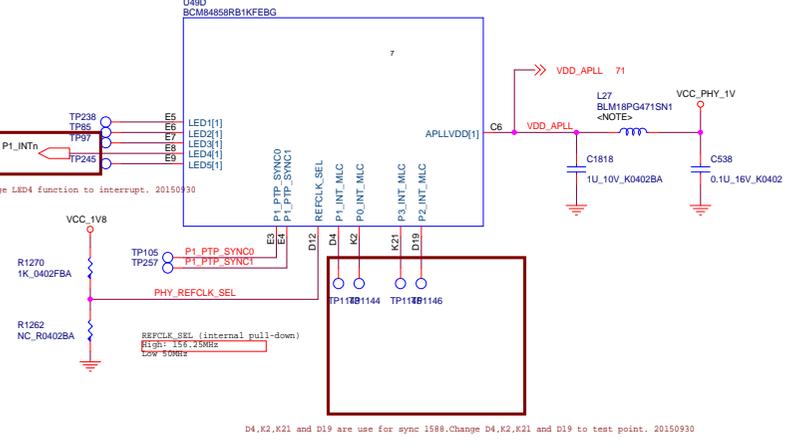
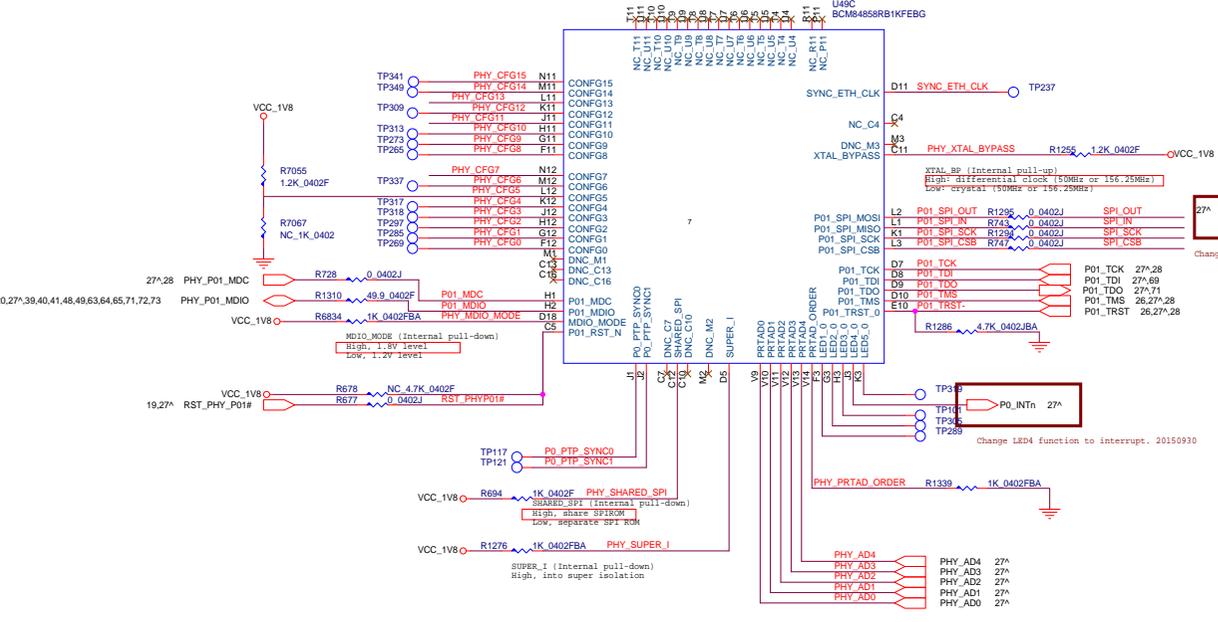
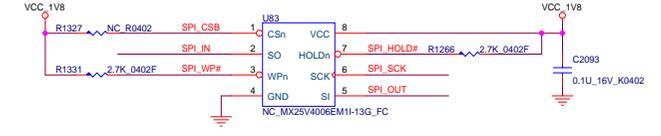
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File	02-01_BCM84848_PHY_A	
Size	Document Number	Rev
C	1ADSS-0XXXXX	1.1
Date:	Tuesday, September 13, 2016	Sheet 46 of 80



SPI EEPROM

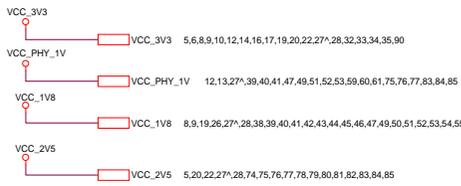


- Config[7]: 10GBT core power down**
 High: Power down 10GBT core
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 High: Firmware forces 1G fiber
 Low: Firmware forces sets speed of device interfaces to 10G
- Config[13]: SPIROM**
 High: Load FW from SPIROM
 Low: Load FW from MDIO interface

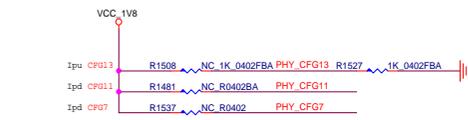
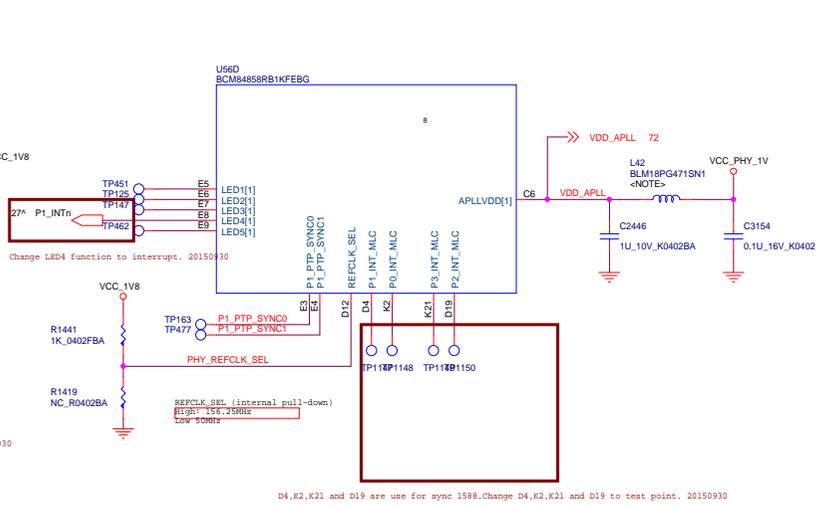
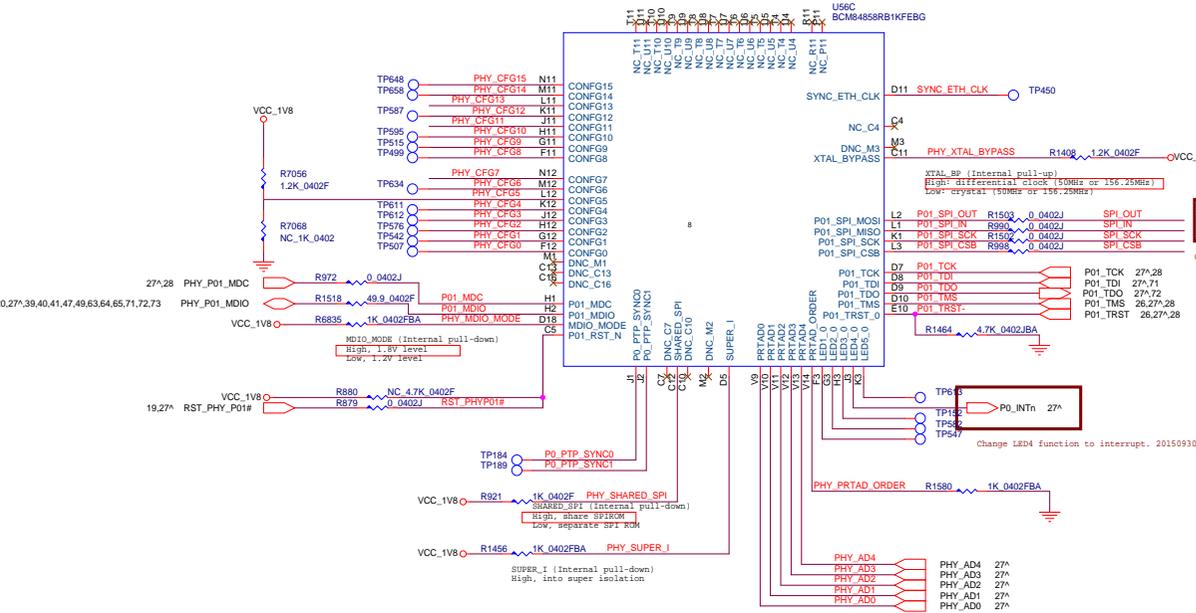
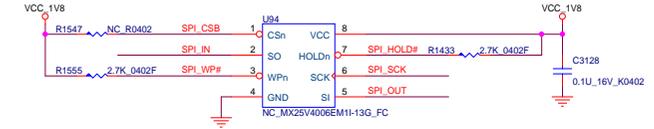
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File		
02-01_BCM84848_PHY_A		
Size	Document Number	Rev
C	1ADSS-0XXXXX	1.1
Date:	Tuesday, September 13, 2016	Sheet 47 of 80



SPI EEPROM

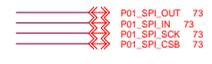


- Config[7]: 10GBT core power down
High: Power down 10GBT core
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- Config[11]: LED control
High: Under user control
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- Config[12]:
High: Firmware forces 1G fiber
Low: Firmware forces sets speed of device interfaces to 10G
- Config[13]: SPIROM
High: Load FW from SPIROM
Low: Load FW from MDIO interface

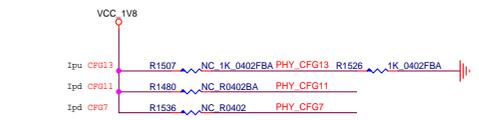
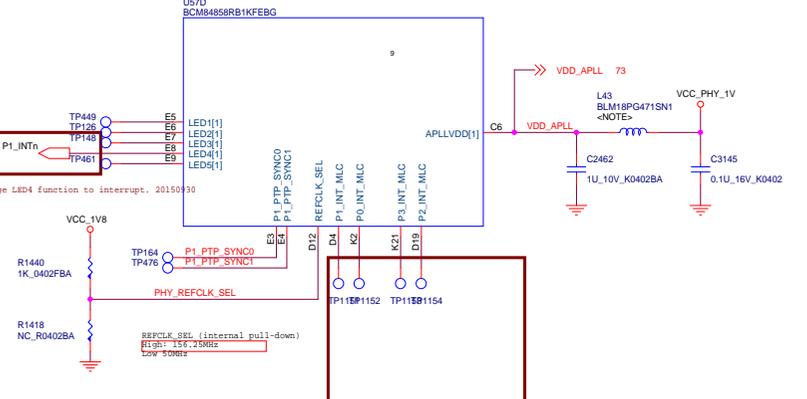
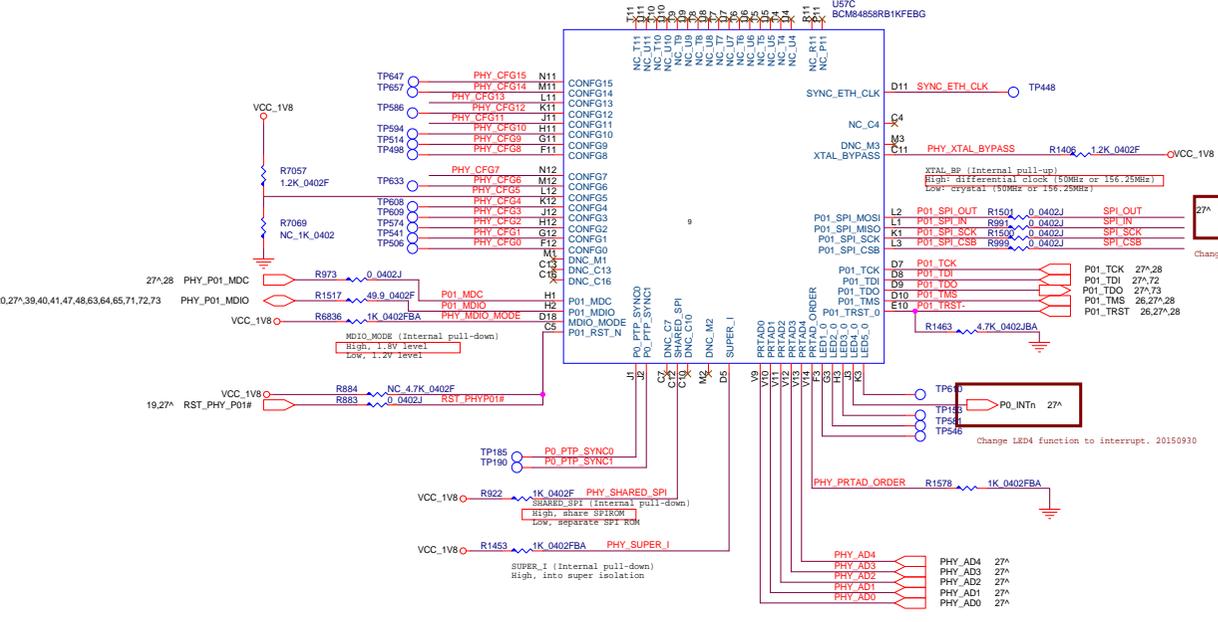
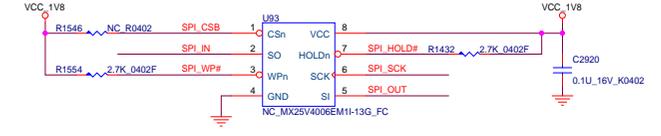
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File		02-01_BCM84848_PHY_A	
Size	Document Number		
C	1ADSS-0XXXXX	Rev	1.1
Date:	Tuesday, September 13, 2016	Sheet	48 of 80



SPI EEPROM

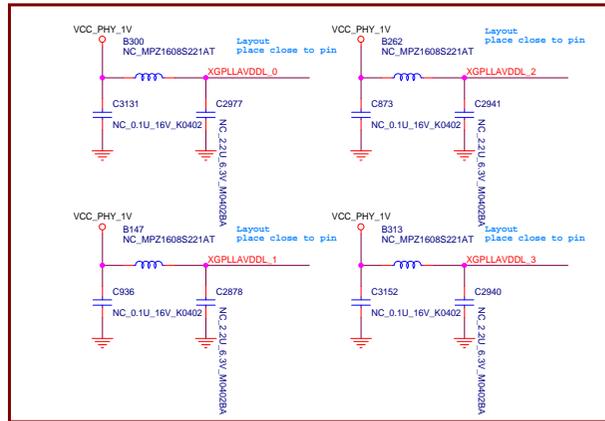


- Config[7]: 10GBT core power down**
 High: Power down 10GBT core
 Low: Power-up 10GBT core
- Config[11]: LED control**
 High: Under user control
 Low: LED 1, 2, 3, 5 are predefined as configured. LED 4 under user control.
- Config[12]:**
 High: Firmware forces 1G fiber
 Low: Firmware forces sets speed of device interfaces to 10G
- Config[13]: SPIROM**
 High: Load FW from SPIROM
 Low: Load FW from MDIO interface

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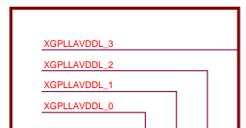
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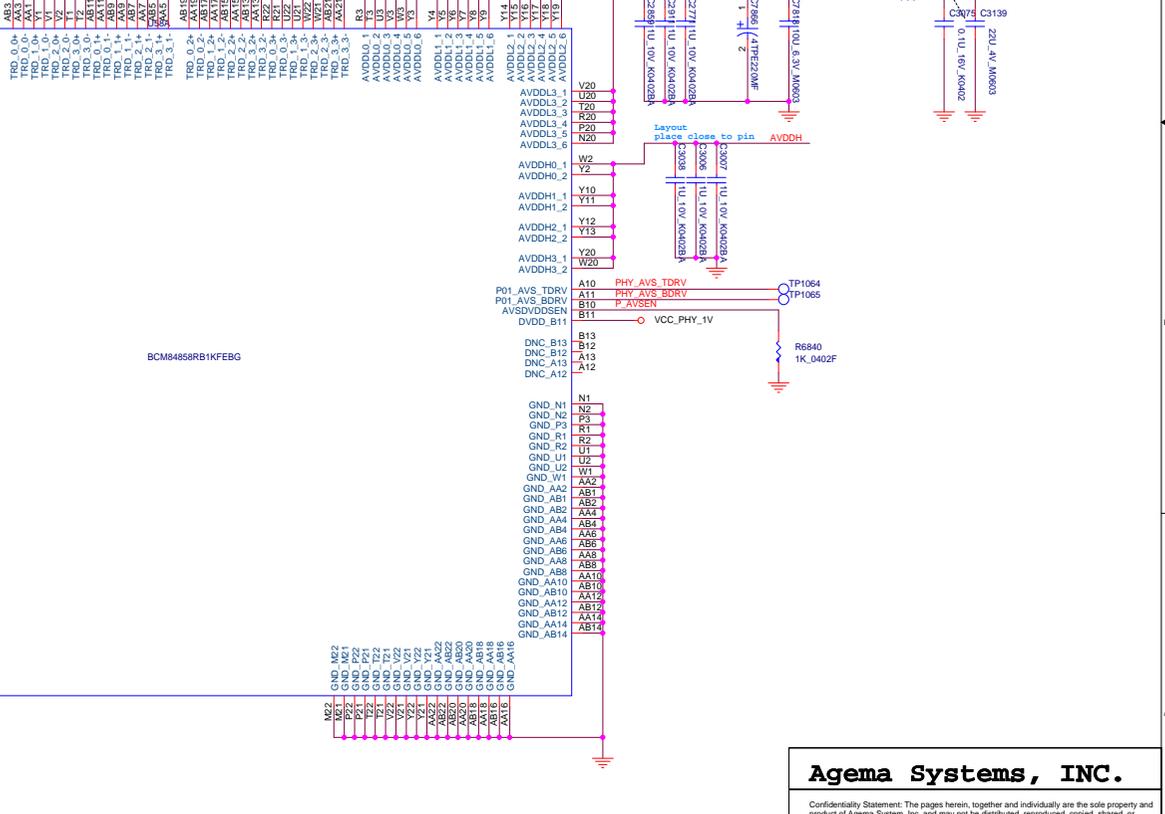
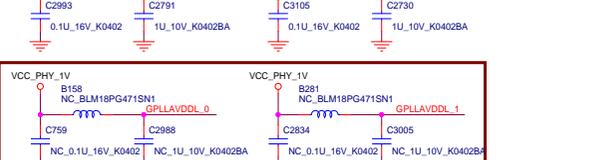
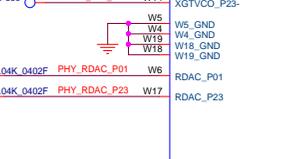
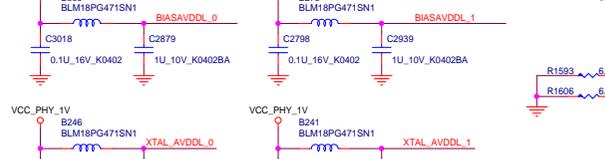
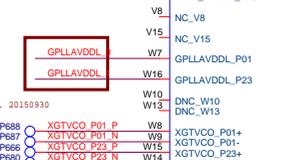
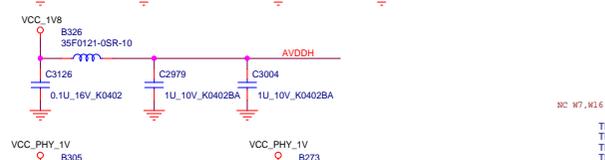
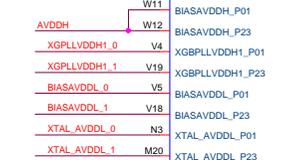
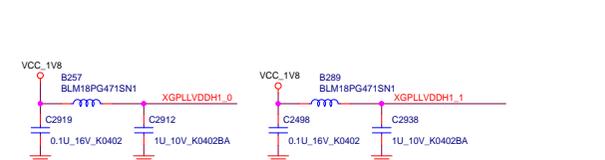
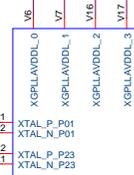
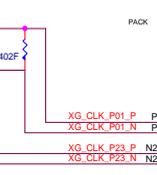
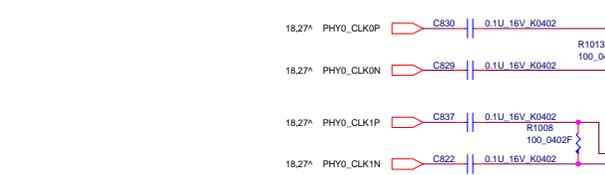


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27A.89	TRD_0_0-	TRD_0_0-
27A.89	TRD_1_0+	TRD_1_0+
27A.89	TRD_1_0-	TRD_1_0-
27A.89	TRD_2_0+	TRD_2_0+
27A.89	TRD_2_0-	TRD_2_0-
27A.89	TRD_3_0+	TRD_3_0+
27A.89	TRD_3_0-	TRD_3_0-
27A.89	TRD_0_1+	TRD_0_1+
27A.89	TRD_0_1-	TRD_0_1-
27A.89	TRD_1_1+	TRD_1_1+
27A.89	TRD_1_1-	TRD_1_1-
27A.89	TRD_2_1+	TRD_2_1+
27A.89	TRD_2_1-	TRD_2_1-
27A.89	TRD_3_1+	TRD_3_1+
27A.89	TRD_3_1-	TRD_3_1-

NC V6,V7,V16 and V17, 20150930



TRD_0_0+	AB3
TRD_0_0-	AA3
TRD_1_0+	AA1
TRD_1_0-	AA1
TRD_2_0+	V1
TRD_2_0-	V1
TRD_3_0+	V1
TRD_3_0-	V1
TRD_0_1+	AA11
TRD_0_1-	AA11
TRD_1_1+	AA9
TRD_1_1-	AA9
TRD_2_1+	AA7
TRD_2_1-	AA7
TRD_3_1+	AA5
TRD_3_1-	AA5
TRD_0_2+	AA19
TRD_0_2-	AA19
TRD_1_2+	AA17
TRD_1_2-	AA17
TRD_2_2+	AA5
TRD_2_2-	AA5
TRD_3_2+	AA3
TRD_3_2-	AA3
TRD_0_3+	R21
TRD_0_3-	R21
TRD_1_3+	U22
TRD_1_3-	U22
TRD_2_3+	W22
TRD_2_3-	W22
TRD_3_3+	AA21
TRD_3_3-	AA21
TRD_0_4+	AA19
TRD_0_4-	AA19
TRD_1_4+	AA17
TRD_1_4-	AA17
TRD_2_4+	AA5
TRD_2_4-	AA5
TRD_3_4+	AA3
TRD_3_4-	AA3



BCM8488B1KFEFG

NC GPLLAVDDL, 20150930

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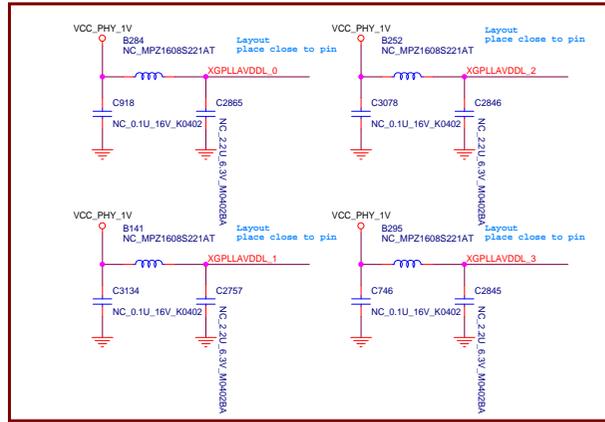
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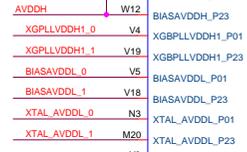
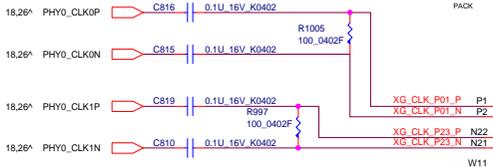
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Date: **Tuesday, September 13, 2016**

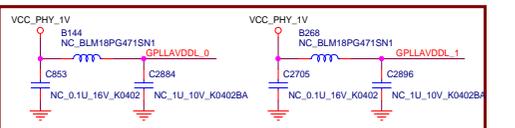
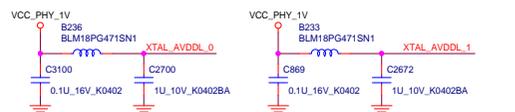
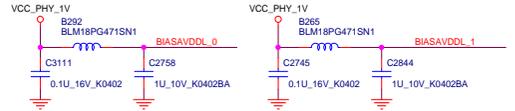
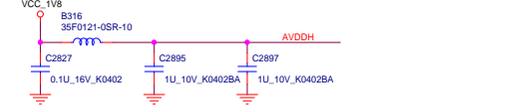
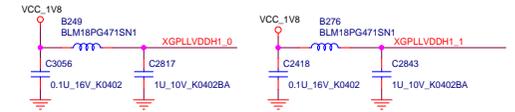
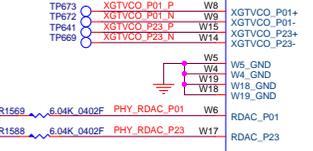


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26A.87	TRD_0_0-	TRD_0_0-
26A.87	TRD_1_0+	TRD_1_0+
26A.87	TRD_1_0-	TRD_1_0-
26A.87	TRD_2_0+	TRD_2_0+
26A.87	TRD_2_0-	TRD_2_0-
26A.87	TRD_3_0+	TRD_3_0+
26A.87	TRD_3_0-	TRD_3_0-
26A.87	TRD_0_1+	TRD_0_1+
26A.87	TRD_0_1-	TRD_0_1-
26A.87	TRD_1_1+	TRD_1_1+
26A.87	TRD_1_1-	TRD_1_1-
26A.87	TRD_2_1+	TRD_2_1+
26A.87	TRD_2_1-	TRD_2_1-
26A.87	TRD_3_1+	TRD_3_1+
26A.87	TRD_3_1-	TRD_3_1-
26A.87	TRD_0_2+	TRD_0_2+
26A.87	TRD_0_2-	TRD_0_2-
26A.87	TRD_1_2+	TRD_1_2+
26A.87	TRD_1_2-	TRD_1_2-
26A.87	TRD_2_2+	TRD_2_2+
26A.87	TRD_2_2-	TRD_2_2-
26A.87	TRD_3_2+	TRD_3_2+
26A.87	TRD_3_2-	TRD_3_2-
26A.87	TRD_0_3+	TRD_0_3+
26A.87	TRD_0_3-	TRD_0_3-
26A.87	TRD_1_3+	TRD_1_3+
26A.87	TRD_1_3-	TRD_1_3-
26A.87	TRD_2_3+	TRD_2_3+
26A.87	TRD_2_3-	TRD_2_3-
26A.87	TRD_3_3+	TRD_3_3+
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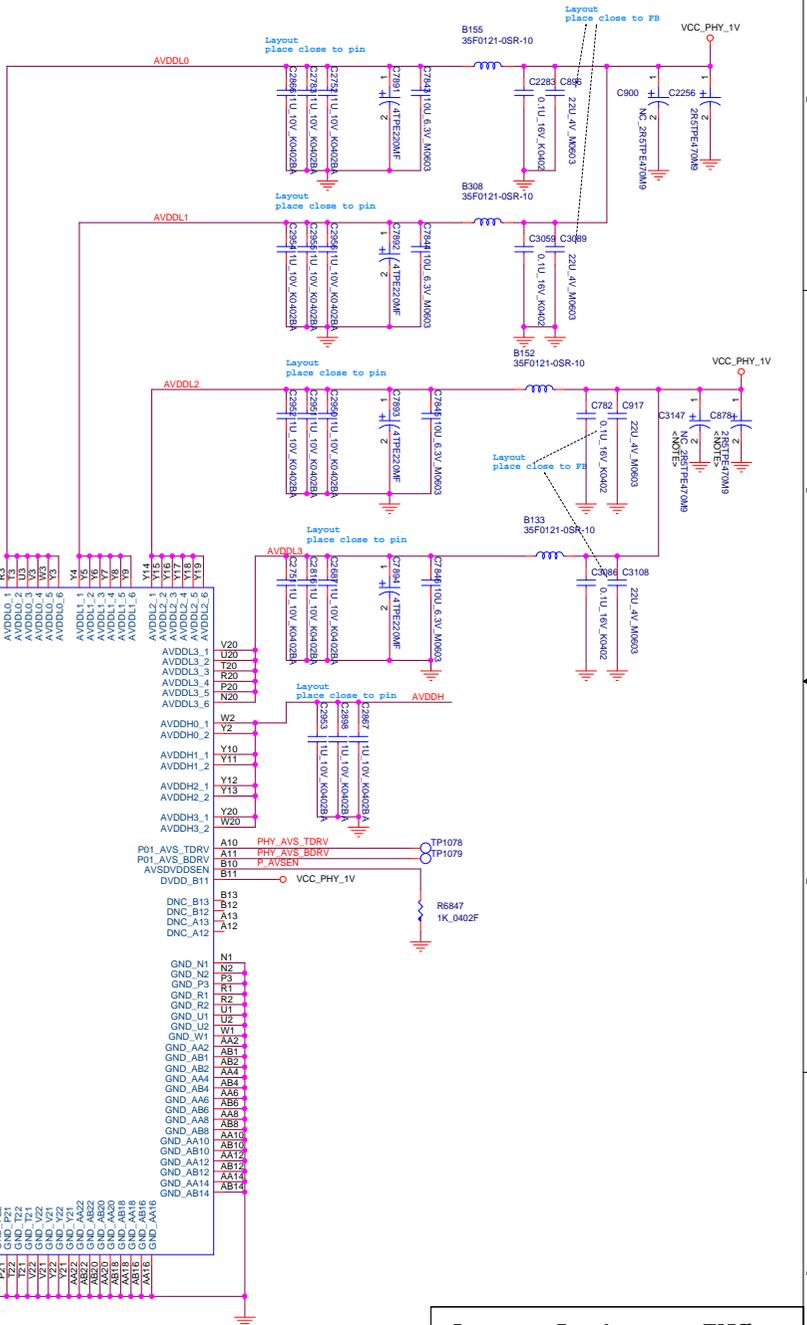
NC V6,V7,V16 and V17, 20150930



NC W7,W16, 20150930



NC GPLLAVDDL, 20150930



BCM84868B1KFE6G

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M21	GND_M21	GND_M21
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M19	GND_M19	GND_M19
M18	GND_M18	GND_M18
M17	GND_M17	GND_M17
M16	GND_M16	GND_M16
M15	GND_M15	GND_M15
M14	GND_M14	GND_M14
M13	GND_M13	GND_M13
M12	GND_M12	GND_M12
M11	GND_M11	GND_M11
M10	GND_M10	GND_M10
M9	GND_M9	GND_M9
M8	GND_M8	GND_M8
M7	GND_M7	GND_M7
M6	GND_M6	GND_M6
M5	GND_M5	GND_M5
M4	GND_M4	GND_M4
M3	GND_M3	GND_M3
M2	GND_M2	GND_M2
M1	GND_M1	GND_M1
M0	GND_M0	GND_M0
M22	GND_M22	GND_M22
M21	GND_M21	GND_M21
M20	GND_M20	GND_M20
M19	GND_M19	GND_M19
M18	GND_M18	GND_M18
M17	GND_M17	GND_M17
M16	GND_M16	GND_M16
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M13	GND_M13	GND_M13
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M8	GND_M8	GND_M8
M7	GND_M7	GND_M7
M6	GND_M6	GND_M6
M5	GND_M5	GND_M5
M4	GND_M4	GND_M4
M3	GND_M3	GND_M3
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M1	GND_M1	GND_M1
M0	GND_M0	GND_M0

Agema Systems, INC.

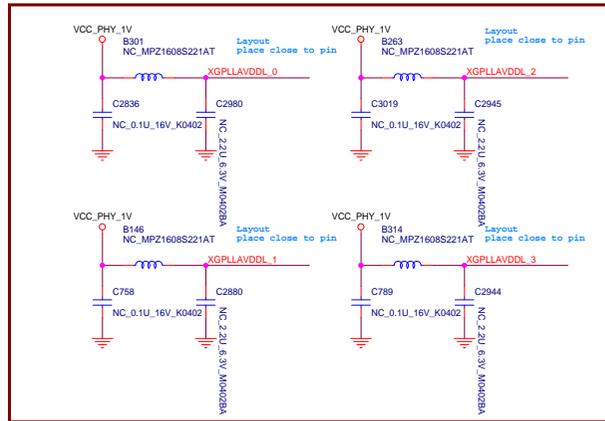
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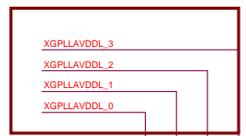
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Date: **Tuesday, September 13, 2016**

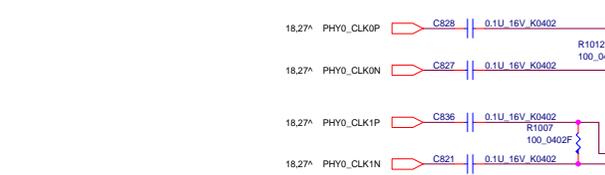


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27A.88	TRD_0_0-	TRD_0_0-
27A.88	TRD_1_0+	TRD_1_0+
27A.88	TRD_1_0-	TRD_1_0-
27A.88	TRD_2_0+	TRD_2_0+
27A.88	TRD_2_0-	TRD_2_0-
27A.88	TRD_3_0+	TRD_3_0+
27A.88	TRD_3_0-	TRD_3_0-
27A.88	TRD_0_1+	TRD_0_1+
27A.88	TRD_0_1-	TRD_0_1-
27A.88	TRD_1_1+	TRD_1_1+
27A.88	TRD_1_1-	TRD_1_1-
27A.88	TRD_2_1+	TRD_2_1+
27A.88	TRD_2_1-	TRD_2_1-
27A.88	TRD_3_1+	TRD_3_1+
27A.88	TRD_3_1-	TRD_3_1-
27A.88	TRD_0_2+	TRD_0_2+
27A.88	TRD_0_2-	TRD_0_2-
27A.88	TRD_1_2+	TRD_1_2+
27A.88	TRD_1_2-	TRD_1_2-
27A.88	TRD_2_2+	TRD_2_2+
27A.88	TRD_2_2-	TRD_2_2-
27A.88	TRD_3_2+	TRD_3_2+
27A.88	TRD_3_2-	TRD_3_2-
27A.88	TRD_0_3+	TRD_0_3+
27A.88	TRD_0_3-	TRD_0_3-
27A.88	TRD_1_3+	TRD_1_3+
27A.88	TRD_1_3-	TRD_1_3-
27A.88	TRD_2_3+	TRD_2_3+
27A.88	TRD_2_3-	TRD_2_3-
27A.88	TRD_3_3+	TRD_3_3+
27A.88	TRD_3_3-	TRD_3_3-

NC V6,V7,V16 and V17, 20150930

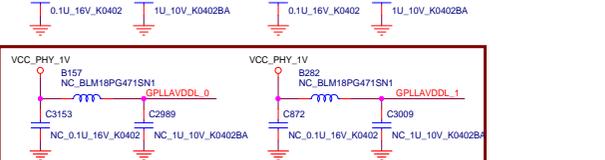
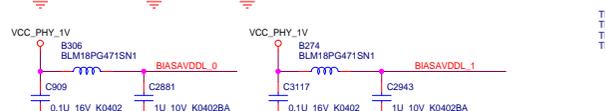
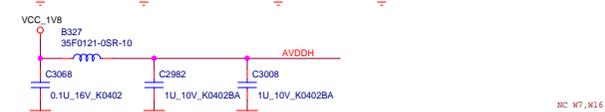
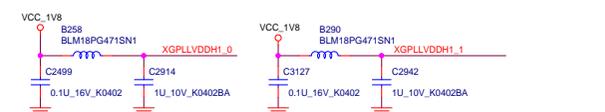


TRD_0_0+	AB3
TRD_0_0-	AA3
TRD_1_0+	AA1
TRD_1_0-	VA1
TRD_2_0+	V1
TRD_2_0-	V1
TRD_3_0+	V1
TRD_3_0-	V1
TRD_0_1+	AA11
TRD_0_1-	AA11
TRD_1_1+	AA9
TRD_1_1-	AA7
TRD_2_1+	AA5
TRD_2_1-	AA3
TRD_3_1+	AA1
TRD_3_1-	AA1
TRD_0_2+	AA19
TRD_0_2-	AA19
TRD_1_2+	AA17
TRD_1_2-	AA17
TRD_2_2+	AA15
TRD_2_2-	AA15
TRD_3_2+	AA13
TRD_3_2-	AA13
TRD_0_3+	AA11
TRD_0_3-	AA11
TRD_1_3+	AA9
TRD_1_3-	AA9
TRD_2_3+	AA7
TRD_2_3-	AA7
TRD_3_3+	AA5
TRD_3_3-	AA5
TRD_0_4+	AA19
TRD_0_4-	AA19
TRD_1_4+	AA17
TRD_1_4-	AA17
TRD_2_4+	AA15
TRD_2_4-	AA15
TRD_3_4+	AA13
TRD_3_4-	AA13
TRD_0_5+	AA11
TRD_0_5-	AA11
TRD_1_5+	AA9
TRD_1_5-	AA9
TRD_2_5+	AA7
TRD_2_5-	AA7
TRD_3_5+	AA5
TRD_3_5-	AA5

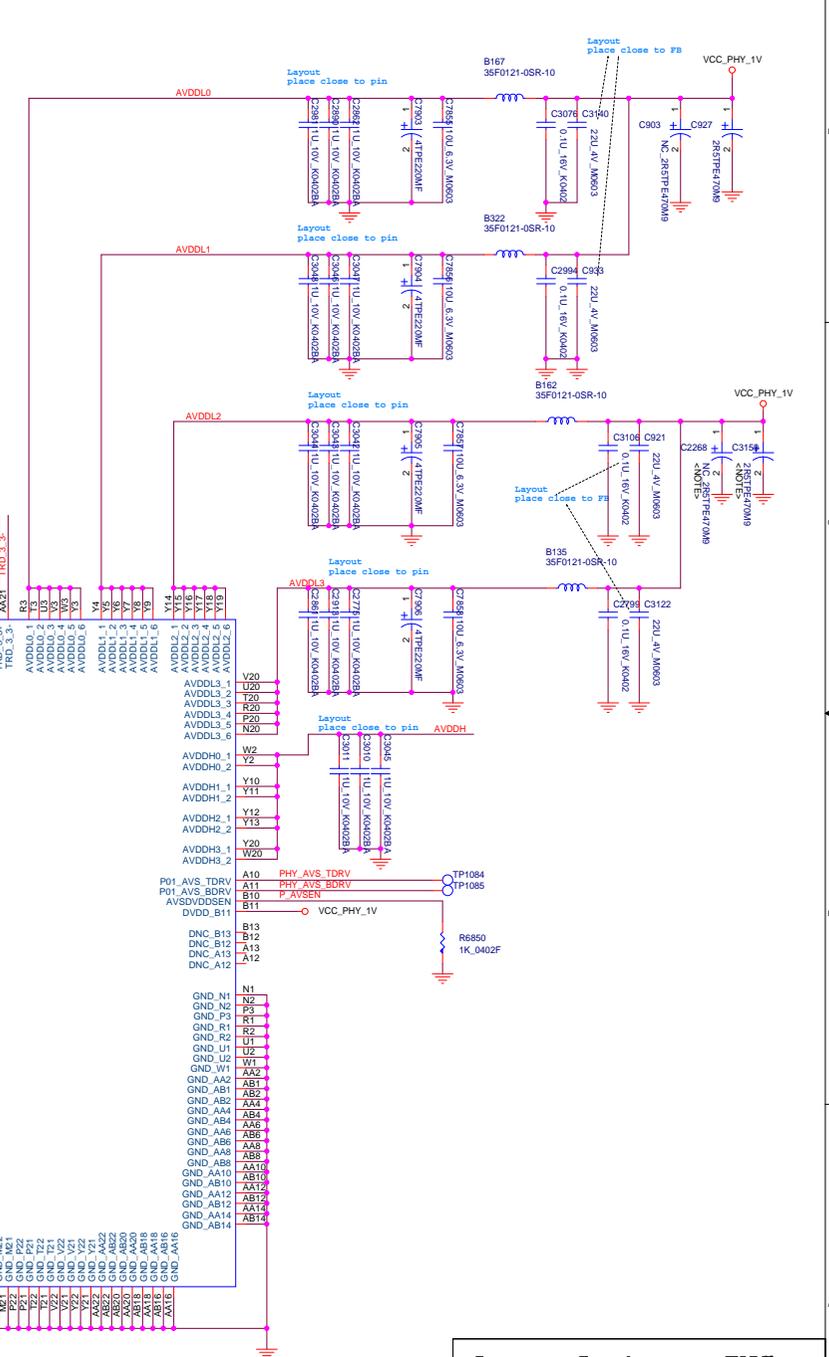


XGPLLAVDDL_0	AB3
XGPLLAVDDL_1	AA3
XGPLLAVDDL_2	VA1
XGPLLAVDDL_3	V1
XTAL_P_P01	P1
XTAL_N_P01	P2
XTAL_P_P23	N22
XTAL_N_P23	N21
BIASAVDDH_P01	W11
BIASAVDDH_P23	W12
XGBPLLVDDH1_P01	V4
XGBPLLVDDH1_P23	V19
BIASAVDDL_P01	V5
BIASAVDDL_P23	V18
XTAL_AVDDL_0	N3
XTAL_AVDDL_P01	M20
XTAL_AVDDL_P23	M20
NC_V8	V8
NC_V15	V15
GPLLAVDDL	W7
GPLLAVDDL_P01	W10
GPLLAVDDL_P23	W16
DNC_W10	W13
DNC_W13	W13
XGTVCCO_P01_P	W8
XGTVCCO_P01_N	W9
XGTVCCO_P23_P	W15
XGTVCCO_P23_N	W14
W5_GND	W5
W4_GND	W4
W18_GND	W18
W19_GND	W19
PHY_RDAC_P01	W6
PHY_RDAC_P23	W17

NC W7,W16, 20150930



NC GPLLAVDDL, 20150930



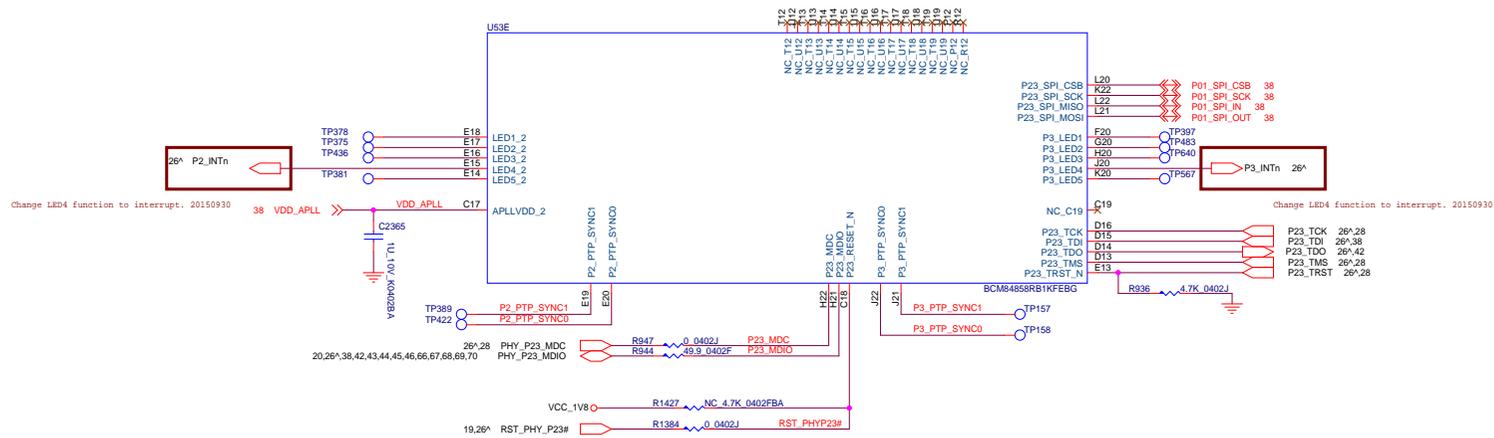
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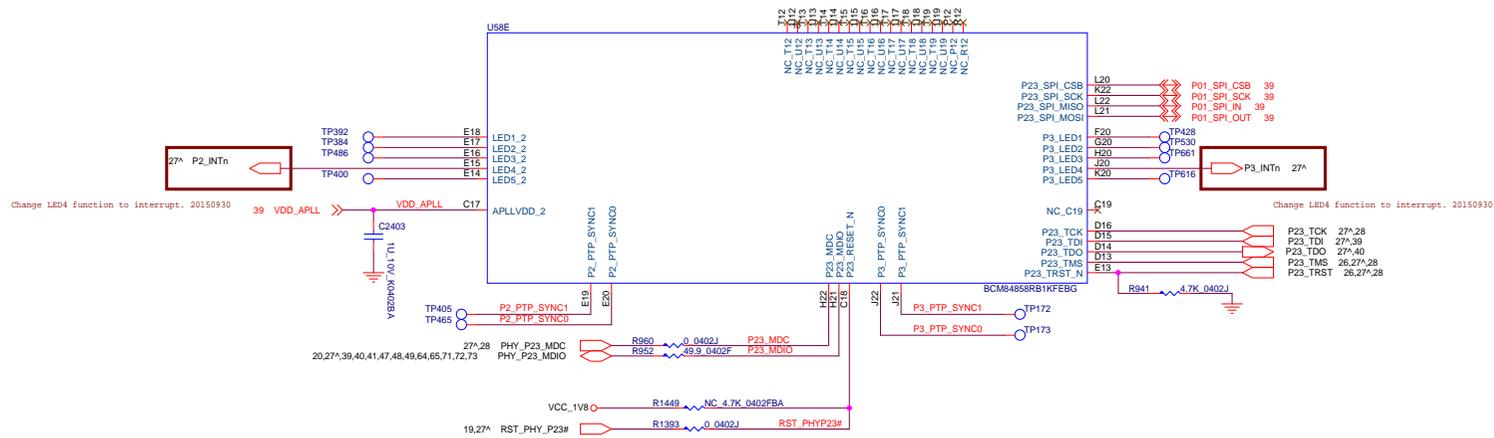
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M20	GND_M20
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M2	GND_M2
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M19	GND_M19
M18	GND_M18
M17	GND_M17
M16	GND_M16
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M8	GND_M8
M7	GND_M7
M6	GND_M6
M5	GND_M5
M4	GND_M4
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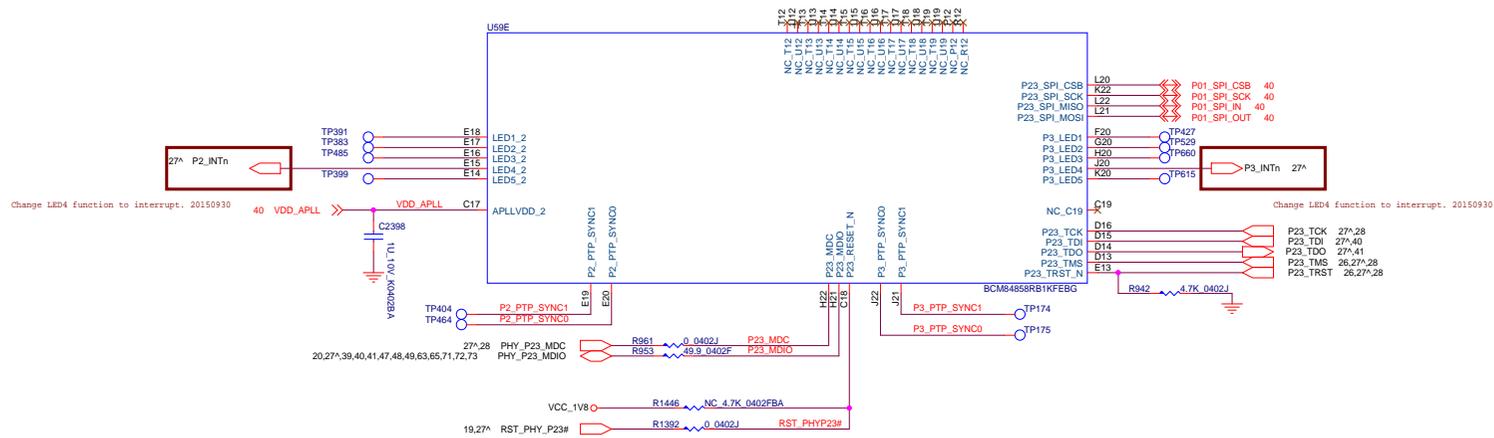
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C	1ADSS-0XXXXX	Rev 1.1
Date:	Tuesday, September 15, 2016	Sheet 81 of 80



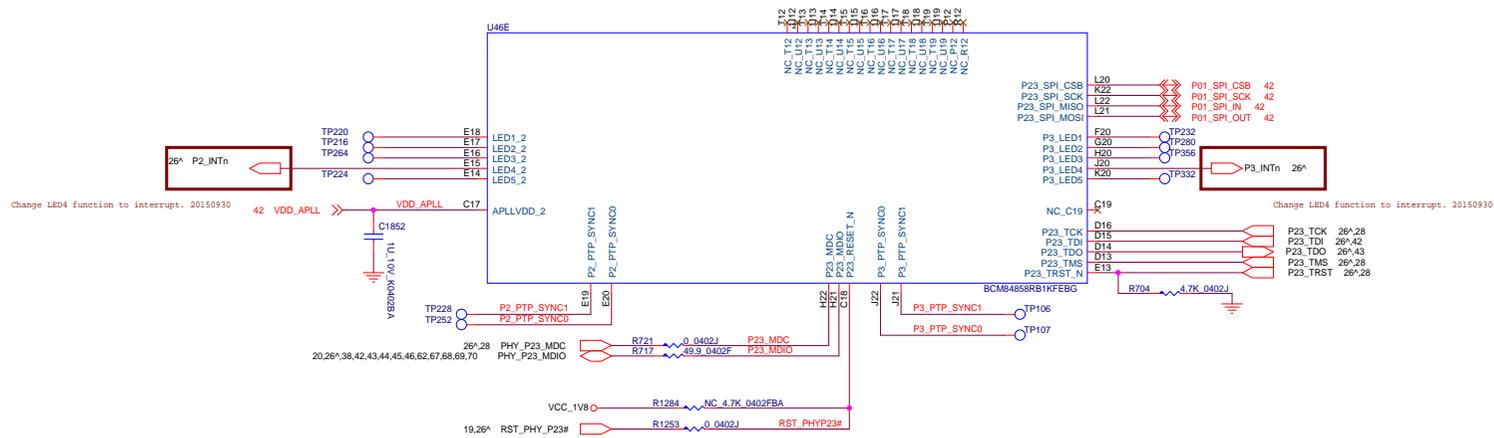


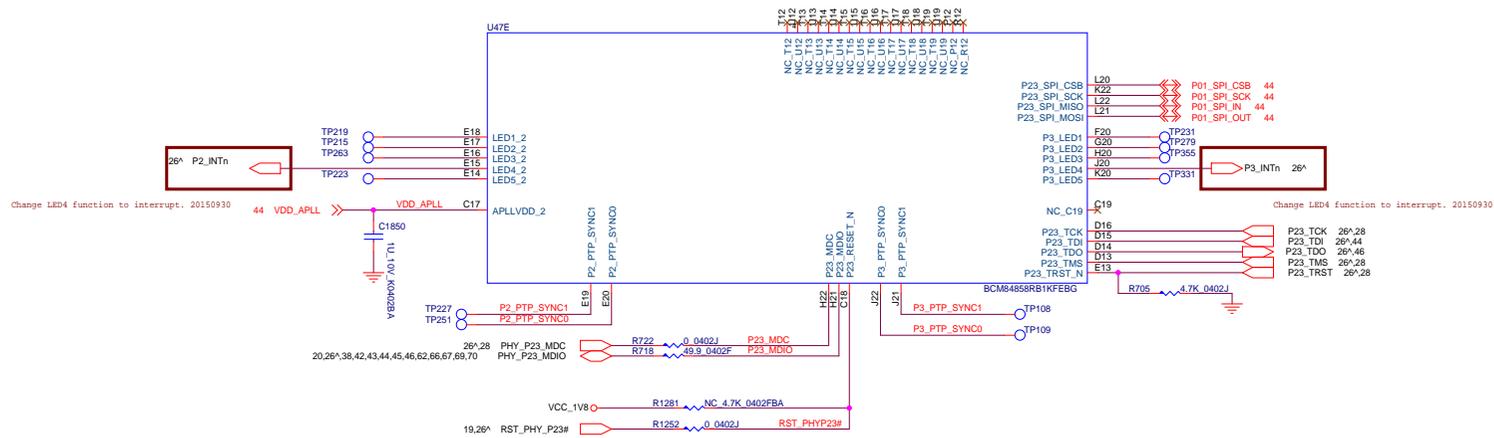


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Date:	Tuesday, September 13, 2016	Sheet 64 of 80

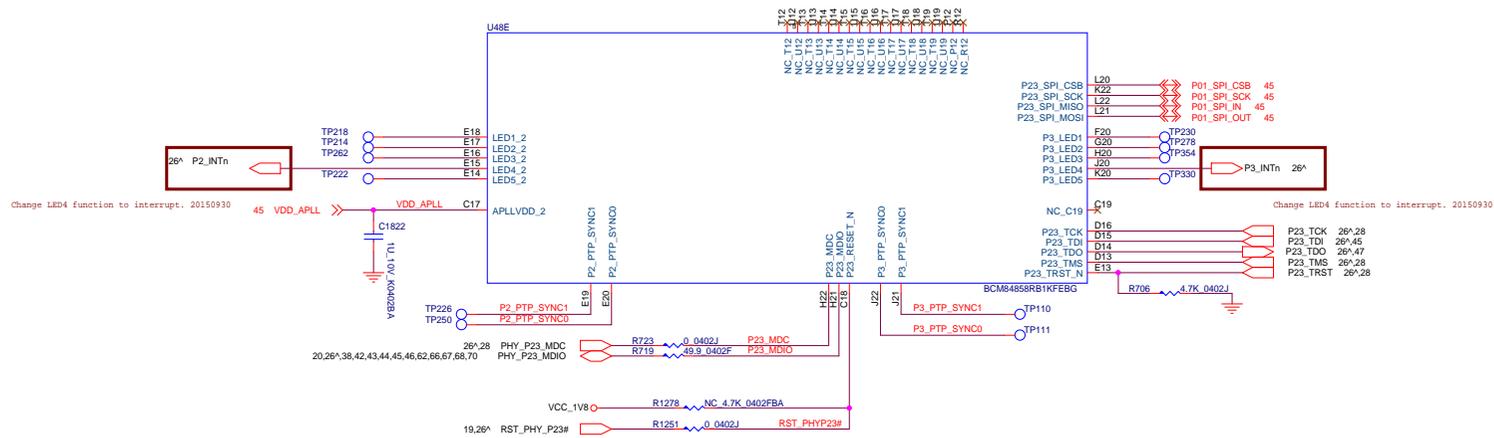


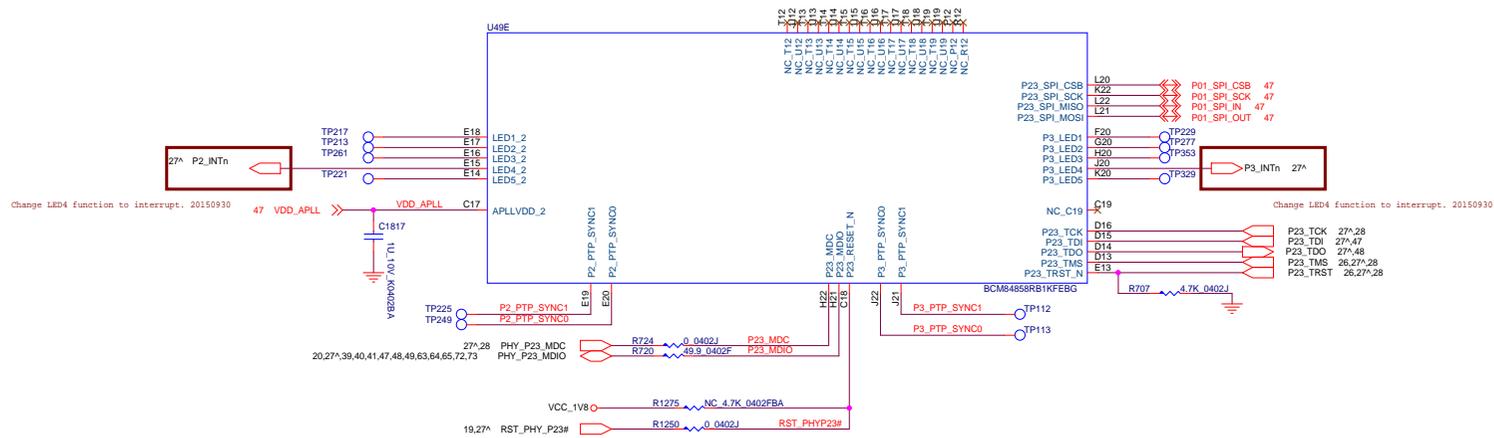


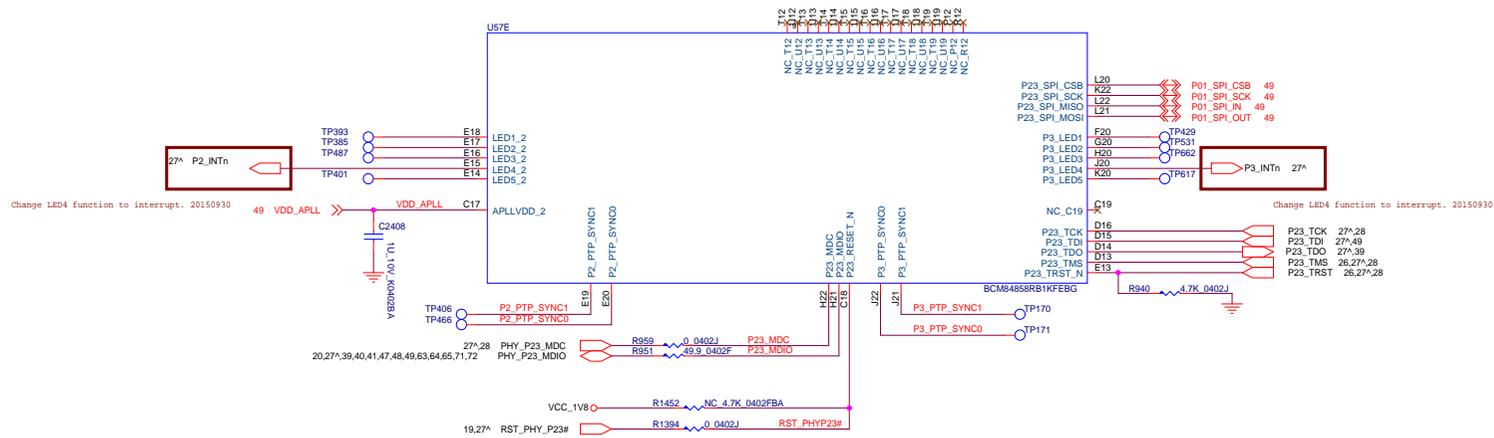
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Date:	Tuesday, September 13, 2016	Sheet	68 of 80



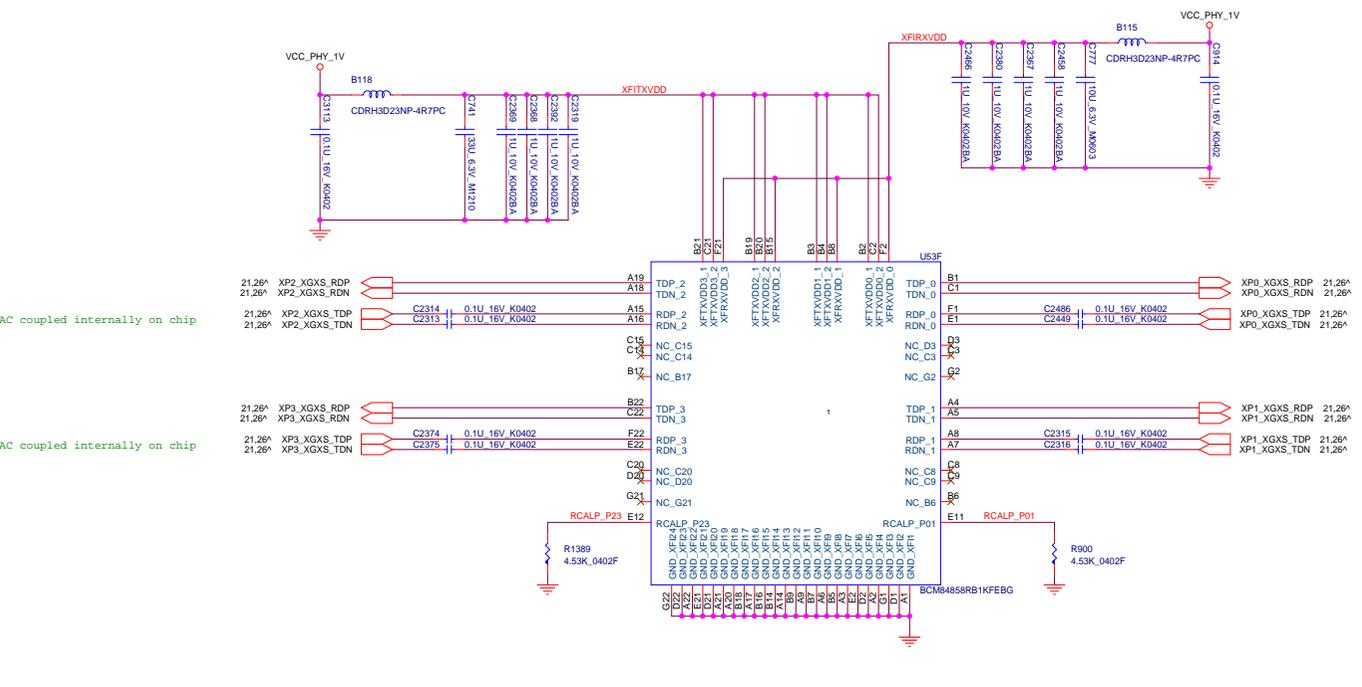
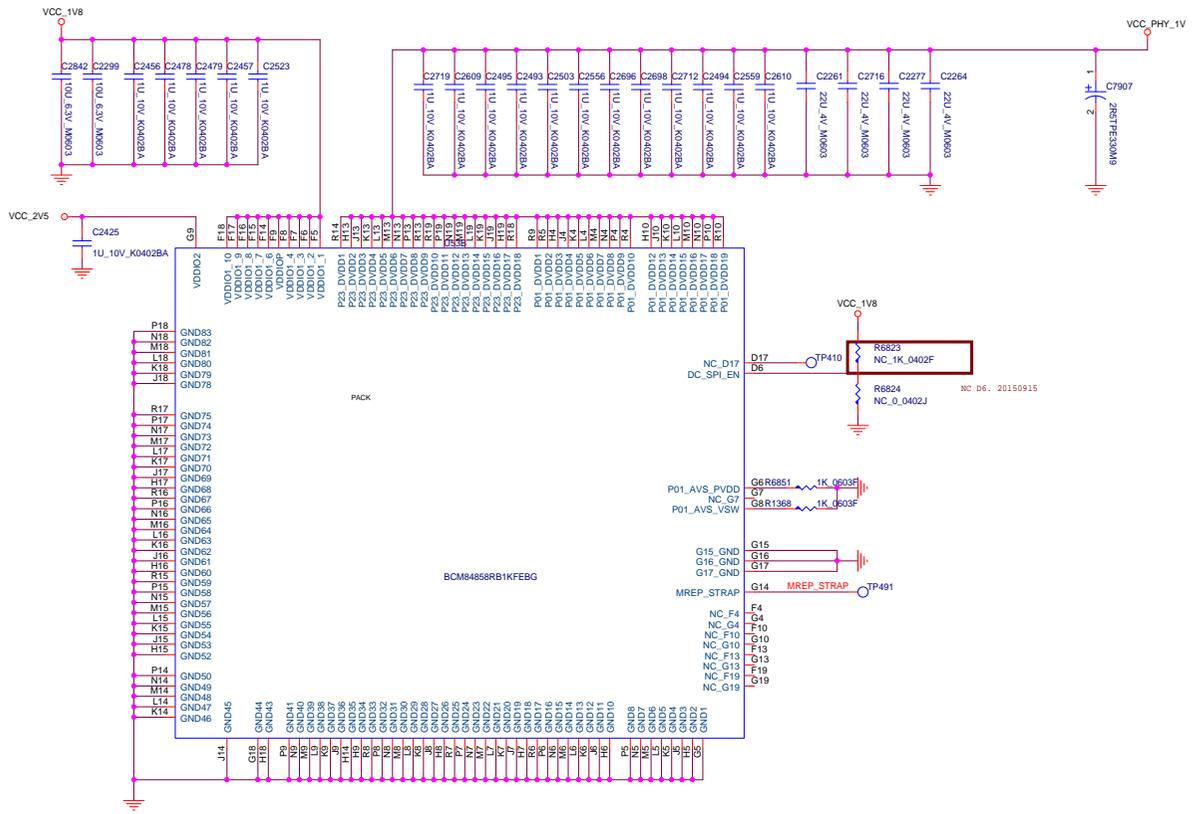




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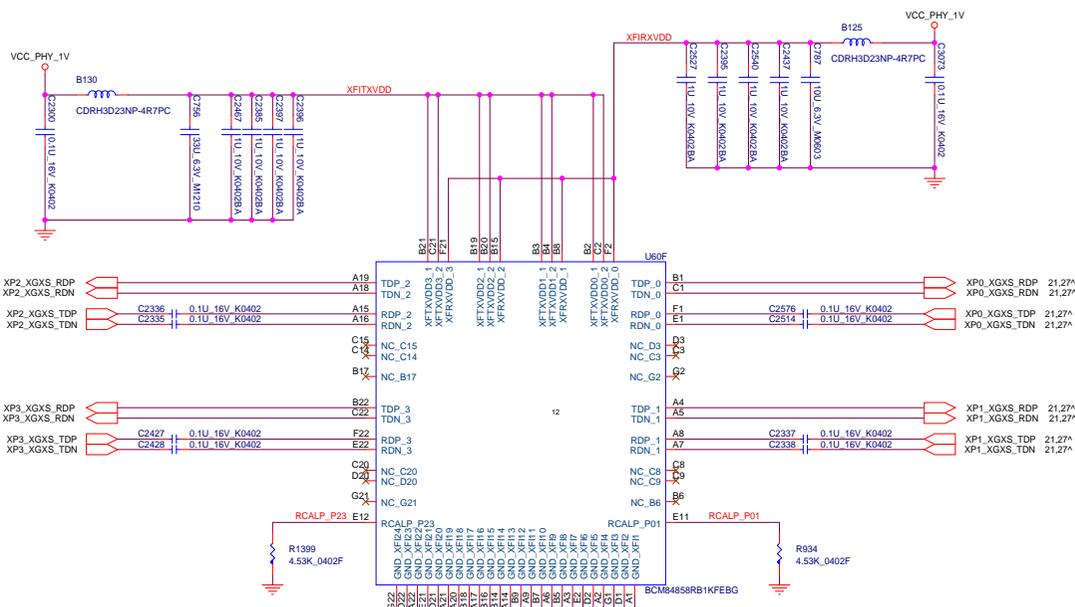
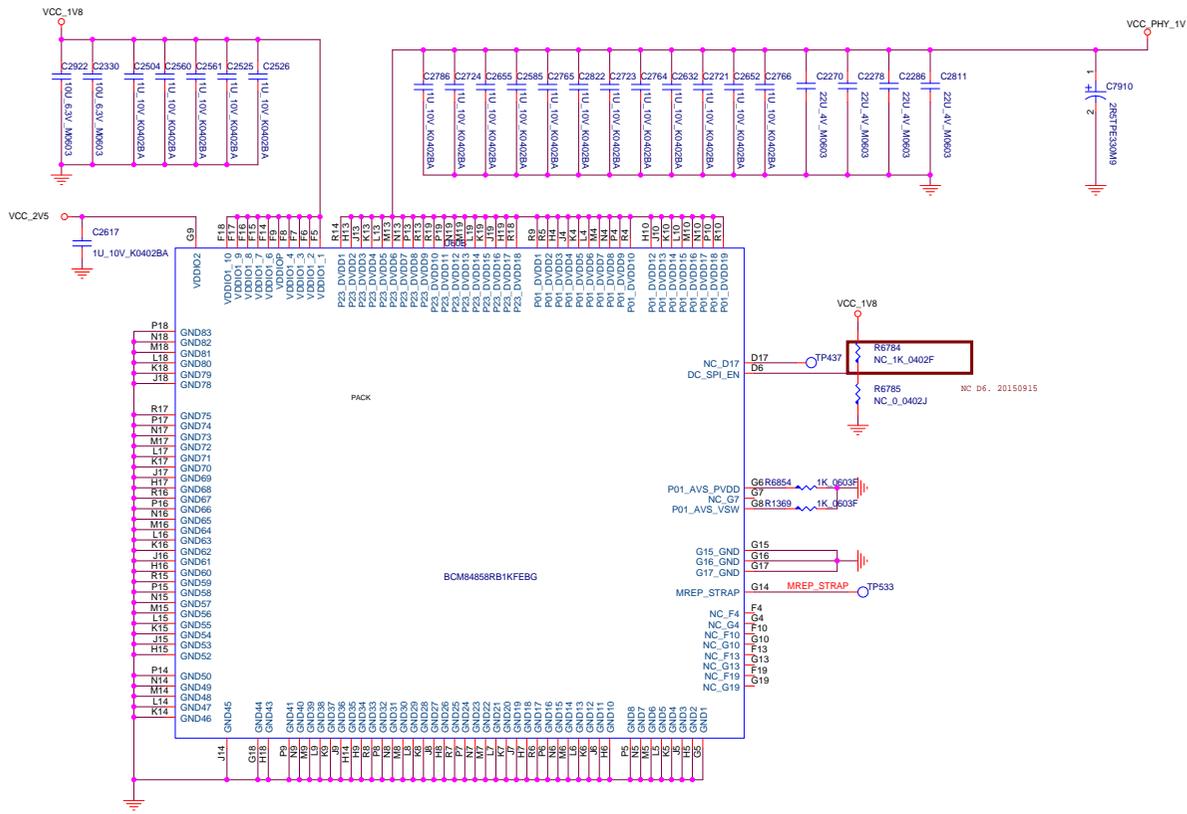
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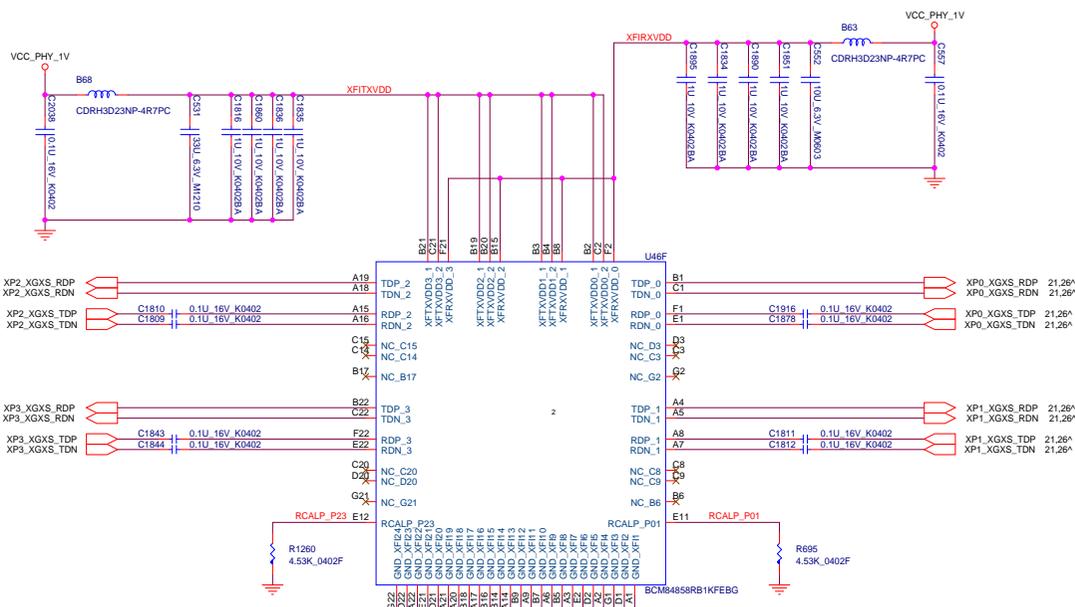
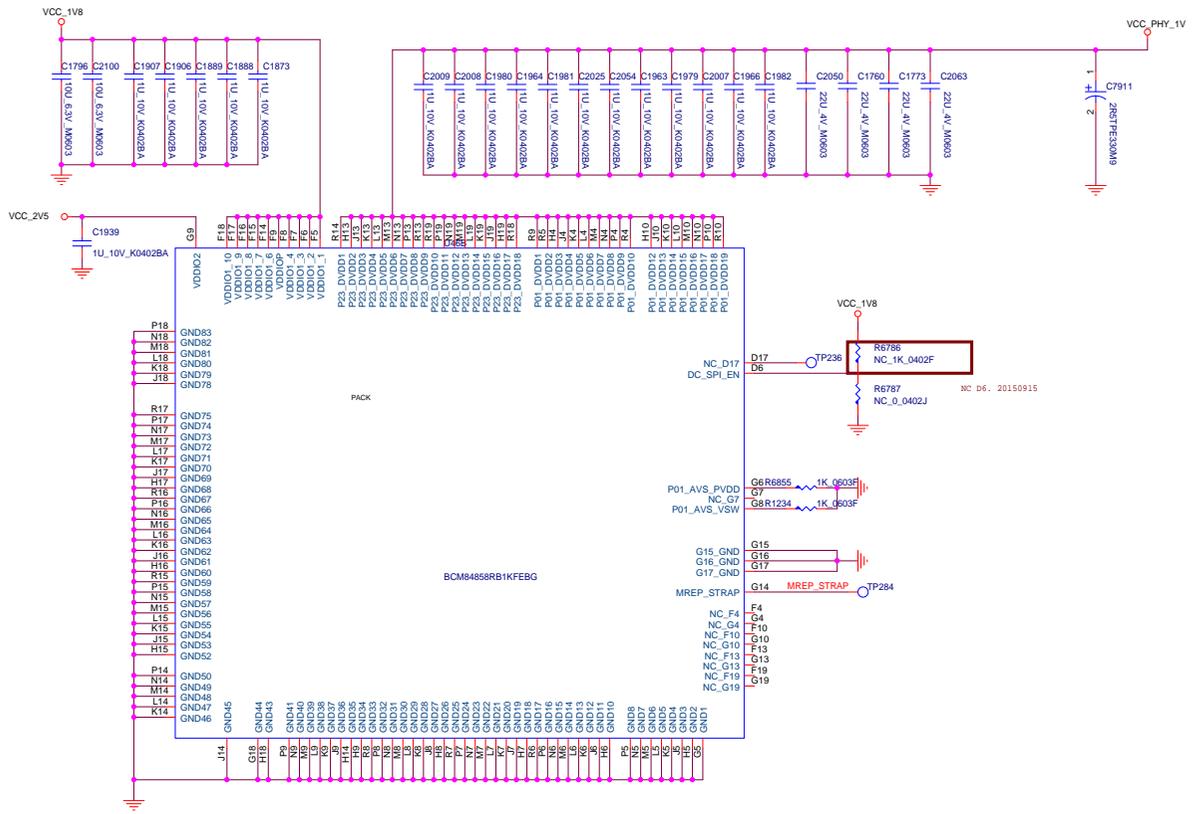


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Date:	Tuesday, September 13, 2016	Sheet 74 of 80

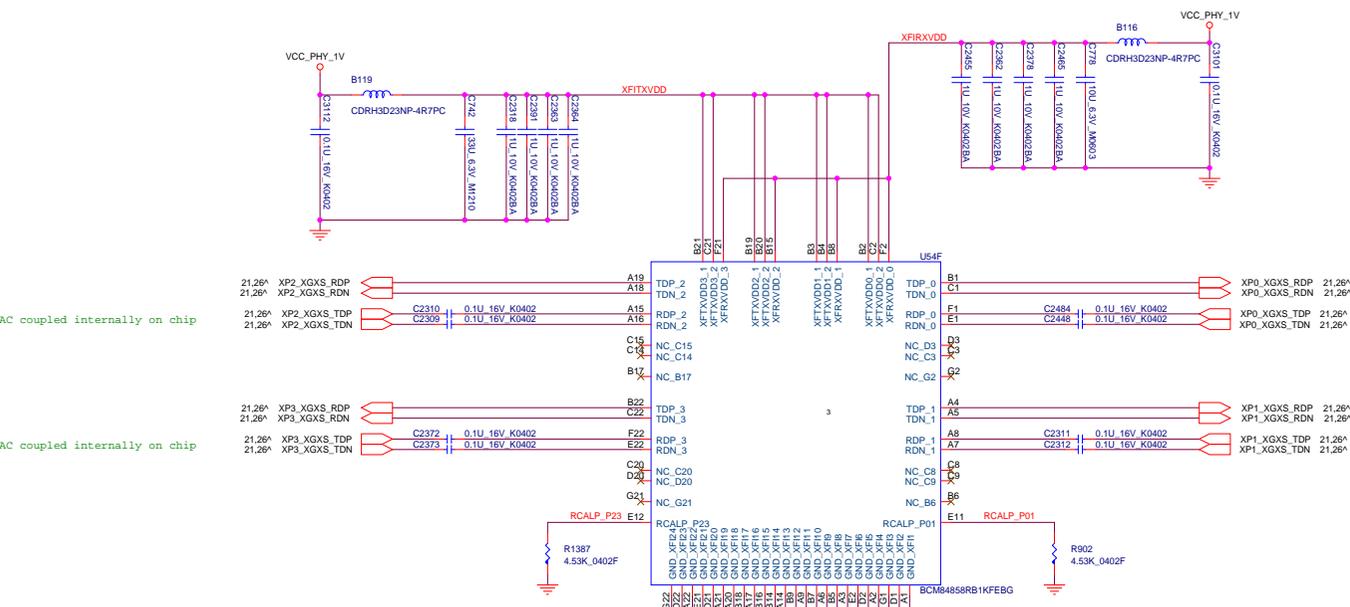
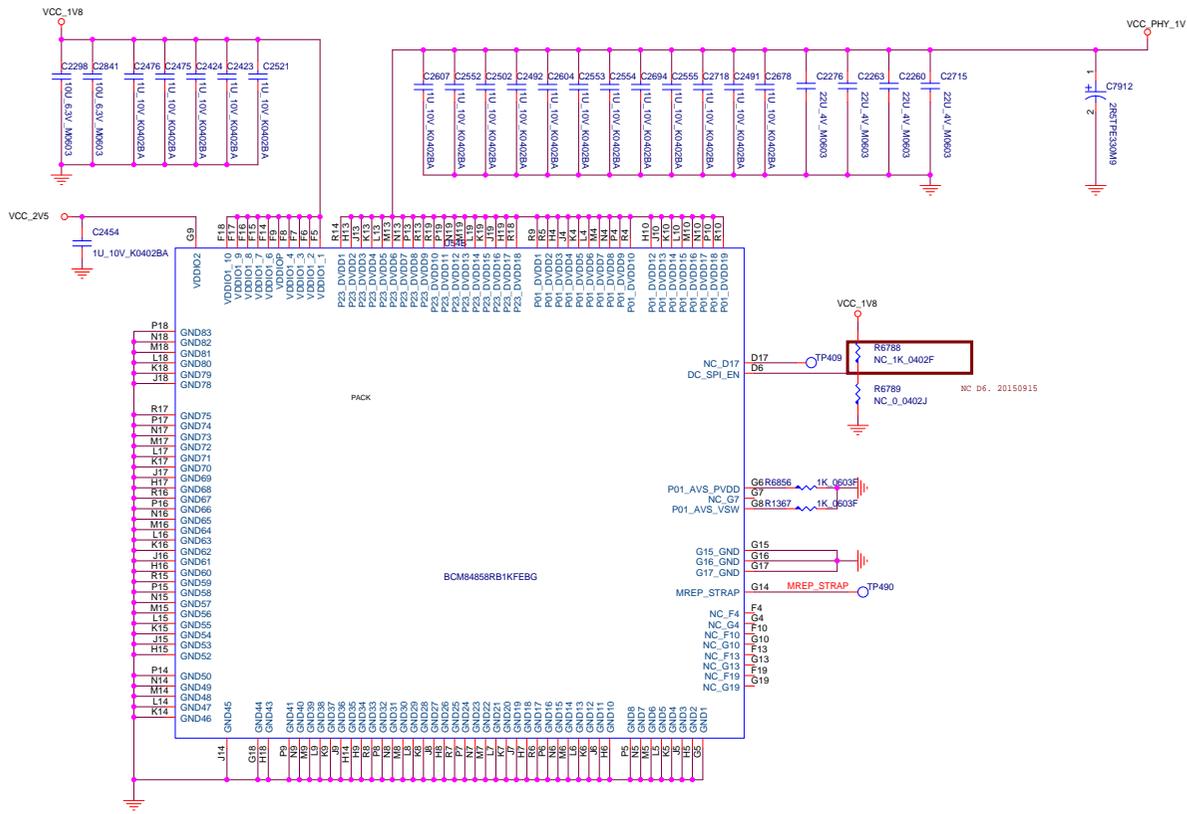


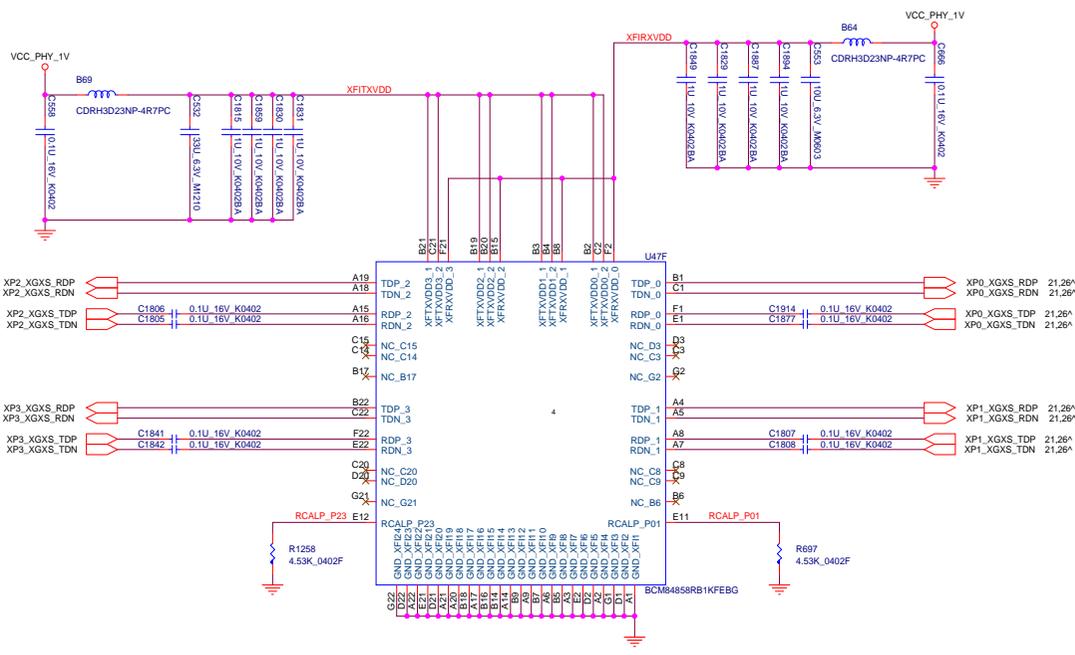
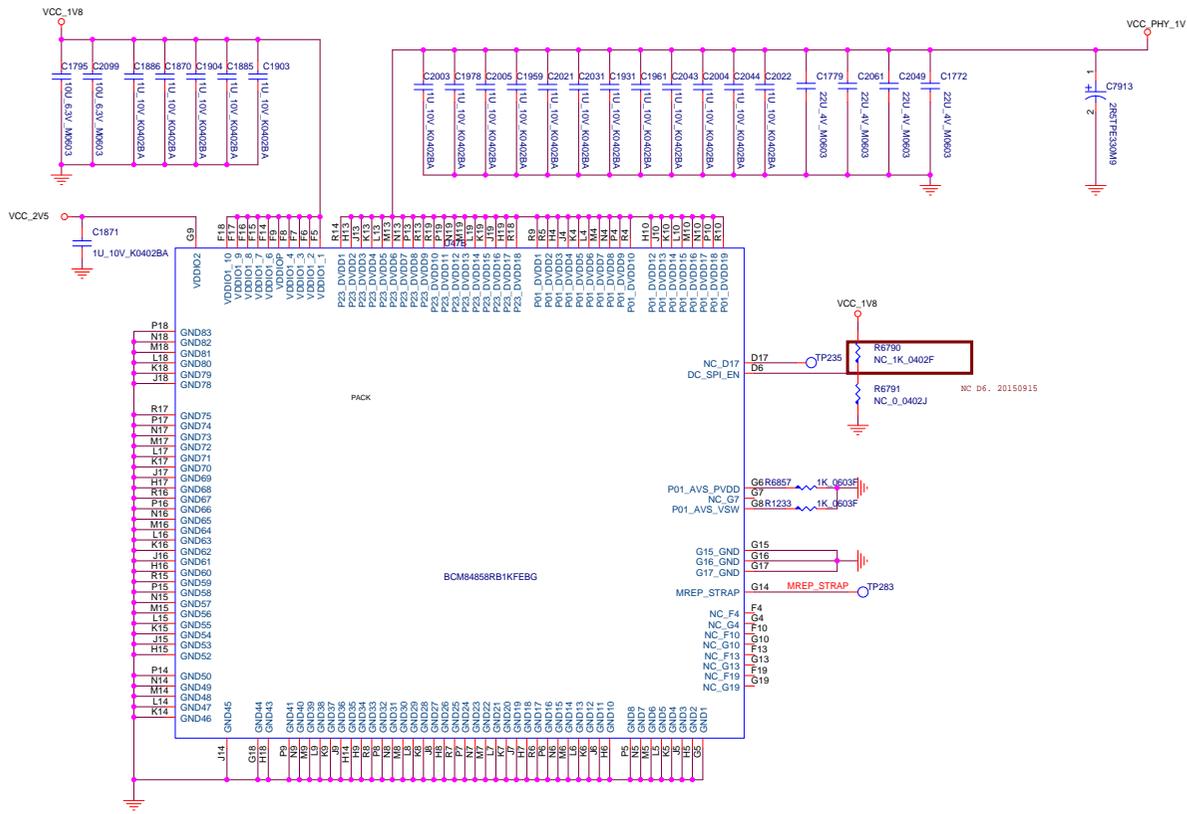


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Date:	Tuesday, September 13, 2016	Sheet 78 of 80





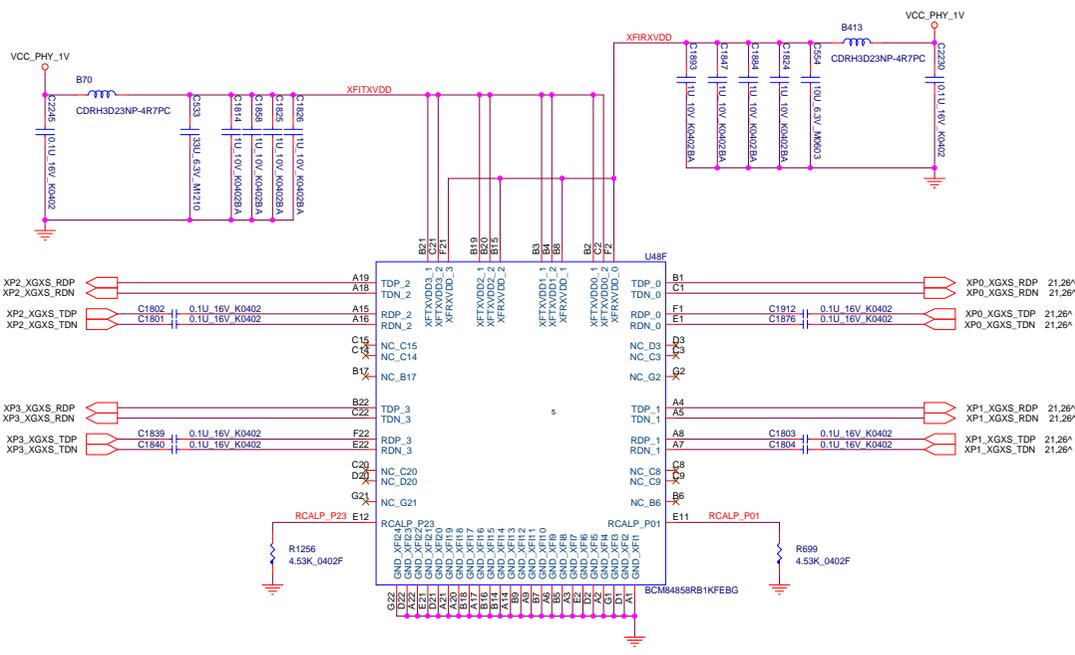
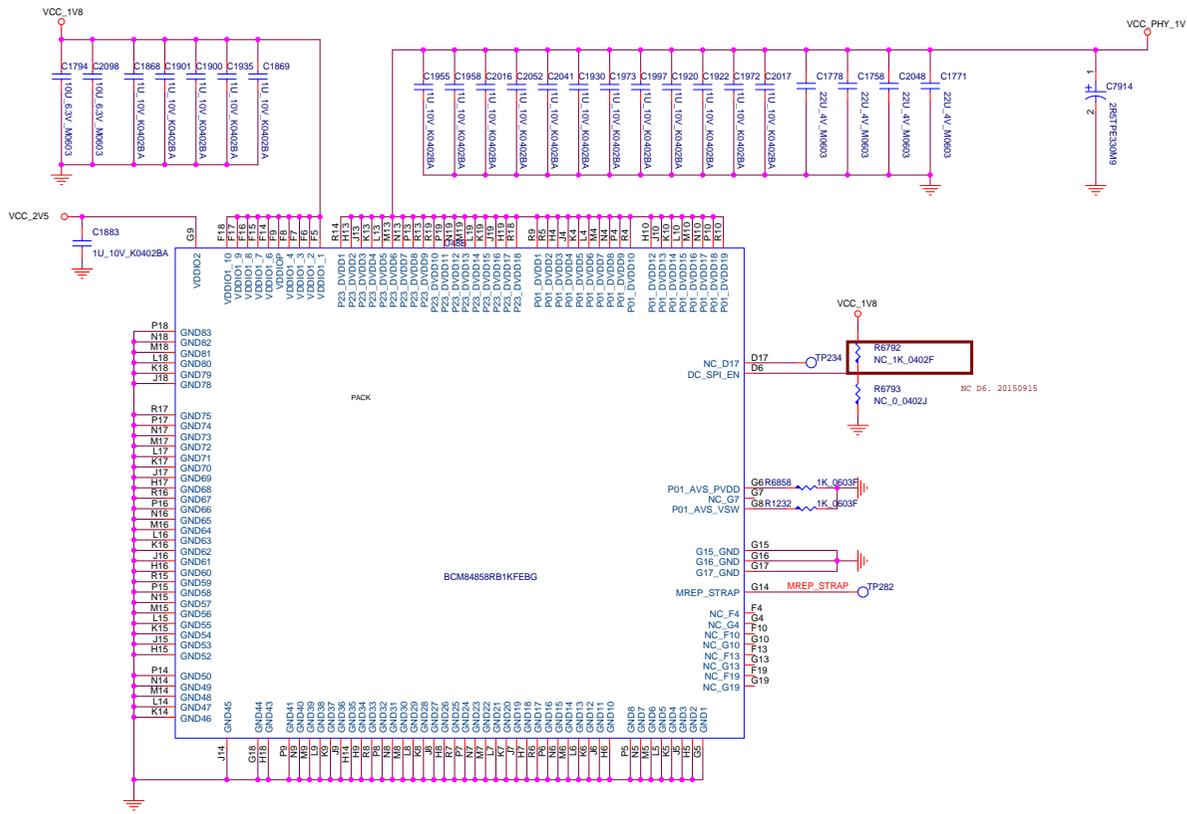
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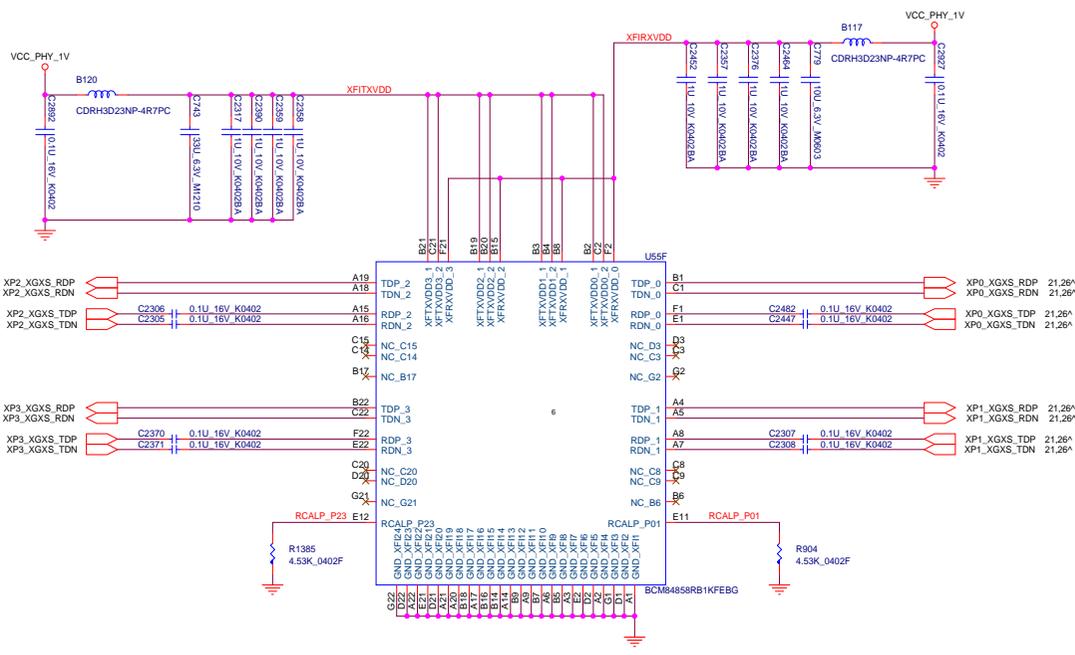
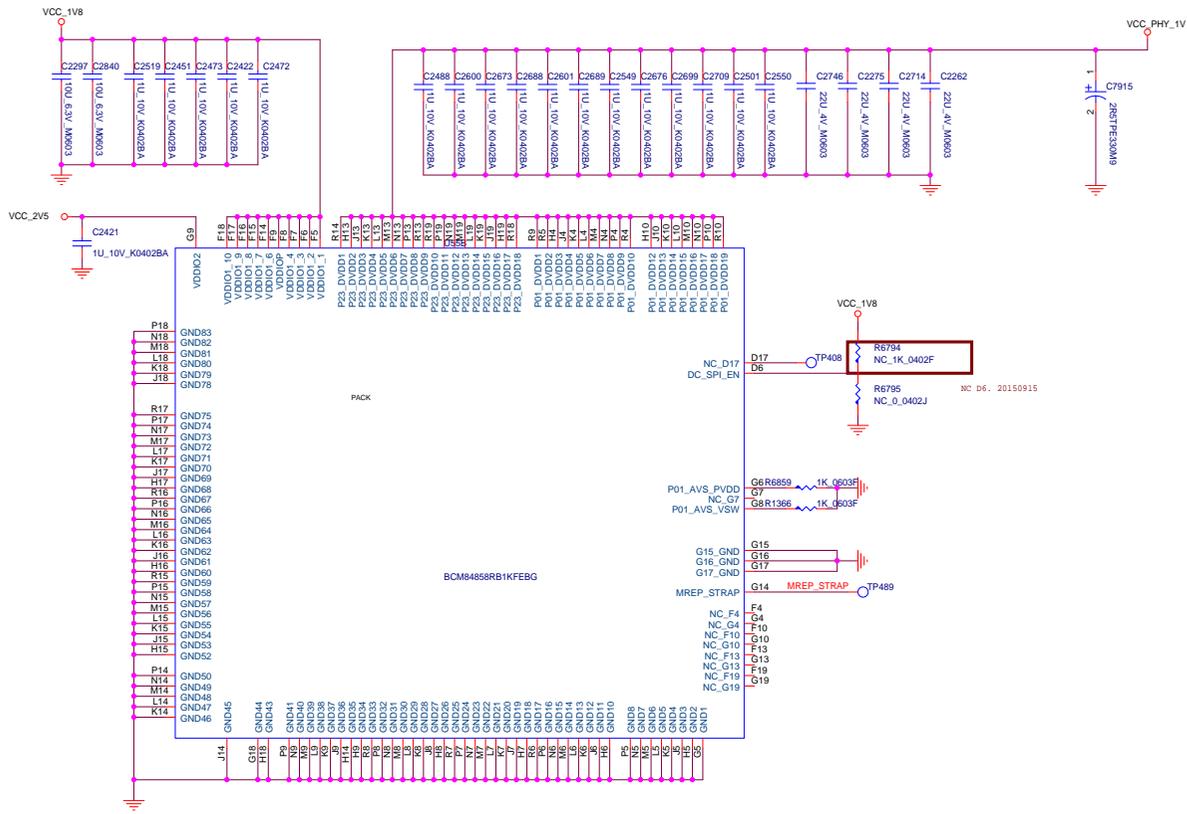
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Date:	Tuesday, September 13, 2016	Sheet 80 of 80

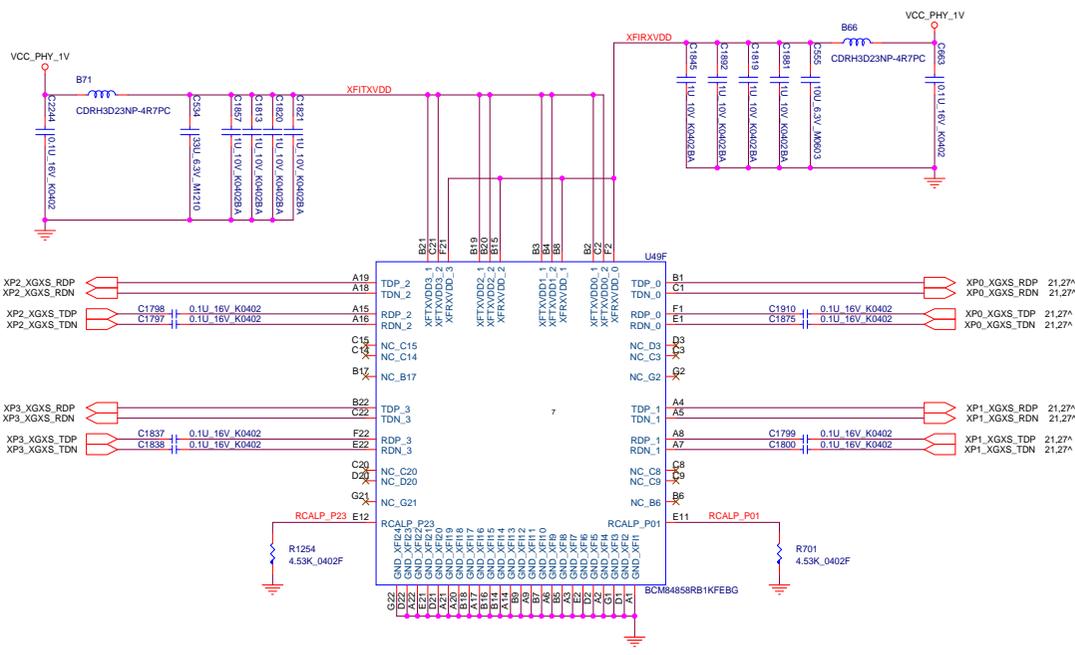
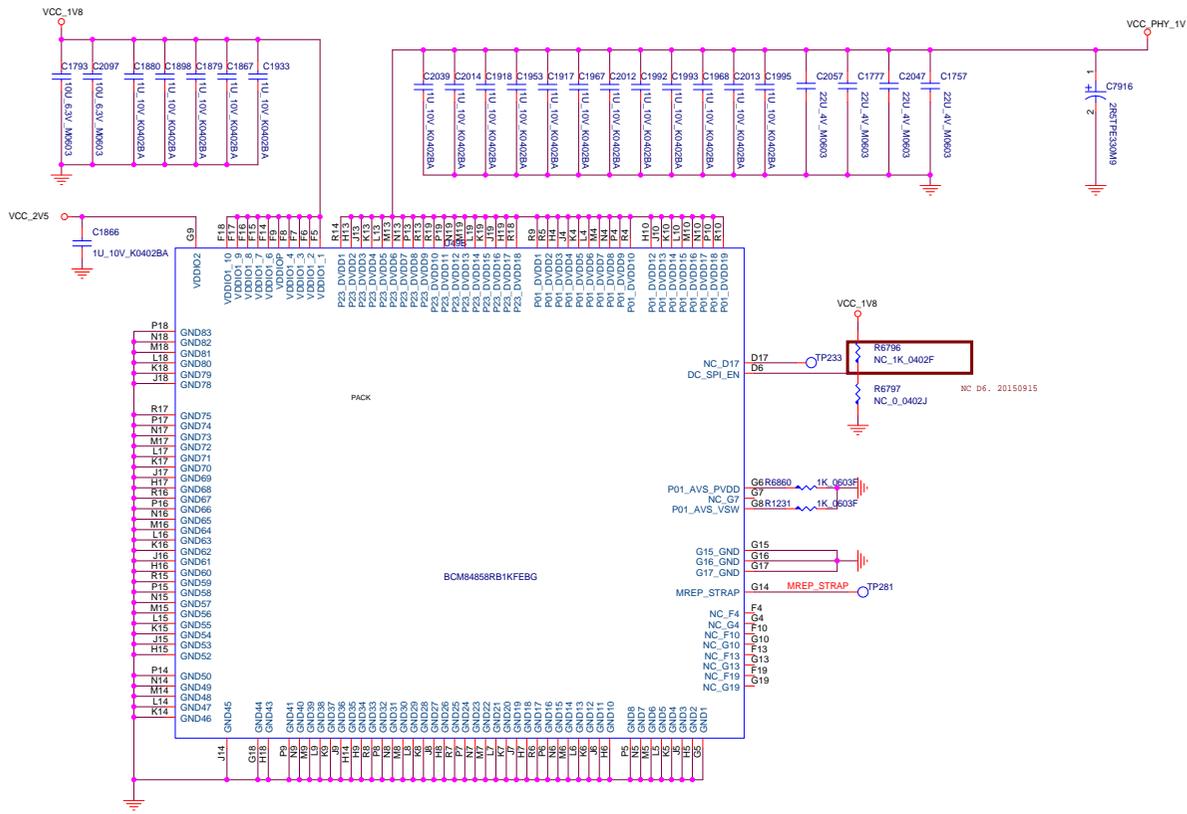




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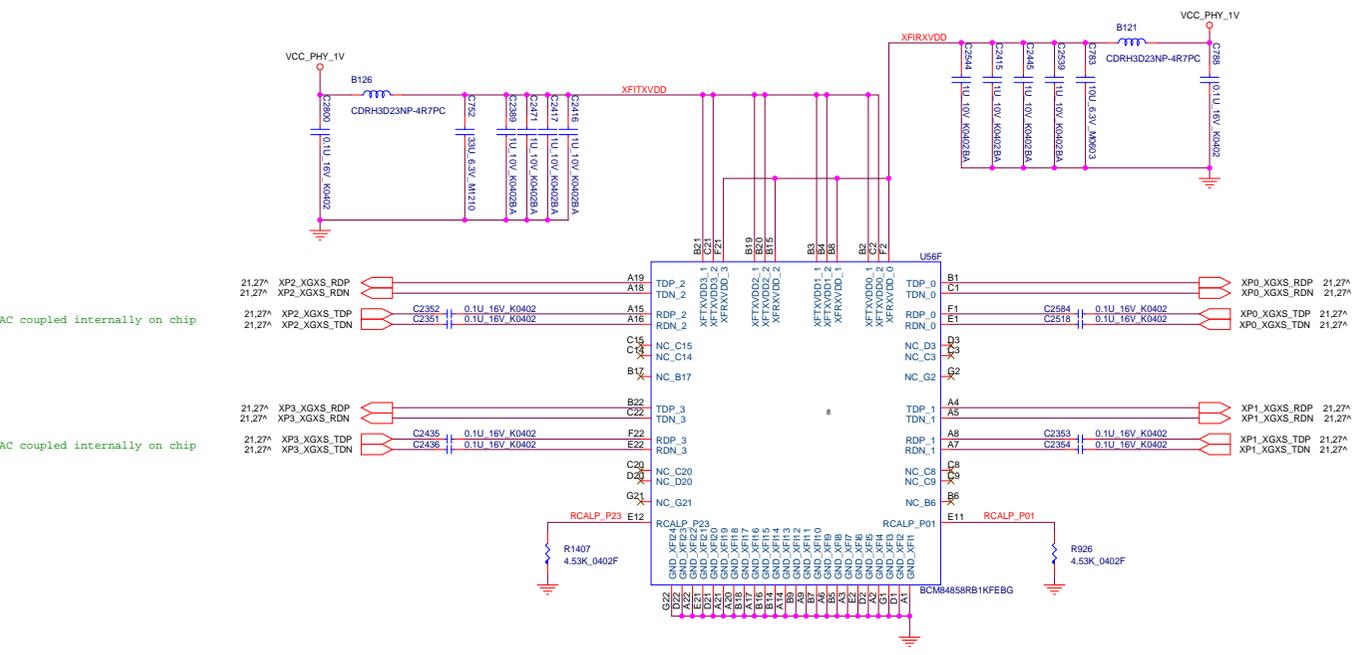
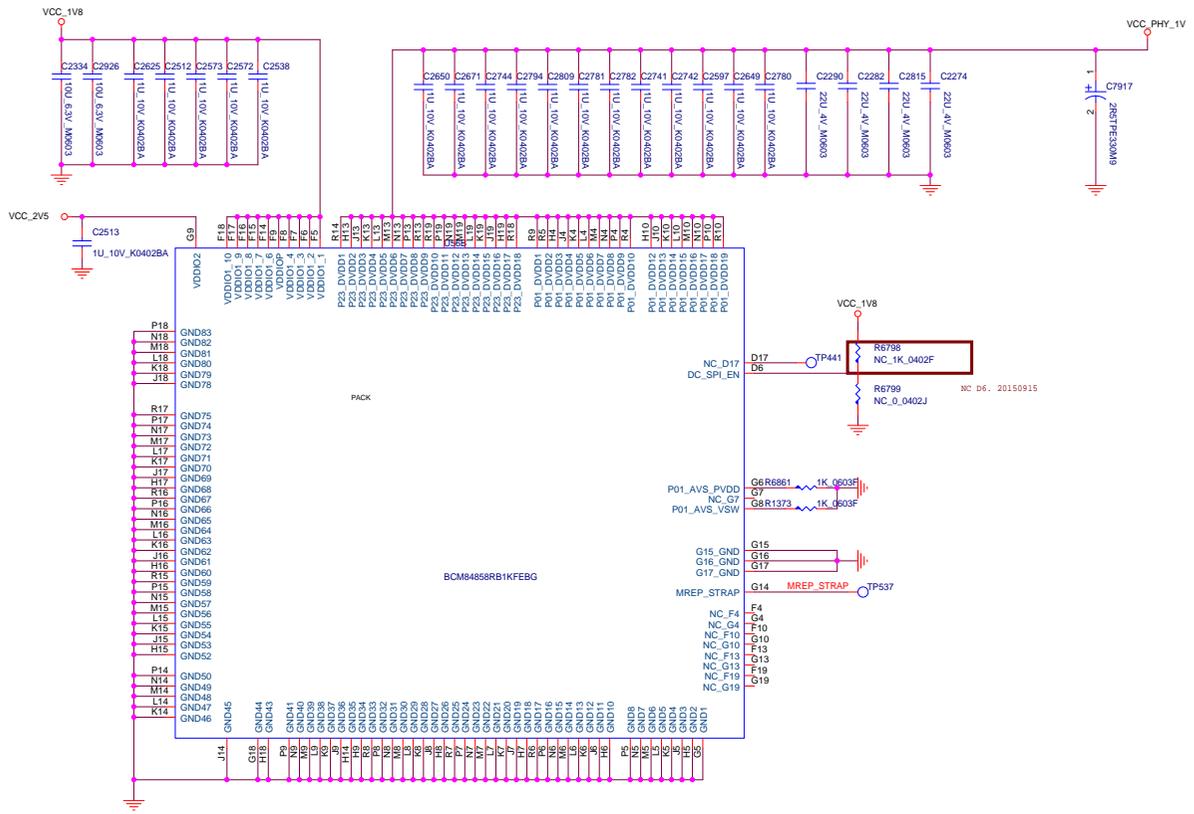
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Size	Document Number	Rev
C	1ADSS-0XXXX	1.1
Date:	Tuesday, September 13, 2016	Sheet 82 of 80



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Date:	Tuesday, September 13, 2016	Sheet	83 of 80

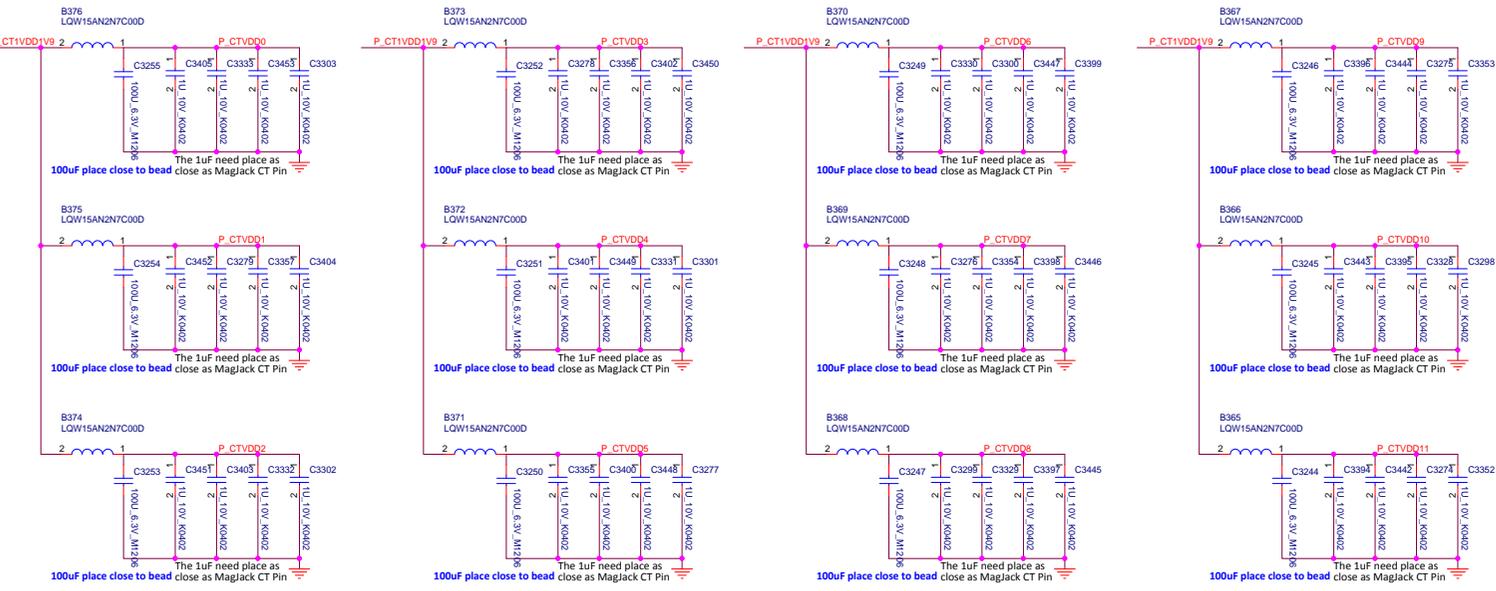
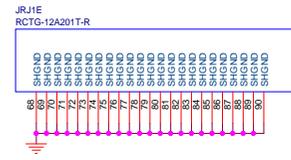
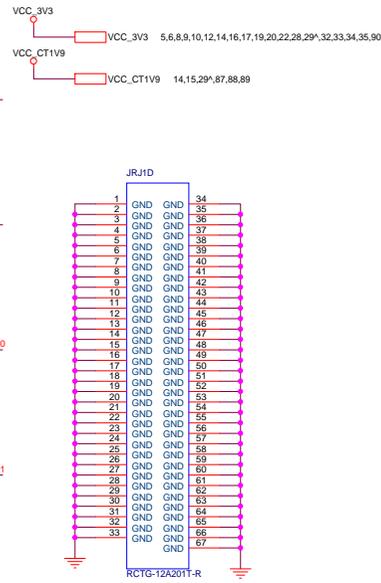
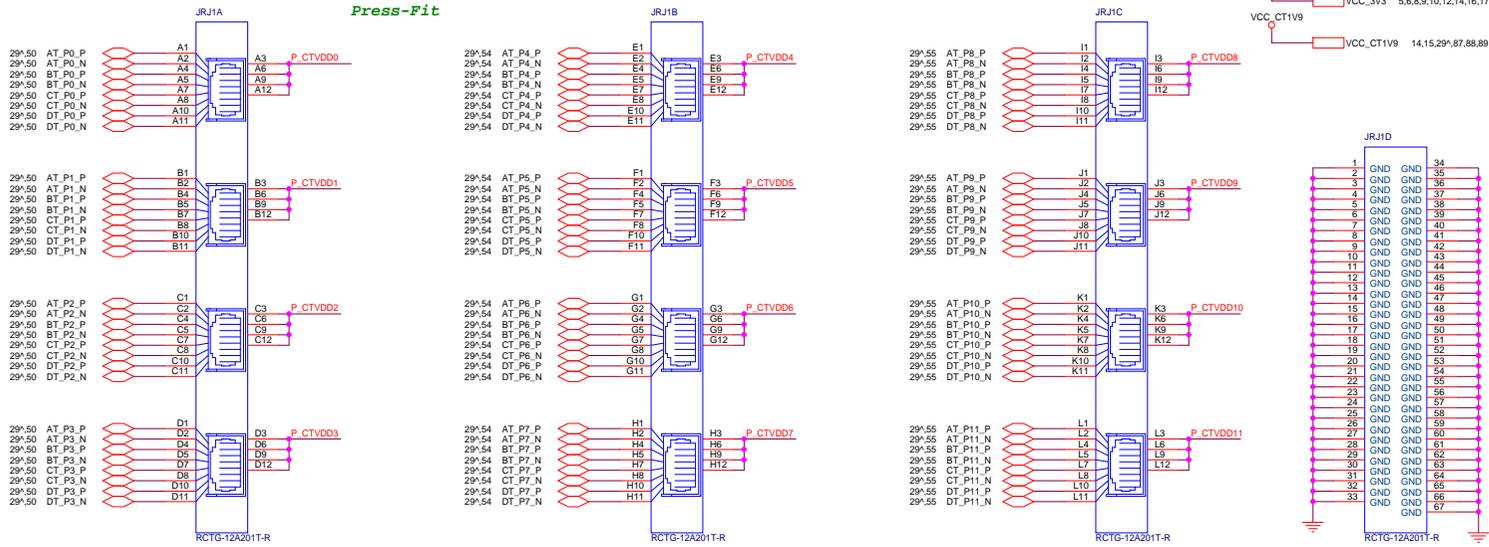


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Size	Document Number	Rev
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Date:	Tuesday, September 13, 2016	Sheet 84 of 80

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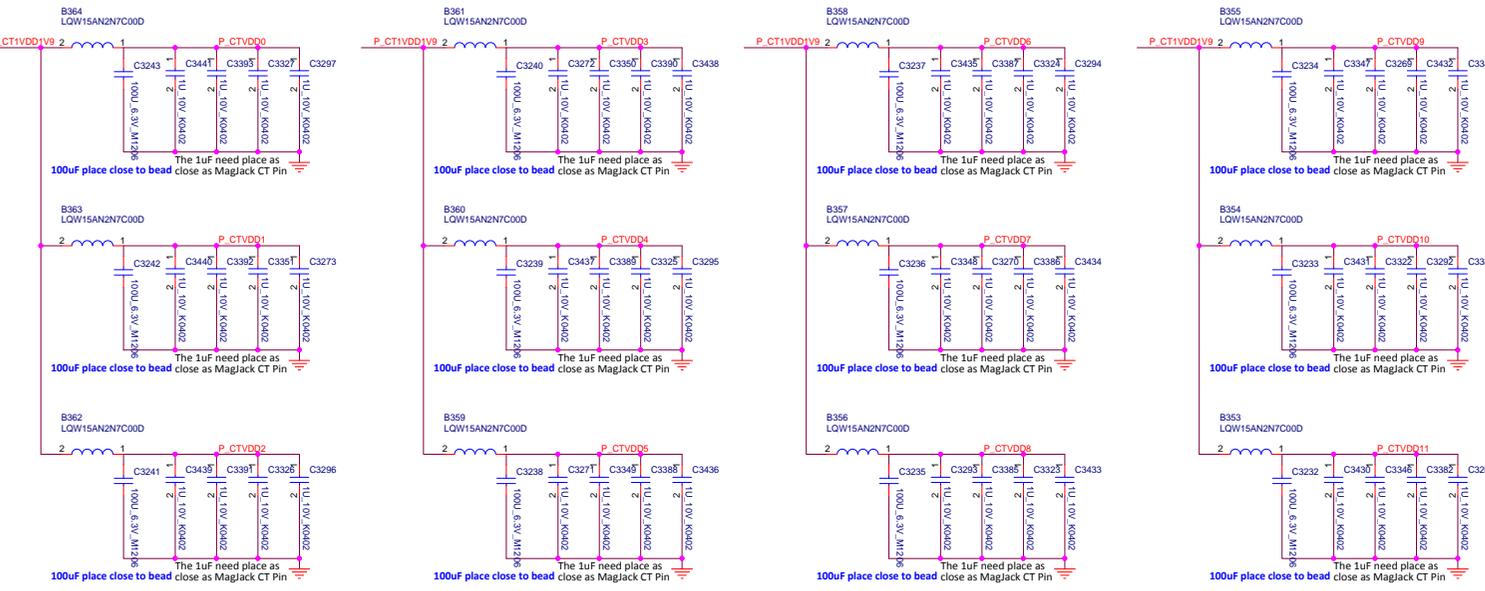
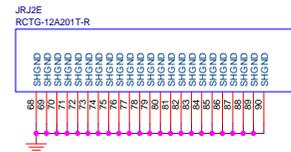
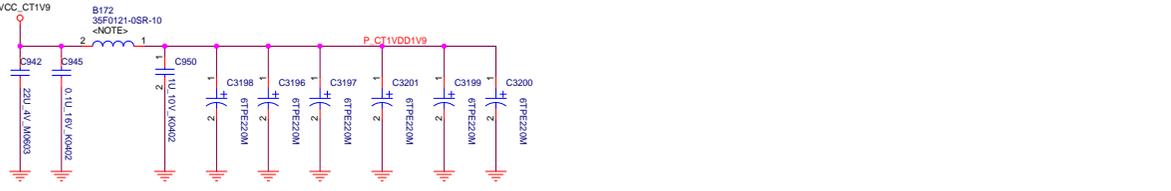
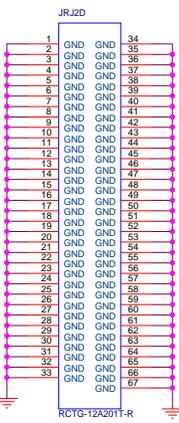
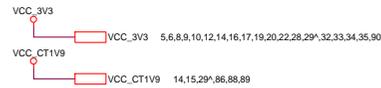
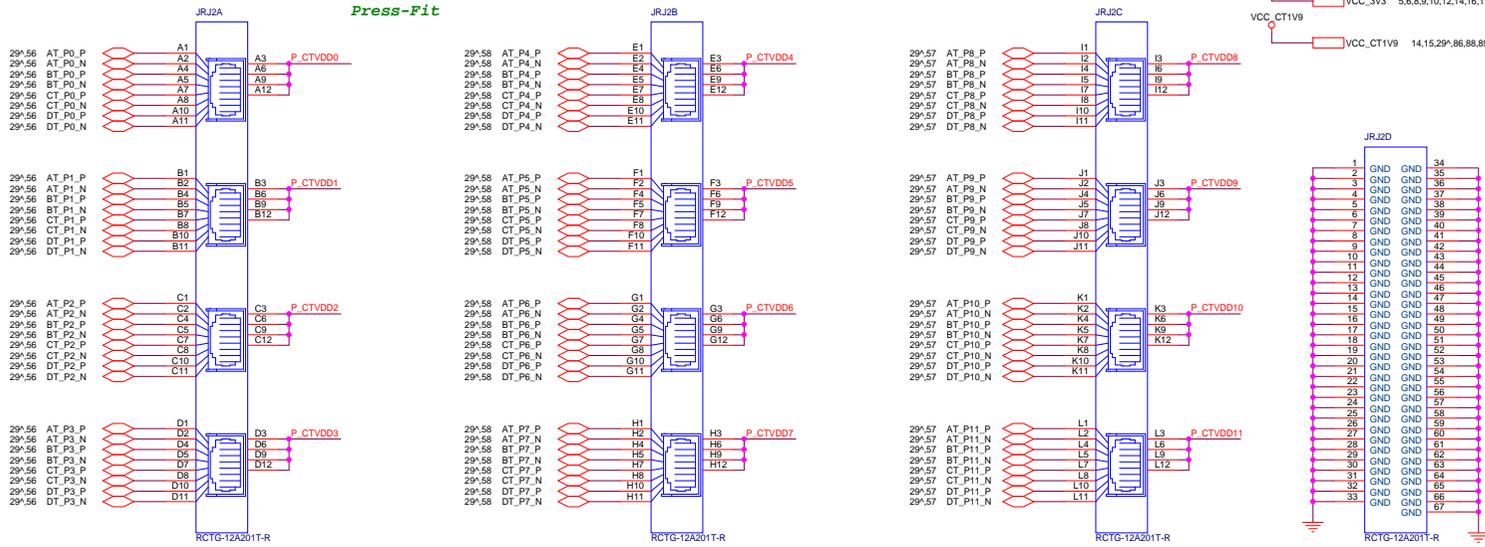


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Date:	Tuesday, September 13, 2016	Sheet 86 of 80

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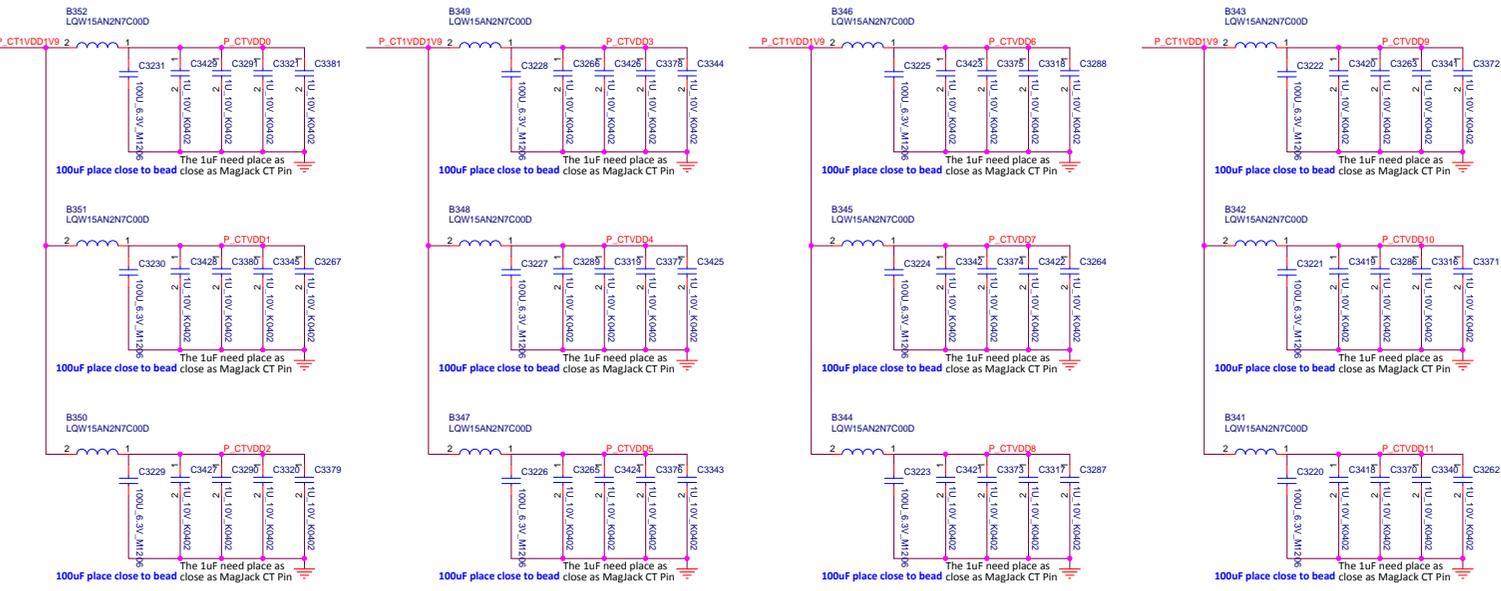
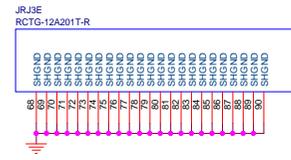
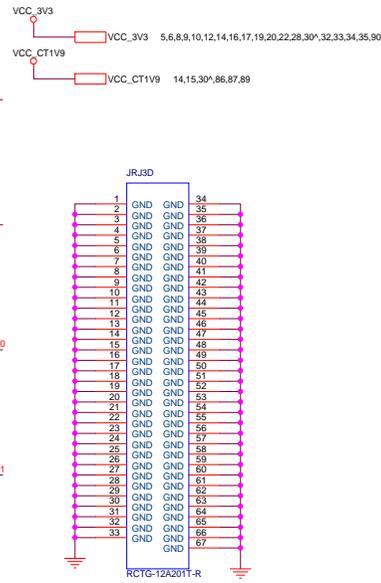
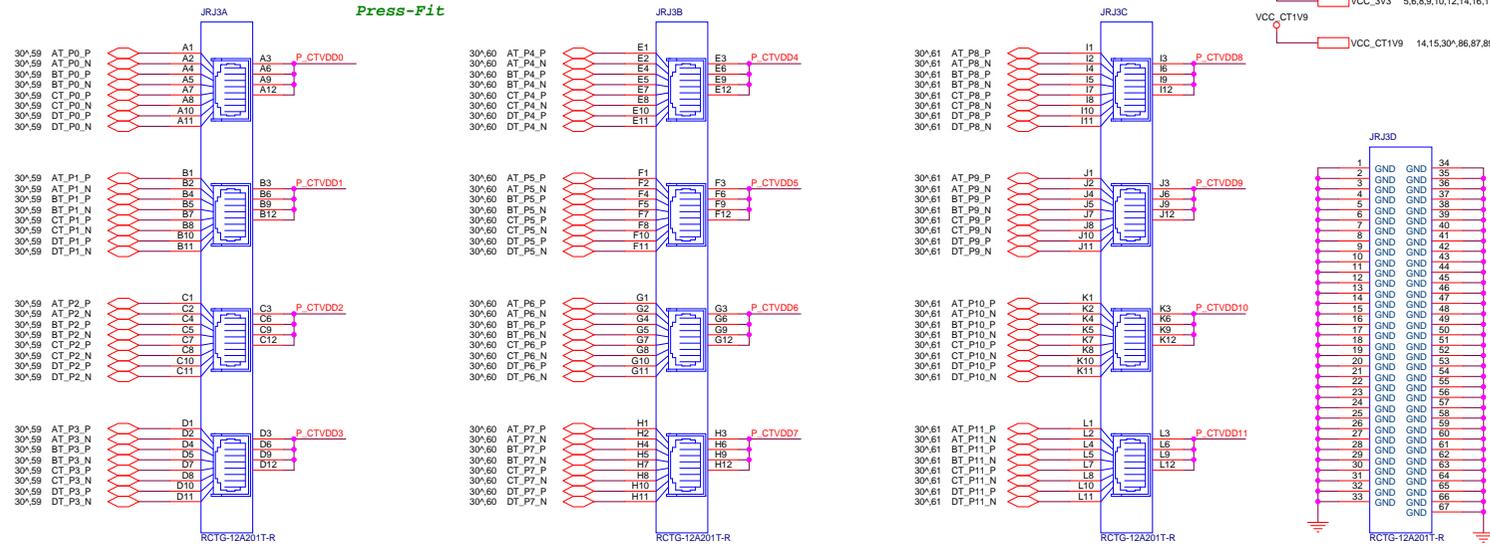


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Date:	Tuesday, September 13, 2016	Sheet 87 of 90

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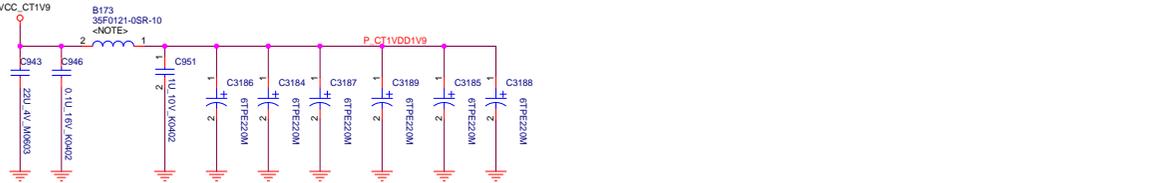
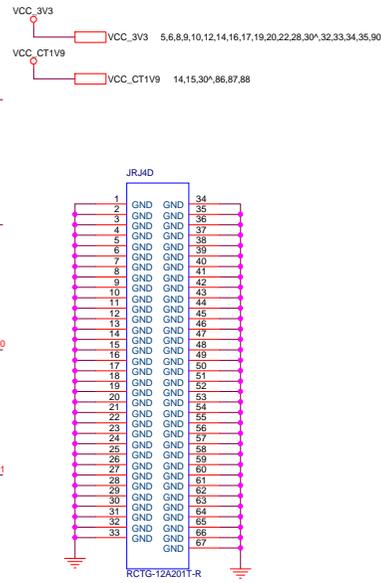
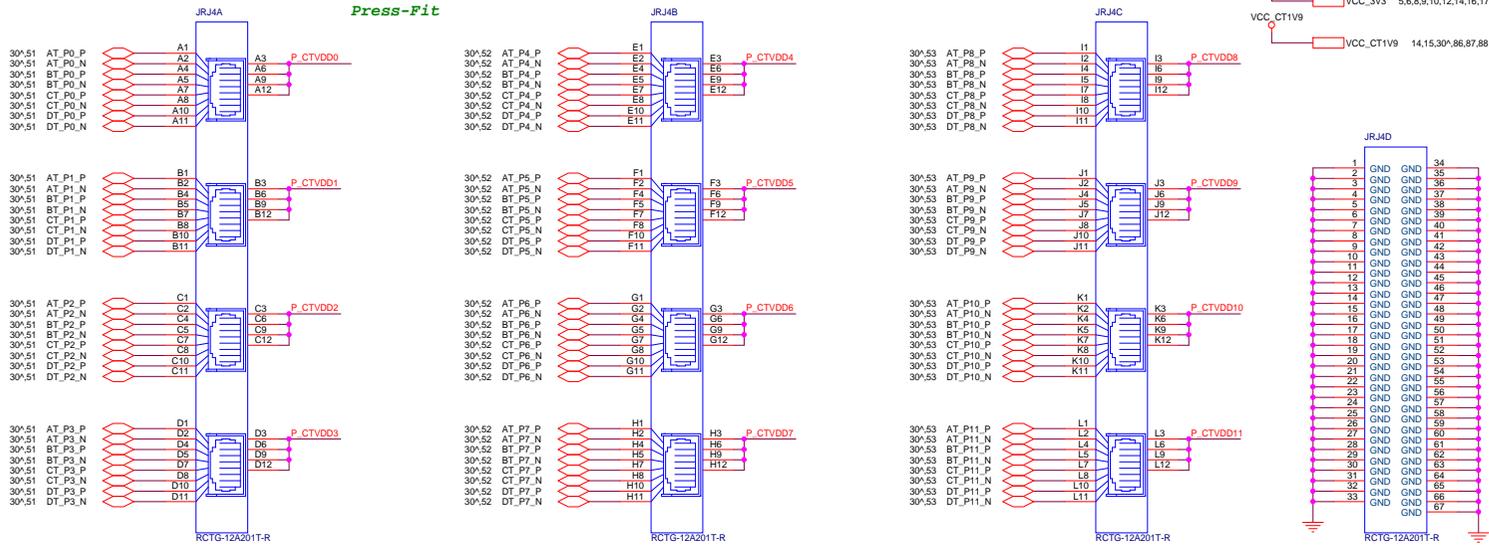


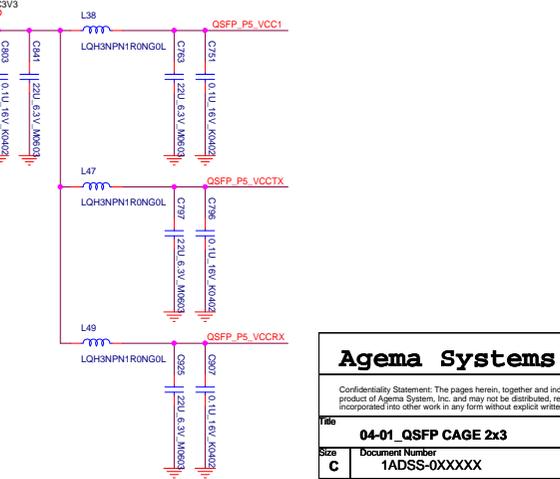
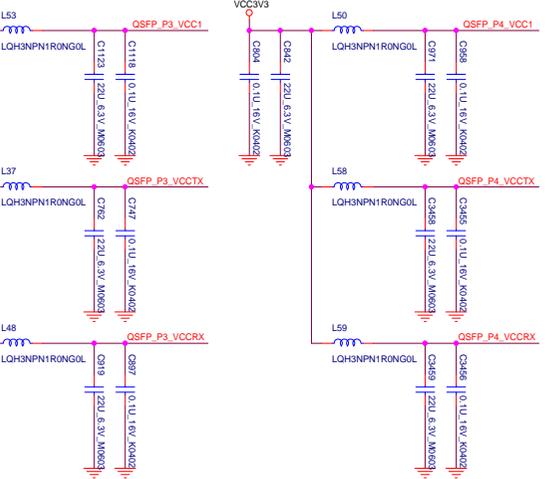
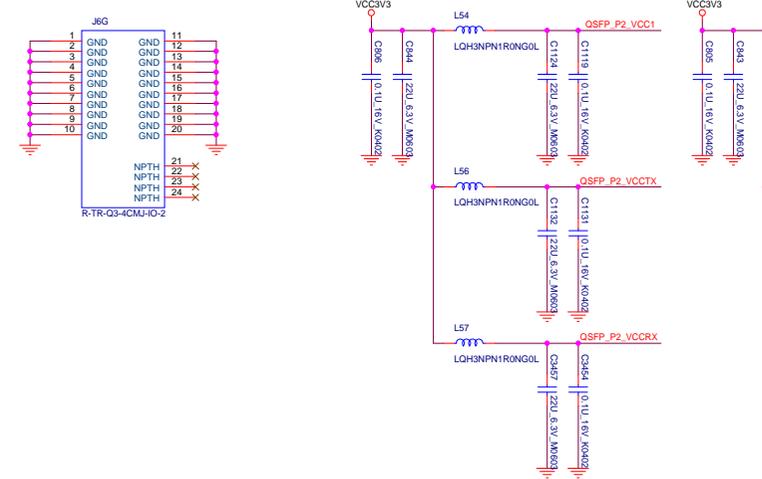
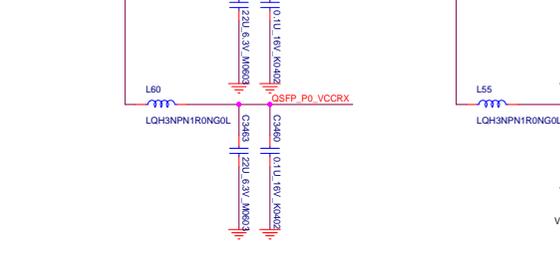
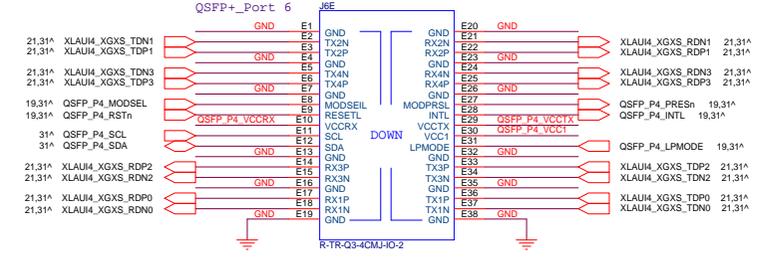
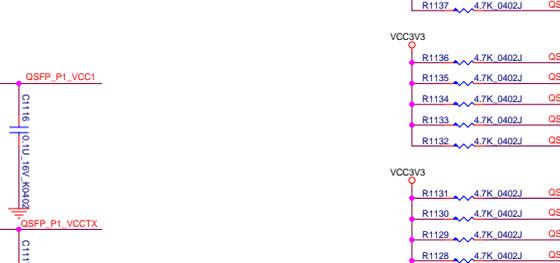
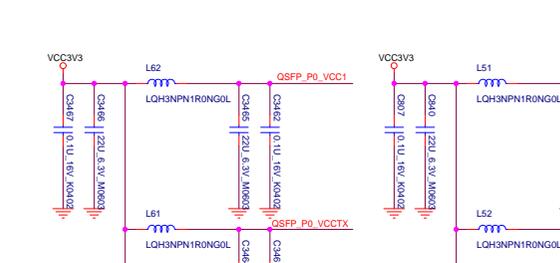
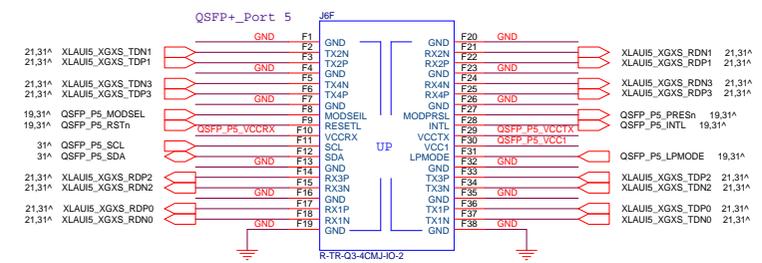
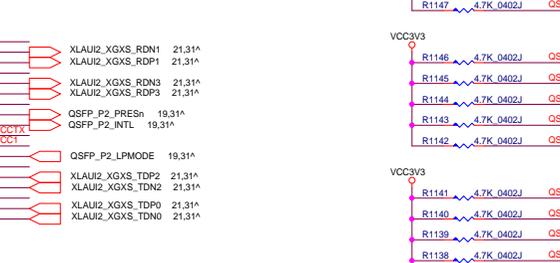
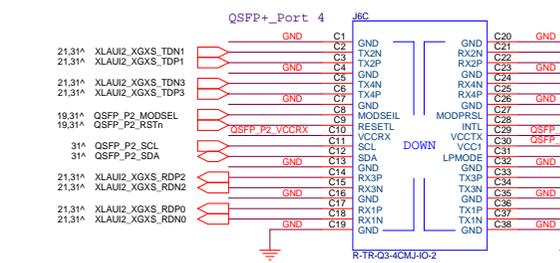
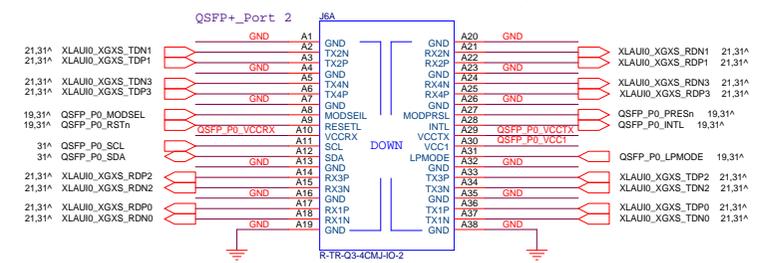
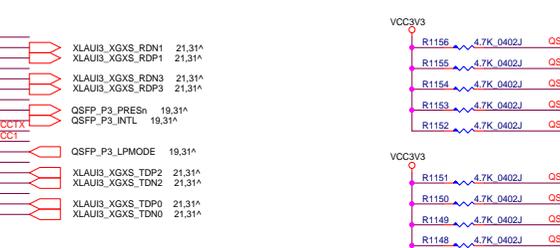
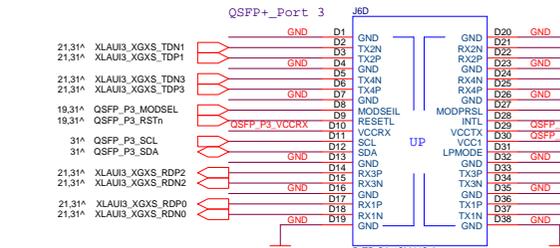
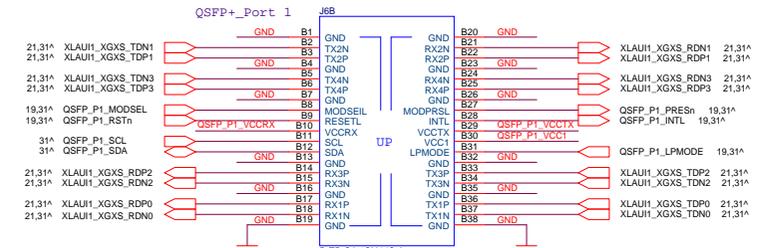
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Size	Document Number	Rev
C	1ADSS-0XXXX	1.1
Date:	Tuesday, September 13, 2016	Sheet 88 of 90

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Date:	Tuesday, September 13, 2016	Sheet 80 of 80