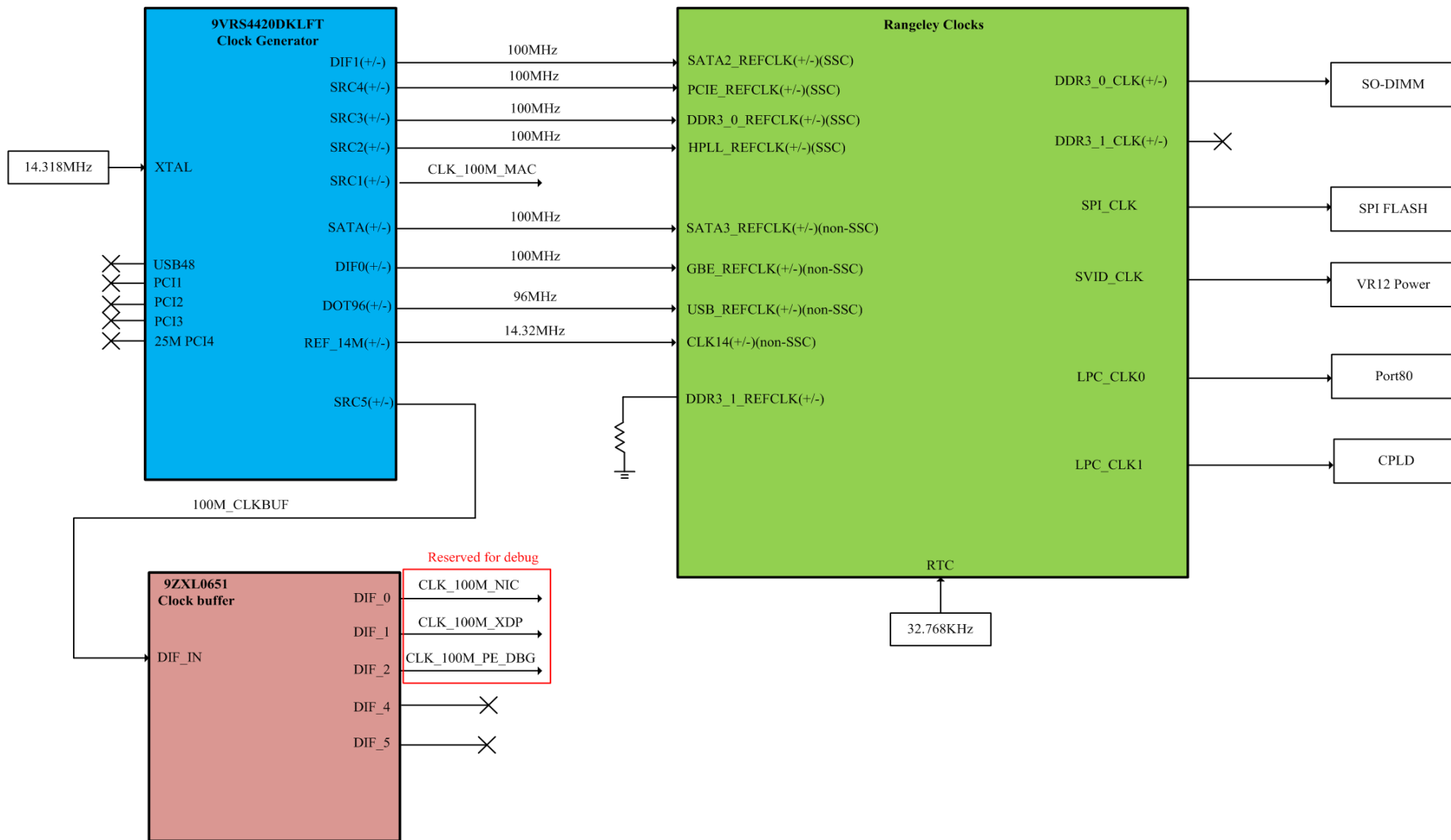


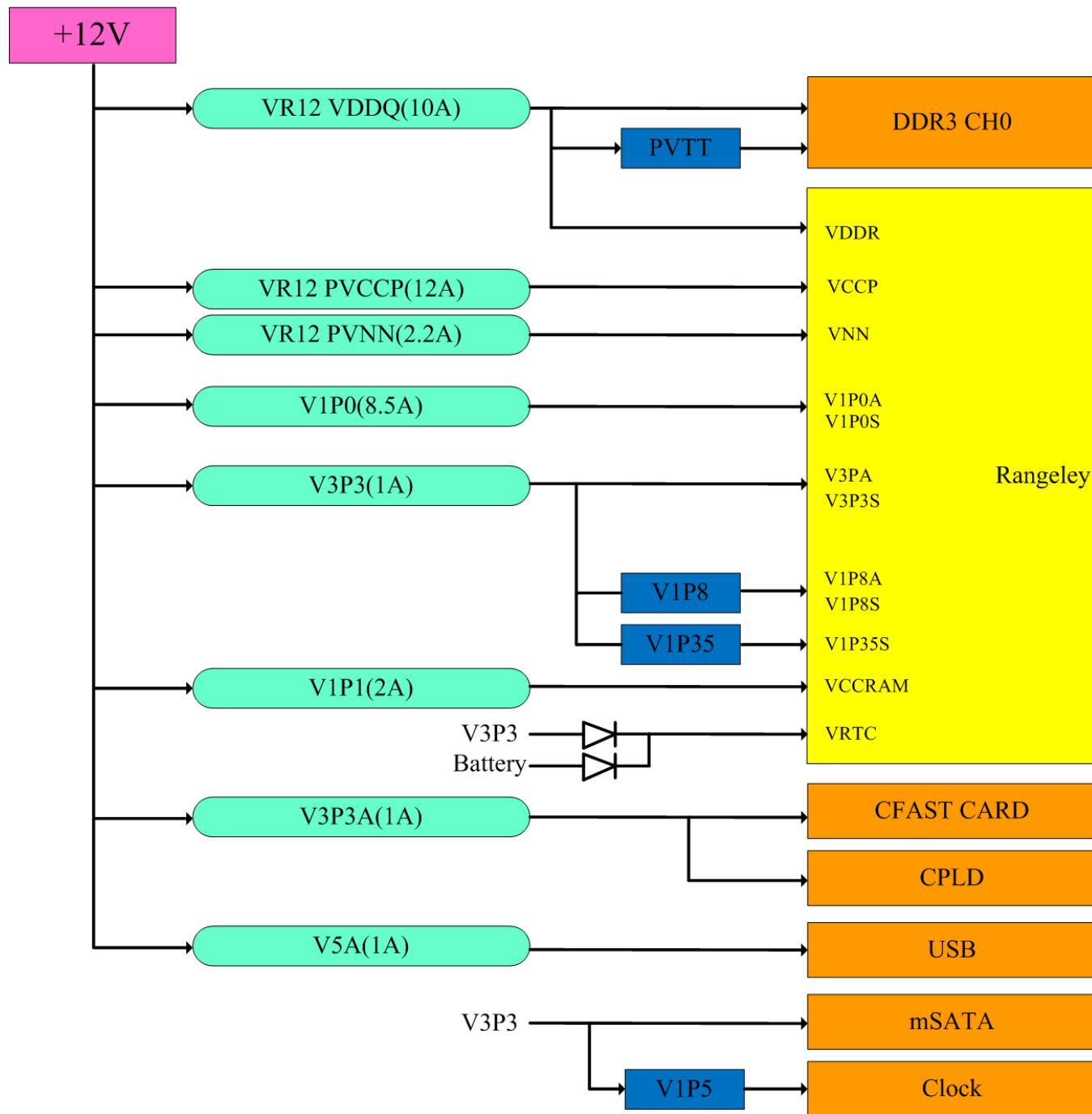
Revision History		Date
0.1	PCB Part Number change to : 2976522000	Sep 1, 2014
1.1	1. PCB Part Number : 2976522000 2. U107 cahnge to 74LVC1G126GW for update BIOS 3. change R387 to 1Kohm and C381 to 10uF. It will sloved RTC time be eliminate default issue.	Feb 1, 2016

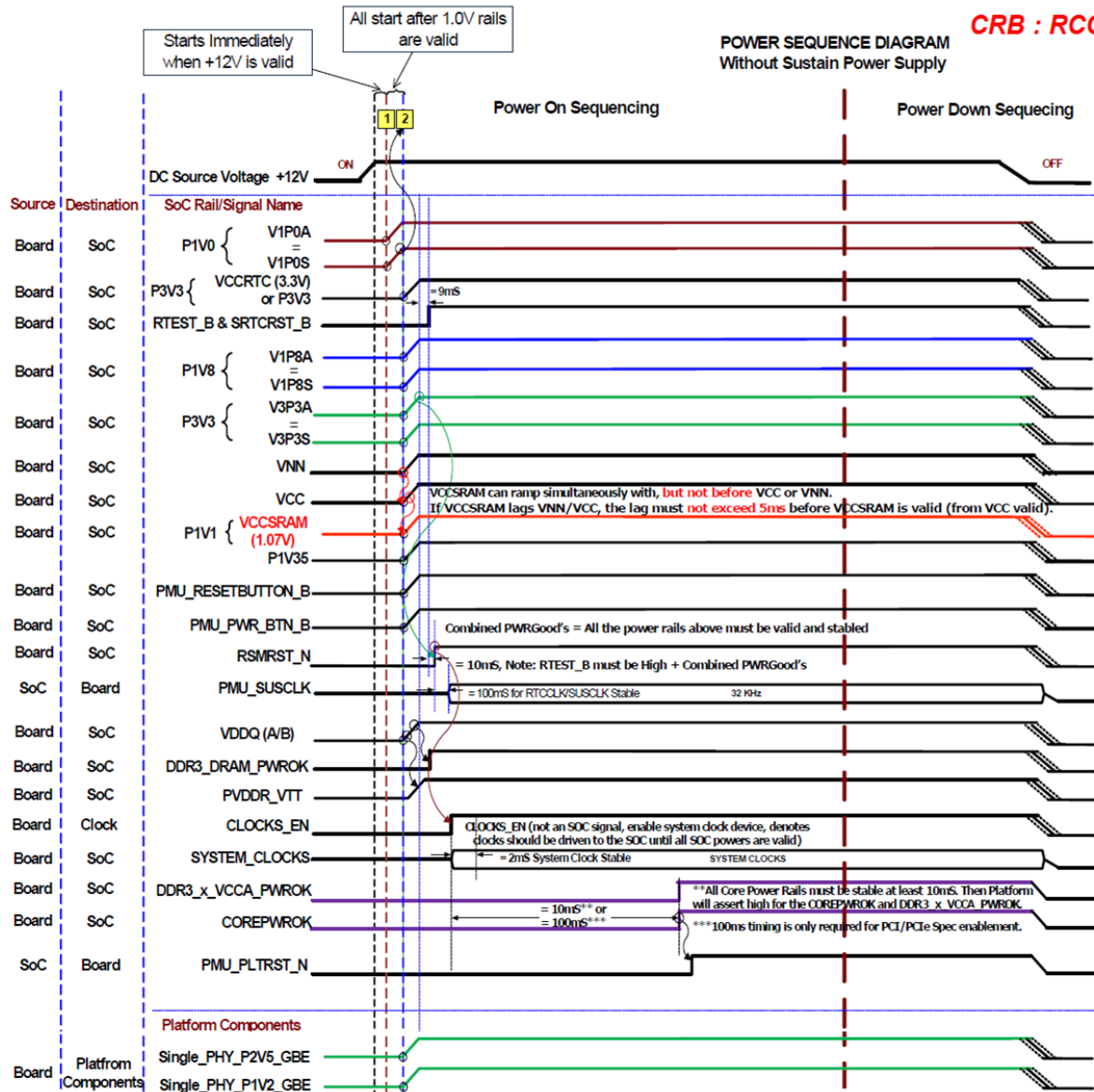
Page Descriptions
01_History 02_Function Block 03_Clock Diagram 04_Power Distribution 05_Power Sequencing 06_SMBus Diagram 07_GPIO Map 08_Rangeley_DDR3_A 09_Rangeley_DDR3_B 10_Rangeley_PCl_e_GbE 11_Rangeley_SATA_USB 12_Rangeley_LPC_SMB_MISC 13_Rangeley_POWER_1 14_Rangeley_POWER_2 15_Rangeley_GND 16_CLOCK GENERATOR 17_DDR3-SODIMM_A 18_DDR3-SODIMM_B 19_Debug_UART_USB_DC12V_PCl_eCon 20_XDP_PORT80_BIOS 21_MISC_RESET 22_POWER_CPU_DDR_1 23_POWER_CPU_DDR_2_VTT 24_POWER_CPU_VCCP_VNN_1 25_POWER_CPU_VCCP_VNN_2 26_POWER_CPU_1V0_1V1 27_POWER_CPU_3V3 & 1V35_1V8 28_POWER_CPU_5V0A_3V3A 29_CPLD 30_B2B_Connector 31_SMB_MUX/CPLD JTAG

Note:
1.All of resistors are 5%, 0603 SMD except other specified description.
2.All of capacitors are 50V except other specified description.
3.All of aluminous capacitors are 105 degree C except other specified description.
4. # for LOW active signals(name#)

SCHEMATICS OF	FILE NAME	DRAWN	DESIGNED	CHECKED	APPROVED	Agema Systems, INC.
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						File 01_History
						Size C
						Document Number 1ADSS-0XXXXX
						Rev 1.1
						Date: Friday, October 07, 2016
						Sheet 1 of 31



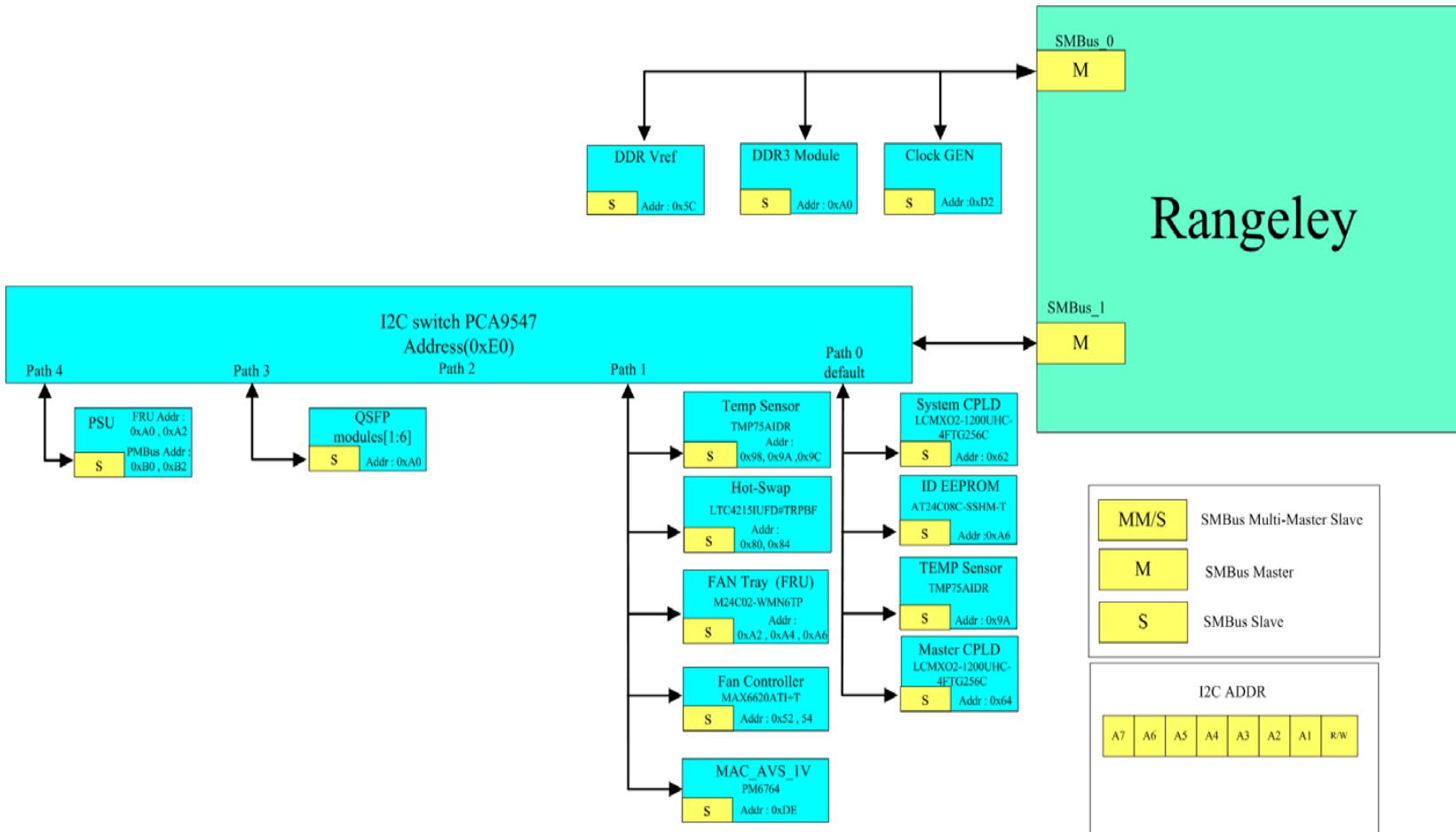




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File		
05_Power Sequencing		
Size	Document Number	Rev
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MM/S SMBus Multi-Master Slave

M SMBus Master

S SMBus Slave

I2C ADDR

A7	A6	A5	A4	A3	A2	A1	R/W
----	----	----	----	----	----	----	-----

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File			06_SMBus Diagram
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Date:	Friday, October 07, 2016	Sheet	6 of 31

5 4 3 2 1

D

C

B

A

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File

07_GPIO Map

Size

C

Document Number

1ADSS-0XXXXX

Rev

1.1

Date

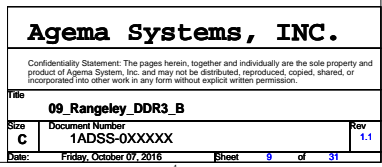
Friday, October 07, 2016

Sheet

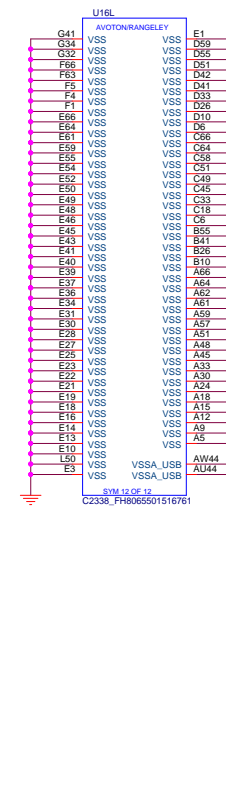
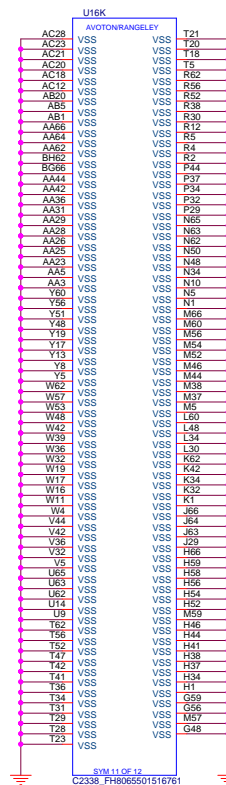
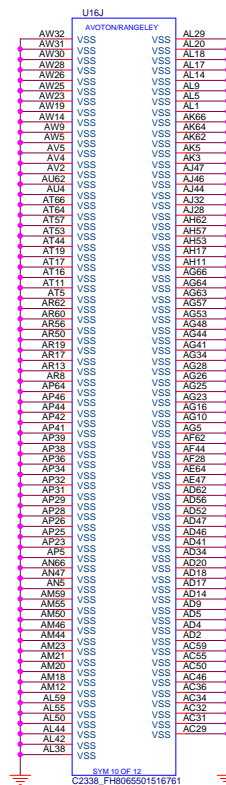
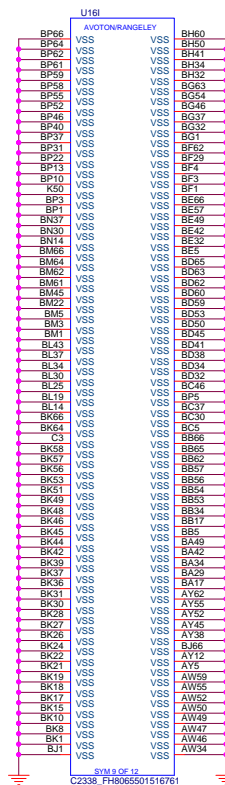
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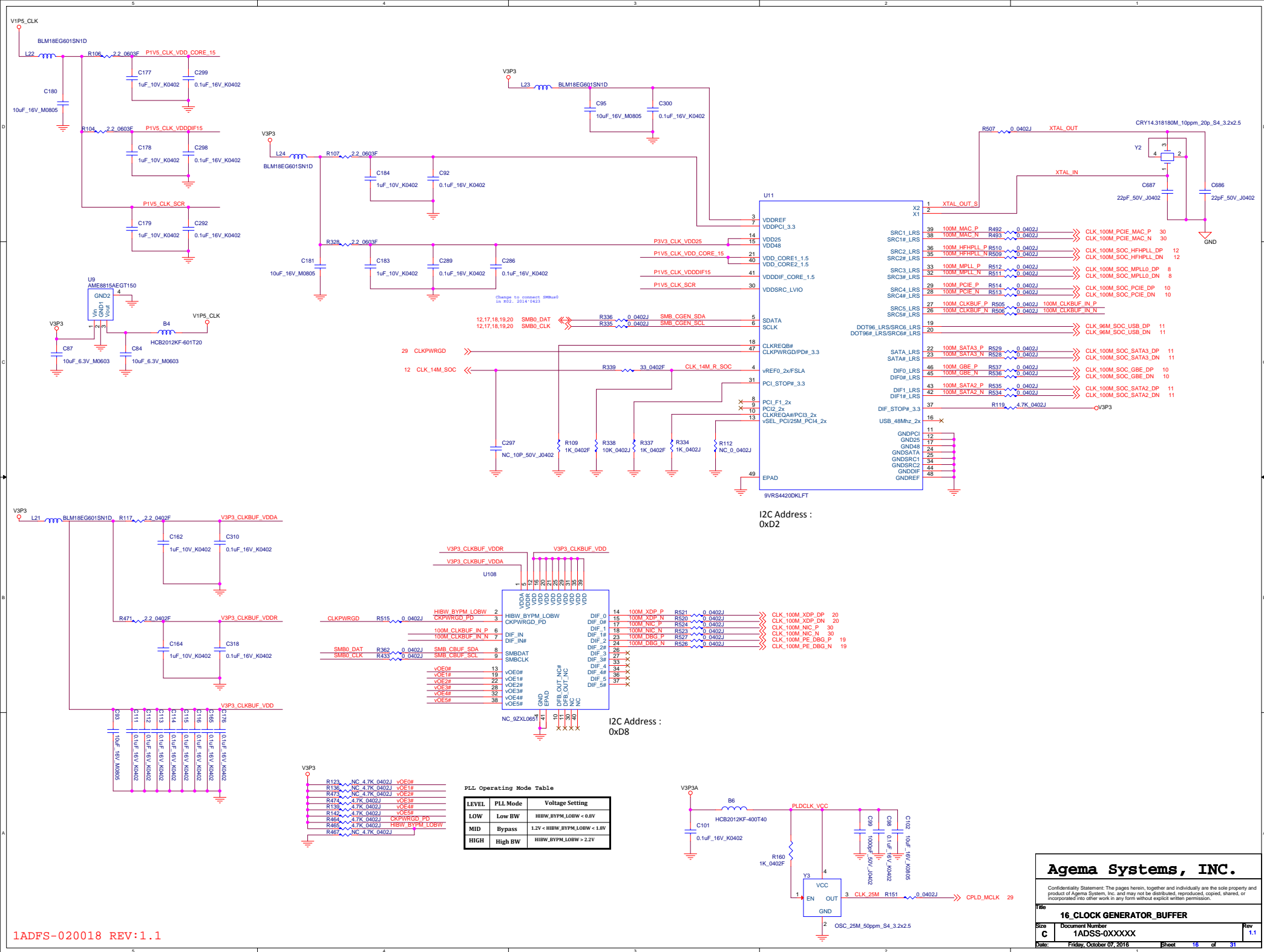
of

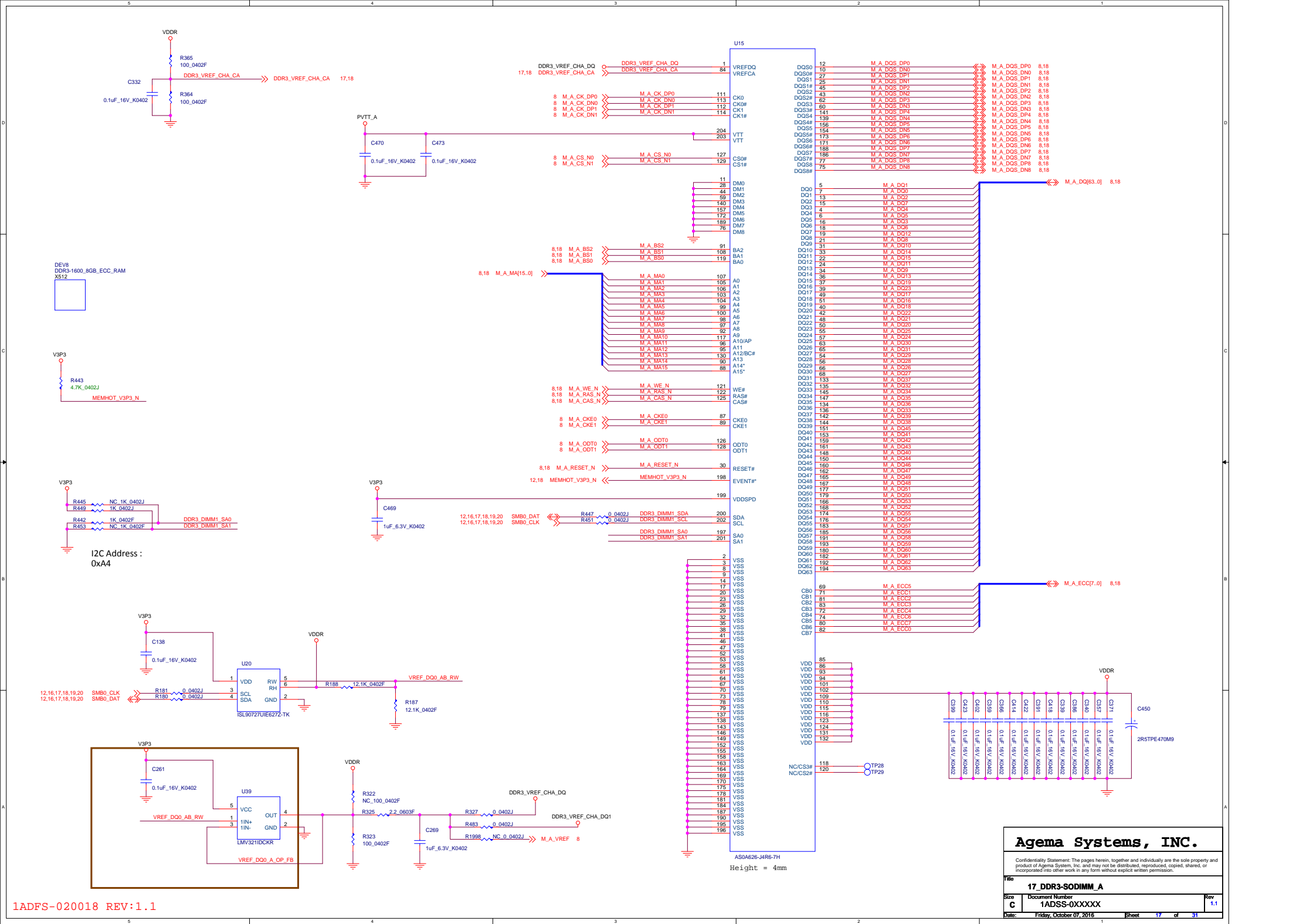
31



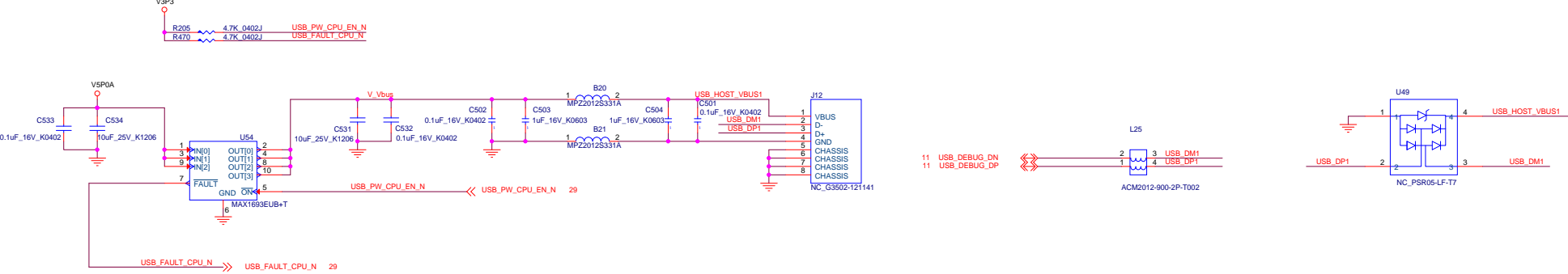




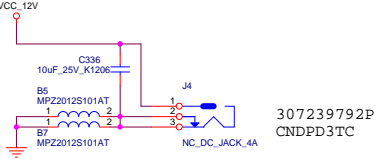




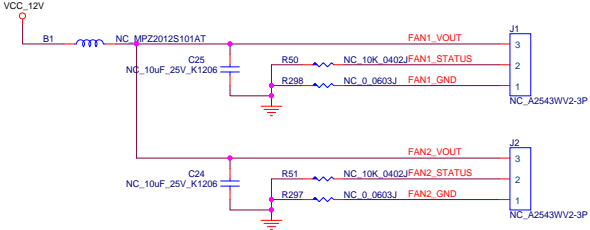
USB Port



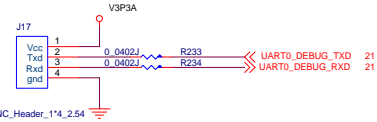
DC-12VIN Connector For Debug



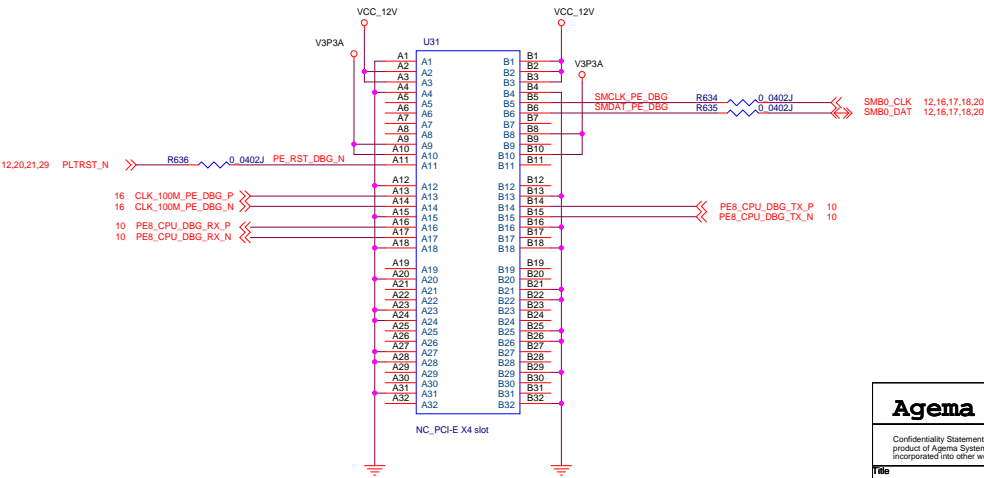
FAN Connector (Reserved)



Console Port (RJ45)



PCIe Slot

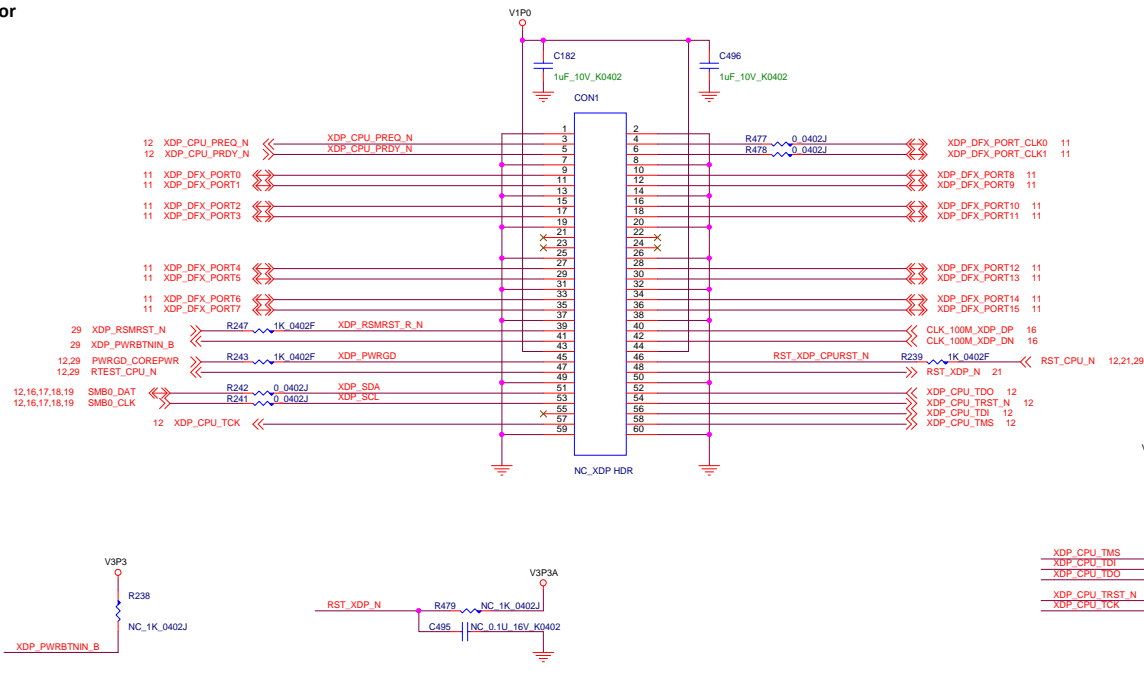


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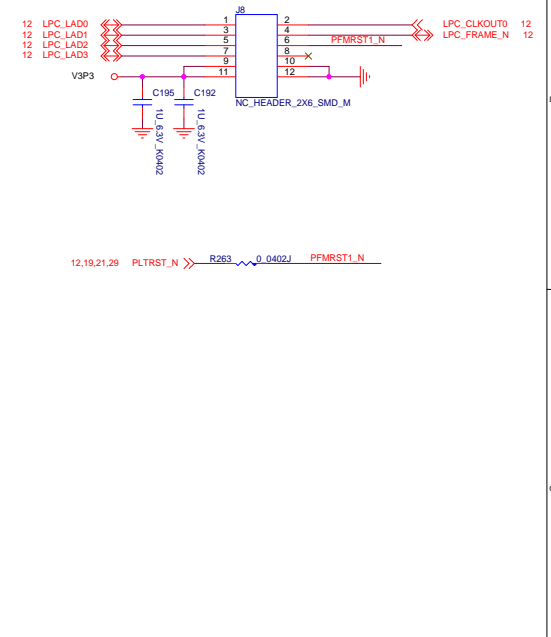
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File	18_Debug_UART_USB_DC12V_PcLeCon		
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1. XDP Connector

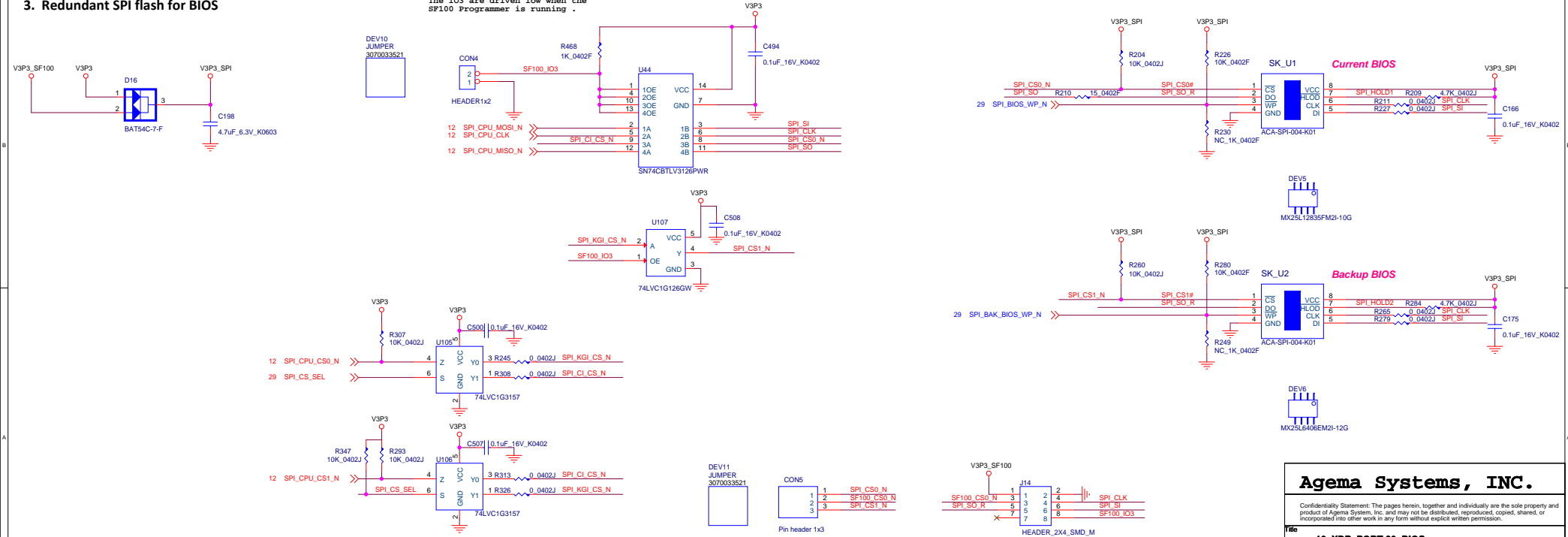


2. PORT-80 Connector



3. Redundant SPI flash for BIOS

The IO3 are driven low when the SF100 Programmer is running .

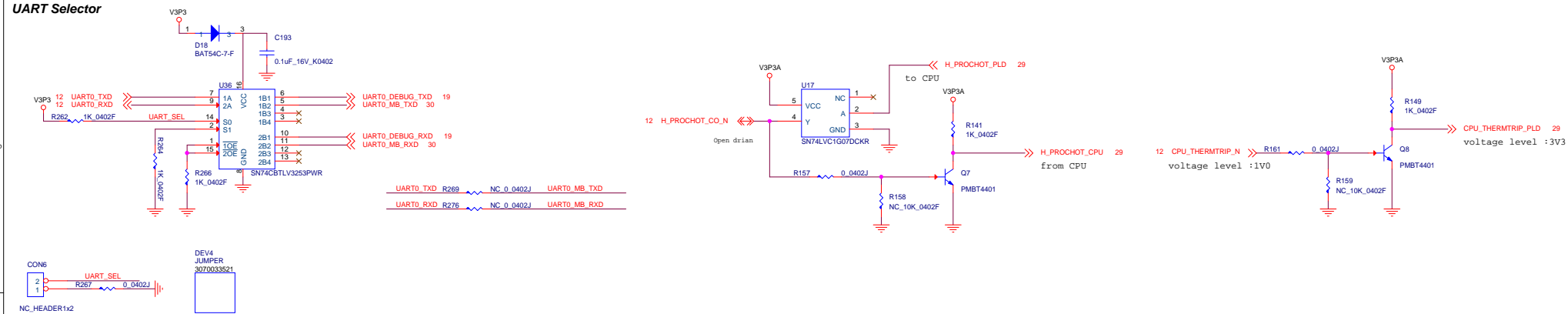


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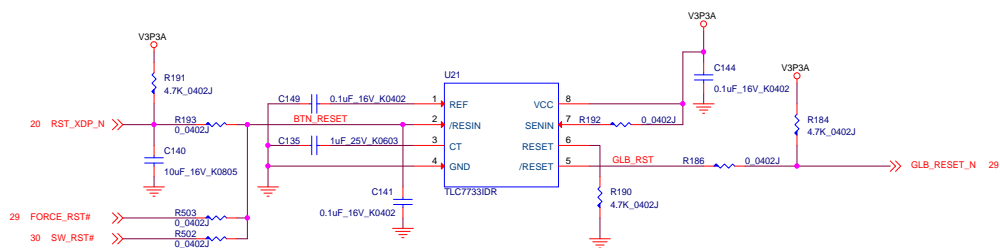
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File	19_XDP_PORT 80_BIOS
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UART Selector



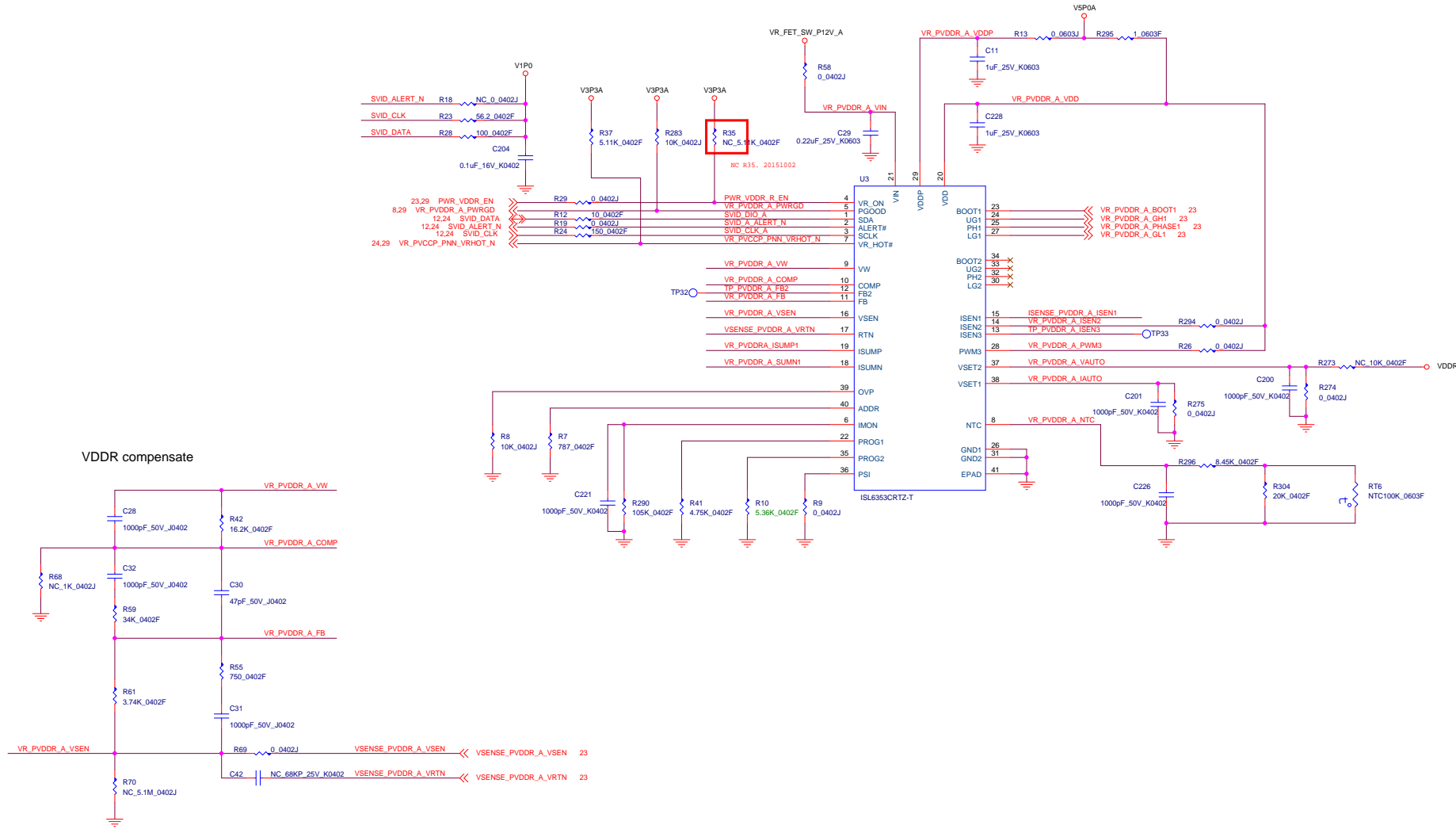
Reset IC



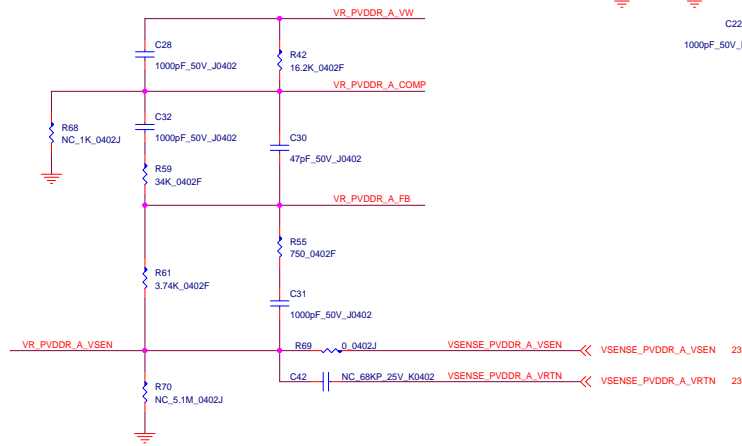
LEDs for debug



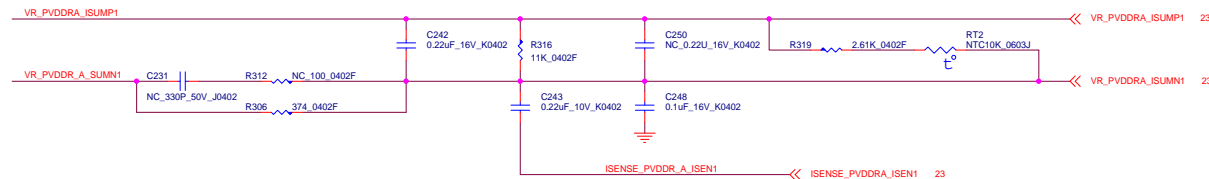
1ADFS-020018 REV:1.1



VDDR compensate



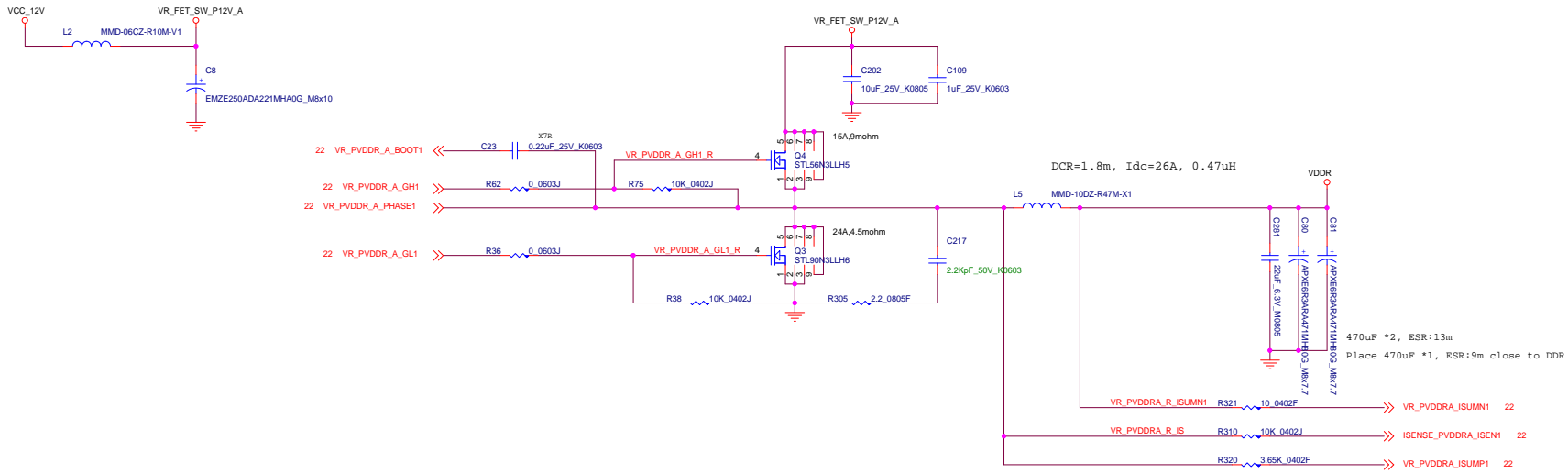
VDDR Isense compensate



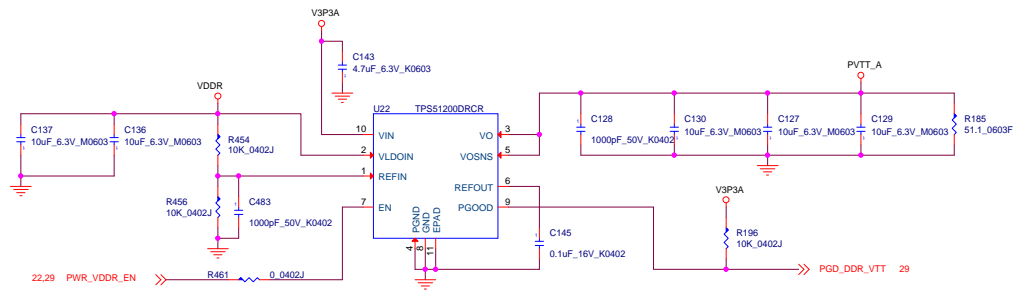
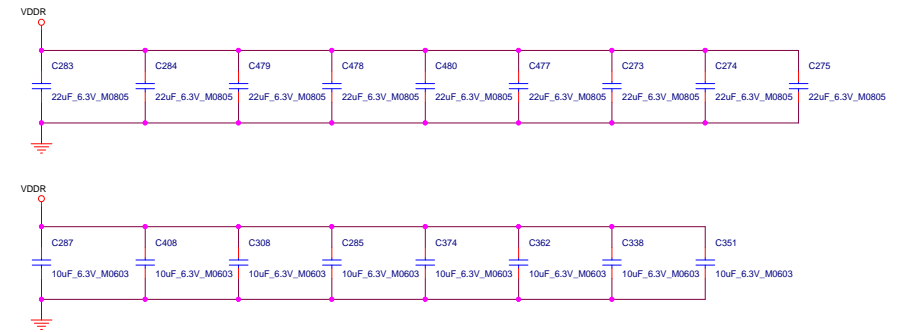
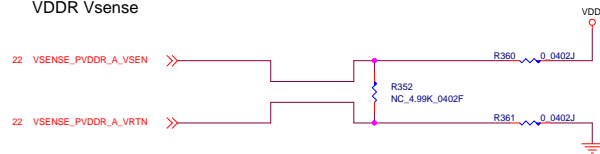
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File	21_POWER_CPU_DDR_1		
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VDDR Vsense



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File	22_POWER_CPU_DDR_2_VTT		
Size	Document Number	1ADSS-0XXXXX	Rev 1.1
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VR_PVCCP_VW

C22
1000pF_50V_J0402

R33
8.06K_0402F

VR_PVCCP_COMP

C15
680pF_50V_J0402

C10
68pF_50V_J0402

R22
20K_0402F

VR_PVCCP_FB

C6
1000pF_50V_K0402

R21
453_0402F

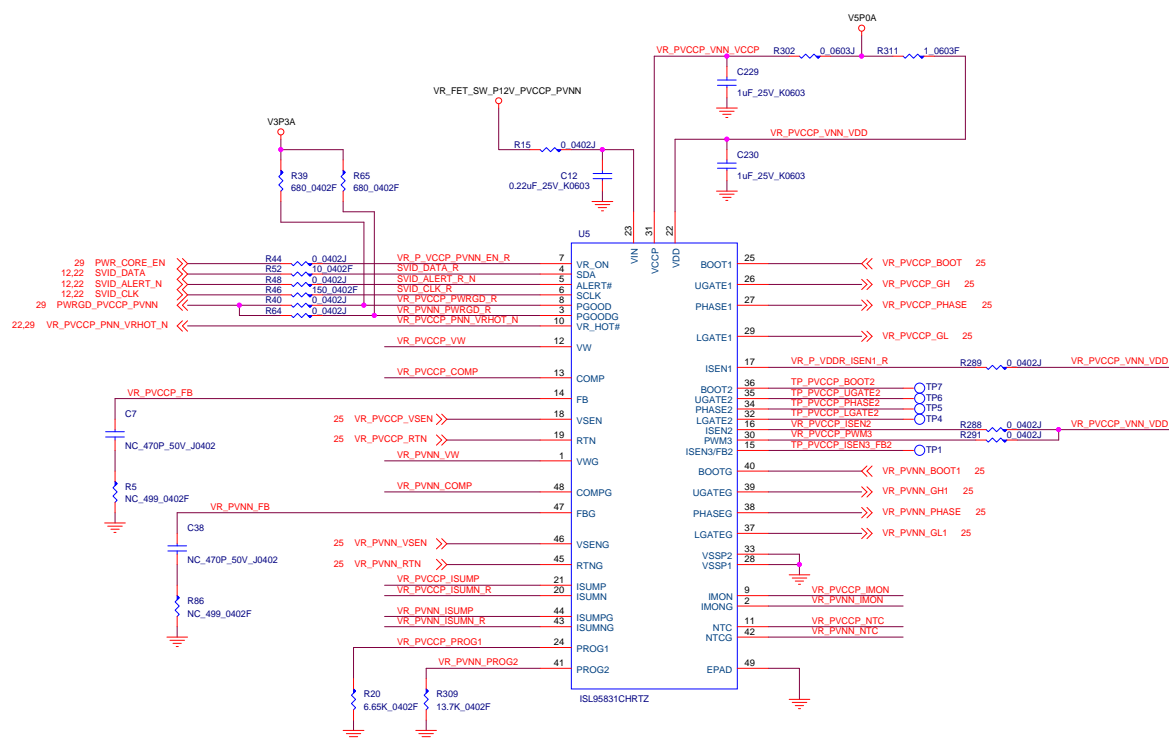
R17
865_0402F

VR_PVCCP_VSEN

The schematic diagram for the VR_PVNN_VW section shows the following components and connections:

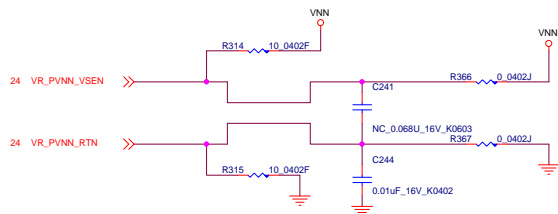
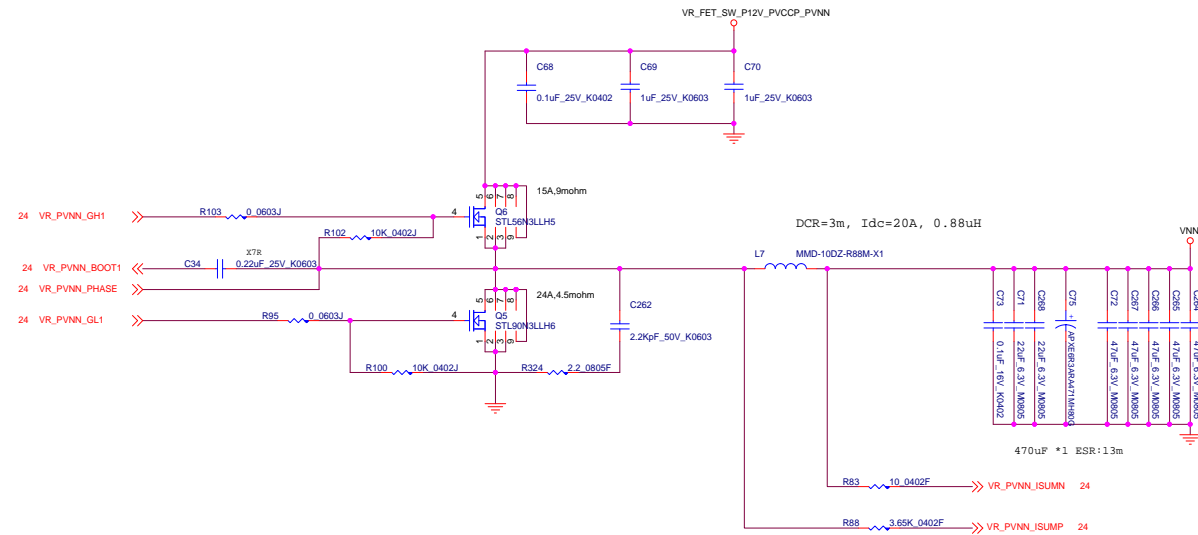
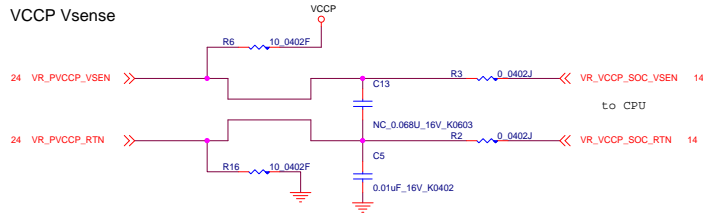
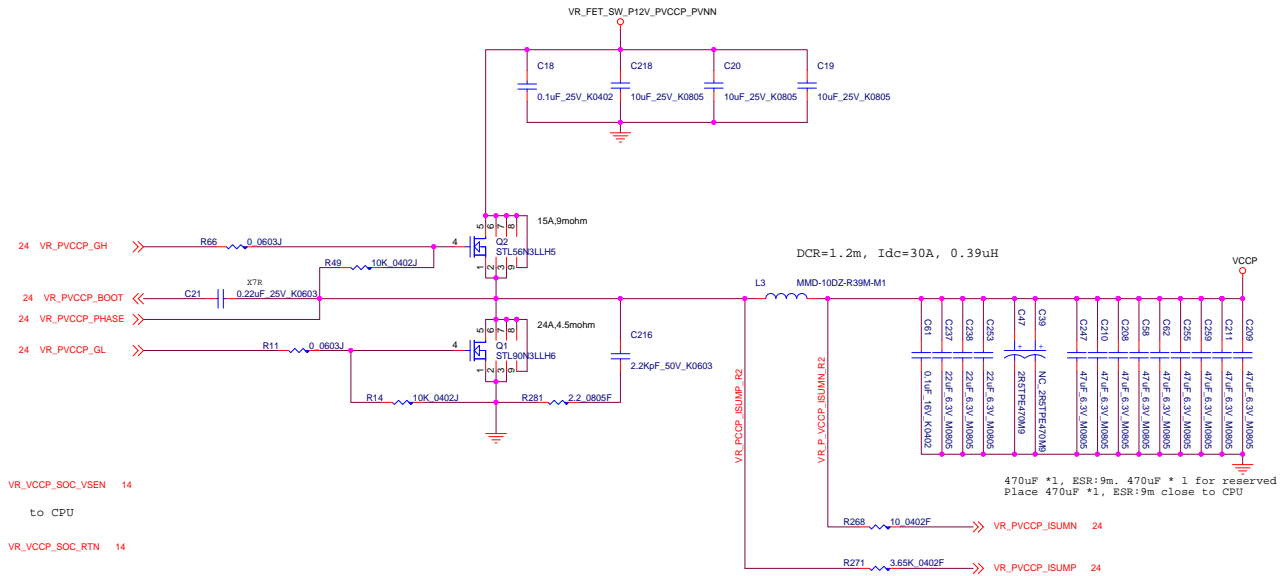
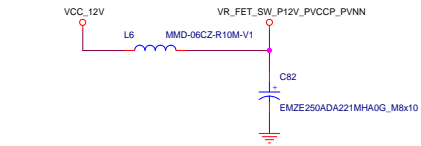
- Capacitors:**
 - C33: 1000pF_50V_J0402
 - C35: 1000pF_50V_J0402
 - C45: 68pF_50V_J0402
 - C48: 330pF_50V_J0402
- Resistors:**
 - R63: 8.06K_0402F
 - R72: 10K_0402J
 - R87: 249_0402F
 - R89: 422_0402F
- Inductors:**
 - VR_PVNN_VW
 - VR_PVNN_COMP
 - VR_PVNN_FB
 - VR_PVNN_VSEN

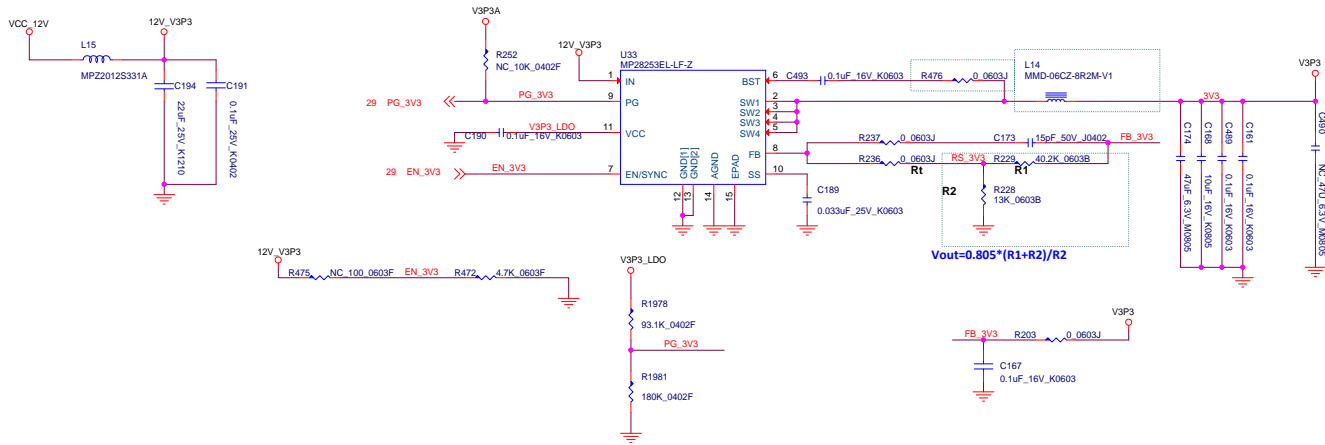
The components are interconnected between various power and ground planes, including VR_PVNN_VW, VR_PVNN_COMP, VR_PVNN_FB, and VR_PVNN_VSEN.



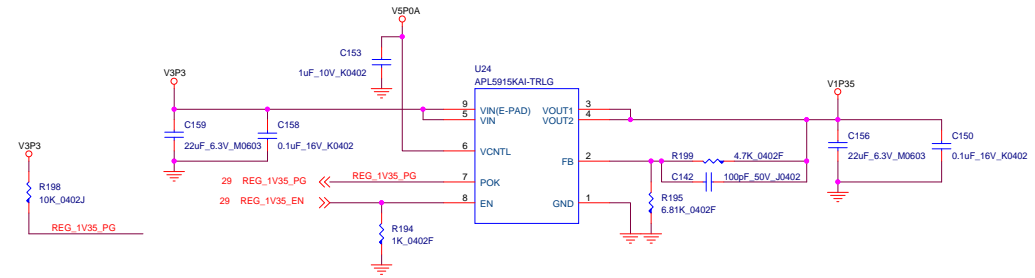
The schematic diagram shows a voltage divider circuit. A 5V source (NC_1KP_50V_K0402) is connected to a network of resistors and an NTC. The network consists of R286 (37.4K_0402F) in series with a parallel combination of R282 (3.92K_0402F) and RT1 (NTC100K_0603F). The output voltage is labeled VR_PVCCP_NTC.

[illegible][illegible]

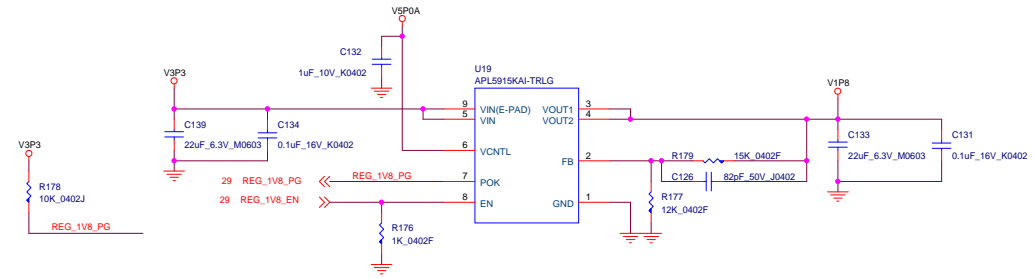




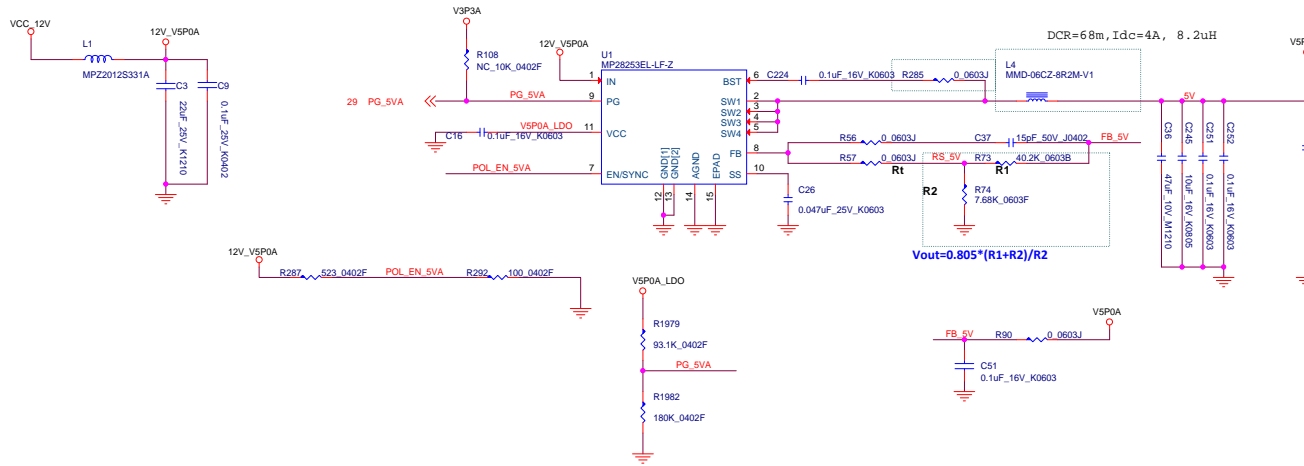
3.3V to 1.35V



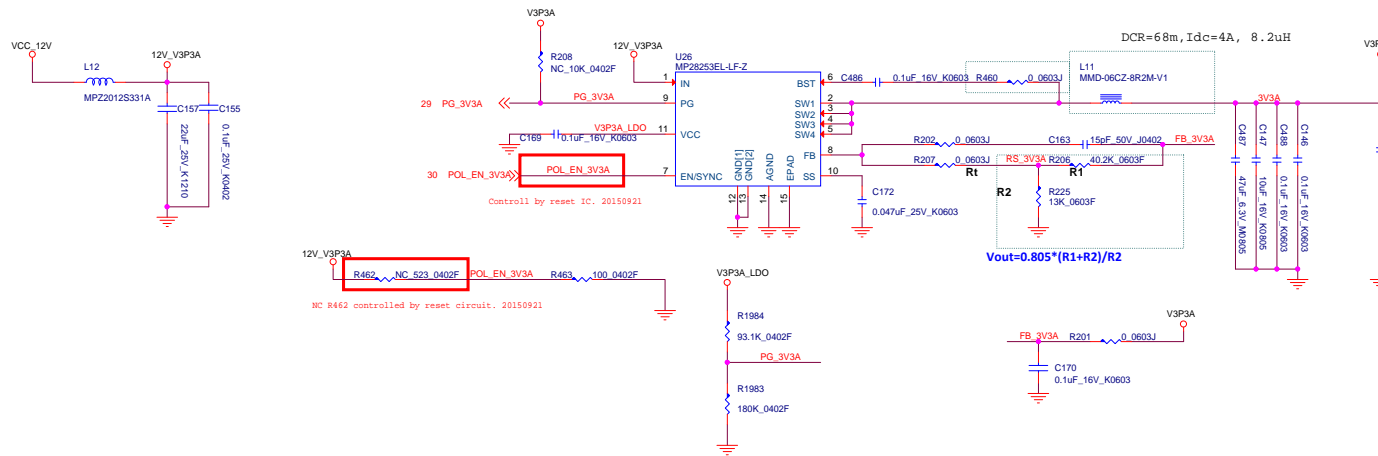
3.3V to 1.8V



5V_early @ 1A



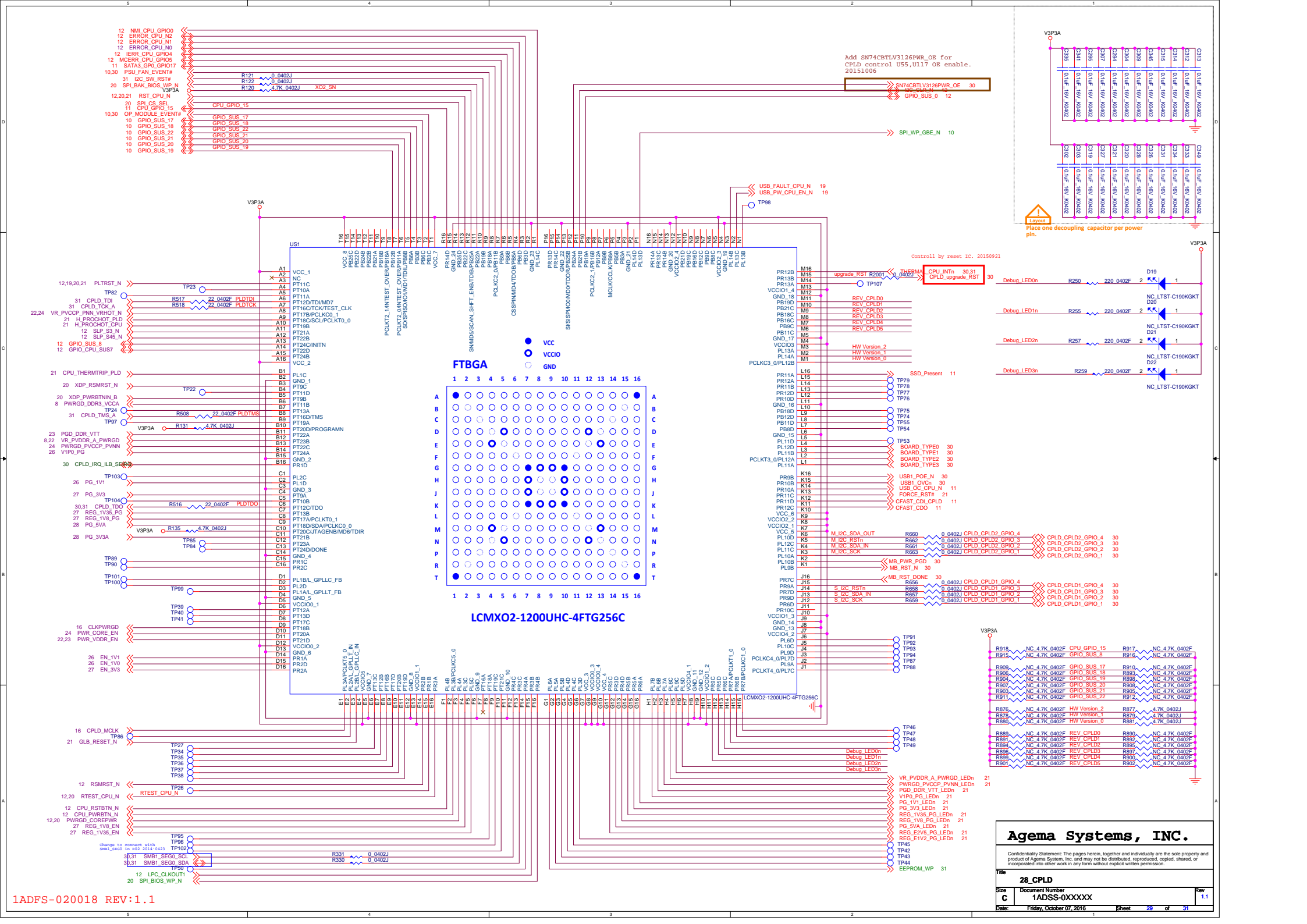
3.3V_early @ 1A

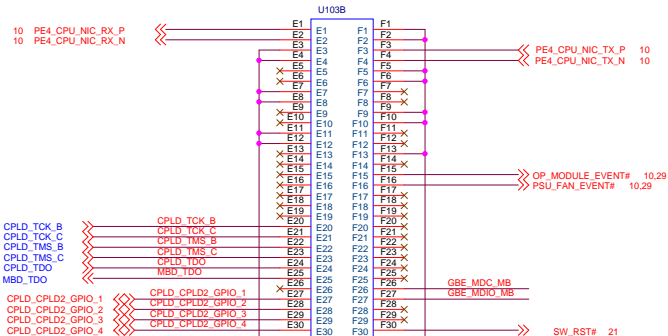
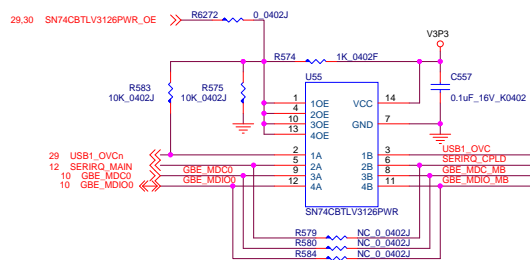
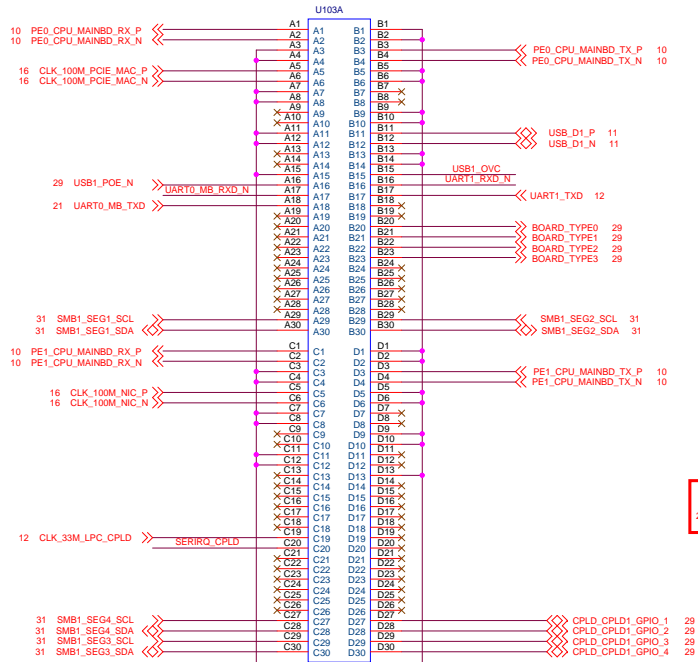


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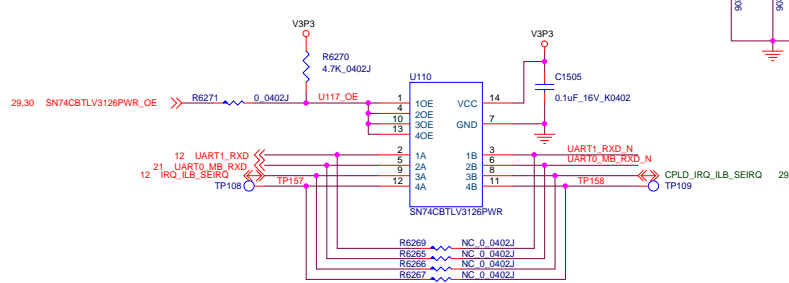
File	27_POWER_CPU_5V0A_3V3A		
Size	Document Number	1ADSS-0XXXXX	Rev 1.1
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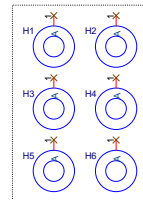


29 CPD1_upgrade_RST#
28 POL_EN_3V3A
29,31 THERMAL_CPU_INT#

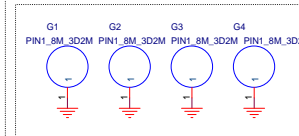
Control by reset IC: 20151005



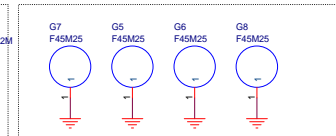
FOR SMT



FOR CPU BOARD



FOR CPU HEAT-SINK WITH STAND OFF
PUT AT SIDE2

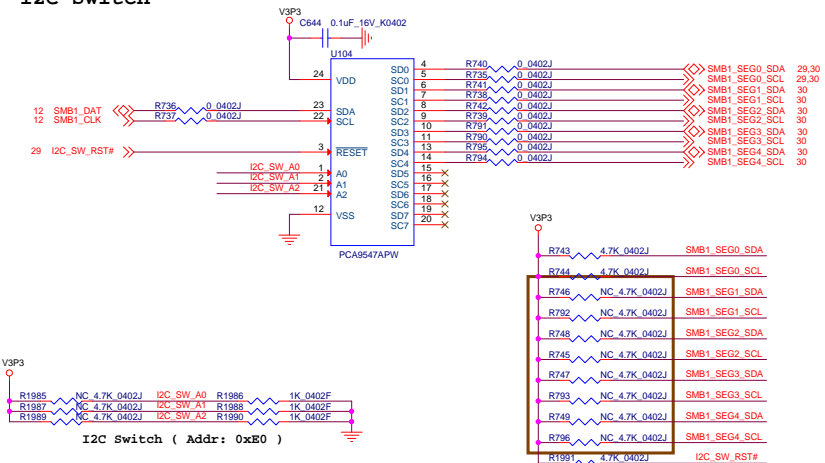


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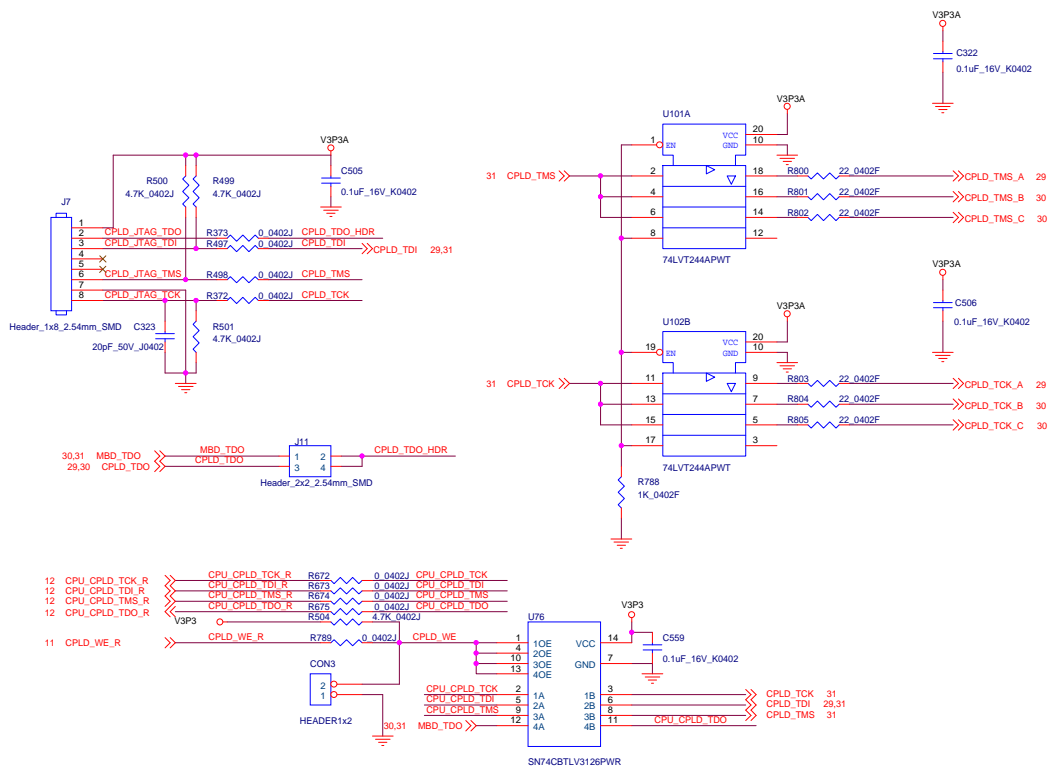
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File	29_B2B_Connector		
Size	Document Number	1ADSS-0XXXXX	
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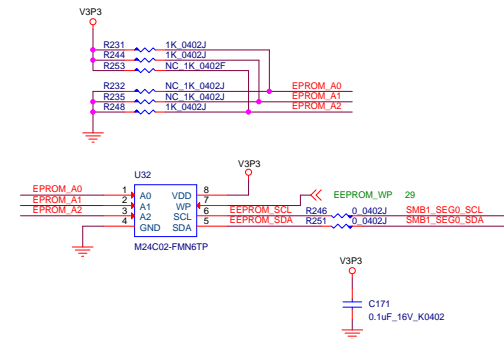
I2C Switch



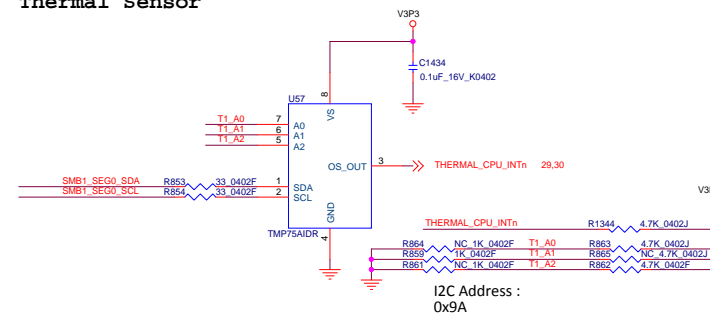
NC I2C pull high resistor to isolate the 3V3 leakage problem. 20151015



ID EEPROM



Thermal Sensor



I2C Address :
0x9A

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Title			
30_I2C_SW_TEMP Sensor_ID EEPROM			
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