Yosemite SIDE PLANE

PCB REV: D
PCBA REV: D3A
FAB: 5
SCH Rev: V01
LAST UPDATE: 2015/12/22

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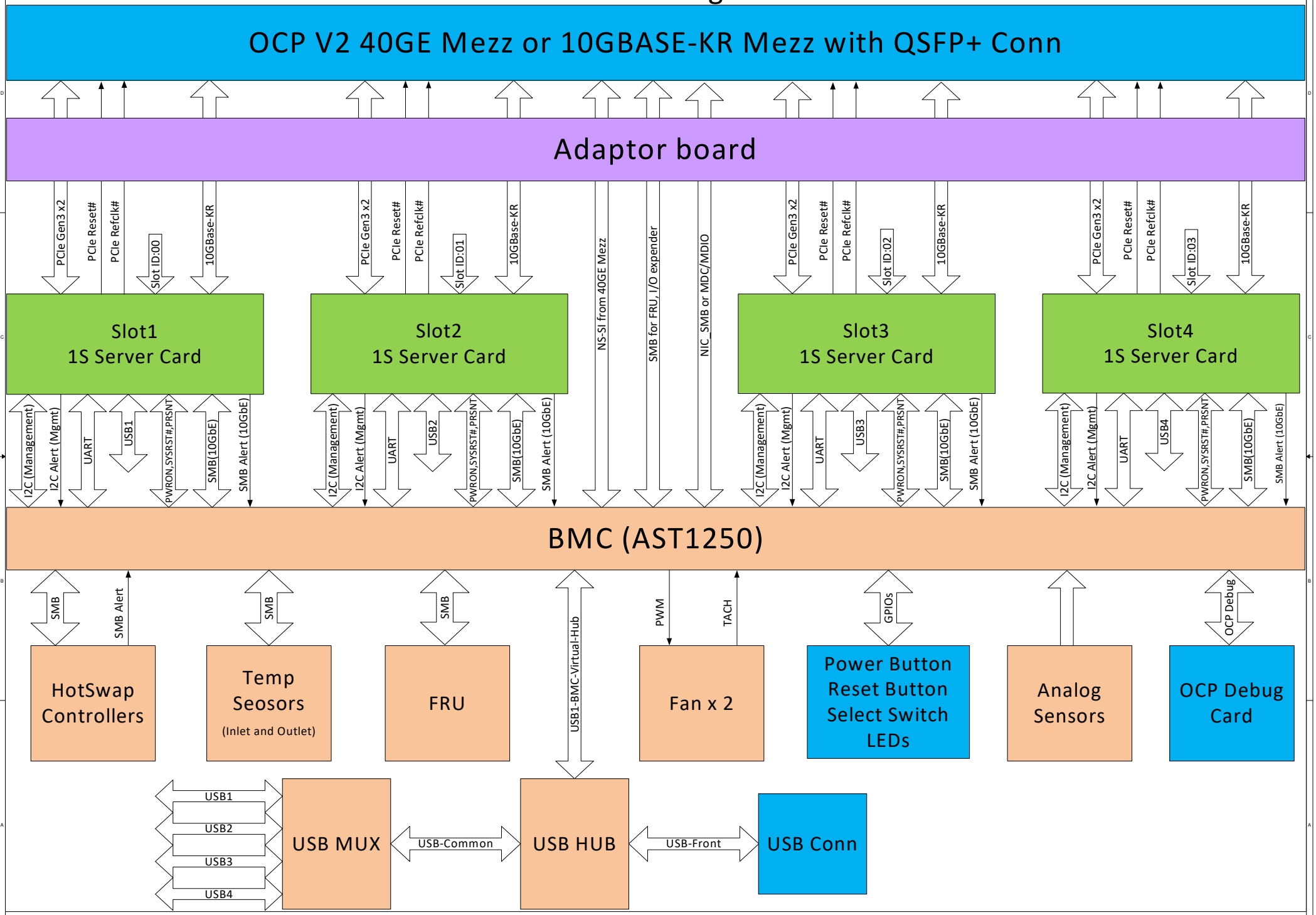
Yosemite Block Diagram V0.07



Board Block Diagram

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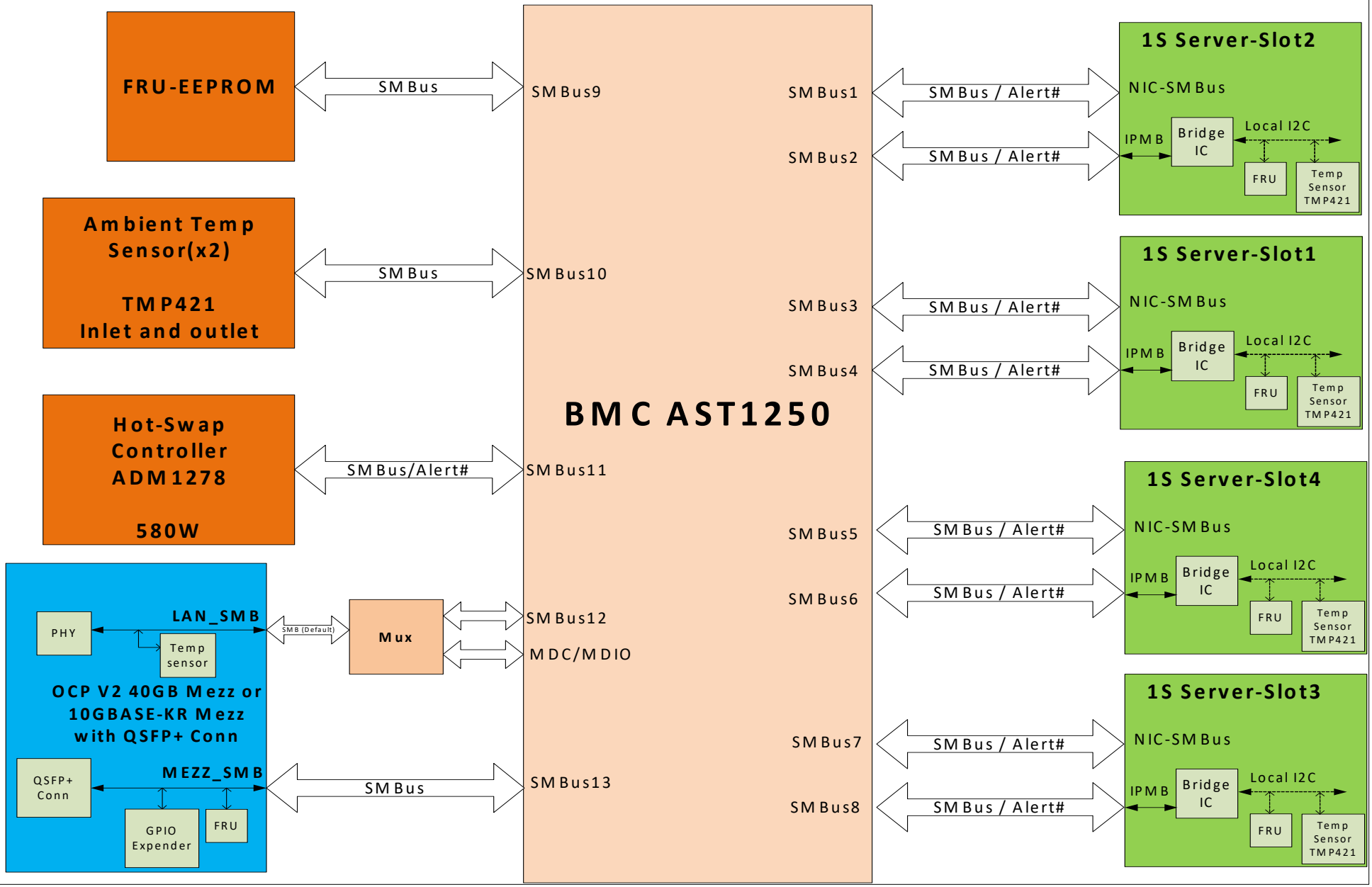
Yosemite SMB Diagram V0.05



SMBus Block Diagram

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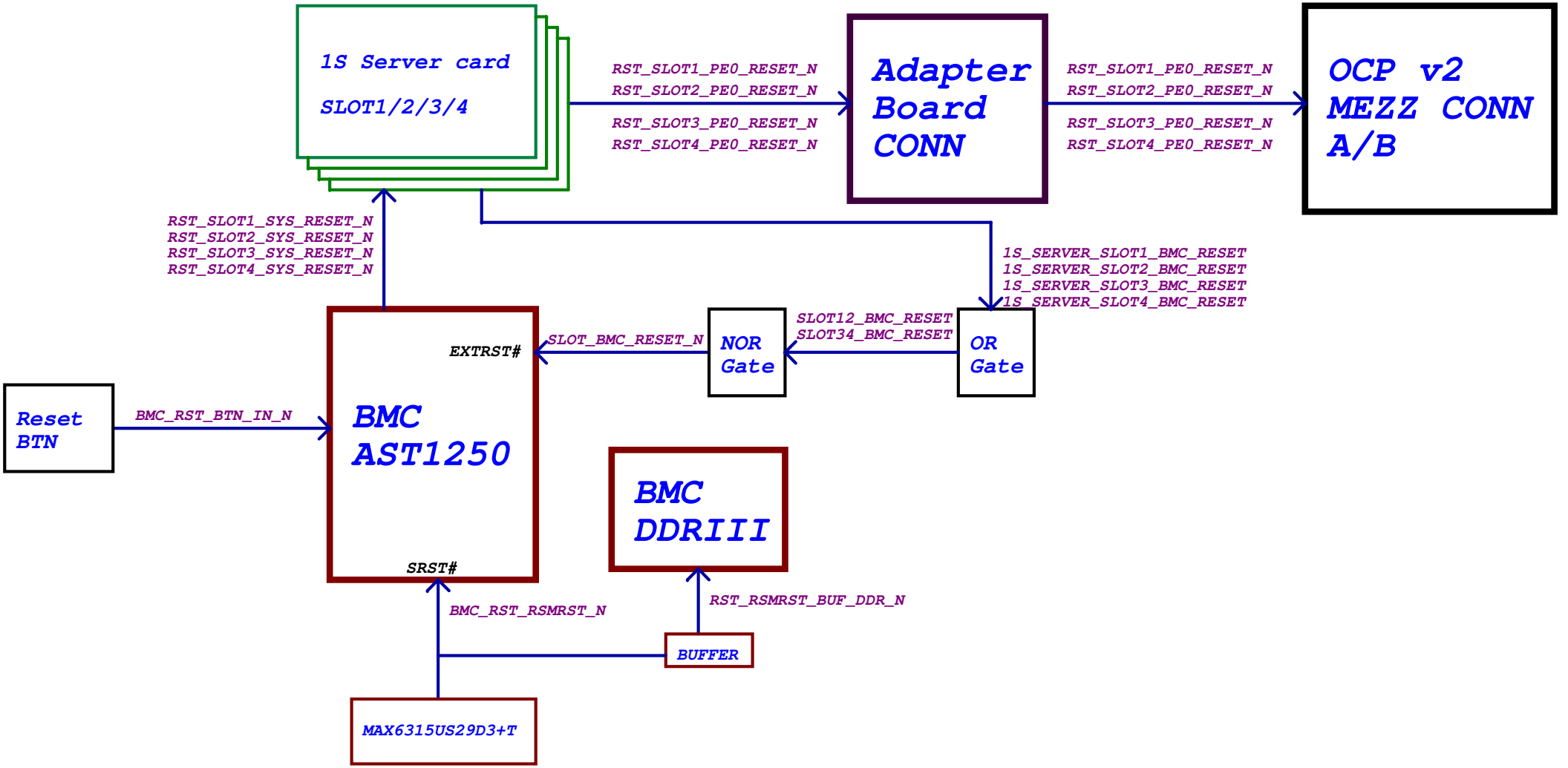
Reset Block Diagram v02



Reset Block Diagram

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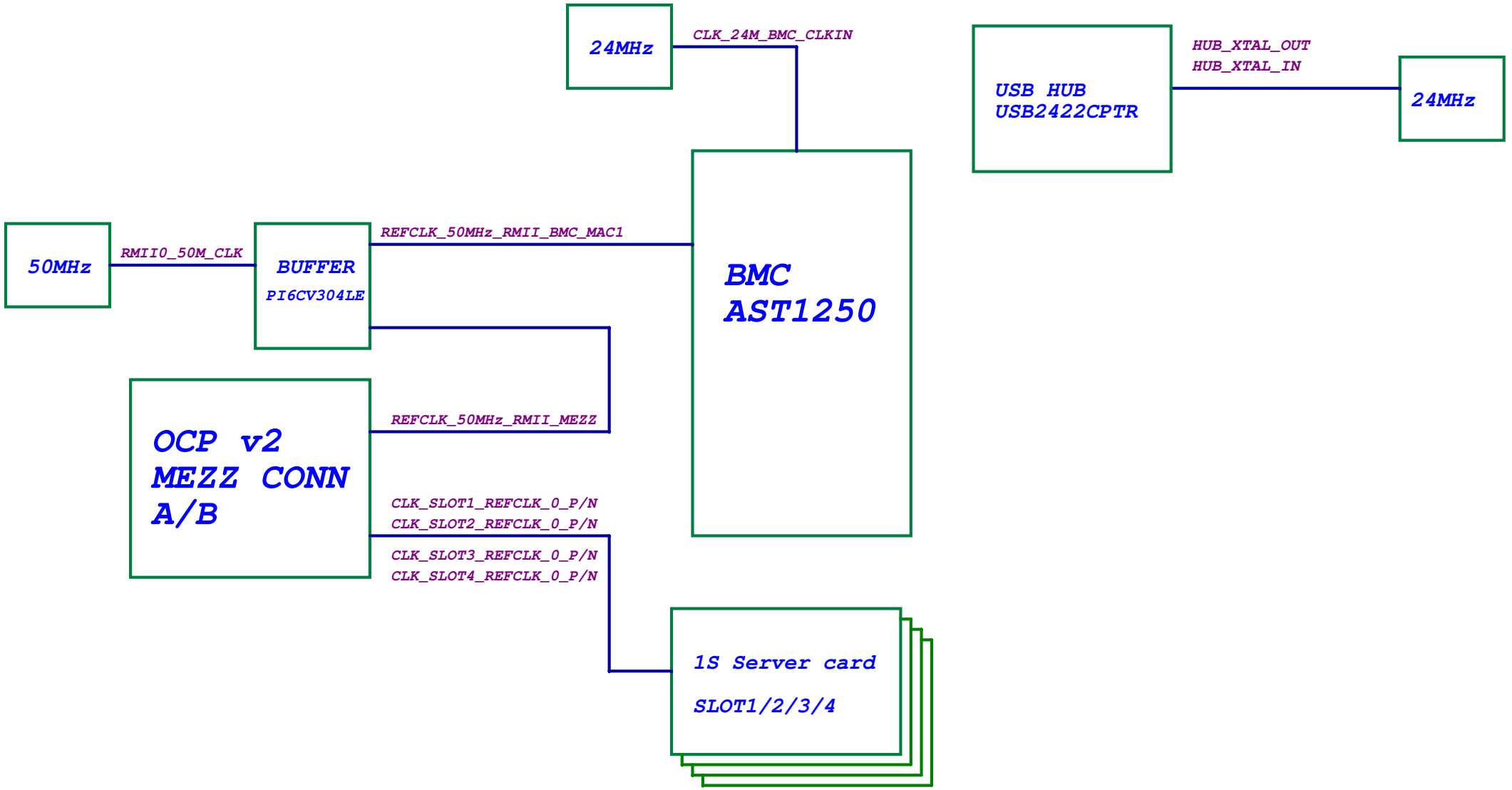

Clock Block Diagram

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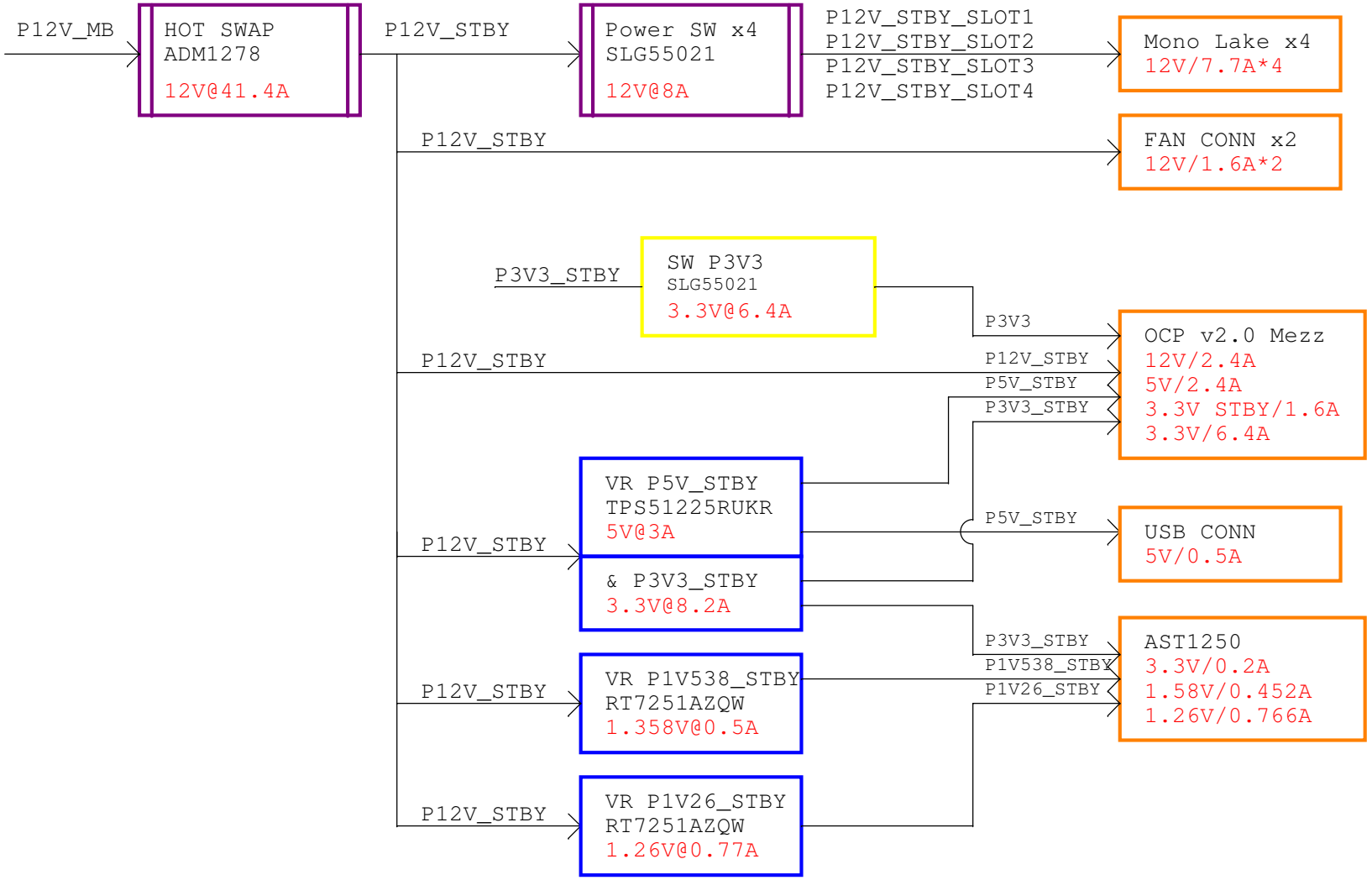
Power Block Diagram v0.4



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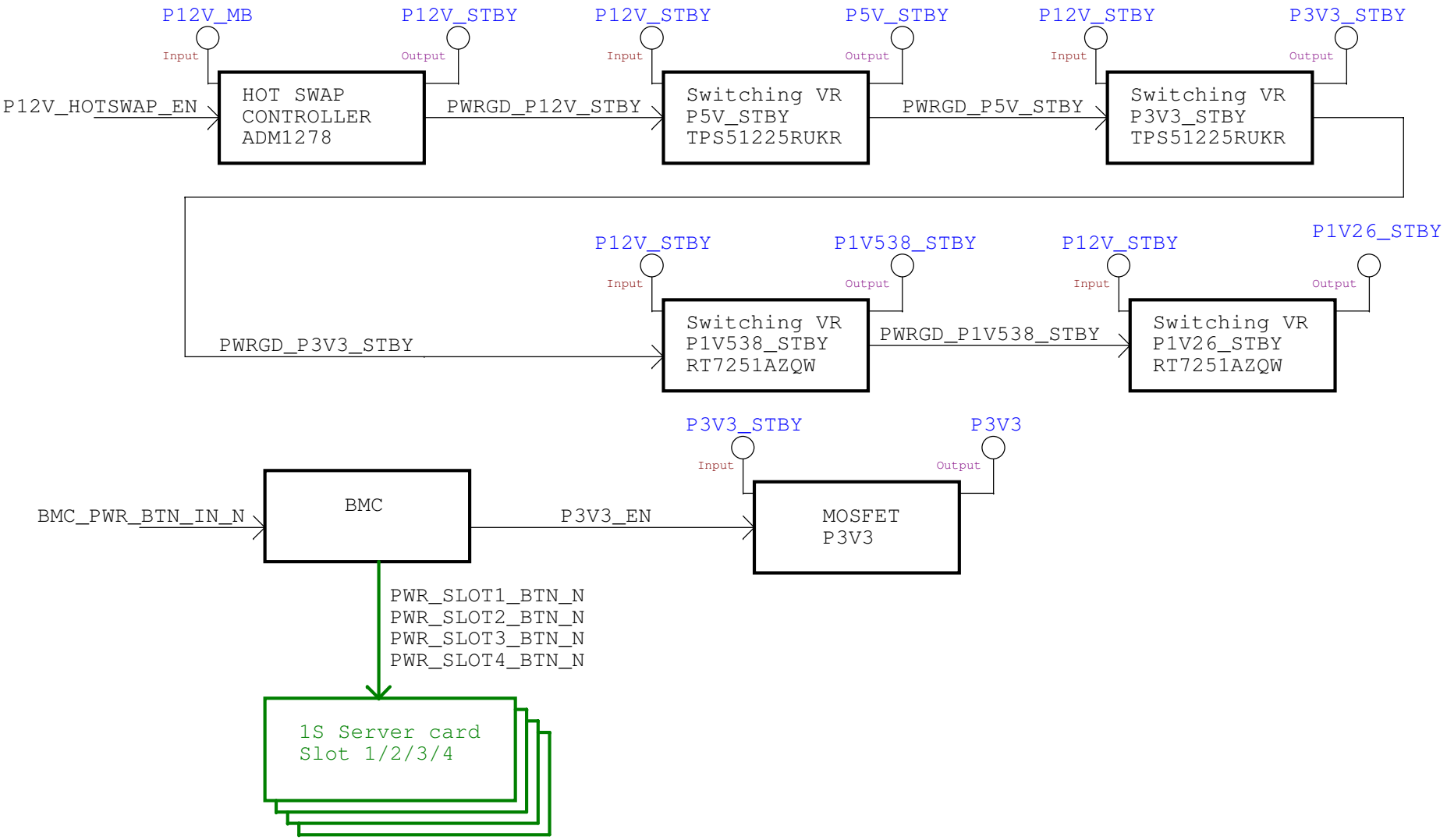
Power Sequence SYSTEM v0.4



Power Sequence SYSTEM

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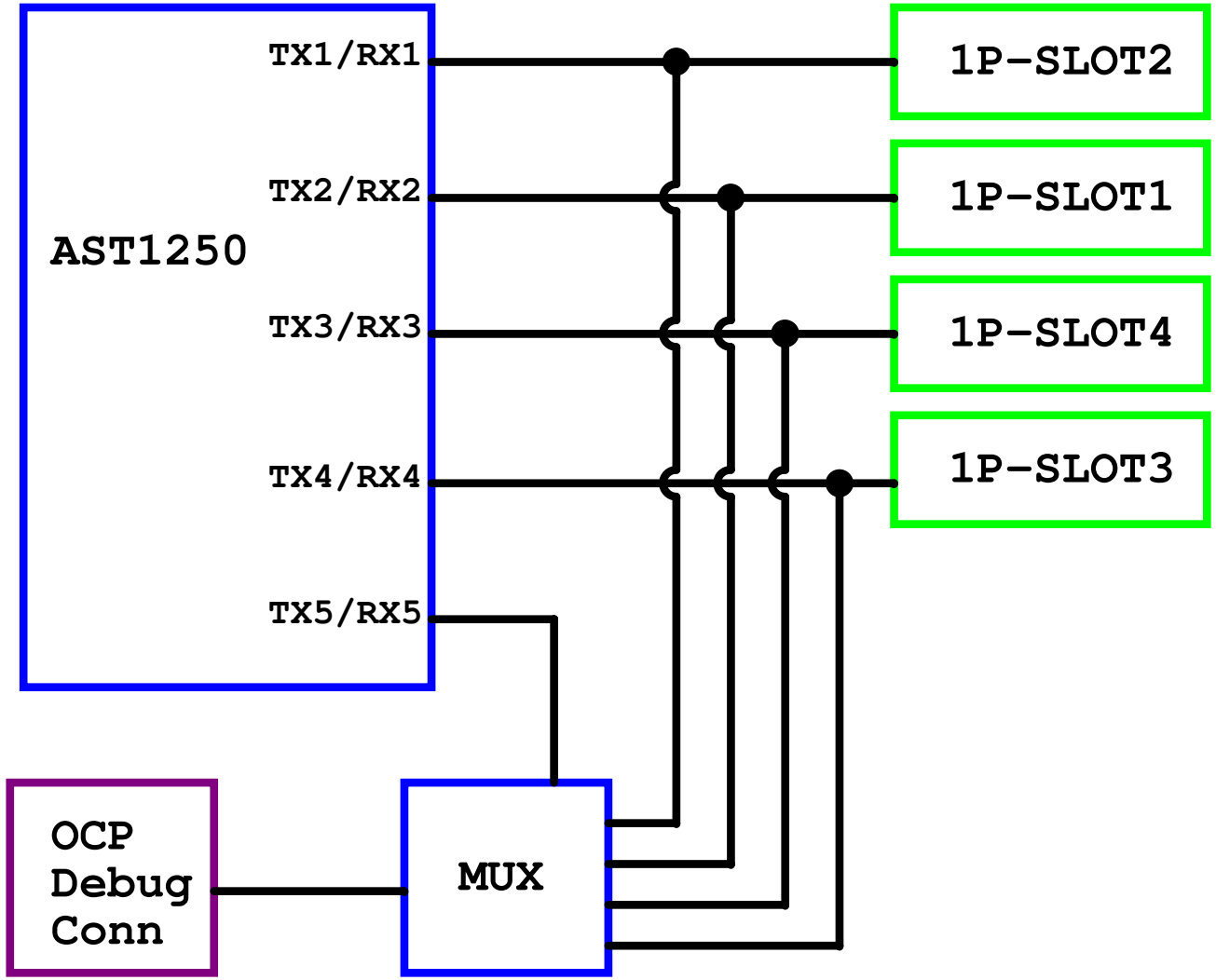
UART Topology v0.2



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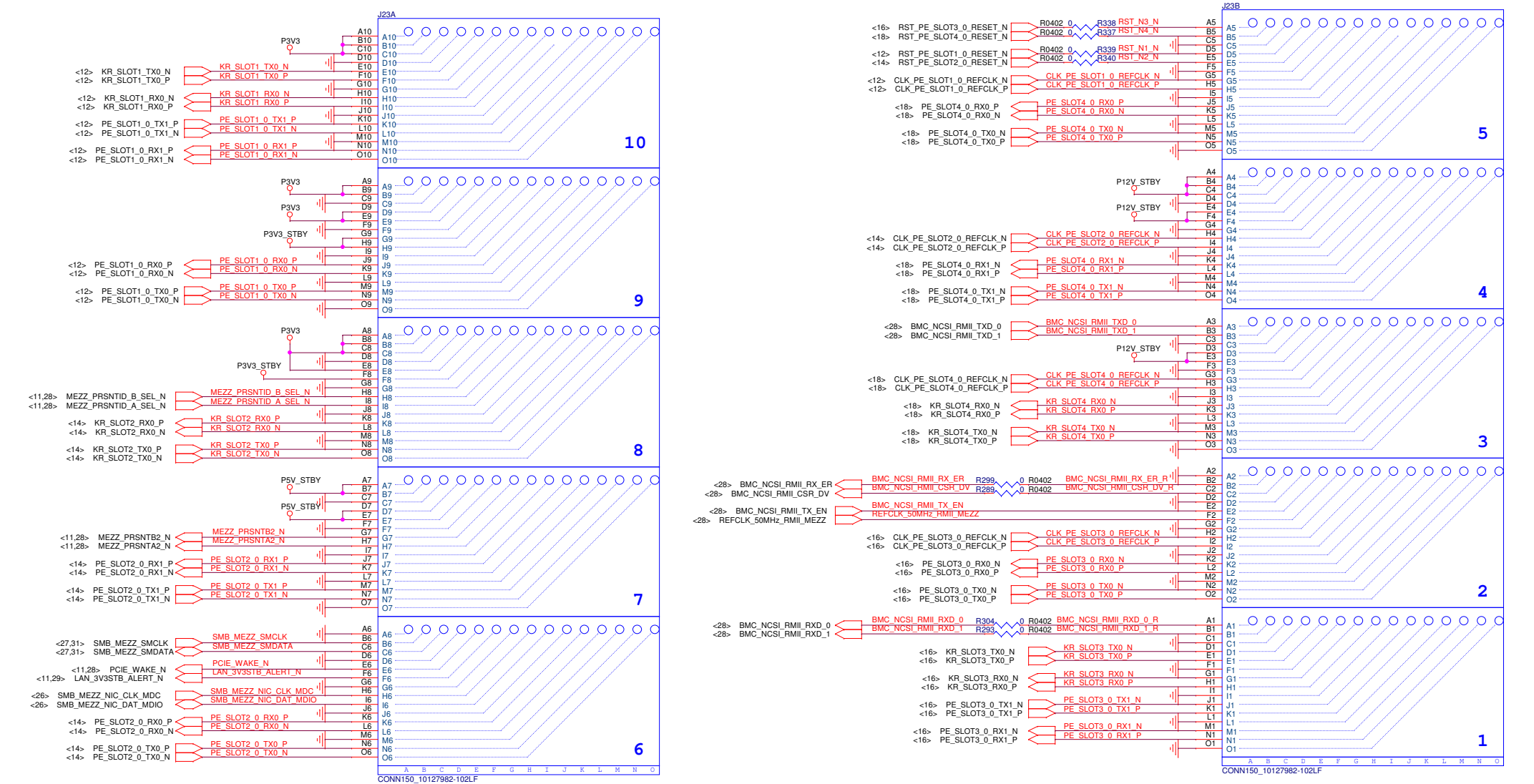
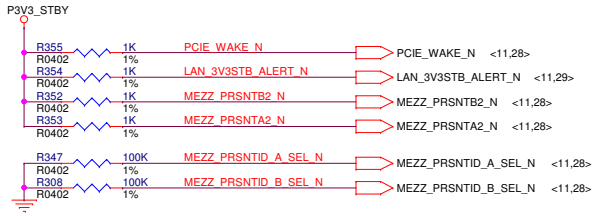
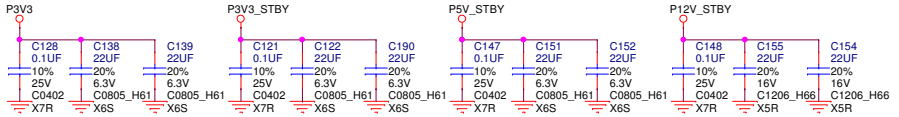
	10	9	8	7	6	5	4	3	2	1
P	No Pin		No Pin		No Pin		No Pin		No Pin	
O	PE_SLOT1_0_RX1_N	GND	KR_SLOT2_TX0_N	GND	PE_SLOT2_0_TX0_N	GND	PE_SLOT4_0_TX1_P	GND	PE_SLOT3_0_TX0_P	GND
N	PE_SLOT1_0_RX1_P	PE_SLOT1_0_TX0_N	KR_SLOT2_TX0_P	PE_SLOT2_0_TX1_N	PE_SLOT2_0_TX0_P	PE_SLOT4_0_TX0_P	PE_SLOT4_0_TX1_N	KR_SLOT4_TX0_P	PE_SLOT3_0_TX0_N	PE_SLOT3_0_RX1_P
M	GND	PE_SLOT1_0_TX0_P	GND	PE_SLOT2_0_TX1_P	GND	PE_SLOT4_0_TX0_N	GND	KR_SLOT4_TX0_N	GND	PE_SLOT3_0_RX1_N
L	PE_SLOT1_0_TX1_N	GND	KR_SLOT2_RX0_N	GND	PE_SLOT2_0_RX0_N	GND	PE_SLOT4_0_RX1_P	GND	PE_SLOT3_0_RX0_P	GND
K	PE_SLOT1_0_TX1_P	PE_SLOT1_0_RX0_N	KR_SLOT2_RX0_P	PE_SLOT2_0_RX1_N	PE_SLOT2_0_RX0_P	PE_SLOT4_0_RX0_N	PE_SLOT4_0_RX1_N	KR_SLOT4_RX0_P	PE_SLOT3_0_RX0_N	PE_SLOT3_0_TX1_P
J	GND	PE_SLOT1_0_RX0_P	GND	PE_SLOT2_0_RX1_P	GND	PE_SLOT4_0_RX0_P	GND	KR_SLOT4_RX0_N	GND	PE_SLOT3_0_TX1_N
I	KR_SLOT1_RX0_P	GND	MEZZ_PRSNTID_A_SEL_N	GND	SMB_MEZZ_NIC_DAT_MDIO	GND	CLK_PE_SLOT2_0_REFCLK_P	GND	CLK_PE_SLOT3_0_REFCLK_P	GND
H	KR_SLOT1_RX0_N	P3V3_STBY	MEZZ_PRSNTID_B_SEL_N	MEZZ_PRSNTA2_N	SMB_MEZZ_NIC_CLK_MDC	CLK_PE_SLOT1_0_REFCLK_P	CLK_PE_SLOT2_0_REFCLK_N	CLK_PE_SLOT4_0_REFCLK_P	CLK_PE_SLOT3_0_REFCLK_N	KR_SLOT3_RX0_P
G	GND	P3V3_STBY	GND	MEZZ_PRSNTB2_N	GND	CLK_PE_SLOT1_0_REFCLK_N	GND	CLK_PE_SLOT4_0_REFCLK_N	GND	KR_SLOT3_RX0_N
F	KR_SLOT1_TX0_P	GND	P3V3_STBY	GND	LAN_3V3STB_ALERT_N	GND	P12V_STBY	GND	BMC_NCSI_RMII_TX_EN	GND
E	KR_SLOT1_TX0_N	P3V3	P3V3	P5V_STBY	PCIE_WAKE_N	**RST_N2_N**	P12V_STBY	P12V_STBY	REFCLK_50MHz_RMII_MEZZ	KR_SLOT3_TX0_P
D	GND	P3V3	GND	P5V_STBY	GND	**RST_N1_N**	GND	P12V_STBY	GND	KR_SLOT3_TX0_N
C	P3V3	GND	P3V3	GND	SMB_MEZZ_SMDATA	GND	P12V_STBY	GND	BMC_NCSI_RMII_CSR_DV_R	GND
B	P3V3	P3V3	P3V3	P5V_STBY	SMB_MEZZ_SMCLK	**RST_N4_N**	P12V_STBY	BMC_NCSI_RMII_TXD_1	BMC_NCSI_RMII_RX_ER	BMC_NCSI_RMII_RXD_1_R
A	P3V3	P3V3	P3V3	P5V_STBY	GND	**RST_N3_N**	P12V_STBY	BMC_NCSI_RMII_TXD_0	GND	BMC_NCSI_RMII_RXD_0_R

Adapter Board CONN Pin mapping

Vertical Air Max conn: FCI# 10127982-102LF







Adapter Board CONN

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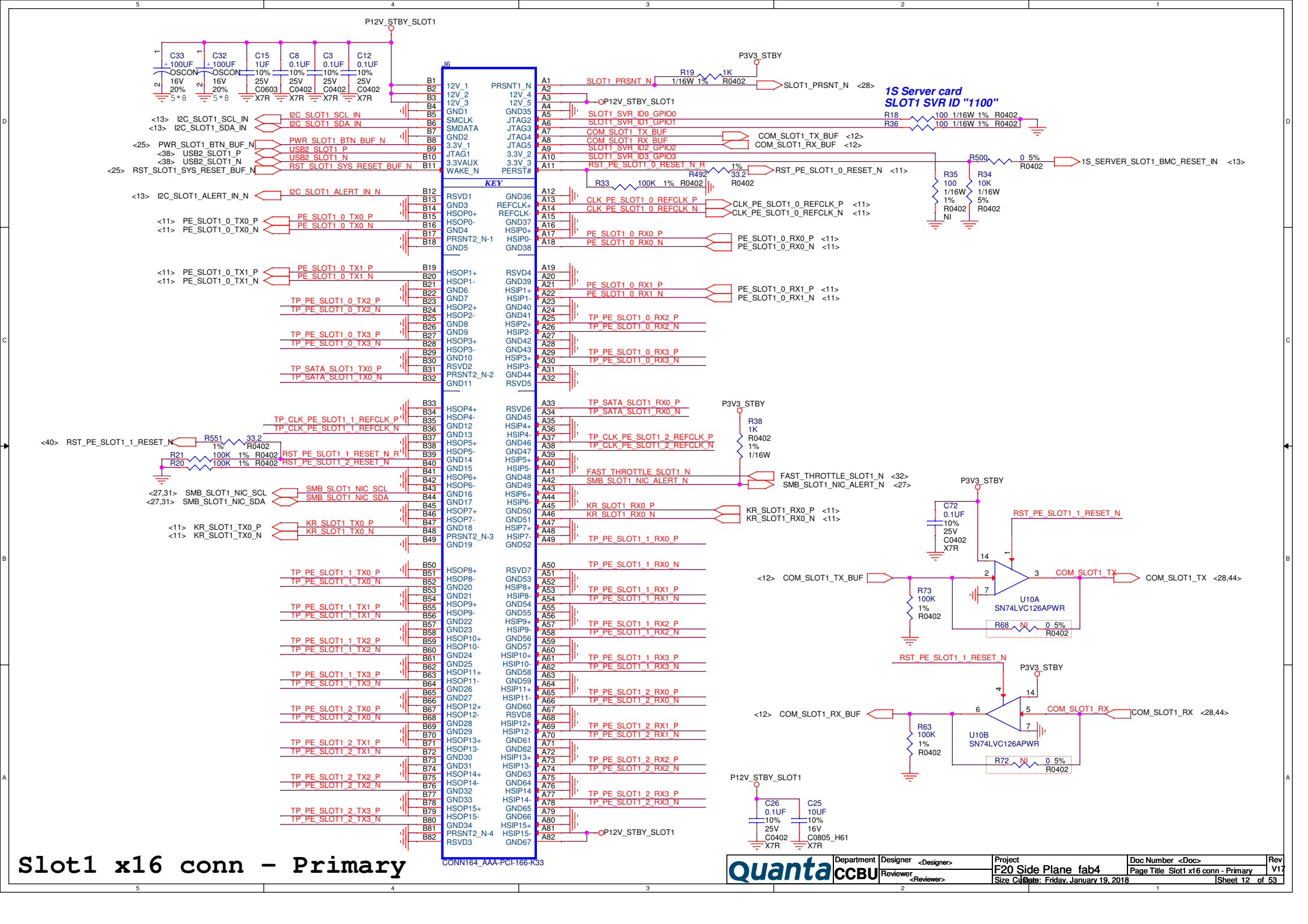
P12V_STBY_SLOT1
C33 100UF OSCON 16V 20% 5*8
C32 100UF OSCON 16V 20% 5*8
C15 1UF 10% 25V C0603 X7R
C8 0.1UF 10% 25V C0402 X7R
C3 0.1UF 10% 25V C0402 X7R
C12 0.1UF 10% 25V C0402 X7R
J6
CONN164_AAA-PCI-166-K33
KEY
P3V3_STBY
R19 1K 1/16W 1% R0402
SLOT1_PRSNT_N
SLOT1_PRSNT_N <28>
1S Server card
SLOT1 SVR ID "1100"
R18 100 1/16W 1% R0402
R36 100 1/16W 1% R0402
SLOT1_SVR_ID0_GPIO0
SLOT1_SVR_ID1_GPIO1
SLOT1_SVR_ID2_GPIO2
SLOT1_SVR_ID3_GPIO3
COM_SLOT1_TX_BUF
COM_SLOT1_RX_BUF
R500 0 5% R0402
1S_SERVER_SLOT1_BMC_RESET_IN <13>
RST_PE_SLOT1_0_RESET_N <11>
R492 33.2 1% R0402
R33 100K 1% R0402
R35 100 1/16W 1% R0402 NI
R34 10K 1/16W 5% R0402
I2C_SLOT1_SCL_IN
I2C_SLOT1_SDA_IN
PWR_SLOT1_BTN_BUF_N
USB2_SLOT1_P
USB2_SLOT1_N
RST_SLOT1_SYS_RESET_BUF_N
I2C_SLOT1_ALERT_IN_N
PE_SLOT1_0_TX0_P
PE_SLOT1_0_TX0_N
PE_SLOT1_0_RX0_P
PE_SLOT1_0_RX0_N
PE_SLOT1_0_TX1_P
PE_SLOT1_0_TX1_N
PE_SLOT1_0_RX1_P
PE_SLOT1_0_RX1_N
TP_PE_SLOT1_0_TX2_P
TP_PE_SLOT1_0_TX2_N
TP_PE_SLOT1_0_RX2_P
TP_PE_SLOT1_0_RX2_N
TP_PE_SLOT1_0_TX3_P
TP_PE_SLOT1_0_TX3_N
TP_PE_SLOT1_0_RX3_P
TP_PE_SLOT1_0_RX3_N
TP_SATA_SLOT1_TX0_P
TP_SATA_SLOT1_TX0_N
TP_SATA_SLOT1_RX0_P
TP_SATA_SLOT1_RX0_N
TP_CLK_PE_SLOT1_1_REFCLK_P
TP_CLK_PE_SLOT1_1_REFCLK_N
TP_CLK_PE_SLOT1_2_REFCLK_P
TP_CLK_PE_SLOT1_2_REFCLK_N
RST_PE_SLOT1_1_RESET_N
R551 33.2 1% R0402
R21 100K 1% R0402
R20 100K 1% R0402
RST_PE_SLOT1_1_RESET_N_R
RST_PE_SLOT1_2_RESET_N
SMB_SLOT1_NIC_SCL
SMB_SLOT1_NIC_SDA
SMB_SLOT1_NIC_ALERT_N
FAST_THROTTLE_SLOT1_N
R38 1K R0402 1% 1/16W
KR_SLOT1_TX0_P
KR_SLOT1_TX0_N
KR_SLOT1_RX0_P
KR_SLOT1_RX0_N
TP_PE_SLOT1_1_TX0_P
TP_PE_SLOT1_1_TX0_N
TP_PE_SLOT1_1_RX0_P
TP_PE_SLOT1_1_RX0_N
TP_PE_SLOT1_1_TX1_P
TP_PE_SLOT1_1_TX1_N
TP_PE_SLOT1_1_RX1_P
TP_PE_SLOT1_1_RX1_N
TP_PE_SLOT1_1_TX2_P
TP_PE_SLOT1_1_TX2_N
TP_PE_SLOT1_1_RX2_P
TP_PE_SLOT1_1_RX2_N
TP_PE_SLOT1_1_TX3_P
TP_PE_SLOT1_1_TX3_N
TP_PE_SLOT1_1_RX3_P
TP_PE_SLOT1_1_RX3_N
TP_PE_SLOT1_2_TX0_P
TP_PE_SLOT1_2_TX0_N
TP_PE_SLOT1_2_RX0_P
TP_PE_SLOT1_2_RX0_N
TP_PE_SLOT1_2_TX1_P
TP_PE_SLOT1_2_TX1_N
TP_PE_SLOT1_2_RX1_P
TP_PE_SLOT1_2_RX1_N
TP_PE_SLOT1_2_TX2_P
TP_PE_SLOT1_2_TX2_N
TP_PE_SLOT1_2_RX2_P
TP_PE_SLOT1_2_RX2_N
TP_PE_SLOT1_2_TX3_P
TP_PE_SLOT1_2_TX3_N
TP_PE_SLOT1_2_RX3_P
TP_PE_SLOT1_2_RX3_N
P12V_STBY_SLOT1
C72 0.1UF 10% 25V C0402 X7R
C26 0.1UF 10% 25V C0402 X7R
C25 10UF 10% 16V C0805_H61 X7R
R73 100K 1% R0402
R63 100K 1% R0402
U10A SN74LVC126APWR
U10B SN74LVC126APWR
R68 NI 0 5% R0402
R72 NI 0 5% R0402
COM_SLOT1_TX
COM_SLOT1_RX
Slot1 x16 conn – Primary
Quanta
Department CCBU
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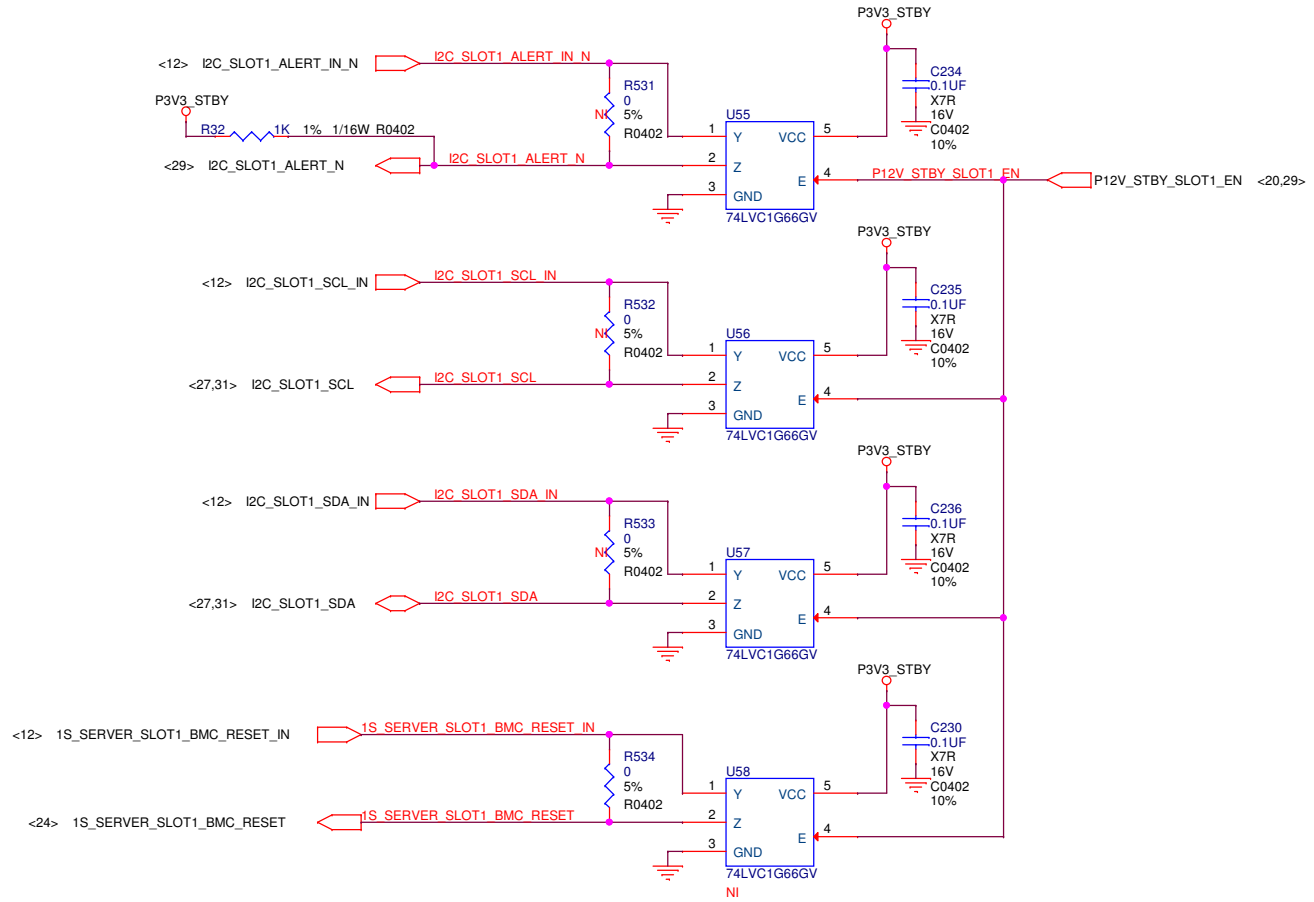

Slot1 Bilateral switch

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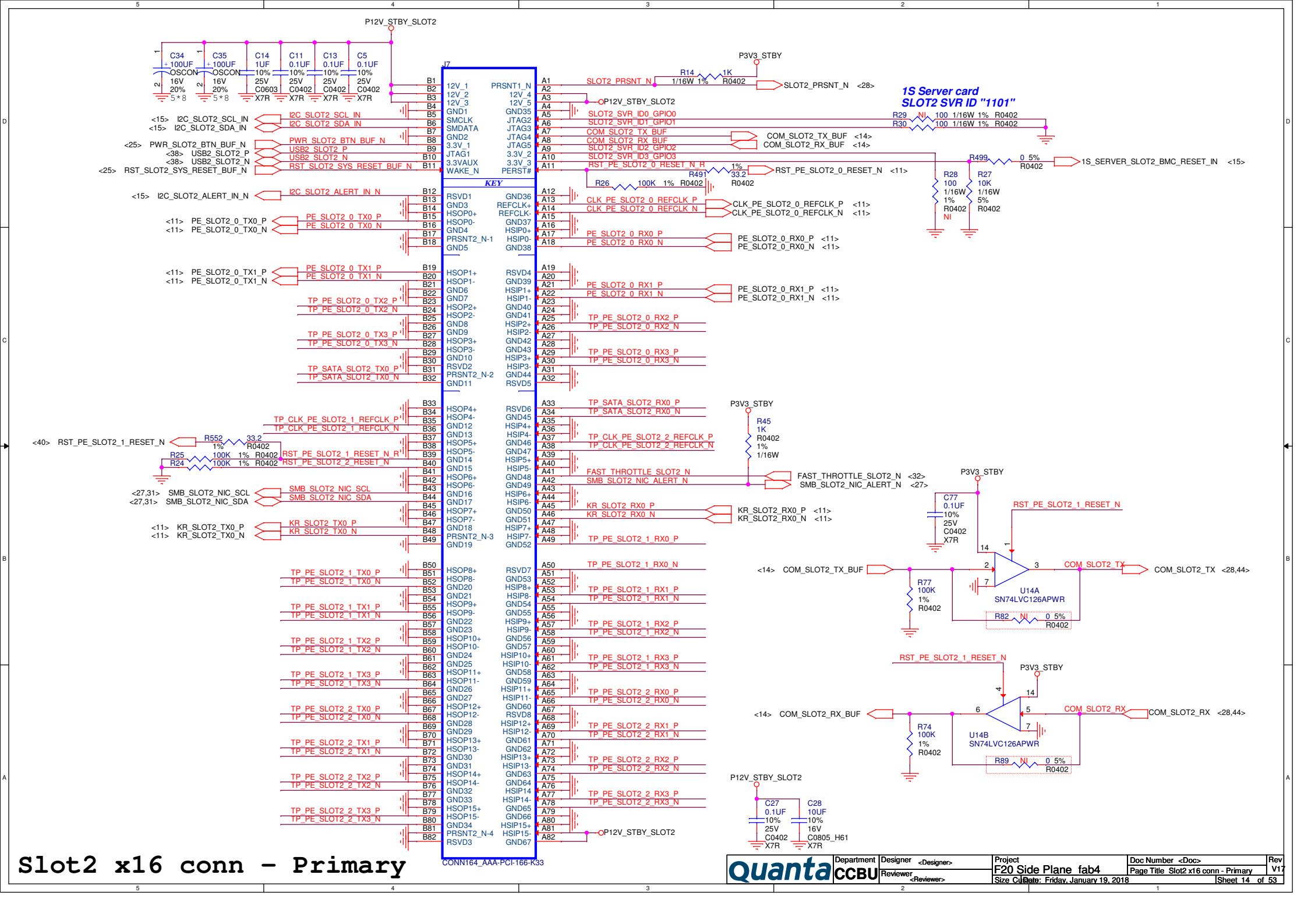
P12V_STBY_SLOT2
C34 100UF OSCON 16V 20% 5*8
C35 100UF OSCON 16V 20% 5*8
C14 1UF 10% 25V C0603 X7R
C11 0.1UF 10% 25V C0402 X7R
C13 0.1UF 10% 25V C0402 X7R
C5 0.1UF 10% 25V C0402 X7R
J7
CONN164_AAA-PCI-166-K33
KEY
P3V3_STBY
R14 1K 1/16W 1% R0402
SLOT2_PRSNT_N
SLOT2_PRSNT_N <28>
1S Server card
SLOT2 SVR ID "1101"
R29 NI 100 1/16W 1% R0402
R30 100 1/16W 1% R0402
SLOT2_SVR_ID0_GPIO0
SLOT2_SVR_ID1_GPIO1
SLOT2_SVR_ID2_GPIO2
SLOT2_SVR_ID3_GPIO3
COM_SLOT2_TX_BUF
COM_SLOT2_RX_BUF
R499 0 5% R0402
1S_SERVER_SLOT2_BMC_RESET_IN <15>
RST_PE_SLOT2_0_RESET_N <11>
R491 33.2 1% R0402
R26 100K 1% R0402
R28 100 1/16W 1% R0402 NI
R27 10K 1/16W 5% R0402
I2C_SLOT2_SCL_IN
I2C_SLOT2_SDA_IN
I2C_SLOT2_ALERT_IN_N
PWR_SLOT2_BTN_BUF_N
USB2_SLOT2_P
USB2_SLOT2_N
RST_SLOT2_SYS_RESET_BUF_N
PE_SLOT2_0_TX0_P
PE_SLOT2_0_TX0_N
PE_SLOT2_0_TX1_P
PE_SLOT2_0_TX1_N
TP_PE_SLOT2_0_TX2_P
TP_PE_SLOT2_0_TX2_N
TP_PE_SLOT2_0_TX3_P
TP_PE_SLOT2_0_TX3_N
TP_SATA_SLOT2_TX0_P
TP_SATA_SLOT2_TX0_N
CLK_PE_SLOT2_0_REFCLK_P
CLK_PE_SLOT2_0_REFCLK_N
PE_SLOT2_0_RX0_P
PE_SLOT2_0_RX0_N
PE_SLOT2_0_RX1_P
PE_SLOT2_0_RX1_N
TP_PE_SLOT2_0_RX2_P
TP_PE_SLOT2_0_RX2_N
TP_PE_SLOT2_0_RX3_P
TP_PE_SLOT2_0_RX3_N
TP_SATA_SLOT2_RX0_P
TP_SATA_SLOT2_RX0_N
TP_CLK_PE_SLOT2_1_REFCLK_P
TP_CLK_PE_SLOT2_1_REFCLK_N
TP_CLK_PE_SLOT2_2_REFCLK_P
TP_CLK_PE_SLOT2_2_REFCLK_N
RST_PE_SLOT2_1_RESET_N
R552 33.2 1% R0402
R25 100K 1% R0402
R24 100K 1% R0402
RST_PE_SLOT2_1_RESET_N_R
RST_PE_SLOT2_2_RESET_N
R45 1K R0402 1% 1/16W
FAST_THROTTLE_SLOT2_N
SMB_SLOT2_NIC_ALERT_N
SMB_SLOT2_NIC_SCL
SMB_SLOT2_NIC_SDA
KR_SLOT2_RX0_P
KR_SLOT2_RX0_N
KR_SLOT2_TX0_P
KR_SLOT2_TX0_N
TP_PE_SLOT2_1_RX0_P
TP_PE_SLOT2_1_RX0_N
TP_PE_SLOT2_1_TX0_P
TP_PE_SLOT2_1_TX0_N
TP_PE_SLOT2_1_RX1_P
TP_PE_SLOT2_1_RX1_N
TP_PE_SLOT2_1_TX1_P
TP_PE_SLOT2_1_TX1_N
TP_PE_SLOT2_1_RX2_P
TP_PE_SLOT2_1_RX2_N
TP_PE_SLOT2_1_TX2_P
TP_PE_SLOT2_1_TX2_N
TP_PE_SLOT2_1_RX3_P
TP_PE_SLOT2_1_RX3_N
TP_PE_SLOT2_1_TX3_P
TP_PE_SLOT2_1_TX3_N
TP_PE_SLOT2_2_RX0_P
TP_PE_SLOT2_2_RX0_N
TP_PE_SLOT2_2_TX0_P
TP_PE_SLOT2_2_TX0_N
TP_PE_SLOT2_2_RX1_P
TP_PE_SLOT2_2_RX1_N
TP_PE_SLOT2_2_TX1_P
TP_PE_SLOT2_2_TX1_N
TP_PE_SLOT2_2_RX2_P
TP_PE_SLOT2_2_RX2_N
TP_PE_SLOT2_2_TX2_P
TP_PE_SLOT2_2_TX2_N
TP_PE_SLOT2_2_RX3_P
TP_PE_SLOT2_2_RX3_N
TP_PE_SLOT2_2_TX3_P
TP_PE_SLOT2_2_TX3_N
P12V_STBY_SLOT2
C77 0.1UF 10% 25V C0402 X7R
C27 0.1UF 10% 25V C0402 X7R
C28 10UF 10% 16V C0805_H61 X7R
R77 100K 1% R0402
R74 100K 1% R0402
U14A SN74LVC126APWR
U14B SN74LVC126APWR
R82 NI 0 5% R0402
R89 NI 0 5% R0402
COM_SLOT2_TX
COM_SLOT2_RX
COM_SLOT2_TX <28,44>
COM_SLOT2_RX <28,44>
Slot2 x16 conn - Primary
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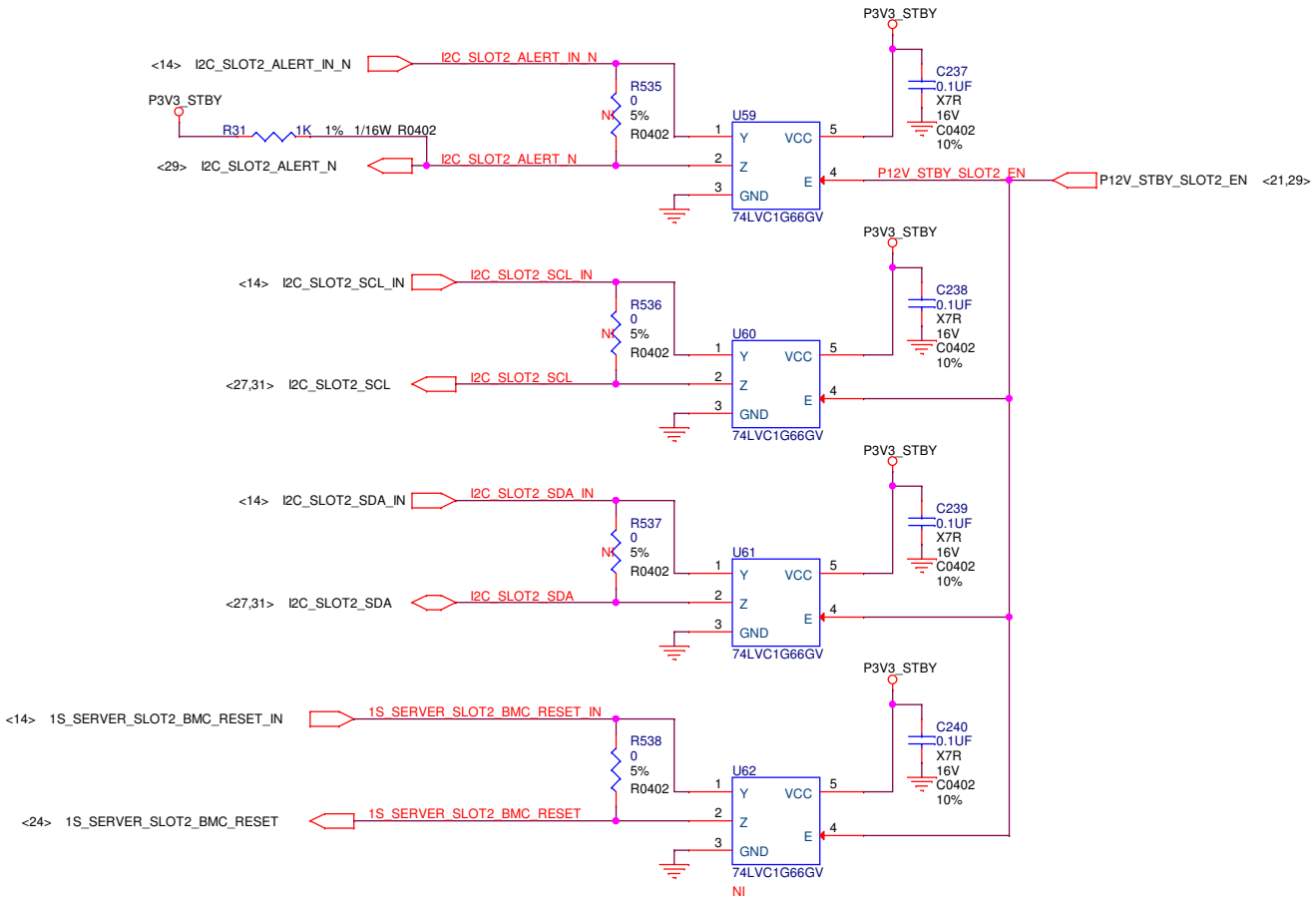

Slot2 x16 conn - Extension

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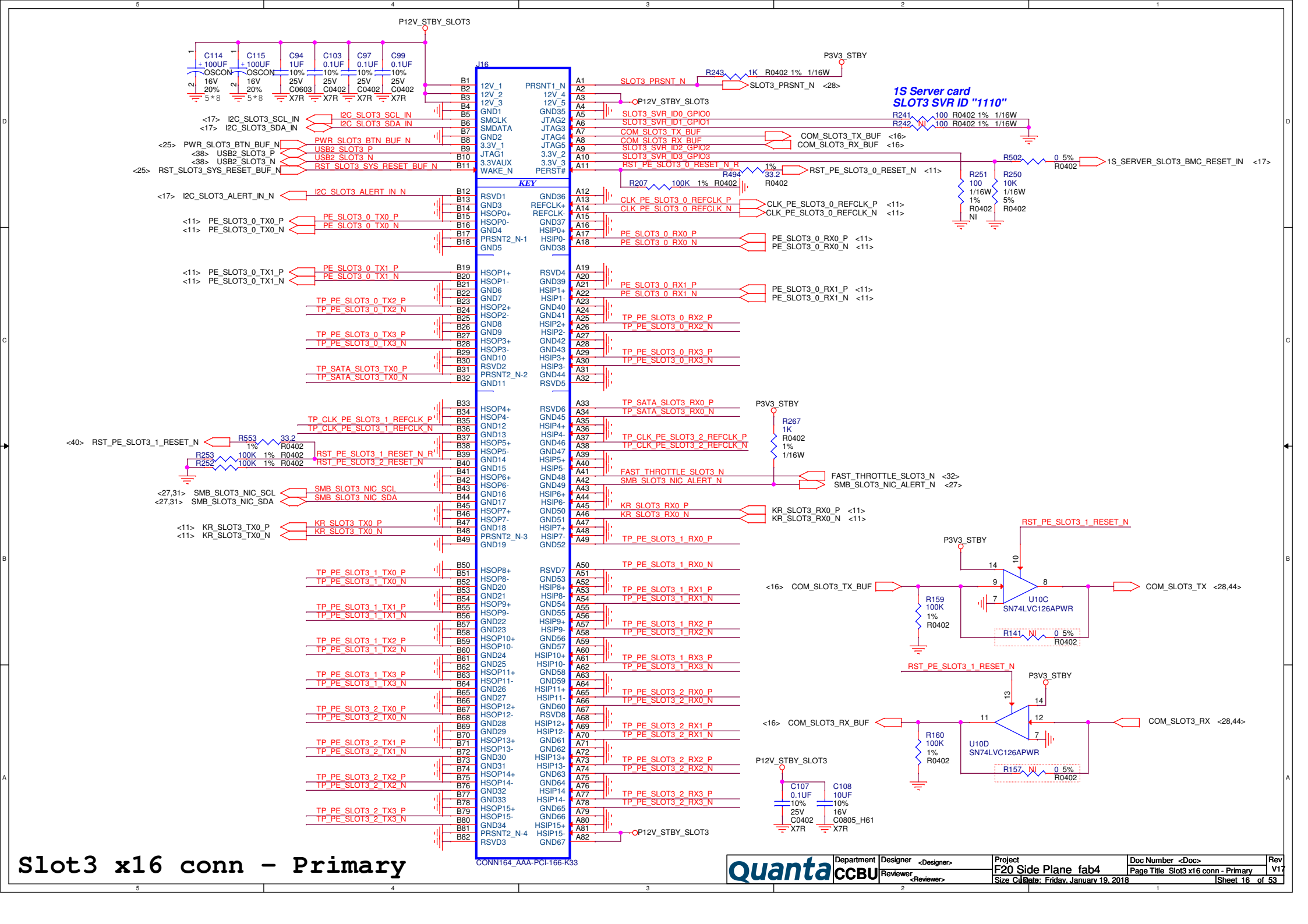

Slot3 x16 conn - Primary

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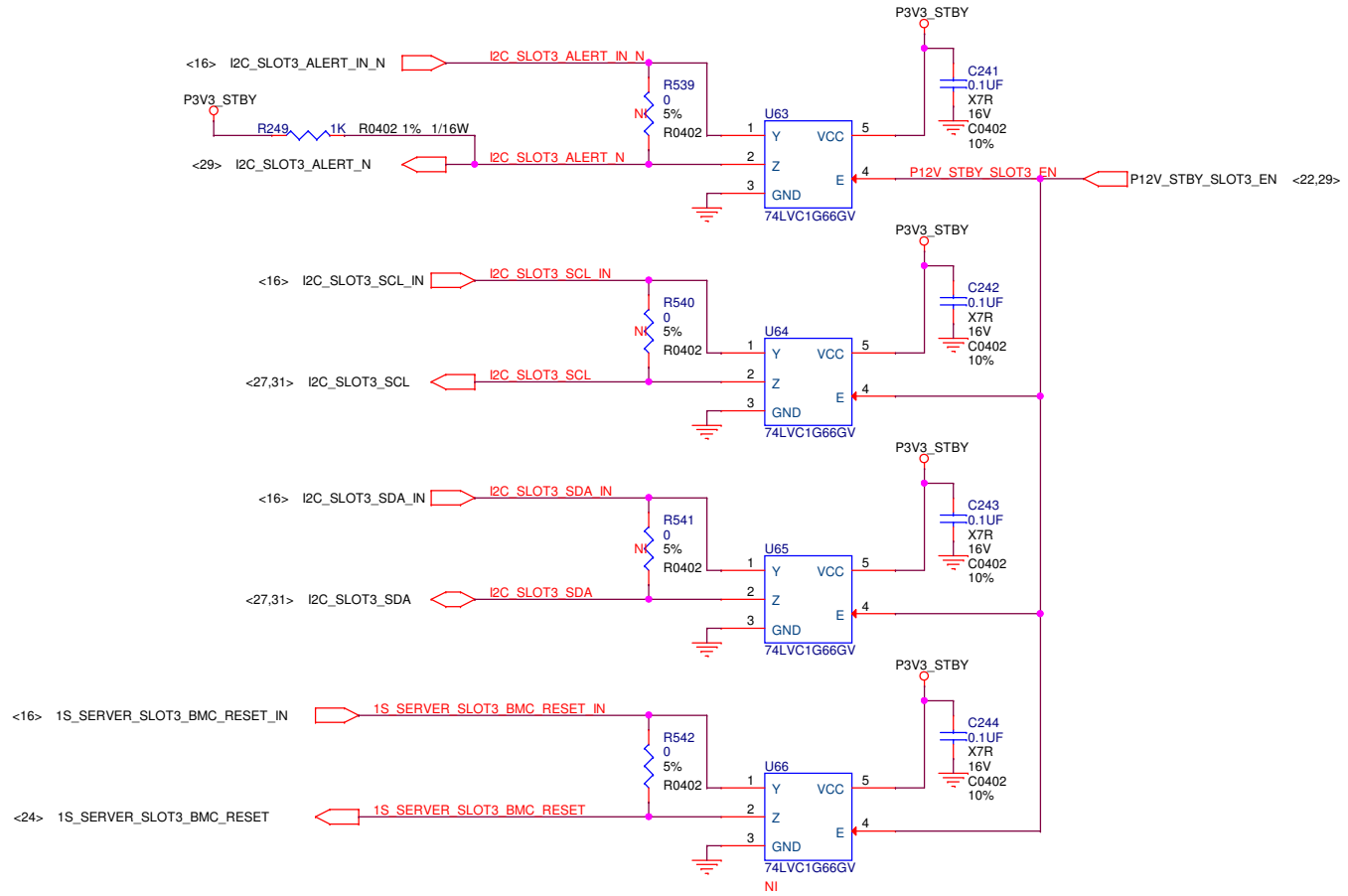
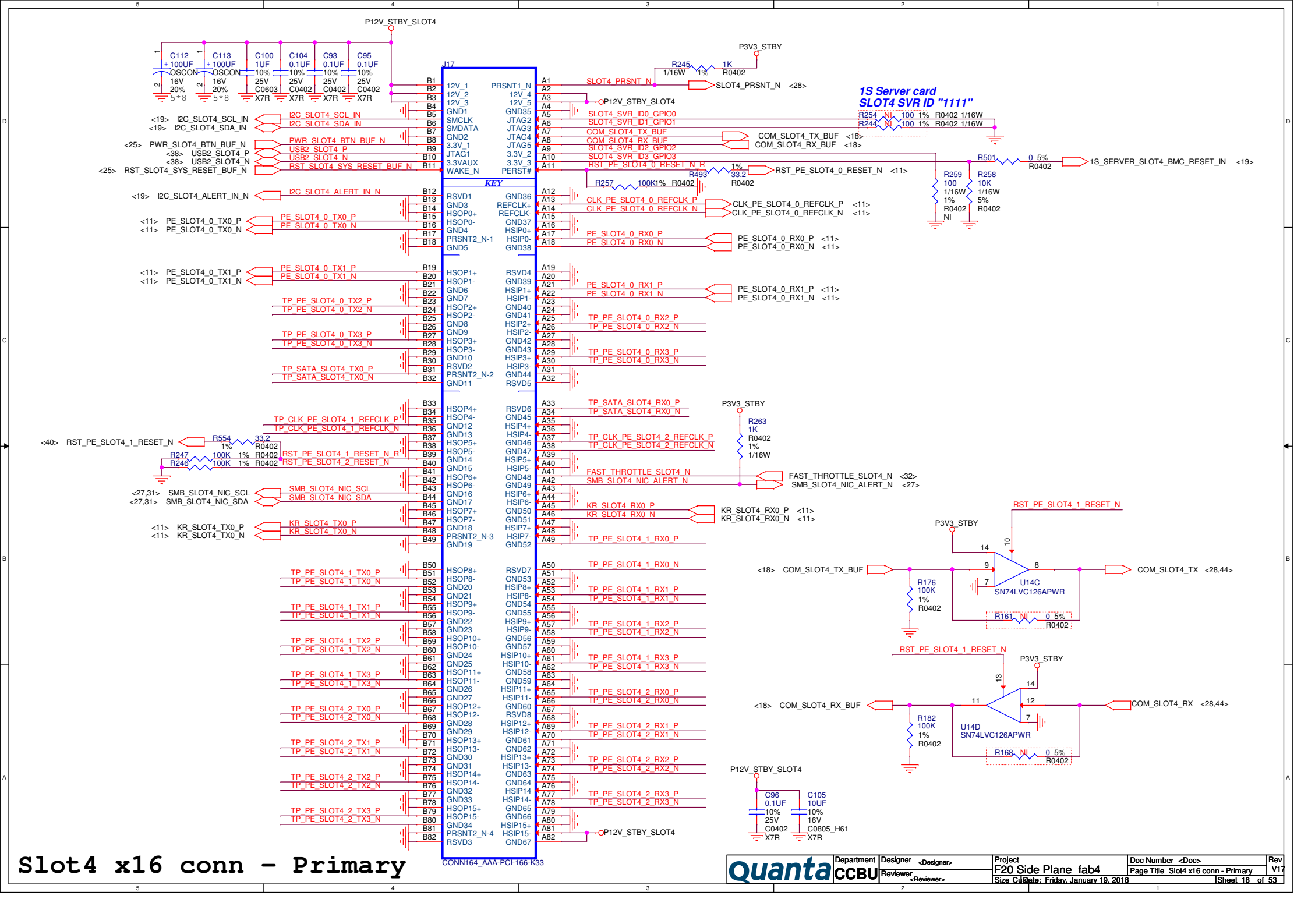


Slot3 x16 conn - Extension

Quanta	Department CCBU	Designer <Designer>	Project F20 Side Plane fab4	Doc Number <Doc>	Rev V17
		Reviewer <Reviewer>		Page Title Slot3 x16 conn - Extension	
			Size Custom Date: Friday, January 19, 2018	Sheet 17 of 53	


P12V_STBY_SLOT4
C112 100UF OSCON 16V 20% 5*8
C113 100UF OSCON 16V 20% 5*8
C100 1UF 10% 25V C0603 X7R
C104 0.1UF 10% 25V C0402 X7R
C93 0.1UF 10% 25V C0402 X7R
C95 0.1UF 10% 25V C0402 X7R
J17
CONN164_AAA-PCI-166-K33
KEY
P3V3_STBY
R245 1K 1/16W 1% R0402
SLOT4_PRSNT_N
SLOT4_PRSNT_N <28>
1S Server card
SLOT4 SVR ID "1111"
R254 NI 100 1% R0402 1/16W
R244 NI 100 1% R0402 1/16W
SLOT4_SVR_ID0_GPIO0
SLOT4_SVR_ID1_GPIO1
SLOT4_SVR_ID2_GPIO2
SLOT4_SVR_ID3_GPIO3
COM_SLOT4_TX_BUF
COM_SLOT4_RX_BUF
COM_SLOT4_TX_BUF <18>
COM_SLOT4_RX_BUF <18>
R501 0 5% R0402
1S_SERVER_SLOT4_BMC_RESET_IN <19>
R259 100 1/16W 1% R0402 NI
R258 10K 1/16W 5% R0402
R493 33.2 1% R0402
RST_PE_SLOT4_0_RESET_N <11>
RST_PE_SLOT4_0_RESET_N_R
R257 100K 1% R0402
CLK_PE_SLOT4_0_REFCLK_P
CLK_PE_SLOT4_0_REFCLK_N
CLK_PE_SLOT4_0_REFCLK_P <11>
CLK_PE_SLOT4_0_REFCLK_N <11>
PE_SLOT4_0_RX0_P
PE_SLOT4_0_RX0_N
PE_SLOT4_0_RX0_P <11>
PE_SLOT4_0_RX0_N <11>
PE_SLOT4_0_RX1_P
PE_SLOT4_0_RX1_N
PE_SLOT4_0_RX1_P <11>
PE_SLOT4_0_RX1_N <11>
TP_PE_SLOT4_0_RX2_P
TP_PE_SLOT4_0_RX2_N
TP_PE_SLOT4_0_RX3_P
TP_PE_SLOT4_0_RX3_N
TP_SATA_SLOT4_RX0_P
TP_SATA_SLOT4_RX0_N
P3V3_STBY
R263 1K R0402 1% 1/16W
TP_CLK_PE_SLOT4_2_REFCLK_P
TP_CLK_PE_SLOT4_2_REFCLK_N
FAST_THROTTLE_SLOT4_N
SMB_SLOT4_NIC_ALERT_N
FAST_THROTTLE_SLOT4_N <32>
SMB_SLOT4_NIC_ALERT_N <27>
KR_SLOT4_RX0_P
KR_SLOT4_RX0_N
KR_SLOT4_RX0_P <11>
KR_SLOT4_RX0_N <11>
TP_PE_SLOT4_1_RX0_P
TP_PE_SLOT4_1_RX0_N
TP_PE_SLOT4_1_RX1_P
TP_PE_SLOT4_1_RX1_N
TP_PE_SLOT4_1_RX2_P
TP_PE_SLOT4_1_RX2_N
TP_PE_SLOT4_1_RX3_P
TP_PE_SLOT4_1_RX3_N
TP_PE_SLOT4_2_RX0_P
TP_PE_SLOT4_2_RX0_N
TP_PE_SLOT4_2_RX1_P
TP_PE_SLOT4_2_RX1_N
TP_PE_SLOT4_2_RX2_P
TP_PE_SLOT4_2_RX2_N
TP_PE_SLOT4_2_RX3_P
TP_PE_SLOT4_2_RX3_N
P12V_STBY_SLOT4
C96 0.1UF 10% 25V C0402 X7R
C105 10UF 10% 16V C0805_H61 X7R
RST_PE_SLOT4_1_RESET_N
RST_PE_SLOT4_1_RESET_N_R
RST_PE_SLOT4_2_RESET_N
R554 33.2 1% R0402
R247 100K 1% R0402
R246 100K 1% R0402
U14C SN74LVC126APWR
R176 100K 1% R0402
R161 NI 0 5% R0402
COM_SLOT4_TX <28,44>
U14D SN74LVC126APWR
R182 100K 1% R0402
R168 NI 0 5% R0402
COM_SLOT4_RX <28,44>
SMB_SLOT4_NIC_SCL
SMB_SLOT4_NIC_SDA
I2C_SLOT4_SCL_IN
I2C_SLOT4_SDA_IN
I2C_SLOT4_ALERT_IN_N
PWR_SLOT4_BTN_BUF_N
USB2_SLOT4_P
USB2_SLOT4_N
RST_SLOT4_SYS_RESET_BUF_N
PE_SLOT4_0_TX0_P
PE_SLOT4_0_TX0_N
PE_SLOT4_0_TX1_P
PE_SLOT4_0_TX1_N
TP_PE_SLOT4_0_TX2_P
TP_PE_SLOT4_0_TX2_N
TP_PE_SLOT4_0_TX3_P
TP_PE_SLOT4_0_TX3_N
TP_SATA_SLOT4_TX0_P
TP_SATA_SLOT4_TX0_N
KR_SLOT4_TX0_P
KR_SLOT4_TX0_N
TP_CLK_PE_SLOT4_1_REFCLK_P
TP_CLK_PE_SLOT4_1_REFCLK_N
TP_PE_SLOT4_1_TX0_P
TP_PE_SLOT4_1_TX0_N
TP_PE_SLOT4_1_TX1_P
TP_PE_SLOT4_1_TX1_N
TP_PE_SLOT4_1_TX2_P
TP_PE_SLOT4_1_TX2_N
TP_PE_SLOT4_1_TX3_P
TP_PE_SLOT4_1_TX3_N
TP_PE_SLOT4_2_TX0_P
TP_PE_SLOT4_2_TX0_N
TP_PE_SLOT4_2_TX1_P
TP_PE_SLOT4_2_TX1_N
TP_PE_SLOT4_2_TX2_P
TP_PE_SLOT4_2_TX2_N
TP_PE_SLOT4_2_TX3_P
TP_PE_SLOT4_2_TX3_N
Slot4 x16 conn - Primary
Quanta
Department CCBU
Designer <Designer>
Reviewer <Reviewer>
Project F20 Side Plane fab4
Doc Number <Doc>
Page Title Slot4 x16 conn - Primary
Rev V17
Size C
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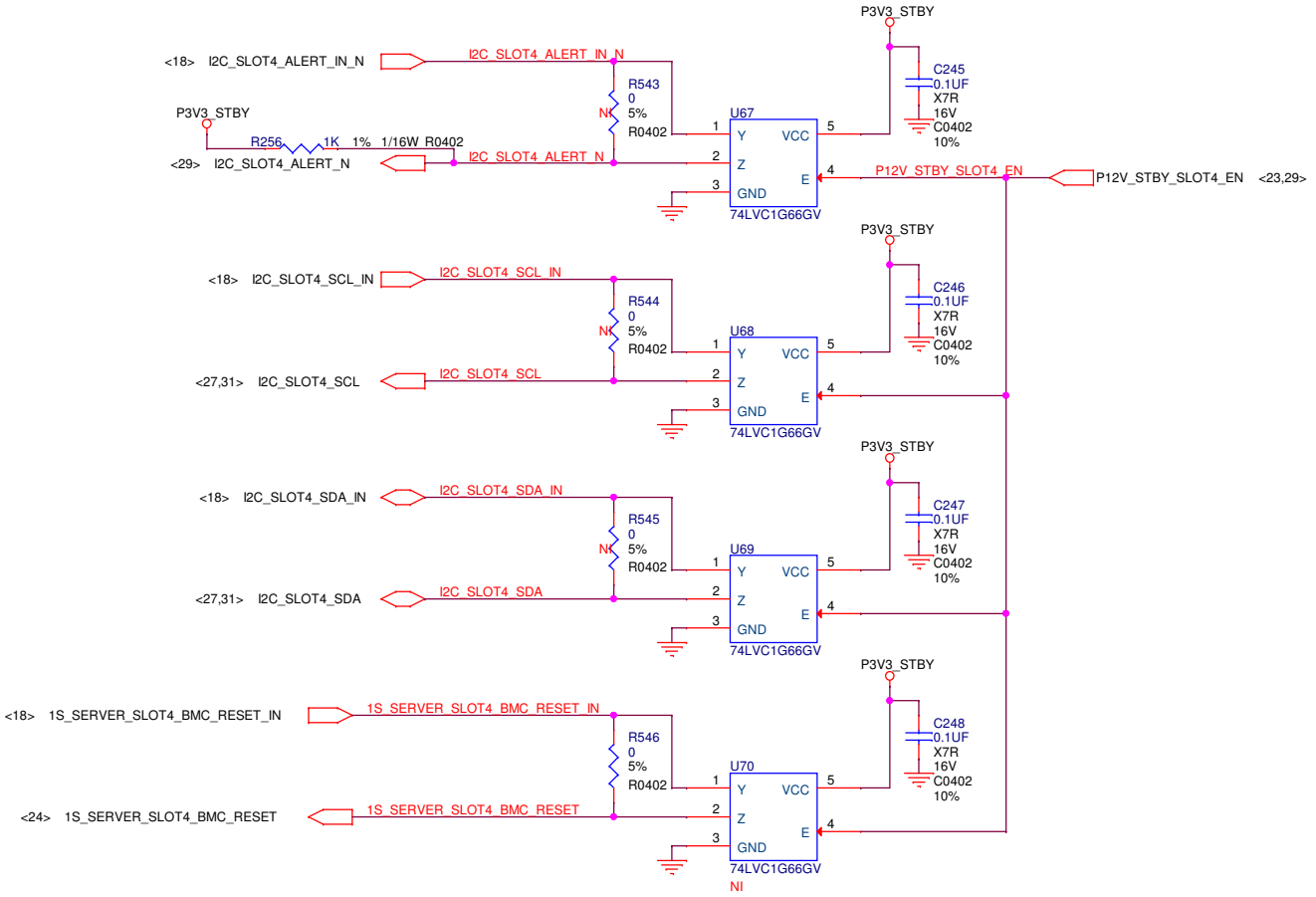
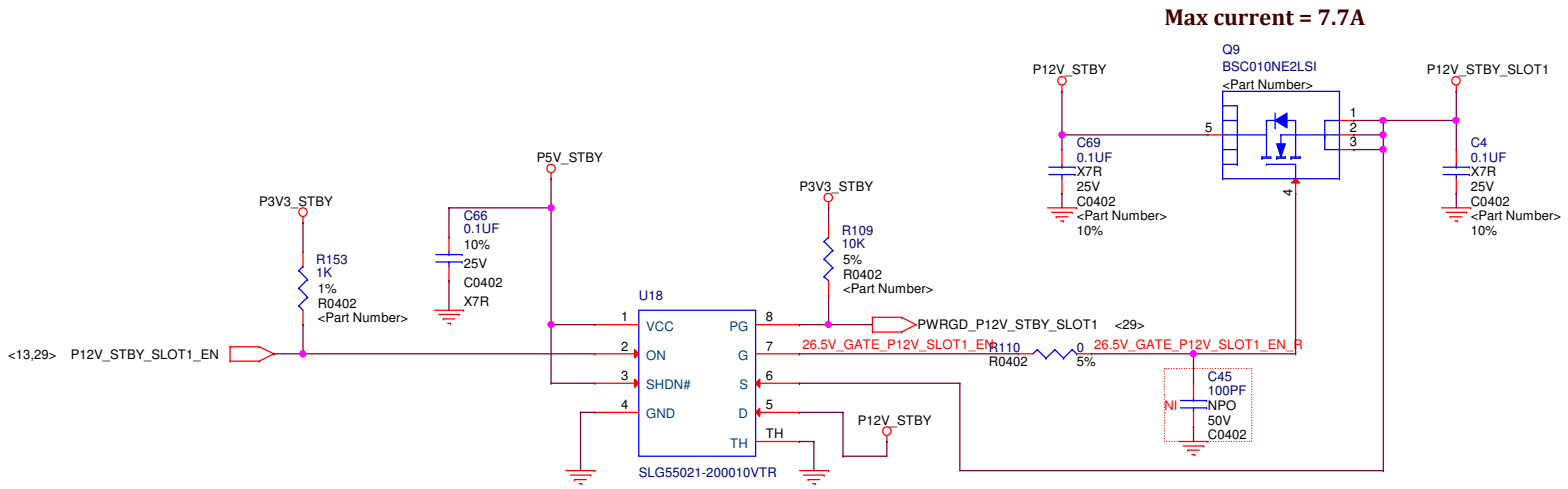


Slot4 x16 conn - Extension

Quanta	Department CCBU	Designer <Designer>	Project F20 Side Plane fab4	Doc Number <Doc>	Rev V17
		Reviewer <Reviewer>	Size Custom Date: Friday, January 19, 2018	Page Title Slot4 x16 conn - Extension	Sheet 19 of 53



Slot1 Power Switch

Quanta	Department CCBU	Designer <Designer>	Project F20 Side Plane fab4	Doc Number <Doc>
		Reviewer <Reviewer>	Size B Date: Friday, January 19, 2018	Page Title Slot1 Power Switch
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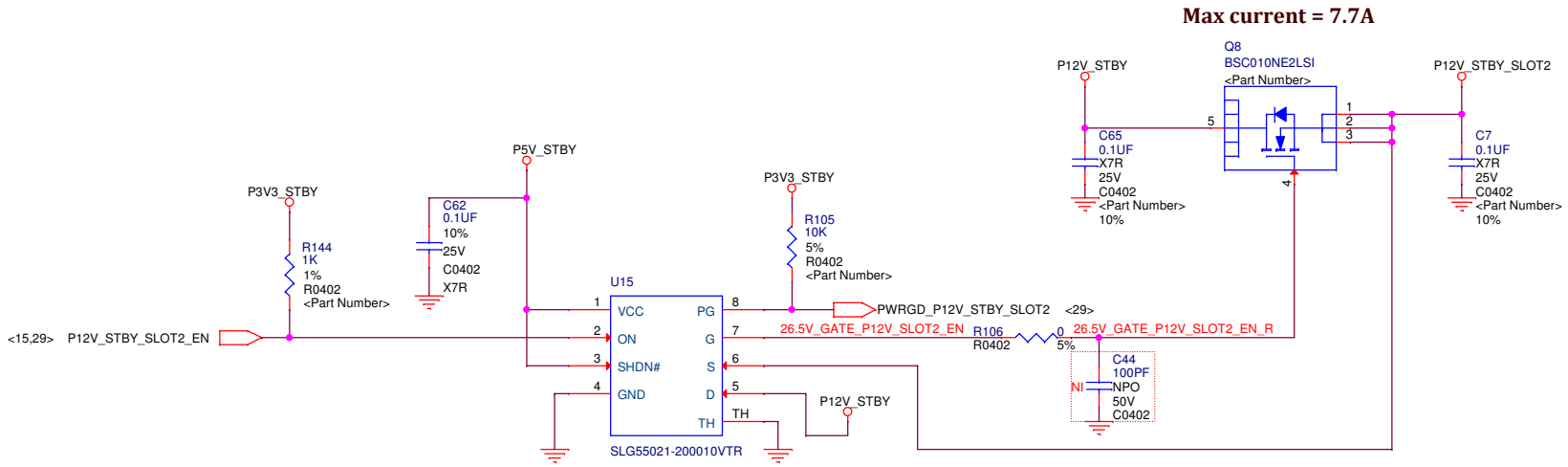
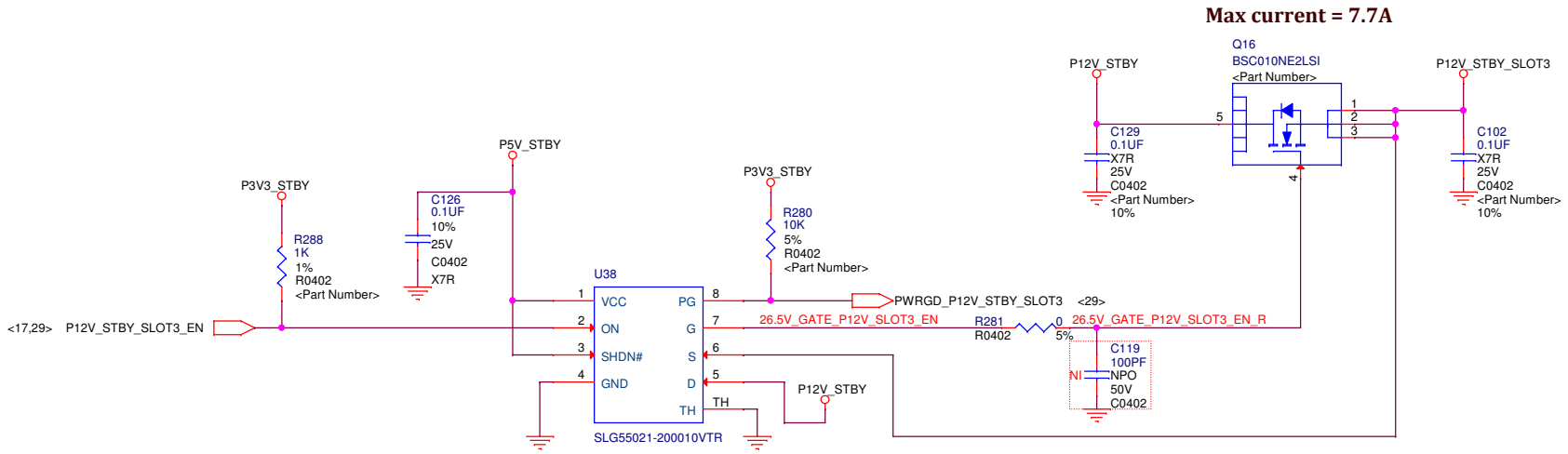


Slot2 Power Switch

Quanta	Department CCBU	Designer <Designer>	Project F20 Side Plane fab4	Doc Number <Doc> / Page Title Slot2 Power Switch / Rev V17
		Reviewer <Reviewer>	Size B Date: Friday, January 19, 2018	Sheet 21 of 53



Slot3 Power Switch

Quanta	Department CCBU	Designer <Designer>	Project F20 Side Plane fab4	Doc Number <Doc>
		Reviewer <Reviewer>	Size B Date: Friday, January 19, 2018	Page Title Slot3 Power Switch
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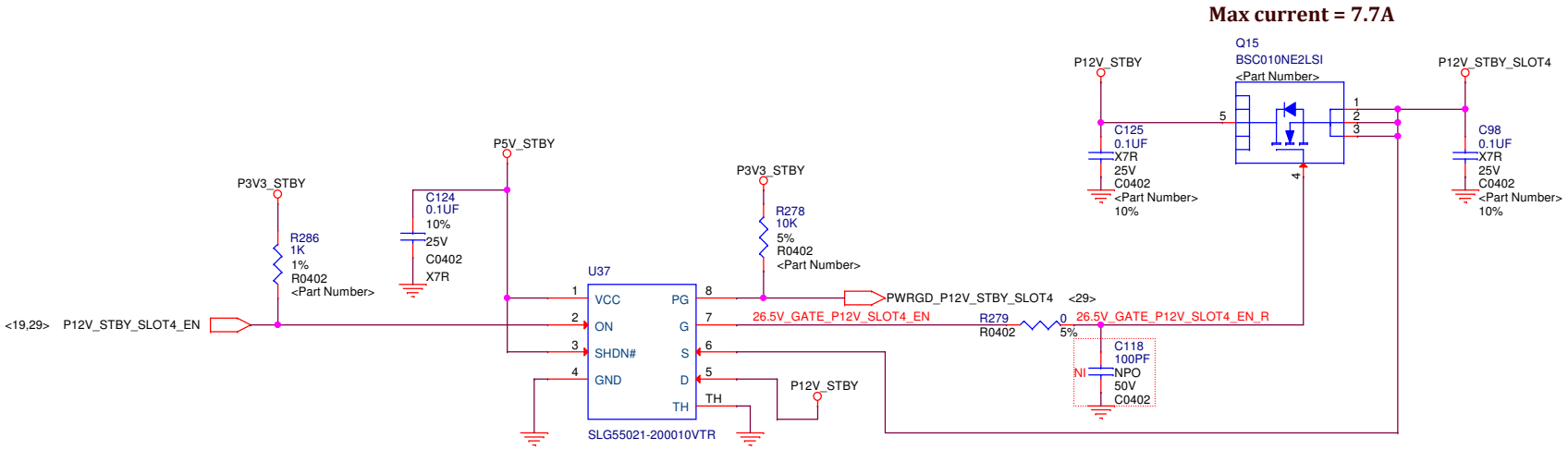
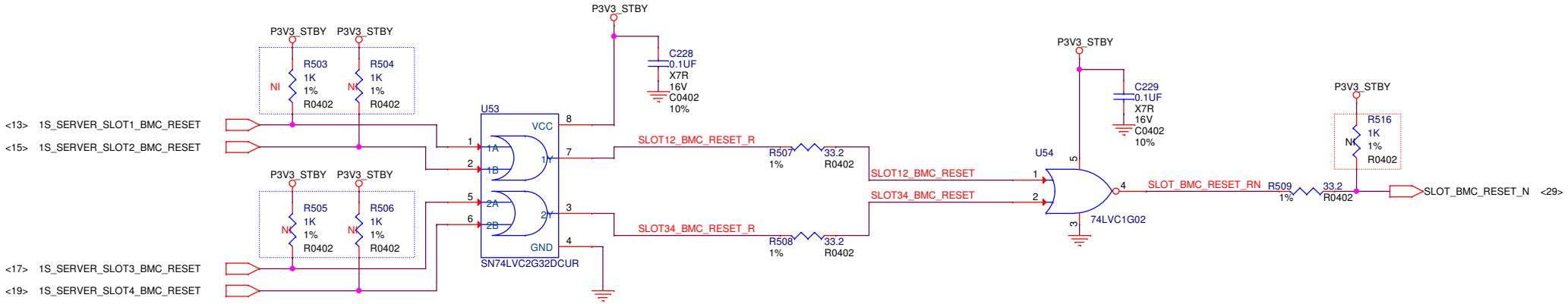


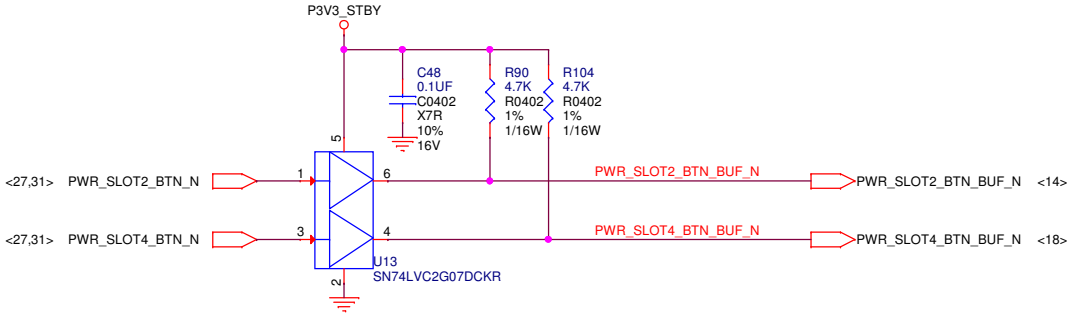
Slot4 Power Switch

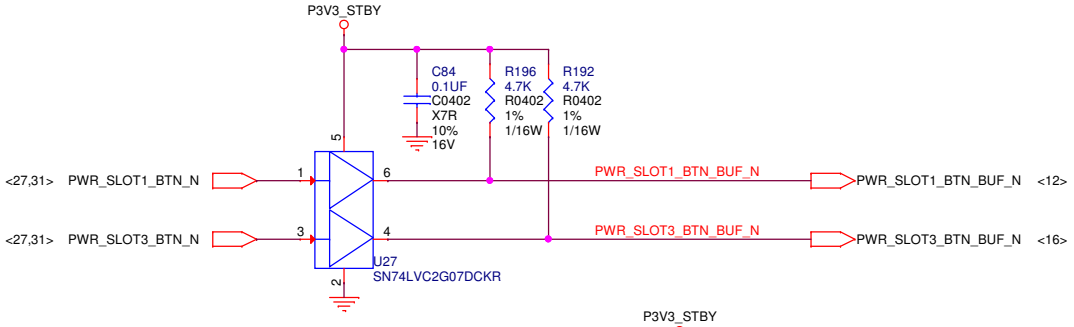
Quanta	Department CCBU	Designer <Designer>	Project F20 Side Plane fab4	Doc Number <Doc>	Rev V17
		Reviewer <Reviewer>	Size B Date: Friday, January 19, 2018	Page Title Slot4 Power Switch	Sheet 23 of 53

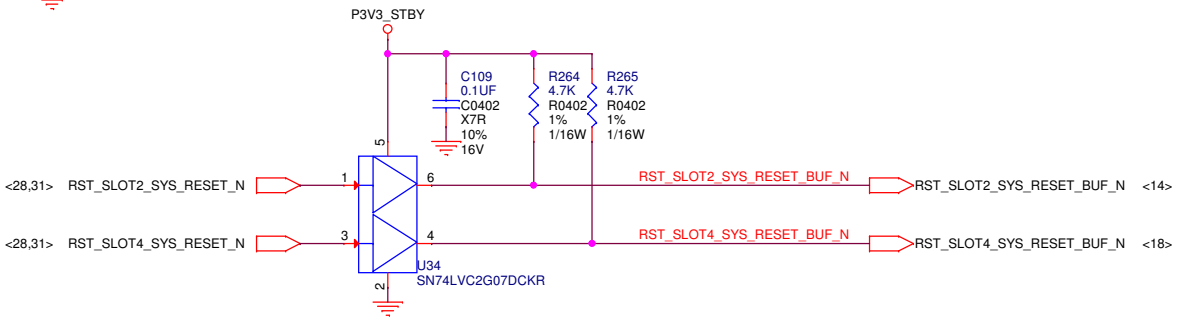


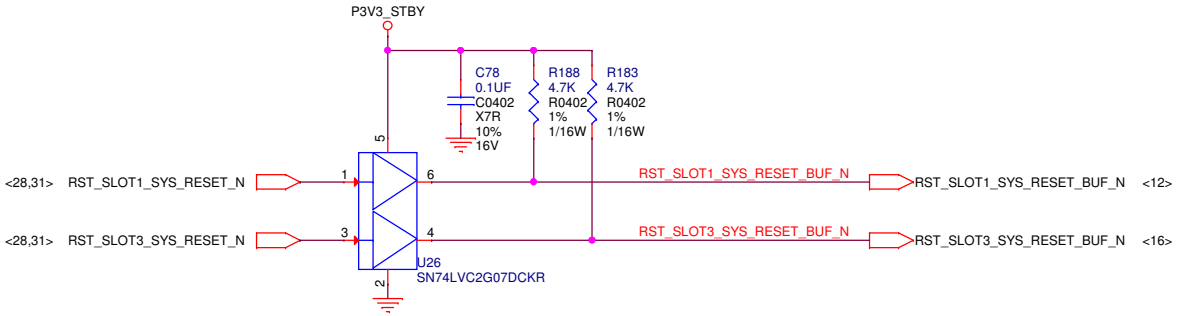
BMC RESET

Quanta	Department CCBU	Designer <Designer>	Project F20 Side Plane fab4	Doc Number <Doc>	Rev V17
		Reviewer <Reviewer>	Size B Date: Friday, January 19, 2018	Page Title BMC RESET	Sheet 24 of 53



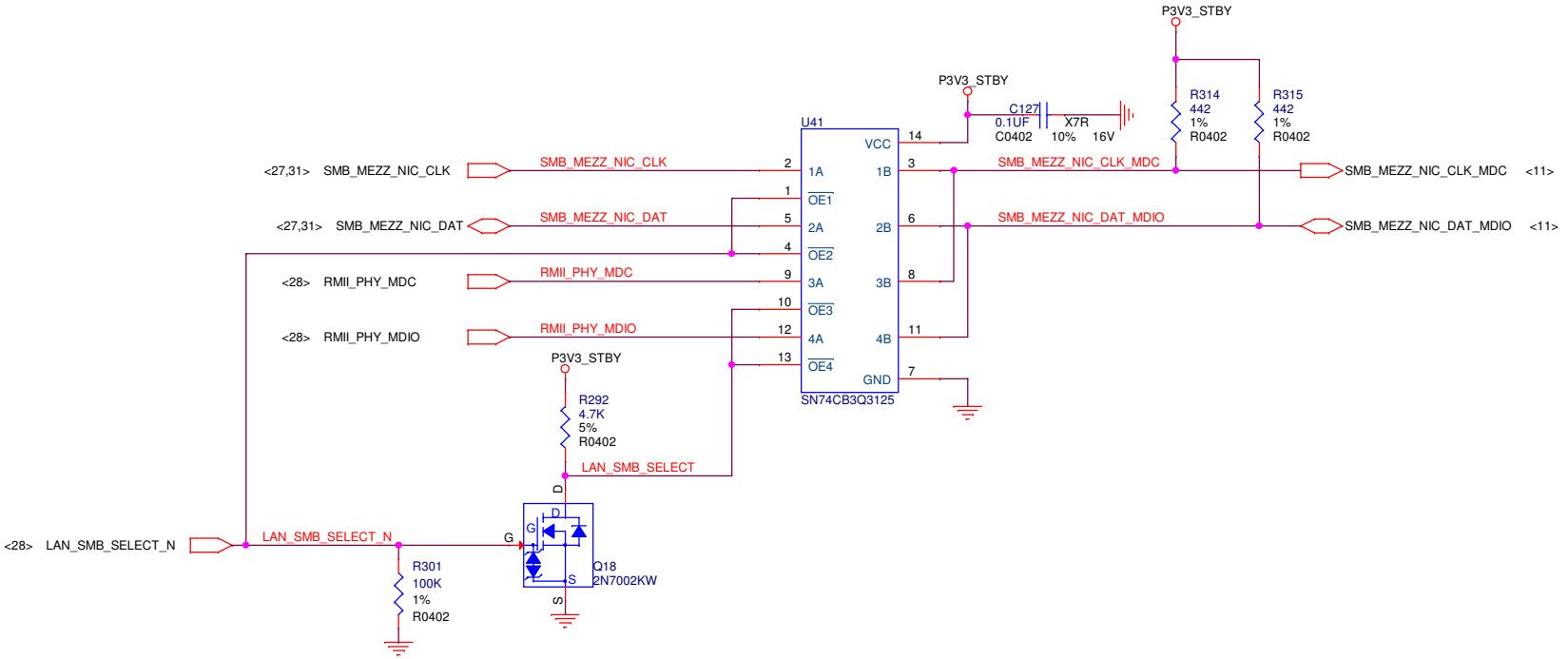






PWR/RST BTN BUFFER

Quanta	Department CCBU	Designer <Designer>	Project F20 Side Plane fab4	Doc Number <Doc>	Rev V17
		Reviewer <Reviewer>	Size B Date: Friday, January 19, 2018	Page Title PWR/RST BTN BUFFER	Sheet 25 of 53



LAN_SMB_SELECT_N
Low: select SMB_MEZZ_NIC_CLK/DAT(default)
High: select RMII_PHY_MDC/MDIO

OCP MEZZ Card NIC SMB/MDC MUX

Quanta	Department CCBU	Designer <Designer>	Project F20 Side Plane fab4	Doc Number <Doc>	Rev
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BMC 1 OF 4

Quanta	Department CCBU	Designer <Designer>	Project F20 Side Plane fab4	Doc Number <Doc>
		Reviewer <Reviewer>	Size B Date: Friday, January 19, 2018	Page Title BMC 1 OF 4
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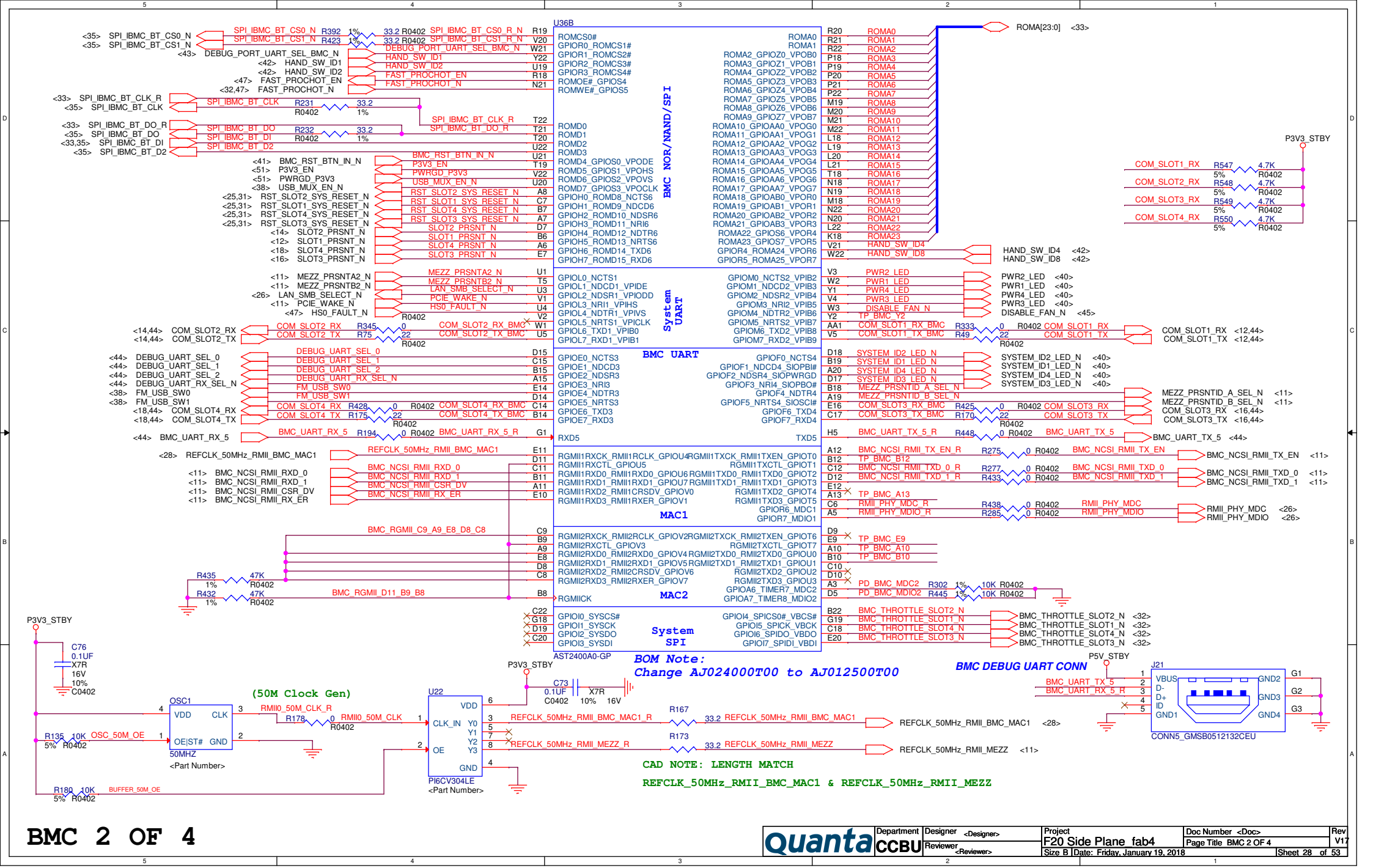

BMC 2 OF 4

Quanta	Department CCBU	Designer <Designer>	Project F20 Side Plane fab4
		Reviewer <Reviewer>	Size B Date: Friday, January 19, 2018

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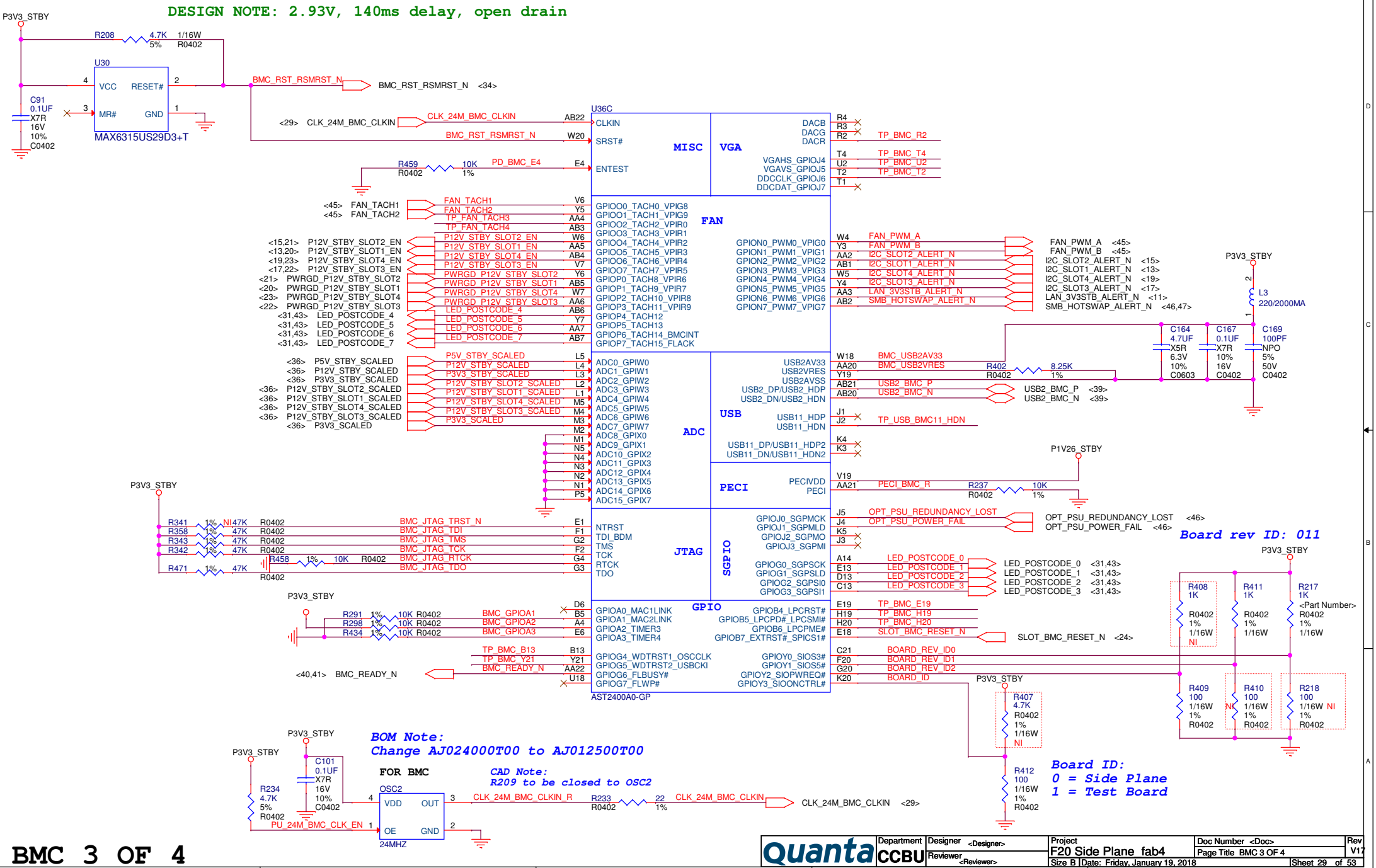
DESIGN NOTE: 2.93V, 140ms delay, open drain
P3V3_STBY
R208 4.7K 5% 1/16W R0402
U30
VCC RESET# MR# GND
MAX6315US29D3+T
C91 0.1UF X7R 16V 10% C0402
BMC_RST_RSMRST_N
BMC_RST_RSMRST_N <34>
U36C
CLK_24M_BMC_CLKIN
BMC_RST_RSMRST_N
R459 10K 1% R0402
PD_BMC_E4
MISC
VGA
DACB DACG DACR
VGAHS_GPIOJ4 VGAVS_GPIOJ5 DDCCLK_GPIOJ6 DDCDAT_GPIOJ7
TP_BMC_R2 TP_BMC_T4 TP_BMC_U2 TP_BMC_T2
FAN
FAN_TACH1 FAN_TACH2 TP_FAN_TACH3 TP_FAN_TACH4
P12V_STBY_SLOT2_EN P12V_STBY_SLOT1_EN P12V_STBY_SLOT4_EN P12V_STBY_SLOT3_EN
PWRGD_P12V_STBY_SLOT2 PWRGD_P12V_STBY_SLOT1 PWRGD_P12V_STBY_SLOT4 PWRGD_P12V_STBY_SLOT3
LED_POSTCODE_4 LED_POSTCODE_5 LED_POSTCODE_6 LED_POSTCODE_7
GPIOO0_TACH0_VPIG8 GPIOO1_TACH1_VPIG9 GPIOO2_TACH2_VPIR0 GPIOO3_TACH3_VPIR1 GPIOO4_TACH4_VPIR2 GPIOO5_TACH5_VPIR3 GPIOO6_TACH6_VPIR4 GPIOO7_TACH7_VPIR5 GPIOP0_TACH8_VPIR6 GPIOP1_TACH9_VPIR7 GPIOP2_TACH10_VPIR8 GPIOP3_TACH11_VPIR9 GPIOP4_TACH12 GPIOP5_TACH13 GPIOP6_TACH14_BMCINT GPIOP7_TACH15_FLACK
GPION0_PWM0_VPIG0 GPION1_PWM1_VPIG1 GPION2_PWM2_VPIG2 GPION3_PWM3_VPIG3 GPION4_PWM4_VPIG4 GPION5_PWM5_VPIG5 GPION6_PWM6_VPIG6 GPION7_PWM7_VPIG7
FAN_PWM_A FAN_PWM_B I2C_SLOT2_ALERT_N I2C_SLOT1_ALERT_N I2C_SLOT4_ALERT_N I2C_SLOT3_ALERT_N LAN_3V3STB_ALERT_N SMB_HOTSWAP_ALERT_N
P3V3_STBY
L3 220/2000MA
C164 4.7UF X5R 6.3V 10% C0603
C167 0.1UF X7R 10% 16V C0402
C169 100PF NPO 5% 50V C0402
ADC
P5V_STBY_SCALED P12V_STBY_SCALED P3V3_STBY_SCALED P12V_STBY_SLOT2_SCALED P12V_STBY_SLOT1_SCALED P12V_STBY_SLOT4_SCALED P12V_STBY_SLOT3_SCALED P3V3_SCALED
ADC0_GPIW0 ADC1_GPIW1 ADC2_GPIW2 ADC3_GPIW3 ADC4_GPIW4 ADC5_GPIW5 ADC6_GPIW6 ADC7_GPIW7 ADC8_GPIX0 ADC9_GPIX1 ADC10_GPIX2 ADC11_GPIX3 ADC12_GPIX4 ADC13_GPIX5 ADC14_GPIX6 ADC15_GPIX7
USB
USB2AV33 USB2VRES USB2AVSS USB2_DP/USB2_HDP USB2_DN/USB2_HDN
BMC_USB2AV33 BMC_USB2VRES R402 8.25K 1% R0402 USB2_BMC_P USB2_BMC_N
USB11_HDP USB11_HDN
TP_USB_BMC11_HDN
USB11_DP/USB11_HDP2 USB11_DN/USB11_HDN2
PECI
PECIVDD PECI
P1V26_STBY
PECI_BMC_R R237 10K 1% R0402
JTAG
NTRST TDI_BDM TMS TCK RTCK TDO
BMC_JTAG_TRST_N BMC_JTAG_TDI BMC_JTAG_TMS BMC_JTAG_TCK BMC_JTAG_RTCK BMC_JTAG_TDO
R341 R358 R343 R342 R471 47K R0402
R458 1% 10K R0402
SGPIO
GPIOJ0_SGPMCK GPIOJ1_SGPMLD GPIOJ2_SGPMO GPIOJ3_SGPMI
GPIOG0_SGPSCK GPIOG1_SGPSLD GPIOG2_SGPSI0 GPIOG3_SGPSI1
OPT_PSU_REDUNDANCY_LOST OPT_PSU_POWER_FAIL
LED_POSTCODE_0 LED_POSTCODE_1 LED_POSTCODE_2 LED_POSTCODE_3
GPIO
GPIOA0_MAC1LINK GPIOA1_MAC2LINK GPIOA2_TIMER3 GPIOA3_TIMER4
BMC_GPIOA1 BMC_GPIOA2 BMC_GPIOA3
R291 R298 R434 10K R0402
GPIOB4_LPCRST# GPIOB5_LPCPD#_LPCSMI# GPIOB6_LPCPME# GPIOB7_EXTRST#_SPICS1#
TP_BMC_E19 TP_BMC_H19 TP_BMC_H20 SLOT_BMC_RESET_N
GPIOG4_WDTRST1_OSCCLK GPIOG5_WDTRST2_USBCKI GPIOG6_FLBUSY# GPIOG7_FLWP#
GPIOY0_SIOS3# GPIOY1_SIOS5# GPIOY2_SIOPWREQ# GPIOY3_SIOONCTRL#
TP_BMC_B13 TP_BMC_Y21 BMC_READY_N
BOARD_REV_ID0 BOARD_REV_ID1 BOARD_REV_ID2 BOARD_ID
AST2400A0-GP
Board rev ID: 011
R408 1K R0402 1% 1/16W NI
R411 1K R0402 1% 1/16W
R217 1K <Part Number> R0402 1% 1/16W
R409 100 1/16W 1% R0402
R410 100 1/16W NI 1% R0402
R218 100 1/16W NI 1% R0402
R407 4.7K R0402 1% 1/16W NI
R412 100 1/16W 1% R0402
Board ID:
0 = Side Plane
1 = Test Board
BOM Note:
Change AJ024000T00 to AJ012500T00
FOR BMC
CAD Note:
R209 to be closed to OSC2
C101 0.1UF X7R 16V 10% C0402
R234 4.7K 5% R0402
PU_24M_BMC_CLK_EN
OSC2
VDD OUT OE GND
24MHZ
CLK_24M_BMC_CLKIN_R
R233 22 1% R0402
CLK_24M_BMC_CLKIN
CLK_24M_BMC_CLKIN <29>
BMC 3 OF 4
Quanta
Department CCBU
Designer <Designer>
Reviewer <Reviewer>
Project F20 Side Plane fab4
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Page Title BMC 3 OF 4
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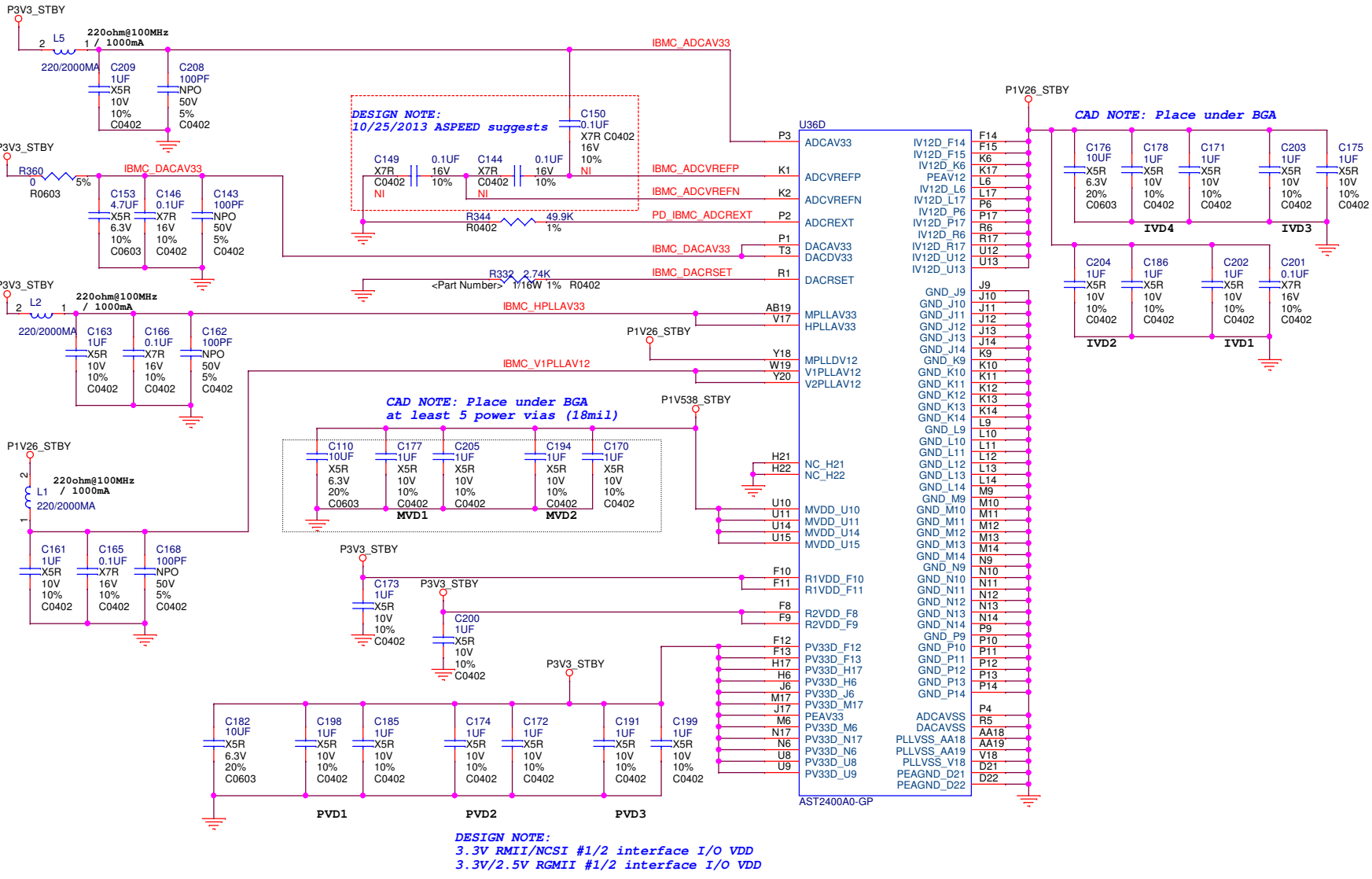

BMC 4 OF 4

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		Reviewer <Reviewer>	Size B Date: Friday, January 19, 2018	Page Title BMC 4 OF 4
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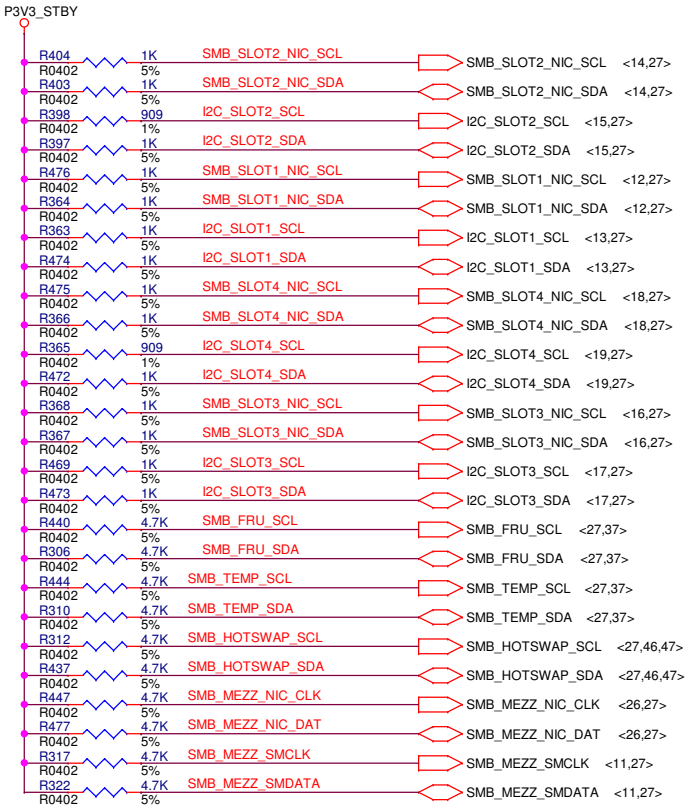
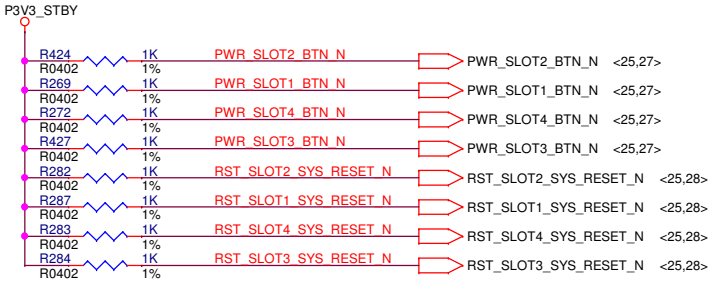
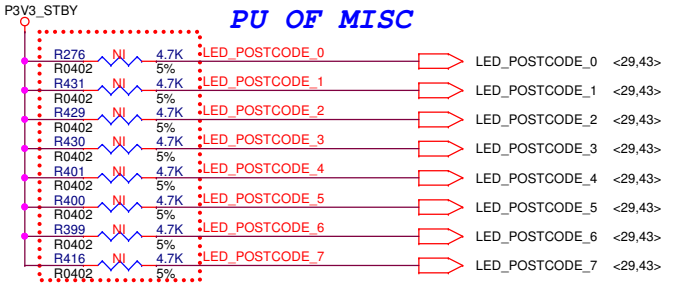
PU OF BMC SMBUS

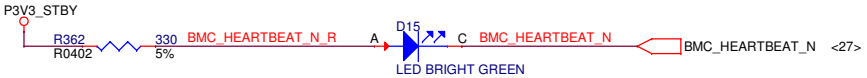




PU OF MISC

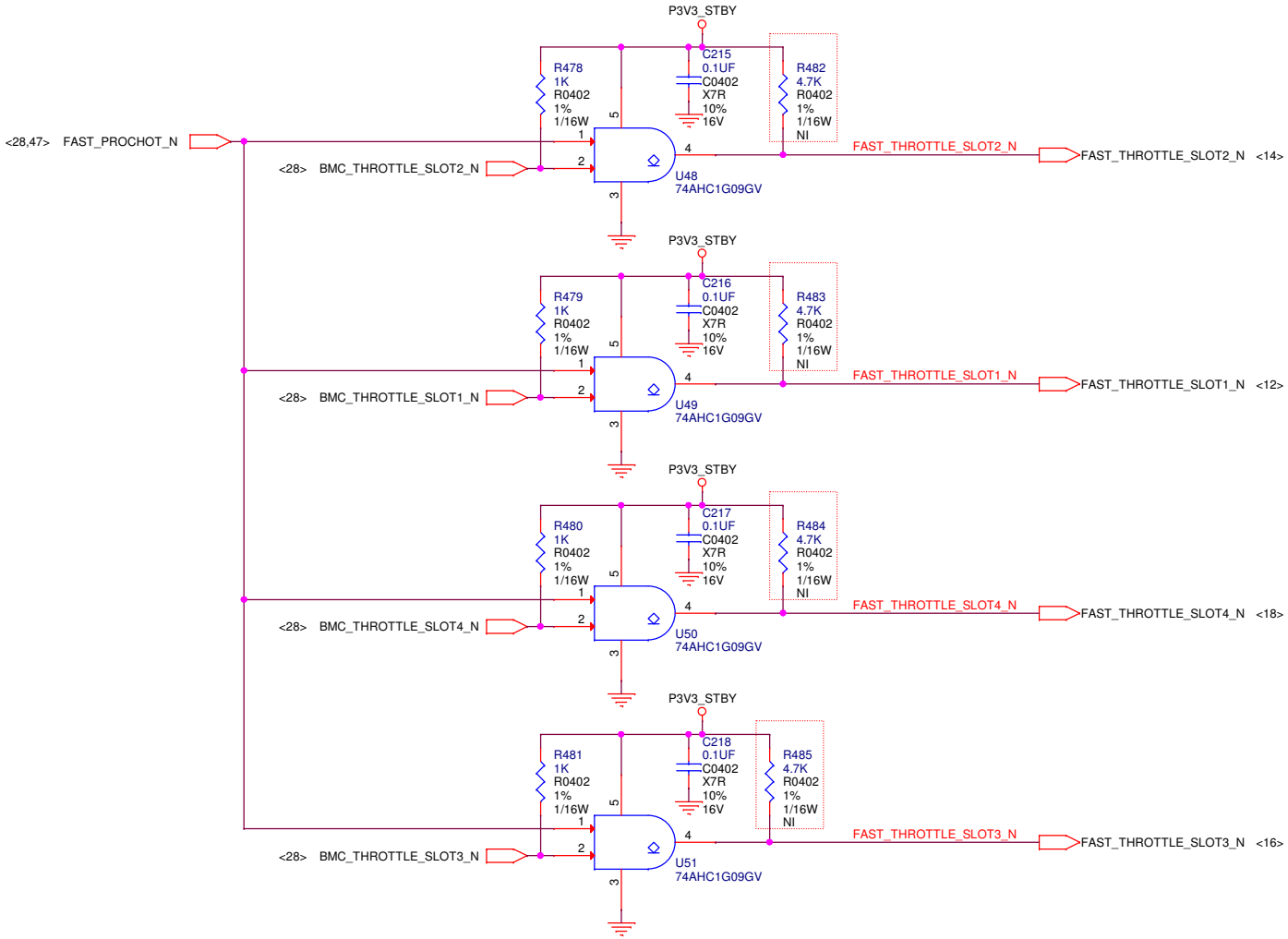


HEART BEATING LED



BMC PULL UP

Quanta	Department CCBU	Designer <Designer>	Project F20 Side Plane fab4	Doc Number <Doc>	Rev V17
		Reviewer <Reviewer>	Size B Date: Friday, January 19, 2018	Page Title BMC PULL UP	Sheet 31 of 53



FAST_THROTTLE_N

Quanta	Department CCBU	Designer <Designer>	Project F20 Side Plane fab4	Doc Number <Doc>	Rev V17
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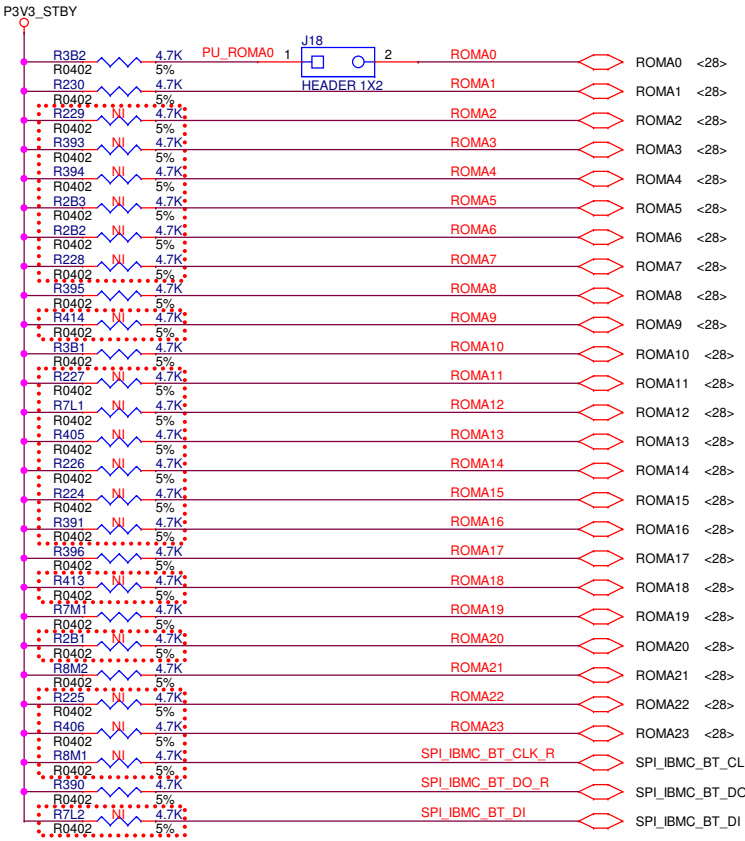


```
ROMA[1:0] : ARM CPU boot code selection
 00 : Boot from NOR flash memory
 01 : Boot from NAND flash memory
*10 : Boot from SPI flash memory
 11 : Disable ARM CPU operation

ROMA[3:2] : VGA memory size selection
*00 : Select 8 MB VGA memory
 01 : Select 16 MB VGA memory
 10 : Select 32 MB VGA memory
 11 : Select 64 MB VGA memory

ROMA4 : Boot flash memory extended option
NOR type flash: data bus width selection
*0 : Select 8 bits interface
 1 : Select 16 bits interface

SPI type flash: boot address mode selection
*0 : Boot with 24 bits address mode
 1 : Boot with 32 bits address mode

ROMA5 : Enable VGA BIOS ROM
*0: No VGA BISO ROM (for on-board applications)
 1: Enable VGA BIOS ROM (for add-on card applications)

ROMA6 : Define MAC#1 interface
 *0: RMII/NCSI
  1: RGMII

ROMA7 : Define MAC#2 interface
*0: RMII/NCSI
1: RGMII

ROMA[9:8] : H-PLL default clock frequency selection
 00: Select 384 MHz
*01: Select 360 MHz
 10: Select 336 MHz
 11: Select 204 MHz

ROMA[11:10] : CPU/AHB clock frequency ratio selection
 00 : Select CPU:AHB = 1:1
*01 : Select CPU:AHB = 2:1
 10 : Select CPU:AHB = 4:1
 11 : Select CPU:AHB = 3:1
```

```
ROMA[13:12] : SPI mode selection
*00 : Disable SPI interface
 01 : Enable SPI Master
 10 : Enable SPI Master and SPI Slave to AHB Bridge
11 : Enable SPI Bypass

ROMA14 : Enable LPC dedicated reset pin function
*0 : LPC reset is shared with PCI reset pin
 1 : LPC reset is located at pin number E19, shared with GPIOB4.

ROMA15 : VGA Class Code selection
*0 : Select the Class Code for video device
1 : Select the Class Code for VGA device

ROMA16 : SuperIO configuration address selection
*0 : Decode 0x2E
 1 : Decode 0x4E

ROMA17 : Enable BMC 2nd boot watchdog timer
 0 : Disable
*1 : Enable BMC 2nd boot watchdog timer start counting at power up.

ROMA23,ROMA18 : Clock source selection
 *00 : 24MHz
  01: 48MHz
  10 : 25MHz USBCKI = 24MHz
  11:  25MHz USBCKI = 48MHz


ROMA19 : Disable MSI controller
 0 : Enable
*1 : Disable

ROMA20 : DISABLE LPC TO DECODE SUPERIO 0X2E / 0X4E ADDRESS
*0 : Disable, normal reset sequence
 1 : Enable

ROMA21 :;Enable GPIOD pass-through mode
 0: Disable, pass through can be enabled by SCU8C[11:8].
*1: Enable pass-through at power on.

ROMA22 : Enable GPIOE pass-through mode
*0: Disable, pass through can be enabled by SCU8C[15:12]
 1: Enable pass-through at power on.

ROMD[2:0]
DRAM configration setting
 000: DDR3 SDRAM with CL= 5, CWL = 5
*010: DDR3 SDRAM with CL = 6, CWL = 5
 100: DDR3 SDRAM with CL = 7, CWL = 6
 110: DDR3 SDRAM with CL = 8, CWL = 6
 001: DDR2 SDRAM with CL = 4
 011: DDR2 SDRAM with CL = 5
 101: DDR2 SDRAM with CL = 6
 111: DDR2 SDRAM with CL = 7
```

BMC HW STRAPPING

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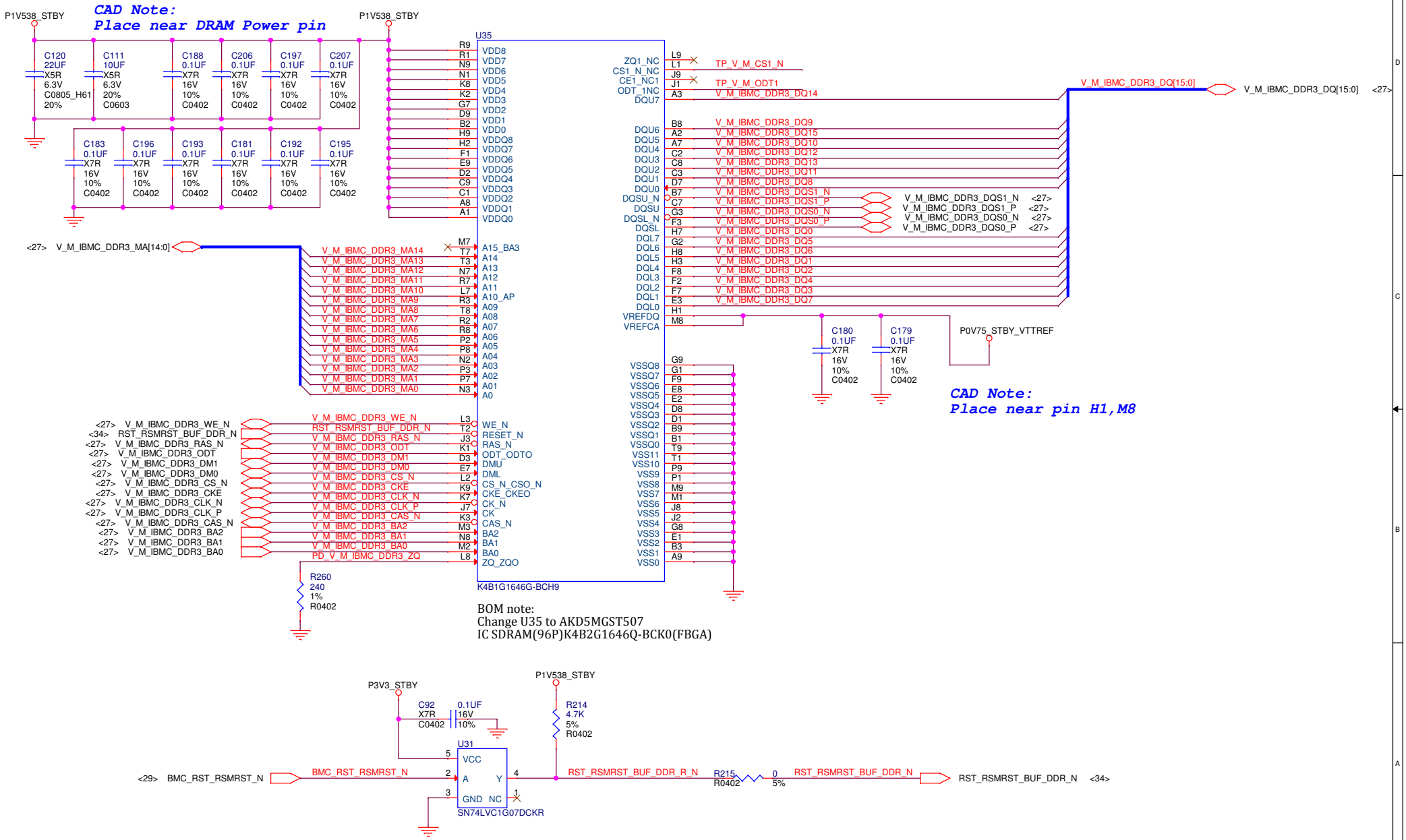

BMC DDRIII SDRAM

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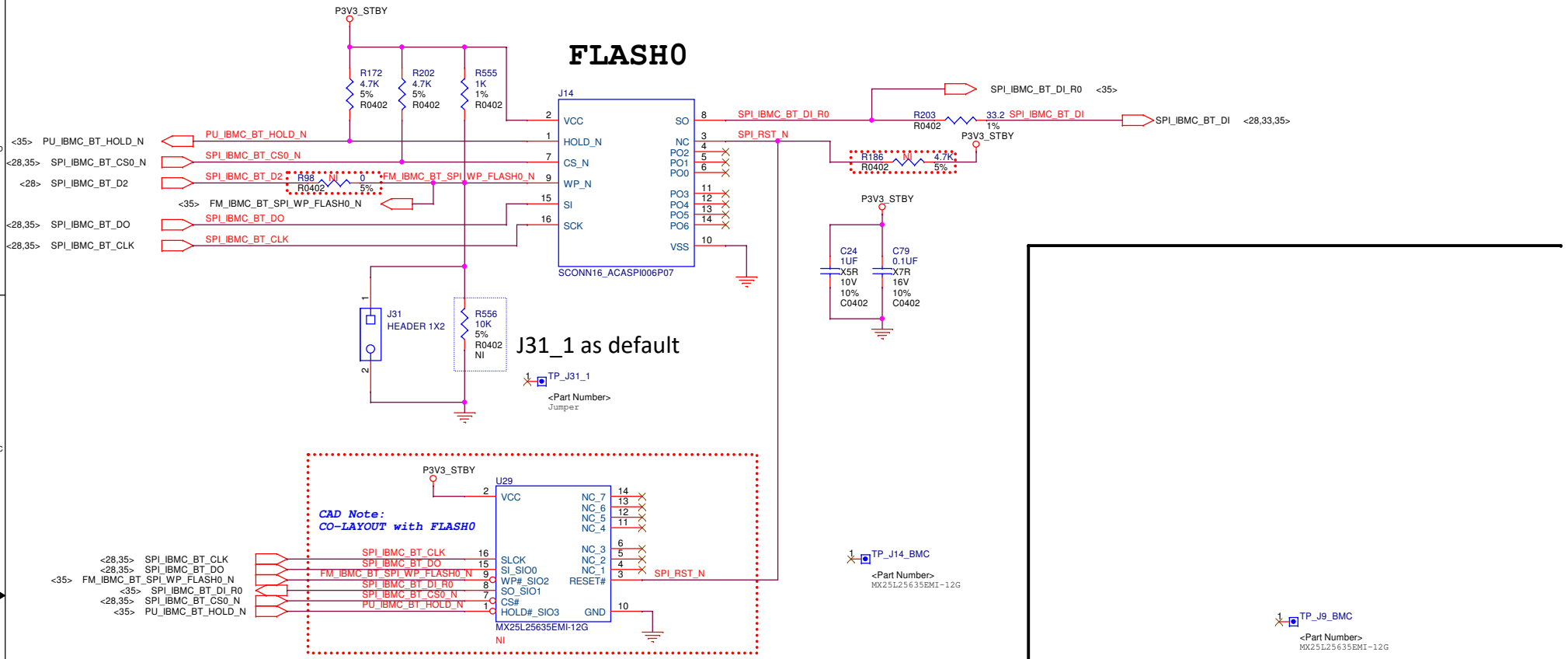
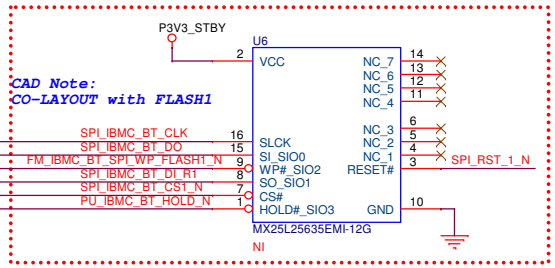
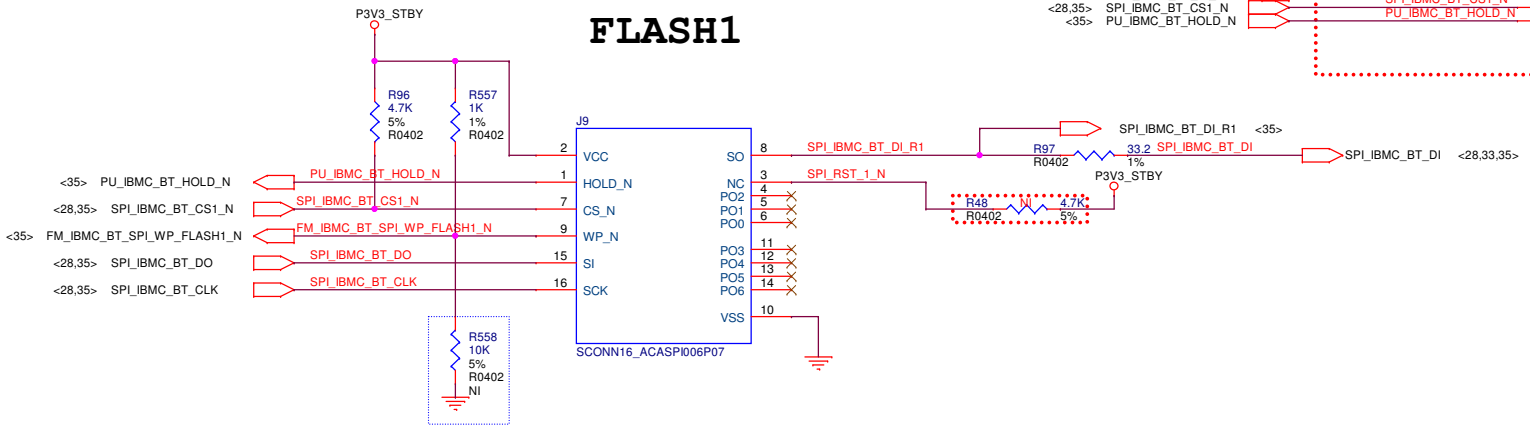
FLASH0





FLASH1



BMC SPI FLASH

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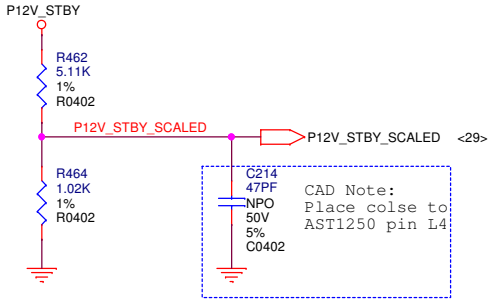
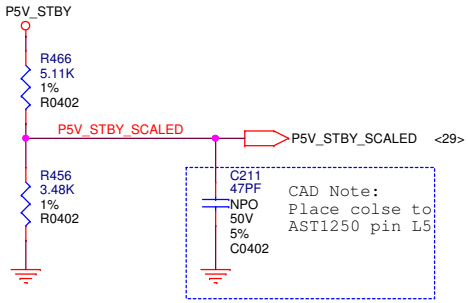
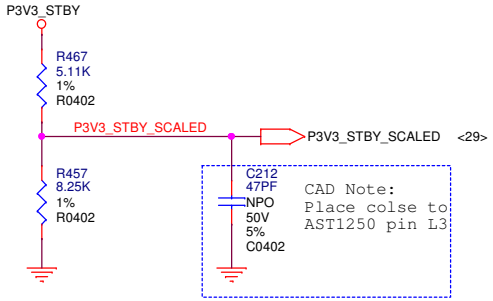
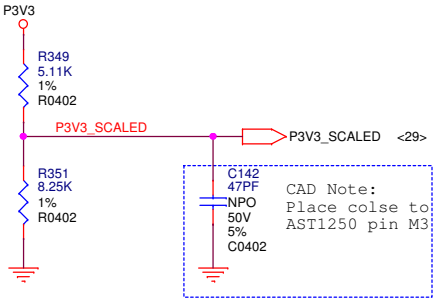
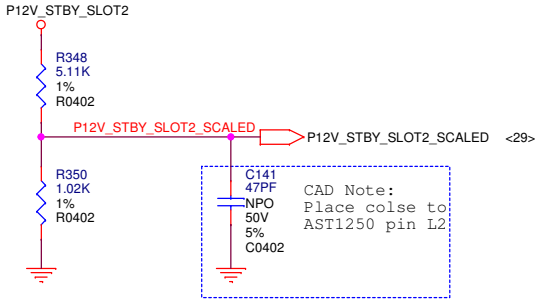
ROUTE ALL ADC NETS AT 6 MILLS WIDE

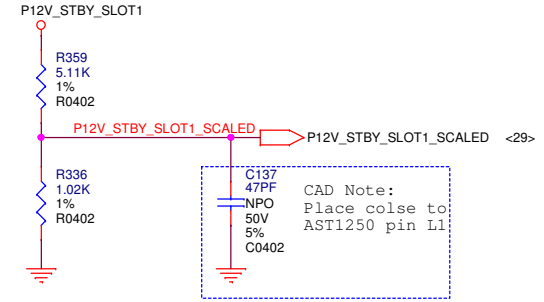


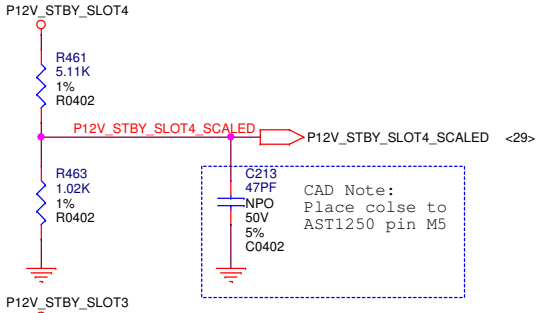


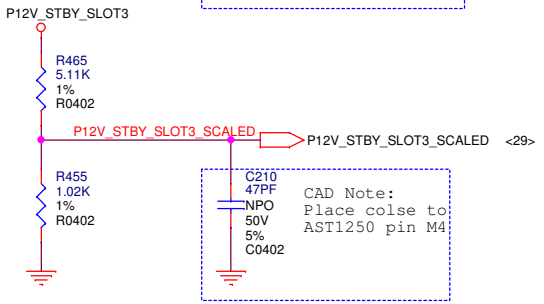












BMC VOLTAGE SENSOR

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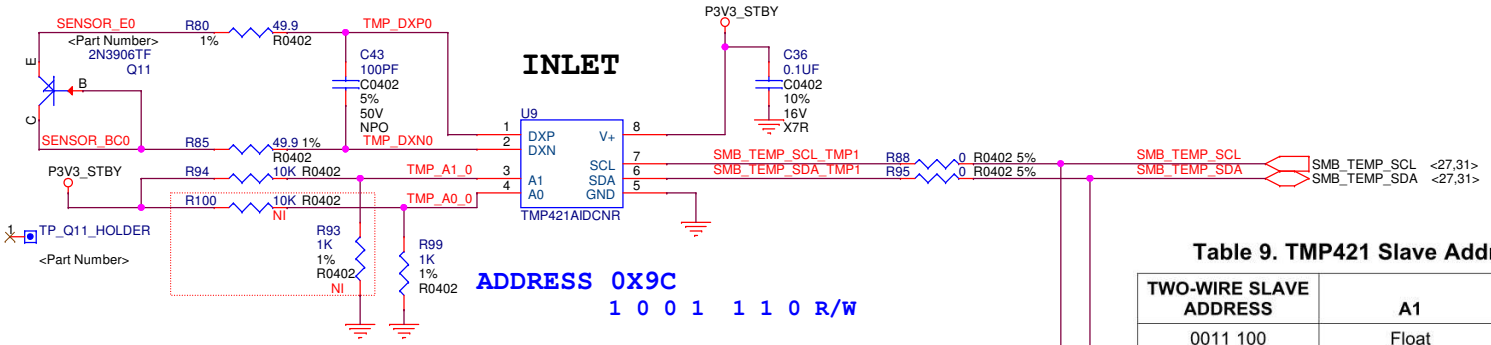


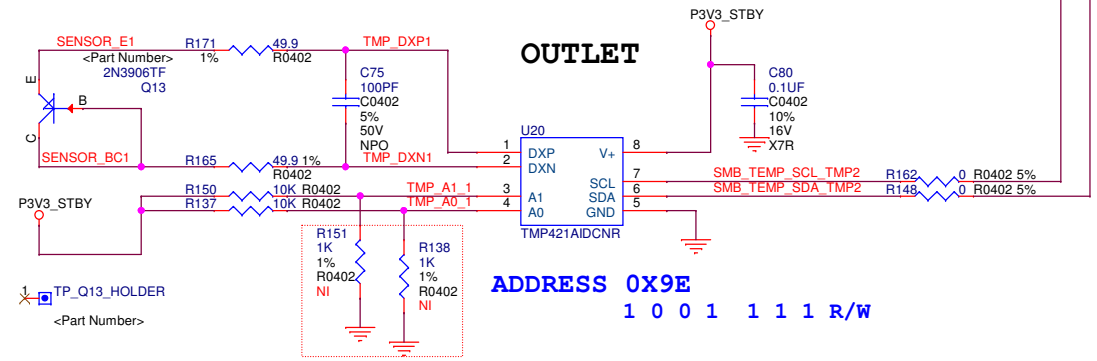


Table 9. TMP421 Slave Address Options

TWO-WIRE SLAVE ADDRESS	A1	A0
0011 100	Float	0
0011 101	Float	1
0011 110	0	Float
0011 111	1	Float
0101 010	Float	Float
1001 100	0	0
1001 101	0	1
1001 110	1	0
1001 111	1	1

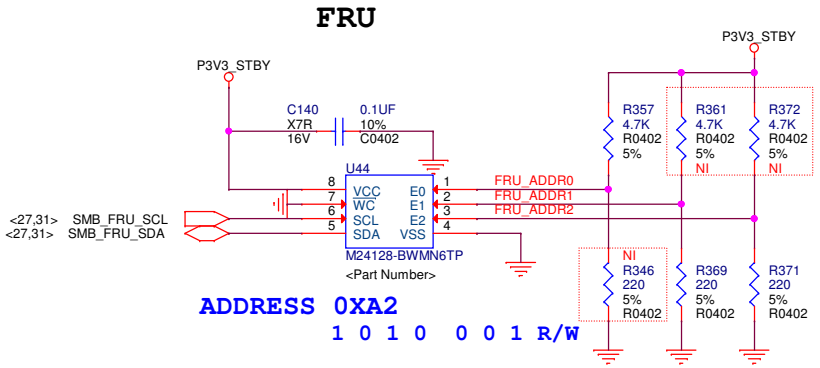


Table 2. Device Select Code

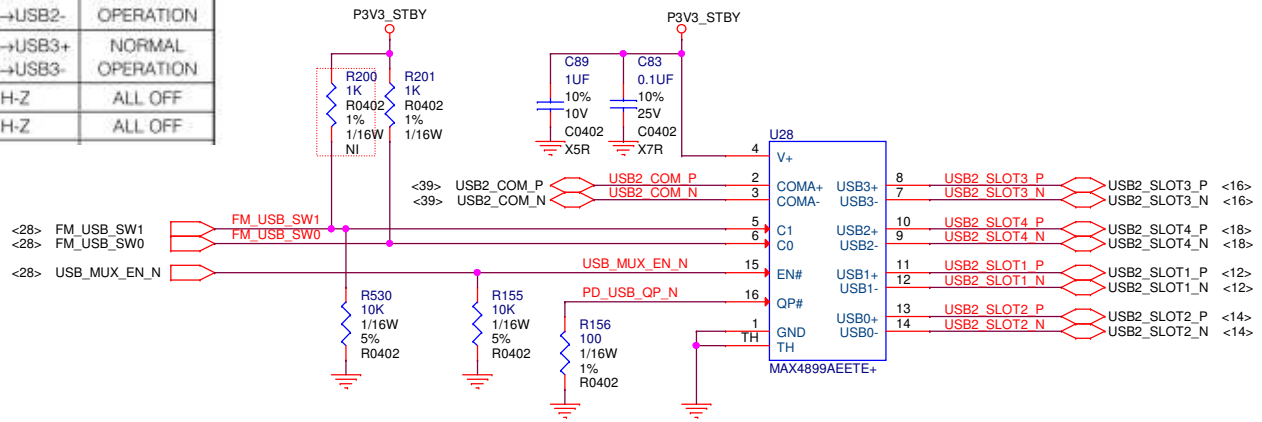
	Device Type Identifier[1]				Chip Enable Address[2]			$\overline{RW}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	E2	E1	E0	$\overline{RW}$

Note: 1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

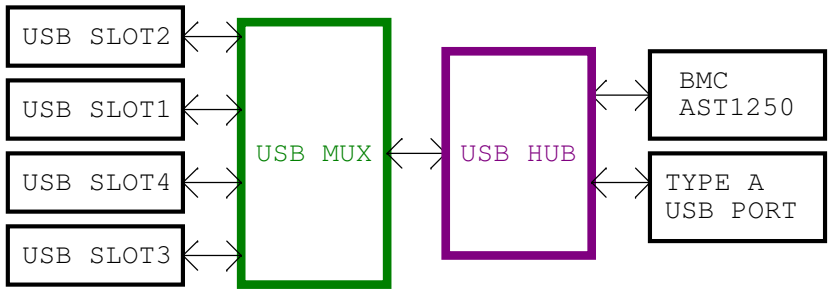
FRU address

TEMP SENSOR / FRU

MAX4899AE					
$\overline{QP}$	$\overline{EN}$	C_1	C_0	FUNCTION	COMMENT
0	0	0	0	COMA+ →USB0+ COMA- →USB0-	NORMAL OPERATION
0	0	0	1	COMA+ →USB1+ COMA- →USB1-	NORMAL OPERATION
0	0	1	0	COMA+ →USB2+ COMA- →USB2-	NORMAL OPERATION
0	0	1	1	COMA+ →USB3+ COMA- →USB3-	NORMAL OPERATION
0	1	X	X	HIGH-Z	ALL OFF
1	1	X	X	HIGH-Z	ALL OFF



DESIGN NOTE:



USB MUX

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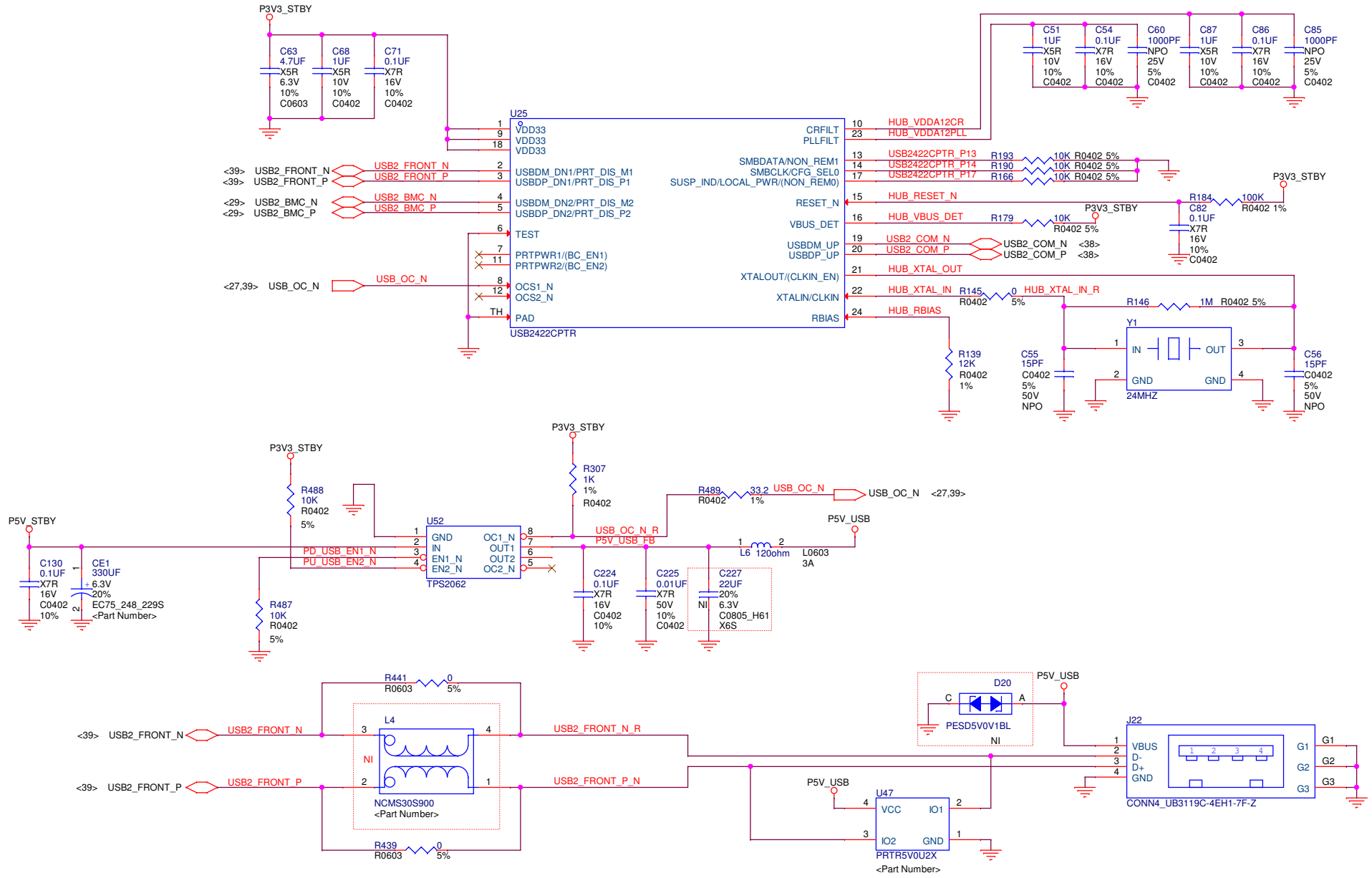

USB HUB

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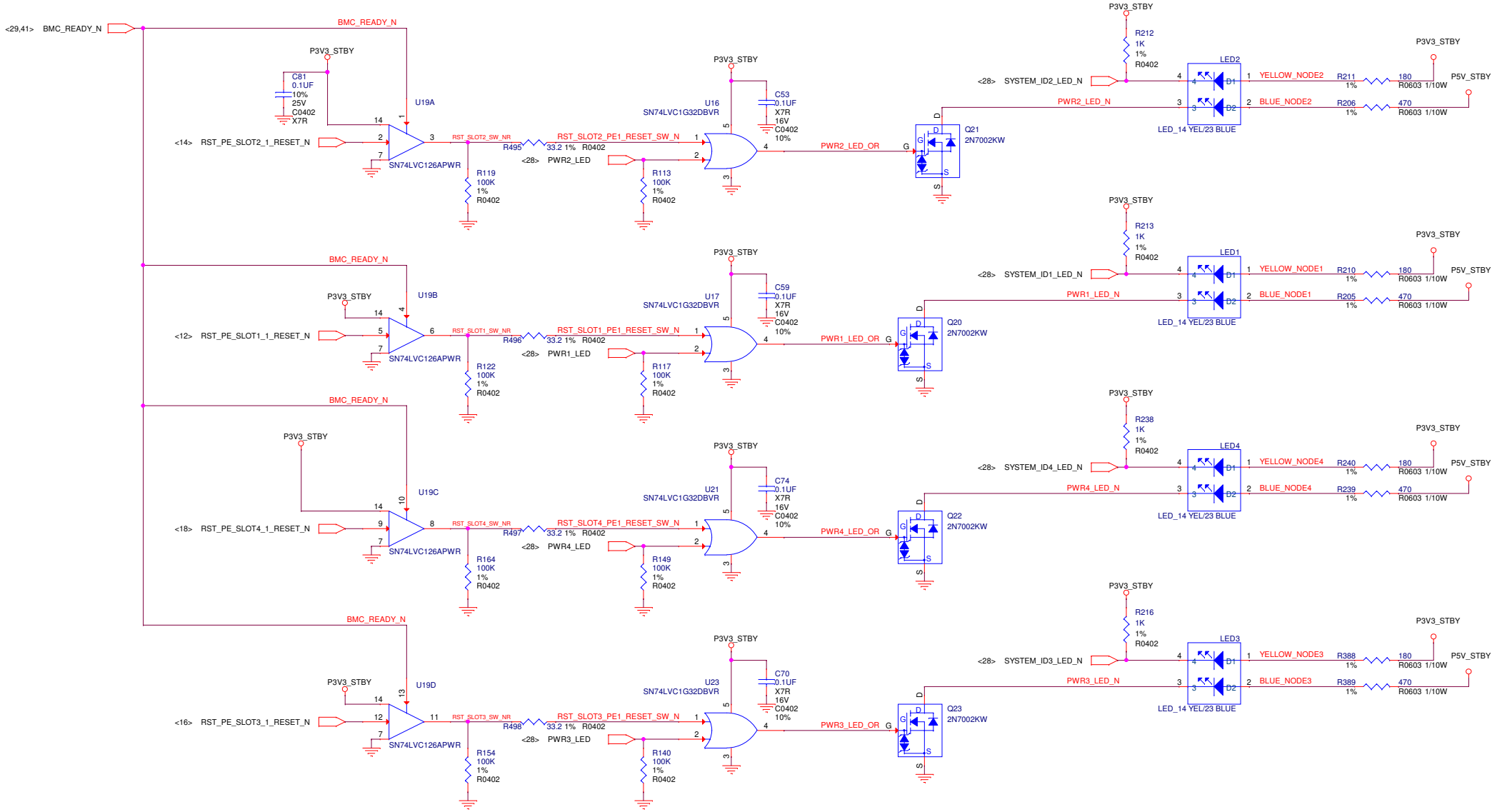

POWER	System Identify	Status	
off	off	X	LED consistently off
off	on	Good	LED blue for 0.1sec, off for 0.9sec, and loop
on	off	Good	LED consistently blue
on	on	Good	LED blue for 0.9sec, off for 0.1sec, and loop
off	on	Bad	LED yellow for 0.1sec, off for 0.9sec, and loop
on	off	Bad	LED consistently yellow
on	on	Bad	LED yellow for 0.9sec, off for 0.1sec, and loop

PWR/SYSTEM_ID LED

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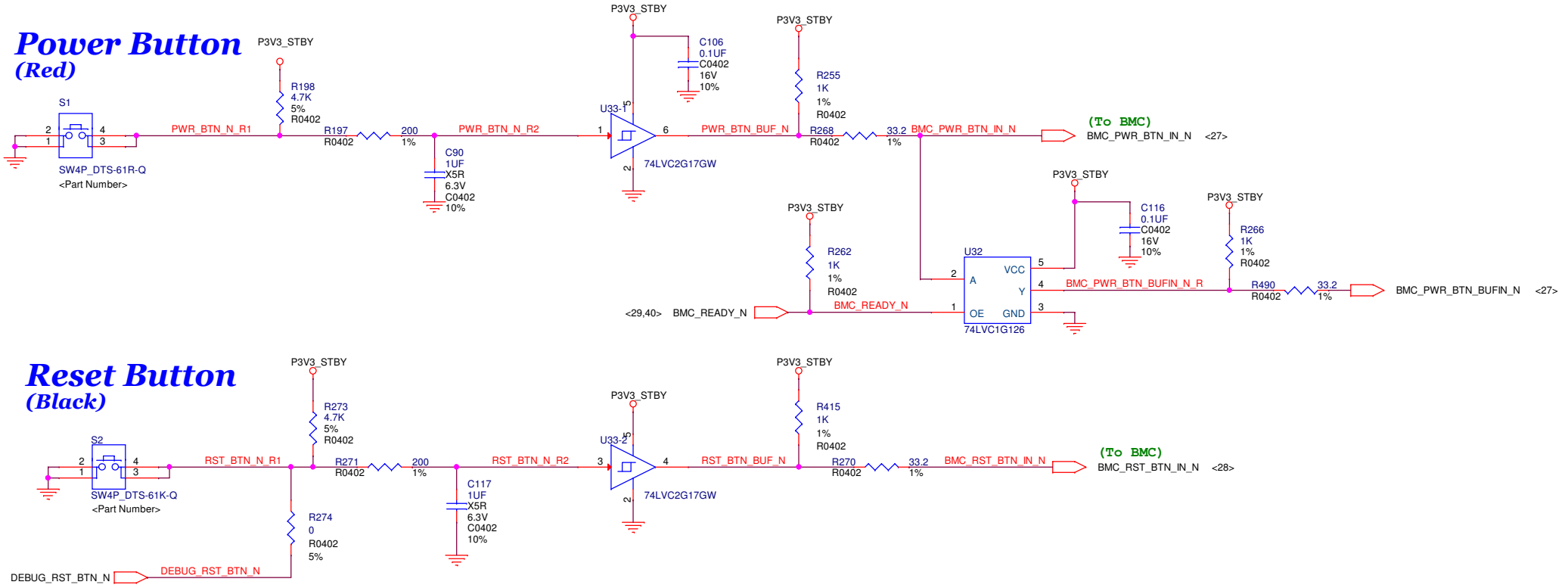

PWR/RST BUTTON

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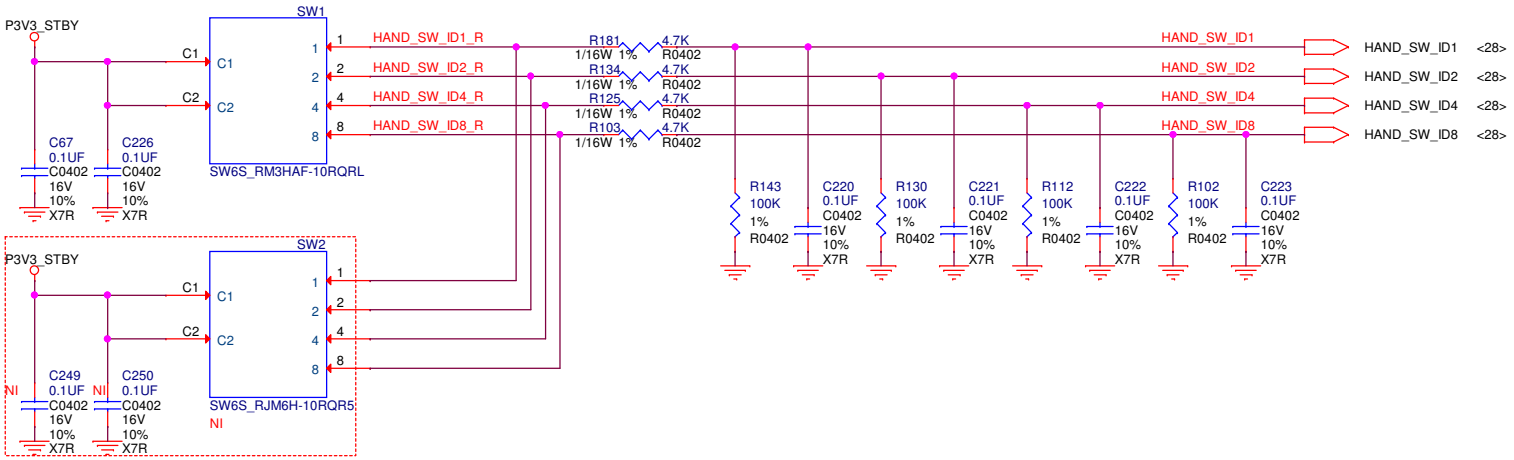

HAND_ SW_ID8	HAND_ SW_ID4	HAND_ SW_ID2	HAND_ SW_ID1	Position	
L	L	L	L	1	1S SERVER SLOT1 SELECT (DEFAULT)
L	L	L	H	2	1S SERVER SLOT2 SELECT
L	L	H	L	3	1S SERVER SLOT3 SELECT
L	L	H	H	4	1S SERVER SLOT4 SELECT
L	H	L	L	5	BMC DEBUG PORT SELECT
L	H	L	H	6	1S SERVER SLOT1 SELECT
L	H	H	L	7	1S SERVER SLOT2 SELECT
L	H	H	H	8	1S SERVER SLOT3 SELECT
H	L	L	L	9	1S SERVER SLOT4 SELECT
H	L	L	H	10	BMC DEBUG PORT SELECT

SELECT SWITCH

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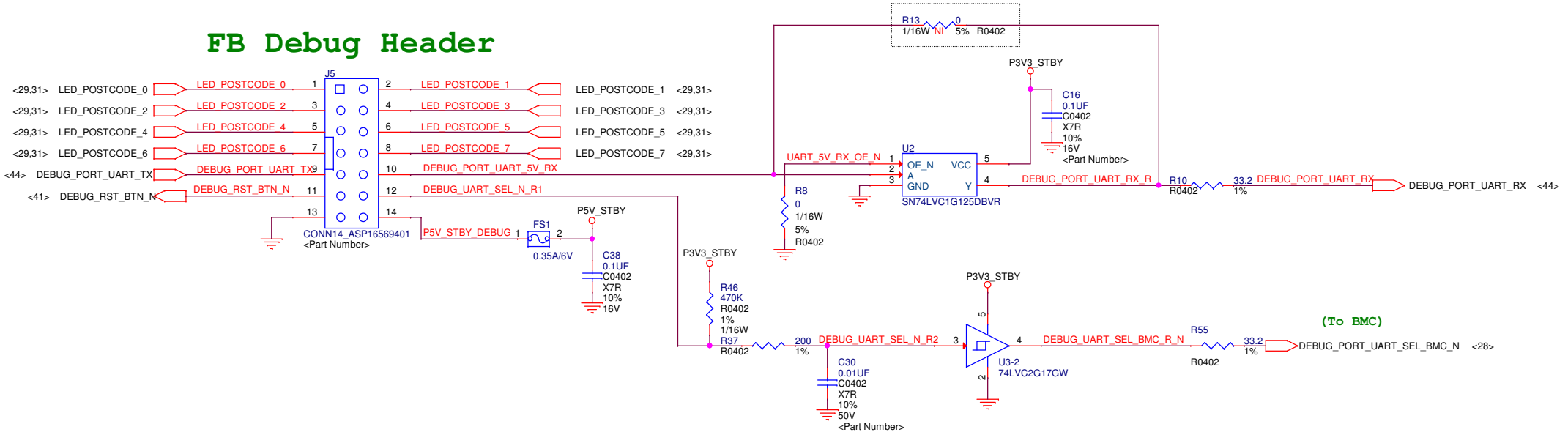
FB Debug Header



DEBUG

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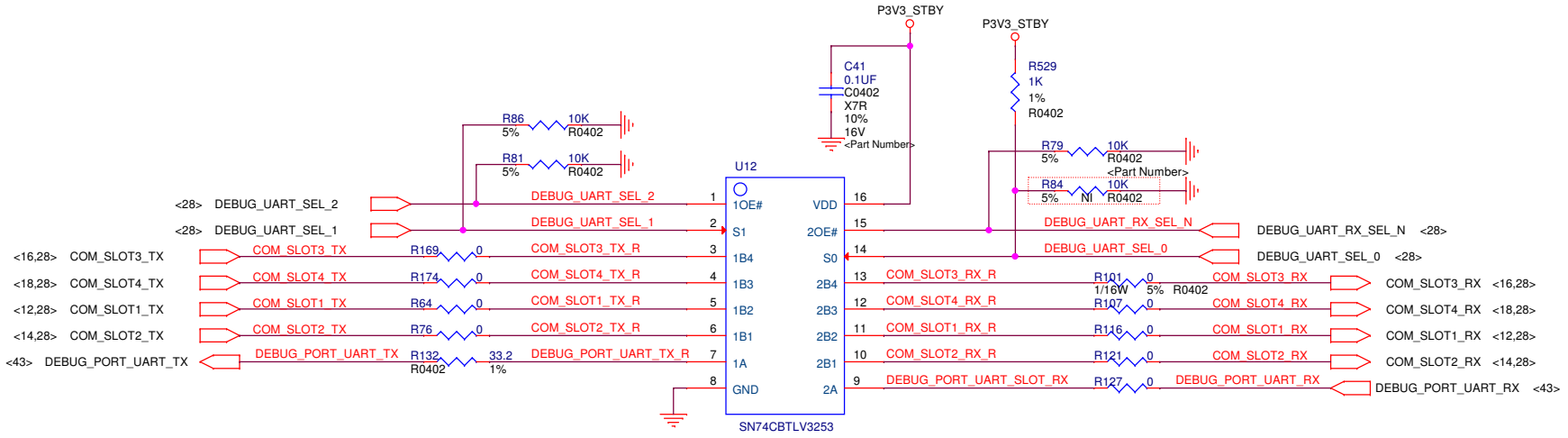

SEL_2	SEL_1	SEL_0	RX_SEL_N	
0	0	0	0	SLOT2
0	0	1	0	SLOT1
0	1	0	0	SLOT4
0	1	1	0	SLOT3
0	X	X	1	SLOT RX Disable
1	0	0	1	BMC Debug

UART select table

UART

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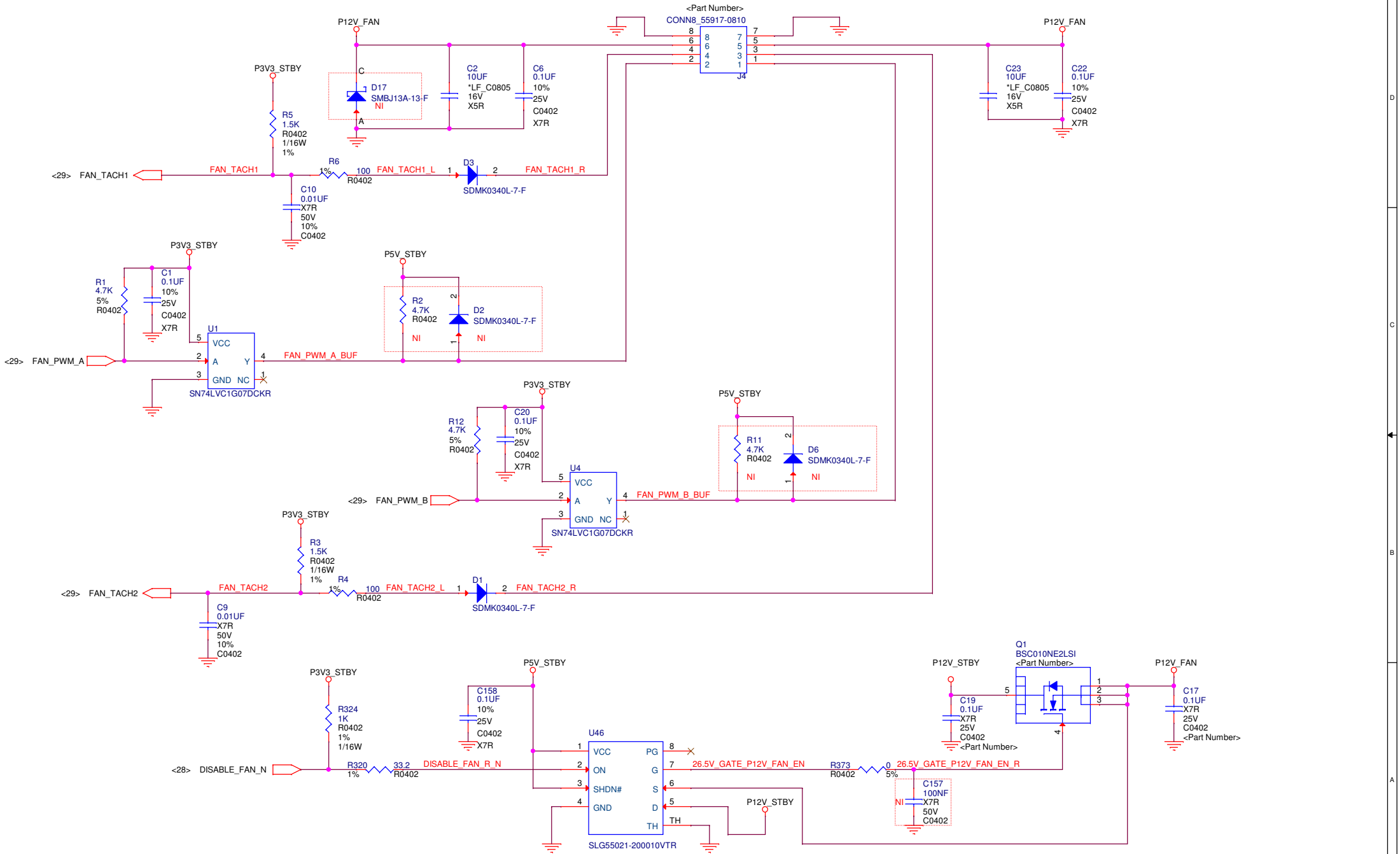
P12V_FAN
<Part Number>
CONN8_55917-0810
J4
C2
10UF
*LF_C0805
16V
X5R
C6
0.1UF
10%
25V
C0402
X7R
C23
10UF
*LF_C0805
16V
X5R
C22
0.1UF
10%
25V
C0402
X7R
P3V3_STBY
D17
SMBJ13A-13-F
NI
R5
1.5K
R0402
1/16W
1%
<29> FAN_TACH1
FAN_TACH1
R6
100
R0402
FAN_TACH1_L
D3
SDMK0340L-7-F
FAN_TACH1_R
C10
0.01UF
X7R
50V
10%
C0402
P3V3_STBY
P5V_STBY
R1
4.7K
5%
R0402
C1
0.1UF
10%
25V
C0402
X7R
U1
VCC
A
Y
GND
NC
SN74LVC1G07DCKR
<29> FAN_PWM_A
FAN_PWM_A_BUF
R2
4.7K
R0402
D2
SDMK0340L-7-F
NI
P3V3_STBY
P5V_STBY
R12
4.7K
5%
R0402
C20
0.1UF
10%
25V
C0402
X7R
U4
SN74LVC1G07DCKR
<29> FAN_PWM_B
FAN_PWM_B_BUF
R11
4.7K
R0402
D6
SDMK0340L-7-F
NI
P3V3_STBY
R3
1.5K
R0402
1/16W
1%
<29> FAN_TACH2
FAN_TACH2
R4
100
R0402
FAN_TACH2_L
D1
SDMK0340L-7-F
FAN_TACH2_R
C9
0.01UF
X7R
50V
10%
C0402
P3V3_STBY
P5V_STBY
R324
1K
R0402
1%
1/16W
C158
0.1UF
10%
25V
C0402
X7R
<28> DISABLE_FAN_N
R320
33.2
1%
R0402
DISABLE_FAN_R_N
U46
VCC
ON
SHDN#
GND
PG
G
S
D
TH
SLG55021-200010VTR
26.5V_GATE_P12V_FAN_EN
R373
0
5%
R0402
26.5V_GATE_P12V_FAN_EN_R
P12V_STBY
C157
100NF
X7R
50V
C0402
NI
P12V_STBY
Q1
BSC010NE2LSI
<Part Number>
C19
0.1UF
X7R
25V
C0402
<Part Number>
P12V_FAN
C17
0.1UF
X7R
25V
C0402
<Part Number>
FAN CONN
Quanta
Department
CCBU
Designer
<Designer>
Reviewer
<Reviewer>
Project
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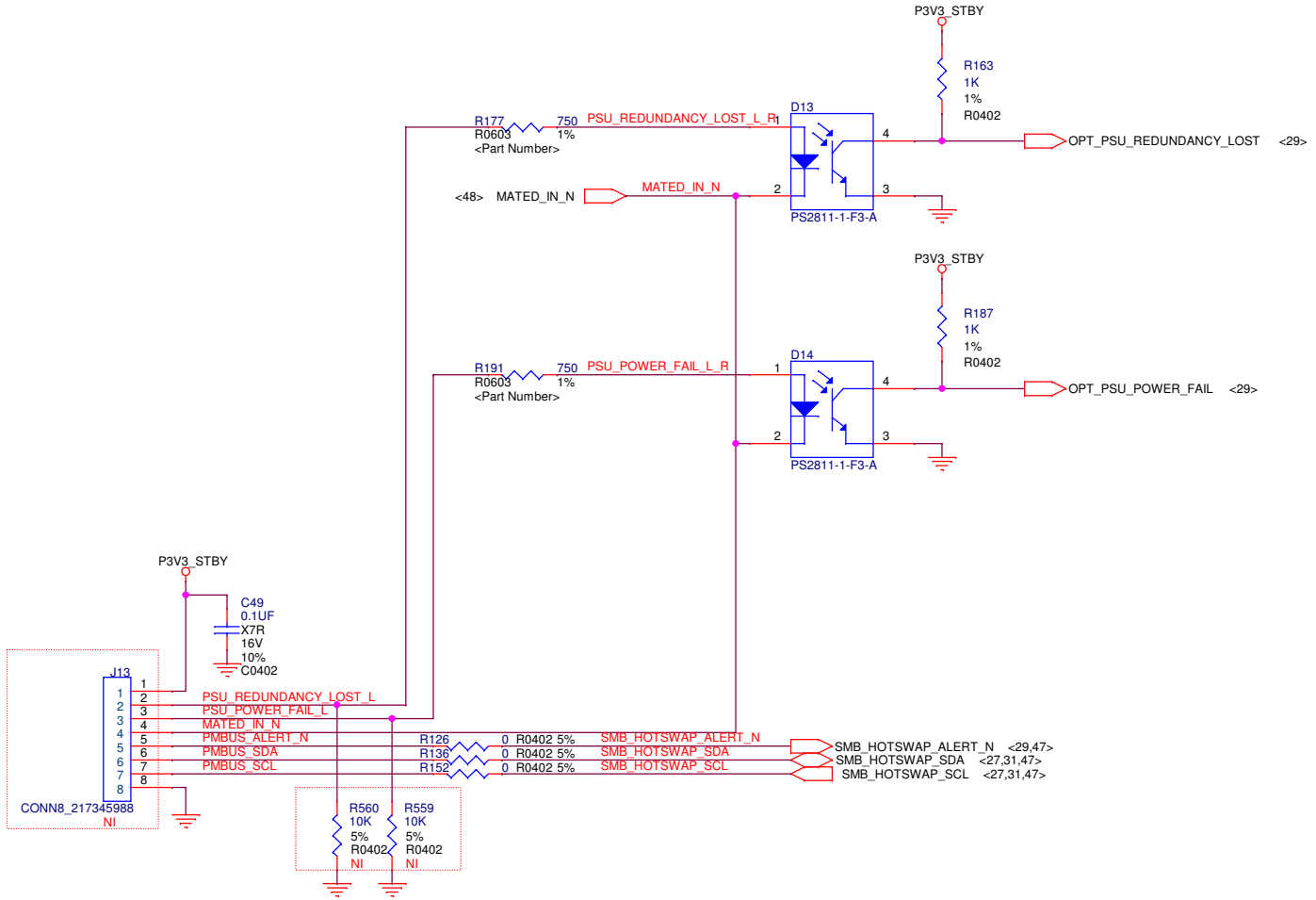

Power Side Band

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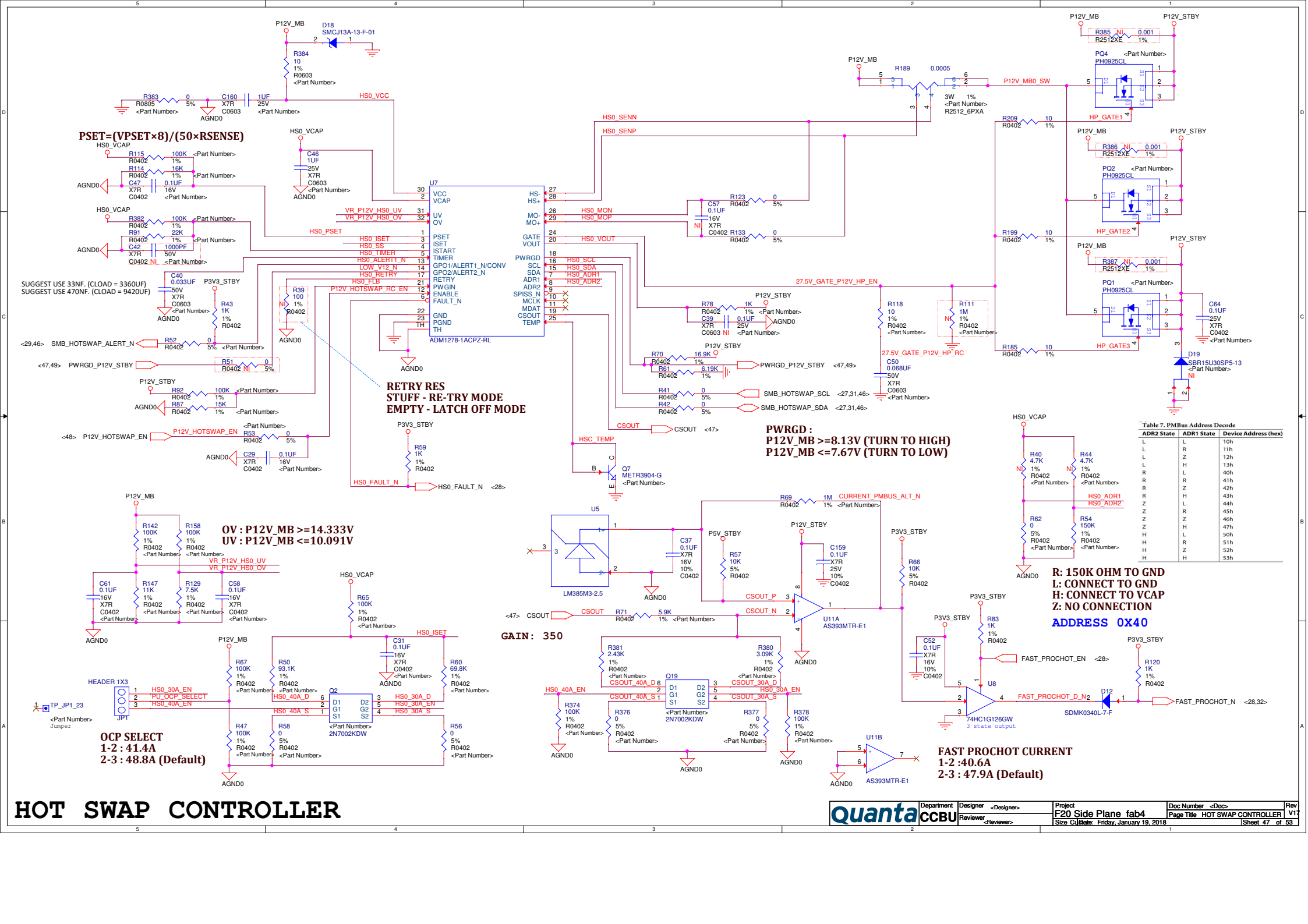
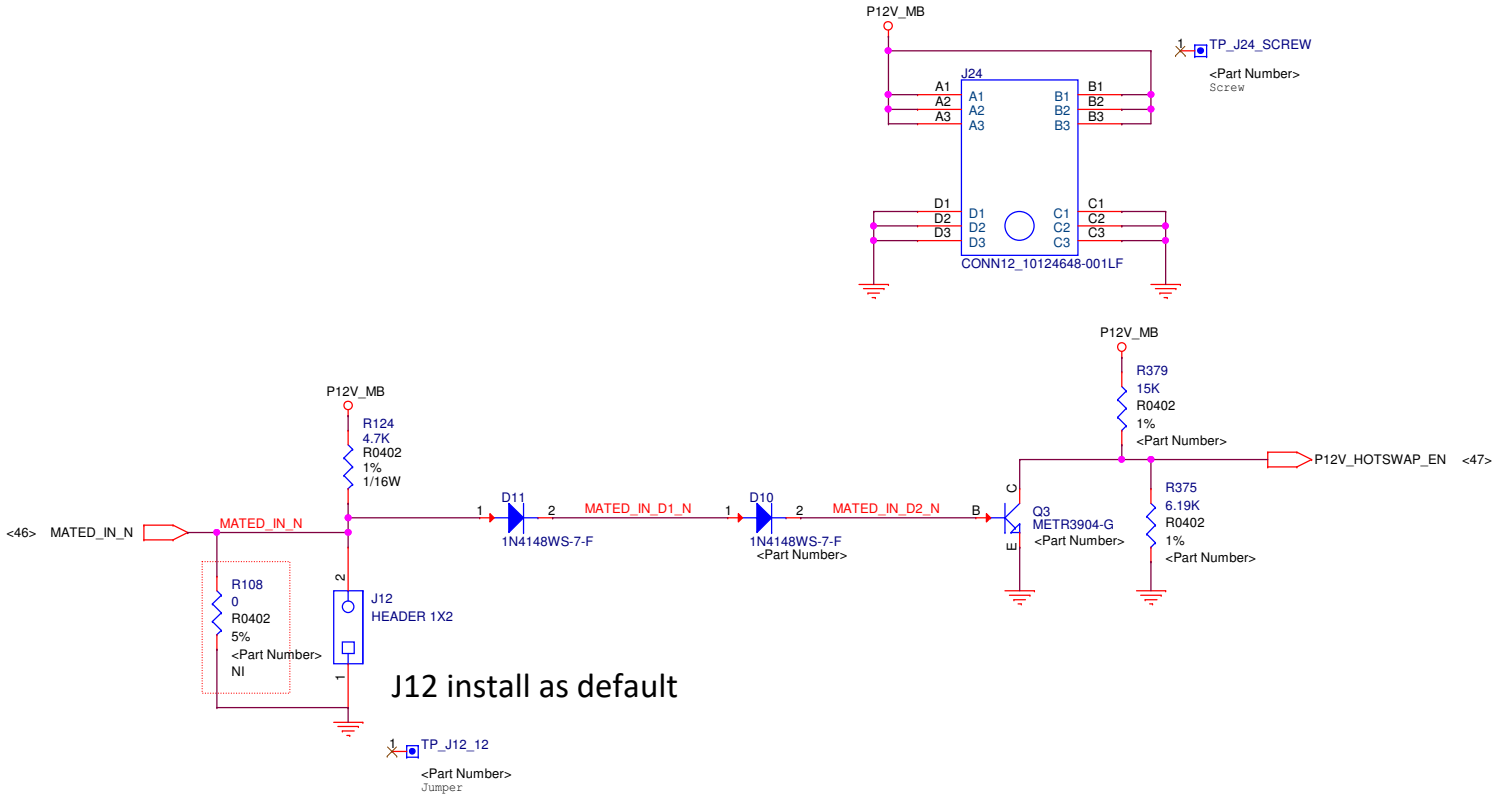


Table 7. PMBus Address Decode

ADR2 State	ADR1 State	Device Address (hex)
L	L	10h
L	R	11h
L	Z	12h
L	H	13h
R	L	40h
R	R	41h
R	Z	42h
R	H	43h
Z	L	44h
Z	R	45h
Z	Z	46h
Z	H	47h
H	L	50h
H	R	51h
H	Z	52h
H	H	53h



POWER CONN

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Design specification

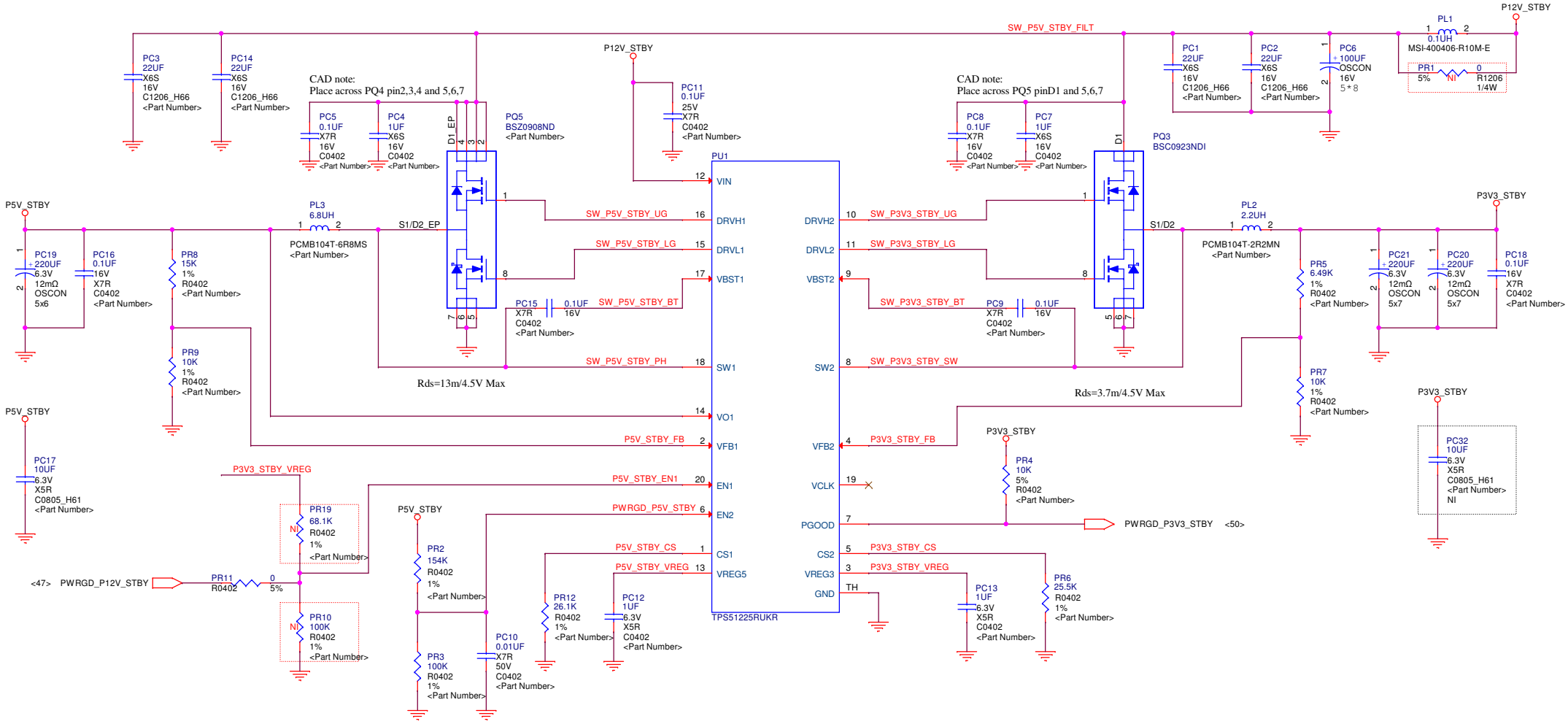
P5V_STBY

Output Voltage = 5V±5%
Output Ripple & Noise < 30mV
Transient Tolerance = 500mV
TDC = 2.9A
Max current = 2.9A
Over-Current Protection(Max Rating × 1.5) = 4.35A
Slew Rate = 2.5A/us
Work Frequency = 300kHZ
Efficiency > 90% @TDC

Design specification

P3V3_STBY

Output Voltage = 3V3±5%
Output Ripple & Noise < 30mV
Transient Tolerance = 330mV
TDC = 8.2A
Max current = 8.2A
Over-Current Protection(Max Rating × 1.5) =12.3A
Slew Rate = 2.5A/us
Work Frequency = 355kHZ
Efficiency > 90% @TDC



VR P5V_STBY & P3V3_STBY

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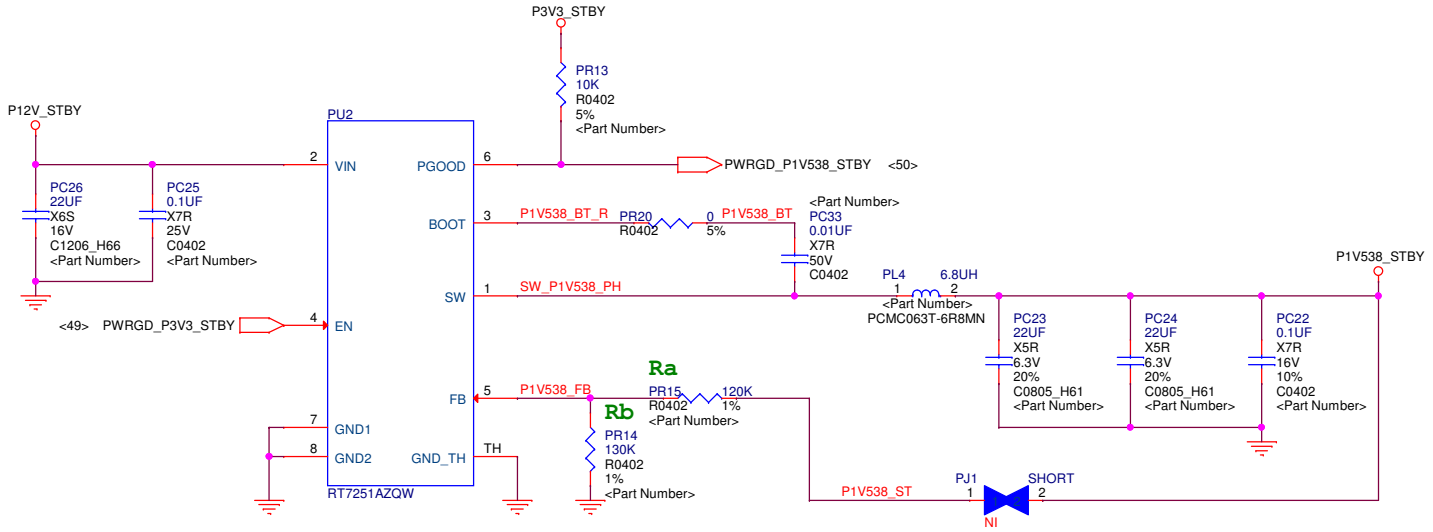
Design Specification

P1V538_STBY

Output Voltage = 1V538±5%
Output Ripple & Noise < 30mV
Transient Tolerance = 155mV
TDC = 1.22A
Max current = 1.22A
Over-Current Protection(Max Rating × 1.5) =1.83A
Slew Rate = 2.5A/us
Work Frequency = 340kHZ
Efficiency > 90% @TDC

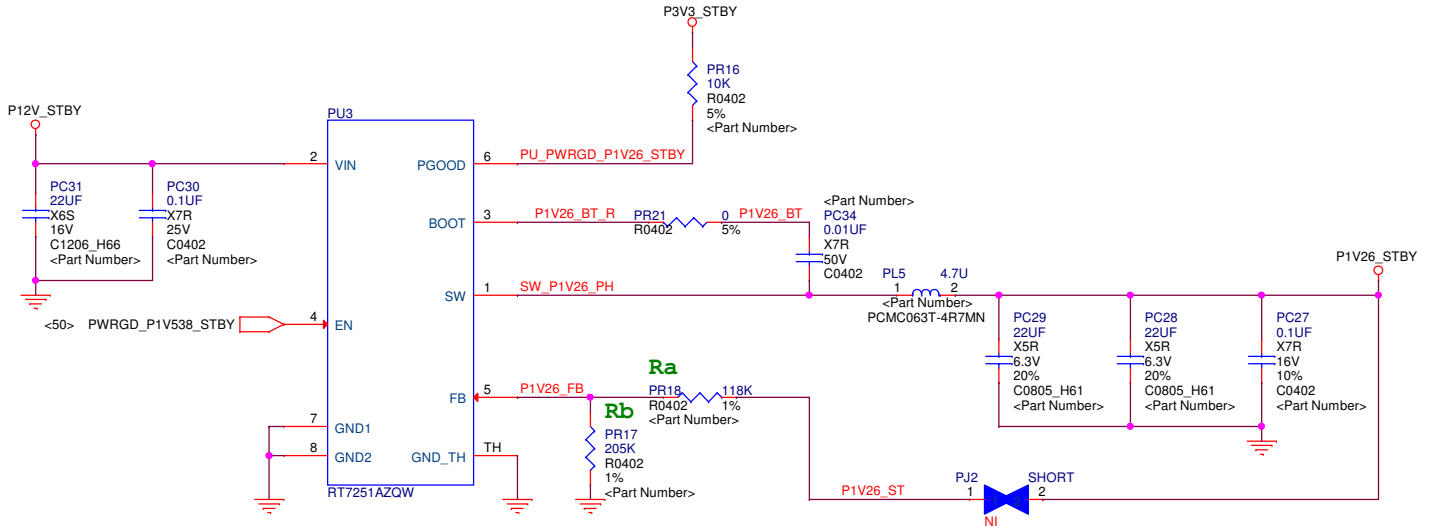


VOUT=0.8(1+Ra/Rb)=1.538V

Design Specification

P1V26_STBY

Output Voltage = 1V26±5%
Output Ripple & Noise < 30mV
Transient Tolerance = 126mV
TDC = 0.77A
Max current = 0.77A
Over-Current Protection(Max Rating × 1.5) =1.16A
Slew Rate = 2.5A/us
Work Frequency = 340kHZ
Efficiency > 90% @TDC



VOUT=0.8(1+Ra/Rb)=1.26V

VR P1V538_STBY & P1V26_STBY

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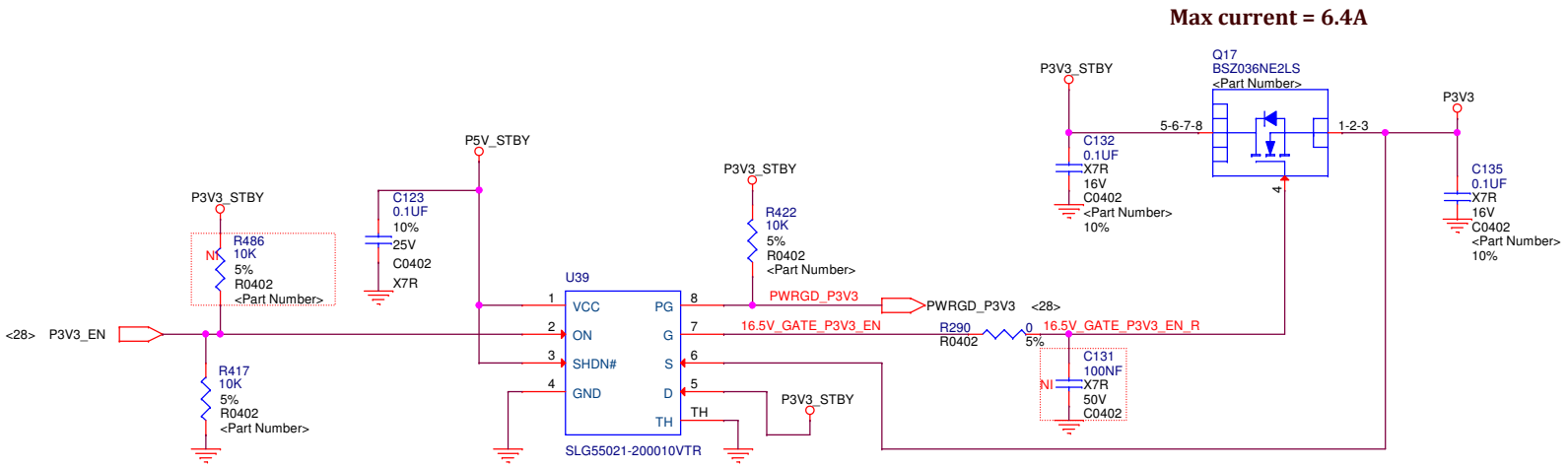

P3V3 Power Switch

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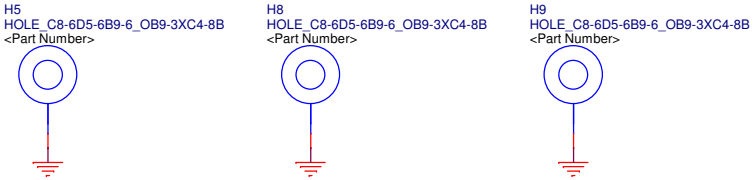
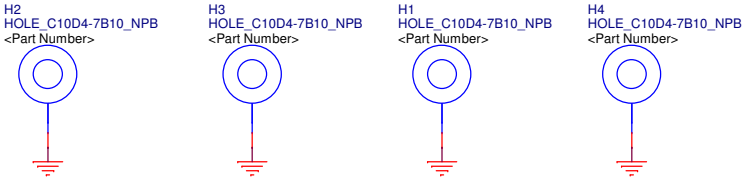
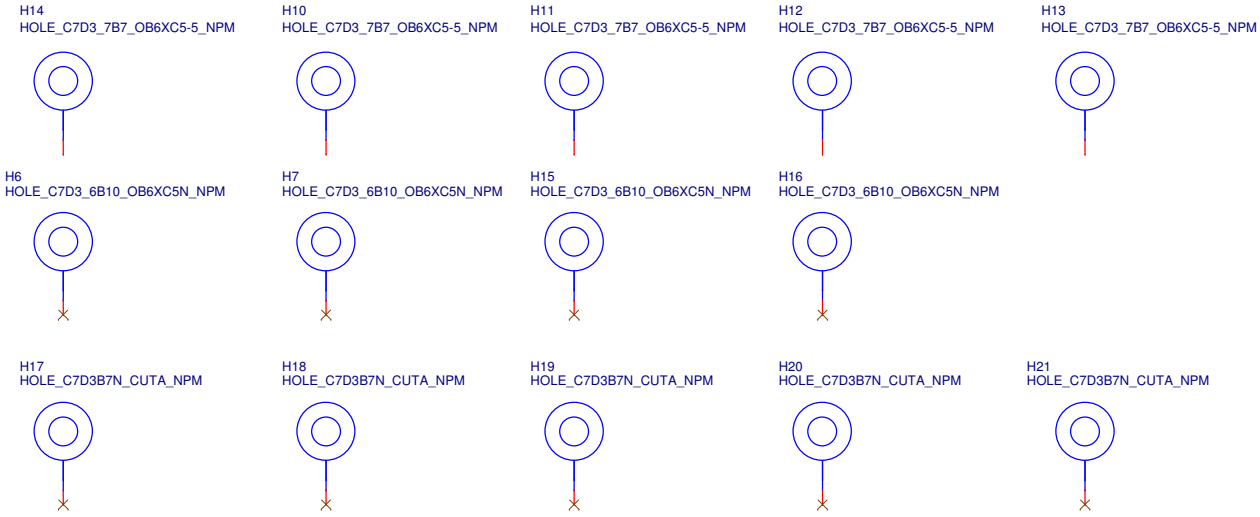
SMT THUMB SCREW * 3pcs



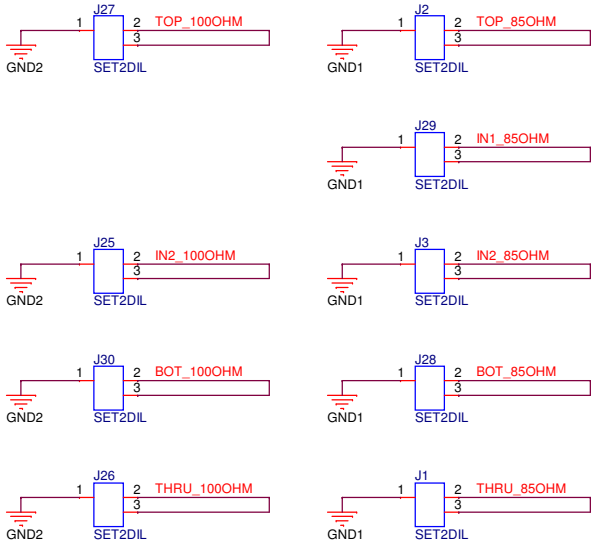
SMT NUT * 4pcs



Key Holes * 14pcs



SET2DIL



Mechanical

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