Lightning

Re-timer Card

PCB P/N: 15702

Version: 1

Project Code: BPD00Q010001

Layer: 8Layers

Board Number:	15702-1A
Project name:	Lightning_PMC
Model Name:	Retimer Card
Layer Count:	8 Layer
Date:	2016/5/12
Material:	TU863+VLP / NPG171+VLP
Green factor/Surface treatment/Tg:	Halogen-Free/ OSP/Tg>170
Customer:	XXXXX
EE engineer	Dennis Jang
SI Engineer	Scott Lee

Version: 01

Layer		Cu oz	Thickness Wiwynn	Glass/Copper Style	Er Wiwynn		Df(1G)
	Mask		0.5		3.4		0.025
Top	Signal	0.5 oz+plating	2.1				
	Prepreg		3		3.9		0.009
L2	GND	1 oz	1.3				
	Core		4		3.9		0.009
L3	Signal	1 oz	1.3				
	Prepreg		16		4.5		0.009
L4	GND	1 oz	1.3				
	Core		4		3.9		0.009
L5	GND	1 oz	1.3				
	Prepreg		16		4.5		0.009
L6	Signal	1 oz	1.3				
	Core		4		3.9	0	0.009
L7	GND	1 oz	1.3				
	Prepreg		3		3.9	0	0.009
Bottom	Signal	0.5 oz+plating	2.1				
	Mask		0.5		3.4	0	0.025
Thickness requirement: 1.6 +8.5% / -10% mm		mil	63				
		mm	1.60				

Single Ended Type(mil)

	Imp Variation	50 Inner/Outer+/-5ohm			
	Bus	MISC.			
	Type	SE			
	Layers	1,3,6,8			
		Wiwynn			
		Width	Imp	Width	Imp
S1		4.75(L2)	50.46		
P2		reference layer			
S3		4.75(L2/L4)	49.57		
P4		reference layer			
P5		reference layer			
S6		4.75(L5/L7)	49.57		
P7		reference layer			
S8		4.75(L7)	50.46		

Differential Type(mil)

	Imp Variation	85 Inner/Outer+/-10%					
	Bus	PCIe / CLK / USB					
	Type	DP					
	Layers	1,3,6,8					
		Wiwynn					
		Width	Space	Imp	Width	Space	Imp
S1		5.38(L2)	6.2	85.36			
P2		reference layer					
S3		5.25(L2/L4)	7.5	85.23			
P4		reference layer					
P5		reference layer					
S6		5.25(L5/L7)	7.5	85.23			
P7		reference layer					
S8		5.38(L7)	6.2	85.36			

Wiwynn
8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist.,
New Taipei City 22102, Taiwan (R.O.C.)
H/W R&D Dept. II

Title: COVER_PAGE

Size: A3 | Document Number: Lightning_Re-timer_Card | Rev: 1

Date: Thursday, October 27, 2016 | Sheet 1 of 24

LIGHTNING RE-TIMER CARD

Approvals

REV	DATE	Reviewer	DESCRIPTION
V01	2016/10/19	Eric YH Yang	First review

Contents

NET NAME

<Routing Class>_{Trace Width}_<Domain>_<Sub-domain>_<{#}Signal Name{DP/DN}>

Note that <Field> is ,andatory field, wheraeas {Field} is optional field

Field : Description on Field :

Routing Class : Define the impedance, single end or differential, and the length tolerance to the net

ZDEF: Default impedance refer to the board stackup of single end signals

Z50: 50 ohm impedance of single end signals

D85: 85 ohm impedance of differentail end signals

BREAK: Traces should be as short as possible

Trace Width :Specify the trace width if necessary

W10: 10 mils trace width

Domain: Nets belong to specific ASIC or component

LEOPARD : LEOPARD's domain

Retimer : Retimer's domain

Mini SAS : Mini SAS HD connector's domain

CONN : Connect to connector

Sub-domain:BMC and SOC's specific interface

I2C : I2C bus

100M : 100M clock signal

PCIE : PCIE bus

TX: Transmitter signal

RX: Receiver signal

{#} Signal Name{DP/DN} : '#' only for low-active signals

'DP/DN' only for differentail pairs

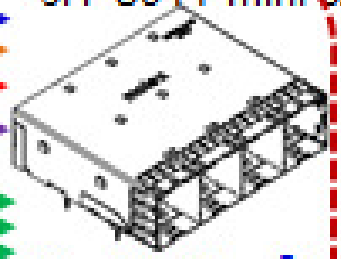
PWRBTN#: low-active of power button

DN: Negative half of a differentail

Wiwynn
8F,90,Sec. 1,Hsin Tai Wu Rd,
New Taipei City 22102, Taiwan (R.O.C.)
H/W R&D Dept. II

Title		
COVER PAGE		
Size: A3	Document Number: Lightning_Re-timer_Card	Rev: 1
Date: Thursday, October 27, 2016	Sheet 2 of 24	

Re-timer Card



SFF-8644 mini SAS HD

To PEB of Lightning

SFF-8644 to SFF-8644 cable

USB cable

12V

VR

1.0V / 1.8V

IDT
89HT0832PZCHLG8
20 x 13 mm

4*PCIe x4

4x I2C

4x PERST_N

4x USB2.0

I2C

PERST_N

USB CONN

USB

USB Hub

4x USB2.0

4*PCIe x4

CLK Buffer

4* 100MHz

Leopard

USB CONN

USB2.0

PCH WELLSBURG

100MHz

CLK Buffer

100MHz

PLTRST_N

CPLD

RST_PERST0_N

PCIE X24 Slot

PCIe x24

I2C

PCIe x24

CPU0 Broadwell EP

BMC AST1250

PCIe x16 GF

Riser Card

100MHz

I2C

PERST_N

PCIE X16 Upper Slot

PCIe x16

100MHz

PCIE X8 Lower Slot

PCIE X8

PCIE X16

PCIE X24 Golden Finger

I2C

I2C

I2C Switch PCA9540B

I2C

I2C

100MHz

PERST_N

wiwynn	Wiwynn 8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist., New Taipei City 22102, Taiwan (R.O.C.) *H/W R&D Dept. II*	
Title	System BLOCK DIAGRAM	
Size A3	Document Number Lightning_Re-timer_Card	Rev 1
Date: Thursday, October 27, 2016	Sheet 3 of 24	

TABLE OF CONTENTS

562R2F- GP
562 = 562 ohm, (2K2R means 2.2K ohm)
2 = size 0402
F = 1% tolerance
GP= Green Part (RoHS)
Wiwynn RC size code as below:
1 = 0201
2= 0402
3= 0603
5= 0805
6= 1206
Wiwynn R tolerance code as below:
D=0.5%
F= 1%
J= 5%

SCD1U10V2KX-5GP
D1U = 0.1uF (2D2U means 2.2uF)
10Voltage (6D3V means 6.3V)
2 = size 0402, K tolerance
K=tolerance
[Wiwynn C code as below:]
G=2%
J=5%
K=10%
M=20%
X=temp characteristics
[Wiwynn C Series/Temp]
N=NPO
X=X7R/X5R
Y=Y5V
-5=different symbol/customer
GP= Green Part (RoHS)

Wiwynn
8F,90,Sec. 1,Hsin Tai Wu Rd,
New Taipei City 22102, Taiwan (R.O.C.)
H/W R&D Dept. II

Title: TABLE OF CONTENTS

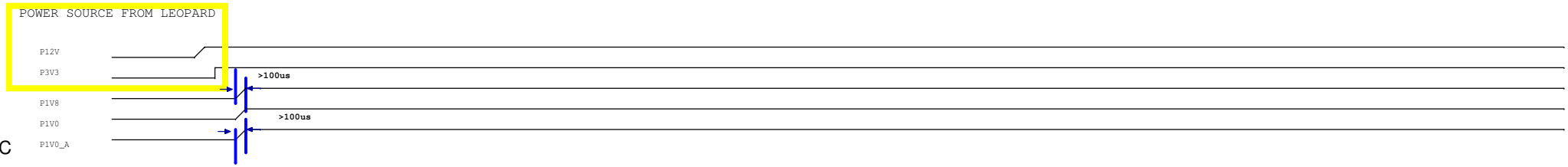
Size: A3 | Document Number: Lightning_Re-timer_Card | Rev: 1

Date: Thursday, October 27, 2016 | Sheet 4 of 24

The T0832P has no power sequencing requirements between any of its power rails (VDD, VDDA, VDD18, VDD3).

VDDA and VDD18 require ramp times greater than 100µs.

VDD3 can operate at 1.8V to 3.3V, and I/O pins referenced to it, as described below, must not exceed the VDD3 level.

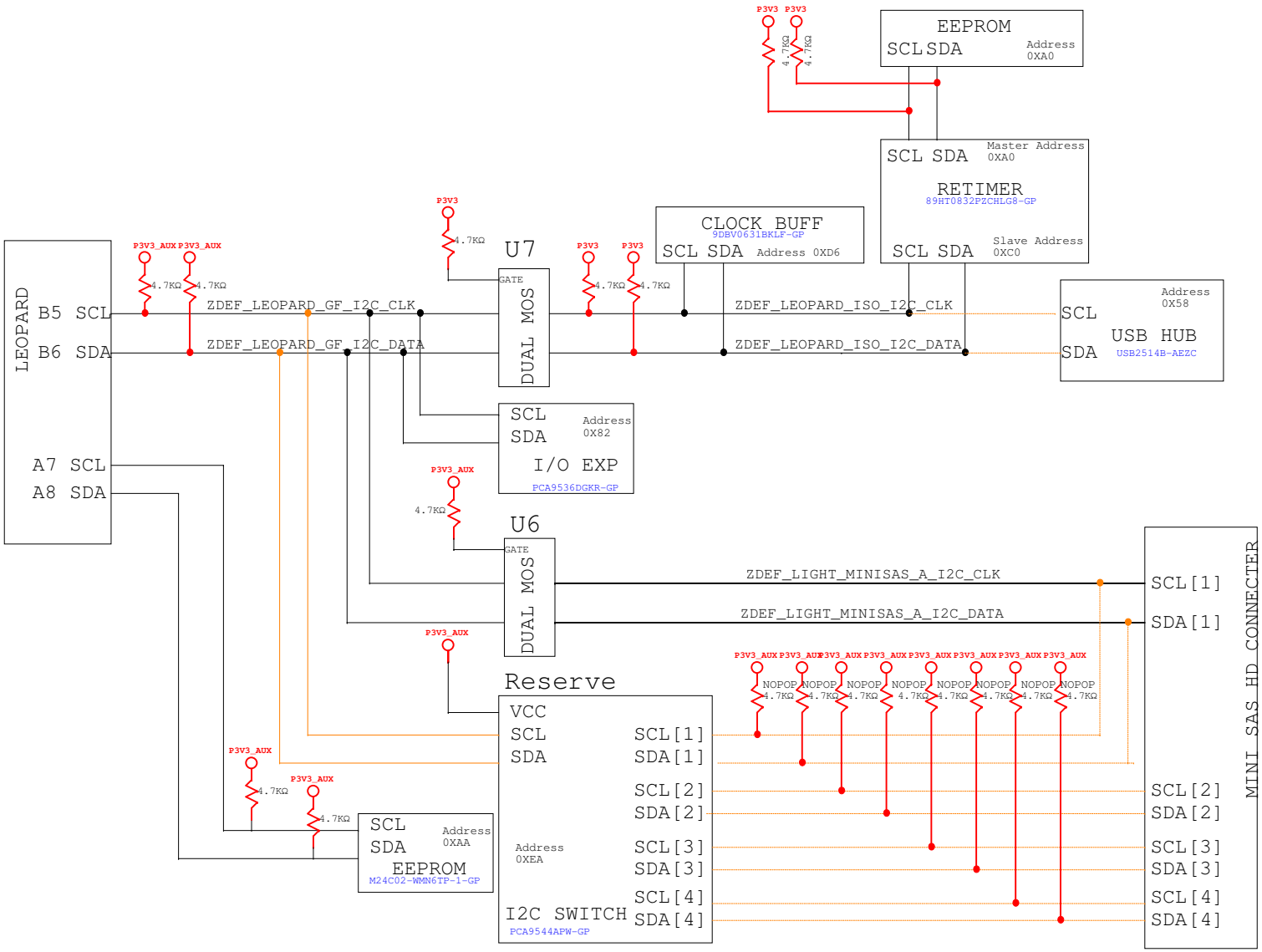


Wiwynn
8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist.,
New Taipei City 22102, Taiwan (R.O.C.)
H/W R&D Dept. II

Title: Power Sequence

Size: A3 | Document Number: Lightning_Re-timer_Card | Rev: 1

Date: Thursday, October 27, 2016 | Sheet 5 of 24



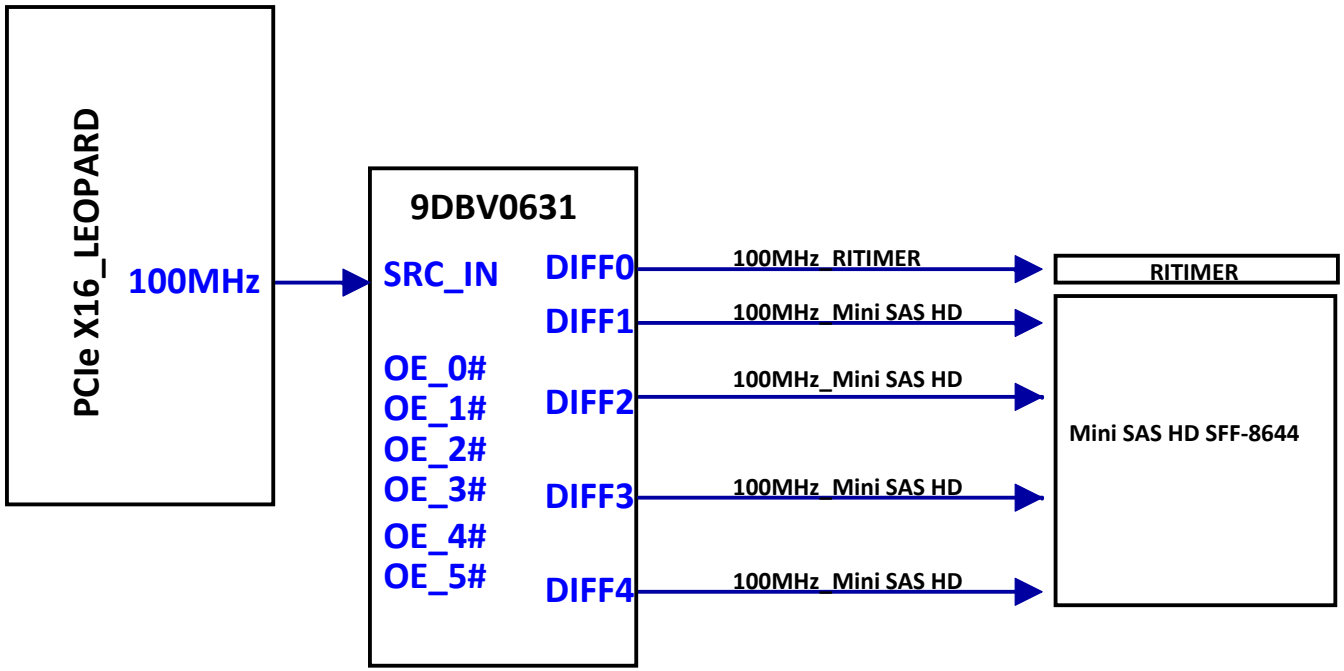
wiwynn

Wiwynn
8F, 99, Sec.1, Xintai 5th Rd., Xizhi Dist., New Taipei City 22102, Taiwan (R.O.C.)
MW R&D Dept. II

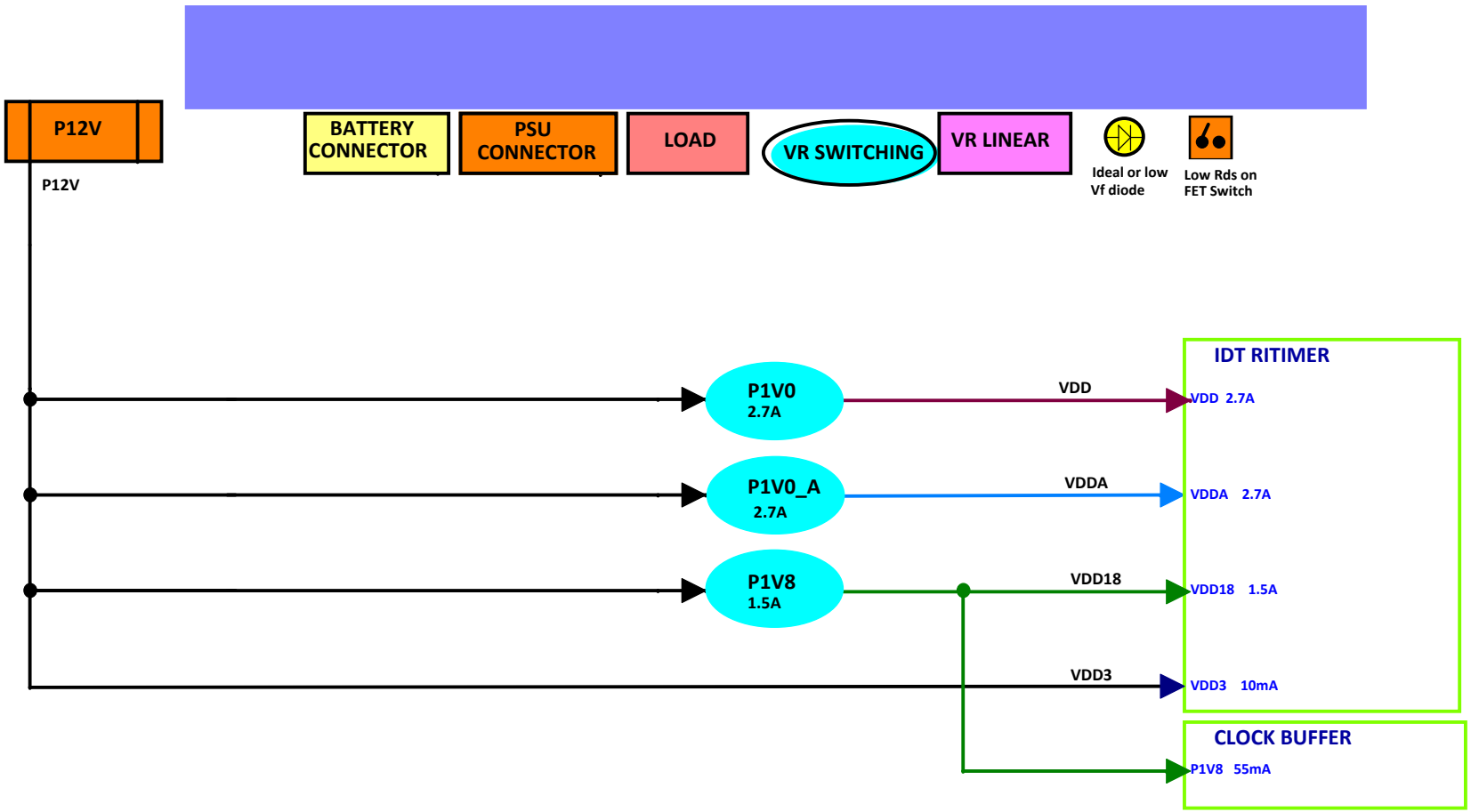
Title: I2C_Topology

Size: A1 | Document Number: Lightning_Re-timer_Card | Rev: 1

Date: Thursday, October 27, 2016 | Sheet 6 of 24



Wiwynn	8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist., New Taipei City 22102, Taiwan (R.O.C.)	
	HW R&D Dept. II	
Title: CLOCK_TREE		
Size: A3	Document Number: Lightning_Re-timer_Card	Rev: 1
Date: Thursday, October 27, 2016	Sheet 7 of 24	



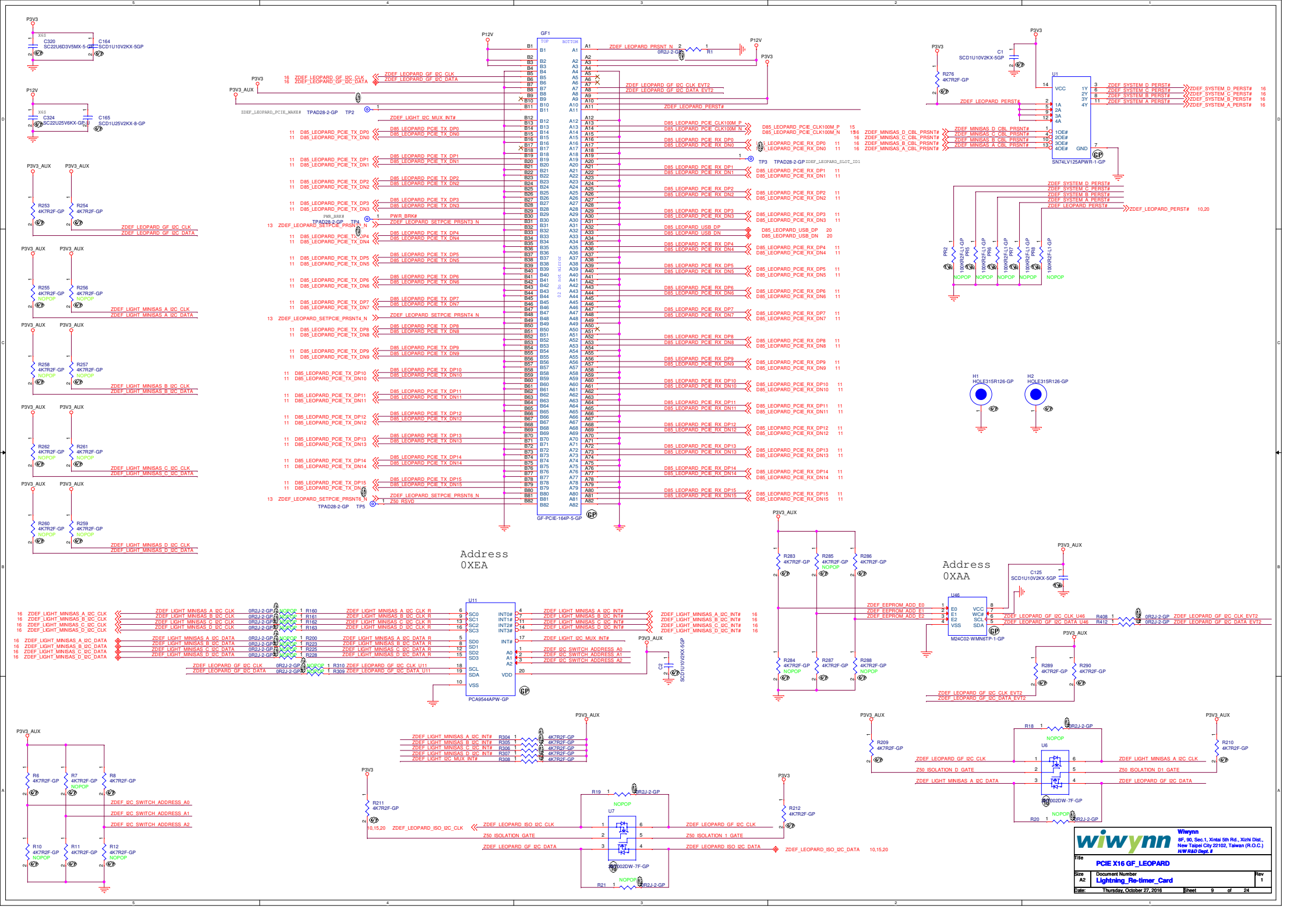
IDT 89HT0832PZCHLG8 Power Consumption		
Power Rail	Current	Power (W)
VDD – 1.0V	2.7 A	2.835 W
VDDA – 1.0V	2.7 A	2.835 W
VDD18 – 1.8V	1.5 A	2.97 W
VDD3 – 3.3V	10 mA	0.036 W
Total		8.676 W

Wiwynn
8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist.,
New Taipei City 22102, Taiwan (R.O.C.)
H/W R&D Dept. II

Title: POWER DISTRIBUTION DIAG

Size: A3 | Document Number: Lightning_Re-timer_Card | Rev: 1

Date: Thursday, October 27, 2016 | Sheet 8 of 24


Address
0XEA
Address
0XAA
GF1
GF-PCIE-164P-5-GP
U11
PCA9544APW-GP
U1
SN74LV125APWR-1-GP
U46
M24C02-WMN6TP-1-GP
U6
U7
002DW-7F-GP
H1
HOLE315R126-GP
H2
HOLE315R126-GP
P3V3
P12V
P3V3_AUX
ZDEF_LEOPARD_GF_I2C_CLK
ZDEF_LEOPARD_GF_I2C_DATA
ZDEF_LIGHT_I2C_MUX_INT#
ZDEF_LEOPARD_PERST#
ZDEF_LEOPARD_ISO_I2C_CLK
ZDEF_LEOPARD_ISO_I2C_DATA
ZDEF_I2C_SWITCH_ADDRESS_A0
ZDEF_I2C_SWITCH_ADDRESS_A1
ZDEF_I2C_SWITCH_ADDRESS_A2
Wiwynn
8F., 88, Sec.1, Xintai 5th Rd., Xizhi Dist.,
New Taipei City 22102, Taiwan (R.O.C.)
H/W R&D Dept. #
PCIE X16 GF_LEOPARD
Size A2
Document Number
Lightning_Re-timer_Card
Rev 1
Date: Thursday, October 27, 2016
Sheet 9 of 24

Master Address
0XA0

Slave Address
0XC0

Bit	Slave I2C Address	Master I2C Address
1	SI2C_ADDR[1]	MI2C_ADDR[1]
2	SI2C_ADDR[2]	MI2C_ADDR[2]
3	SI2C_ADDR[3]	MI2C_ADDR[3]
4	0	MI2C_ADDR[4]
5	SI2C_ADDR[5]	1
6	1	0
7	1	1

MI2C_SMODE	I	Master I²C Slow Mode. This signal is used to indicate the speed of the master I²C interface: high for 100KHz, low for 400KHz.
MI2C_EESIZE	I	Master I²C EEPROM Size. This signal is used to indicate the size of external EEPROM: Low for small EEPROM, i.e., single byte addressing, 16Kbits or smaller High for large EEPROM, i.e., dual byte addressing, 32Kbits or larger
INVPR_N	I	Invert Port Reset, active low. This pin defines the active level for PRTRST[3:0]N. VSS: inverted, PRTRST[3:0]N is active high, ports are reset when these signals are high VDD: normal, PRTRST[3:0]N is active low, ports are reset when these signals are low

Internal 31k pull up

Internal 96k pull up

FOX-CONN10A-S8-GP

89HT0832PZCHLG8-GP

24LC32A-I-SN-GP

Programing Retimer

Debug Retimer

PIN-SCN3-S1-GP

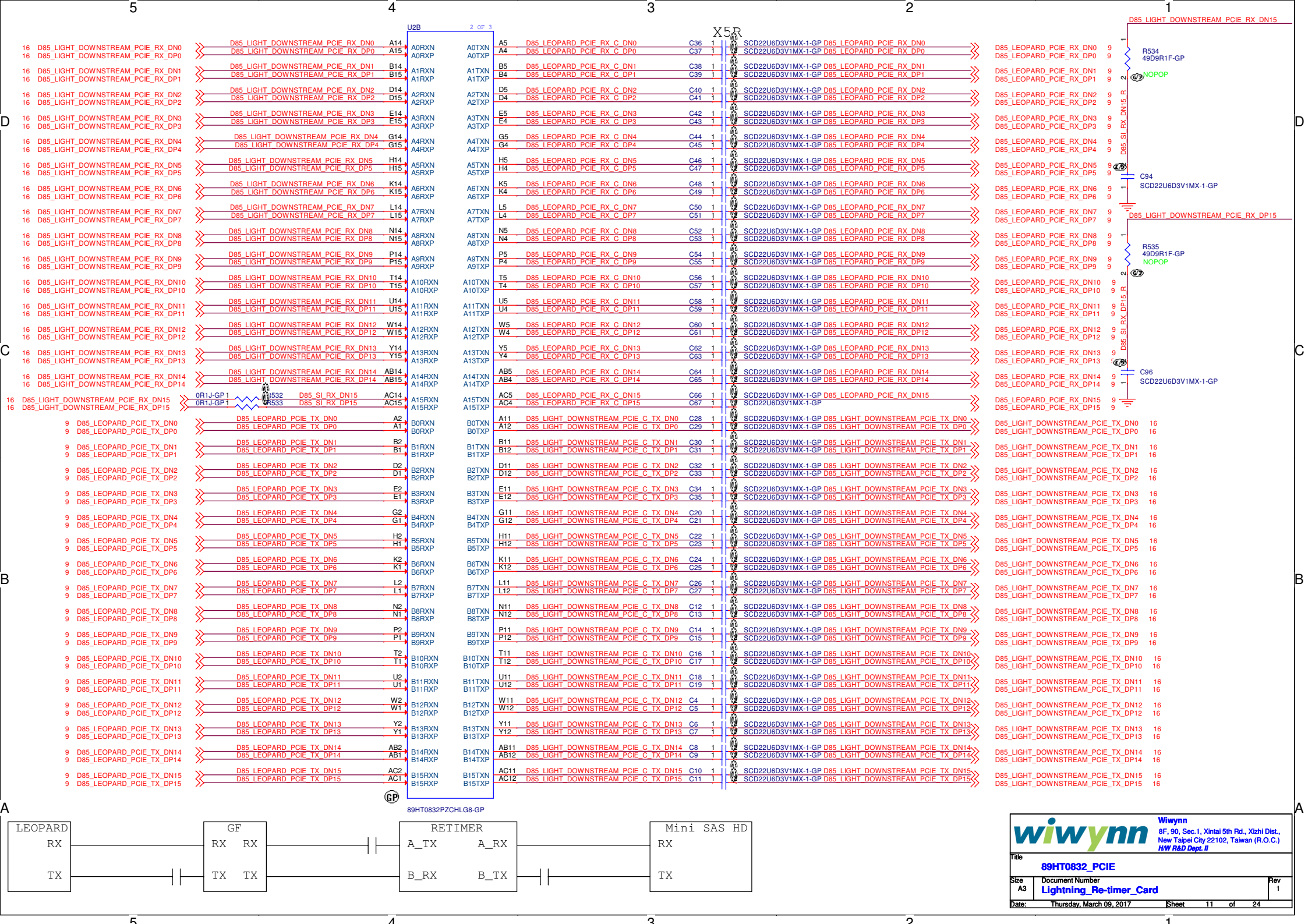
Address
0XA0

Wiwynn
8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist.,
New Taipei City 22102, Taiwan (R.O.C.)
H/W R&D Dept. II

Title: 89HT0832_MISC & I2C_Device

Size: A3 | Document Number: Lightning_Re-timer_Card | Rev: 1

Date: Thursday, October 27, 2016 | Sheet 10 of 24

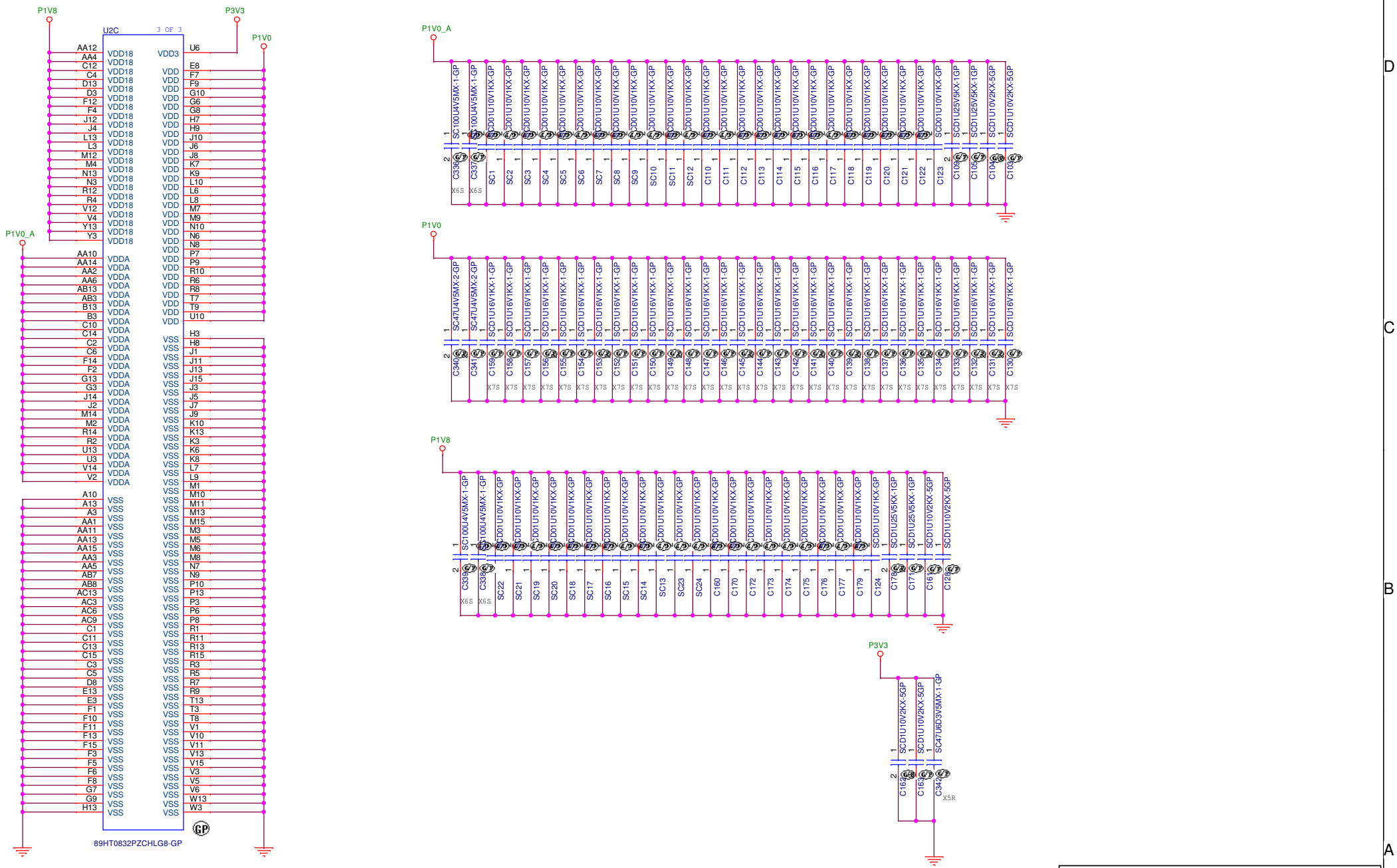


Wiwynn
8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist., New Taipei City 22102, Taiwan (R.O.C.)
H/W R&D Dept. II

Title: 89HT0832_PCIE

Size: A3 | Document Number: Lightning_Re-timer_Card | Rev: 1

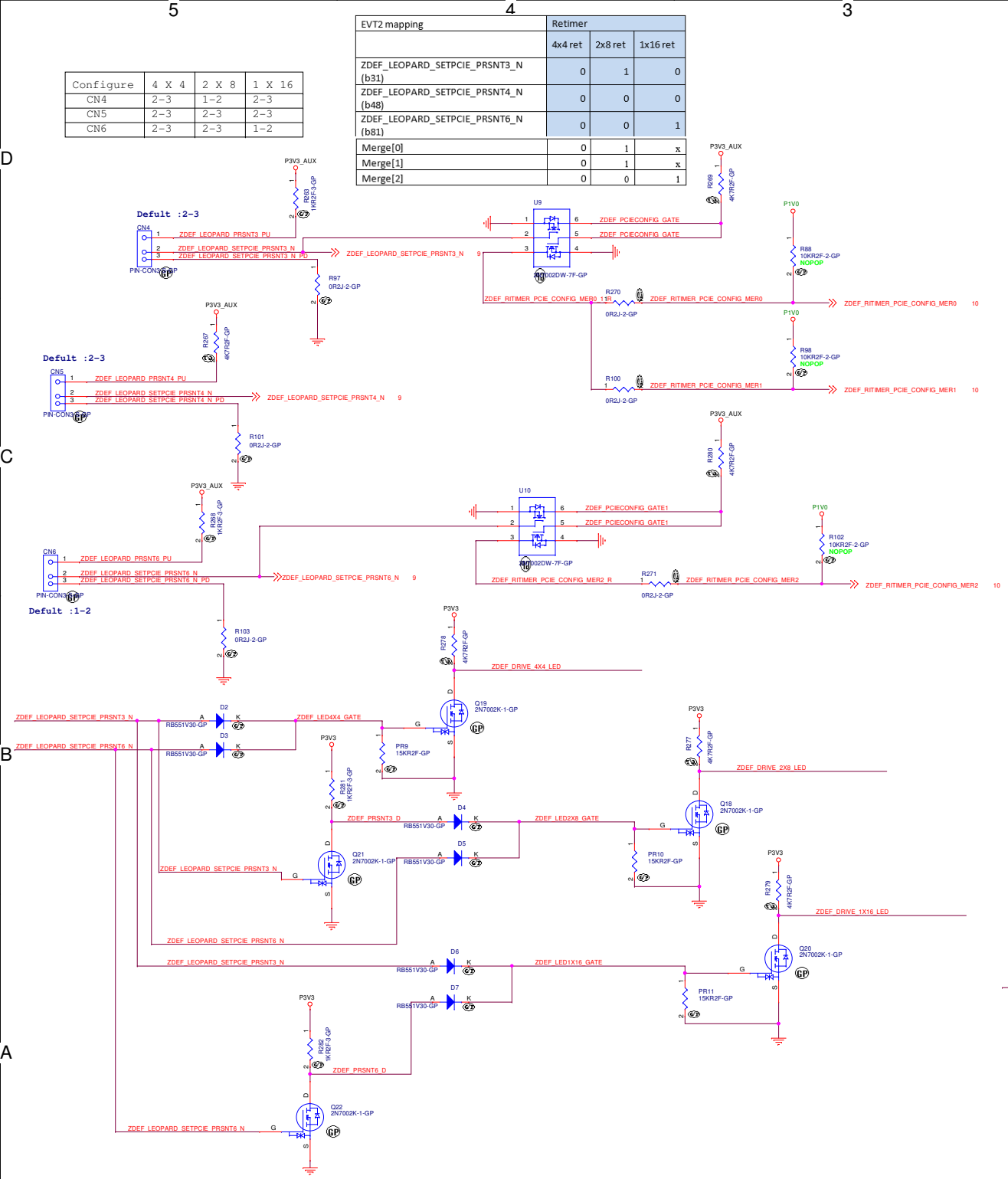
Date: Thursday, March 09, 2017 | Sheet 11 of 24

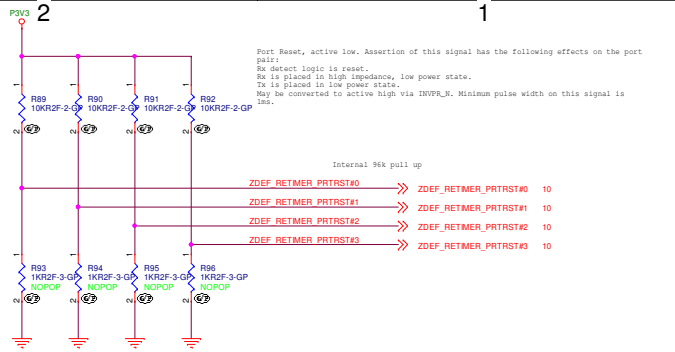


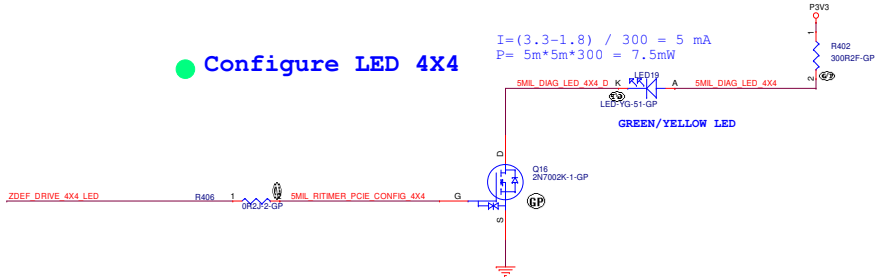
Wiwynn	8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist., New Taipei City 22102, Taiwan (R.O.C.)	
	H/W R&D Dept. II	
Title	89HT0832_Power & GND	
Size A3	Document Number Lightning_Re-timer_Card	Rev 1
Date: Thursday, March 09, 2017	Sheet 12 of 24	

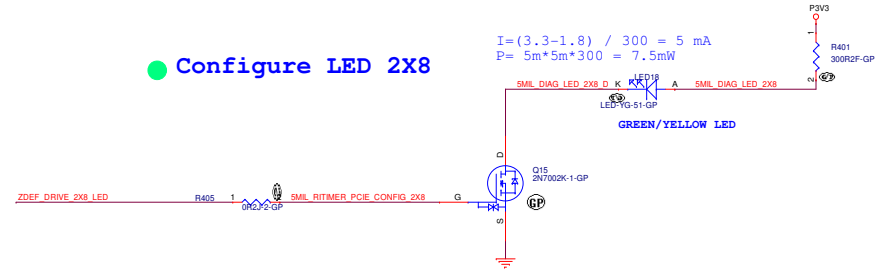
Configure	4 X 4	2 X 8	1 X 16
CN4	2-3	1-2	2-3
CN5	2-3	2-3	2-3
CN6	2-3	2-3	1-2

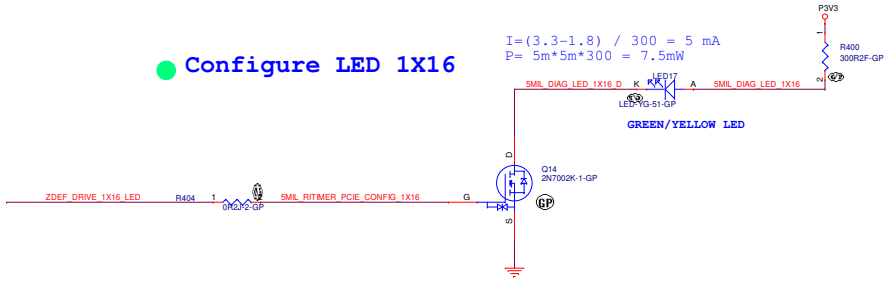
EVT2 mapping	Retimer		
	4x4 ret	2x8 ret	1x16 ret
ZDEF_LEOPARD_SETPCIE_PRSNT3_N (b31)	0	1	0
ZDEF_LEOPARD_SETPCIE_PRSNT4_N (b48)	0	0	0
ZDEF_LEOPARD_SETPCIE_PRSNT6_N (b81)	0	0	1
Merge[0]	0	1	x
Merge[1]	0	1	x
Merge[2]	0	0	1



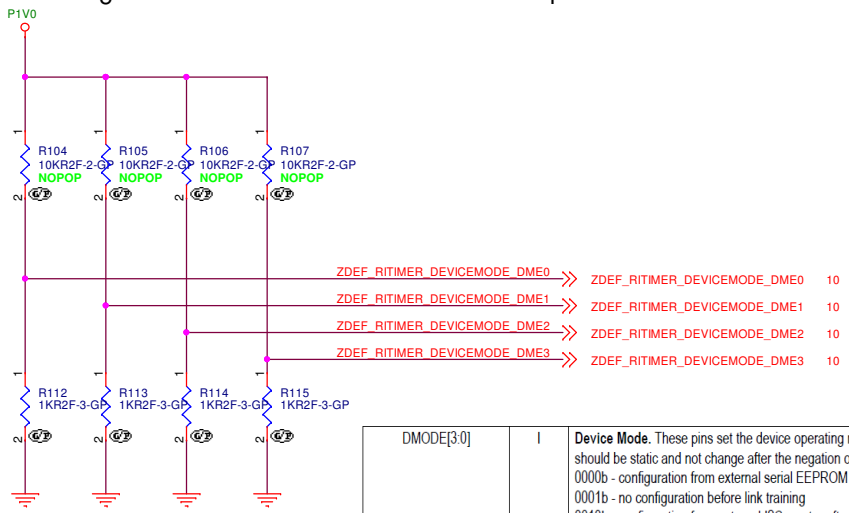




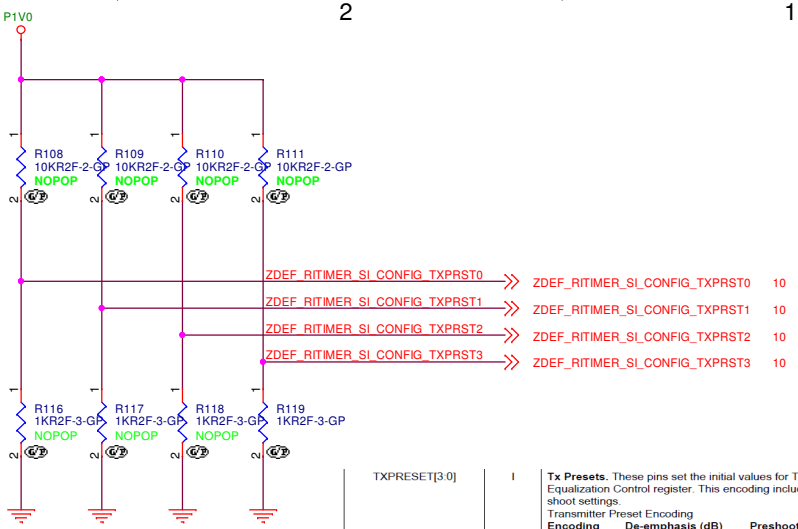




Wiwynn	8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist., New Taipei City 22102, Taiwan (R.O.C.) HW R&D Dept. II
Title	89HT0832_HW_STRAP(1/2)
Size A2	Document Number Lightning_Re-timer_Card
Rev	1
Date: Thursday, October 27, 2016	Sheet 13 of 24

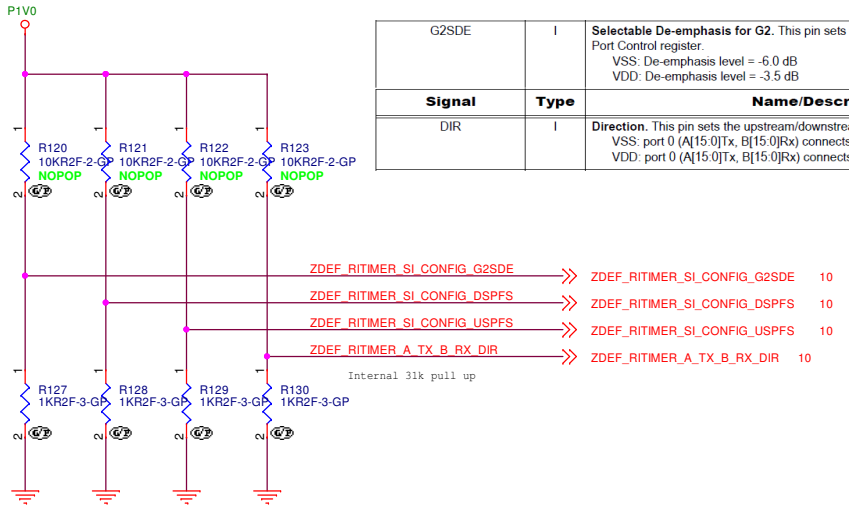


DMODE[3:0]	I	**Device Mode.** These pins set the device operating mode of the T0832P. These pins should be static and not change after the negation of PERSTN. 0000b - configuration from external serial EEPROM 0001b - no configuration before link training 0010b - configuration from external I2C master after power on reset.

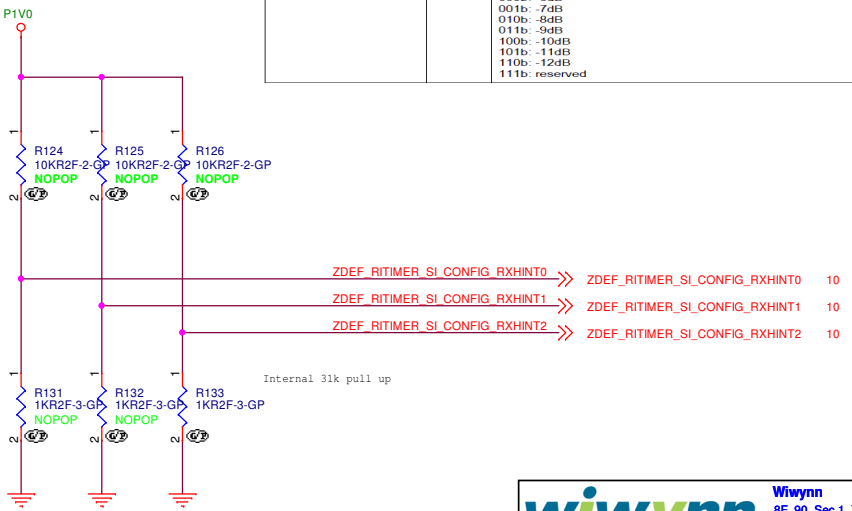


TXPRESET[3:0]	I	**Tx Presets.** These pins set the initial values for Transmitter Presets for the Lane Equalization Control register. This encoding includes both TX de-emphasis and pre-shoot settings. Transmitter Preset Encoding **Encoding** / **De-emphasis (dB)** / **Preshoot (dB)** 0000b: -6 / 0 0001b: -3.5 / 0 0010b: -4.5 / 0 0011b: -2.5 / 0 0100b: 0 / 0 0101b: 0 / 2 0110b: 0 / 2.5 0111b: -6 / 3.5 1000b: -3.5 / 3.5 1001b: 0 / 3.5 1010b: Note 1 / Note 1 1011b — 1111b: Reserved **Note 1**: The Transmitter Preset encoding of 1010b corresponds to the maximum Vtx-boost that the Transmitter advertises with FS and LF in both full swing and reduced swing modes with C_{-1} = 0, and C_{+1} = (FS-LF)/2.

DSPFS	I	**Downstream Port Full Scale.** This pin sets the downstream port(s) full scale output pk-pk differential voltage. VSS: HLEV=1, 1V transmitter differential swing VDD: HLEV=7, 1.3V transmitter differential swing
USPFS	I	**Upstream Port Full Scale.** This pin sets the upstream port(s) full scale output pk-pk differential voltage. VSS: HLEV=1, 1V transmitter differential swing VDD: HLEV=7, 1.3V transmitter differential swin



G2SDE	I	**Selectable De-emphasis for G2.** This pin sets the initial value of the SDE bit in the Port Control register. VSS: De-emphasis level = -6.0 dB VDD: De-emphasis level = -3.5 dB
Signal	**Type**	**Name/Description**
DIR	I	**Direction.** This pin sets the upstream/downstream direction. VSS: port 0 (A[15:0]Tx, B[15:0]Rx) connects to RC, or upstream device VDD: port 0 (A[15:0]Tx, B[15:0]Rx) connects to EP, or downstream device



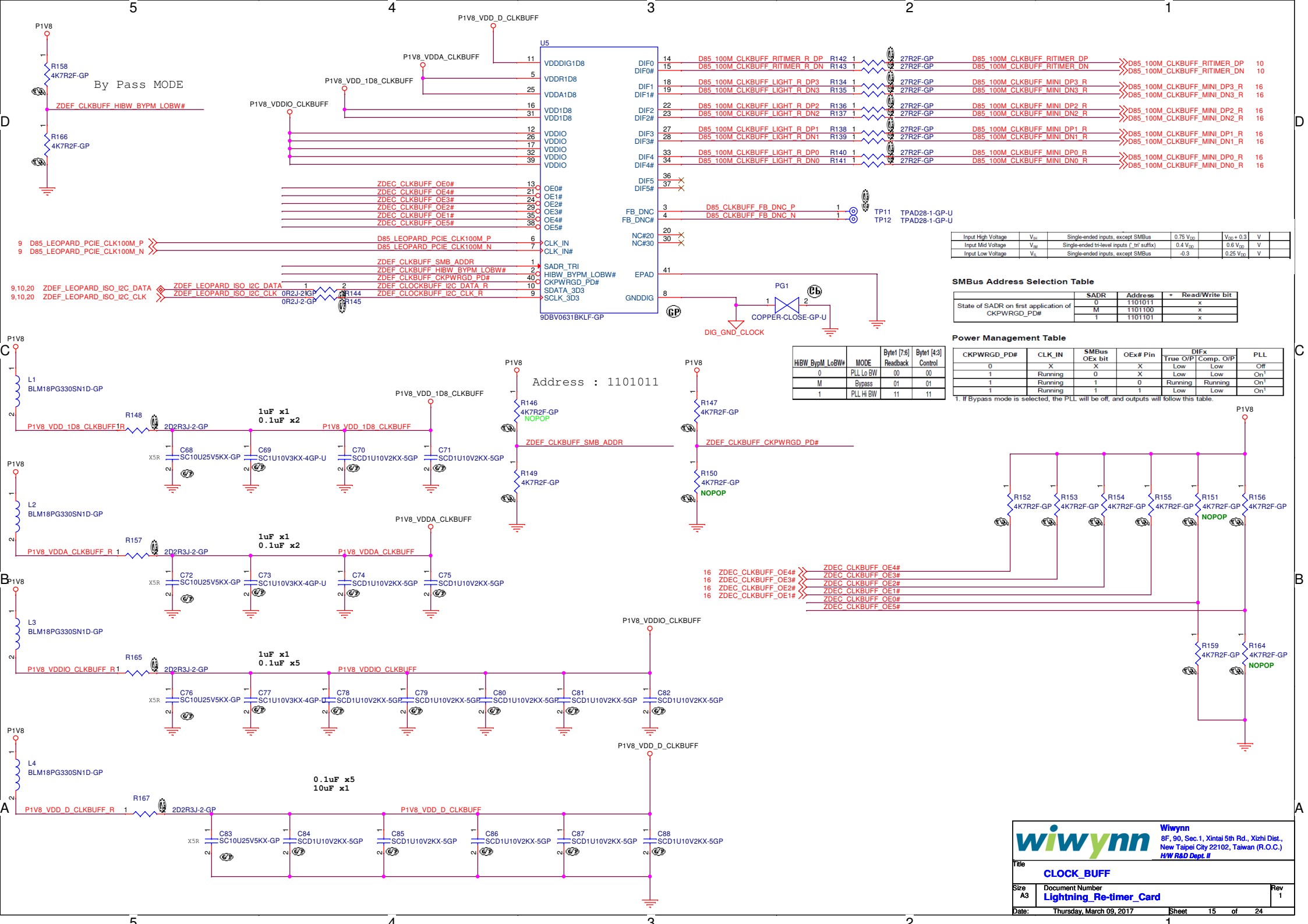
RXHINT[2:0]	I	**Rx Hint.** These pins set the default initial values for Receiver Hint for the Lane Equalization Control register. Receiver equalization values are shown below: 000b: -6dB 001b: -7dB 010b: -8dB 011b: -9dB 100b: -10dB 101b: -11dB 110b: -12dB 111b: reserved

Wiwynn
8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist.,
New Taipei City 22102, Taiwan (R.O.C.)
H/W R&D Dept. II

Title: **89HT0832_HW_STRAP(2/2)**

Size: A3 | Document Number: **Lightning_Re-timer_Card** | Rev: 1

Date: Thursday, October 27, 2016 | Sheet 14 of 24



Input High Voltage	V_{IH}	Single-ended inputs, except SMBus	0.75 V_{DD}		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IM}	Single-ended tri-level inputs ('_tri' suffix)	0.4 V_{DD}		0.6 V_{DD}	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus	-0.3		0.25 V_{DD}	V	

SMBus Address Selection Table

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	x
	M	1101100	x
	1	1101101	x

HiBW_BypM_LoBW#	MODE	Byte1 [7:6] Readback	Byte1 [4:3] Control
0	PLL Lo BW	00	00
M	Bypass	01	01
1	PLL Hi BW	11	11

Power Management Table

CKPWRGD_PD#	CLK_IN	SMBus OEx bit	OEx# Pin	DIFx True O/P	DIFx Comp. O/P	PLL
0	X	X	X	Low	Low	Off
1	Running	0	X	Low	Low	On[1]
1	Running	1	0	Running	Running	On[1]
1	Running	1	1	Low	Low	On[1]

1. If Bypass mode is selected, the PLL will be off, and outputs will follow this table.

Wiwynn
8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist., New Taipei City 22102, Taiwan (R.O.C.)
H/W R&D Dept. II

Title: CLOCK_BUFF

Size: A3 | Document Number: Lightning_Re-timer_Card | Rev: 1

Date: Thursday, March 09, 2017 | Sheet 15 of 24

Lanes from re-timer downstream	MINI SAS HD on Re-timer	MINI SAS HD on PEB	Lanes from PEB upstream
Lane0~Lane3	Port D	Port D	Lane12~Lane15
Lane4~Lane7	Port C	Port C	Lane8~Lane11
Lane8~Lane11	Port B	Port B	Lane4~Lane7
Lane12~Lane15	Port A	Port A	Lane0~Lane3

	EVT PIN DEFINE	DVT PIN DEFINE
A1	REF_CLK_P	REF_CLK_P
A2	REF_CLK_N	REF_CLK_N
B1	PERST#	PERST#
B2	SDA	CBLPRSNT#
C1	SCL	SCL
C2	CBLPRSNT#	SDA
D1	USB_DN	USB_DN
D2	USB_DP	USB_DP

Co-lay

ADD=100001(0x82)

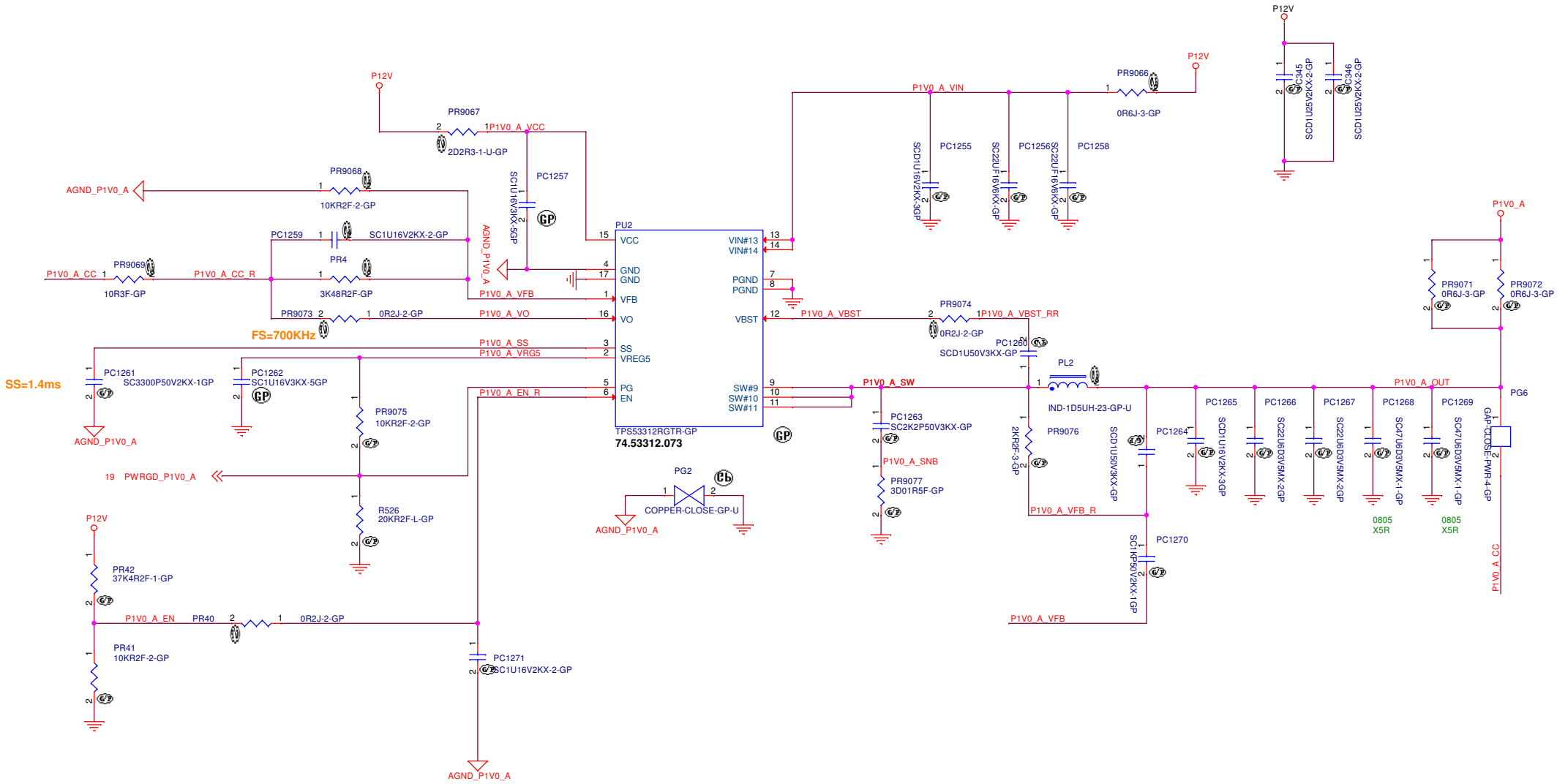
wiwynn	Wiwynn 8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist., New Taipei City 22102, Taiwan (R.O.C.) WW R&D Dept. II

Title: EXT_Mini_SA_HD_CONN

Size: A2 | Document Number: Lightning_Re-timer_Card | Rev: 1

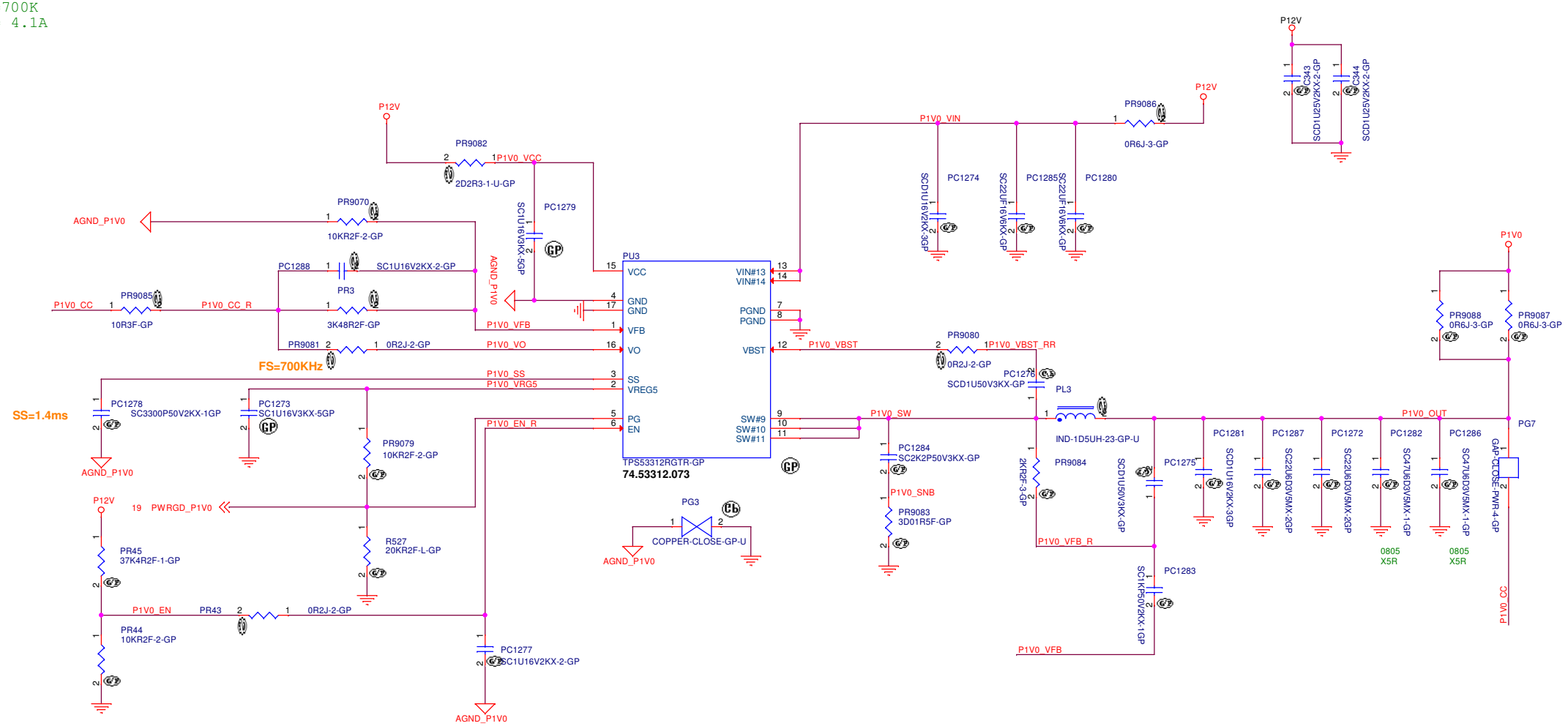
Date: Friday, March 10, 2017 | Sheet 16 of 24

DESIGN NOTE:
VOUT=1V
IOUT=2.7A TDC
IOUT=2.7A MAX
FSW=700K
OCP= 4.1A



wiwynn	Wiwynn 8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist., New Taipei City 22102, Taiwan (R.O.C.) *HW R&D Dept. II*		
Title	P1V0_A		
Size A3	Document Number Lightning_Re-timer_Card		Rev 1
Date: Thursday, March 09, 2017		Sheet 17 of 24	

DESIGN NOTE:
VOUT=1V
IOUT=2.7A TDC
IOUT=2.7A MAX
FSW=700K
OCP= 4.1A



Wiwynn 8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist., New Taipei City 22102, Taiwan (R.O.C.) *H/W R&D Dept. II*		
Title: **P1V0**		
Size: A3	Document Number: **Lightning_Re-timer_Card**	Rev: 1
Date: Thursday, March 09, 2017	Sheet 18 of 24	

DESIGN NOTE:
VOUT=1.8V
IOUT=1.5A TDC
IOUT=1.5A MAX
FSW=700KHz
OCP= 4.1A

FS=700KHz

SS=1.4ms

TPS53312RGTR-GP
74.53312.073

● Power Status LED

Wiwynn	8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist., New Taipei City 22102, Taiwan (R.O.C.)
	H/W R&D Dept. II
Title	P1V8
Size A3	Document Number: Lightning_Re-timer_Card
Rev	1
Date:	Thursday, March 09, 2017
Sheet	19 of 24

USB HUB

ADD=0101100 (0x58)

U14
USB2514B-AEZC-TR-GP-U

Pin	Name	Cable color	Description
1	VCC	Red	+5 VDC
2	D-	White	Data -
3	D+	Green	Data +
4	ID		May be N/C, GND or used as an attached device presence indicator (tied to GND with resistor)
5	GND	Black	Ground

Common chock and RES need to be co-lay

Replace U22's P/N to 075.09904.0A7C

Wiwynn	8F, 90, Sec.1, Xintai 5th Rd., Xizhi Dist., New Taipei City 22102, Taiwan (R.O.C.)
	H/W R&D Dept. II
Title	USB_HUB
Size A3	Document Number: Lightning_Re-timer_Card
Rev	1
Date: Thursday, October 27, 2016	Sheet 20 of 24