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Open Domain Specific Architecture:
The Impact of ODSA

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OPEN
Compute Project

The Impact of Open Domain Specific Architecture (ODSA)

Agenda

- Background on the Open Compute Project
- Open Domain Specific Architecture (ODSA) Sub-Project
- Drivers for Domain Specific Architectures
- Evolution of the industry
- Chiplet and SIP use cases
- Market Opportunity
- ODSA Collaboration

ODSA: Open Domain-Specific Architecture

- Domain-specific architecture: Programmable devices optimized for specific applications or class of applications. Meet the demands of high-intensity workloads in the data center and at the edge – e.g. machine learning, video processing

- Chiplets: Implement an integrated product as a collection of die in a single package, instead of a single die. Each die is a chiplet. Can reduce development and manufacturing costs.

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History of Open Compute Project (OCP)

- In 2009 Facebook, confronting exponential growth, was forced to rethink infrastructure architecture
- Small team of engineers spent next two years re-envisioning and designing software, servers, racks, power supplies, cooling and data center design
- In 2011 Facebook shared it's designs and released them to the public
- Along with Intel, Rackspace, Goldman Sachs and Andy Becholtsheim, the Open Compute Project (OCP) was launched and the Open Compute Project Foundation created
- Today, OCP has grown into a massive global community with over 150 member companies

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ODSA within OCP: A new Server Sub-Project)

- **ODSA organized within the Open Compute Project (OCP):**
  - ODSA aligned as OCP Server sub-project
  - Initial concept brought to OCP by Netronome
  - First silicon focused effort within OCP
- **Extending Moore's Law:**
  - Domain-Specific Architectures: Typically programmable silicon products that accelerate high-intensity workloads (e.g. Tensorflow, Network Processor, Antminer…)
  - Chiplets / SIPs go beyond MCM → Build complex products from multiple die, instead of monolithic devices, to reduce TTM, R&D expense and manufacturing costs.
- **Open Domain-Specific Architecture: An architecture for a domain-specific products**
  - Today: All multi-chiplet products are based on proprietary interfaces
  - Tomorrow: Select best-of-breed chiplets from multiple vendors
  - Incubating a new group, to define a new open interface and standards to build a PoC

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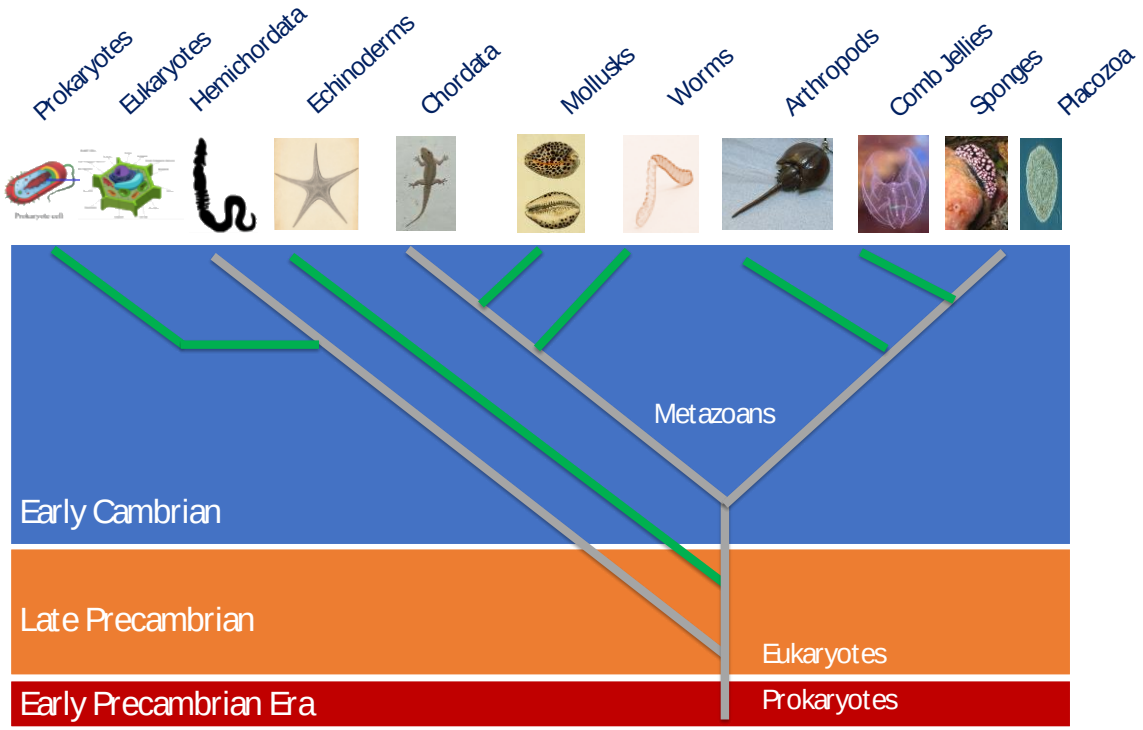
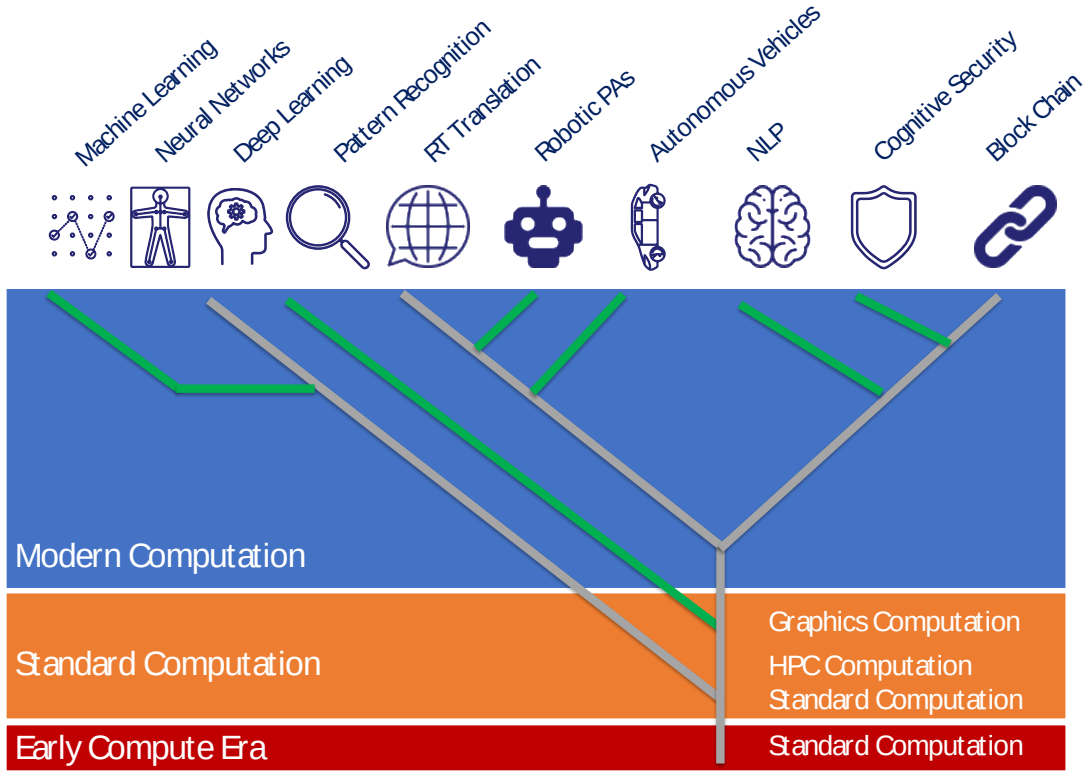
Cambrian Explosion of Workloads



Bio-Diversity Exploded from single cells into multi-cell organisms during the Cambrian explosion; all major phylla were established in this transition



AI and Machine-learning and data-heavy workloads have exploded in past 5 years and will diversify as new applications are discovered constantly…

All images from Creative Commons

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Chiplet and SIP Technology Is Happening Today!

- Many major semiconductor companies have brought to market chiplet / SIP based products
- Developed using hybrid flows of internally developed tools and EDA industry available point solution

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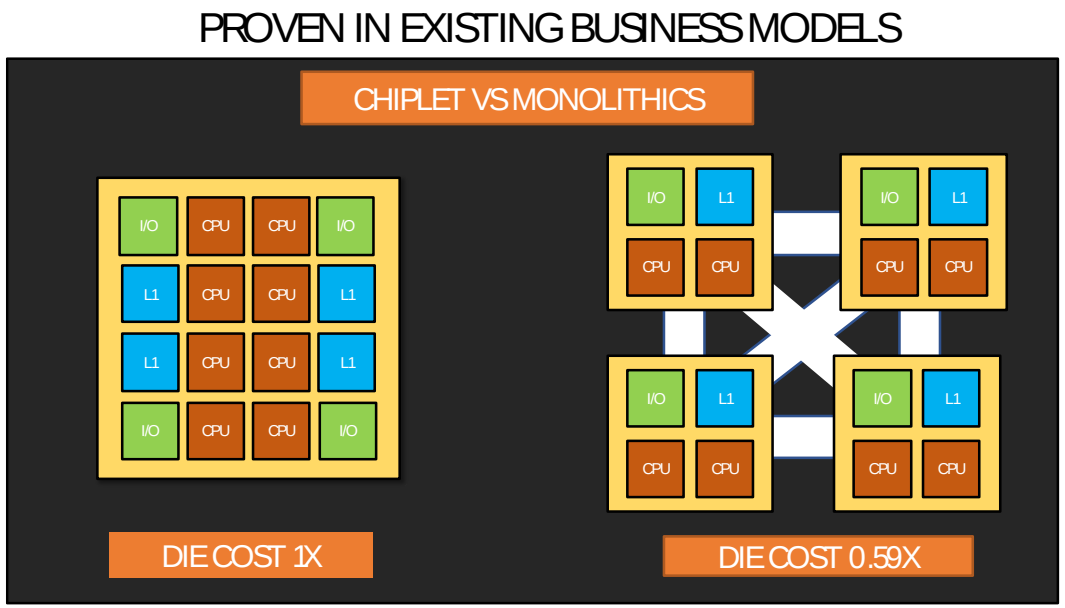
- ODSA seeks to enable internally developed and 3rd party chiplets to be readily integrated
- ODSA seeks to democratize this evolution of chiplet and SIP technology for the larger mass market through an open eco-system marketplace
- Focus on three (3) use cases:
  - IO Disaggregation, Core Disaggregation, System Integration



[L. Su, IEDM'17]

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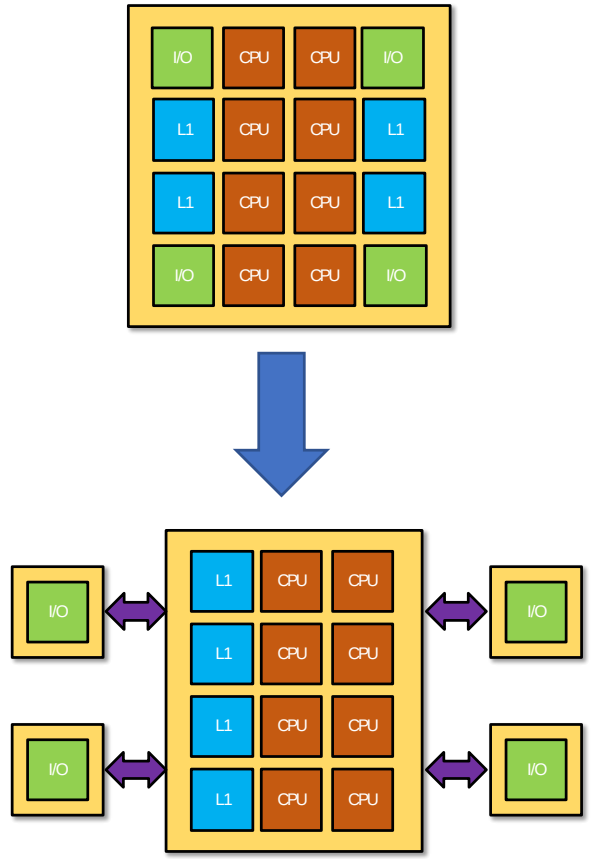
Major Chiplet / System in a Package (SIP) use cases: IO Disaggregation

- **Use case:** IO Disaggregation
- **What:**
  - Separating core and un-core
  - High speed IO Interfaces moved to chiplets
  - Ex: PCIe I/F, Memory I/F, Network I/F
- **Why:**
  - Focus resources on value added core functions
  - Reduce development and qual intervals → shorter TTM
  - PPA: Target IP / Core to process nodes that yield highest Performance, Power, Area for a given function



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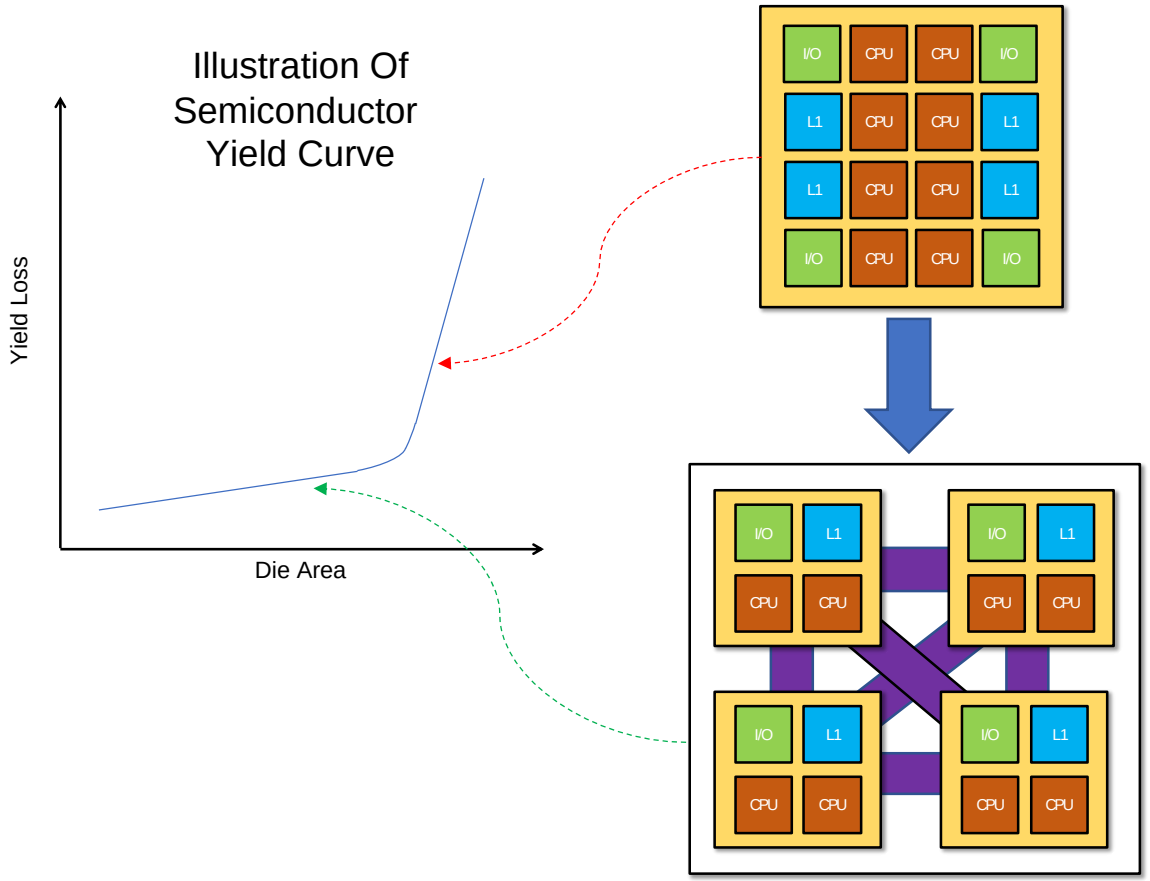
Major Chiplet / System in a Package (SIP) use cases: Logic Disaggregation

- **Use case:** Logic Disaggregation
- **What:**
  - Sub-divide large area of monolithic low yield device into multiple lower area / higher yielding devices
- **Why:**
  - Shift final product from costly, non-linear portion of semiconductor yield curve to lower-cost, higher yielding linear portion



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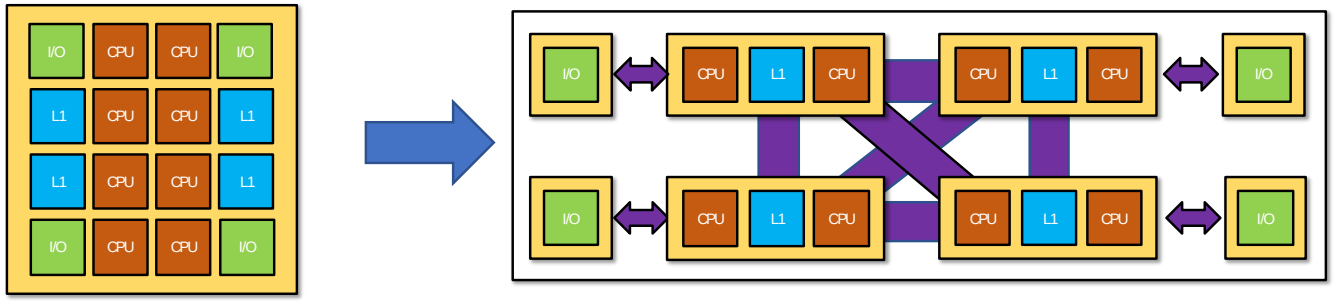
Major Chiplet / System in a Package (SIP) use cases: Combined

- Optimize for process node vs. PPA
  - →Select the best node for the given function
- Maximize yield curve for linear intercepts
- Amortize cost of development and qualification of the chiplets and re-use them for subsequent products
- Combine with known good die chiplets (KGD) from 3rd parties



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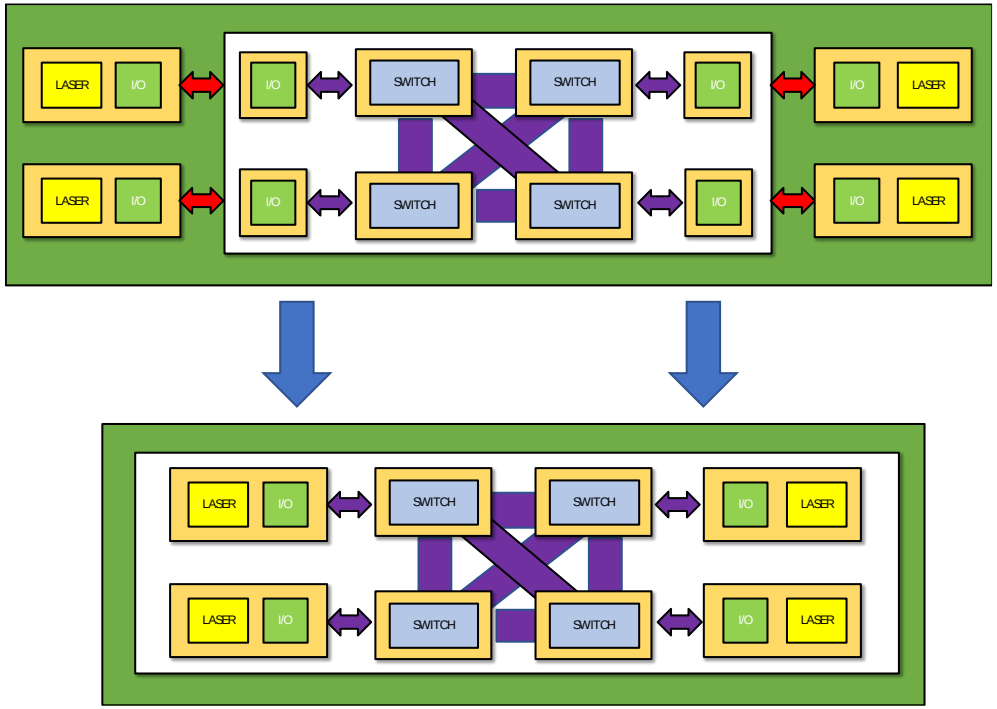
Major Chiplet / System in a Package (SIP) use cases: System Integration

- **Use case:** System Integration
- **What:**
  - Integrate multiple SoCs and components into a single SIP package
  - Obtain KGD from multiple 3rd party suppliers
  - Ex: co-packaged optics and switch
- **Why:**
  - Significant system footprint reduction
  - IO power reduction: driving inches of PCB vs. mm of substrate ➔ mJ → pJ
  - Huge win @ scale: even 5W ~ 10W savings power system adds up to MW savings



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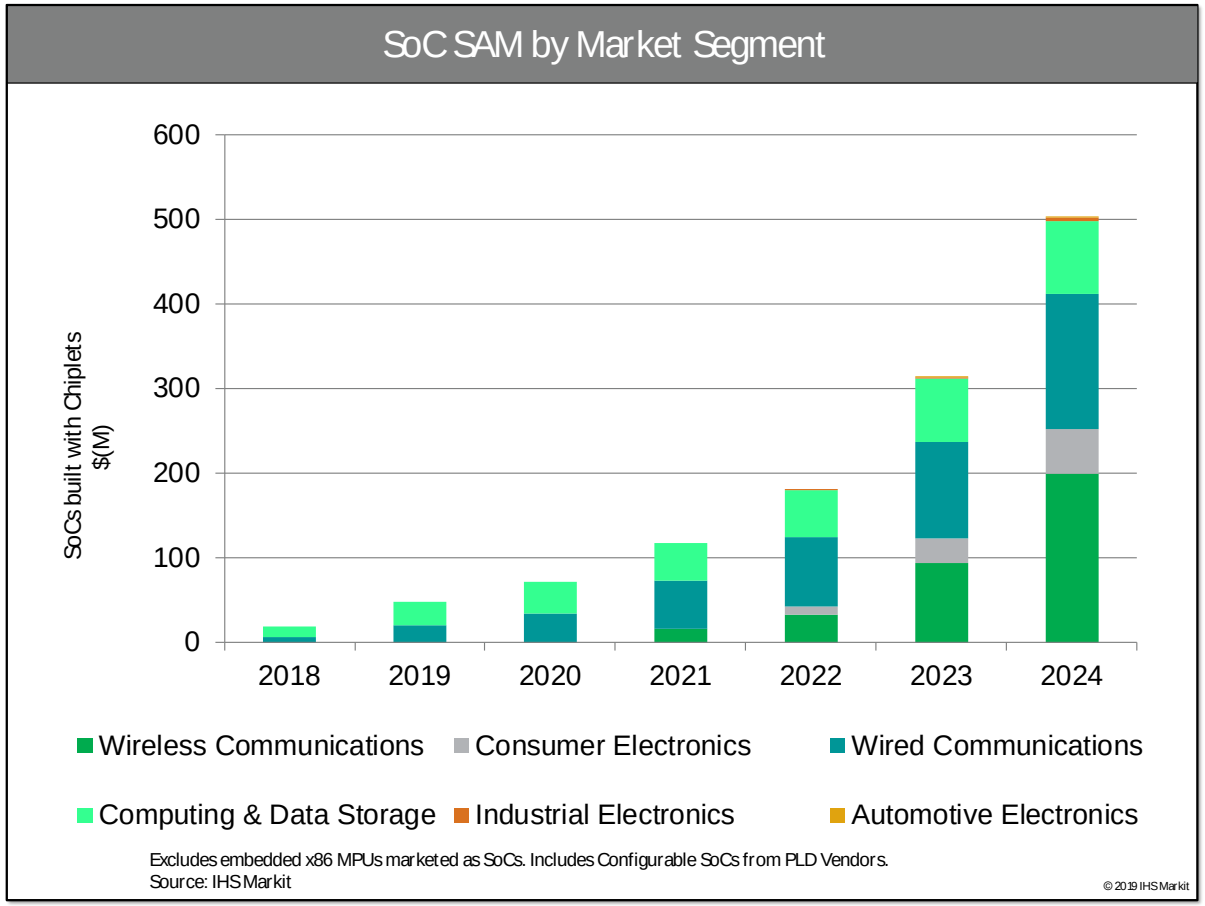
Transformative Market Opportunity: The Tip of the Spear

- Independent research from IHS Markit
- Four (4) segments for chiplets analyzed (SoCs, MPU, GPU, PLD (FPGA/CPLDs)
- Six Verticals (wireless, wireline, consumer, computing, industrial, automotive)

Subset of IHS Markit Data:
- System on a Chip (SoC) segment
- **Conclusion**: Immediate opportunity for chiplets and an open interface

Tip of the spear !!!



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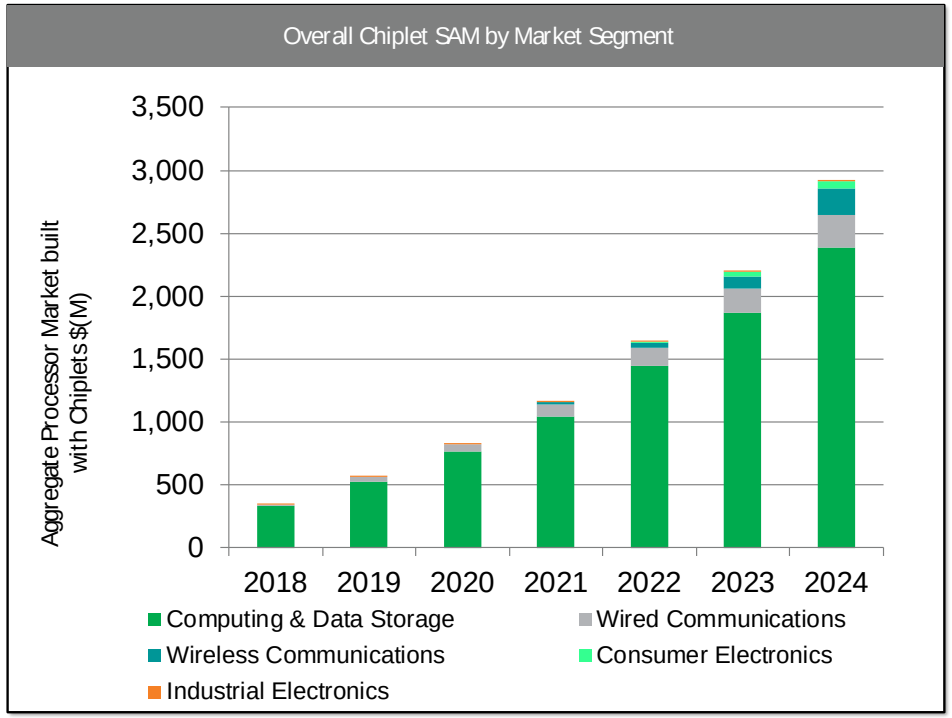
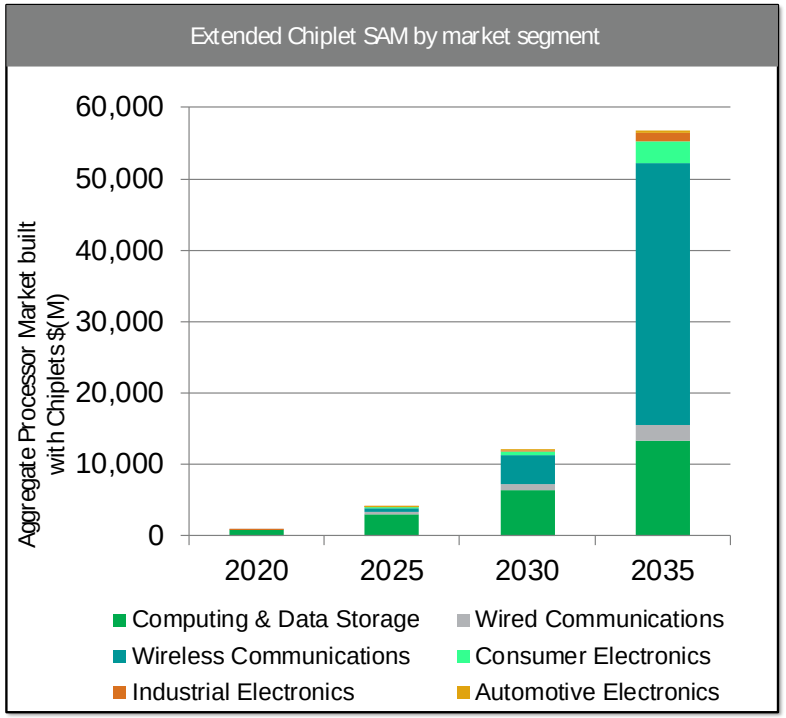
Transformative Market Opportunity: The End Game





- Initially dominated by compute uses case, other market segments grow to dominate
- **Takeaway**: an open chiplet eco-system with open interface standards is a huge opportunity

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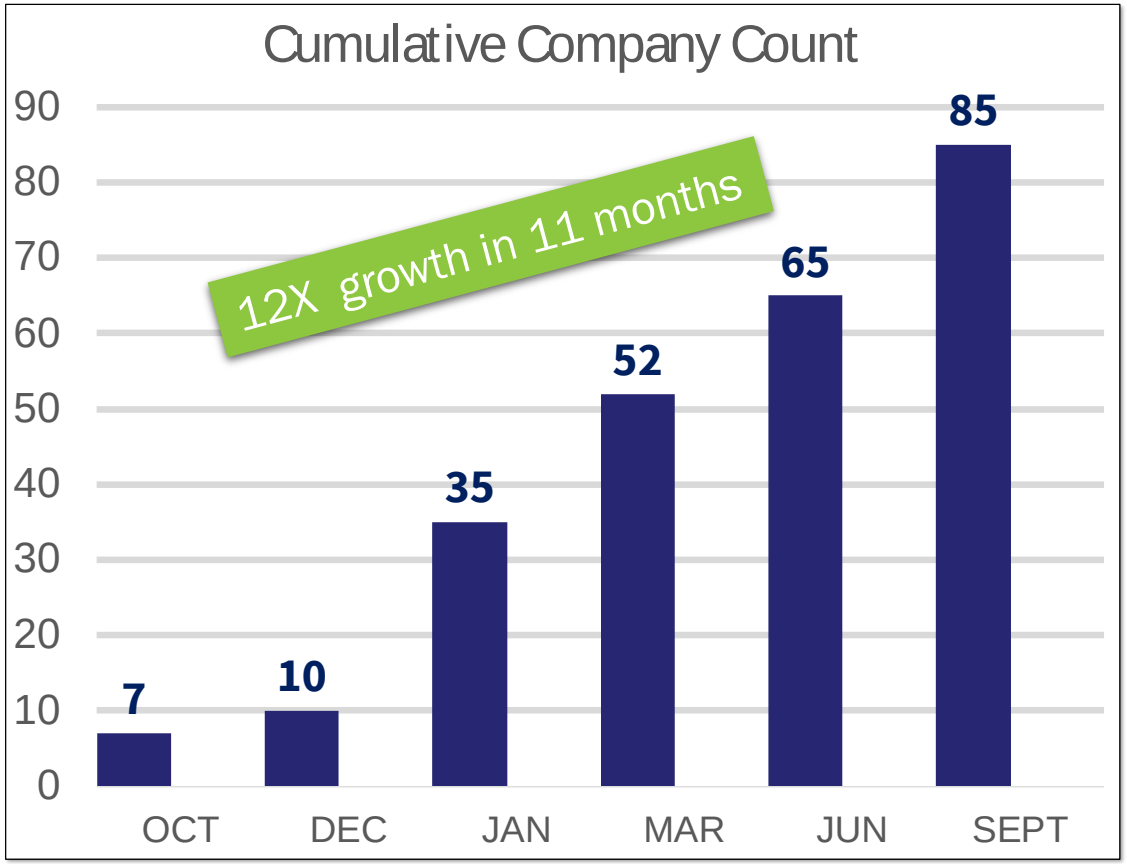
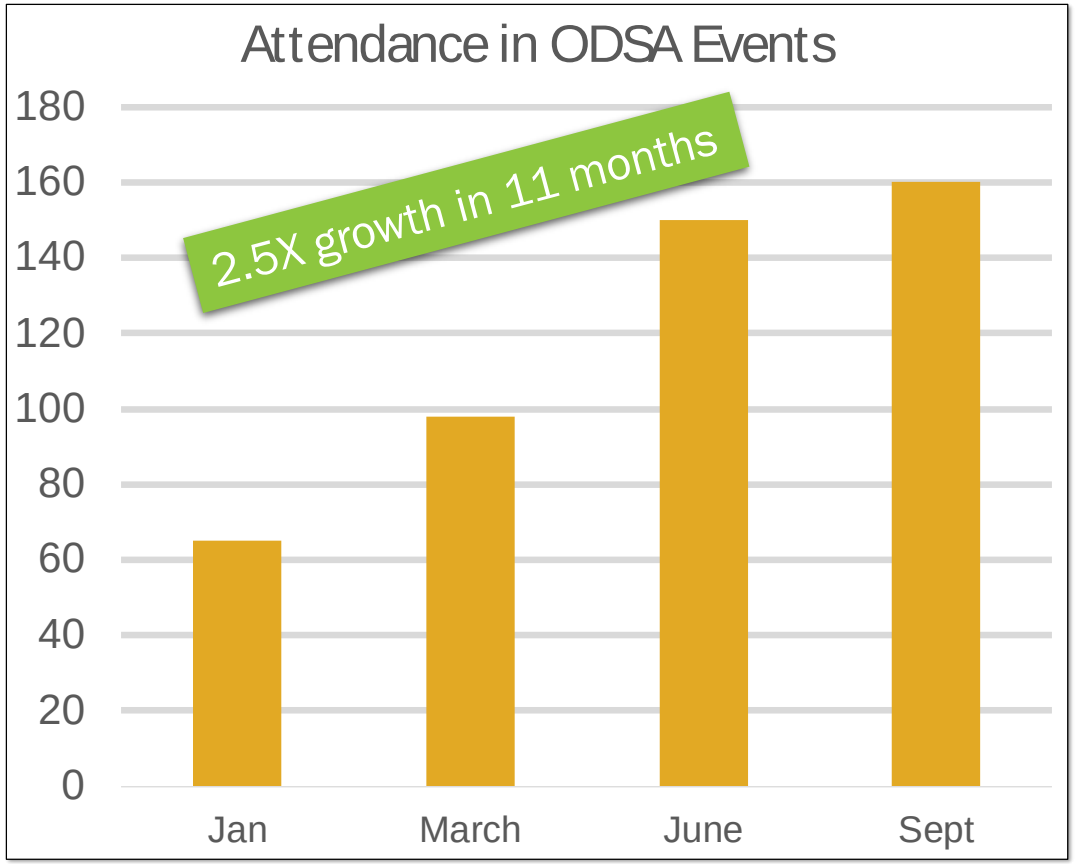
Growth of ODSA since Inception





Source: OCP ODSA Survey, Workshop Registration Data

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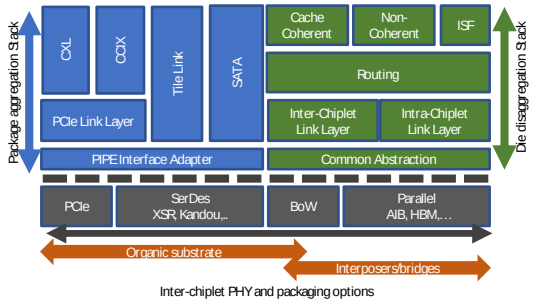
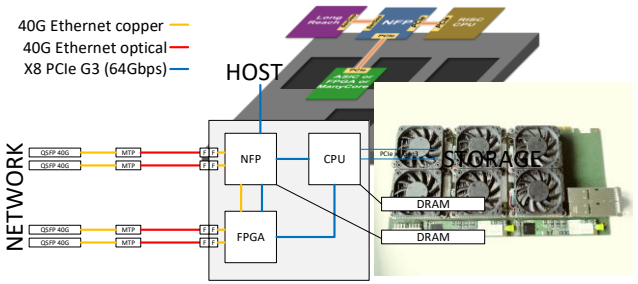
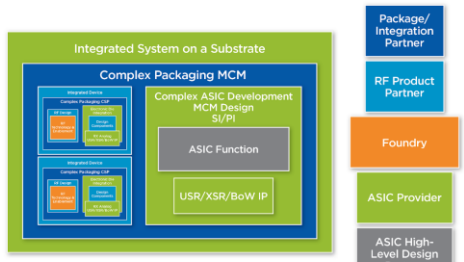
ODSA Vision of Chiplet Eco-System



Multi-technology ODSA stack

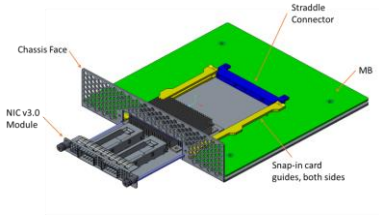


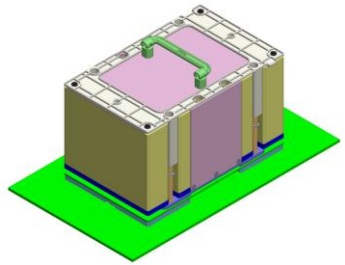
Reference architectures for: Networking, Storage, Inferencing, Training, Video and Image processing

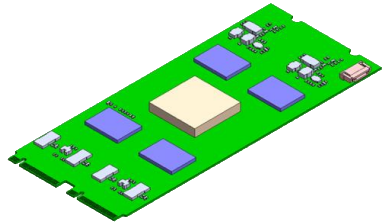


Business, Tools Workflow to assemble Product

Chiplet Marketplace







OCP Form Factors drive Power,I/O Footprint, Performance

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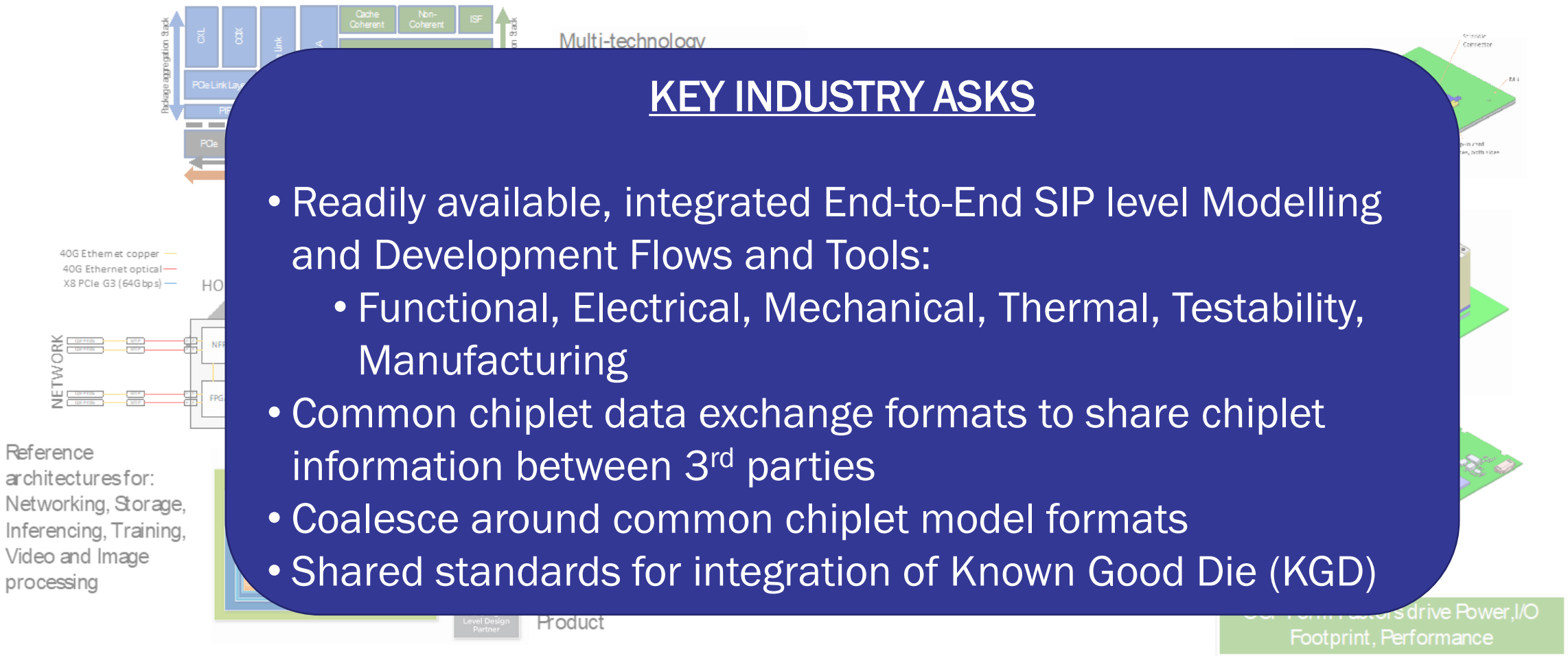

KEY INDUSTRY ASKS

- Readily available, integrated End-to-End SIP level Modelling and Development Flows and Tools:
  - Functional, Electrical, Mechanical, Thermal, Testability, Manufacturing
- Common chiplet data exchange formats to share chiplet information between 3rd parties
- Coalesce around common chiplet model formats
- Shared standards for integration of Known Good Die (KGD)

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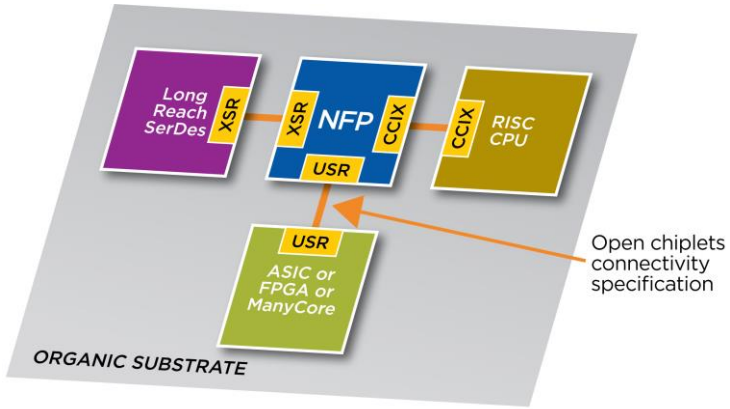
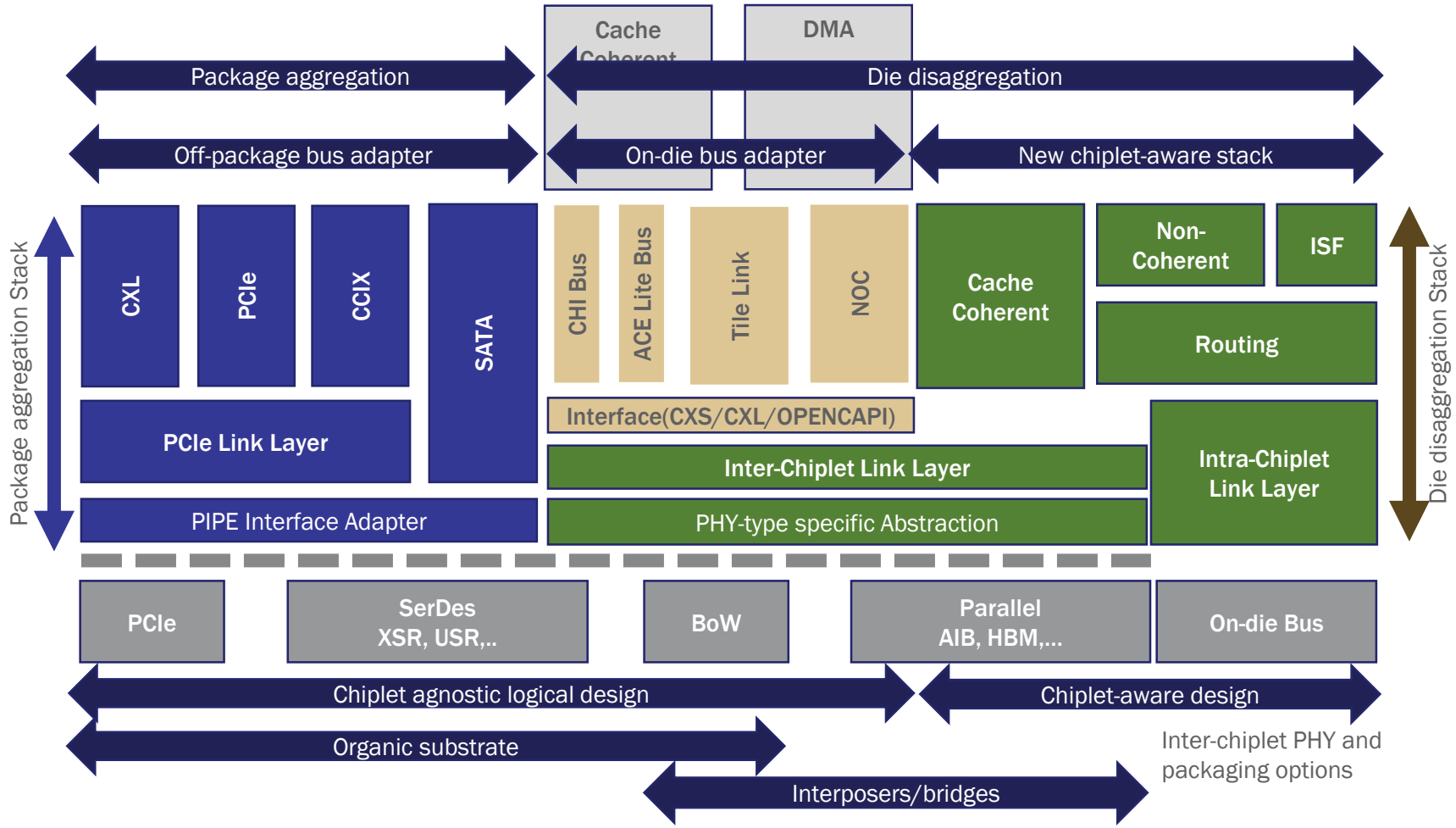
ODSA Stack: Current View

!! Coming Along Nicely !!



Multiple chiplets need to function as though they are on one die



On-die custom protocol (could be open e.g. AXI)

Off-package protocol (e.g. PCIe)

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ODSA Workstreams

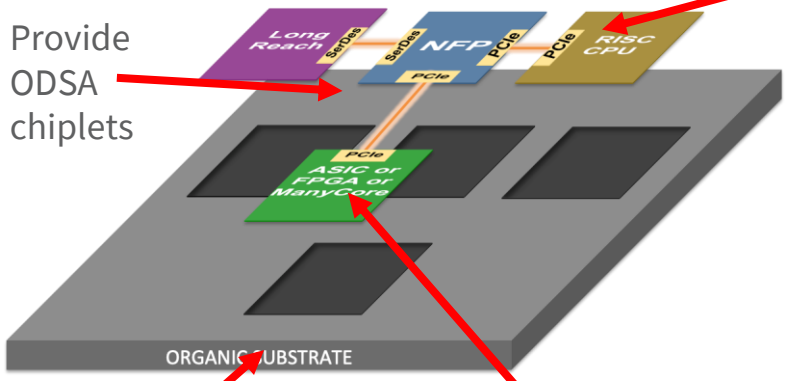
Please Help! Join a Workstream!

Join the PoC, Build fast:
(Quinn Jacobson/Jawad Nasrullah/
Jayaprakash Balachandran)

Join Interface/Standards:
(Mark Kuemerle/Ramin Farjad/
Robert Wang/David Kehlet)

Join Business, IP and workflow:
(Sam Fuller/Dharmesh Jani)

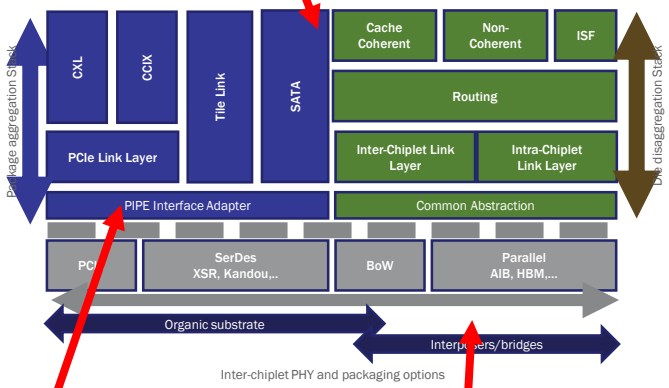
Provide ODSA chiplets



Develop Packaging + Socket, Dev Board

Provide FPGA IP

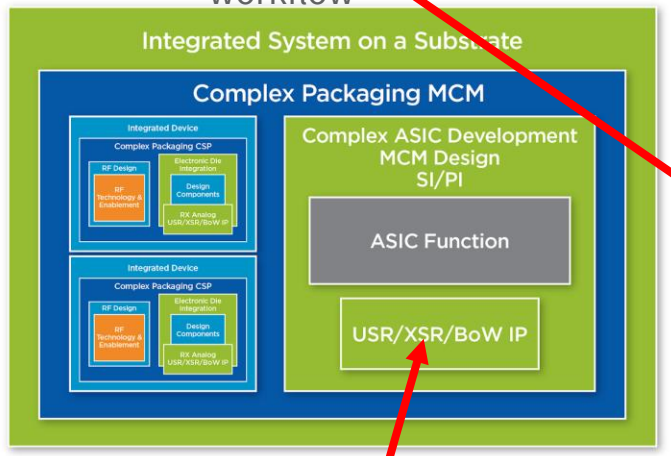
Develop software



Define Architectural Interface

Provide PHY Technology

Define test and assembly workflow



Provide Chiplet IP

Workstream contact information at the ODSA wiki

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Active Projects

Project	Objective	Organizations Participating	Recent Results	Upcoming Milestones	Needs
PHY Analysis	PHY requirements PHY analysis Cross-PHY abstraction (PIPE)	Alphawave, AnalogX, Aquantia, Avera Semi, Facebook, Intel, Kandou, Netronome, zGlue,	PHY Analysis paper (published at Hot Interconnect)	PIPE abstraction	
BoW Interface	No technology license fee, easy to port inter-chiplet interface spec	Aquantia, Avera Semi, Netronome	BoW Interface proposal (published at Hot Interconnect)	BoW specification 0.7 End September, 2019	Test chips, Chiplet library supporting interface
Prototype	product that integrates existing die from multiple companies into one package	Achronix, Cisco, Netronome, NXP, Samtec, Sarcina, zGlue, Macom, Facebook	Decomposable design flow.	Committed schedule	End user End user participation ~30% funding is open
Chiplet design exchange	Open chiplet physical description format.	Ayar, Cadence, NXP, zGlue,	Draft spec	ZEF Exchange format draft specification	
Link and Network Layer	Interface and implementations – requirements and proposals	Achronix, Avera Semi, Intel, Netronome, NXP, Xilinx			
Multi-chiplet test	Test requirements for an open-chiplet interface				
Chiplet monitoring	Monitoring infrastructure for chiplet operation				
Business workflow	Formalize learnings from prototype effort				

Engineers from:
Achronix, AnalogX, ASE, Avera Semi, Ayar, Cadence, Cisco, Facebook, Ferric, Intel, Kandou, Macom, Marvel, Netronome, NXP, On Semi, Samtec, Sarcina, Synopsys, Xilinx, zGlue

Wiki: https://www.opencompute.org/wiki/Server/ODSA, meet Fridays at 8 AM Pacific Time.
Please join us.

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ODSA Collaboration Results

- **Physical Interface Definition:**
  - PHY: Multi-company (zGlue, Netronome, Alphawave, Aquantia) analysis. First cross-PHY analysis published at Hot Interconnect
  - Bunch of Wires (BoW) PHY – new low-cost inter-chiplet PHY. Developed cooperatively by Aquantia, Avera Semi and Netronome with input from Xilinx, Global Foundries. Published at Hot Interconnect, IEEE Micro (Jan'20).
  - PIPE Abstraction – a new layer to "abstract" the interface PHY. Supported by Intel in their most recent PHY specification.
- **SIP Proof-of-concept / Prototype:**
  - Software development vehicle: Designed collaboratively by Cisco, Facebook, Macom, zGlue. Components from Achronix, NXP, Netronome. Working toward integrated into SIP. Design is highly scalable → able to add new participants easily.
- **Chiplet Design Exchange (CDX) Project:**
  - Project to facilitate the design of physical chiplet information for CAD tool integration (zGlue, ASE, Cadence, Macom)
- **Independent Market survey conducted by IHS Markit**
- **Everything is on our wiki -** https://www.opencompute.org/wiki/Server/ODSA

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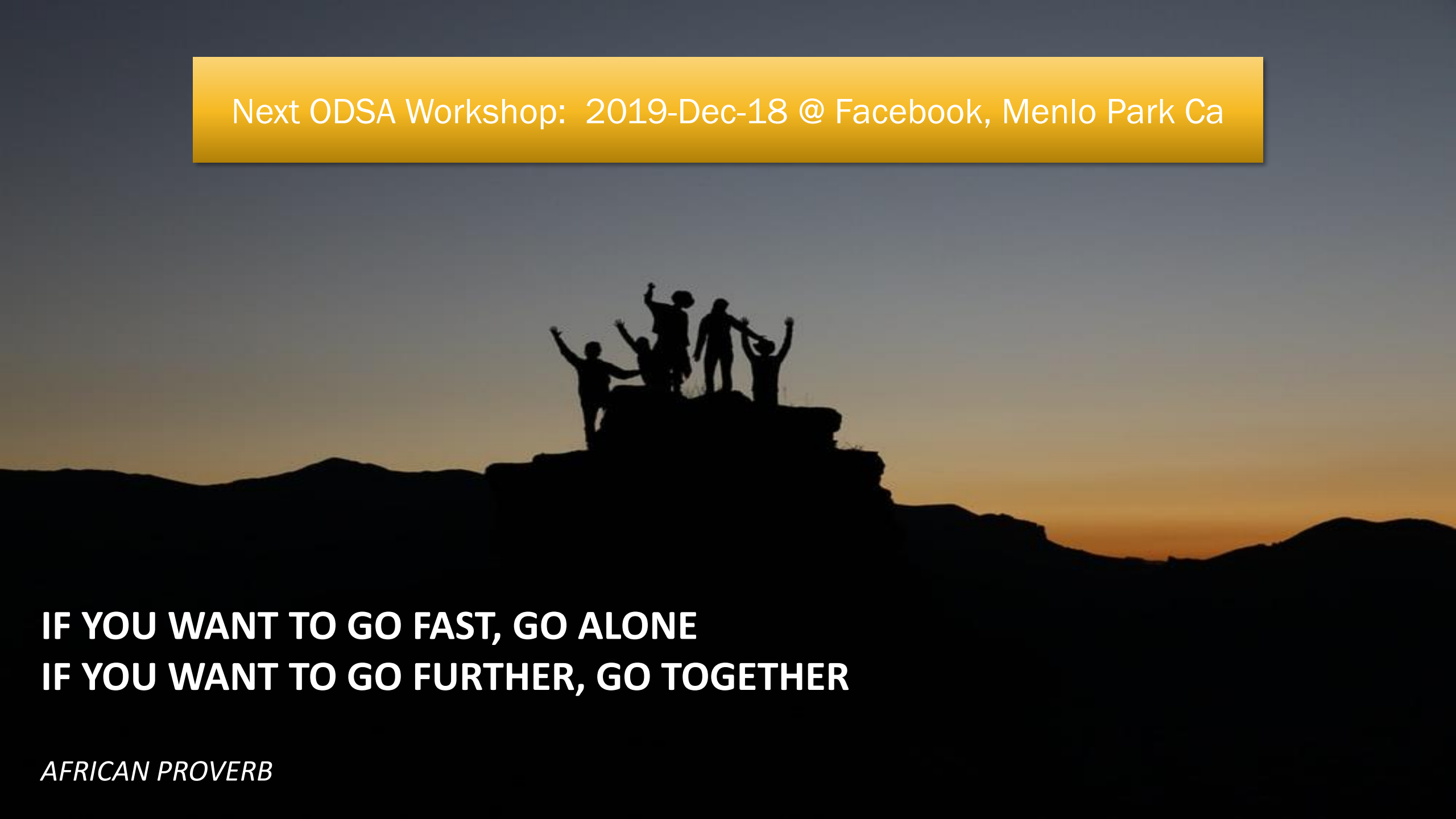
Looking Ahead

Time to begin planning Implementation

- PHY Layer:
  - Open or nearly-open PHY layer
  - Association to share development costs for proprietary PHY layer
  - Combination of the two
- Adapter Logic
  - PIPE adapter logic
  - IO Coherent link layer protocol –an ODSA member company may offer
  - Coherent link layer protocol – open
  - Bus adapters
- Easy to use no-friction interface will be widely used
  - Open source implementation is a good start

Next ODSA Workshop: 2019-Dec-18 @ Facebook, Menlo Park Ca



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AFRICAN PROVERB

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