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# Partial Width, Density Optimized HPM Form Factor (M-DNO) Base Specification

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Part of the

Datacenter – Modular Hardware Systems (DC-MHS) Rev 1.0 Family

Version 1.0 Release Candidate 4

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THE POSSIBILITY OF SUCH DAMAGE.

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## 2. Version Table

| Date      | Version # | Description  |
|-----------|-----------|--|
| 4/21/2022 | 0.7       | <ul style="list-style-type: none"> <li>Initial Public Release</li> </ul>   |
| 6/22/2022 | 0.8       | <ul style="list-style-type: none"> <li>Added Specification Compliance Table</li> <li>Separated hole dimensioning to separate drawings</li> <li>Added required pad size and recommended KOZs for all holes throughout document</li> <li>Adjusted fixed riser connector positioning</li> <li>Updated approach in Primary Side Component Height section</li> <li>Added start of "zone" approach to PIC connector placement</li> <li>Various text clarifications / edits</li> <li>Various drawing updates and fixes</li> </ul>   |
| 8/24/2022 | 0.9       | <ul style="list-style-type: none"> <li>Rewrite of secondary side stackup, board thickness, board pan etc. (10.3, 10.4)</li> <li>Removed Type 1 (many)</li> <li>Changed certain values for Type 3 to TBD (many)</li> <li>Placed all mounting hole information in one place (10.2)</li> <li>Changed "mid-board" mounting holes from required to HPM Designer preference for all board types (10.2)</li> <li>Removed secondary side keep out features for other board type hole locations (10.4)</li> <li>Modified type 4 board outline in custom zone area (10.1)</li> <li>Shifted HPM retention hole location (10.5)</li> <li>Updated dimension scheme for recommended riser connectors, simplified verbiage for riser requirements (10.9)</li> <li>Updated dimension scheme for PICPWR connectors (10.1.6)</li> <li>Aligned PICPWR location optional / required characteristics across all board types (11.1)</li> <li>Added PDB Management Connector (10.8)</li> <li>Miscellaneous image and text cleanup throughout document (see change bars)</li> <li>Added updated approach to primary side component height restrictions (10.12)</li> <li>Added 1016 as a recommended option on far side (12.1)</li> <li>Updated bottom side KOZ for board retention hole to align with FLW update (10.5)</li> <li>Removed cable enablement section (added note to primary side KOZ section)</li> <li>Added 2x3 PICPWR option, additional cleanup in power section (11.x)</li> <li>Added adapted HPM chapter, moved note from power chapter to new chapter (13.x)</li> <li>Simplified Ch 9 (removed board type goals)</li> <li>Added tolerance table and custom tolerance for type 2/3 width (10,10.1)</li> <li>Increased resolution of all figures</li> <li>Additional Tweaks to NearIO verbiage to try and clarify intent (10.9)</li> <li>Added required handle hole geometry (10.6)</li> <li>Added Platform Custom Zone section with content TBD (10.13)</li> <li>Added SFF number for riser connectors (12.1)</li> <li>Scrubbed compliance table, added note not final until 1.0 (4)</li> <li>Updated PIC connector locations (10.8)</li> <li>Added example of re-purposing required mounting hole for Handle hole geometry</li> </ul> |
| 9/26/2022 | 1.0       | <p>1.0 Contains many clarifications and fixes. The most impactful changes for in flight designs based on 0.9 are denoted by '&lt;' at the end of the line item</p> <ul style="list-style-type: none"> <li>Updated document for consistent formatting of <u>requirements</u> and <b>references</b></li> <li>Added 'datum' and cleaned up the terminology table (7)</li> <li>Small tweaks to compliance table (4)</li> <li>Added reference and links to DC-MHS Current Connector List (6) (12)</li> <li>Added reference to peripheral connector SFF-TA-1002 (10.7)</li> <li>Removed adapted HPM chapter</li> <li>Updated riser recommended connector name and power capability (11.1)</li> </ul>   |



|  |  |  |
|--|--|--|
|  |  | <ul style="list-style-type: none"> <li>• Added clarification that tolerance enables Open19 compatibility (10.1)</li> <li>• Reorganized supplemental material, added link to CAD (14)</li> <li>• Reorganized and clarified Sections 10.3 and 10.4 &lt;-</li> <li>• Removed Power Plane section, added note on voltage drop (11)</li> <li>• Renamed and renumbered Power Zone chapter (11)</li> <li>• Updated tolerance table (10)</li> <li>• Updated top side component 6mm and 11.3mm zone shapes (10.12) &lt;-</li> <li>• Updated Platform Infrastructure connector drawing (10.8)</li> <li>• Changed shape of board handle feature (10.6) &lt;-</li> <li>• Added location numbering for PICPWR connectors (11.7)</li> <li>• Added example uses of Platform Custom Zone (10.13)</li> <li>• Moved recommended intrusion switch location (10.8) &lt;-</li> <li>• Added separate image for Type 4 boot location zone (10.8)</li> <li>• Added route KOZ to HPM retention hole (10.5) &lt;-</li> <li>• Added reference to battery voltage requirement from DCSCM (12) &lt;-</li> <li>• Added additional industry references in separate section (13)</li> <li>• Corrected location of Detail B in Figure 11 (10/2) &lt;-</li> <li>• Misc. text / drawing tweaks for clarity not impacting technical content</li> </ul> |
|--|--|--|

### 195 3. Scope

This document defines technical specifications for the Density Optimized Form Factors used in Open Compute Project Data Center Modular Hardware System.

200 Any supplier seeking OCP recognition for a hardware product based on this specification must be 100% compliant with any and all features or requirements described in this specification.

#### 3.1. Items Not In Scope of Specification

- Compute Core (CPU/Memory/Voltage Regulators/SMP routing between CPUs)
- JTAG/Debug connectors for the Compute Core
- CPU, Memory, Heatsink, Liquid and any other thermal solutions
- 205 • Reliability requirements and design-in details
- BOM Population requirements
- Cooling System Connections (Fans, etc).

#### 3.2. Typical OCP Sections Not Applicable

210 This is a Base specification, requiring other MHS specifications to fully define a design. The following typical Sections of an OCP specification are not included because they are not applicable to this specification.

- Rack Compatibility (Discussed in Section 8)
- Physical Spec
- 215 • Thermal Design
- Rear Side Power, I/O, Expansion
- Onboard Power System
- Environmental Regulations/Requirements
- Prescribed Materials
- 220 • Software Support
- System Firmware
- Hardware Management (Leverages OCP DC-SCM V2)
- Security

225 The content expected in these subject areas is expected to be documented in future private and/or public Design Specifications and/or Product Specifications.

#### 4. Specification Compliance Table

230 The following table is intended to summarize the list of attributes and requirements for a design to be MHS – DNO Spec Compliant. It specifies only required attributes for compliance and does not list optional attributes.

| Item                           | Requirement  | Document Reference                                   |
|--------------------------------|--|--|
| <b>Mechanical</b>              |  | <b>Chapter 10</b>                                    |
| 1                              | PCB Tolerance Table  | Section 10, Table 1                                  |
| 2                              | Follow the defined board Outline   | Section 10.1, Figure 5 - Figure 7                    |
| 3                              | All required mounting holes with associated pads and KOZs  | Section 10.2, Figure 8- Figure 11                    |
| 4                              | Unique alignment hole and slot with associated pad and KOZs  | Section 10.2, Figure 8- Figure 11                    |
| 5                              | HPM Board thickness <= maximum defined   | Section 10.4   |
| 6                              | Board Thickness + Backplate Thickness <= maximum defined (Backplate max thickness calculated as specified)         | Section 10.4 & 10.3.4                                |
| 7                              | Secondary side chassis hook keep out zones   | Section 10.3.2, Figure 14- Figure 16                 |
| 8                              | Secondary side universal component height restriction  | Section 10.3.1, Figure 12                            |
| 9                              | HPM Secondary side support of required thickness near or under DIMMs   | Section 10.3.3, Figure 12                            |
| 10                             | Maximum length of a connector's Alignment Post or Retention Barb in Zone 2   | Section 10.3.2                                       |
| 11                             | HPM to Chassis Retention hole and associated KOZs  | Section 10.5, Figure 21                              |
| 12                             | Far Side hole for board handle with defined geometry and KOZs  | Section 10.6, Figure 23                              |
| 13                             | Specified Location for OCP NIC 3.0 Co-Planar Connector   | Section 10.7, Figure 24                              |
| 14                             | Specified Location for DC-SCM Co-Planar Connector  | Section 10.7, Figure 24                              |
| 15                             | Primary control panel connector placed within specified zone   | Section 10.8, Figure 25 & Figure 26                  |
| 16                             | Intrusion switch header placed within specified zone   | Section 10.8, Figure 25 & Figure 26                  |
| 17                             | Host USB connector placed within specified zone  | Section 10.8, Figure 25 & Figure 26                  |
| 18                             | PDB Management connector placed within specified zone  | Section 10.8, Figure 25 & Figure 26                  |
| 19                             | Any implemented board to board riser connectors placed in specific defined location                                | Section 10.9.2, Figure 29 & Figure 30                |
| 20                             | 2 (Type 2,3) or 3 (Type 4) I/O Retention Holes and KOZs  | Section 10.9.2, Section 10.11, Figure 30 & Figure 31 |
| 21                             | All non-exempt soldered components adhere to required Primary Side component height restrictions                   | Section 10.12, Figure 32 & Figure 33                 |
| <b>Power</b>                   |  | <b>Chapter 11</b>                                    |
| 22                             | Far side Ingress / Egress Power Zone with at least one 2x6 + 12SB PICPWR connector in specified location(s)        | Section 11.2, Section 11.7, Figure 38                |
| 23                             | If implemented, Near side Ingress / Egress Power Zone with 2x3+6S or 2x6+12S PICPWR connector(s) in specified zone | Section 11.2, Section 11.7, Figure 38                |
| 24                             | Each implemented riser location connector is PICPWR compliant  | Section 11.3, M-PIC                                  |
| 25                             | HPM delivers at least 87W to each implemented riser location   | Section 11.3   |
| <b>Electrical (I/O System)</b> |  | <b>Chapter 12</b>                                    |
| 26                             | All HSIO connectors (near and far) are M-XIO compliant   | Section 12.1, M-XIO                                  |
| 27                             | Internal USB follows M-PIC specification   | Section 12.2, M-PIC                                  |
| 28                             | Intrusion Switch follows M-PIC specification   | Section 12.3, M-PIC                                  |
| 29                             | If implemented, boot storage follows M-PIC specification   | Section 12.4, M-PIC                                  |
| 30                             | Primary control panel follows M-PIC specification  | Section 12.5, M-PIC                                  |
| 31                             | If implemented, secondary control panel follows M-PIC specification  | Section 12.5, M-PIC                                  |
| 32                             | PDB Management Connector follows M-PIC specification   | Section 12.6, M-PIC                                  |
| 33                             | HPM shall implement battery backed voltage interface per DC-SCM R2.0 "Battery Voltage" requirement                 | Section 12   |

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## 5. Overview

240 The objective of this specification is to outline the requirements of a family of partial width, **DeNsity Optimized Host Processor Module (HPM)** form factors within the OCP **Modular** hardware system group of specifications (**M-DNO** for short). This M-DNO specification embodies design considerations for CPU, DIMMs, and other server processor related features commonly used by the industry today but is not limited to only those functions. For instance, an FPGA array being placed within the Compute Area of the HPM is allowable per this specification. The HPM is designed with standard 19" rack, also known as compliant with EIA - 245 310-E and larger 21" racks in mind but is not limited to only those solutions. This specification considers both monolithic and multi-node / "blade" based system architectures in its definition.

The goals and successes of this specification are defined by allowing multiple generations of Compute Core (CPU/Memory) designs implemented to the specification to enable reuse of chassis and system level components over multiple generations and HPMs. Implementing to 250 this specification and design methodology should result in reduced design investment, reduced validation investment, broader product portfolios and faster development cycle times due to enhanced reuse and leverage opportunity for each HPM designed.

This specification shall define attributes and design requirements that are common and critical to the use and deployment of Enterprise and Cloud solutions and may also apply to Edge 255 optimized service provider products. Examples of these attributes are mechanical form factor, placement guidance of common subsystems and placement guidance of HPM Power and Input-Output (IO) connections.

## 6. DC-MHS Family of Specifications

The **Data Center – Modular Hardware System (DC-MHS)** family of specifications are written to enable interoperability between key elements of datacenter and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks. At the time of this publication there are the following specification workstreams:

- **M-FLW (Modular Hardware System Full Width Specification)** – Host Processor Module (HPM) form factor specification optimized for using the full width of a Standard EIA-310 Rack mountable server. The specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-DNO (Modular Hardware System Partial Width Density Optimized Specification)** – Host Processor Module (HPM) specification targeted to partial width (i.e.  $\frac{1}{2}$  width or  $\frac{3}{4}$  width) form factors. Such form factors are often depth challenged and found not only in enterprise applications but also in Telecommunications, Cloud and Edge Deployments. While the EIA-310 Rack implementation is chosen as a key test case for use, the specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-CRPS (Modular Hardware System Common Redundant Power Supply Specification)** – Specifies the power supply solutions and signaling expected to be utilized by DC-MHS compatible systems.
- **M-PIC (Modular Hardware System Platform Infrastructure Connectivity Specification)** – Specifies common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems. Examples include power management, control panel and cooling amongst others.
- **M-XIO (Modular Hardware System Extensible I/O)** – Specifies the highspeed connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers with peripheral subsystems such as PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.
- **M-PESTI (Modular Hardware System Peripheral Sideband Tunneling Interface)** – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (e.g., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination.
- **Current Connector List** – Vendor and part number information for all connectors referenced by DC-MHS specifications, updated as needed. Full URL: [https://docs.google.com/spreadsheets/d/1Vq\\_JxzZ43ysxBNHJ928vnzlcshA95GYGocAKmJCBC80/](https://docs.google.com/spreadsheets/d/1Vq_JxzZ43ysxBNHJ928vnzlcshA95GYGocAKmJCBC80/)

To access additional DC-MHS specifications please visit the [OCP Server Project Wiki - Working](#)

## 7. Terminology

| Standardized Term           | Meaning  | Alternative Terms    |
|-----------------------------|--|----------------------|
| Shall                       | Indicates a requirement for spec compliance  | Must                 |
| DC-SCM                      | Datacenter Secure Control Module v2 as defined by OCP DC-SCM 2.0 spec  | SCM                  |
| PCB                         | Printed Circuit Board  | PCBA                 |
| HPM (Host Processor Module) | PCB or PCBA form-factor being defined by this spec   | Motherboard, board   |
| Chassis-Board Bracket       | Bracket that attaches to an HPM assembly, that enables a variety of board outlines and hole locations to change over time, and still fit within same chassis base.   | Board Pan<br>Sub Pan |
| Datum                       | A plane, axis or point location from which dimensions and tolerances are referenced.   |                      |
| Near                        | Board location or zone, related to section of board closer to the datum  |                      |
| Far                         | Board location or zone, opposite of location of datum  |                      |
| Platform                    | Complete system including HPM, power, peripherals, etc   |                      |
| Compute Core                | Elements of board design that are critical to processor and memory support, inclusive of CPU and Memory sockets. Examples are Voltage Regulators, High Speed IO routing, High speed trace routing between multiple processors, high speed trace routing between processors and memory, etc |                      |
| IO                          | Input Output, commonly referring to high speed connections to a CPU socket.  |                      |
| PCIe                        | Peripheral Component Interconnect Express  |                      |
| CXL                         | Compute Express Link   |                      |
| HSIO                        | High Speed IO, commonly referring to PCIe routing, PCIe connectors, CXL routing/connectors, etc.   |                      |
| OCP                         | Open Compute Project   |                      |
| OEM                         | Original Equipment Manufacturer  | Enterprise           |
| CSP                         | Cloud Service Provider   |                      |
| ½ Width HPM                 | 210mm wide HPM, enables systems with 2 HPMS side by side in 19" Rack   |                      |

|  |  |                  |
|--|--|------------------|
| $\frac{3}{4}$ Width HPM                            | 295mm wide HPM, enables systems with HPM adjacent to 2xM-CRPS PSUs   |                  |
| Platform Custom Zone                               | Area of system board where space is allotted for Platform designers to implement custom features.  |                  |
| Platform Infrastructure Connectivity Specification | Refer to Section 1 (References)  | M-PIC            |
| Full Width Specification                           | Refer to Section 1 (References)  | M-FLW            |
| Common Redundant Power Supply Specification        | Refer to Section 1 (References)  | M-CRPS, CRPS PSU |
| Extensible I/O Specification                       | Refer to Section 1 (References)  | M-XIO            |
| KOZ  | Keep Out Zone, a design term for PCB designs that defines area of a board design where no components may be placed, usually to enable mechanical attachments or mechanical features. |                  |
| Compliant HPM                                      | An HPM which meets every item listed in this base specification compliance table.  |                  |
| Adapted HPM  | An HPM that utilizes a Compliant HPM as a construct, with a specific set of repeatable modifications which form the adaptation.  |                  |
| HPM Designer                                       | The person or organization designing an HPM (whether compliant or adapted) which implements this base specification.   |                  |
| System Designer                                    | The person or organization designing a system which incorporates HPMs (whether compliant or adapted) into the system design.   |                  |

## 8. Background & Assumptions

M-DNO targets a wide variety of 1 and 2 socket platforms including multi-node and monolithic (one HPM per chassis) systems for use in Enterprise, Cloud, and Edge applications. In these applications the range of targeted chassis can be extremely varied, as can the location of the HPM within the chassis. Monolithic systems are typically, but not limited to, 1RU or 2RU designs. Multi-node systems on the other hand are expected to have a broad application set from 2U (e.g. 4 ½ Width HPMs) to 5U (e.g. 8-12 ½ Width HPMs in vertical orientation) chassis and beyond. Rear and Front service models (including articulating chassis with removable cover) are also considered.

When considering representative system depth targets, the most common environments were distilled into the following categories:

### 1. Standard Depth Rack / Solution

- ~1070mm+ deep with a single ½ width (210mm) or ¾ width (295mm) HPM
- ~1070mm+ deep with two ½ width (210mm) HPMs

### 2. Mid Depth Rack / Solution

- ~430mm to 570mm deep with a single ½ width (210mm) or ¾ width (295mm) HPM

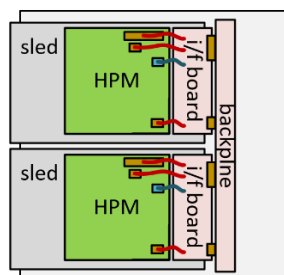
### 3. Short Depth Rack / Solution

- ~350mm to ~430mm deep with a single ½ width (210mm) HPM

This specification shall focus on products targeted to these primary environments. **Section 14.1** illustrates design scenarios for each of these solutions providing the reader a clearer understanding of each category. This specification does not in any way prohibit alternate environments.

V1.0 of this specification does not address native “direct plug” or “blind mate” options for HPMs, these scenarios may be added in a future release. It is assumed that HPMs compliant with V1.0 will leverage an interface board to enable these use cases as demonstrated in **Figure 1**.

**Figure 1: M-DNO HPM with multi-node interface board**



## 8.1. Common Industry Platform Features Considered

### Mechanical

- Chassis installation within minimum EIA-310-E racks (but not limited to)
- PCIe Riser Connector fixed placement
- PCIe Cable route considerations
- Any additional fixed connector placement



**I/O**

- 340 • PCIe (Version 3.0, 4.0, 5.0, and future) Card configurations typically offered by Enterprise OEMs/CSPs/CoSPs.
- In 1U offerings with PCIe CEM based I/O, only Half-Length PCIe cards (167.6mm) are considered. This does not prevent Three-Quarter Length (254mm) cards, but support for Three-Quarter Length cards would restrict Compute Core placement (not defined).
- 345 • Use of Open Compute peripherals connectors on the HPM
  - OCP NIC v3.0
  - DC-SCM v2.0
  - *Note: While each HPM outline requires 1 connector of each type, a system is not limited to 1 device of each type; configurations with 0 or >1 OCP NIC v3 / DC-SCM*
- 350 v2.0 are possible, but outside the scope of this specification

**Power**

- HPM supplied power to each fixed riser locations
- HPM Power Ingress and Egress connector placement for a variety of power layouts (PSUs with Cabled PDB, blind mate to bus bar, multi-node backplane, etc.)
- 355 • Considerations for Power Delivery to important chassis subsystems.

**Thermal**

- Thermal Design considerations including keep-out zone to enable thermal solutions that extend beyond the CPU and Memory sockets.
- 360

**8.2. Architecture Specific Assumptions****Mechanical / Systems**

- M-DNO based systems
  - Do not direct plug PSUs into the HPM but instead leverage Power Distribution Boards (PDB) or other system / rack level power infrastructure
  - Use remote fan designs in air cooled platforms (there is no HPM spec provision for Fan connectors on the HPM)
  - Support riser based I/O cards, cable based I/O cards or a mix of both
  - Leverage a variety of front and rear service models of I/O, PSU, HPM, etc.
- 365
- 370 • Systems designed for larger HPM Types may support use of smaller Types in a common chassis or sled with minimal changes (e.g. cables, riser quantities, standoff locations)
- Multi-node chassis designs leverage static rails with overall inner chassis opening width of 443mm (in 19" rack)
- Monolithic chassis designs leverage slide rails with overall inner chassis width of 431mm (in 19" rack)
- 375
- $\frac{3}{4}$  Width HPM must accommodate 2x 60mm M-CRPS PSUs within chassis opening described above (431mm)

## I/O

- 380 • All M-DNO HPM Types enable (but do not require systems to utilize) use of “off the shelf” OCP NIC V3.0
- Mid / Standard Depth systems will *typically* leverage Coplanar OCP NIC layouts
- Short Depth systems will often require alternate implementation such as “floating” the OCP NIC (or no-pop)
- 385 • PCIe CEM based I/O will be the predominant use case for consideration but alternate form factors are not prohibited

## DC-SCM

- All M-DNO HPM Types enable (but do not require systems to utilize) use of “off the shelf” DC-SCM 2.0
- 390 • Mid / Standard Depth systems will *typically* leverage Coplanar DC-SCM
- Short Depth systems will often require alternate implementation such as “floating” DC-SCM

## 9. HPM Layout

### A Note on Board Types:

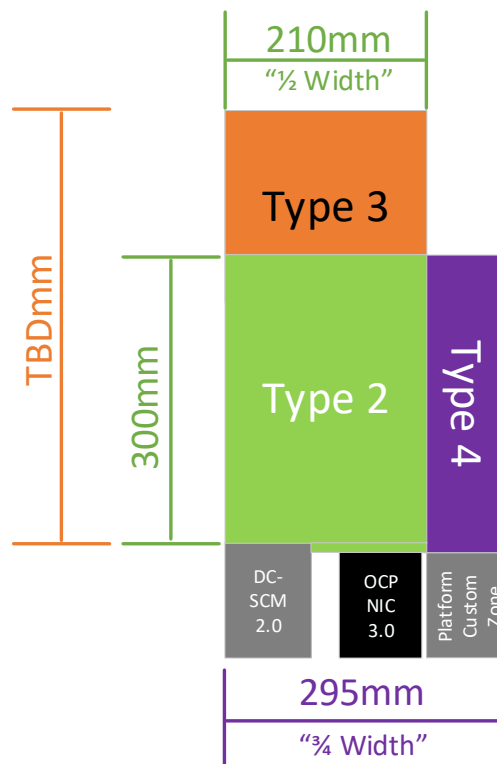
The M-DNO specification workgroup studied various board configurations, sizes, and system intercepts. As the details matured, changes to the board types defined in draft releases were made for Version 1.0.

- “Type 1” was removed due to lack of clear industry use cases
- “Type 3” is included, however, certain details have been left as “TBD” to allow the workgroup additional time to further study the intended use cases. Included details should be considered directional and may change in a future M-DNO release.
- The initial type referencing by number was not reset for V1.0

*In Summary, this specification will provide full detail on Type 2 and Type 4, as well as directional detail on Type 3.*

395 To achieve the goals outlined in **Section 8**, this M-DNO specification defines three different HPM board “Types”. Note that the M-DNO specification does NOT mandate CPU / DIMM quantities or define a specific area for CPU and Memory.

**Figure 2: M-DNO Board Type Layout Overview**

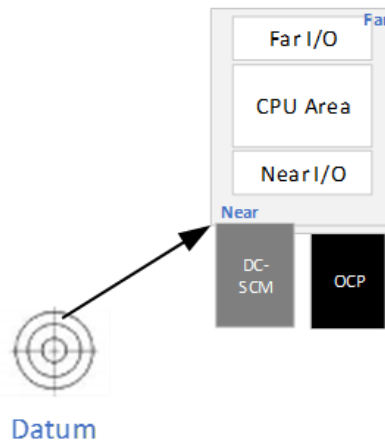


400 **Figure 2** provides a dimensional overview of the three board types, additional definitions and concepts are described below:

1. Due to the wide array of potential HPM and Chassis configurations, this specification defines a **Near** <<Element>> as the <<Element>> closer to the Datum (0,0 reference) and **Far** <<Element>> as the <<Element>> further from the Datum, examples for <<Element>> include:
  - a. Corner
  - b. Edge
  - c. I/O Zone

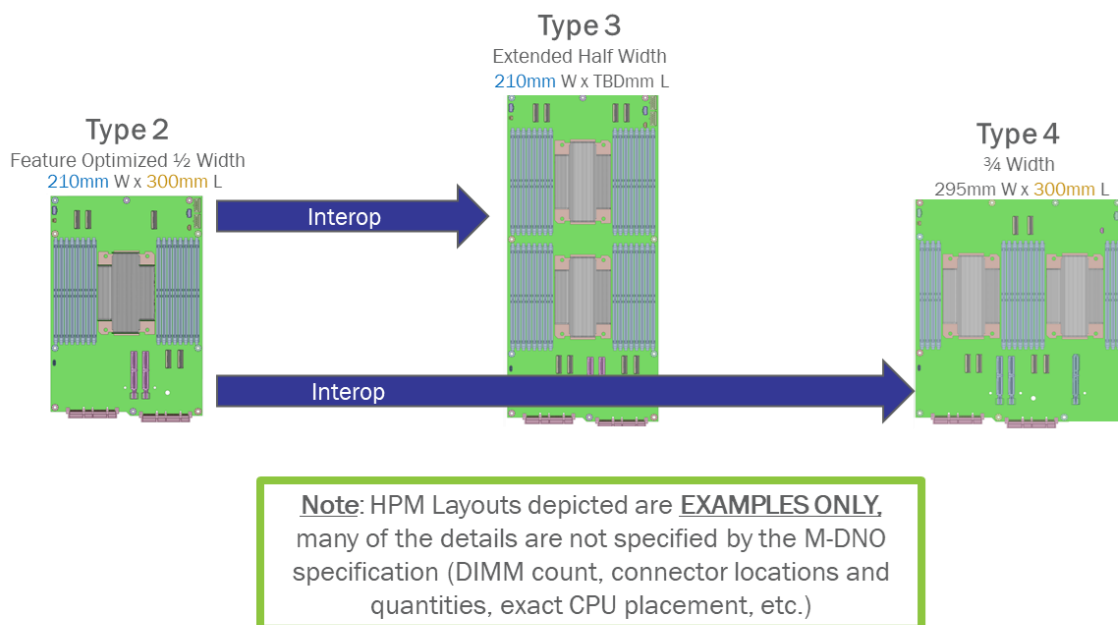
An example of Near and Far terminology usage is shown in **Figure 3**.

**Figure 3: Near and Far Terminology Example**



2. The location of the DC-SCM and OCP NIC connector on the HPM shall be common across all types relative to the Datum point (0,0)
3. "½ Width" refers to the common 210mm HPM width shared by Type 2 and 3
4. "¾ Width" refers to the 295mm HPM width used in Type 4
5. "Full Width" HPMs are outside the scope of this specification and are defined by the M-FLW specification
6. HPMs narrower than ½ Width are also outside the scope of this specification due to the inability of supporting common DCSCM 2.0 and OCP NIC 3.0 connector locations as described in #2. The DC-MHS workgroup may consider narrower HPM designs in the future.
7. The goal of this specification is to provide HPM Interoperability of smaller M-DNO HPM Types in systems designed for larger M-DNO HPM Types with minimal modifications (e.g. board pan or I/O cable changes), as depicted in **Figure 4**:
  - a. Type 2 HPMs can be easily leveraged into systems which support Type 3 HPMs
  - b. Type 2 HPMs can be easily leveraged into systems which support Type 4 HPMs
  - c. These goals do NOT apply between M-DNO and M-FLW HPMs

**Figure 4: M-DNO Type Interop Goals**



430

## 10. Mechanical Requirements

In addition to the drawings and details within this document, DFX/CAD files will be provided for further detail (**Section 14.3**).

Unless otherwise specified all units are in mm.

Unless otherwise specified, PCB dimensions shown in this specification shall comply to **Table 1**.

**Table 1: Standard Tolerances**

| Dimension Type   | Tolerance, unless otherwise specified |
|--|---------------------------------------|
| FROM Origin/Datum hole center TO round fiducial center | +/- 0.076mm (+/- 0.003 inch)          |
| FROM Origin/Datum hole center TO profiled card edge    | +/- 0.254mm (+/- 0.010 inch)          |
| FROM Origin/Datum hole center TO drilled hole center   | +/- 0.127mm (+/- 0.005 inch)          |
| FROM Profiled card edge TO profiled card edge          | +/- 0.127mm (+/- 0.005 inch)          |
| Feature of size (hole diameter, slot width, etc.)      | +/- 0.100mm (+/- 0.004 inch)          |
| PCB thickness  | +/- 10% of nominal                    |

Route KOZ's referenced in this specification, at a minimum, refer to surface layers and microstrip routing. Further application of the Route KOZ to other layers is the choice of the HPM designer and/or Design specification.

### 10.1. HPM Outlines

There are 3 M-DNO HPM Type Outlines defined as described in **Section 9**.

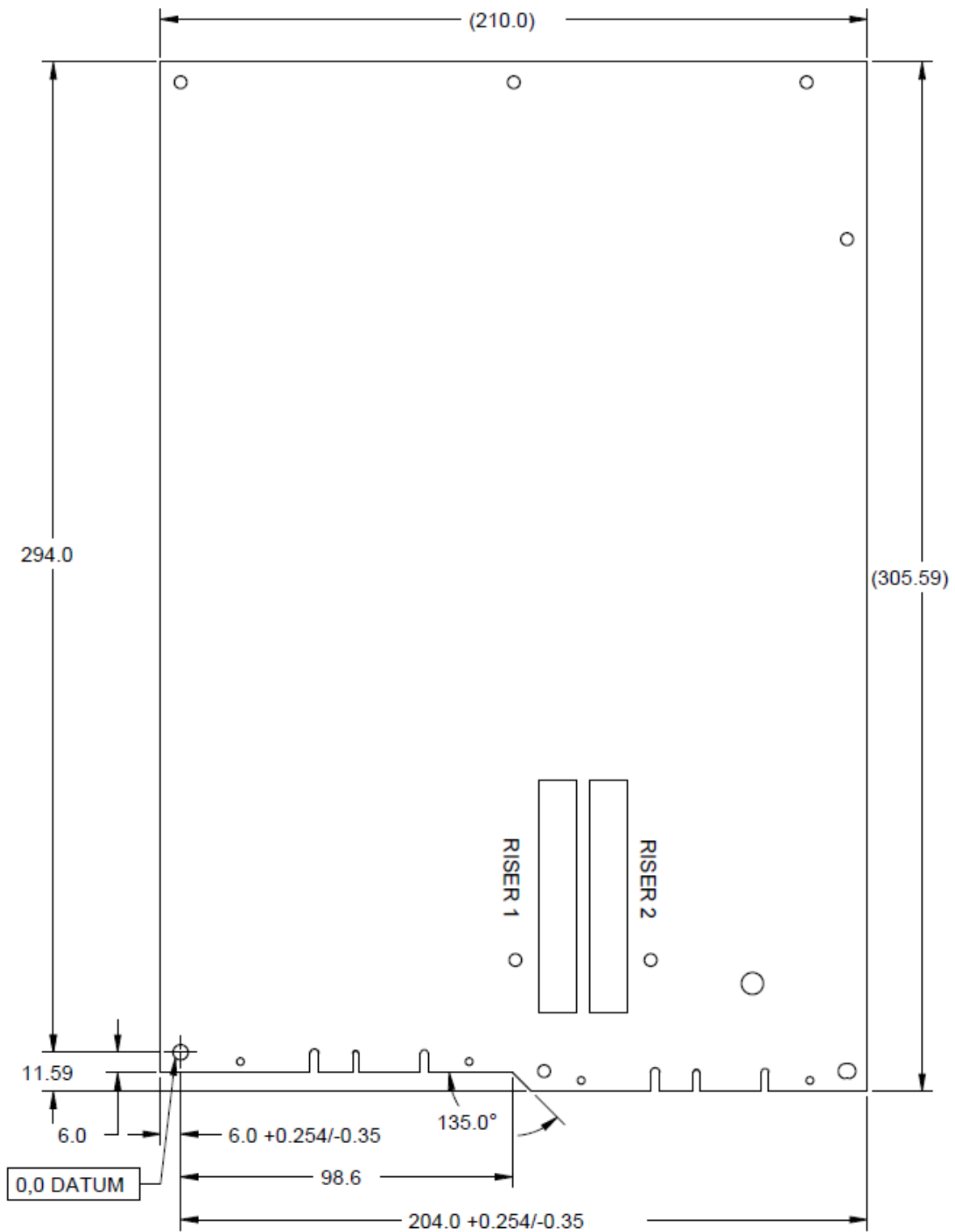
The required M-DNO Type 2,3 and 4 Outlines are defined in **Figure 5 - Figure 7** below.

Note that **Figure 5** and **Figure 6** contain unique tolerances when dimensioning the HPM width. These asymmetric width tolerances allow the HPM designer to optionally choose to set the nominal total width to 209.55 if desired for use within a single-height half-width (SHHW) [Open19](#) "brick".

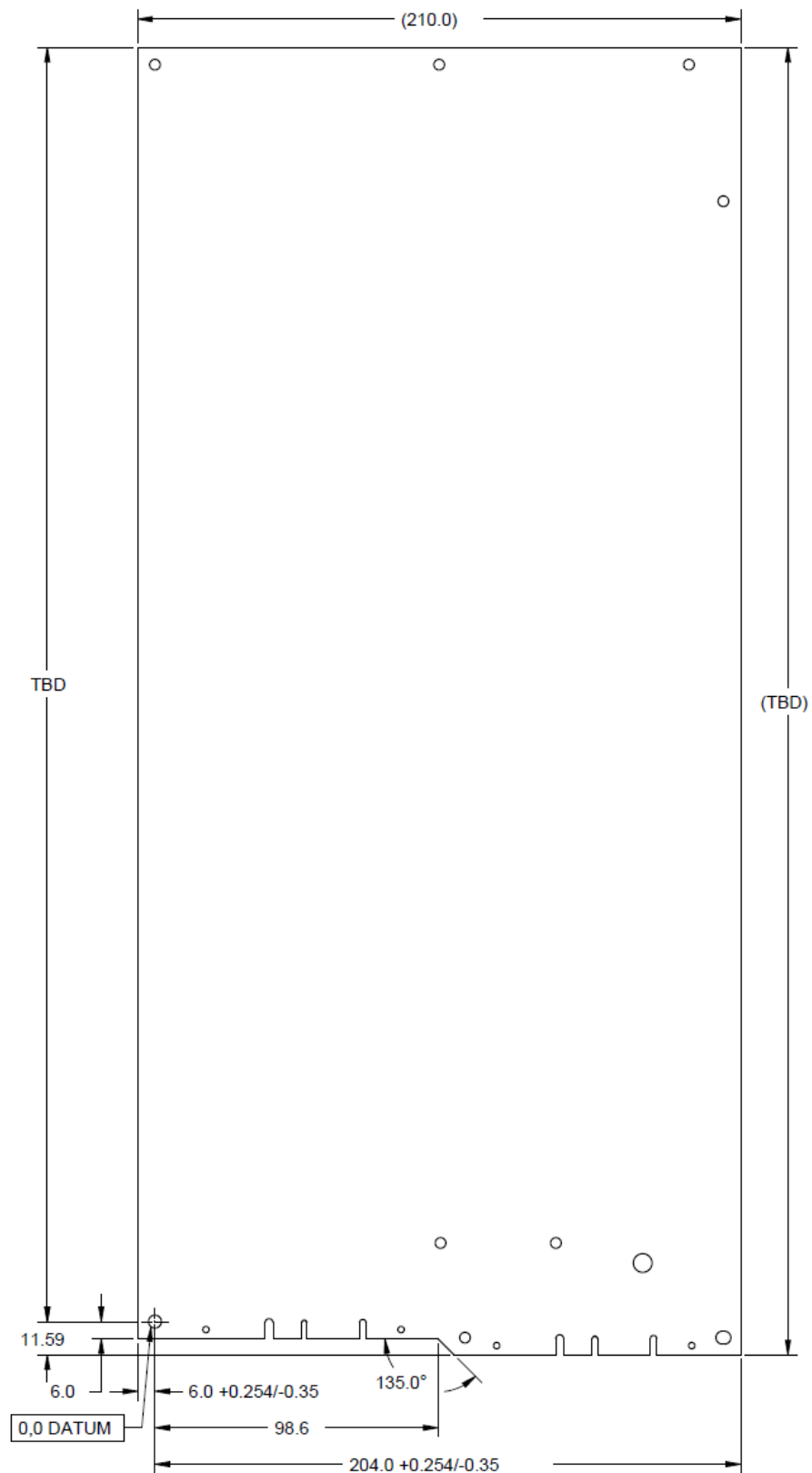
Note that the Type 4 outline near the Platform Custom Zone (described in **Section 10.13**) shown in **Figure 7** may change for connector choice compatibility specific to the usage of the Platform Custom Zone.

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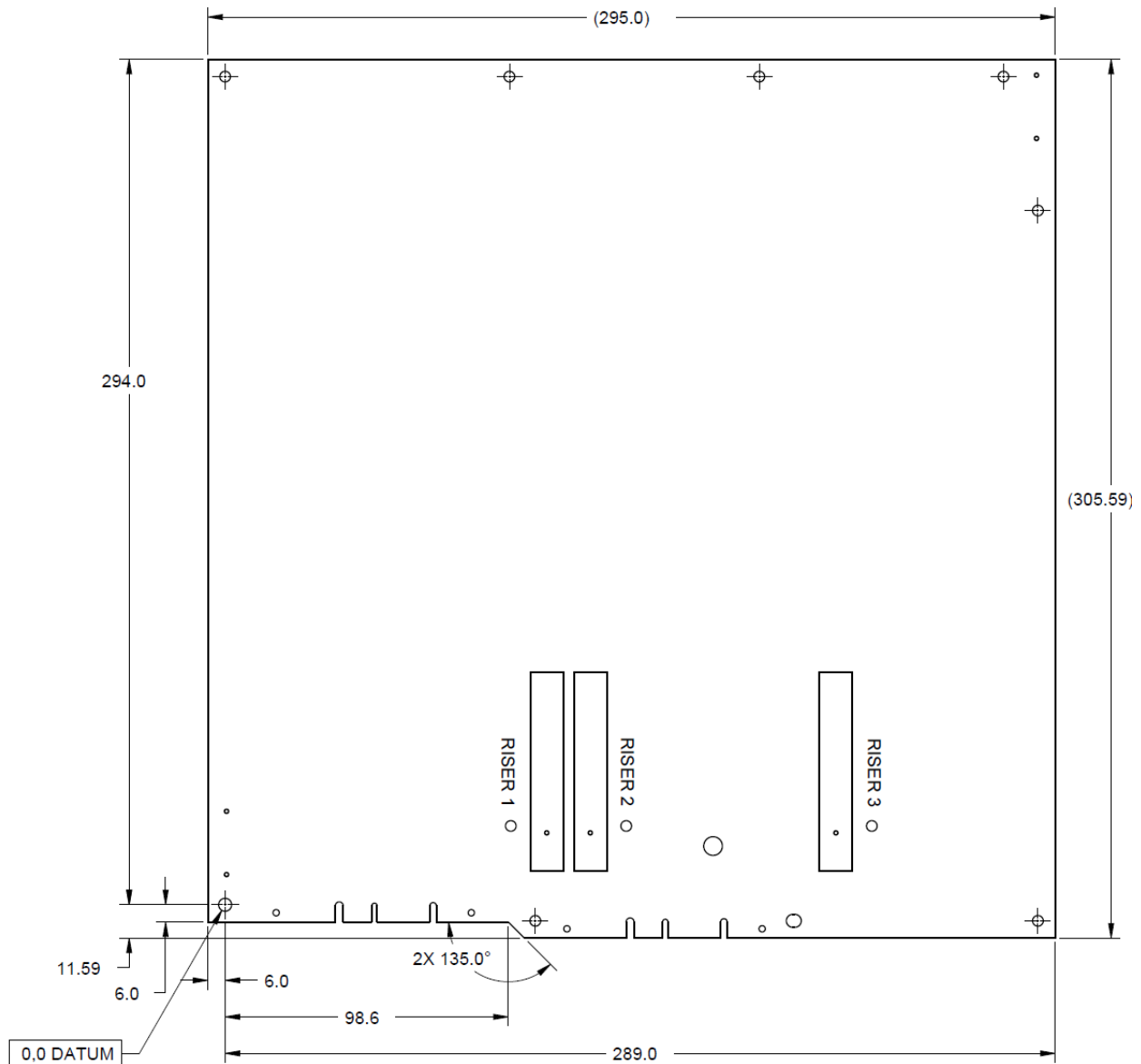
**Figure 5: Type 2 HPM Outline**



**Figure 6: Type 3 HPM Outline**





**Figure 7: Type 4 HPM Outline**

## 10.2. Board Datum and Mounting Hole Information

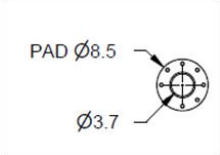
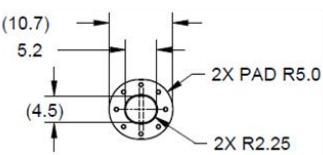
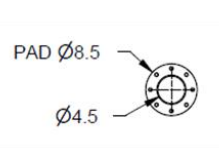
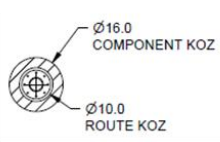
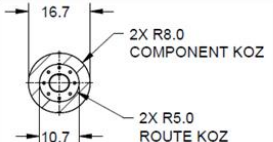
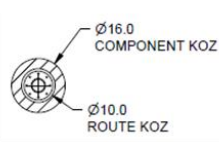
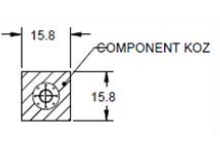
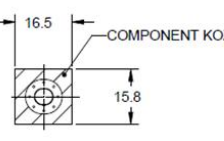
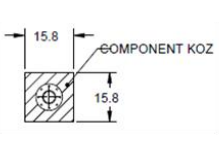
All M-DNO board types leverage a common datum location at the center of the mounting hole in the near corner of the board where the DC-SCM 2.0 connector resides. This allows for fixed elements (riser connectors, peripheral connectors, ...) to have a common reference across all board types.

Detailed hole information common to all board types is provided in **Figure 8**.

All holes shall adhere to the specified size, ground pad dimensions, component KOZ and route KOZ.

470 The component KOZ is intended to keep small components at risk of damage away from the hardware and assembly tools. If a component is larger than 10mm in any dimension (i.e. a DIMM connector), it is considered more robust, and may encroach on the Component KOZ's.

**Figure 8: Hole Detail Reference**

|                    | DETAIL A<br>Standard Mounting Holes  | DETAIL B<br>Unique Alignment Slot  | DETAIL C<br>Unique Alignment Hole  |
|--------------------|--|--|--|
| Hole and Pad Sizes |   |  |   |
| Top Side KOZs      |   |   |   |
| Bottom Side KOZs   |  |  |  |

475 A set of required board mounting hole locations are specified for the 3 M-DNO HPM Types in **Figure 9-Figure 11**. All dimensioned holes are required.

It is expected that HPM designers will add additional mounting holes based on their HPM layout. All additional holes should adhere to Standard Mounting Hole requirements (Detail A in **Figure 8**).

480 It is recommended that HPM designers include a hole adjacent to the Far power zone, an example is depicted but not dimensioned.

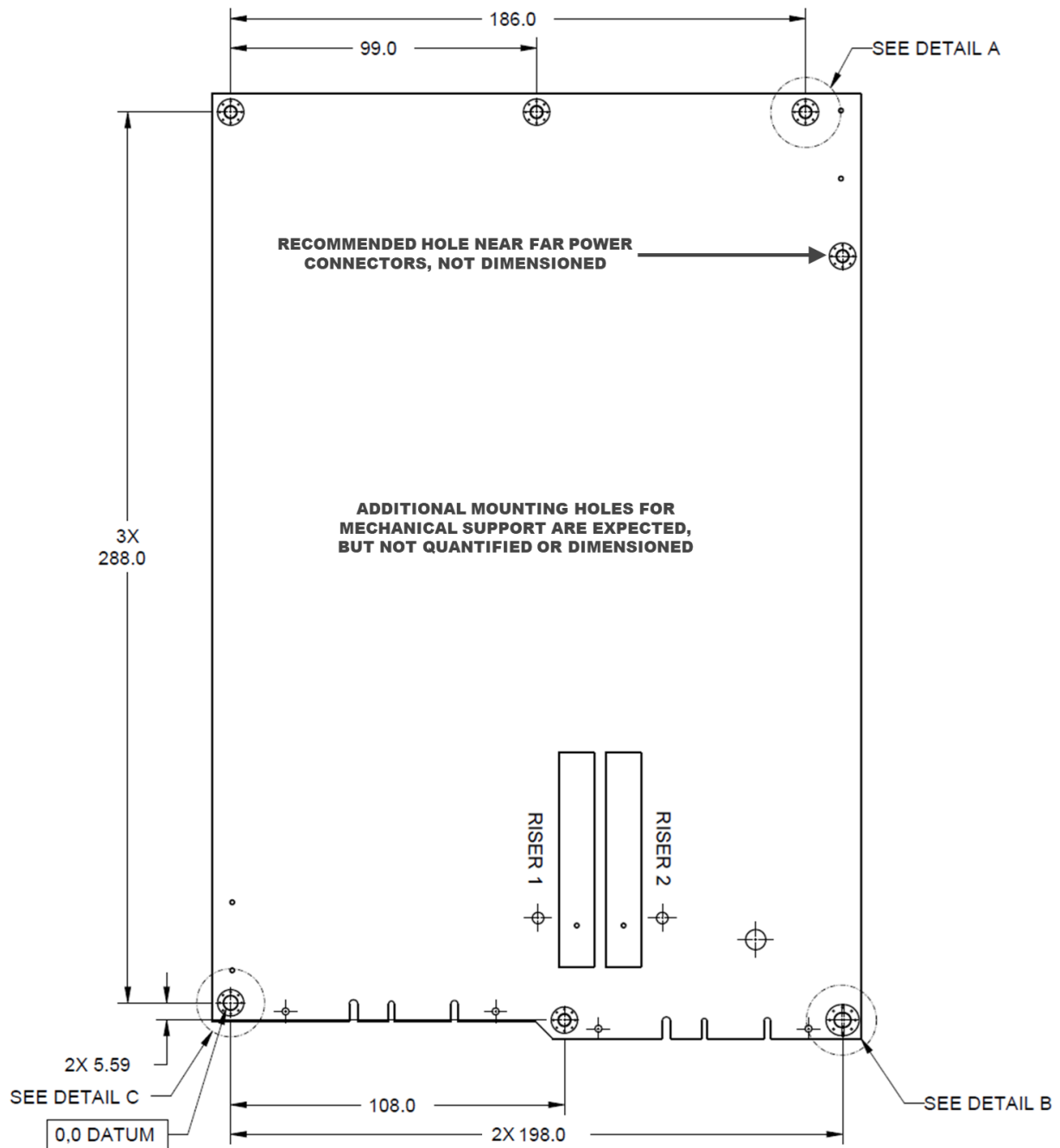
A design should follow good engineering practices in consideration of Platform Shock and Vibration requirements. Shock and Vibration requirements are not in scope of this specification.

#### **Implementors Note:**

The PCB Datum hole (**Figure 8** Detail C) is defined such that a collared standoff with tight tolerance fit can be used to control X-Y tolerances in HPM mounting. Additionally, a slotted hole (**Figure 8** Detail B) is defined to control rotation around the datum, by allowing, as an example, a collared standoff to be used with tight fit to the top/bottom edge of the slot.

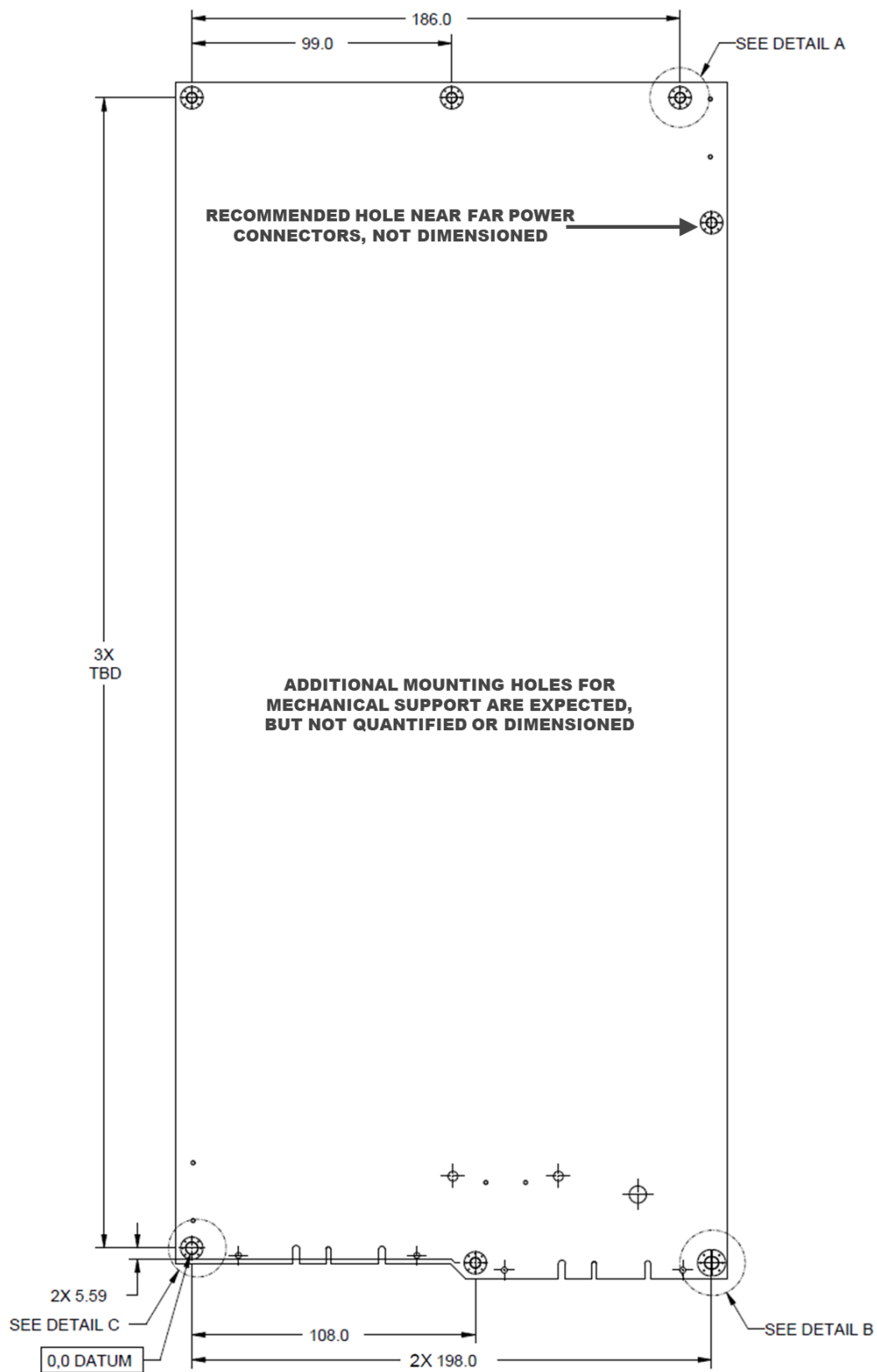
All other mounting holes follow standard mounting hole guidance (Detail A). These mounting holes are expected to have clearance fits to screw hardware.

**Figure 9: Type 2 Mounting Holes**

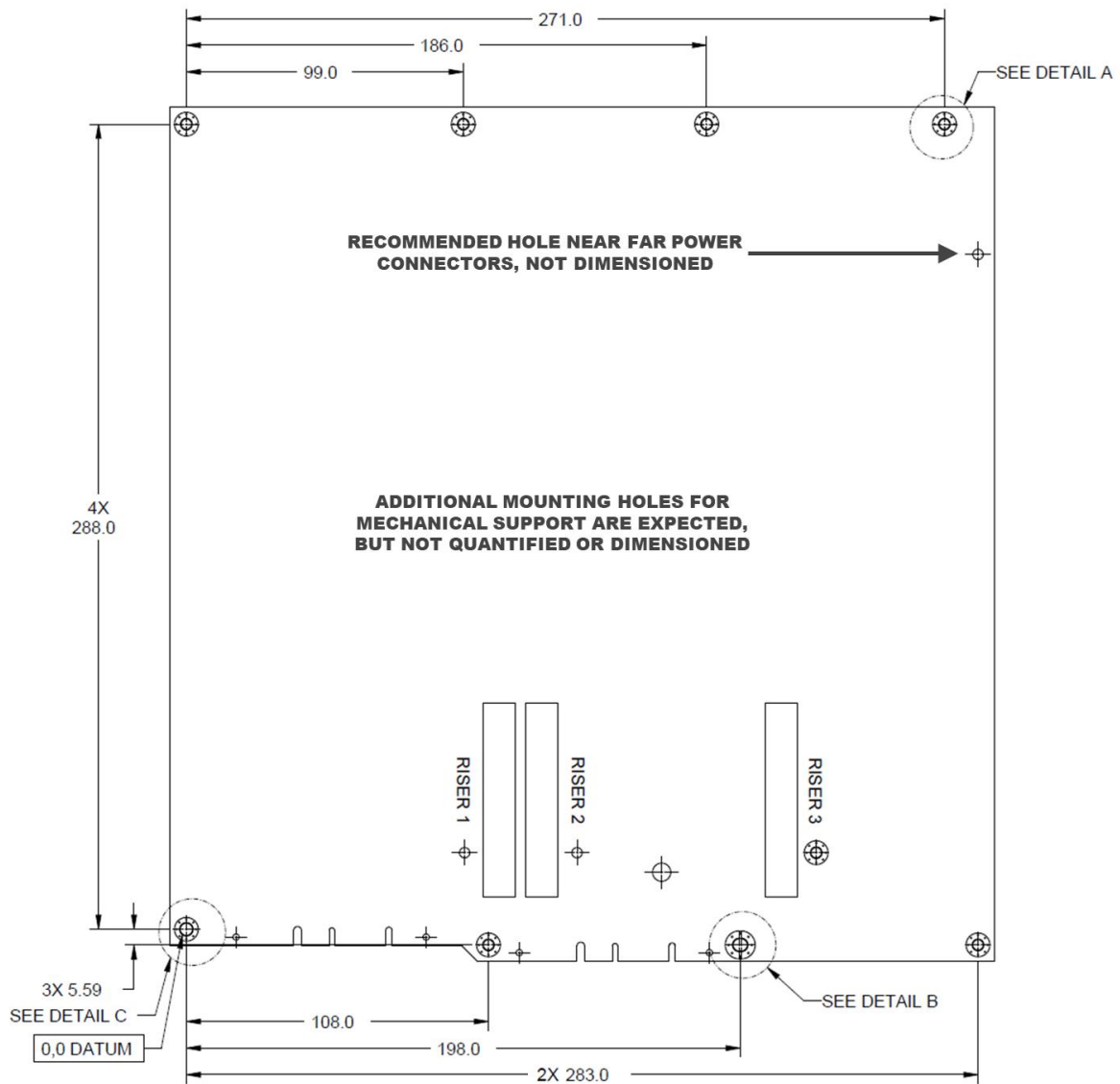


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**Figure 10: Type 3 Mounting Holes**



**Figure 11: Type 4 Mounting Holes**



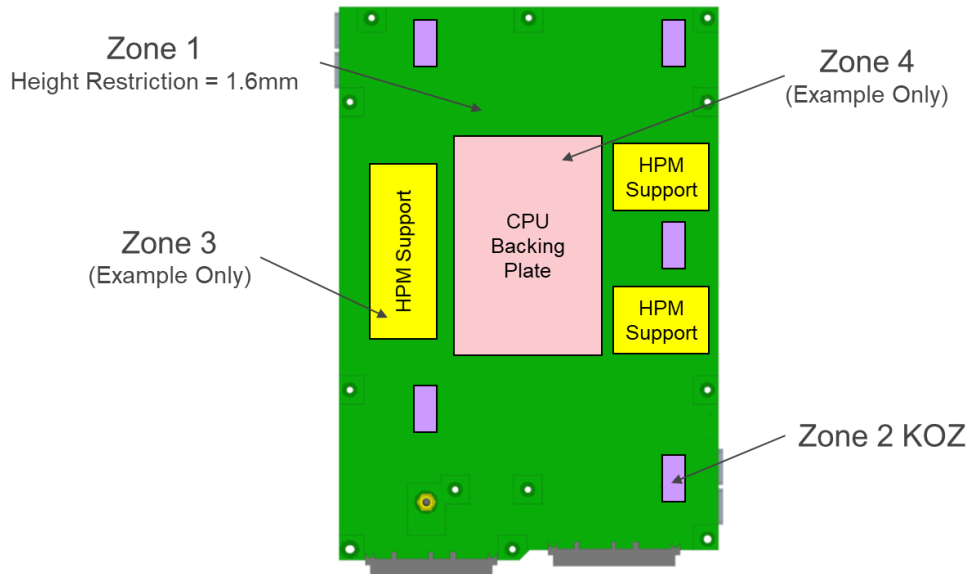
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### 10.3. Secondary Side Zones and Height Restrictions

There are four distinct Zones on the secondary side of the HPM as depicted in **Figure 12**. Each zone serves a unique purpose.

495 Zone 1, 2, 3 and 4 define different Requirements for Compliance.

**Figure 12: Secondary Side Zone Definitions**



#### 10.3.1. Zone 1: Secondary Side Height Restriction

500 Zone 1 universally applies to the entire secondary side of the HPM, except for the defined Zones 2, 3, and 4. HPM electrical components are expected to utilize Zone 1.

There is a required Zone 1 universal secondary side component height restriction of 1.6mm for all board types. This requirement ensures HPM component clearances to chassis base or board pan structures. This is especially important with a max allowable board thickness as defined in **Section 10.4**.

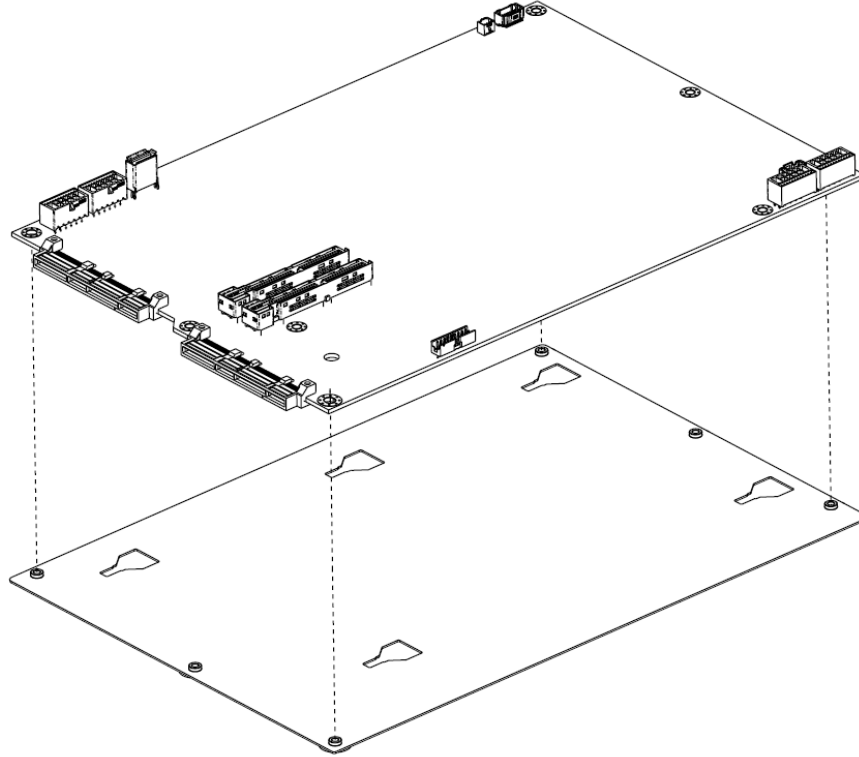
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#### 10.3.2. Zone 2: Chassis to HPM Bracket (Board Pan) KOZ Requirements

M-DNO HPMs shall allow for a Chassis-to-Board Bracket (Board Pan) which enables different board layouts (and mounting hole locations) between HPM Types and Compute Core designs, while maintaining compatibility to a common chassis. An example Board Pan is shown in **Figure 13**.

510

**Figure 13: Example of Chassis-to-Board Bracket (Board Pan)**



**Implementors Note:**

While most monolithic server designs benefit from a Board Pan, it is NOT expected that all systems supporting M-DNO HPMs will require a Board Pan. Specifically, sled-based designs common in multi-node systems typically do not require a board pan.

515 M-DNO HPMs shall support required zero height KOZ locations for chassis hook features that interface between the chassis base and the Chassis-to-Board Bracket as defined in **Figure 14 - Figure 16.**

A supporting chassis base must provide hook geometry to interface the cutouts on the Chassis to Board Bracket.

The geometry of the Board Bracket is not specified.

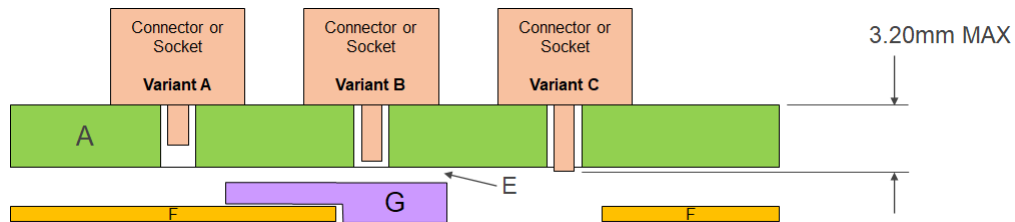
520 Connectors and/or sockets may be placed over the Chassis Hook Keepouts on the Primary Side of the HPM. The maximum length of a connector's Alignment Post or Retention Barb should be 3.20mm MAX such that it will not interfere with chassis hook features.

This length guidance is for Non-Conductive Alignment Posts or Grounded Retention Barbs. Through Hole leads for Power and Signal pins are not permitted in the Chassis Hook Keepout.

### **Implementors Note:**

Alignment Posts and Retention Barbs of connectors that protrude through the HPM can impact an HPM design's ability to be compliant with the Chassis Hook Keepout Zones.

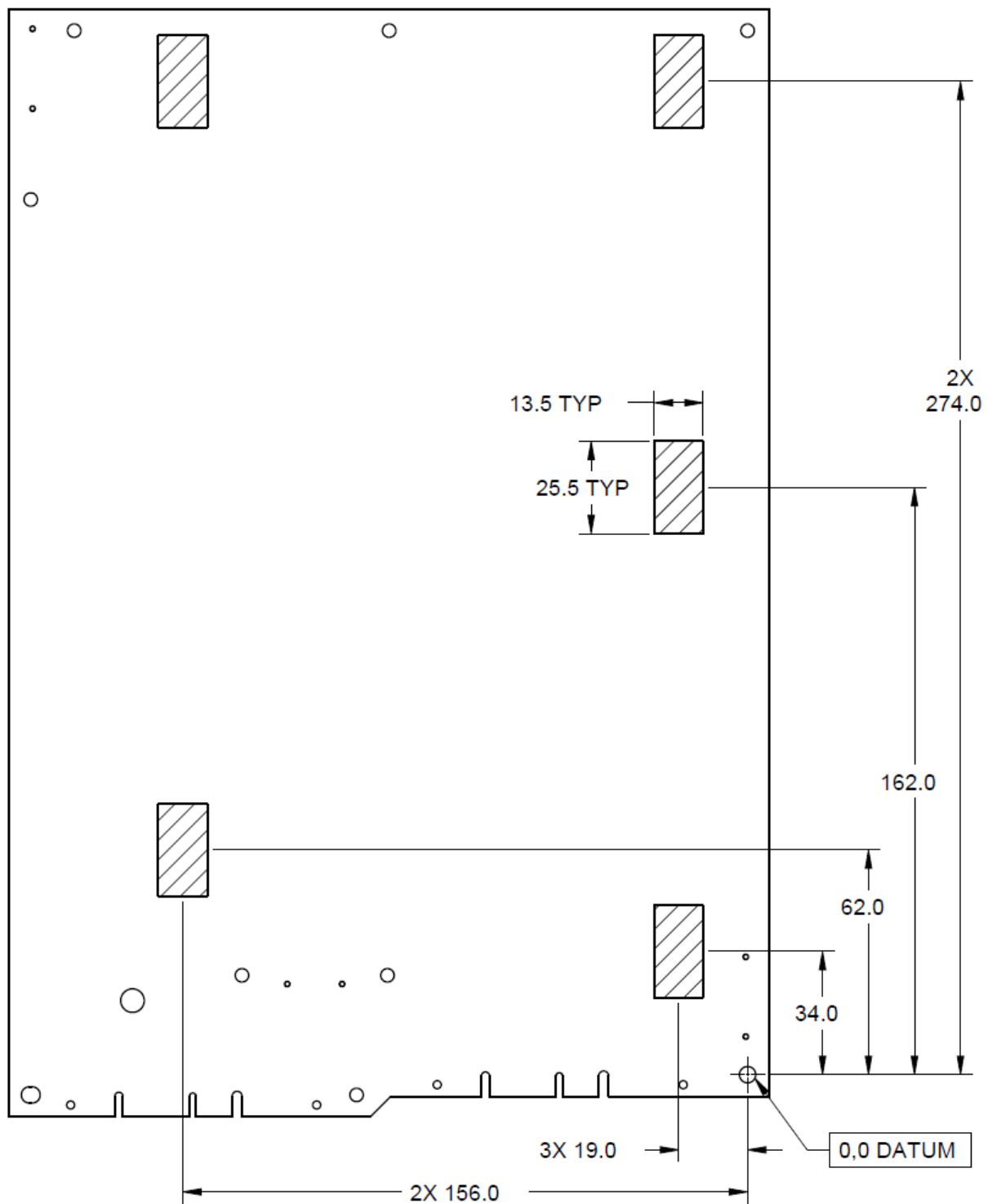
The HPM Designer should choose connector variants with Alignment and Retention features that do not protrude through the secondary side of the HPM to avoid any potential collision with Chassis Hooks during system assembly. Refer to **Table 2: Example Z-Height Compliant Stack-Up, Per Zone** for details on 'A', 'E', 'F' and 'G'.



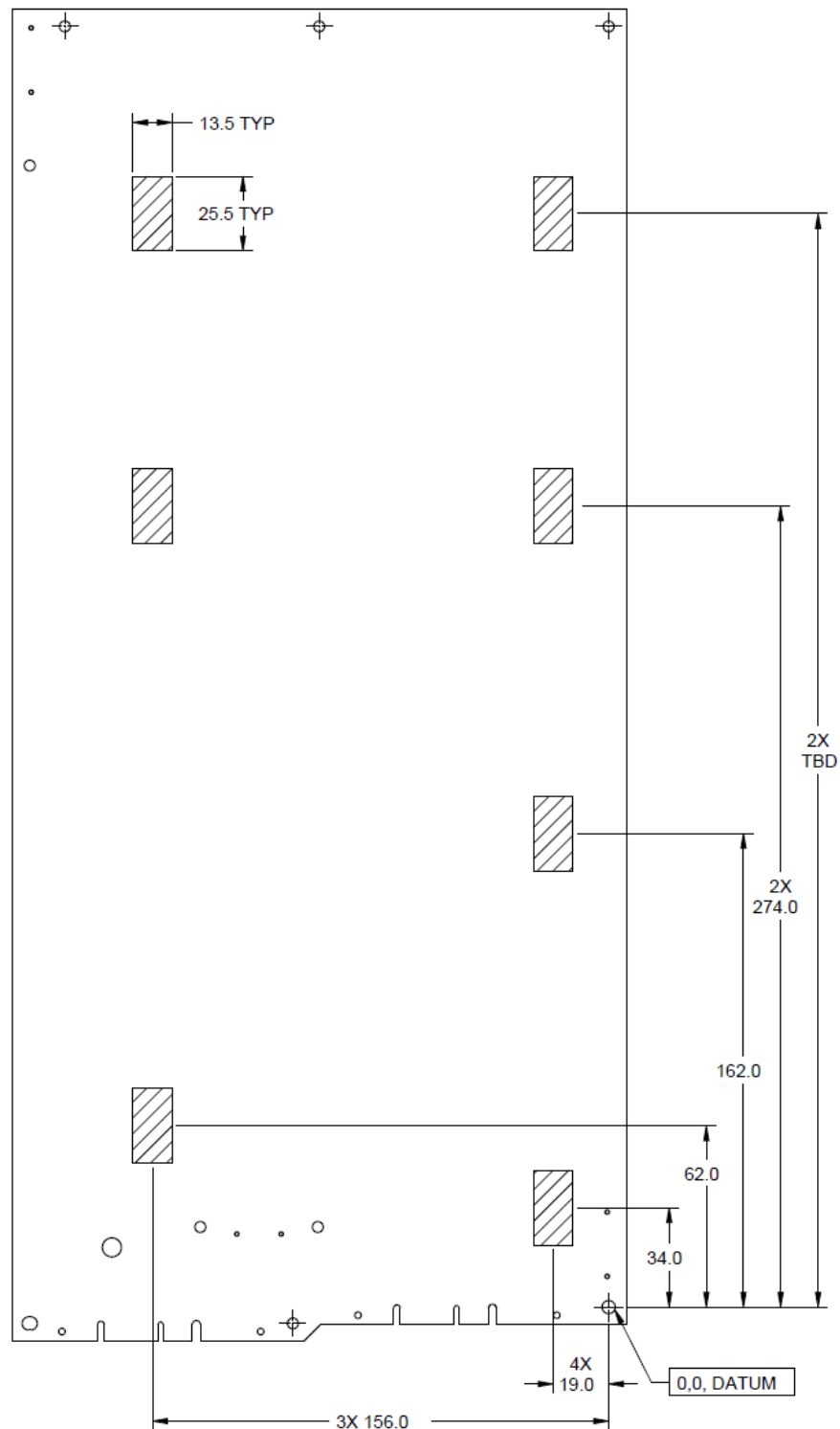
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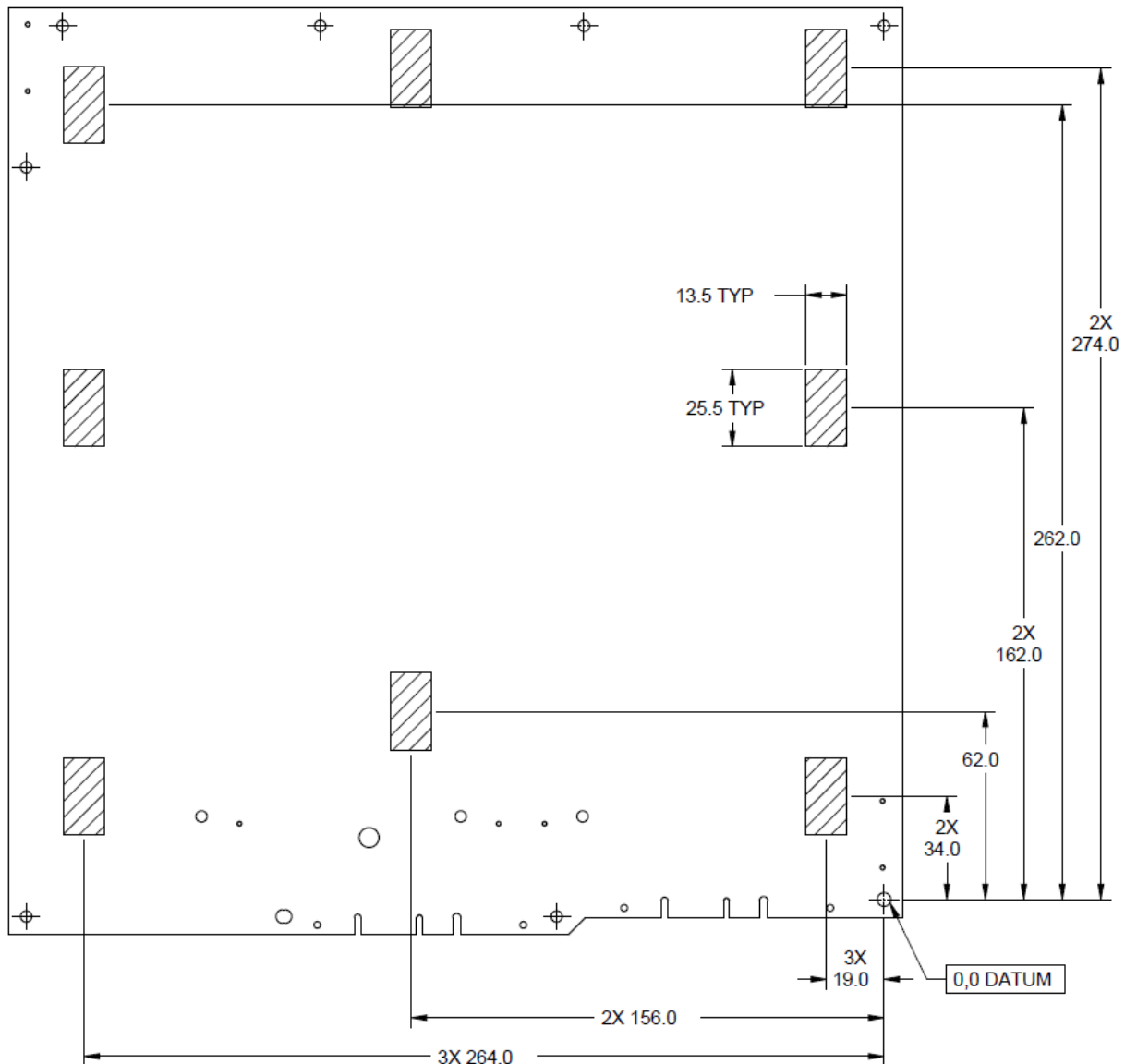
**Figure 14: Type 2 HPM Secondary Side Chassis Hook Locations**



**Figure 15: Type 3 HPM Secondary Side Chassis Hook Locations**



530

**Figure 16: Type 4 HPM Secondary Side Chassis Hook Locations**

### 10.3.3. Zone 3: HPM Secondary Support Requirements

535 To ensure maximum flexibility of HPM primary side layouts, secondary supports need to be incorporated under the DIMM Sockets and / or any other area of the HPM needing extra vertical compression support. These supports help prevent the board from flexing during assembly, when downward forces are applied to the HPM from the primary side.

540 The HPM shall Implement Zone 3 KOZs near or under DIMM sockets. The size, location and quantity is not defined, and left to HPM designer.

The HPM shall provide Secondary Supports that attach in Zone 3 which are 1.78mm +/- 0.10mm thick. They are designed to be close to the board pan or chassis, and provide a vertical

deflection stop for the HPM. The materials used and methods for support are the choice of the HPM Designer.

- 545 This support height creates a common reference surface that Chassis Designers can rely on that is taller than the Secondary Component Z-Height MAX of 1.6mm.

**Implementors Note:**

If an HPM Designer and a Chassis Designer agree to transfer this responsibility for HPM Support, and the HPM Designer provides all the appropriate PCB Keepouts and Guidance necessary to relocate these supports into the Chassis Design, then it will be permissible to remove these supplemental supports from the finished HPM PCB Assembly.

#### 10.3.4. Zone 4: CPU Backing Plate Requirements

- 550 Most server HPM designs need to support CPU backing plates or stiffeners placed under the CPU as part of the CPU Socket design.

The maximum allowable CPU Backing Plate height/volume allowance shall be calculated by:

- Backing Plate allowed Height = 5.86mm – HPM thickness - 0.08mm standoff height tolerance – allowances for other backplate design req's (insulators, deflections, etc)
- See Implementors Note below for examples.

- 555 Backing plates are assumed to be allowed to protrude into cuts in the Chassis-to-Board bracketry and / or HPM sled as shown in **Figure 20: CPU Backing Plate (Zone 4)**.

**Implementors Note:**

HPM and CPU designers should consider these example Scenarios supported by DC-MHS HPM board and Backing plate thickness requirements.

| Board Thickness<br>(Nominal, mm) | Maximum Allowable CPU<br>Backing Plate Thickness (mm) |
|----------------------------------|---|
| 1.57                             | 4.21  |
| 1.93                             | 3.85  |
| 2.36                             | 3.42  |
| 2.55                             | 3.23  |
| 3.18                             | 2.60  |

#### 10.4. HPM Board and Assembly Thickness

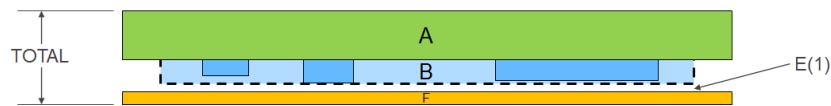
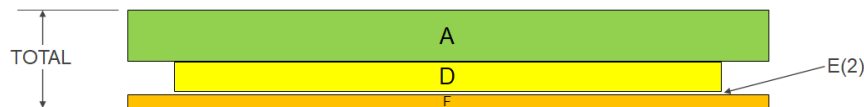
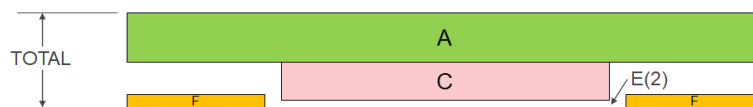
- 560 • The maximum allowed thickness and zone heights in the specification assume a minimum 5.86mm board mounting height.
  - Thickness and zone heights are established to ensure forward compatibility with 1U & 2U System Chassis assumptions.
  - Exceeding the thickness and zone height target values would result in system design impacts and incompatibilities
- 565 • The board mounting height for a given system is not within scope of the HPM specification, and is at discretion of the System designer.
- The maximum allowed HPM thickness is 3.18mm nominal and assumes +/-10% tolerance is allowed.
  - 570 • Note that PCB Tolerances of +/- 10% are supported but are not a factor in determining the fit of the CPU Backing Plate when the HPMs are mounted to standoffs by their bottom surfaces.

**Implementors Note:**

HPM and Chassis designers should consider the height stack-up of each of the 4 zones identified in **Section 10.3. Table 2** and **Figure 17 - Figure 20** demonstrate an example of a compliant stack-up for consideration. Note that the “total Z” value across the 4 zones must always be equivalent (5.86mm shown for example only).

**Table 2: Example Z-Height Compliant Stack-Up, Per Zone**

|      |                    | Zone 1       | Zone 2       | Zone 3       | Zone 4       |  |
|------|--------------------|--------------|--------------|--------------|--------------|--|
| Item | Description        | Z Value (mm) | Z Value (mm) | Z Value (mm) | Z Value (mm) | Notes  |
| A    | HPM                | 3.18         | 3.18         | 3.18         | 3.18         | MAX Thickness (w/o Added tolerance, Assumes bottom mounting)         |
| B    | Bottom Component Z | 1.60         | 0            |              |              | MAX Height   |
| C    | CPU Backing Plate  |              |              |              | 2.60         | MAX Thickness Backplate for MAX Thickness HPM, Hole in Pan/Tray      |
| D    | HPM Bottom Support |              |              | 1.78         |              | HPM Support Thickness +/- 0.10mm, must exceed Bottom Component Z     |
| E(1) | Needed Gap         | 0.28         | 0.58         |              |              | Gap is Larger, Requires Insulation and/or Clearance                  |
| E(2) | Resultant Gap      |              |              | 0.10         | 0.08         | Gap is Small, Contact between Parts is either Desired or Permissible |
| F    | Board Pan          | 0.80         |              | 0.80         |              |  |
| G    | Chassis Hook       |              | 2.10         |              |              | MAX Height from Inside Surface of Chassis                            |
|      | TOTAL              | 5.86         | 5.86         | 5.86         | 5.86         | Example Solution Stack-up  |

**Figure 17: Secondary Side Components (Zone 1)****Figure 18: Chassis Hook Keepouts (Zone 2)****Figure 19: HPM Secondary Support (Zone 3)****Figure 20: CPU Backing Plate (Zone 4)**

**Implementors Note:**

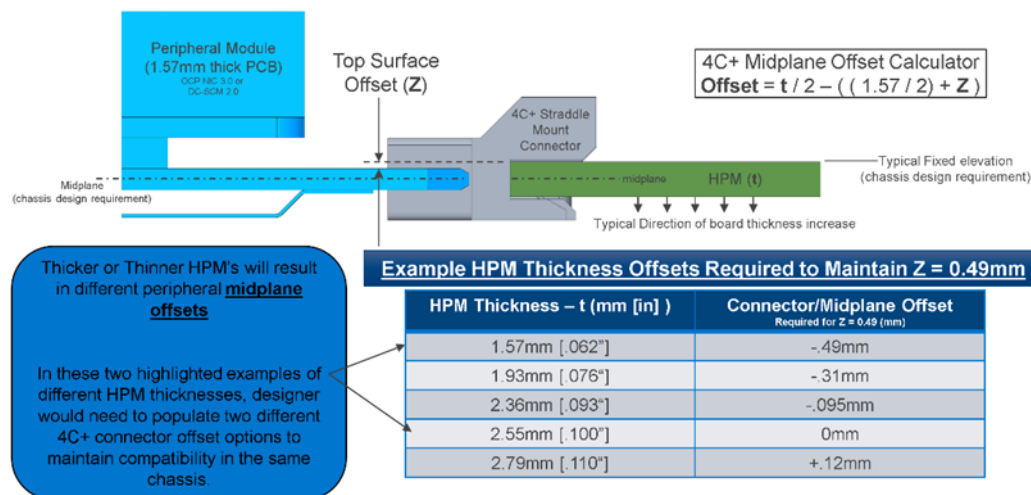
Designers should consider that variations in HPM thickness combined with 4C+ connector selection may result in variation of the vertical offset locations of OCP NIC V3 and DC SCM 2.0 peripherals relative to fixed chassis openings and the primary surface of the HPM. There are common connectors in the industry which will result in varying offset locations.

The diagram below demonstrates how selecting the variance of midplane offset within the 4C+ connector can enable a common resulting peripheral offset relative to the primary surface for varying HPM thickness (example offset  $Z = 0.49$ ).

Note, the host thickness examples shown are common at the time of this specification being published, however, alternate thicknesses may become common in the future.

Designers should consult with vendors of SFF-TA-1002 4C+ to determine best options for their chassis application.

### 4C+ Straddle Mount Connector Offset Example

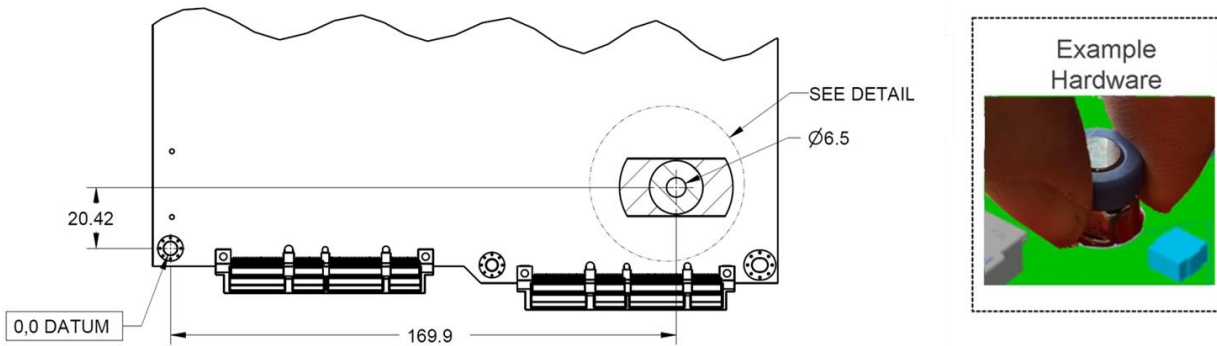
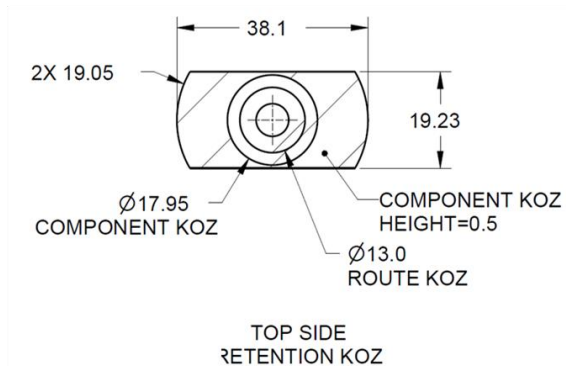
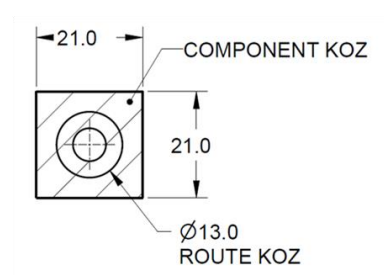


575

## 10.5. HPM to Chassis Retention Mounting

The HPM and Chassis-to-Board Bracket assembly requires retention to the chassis base. There shall be a hole required for motherboard retention to the chassis. The hole is sized for common retention methods such as plungers, thumbscrews, etc. Hole Size, required Primary / Secondary side KOZs and height restrictions around this hole are defined in **Figure 21.**

580

**Figure 21: HPM Assembly to Chassis Retention Enablement****Top Side Details****Bottom Side Details****Implementors Note:**

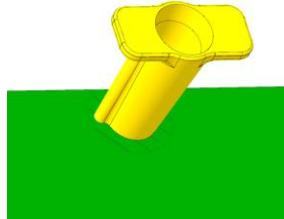
The wide shaped top side 0.5mm Height Restriction in **Figure 21** is in place for finger grip allowances around the retention hardware (which could be a plunger, thumbscrew, wing screw, etc.). Due to hardware and touchpoints being in this area, the goal is to minimize the size of components that could potentially be damaged by fingers coming in close contact to the board surface.



## 10.6. HPM Handle Hole

585 The HPM shall require a hole interface to a mechanical handle. This handle solution may be implemented with, but is not limited to, a plastic handle. An example is shown in **Figure 22**.

*Figure 22: Example Board Handling Feature*



### Implementors Note:

While the hole is required, HPM and / or System designers may choose to not utilize hardware in the hole location and instead provide alternate solutions to assist in board handling. As an example, if the hole location is not accessible when large thermal solutions are installed the designer may instead choose to provide a handling feature / touch point not tied to the HPM itself.

590 The hole location shall be near the Far side edge of the HPM. HPM Designers may choose to either:

1. Replace a required mid-board mounting hole along the Far Side edge (1 hole choice on Type 2 / Type 3, 2 hole choices on Type 4) with the board handle hole. **Figure 23** demonstrates this using a Type 2/3 board for example purposes.

595 **OR**

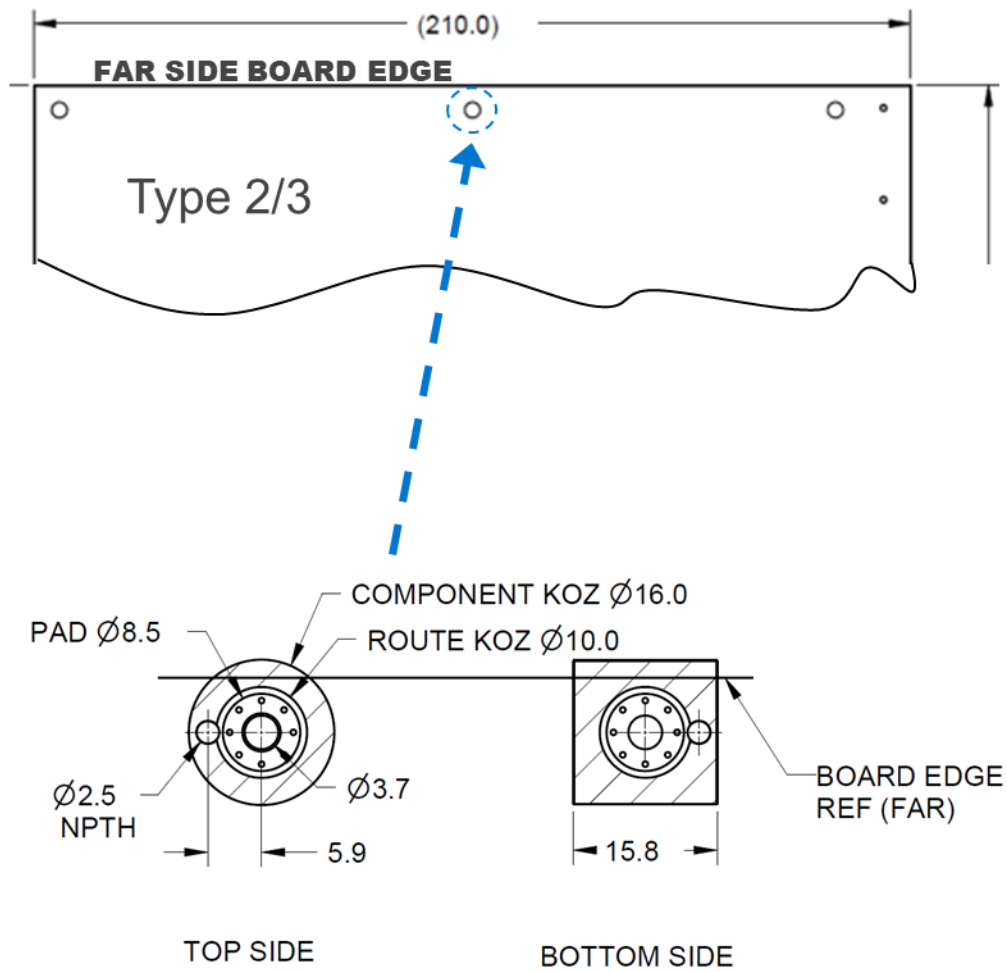
2. Add an additional hole near the Far Side Edge with consideration for Compute Core Details such as cabling for HSIO.

600 The Board Handle hole may also be considered a mounting hole for structural purposes. For example, a designer does NOT need to place a board mounting hole in close proximity to the Board Handle Hole.

The board handle hole shall follow the required dimensions and KOZ in **Figure 23**.

605

**Figure 23: Geometry and KOZ for HPM Handle Hole and Optional Placement Location**



## 10.7. OCP NIC R3 and DC-SCM R2 at Near Edge Locations

This specification defines fixed placement for certain peripheral connectors to maximize reuse across designs.

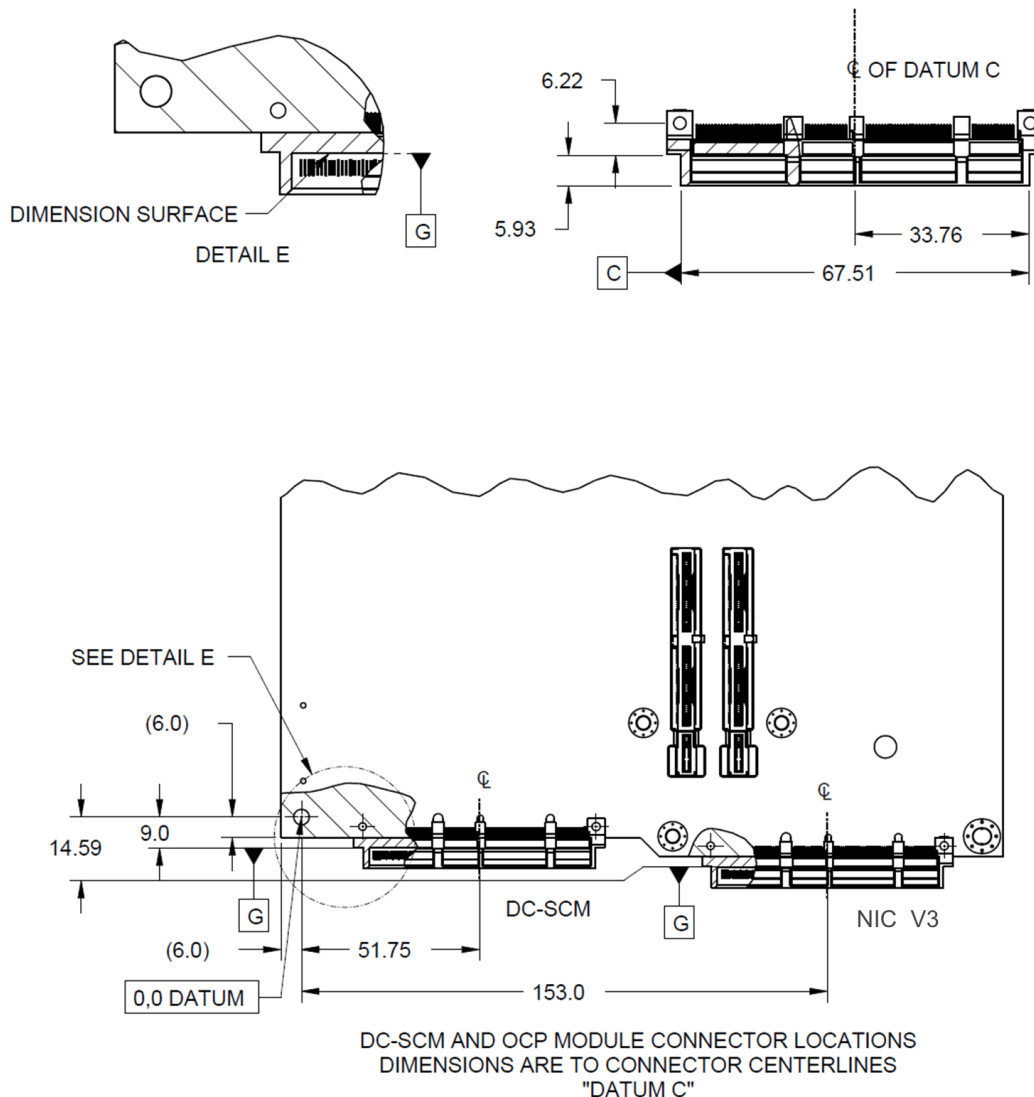
These fixed peripheral subsystem connectors are:

- OCP NIC R3.0
- DC-SCM R2.0

Each of these peripherals leverages connectors defined by SFF-TA-1002, including centerline definitions referenced in the Figures of this specification (Refer to the [DC-MHS Connector List](#) for vendor part number details).

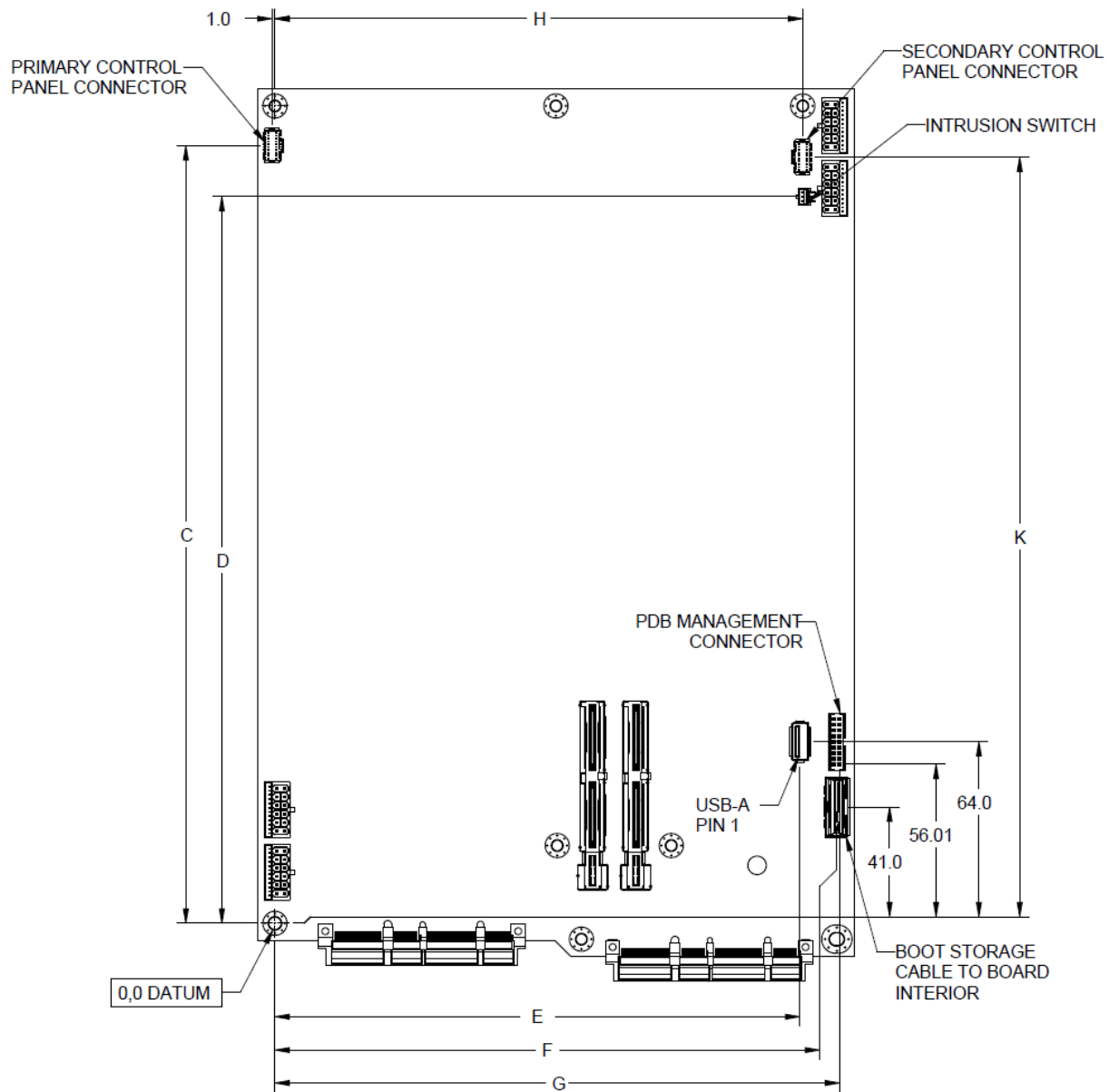
The location of each of the connectors shall be as defined in **Figure 24.**

**Figure 24: Locations of OCP NIC 3.0 and DC-SCM 2.0**



## 10.8. Platform Infrastructure Connector Placement

**Figure 25: Platform Infrastructure Connector Recommended Placements**



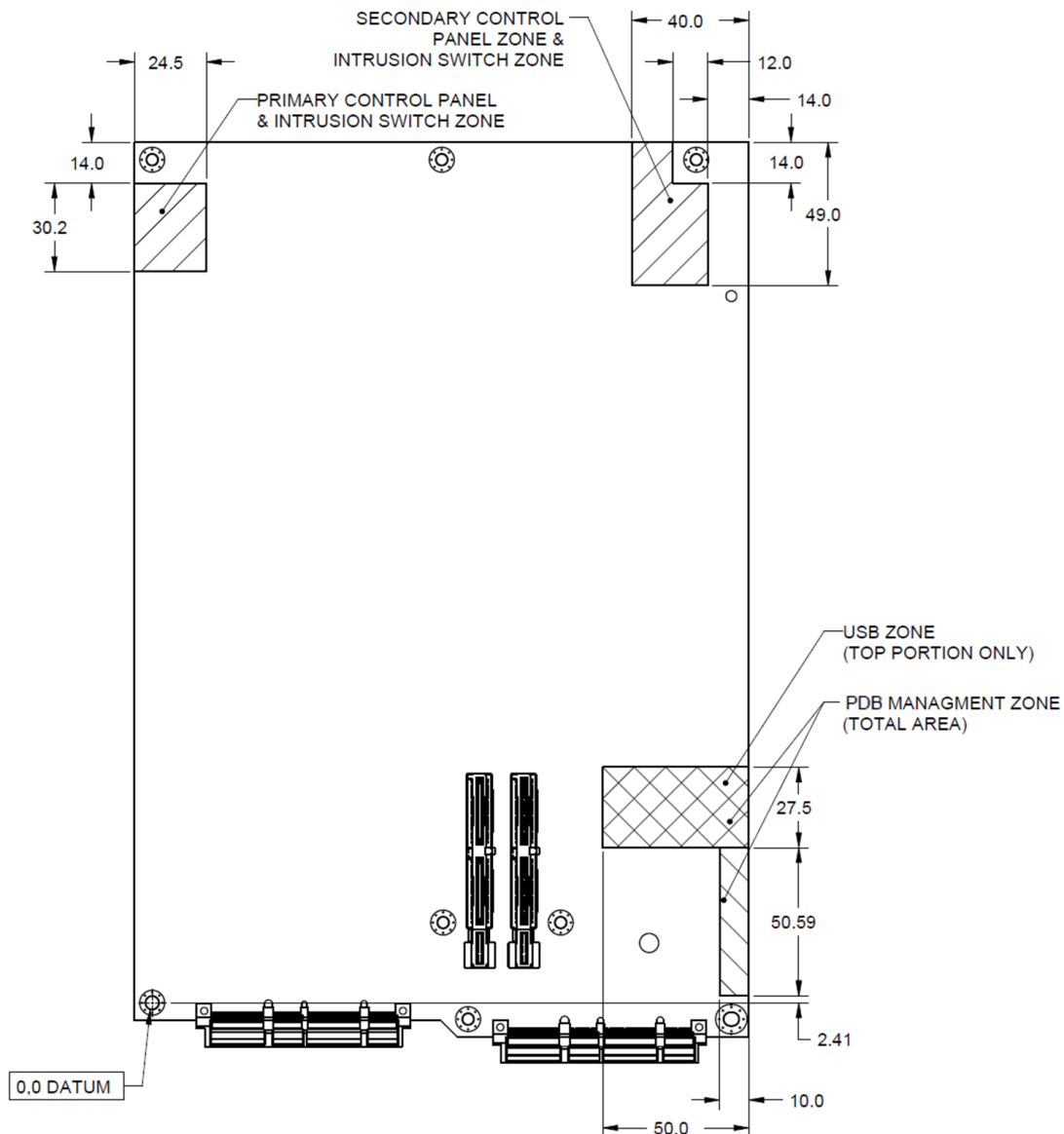
| MISCELLANEOUS CONNECTORS |           |     |     |     |       |     |     |
|--------------------------|-----------|-----|-----|-----|-------|-----|-----|
|                          | DIMENSION |     |     |     |       |     |     |
|                          | C         | D   | E   | F   | G     | H   | K   |
| TYPE                     | MID       | MID | MID | MID | PIN 1 | MID | MID |
| 2                        | 274       | 256 | 185 | 198 | 200   | 186 | 270 |
| 3                        | TBD       | TBD | 185 | 198 | 200   | 186 | TBD |
| 4                        | 274       | 256 | 270 | 283 | 285   | 285 | 270 |

**Figure 25** depicts the recommended location of the miscellaneous connectors defined in the M-PIC specification which are relevant to M-DNO HPMs. Additional information on these connectors is available in **Section 12.2 – Section 12.6** of this document.

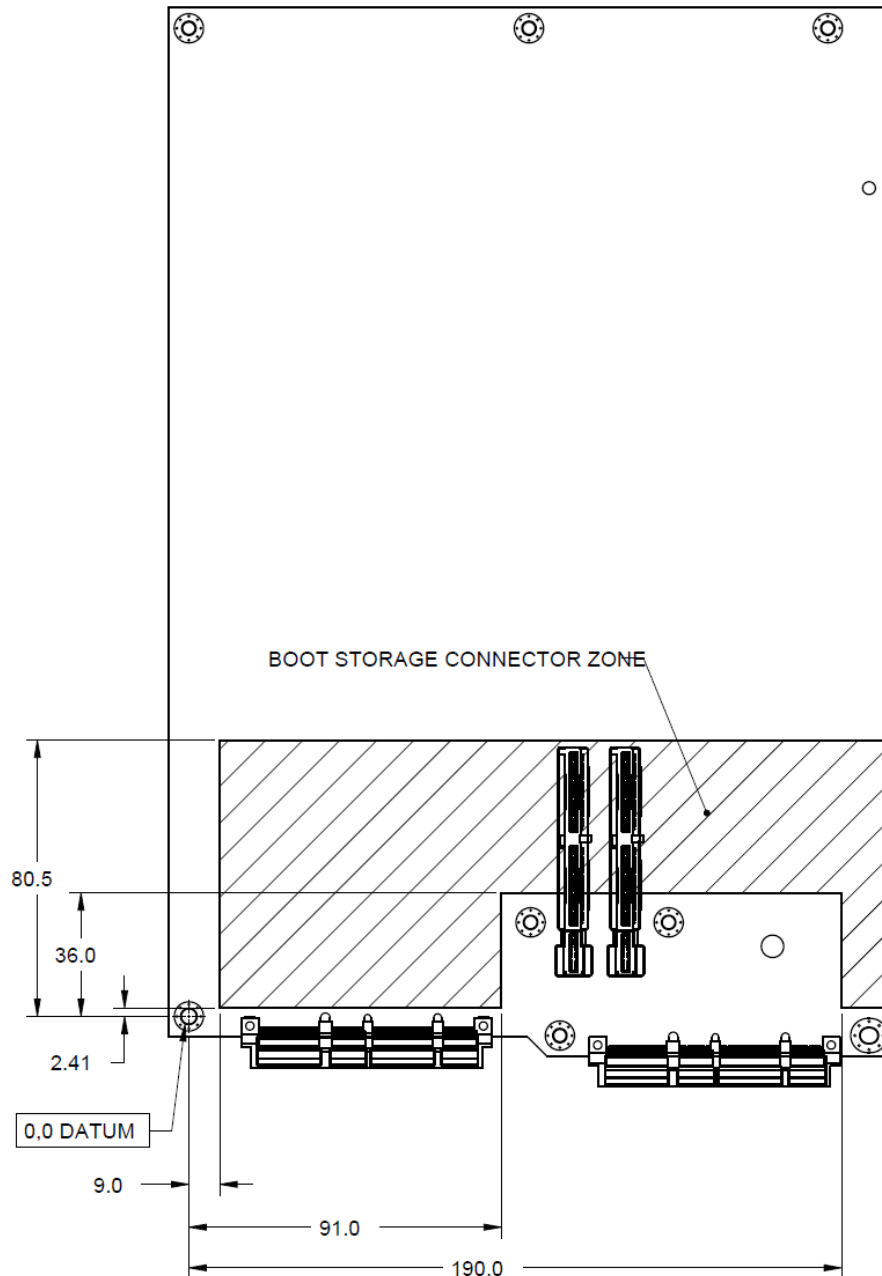
Note that a Type 2 board is represented but applicable dimensions are provided for all board types. These dimensions are intended to provide recommended connector locations that are consistent relative to the closest board corner across all board types.

To ease board layouts while maintaining interoperability, placement zones are specified in **Figure 26 - Figure 28** that connectors may move within if they cannot be placed in the recommended location. Placement of these connectors shall always be within the specified zone. Note that the intrusion switch can share either the primary or secondary control panel zone.

**Figure 26: Intrusion, Control Panel, USB and PDB Management Placement Zones**

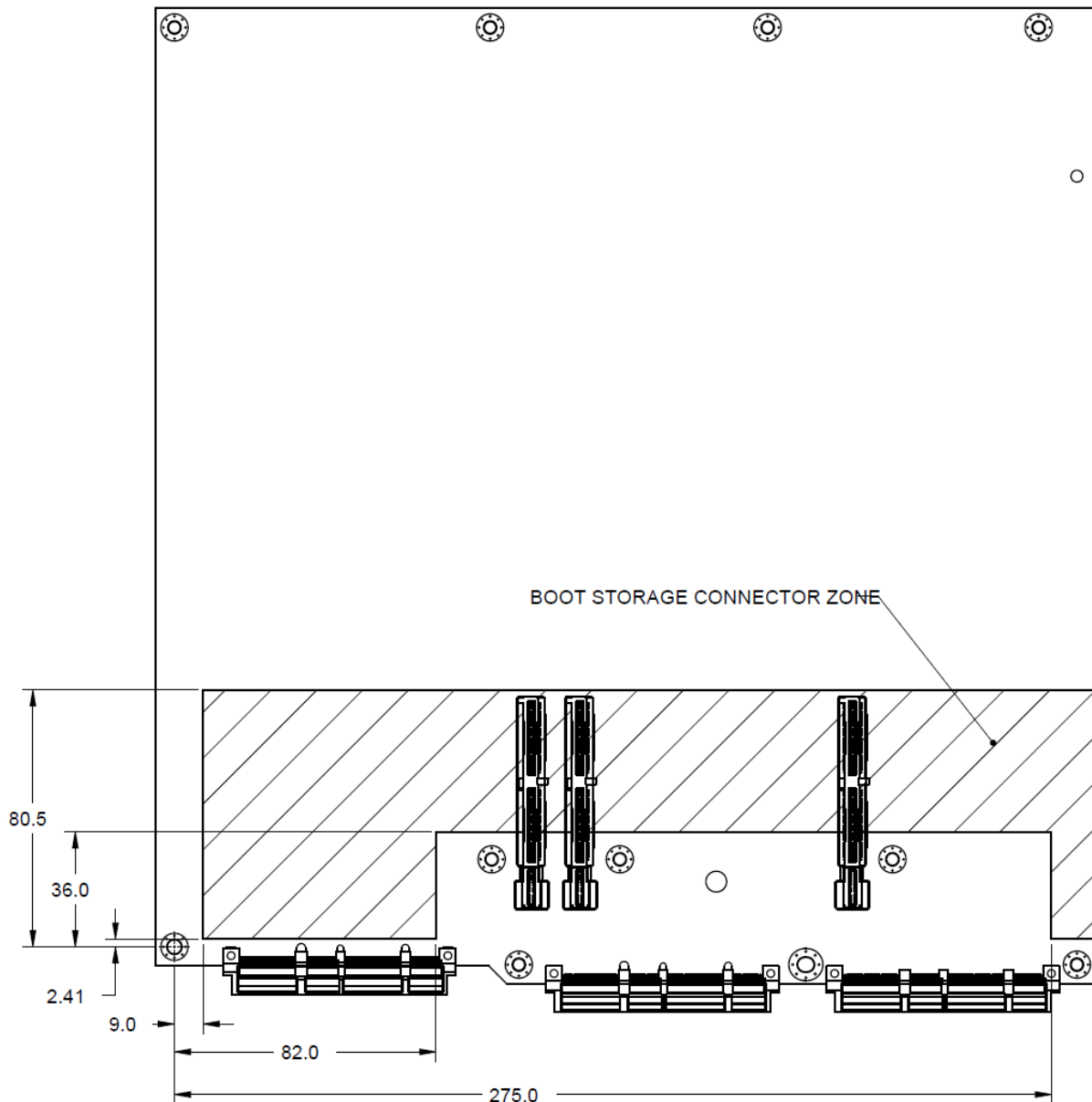


**Figure 27: Boot Storage Placement Zone Type 2/3**



640

**Figure 28: Boot Storage Placement Zone Type 4**



## 10.9. Near Side IO Connectors

645 The M-DNO specification defines multiple HPM Type outlines which support different fixed riser configurations. In addition to any fixed riser implementation(s), cabled high speed I/O (HSIO) connectors may also be placed on the near side of the HPM.

### 10.9.1. Cabled Near Side IO Connectors

If cabled HSIO connectors are implemented, it is recommended to use the connector(s) defined in **Section 12.1** with signaling defined by the M-XIO specification. Placement of these cabled

connectors is not defined but must adhere to primary side component height restrictions (**Section 10.12**).

### 10.9.2. Fixed Riser Connector Locations

To enable chassis and I/O subsystem reuse, three fixed riser locations are defined

- ½ Width M-DNO HPM Types (2/3) support Riser locations 1 and 2
- ¾ Width Types (4) also support Riser location 3.
- Implementation of each riser location is **optional** across all M-DNO board Types.
- HPMs which implement fixed risers shall do so in any / all of the three specified locations
- Utilization of the SFF-TA-1033 connector described in **Section 12.1** is strongly recommended

**Figure 29** dimensions the recommended riser connector in the appropriate (required) locations

While utilization of the recommended connector is encouraged, alternate riser connectors are permitted but shall adhere to the following rules as dimensioned in **Figure 30** and summarized in **Table 3**:

1. Connector locations are fixed horizontally (X – direction)
  - a. The ‘X’ dimensions in **Figure 30** indicate riser centerlines. If a chosen connector centerline is offset from the riser centerline, the designer shall adjust the connector location to accomplish the defined Riser centerline.
2. Connector locations are fixed vertically (Y – direction)
  - a. The dimensioned locations in **Figure 30** represent ‘Y’ length placement zones the connector must fit within
  - b. Riser connectors ‘Y’ dimension shall not exceed the specified connector zone
  - c. The riser connector shall be oriented such that the connector face closest to the near HPM board edge must align with the near end of the connector zone (i.e. must align to the 11.65mm reference from datum)

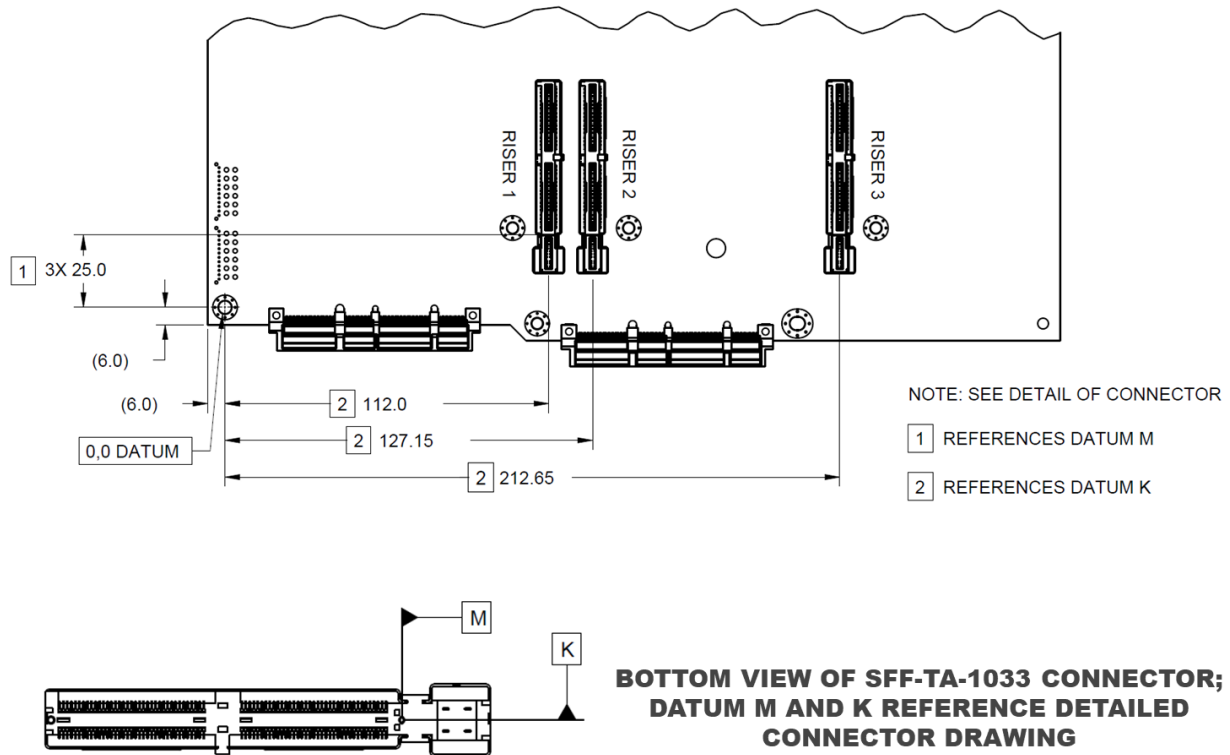
Note: Requirement 2c is intended to force a fixed placement for a given riser connector across HPMs from different designers to enable reuse of risers and other system elements.

**Table 3: Near IO Riser Attribute Requirements**

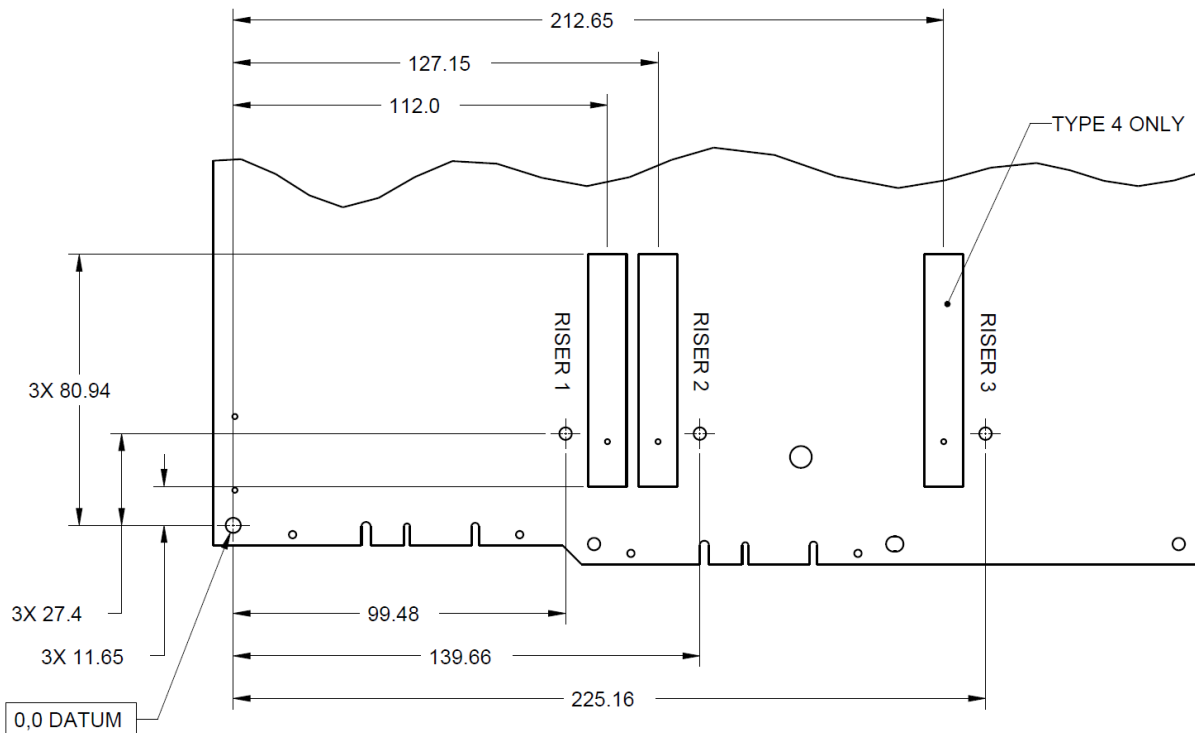
| Item                        | Requirement  |
|-----------------------------|--|
| Connector Choice            | Strongly recommended   |
| X-dimension location        | Required for each implemented riser location, regardless of connector choice |
| Y-dimension location        | Required for each implemented riser location, regardless of connector choice |
| Retention hole X-Y location | Required, regardless of whether the riser is implemented or not              |



**Figure 29: Required Riser Locations with Recommended Connector**



**Figure 30: Fixed Riser Connector and Retention Hole Locations**



## 10.10. Far Side IO Connectors

IO connector locations on the Far side of the HPM are not specified because they are all assumed to be cable-only connections and will not have major dependencies to chassis or subsystem reuse compatibility. The designer is free to choose/place these however they wish while respecting component height restrictions and other specified elements such as the Ingress / Egress power zone. It is recommended that high speed connectors placed on the Far Side leverage connector(s) described in **Section 12.1**.

## 10.11. Riser Retention Hole Requirements for Near Side

There are required holes associated with each Near IO fixed riser location regardless of whether the riser connector is implemented. The intent of requiring these holes is to always make retention holes available to system designers (including systems with cable based I/O).

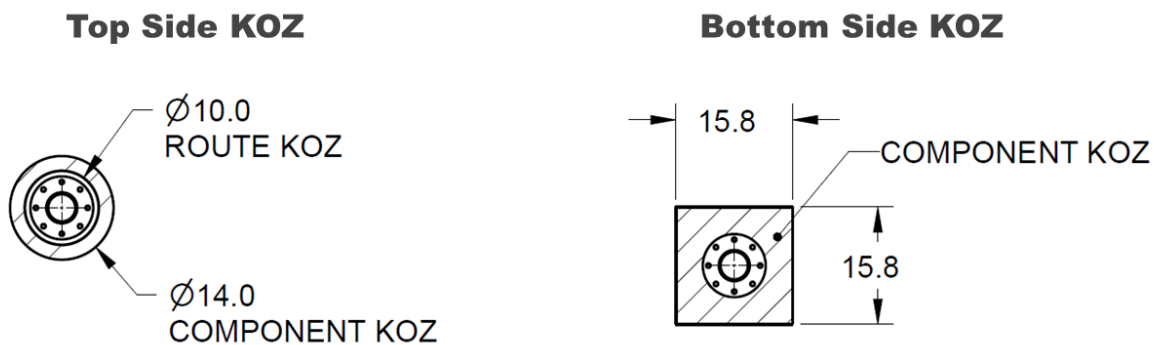
These holes are intended to be used for mechanical module retention (such as PCIe Risers, or other modules that require mechanical retention in the HPM area). There is one associated hole per defined riser location as shown in **Figure 30: Fixed Riser Connector and Retention Hole Locations**.

- The retention holes associated with Riser 1 & Riser 2 are required on all M-DNO HPMs
- The retention hole associated with Riser 3 is required on all M-DNO Type 4 HPMs

Hole and pad dimensions follow standard mounting hole requirements as defined under Detail A of **Figure 8: Hole Detail Reference**.

Required KOZs around the holes are shown in **Figure 31** (note that there is a slight top side deviation from standard mounting holes).

**Figure 31: IO Module Retention Hole KOZs**



System designers may choose the hardware and utilization method for riser retention. The hole location was selected to minimize impact of signal routing to the fixed riser locations as well as be accessible when cards are installed.

## 10.12. Primary Side Component Height Restrictions and KOZs

715 All M-DNO board types shall adhere to a common approach of three different component height restriction zones as shown in **Figure 32** and **Figure 33**.

720 • The **12mm Zone** is intended to allow for extended heatsinks and other thermal solutions while not prohibiting cabling of HSIO. Adherence to the 12mm zone is strongly recommended. While deviations are allowed, HPM designers should limit component selections which exceed the restriction to reduce interference with system design elements which will expect to inhabit this space and may cause system compatibility issues.

725 • The **11.3mm Zone** is intended to avoid interference with PCIe CEM cards directly above the HPM and its peripherals. Adherence to the 11.3mm Zone is required.

- The **6mm Zone** is the most restrictive and is intended to prevent interference with mechanical elements in support of the fixed riser locations and retention holes. Adherence to the 6mm Zone is required.

730 Zone height restrictions apply specifically to soldered circuit board components, mated connector heights or other mated assemblies of soldered components. This does NOT apply to heatsinks of any kind, shrouds or other mechanical parts that are added to the board at a later integration stage.

Allowed exceptions to these zones are:

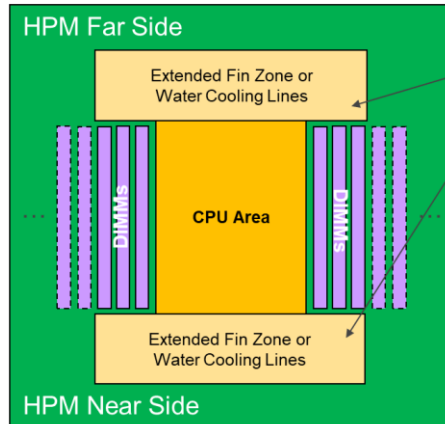
- 735
- DIMM connectors
  - Connectors in specified Fixed Riser locations (**Section 10.9.2**)
  - Plugs to connectors placed by this specification (e.g. vertical PICPWR or USB plugs).

Note that Near IO connectors outside the specified Fixed Riser locations are NOT exempt and should adhere to the defined zone restrictions.

740 This specification does not specify a specific Keep Out Zone for cable enablement.

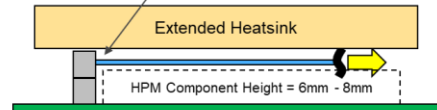
### **Implementors Note:**

HPM designers must take care with component placements relative to cabled HSIO Connectors. Placements should allow for cable routing strategies beneath the defined maximum component heights. Failure to do so will limit potential system intercepts for the HPM.



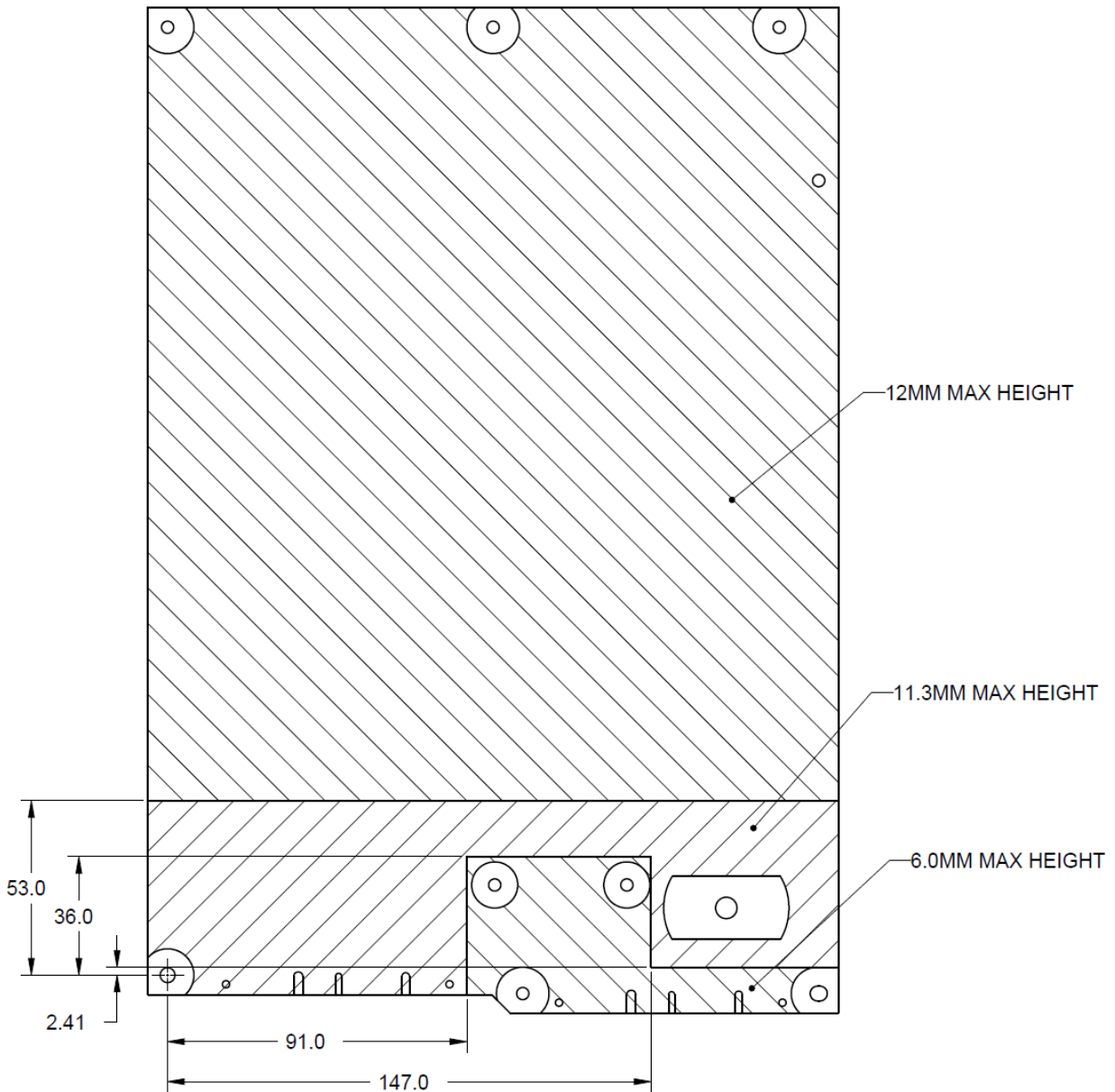
HSIO Connectors placed beneath these thermal solutions will typically require right angle plugs to fit.

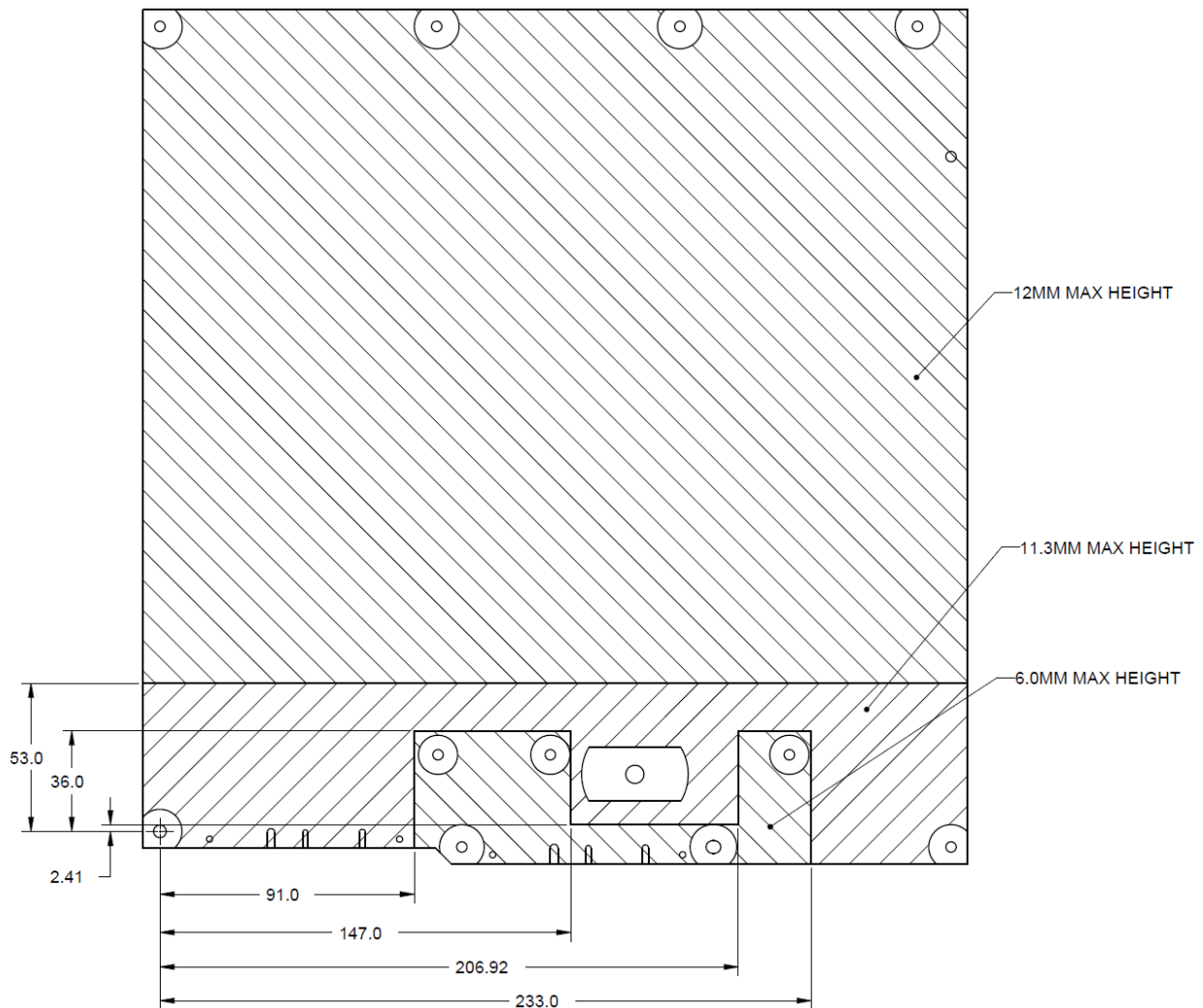
SFF-TA-1016 / SFF-TA-1026 Right Angle Plugs require Lower Component Z-Heights on the HPM to provide for Cable Routing Paths away from the HSIO Connectors.



745

**Figure 32: Type 2 and 3 Primary Side Component Height Restriction Zones**



**Figure 33: Type 4 Primary Side Component Height Restriction Zones**

### 750 10.13. Platform Custom Zone (Type 4 Only)

The Platform Custom Zone (PCZ) is defined as the Near HPM Edge between the Far side of the OCP NIC R3 and the board edge. This area is intentionally undefined, so that System Designers may provide their desired features for the target platform.

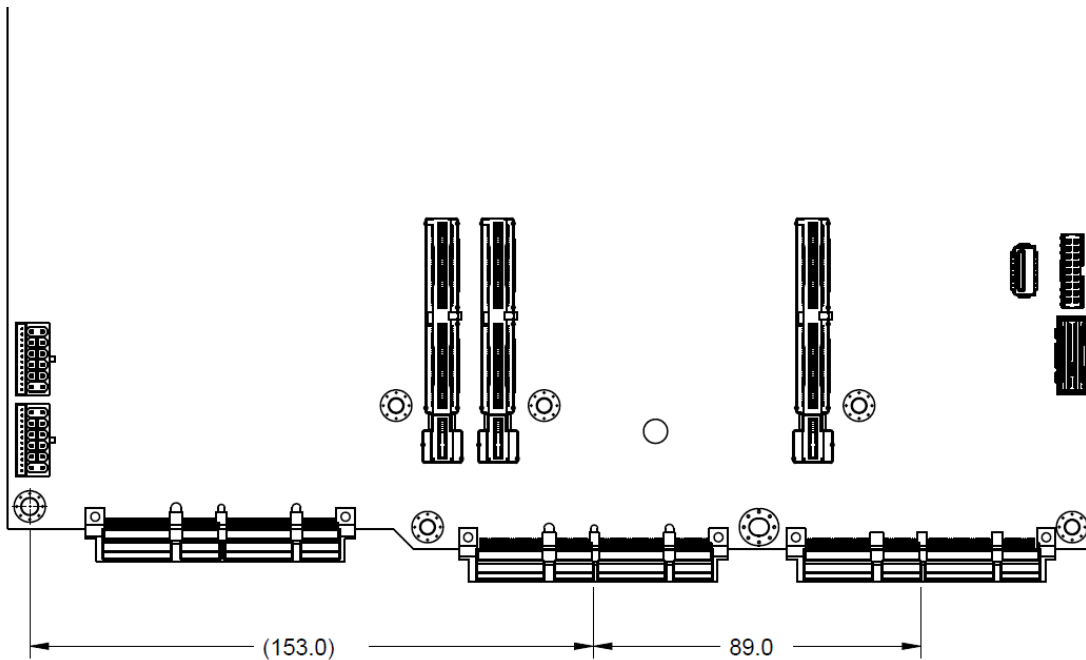
Only Type 4 HPMs support a PCZ (See **Figure 2: M-DNO Board Type Layout Overview**).

755 The specification defines some options that are considered common use cases, to promote greater compatibility between future HPMs.

#### 10.13.1. Second OCP NIC R3

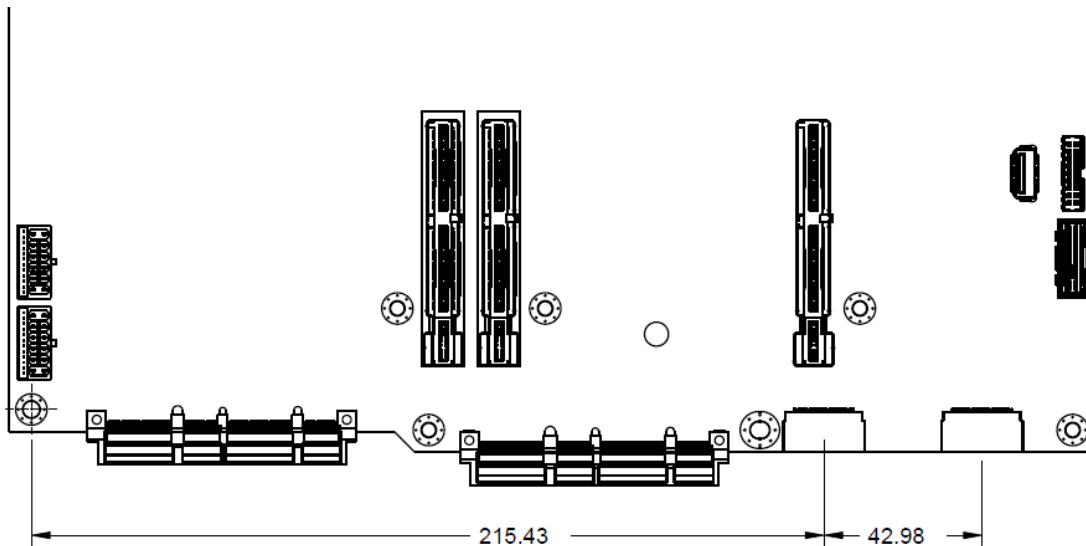
An HPM design may want to support a second OCP NIC R3. These HPM designs should follow the placement guidance in **Figure 34** for the second connector.

760

**Figure 34: Second OCP NIC in Custom Zone****10.13.2. Direct Dock E1.S**

An HPM design may want to support direct docking E1.S (EDSFF) in the Platform Custom zone. These HPM designs should follow the placement guidance for SFF-TA-1002, 1C connectors in **Figure 35**. See M-PIC specification, chapter “E1.S Direct Attach Boot Storage” for complete connector and pinout guidance.

765

**Figure 35: Direct Dock E1.S in Custom Zone**

## 11. Power Zones

M-DNO compliant HPMs are assumed to Ingress / Egress 12V DC. While alternate voltages are under consideration for future versions (e.g. 48V DC implementations), this version assumes the burden for alternate power sources is placed on the system power delivery infrastructure (PDB, bus bar, etc.). For information on Power Management (including Power Gating and use of sideband signals) refer to the M-PIC specification.

### **Implementors Note:**

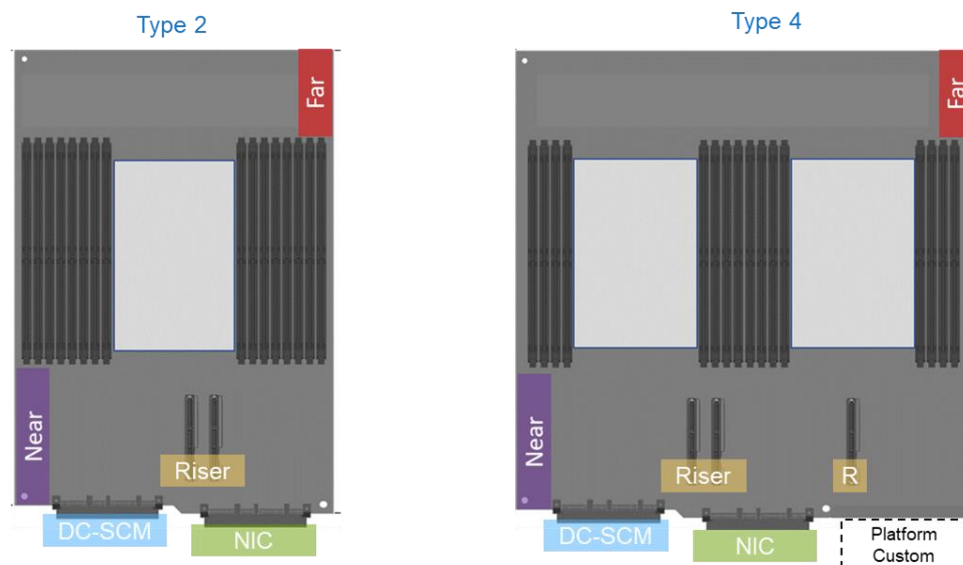
The maximum allowed voltage drop from HPM ingress to HPM PICPWR egress connectors is dependent on system configurations, loading, and downstream load input requirements. Therefore, loading and maximum allowed voltage drop are expected to be defined in private and/or public HPM design specification(s) for system configurations supported per HPM design.

### 11.1. HPM Power Zone Overview

To enable a variety of system power configurations (See **Section 14.2**) there are two defined bi-directional power zones for each HPM type referred to as the “Near” and “Far” Ingress / Egress zones as shown in **Figure 36**. These zones are intentionally placed in opposing corners of the HPM to maximize flexibility of system orientation.

Additional power zones include power egress to DC-SCM, OCP NIC and each fixed Riser location.

**Figure 36: M-DNO Power Zone Overview (Type 2 and 4 Depicted)**





## 11.2. Near and Far Bi-Directional (Ingress / Egress) Power Zones

### Ingress / Egress Cabled Power Connector

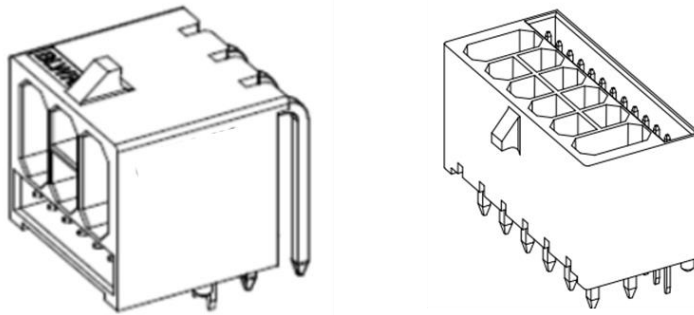
- **Power Connector Type:** 2x6+12SB and/or 2x3+6SB PICPWR .  
Refer to M-PIC Specification and [DC-MHS Connector List](#) for additional details.
- **Connector Power Rating:** 864W (2x6) / 486W (2x3)
- **Typical usage:** Power ingress to HPM and / or egress to peripheral subsystems

It is assumed that most systems will provide power to M-DNO based HPMs via a cabled solution from a Power Distribution Board (PDB).

To maximize reuse of power delivery across all M-DNO HPMs, the required connectors for all Ingress / Egress power is the 2x6+12SB or 2x3+6SB PICPWR. An example of the 2x3+6 and 2x6+12SB is depicted in Figure 37.

Refer to the M-PIC specification for more information on PICPWR compliant connectors.

**Figure 37: Example 2x3 + 6SB (Right Angle) and 2x6 + 12SB PICPWR Connector (Vertical)**



### Far Power Zone - Required

The Far Power Zone is required such that any system capable of providing power to the Far Zone of the HPM can provide ingress power to all M-DNO designs. While it is required for the HPM to implement this zone, the connector(s) may be depopulated.

- Two connector locations are defined for each board type in the Far Power Zone. Refer to **Section 11.7** for specific locations per board Type.
- One of the two defined locations (PICPWR-1 / PICPWR-2) is required and shall implement a 2x6+12SB PICPWR connector.
- The second location is optional and may implement either a 2x6+12SB or 2x3+6SB PICPWR connector if implemented.
- HPM designers electing to implement only a single connector may choose between either of the two specified locations.
- The far power zone connectors should be capable of meeting the full HPM power budget when used for ingress.

**Implementors Note:**

HPMs which implement the cabled PICPWR connectors may still be used in multi-node systems via an interposer or interface board to enable blind mate into system backplane / infrastructure. Refer to **Section 14.1** for an example of such a system.

**Near Power Zone - Recommended**

825 Due to the expected density of HPM designs in this area of the board, the Near Power Zone **may** be implemented at the discretion of the HPM designer. If Near zone power connectors are implemented, the connector(s) may be depopulated.

830 To increase the likelihood that this zone can be implemented, connectors may be placed anywhere within the designated zone area rather than having a fixed location. Refer to **Section 11.7** for this zone outline.

Within the defined zone any combination of 2x3+6SB and 2x6+12SB PICPWR connectors are allowed.

835 To maximize system use cases, it is recommended that HPM designers provide as much Ingress / Egress capability as feasible given HPM layout constraints. At a minimum, a single 2x3+6 (for egress to a peripheral subsystem) is recommended.

**Implementors Note:**

If providing Ingress power via the Near Power Zone is desired, it is recommended that the connector configuration matches the connector configuration of the Far Power zone in order to maximize flexibility for Power Ingress / Egress.

### 11.3. Fixed I/O Riser Location Power

- **Power Connector Type:** Integrated within SFF-TA-1033 Recommended Refer to M-PIC Specification and [DC-MHS Connector List](#) for additional details.
- **Connector Power Rating:** 252W
- **Minimum Power Delivered to Connector by HPM:** 87W  
**Typical usage:** Power egress for 1 (required) or more (optional) 75W PCIe CEM Devices per Riser

For each **implemented** fixed riser location (up to three):

- HPMs shall deliver a minimum of 87W of power to the riser connector (See **Table 4** for calculation of 87W effective total power required *per slot*). This requirement is defined to guarantee each riser location can support a minimum of one 75W PCIe CEM card and reduce power cabling requirements in dense systems.
- HPMs may deliver additional power to the riser connector to enable additional cards at each riser location.
- Additional supplemental I/O power (e.g. auxiliary power for a GPU) is not defined and is assumed to be provided directly by system infrastructure (e.g. cable from PDB).
- I/O Risers shall comply with M-PIC PICPWR sideband signaling requirements.

**Table 4. Minimum HPM Power Provided to Fixed Riser Locations**

| Power Rail                            | 75 W Slot <sup>1</sup>  |
|---------------------------------------|---|
| <b>+3.3Vaux</b>                       | Generated on PCIe riser. Derived from +12V  |
| <b>+3.3V</b><br>(V <sub>cc3_3</sub> ) | Generated on PCIe riser. Derived from +12V  |
| <b>+12V</b><br>Voltage<br>Current     | 12V nominal<br>7.25A total:<br>5.5 A (CEM 5.0) +<br>1.0A (VR conversion to V <sub>cc3_3</sub> ) +<br>0.35A (VR conversion to +3.3Vaux) +<br>0.40A (misc.) |

#### 11.4. DC-SCM 2.0

- 865
- **Power Connector Type:** Refer to the OCP DC-SCM R2.0 spec (Refer to **Section 13**)
  - **Connector Power Rating:** 50W (Refer to the OCP DC-SCM R2.0 spec)
  - **Typical usage:** Power egress for DC-SCM 2.0

#### 11.5. OCP NIC 3.0

- 870
- **Power Connector Type:** Refer to the OCP NIC R3.0 spec (Refer to **Section 13**)
  - **Connector Power Rating:** 80W (Refer to the OCP NIC R3.0 spec)
  - **Typical usage:** Power egress for OCP NIC 3.0

#### 11.6. Platform Custom Zone (Type 4 Only)

- 875
- Power to the Platform Custom Zone is not defined as it is considered implementation specific.

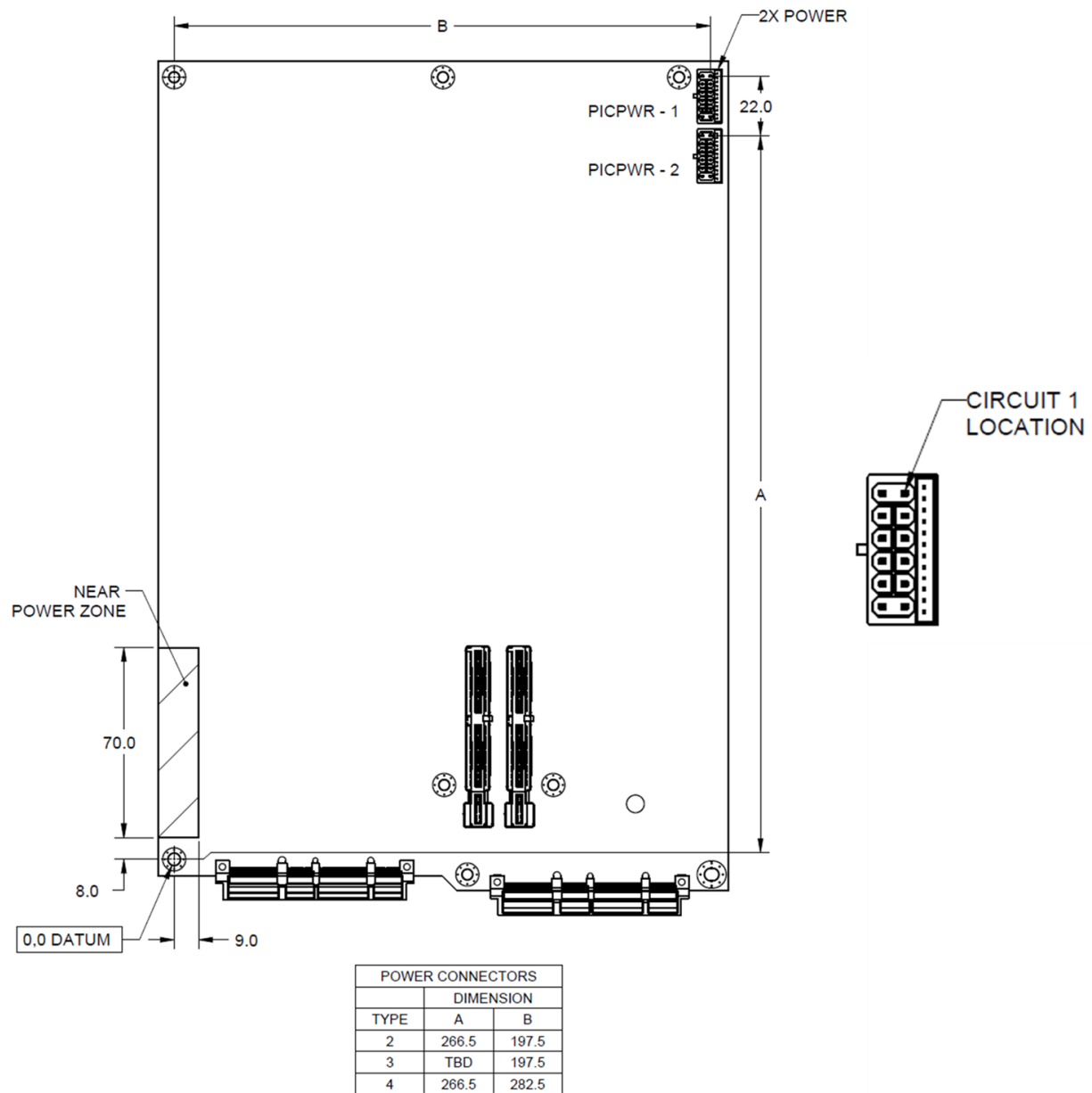
#### 11.7. Ingress / Egress Power Connector Locations

- 880
- As described in **Section 11.1** the two Far power connector locations (PICPWR-1 and PICPWR-2) are fixed for each board type with common spacing between the two locations across all board types. Dimensioning is to Circuit 1 and is intended to be consistent for 2x6+12SB or 2x3+6SB selections.

PICPWR connectors placed within the near power zone shall be numbered beginning with PICPWR-3 and incrementing for each additional connector in order of proximity to the HPM Far side (e.g. PICPWR-3 closer to Far side than PICPWR-4).

- 885
- The drawing and table within **Figure 38** define the required location(s) for each board type.  
Note that while for simplicity only a Type 2 board is depicted the dimensions listed are valid for other board types.

**Figure 38: Near and Far Power Zone Connector Locations**



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## 12. I/O System (Electrical Interfaces)

The HPM shall be required to implement electrical interfaces that must be in compliance with the DC-MHS family of specifications. Refer to **Section 6** for additional details.

HPM shall implement battery backed voltage interface per DC-SCM R2.0 "Battery Voltage" requirement.

This section provides additional guidance for specific connectors on M-DNO HPMs.

### 12.1. High Speed IO (HSIO) Connectors

HSIO connector selections are strongly suggested, but not required for compliance. Use of the suggested HSIO connectors will ensure broader compatibility with chassis, riser, and cable interfaces in the future.

Connector Choices shall be compliant with M-XIO specification.

**Table 5: M-DNO Connector Recommendations**

|             | Recommended Connector      | Note  |
|-------------|----------------------------|---|
| Fixed Riser | SFF-TA-1033                | Compatible with 1016 cabled solutions   |
| Near HSIO   | SFF-TA-1016                | Common interconnect for cabled connections and Riser solutions  |
| Far HSIO    | SFF-TA-1016 or SFF-TA-1026 | Appropriate due to low profile and ability to fit under thermal solutions with appropriate plug selection |

Refer to the [DC-MHS Connector List](#) for vendor part number details.

The Near HSIO location and flexibility is further described in **Section 10.9**.

### 12.2. Internal USB

- **M-PIC Section Reference:** "Internal USB3 Connector"
- **Connector Requirement:** Required (may be de-populated)
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Type A or C USB Compliant

Electrical implementation for an internal USB3 connector follows the M-PIC specification. It is strongly recommended that HPMs implement a Type A connector. For M-DNO HPMs the connector shall be placed as defined in **Section 10.8**.

### 12.3. Intrusion Switch

- **M-PIC Section Reference:** “Intrusion Switch”
- **Connector Requirement:** Required (may be de-populated)
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to M-PIC Specification and [DC-MHS Connector List](#)

Electrical implementation for the intrusion switch follows the M-PIC specification. For M-DNO HPMs the connector shall be placed at the location defined in **Section 10.8**.

### 12.4. Boot Storage

- **M-PIC Section Reference:** “Boot Storage”
- **Connector Requirement:** Recommended
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to M-PIC Specification and [DC-MHS Connector List](#)

Electrical implementation for boot storage follows the M-PIC specification. Due to HPM layout density it is expected that the Cable Optimized connector will be more prevalent in M-DNO designs. Type 4 M-DNO HPMs may choose to utilize the platform custom zone to enable the Direct Attach Boot Storage option. The location for Boot Storage shall follow **Section 10.8**.

### 12.5. Control Panel

- **M-PIC Section Reference:** “Control Panel Interfacing”
- **Connector Requirement:** Primary Required (may be de-pop), Secondary Optional
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed
- **Connector:** Refer to M-PIC Specification and [DC-MHS Connector List](#)

Electrical implementation for the Control Panel(s) follows the M-PIC specification. For M-DNO HPMs the Primary Control Panel is required while the Secondary Control Panel is optional, the location of both control panel connectors shall follow **Section 10.8**.

### 12.6. PDB Management Connector

- **M-PIC Section Reference:** “PDB Management Connector”
- **Connector Requirement:** Required (may be de-populated)
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to M-PIC Specification and [DC-MHS Connector List](#)

Electrical implementation for the PDB Management Connector follows the M-PIC specification. For M-DNO HPMs implementation of this connector is required and the location is defined in **Section 10.8**.

## 13. References

### Relevant Open Compute Specifications

This specification also relies on the following Open Compute Project specifications

1. OCP Server Network Interface Card (NIC) 3.0 – Specifies NIC card form factors targeting a broad ecosystem of NIC solutions and system use cases.  
[Mezz \(NIC\) » Open Compute Project](#)
2. OCP Datacenter Secure Control Module (DC-SCM) 2.0 – Specifies an SCM designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center.  
[Hardware Management/Hardware Management Module - OpenCompute](#)

### Additional Industry References

- ASMEY14.5 – 2018 Dimensioning and Tolerancing
- Open Rack V3
- SNIA SFF-TA-1002
- SNIA SFF-TA-1016
- SNIA SFF-TA-1026
- Open19



## 14. Supplemental Material

### 14.1. M-DNO Conceptual Implementation Examples

The M-DNO specification has multiple form factor types to address various product types and sizes. In this section some of the possible configurations and usages for the different Types will be shown.

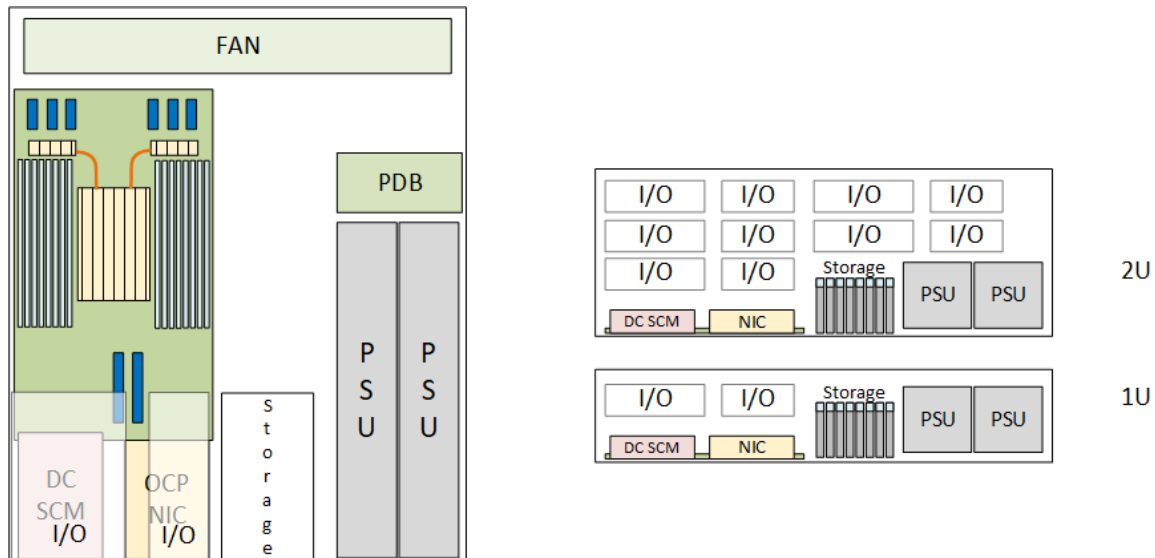
Note: Image representation of elements may not be to scale, and is subject to change

It is understood that the configurations shown represents a small sample of what could be possible. This section also conveys the reasoning behind the different sizes of HPM associated with the three types.

#### Type 2

The Type 2 HPM was optimized to provide an ideal solution for Dense (1/2 Width) 1 Socket designs. Type 2 is intended to support PCIe direct attach risers and EVAC thermal solutions as well as larger CPU sockets.

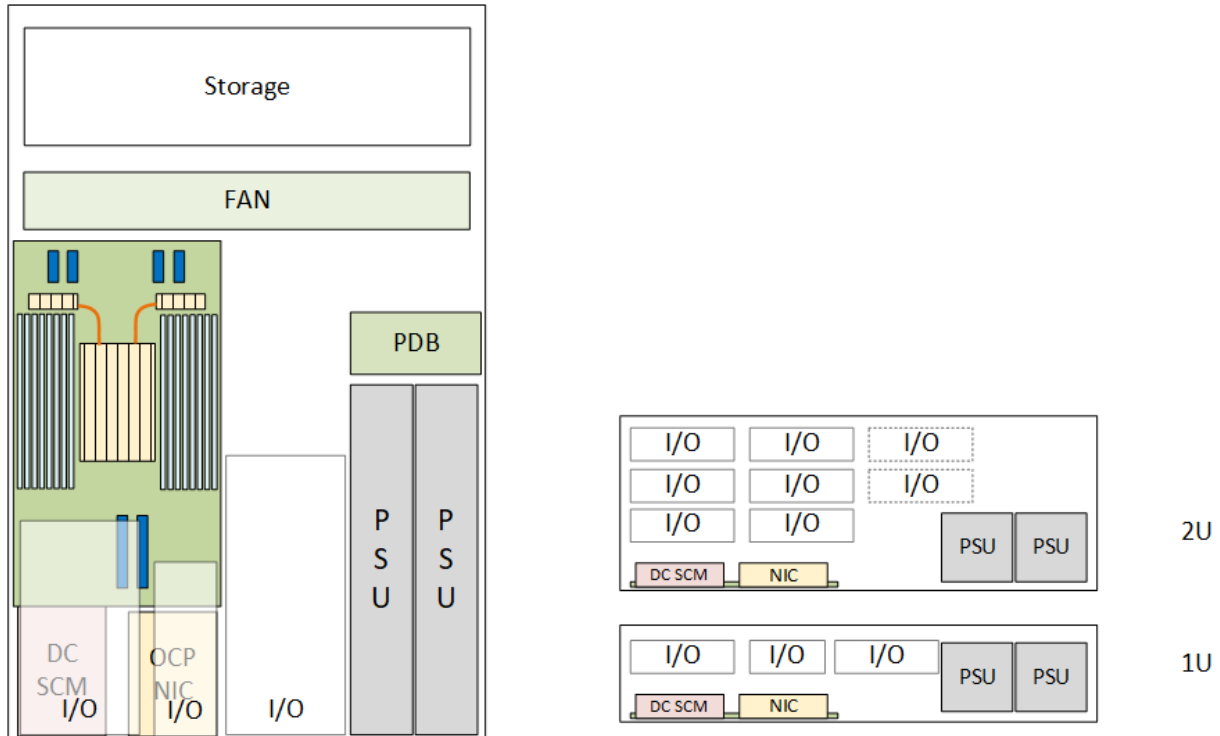
#### Type 2 Configuration Example – 1 Node Edge



1000

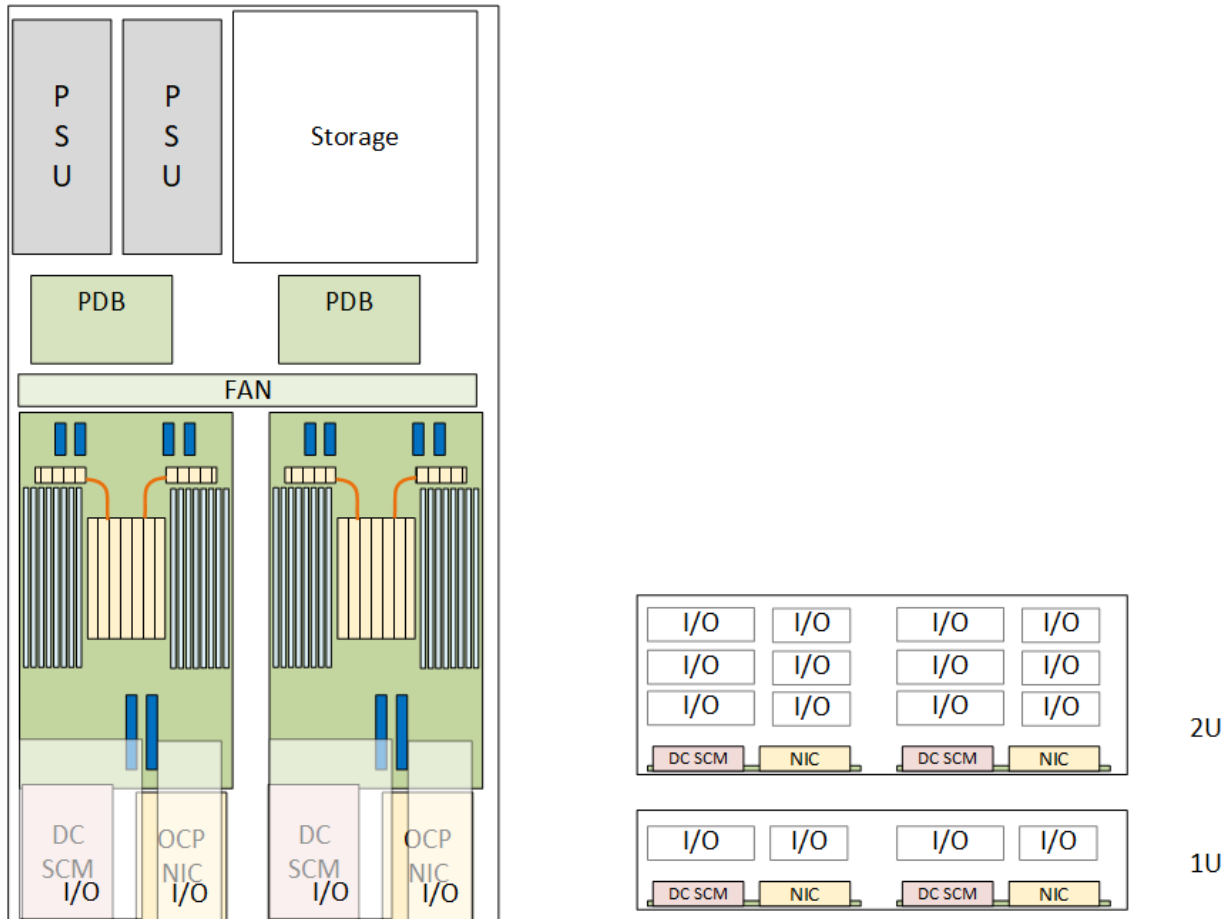
The Type 2 HPM would also be applicable for traditional enterprise server applications in or 1U or 2U heights. The variability of capabilities for I/O and Storage would be plentiful and facilitated by different riser, cable, and mid-plane configurations.

### Type 2 Configuration Example – Enterprise Server



1005 The Type 2 HPM would also be suitable for 2 (or 4) Node products.

### Type 2 Configuration Example – 2 Node

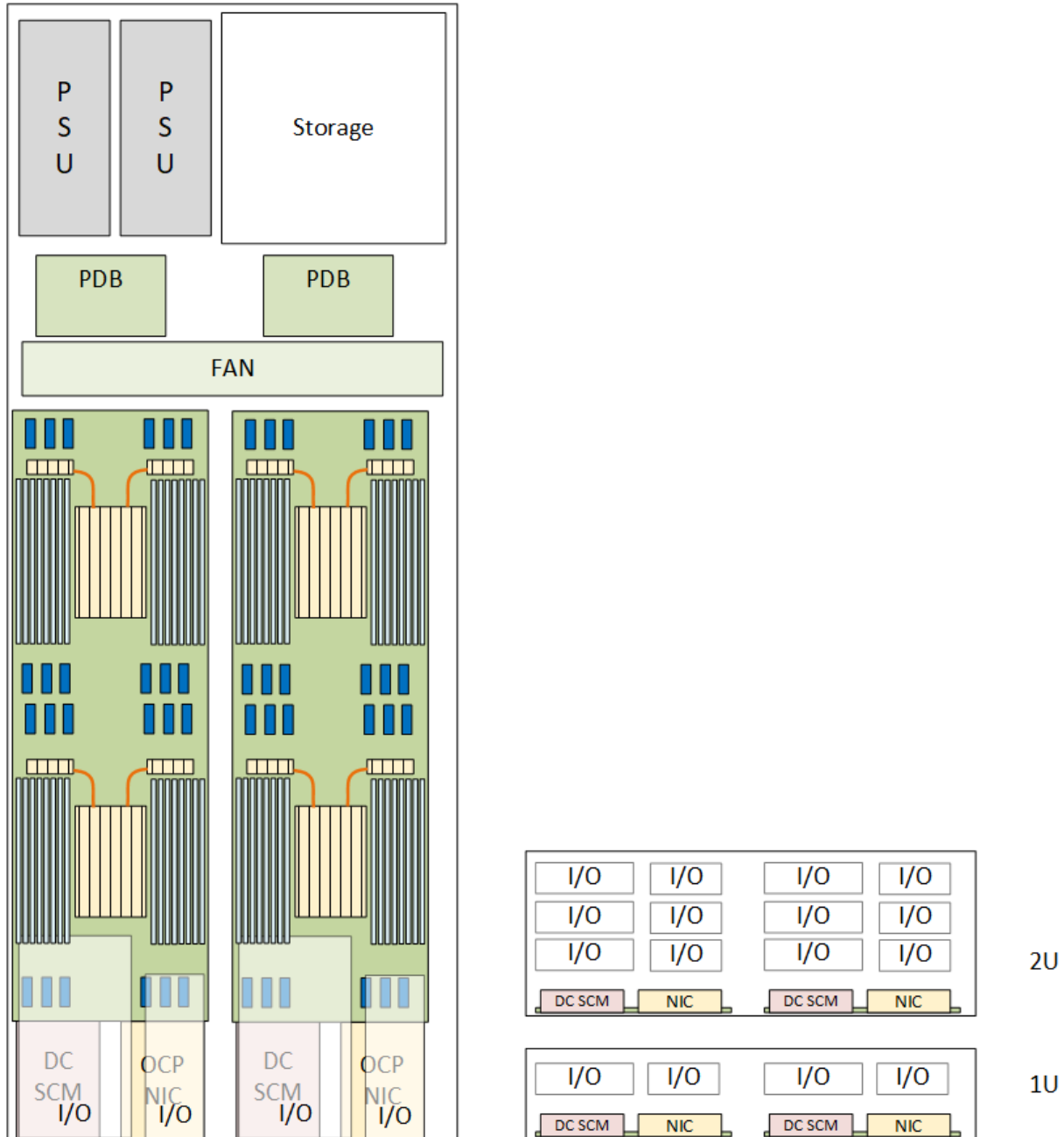


1010

## Type 3

The Type 3 HPM grows in depth to allow 2 socket “shadow core” designs, specifically to support 2 Nodes across a chassis. In this configuration the ability to utilize the full PCIe resources is deprioritized. The ability to support EVAC thermal solutions would be applicable.

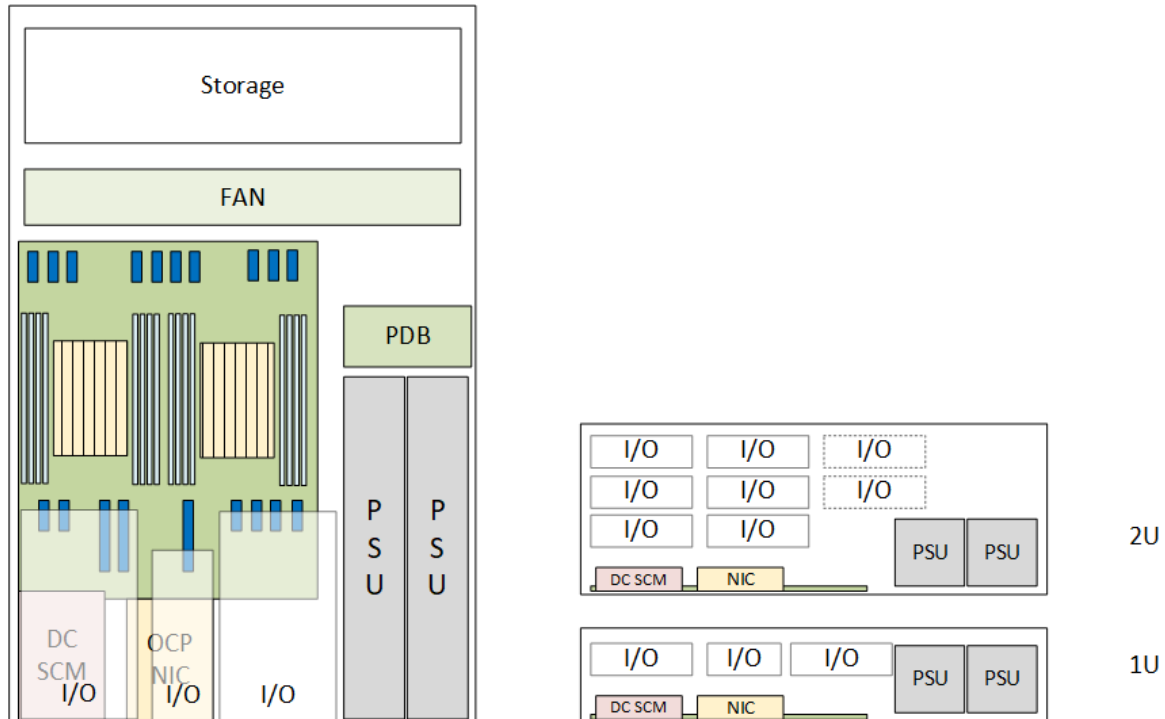
### 1015 Type 3 Configuration Example – 4 Node



## Type 4

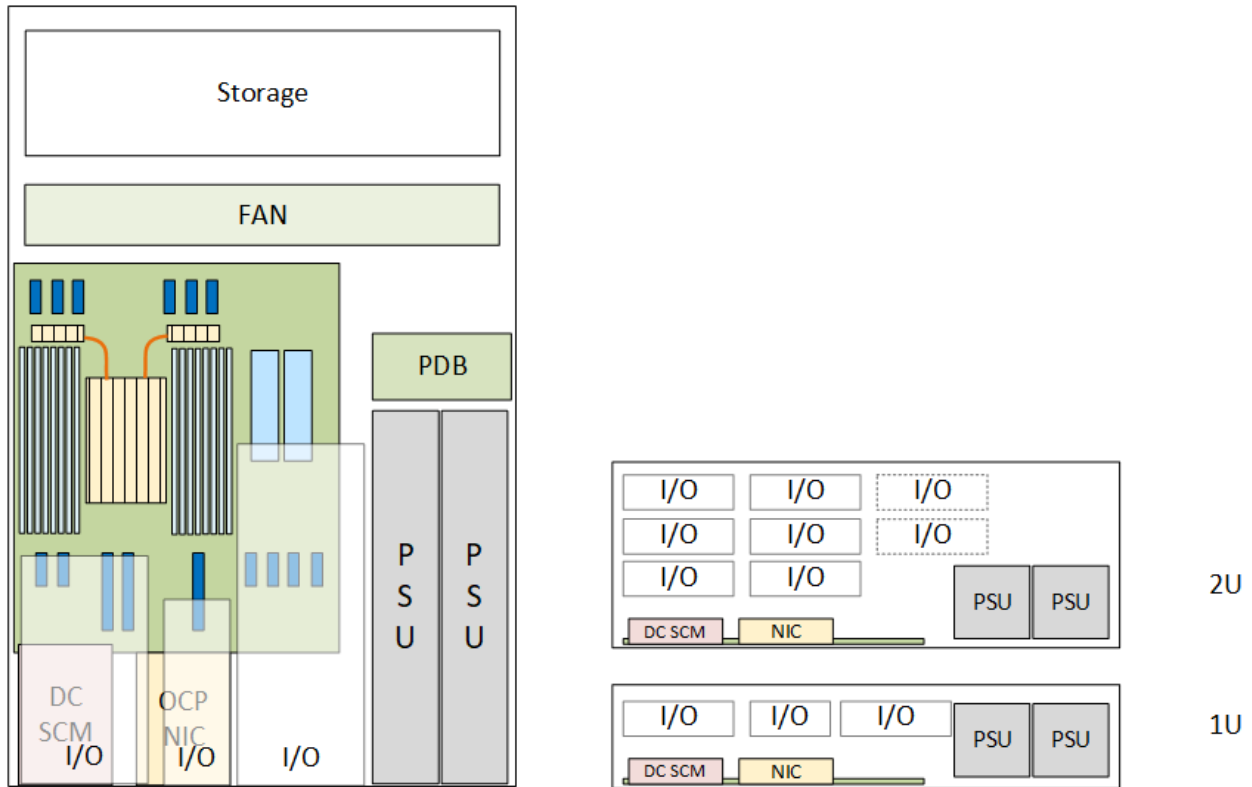
- 1020 The Type 4 HPM is the only Type to grow in width. The primary driver for the Type 4 form factor is ability to support a dual socket “spread core” 2 Node product with adjacent PSUs in a 19” (or larger) rack. To achieve this 2 socket design a concession is made on memory socket support so that only one DIMM per channel is expected on an 8 channel per socket architecture. The other features intended to be supported on a Type 4 HPM would be full PCIe lane count, and
- 1025 EVAC thermal solutions.

### Type 4 Configuration Example – 2 Socket Spread Core



1030 Another possible Type 4 HPM would be a 8 memory channel CPU with 2 DIMMS per channel as in Type 2, but with more on board peripherals than the other ½ width Types.

### Type 4 Configuration Example – Expanded Features 1 Node



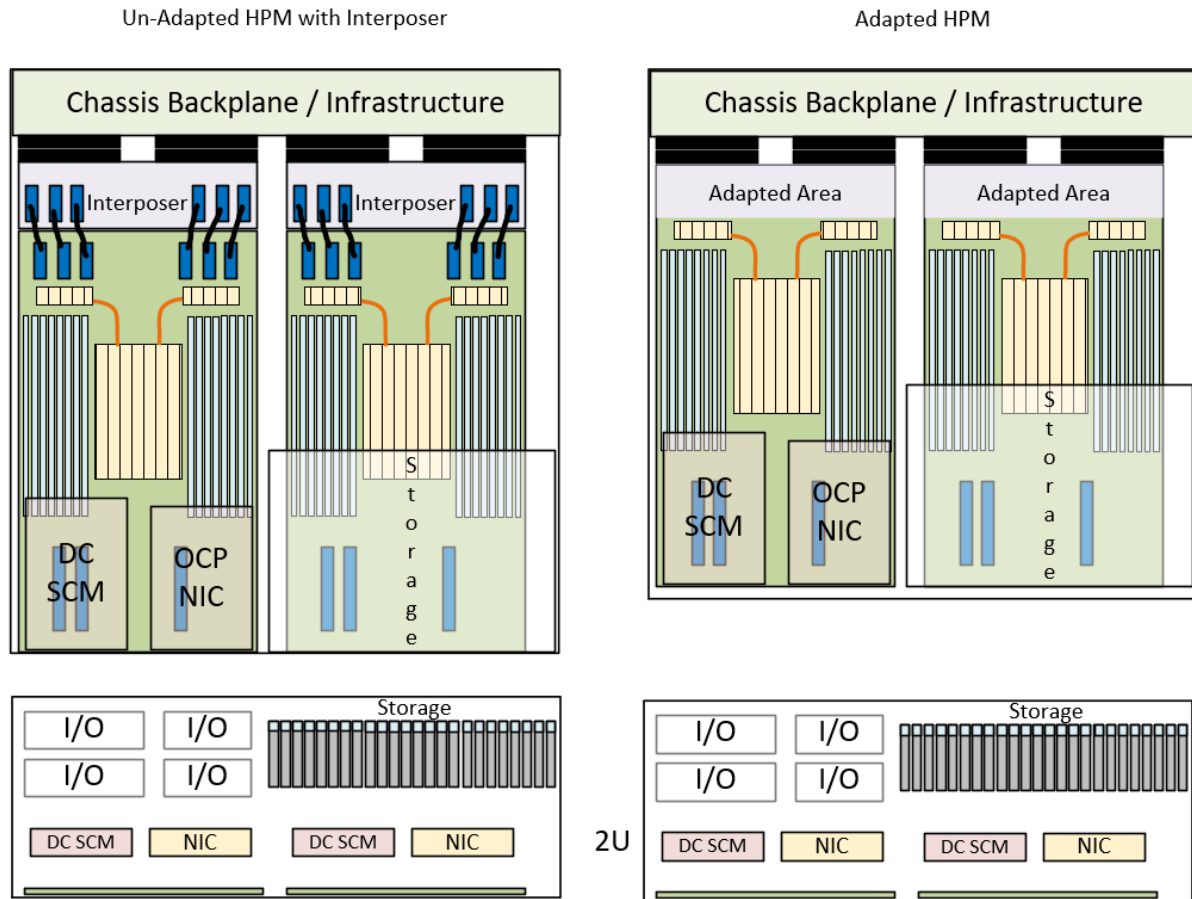
## Multi-Node Specific

### 1035 Multi-Node Adaptation

As described in the Power Zone **Section 11.1**, multi-node HPMs may choose to adapt the HPM to add board to board connectors on the Far board edge intended to directly mate into chassis power infrastructure (mid-plane, PDB, bus bar etc.).

1040 Un-adapted HPMs can also be leveraged with this type of chassis infrastructure by leveraging an interposer board between the HPM and the chassis infrastructure.

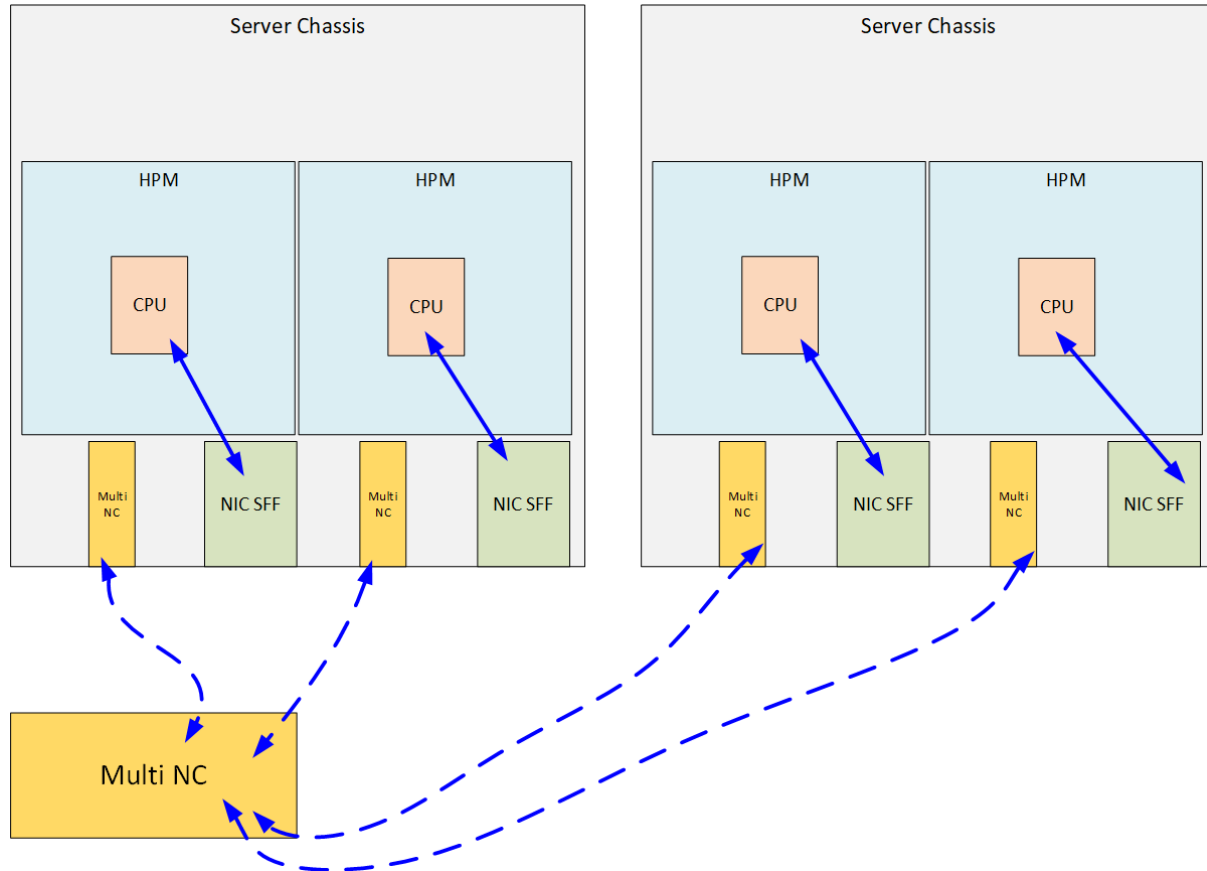
The example below depicts using an un-adapted HPM on the left and an adapted HPM on the right in a similar system. For this example, shown is a Type 2 node opting to “float” the DC-SCM and NIC cards as opposed to placing them Co-Planar. Additionally, a 21” chassis is depicted.



## Multi-Node Management

1050

How to deploy a multi-node management infrastructure using base specification compliant HPMs is outside of the scope of this specification. However, various common methodologies were evaluated to ensure that M-DNO compliant HPMs could be leveraged into these infrastructures. As an example, a small low-cost local node controller could be connected to the DC-SCM 4C+ connector and then connected to a chassis manager or multi-node controller.





## 14.2. M-DNO Power Zone Usage

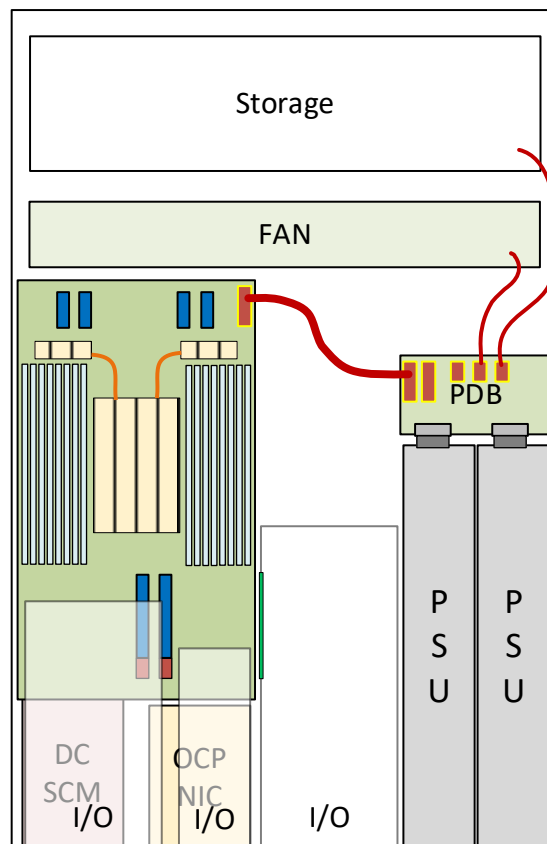
### 1055 Examples

The M-DNO specification provides some flexibility to HPM implementors and system designers when it comes to Power Zone Usage. In this section, demonstration of some expected configurations leveraging these various options are conveyed. For simplicity's sake, the different power flows are demonstrated using the same HPM board Type (Type 2), however the power zone use case flexibility is common across all board types.

The first example listed below shows a simple monolithic (one HPM) system where PSUs feed power to the system PDB, the HPM power zones are utilized in the minimum required model:

- Far Side Ingress: Power from PDB to HPM
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: None
- Supplemental Power to I/O: None

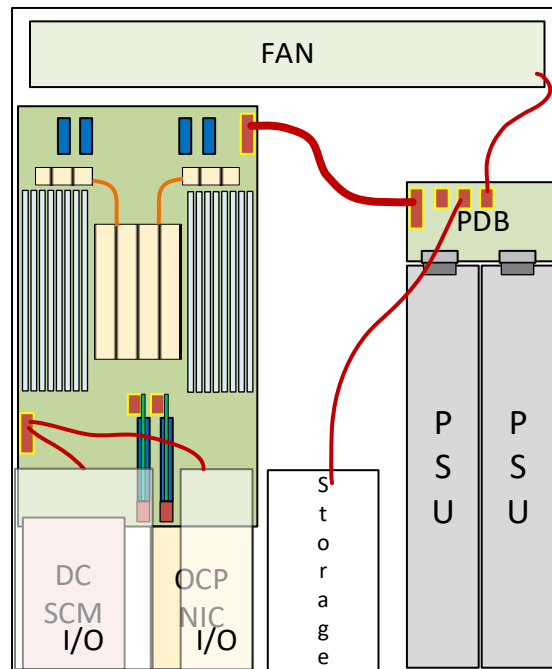
#### **Example 1: Monolithic Basic One Zone Ingress**



In the second example below, a monolithic (one HPM) system where PSUs feed power to the system PDB is shown. However, in this example, the optional Near Side power zone is leveraged:

- Far Side Ingress: Power from PDB to HPM
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: Supplemental power cable to CEM card aux (Note that the PICPWR definition requires a control an active cable to power gate these cables)
- Supplemental Power to I/O: From Near Zone (These cables could also be sourced from the PDB directly and would not require an active cable to power gate as control logic could be based on the PDB.)
- Note that because the HPM depicted supports both power Ingress / Egress zones the same HPM could be used in systems which leverage the far side for ingress power

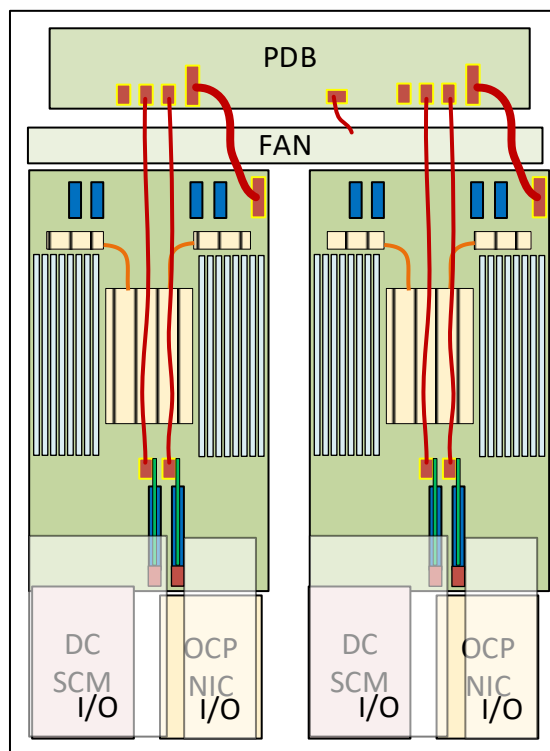
**Example 2: Monolithic Leveraging Both Zones**



The third example below illustrates a multi-node (>1 HPM) system with a Far Side PDB that could be supplied via PSUs, system level bus bars, or even rack level power distribution.

- Far Side Ingress: Power from PDB to HPM (while these connections are depicted with cables the HPM could also be adapted to support a board-to-board connector to chassis power infrastructure like a PDB as noted in **Section 11.1**)
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: None
- Supplemental Power to I/O: From the PDB directly (do not require a “puck” as control logic could be based on the PDB)

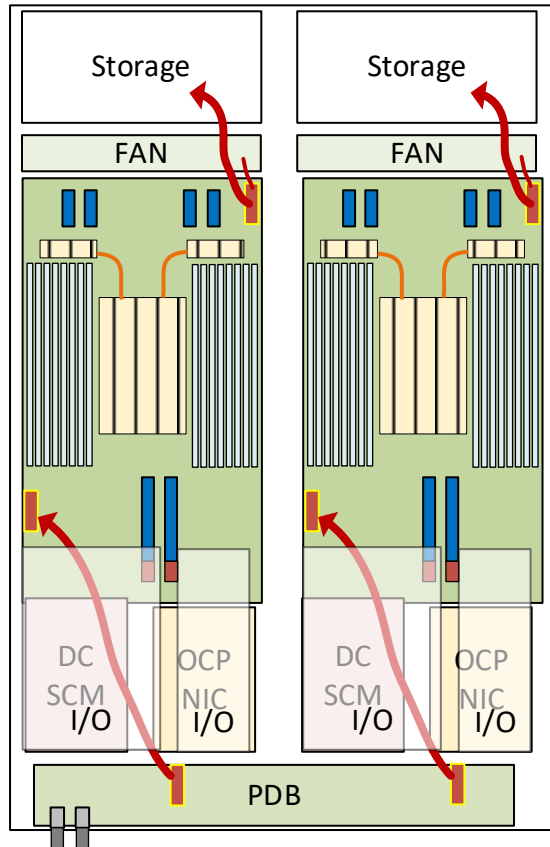
**Example 3: Multi-node with Far Side PDB**



The fourth example below demonstrates a multi-node (>1 HPM) system with a Near Side PDB that could be supplied via PSUs, system level bus bars or even rack level power distribution.

- Far Side Ingress: None
- Far Side Egress: Used to power Storage peripheral subsystem,
- Near Side Ingress: Power from PDB to HPM (cabled)
- Near Side Egress: None
- Supplemental Power to I/O: None
- Note that because the HPM depicted supports both power Ingress / Egress zones the same HPM could be used in systems which use to leverage the far side for ingress power

**Example 4 : Multi-node with Near Side PDB**



### 14.3. M-DNO CAD Files

M-DNO CAD files are available at the following link:

1120 <https://drive.google.com/drive/folders/1YcDWJLH6FwTnaC7UJDD8jyS25bIJHp2Z>

***CAD Snapshot***

