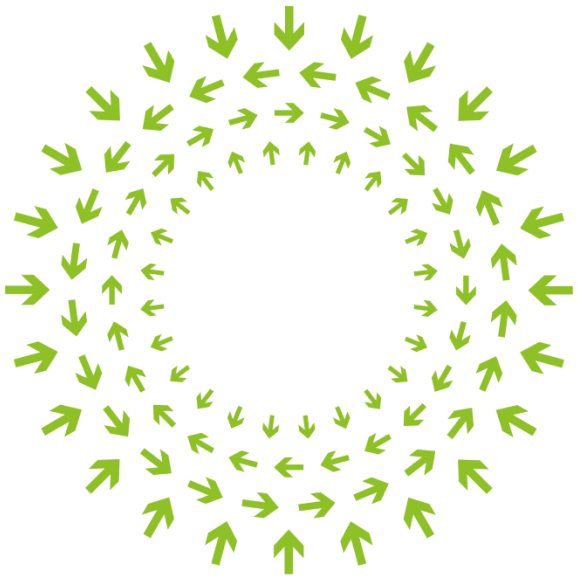

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Datacenter-ready eXtended Peripheral Interface (DC-XPI)

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Revision History

Version	Date	Notes
0.1	07JUN21	Initial draft.
0.2	17JUN21	Added mechanical spacing dimensions for expansion connector. Updated SMBus section. Miscellaneous formatting updates.
0.9	08SEP21	Several minor clarifications and formatting updates. Shared with OCP Server Project Team.

References

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- PCI-SIG®. PCI Express® Card Electromechanical Specification, Revision 4.0, September 2nd, 2019
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- DMTF Standard. DSP0222, Network Controller Sideband Interface (NC-SI) Specification. Distributed Management Task Force (DMTF), Rev 1.2.0b, August 4th, 2020.
- MIPI alliance Specification for I3C Basic^{SM} Version 1.0 – July 19th 2018
- OCP NIC 3.0 Design Specification Version 1.0.9
- SNIA. Protocol Agnostic Multi-Lane High Speed Connector, Rev 1.2, April 3, 2019
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Trademarks

Table of Contents

Objective

Datacenter-ready Modular I/O (**DC-MIO**) defines an architecture for the modularity of peripheral devices within a server. DC-MIO is a component of the Modular Building Block Architecture (**MBA**) along with **DC-SCM** (Datacenter-ready Secure Control Module) and **HPM** (Host Processor/Memory Module). Please refer to the OCP DC-SCM 1.0 Specification for broader context.

In such a modular design, high-density/high-speed I/O connectors are placed close to the CPU, and various peripheral component types can be connected to the HPM using cabled or riser-style I/O adapters. The advantages of this approach are:

- The server motherboard size can be reduced (reducing its cost)
- Peripherals with higher I/O speeds such as PCIe Gen5 can be more easily supported, as a portion of the interconnect can be carried over low loss cables. This may enable situations where use of a retimer is avoided.
- Various peripheral form factors can be supported using different adapters
- Higher power peripherals can be supported without additional power cables

This specification defines a particular interface for I/O modularity called the Datacenter-ready eXtended Peripheral Interface (DC-XPI) within the context of the DC-MIO architecture.

Other standard interfaces have been defined that can be used to connect peripherals in a modular fashion; however, DC-XPI provides all of the following, which was previously not available:

- Support for high (150W) and very high (400W) power peripherals without additional power cables
- Support for a rich set of sideband interfaces including USB2, USB3, and UART
- Support for presence signaling to isolate adapter from peripheral connectivity issues

Overview

The high-level objectives for the DC-XPI interconnect solution are to be able to support any of the following types of peripherals:

- Base Spec
    - 1x PCIe Gen5 x16 CEM-compliant card, up to 150W, e.g. a SmartNIC
        - Note: CEM Cards >75W require a short cable from I/O Adapter to AIC due to the 75W limit on the CEM slot.
    - 2x PCIe Gen5 x8 CEM-compliant cards, up to 75W/each
    - 4x PCIe Gen4 x4 U.2 or EDSFF solid state drives, up to 150W total
    - 1x OCP NIC 3.0 SFF/LFF
        - targeted for single-host configurations
        - NC-SI (if used) needs to be cabled to the HPM

        - capabilities may be expanded in future version of this specification
    - Any non-standard form factor peripheral up to x16 and 150W (e.g. custom accelerator)
- Base Spec + Optional Power Block
    - 1x PCIe Gen5 x16 CEM-compliant card, up to 400W
        - Note: CEM Cards >75W require a short cable from Adapter to AIC
    - 2x PCIe Gen5 x8 CEM-compliant cards, up to 200W/each
        - Note: CEM Cards >75W require a short cable from Adapter to AIC
    - 4x PCIe Gen4 x4 U.2 or EDSFF solid state drives, up to 400W total

This specification defines the following:

- **Interface Functions / Electricals** – defines what types of I/O modules can be supported; ensures support of required sideband signals and power capabilities
- **Connectors** – standardizes connector selection for HPM vendors; drives higher connector volumes; encourages alternative source suppliers; promotes wide usage base to find and solve any issues
- **Interface Pinout** – enables rapid adaptation of I/O modules to alternate platforms; that is, it reduces the problem to mechanical and thermal design

Note that this specification does NOT define the following:

- 48V power to the peripheral(s). 48V is not supported in the defined pinout.
- Mechanical and thermal design of I/O adapters. Given the wide range of server mechanical sizes and configurations, defining a single or small set of universal I/O adapter designs is deemed impractical.
- Specific requirements about where DC-XPI connectors must be physically located on an HPM.
- Link loss budgets for HPM and I/O adapter.
- Specific peripheral connectors that are compatible.
- Fanout logic required to support multiple peripherals on a single I/O adapter.

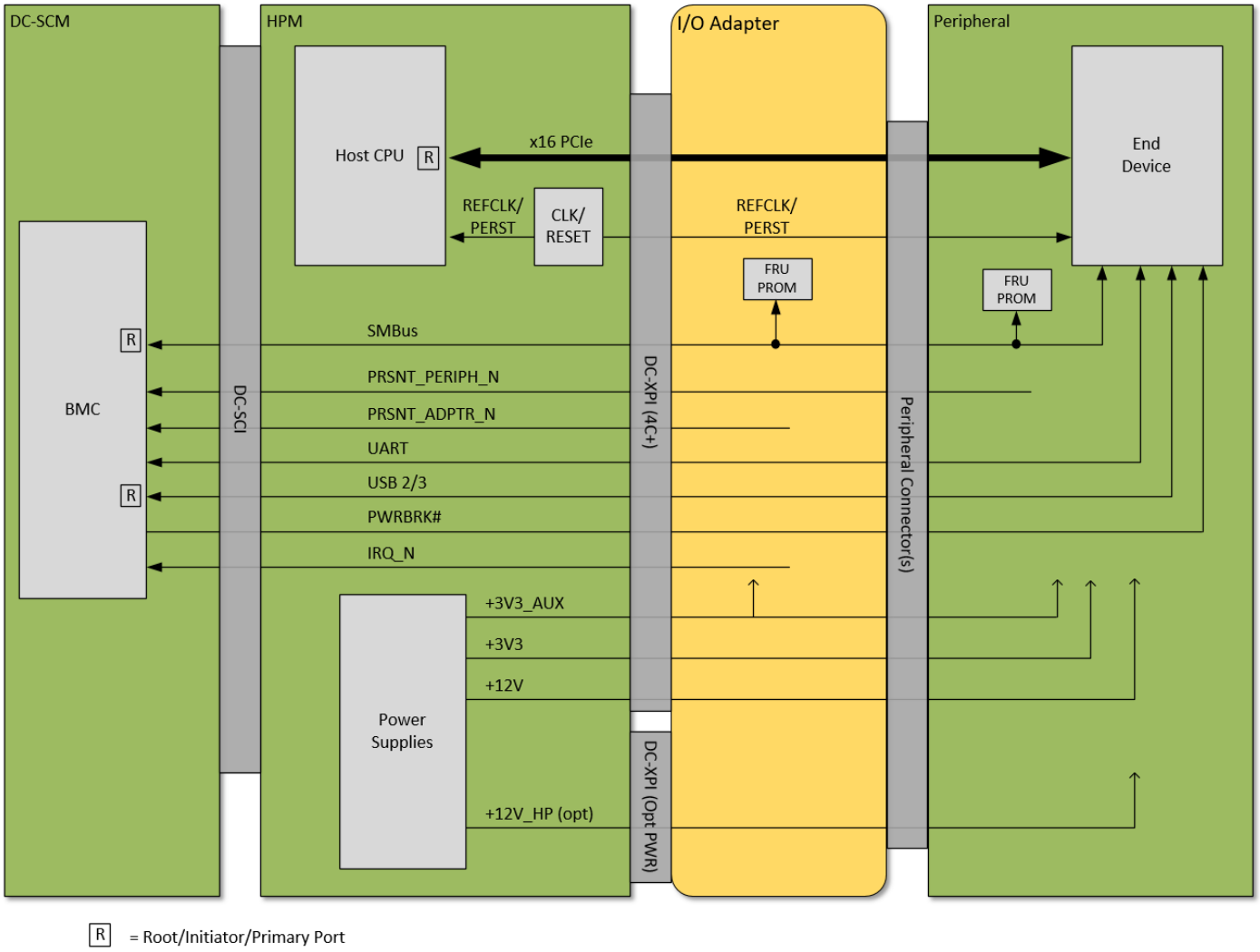
The above items may be areas to explore in future versions of this specification.

DC-XPI Architecture

For the purposes of this specification, the DC-XPI architecture is assumed to consist of the following primary elements:

- **HPM Interface** – SFF-TA-1002 4C+ connector mounted to the HPM/motherboard.
- **I/O Adapter** - Connects HPM Interface to the Peripheral; can be a riser or cable assy.
- **I/O Module** - An I/O Adapter plus any associated mechanicals to allow the I/O Adapter to be secured inside of a server and to mechanically secure the Peripheral(s).
- **Peripheral** - PCIe AIC, EDSFF drive, U.2 drive, SmartNIC, Custom accelerator, etc.

An example block diagram demonstrating the typical architectural building blocks of DC-XPI is shown in the following figure. The I/O adapter is shown in a different color to highlight that it may be a riser-PCB or cabled solution.



DC-XPI Example Block Diagram

Note: Signals PRSNT_PERIPH_N, PRSNT_ADPTR_N and IRQ_N are intentionally shown without detail above. Details of their connections are described later in this specification.

Mechanicals

This specification does not cover the details of I/O Module mechanicals, nor does it specify where a DC-XPI connector must be located on an HPM.

This specification uses a 4C+-sized cable receptacle and plug, which is not currently defined in SFF-TA-1020, but is targeted for addition in an upcoming revision.

There are two primary use cases envisioned for the DC-XPI connectors on an HPM:

Vertical

In this configuration, a vertical DC-XPI connector on the HPM is used with a riser card or cable-based adapter to connect to a peripheral.

In this configuration, the DC-XPI connector **should** be oriented such that the A70/B70 pins are closest to the CPU. This minimizes the length of the high-speed PCIe signals. Note that this is the opposite orientation as compared to a vertical DC-SCM connector.

Horizontal

In this configuration, a co-planar/edge DC-XPI connector on the HPM is used with a cable-based adapter to connect to a peripheral.

In this configuration, the DC-XPI connector **should** be oriented such that the A70/B70 pins are located on the left-hand side of the connector as viewed from outside the server from the side nearest the HPM edge with the connector.

Thermals

This specification does not cover the details of I/O Module thermals.

DC-XPI Card Edge Connector Definition

The DC-XPI card edge connector interface is compliant to the SFF-TA-1002 specification with respect to the 4C+ (168-pin) connector size. Note that while the interface is mechanically compatible with the 4C+ specification, it does not follow the SFF-TA-1007 pinout definition and is therefore not electrically compatible with EDSFF and OCP devices designed to the NIC3 specification. The DC-XPI pinout is defined later in this document.

Also note that the DC-XPI interface is specifically targeted to support PCIe x16 interface widths. Bifurcation or use of a subset of the x16 is supported. Smaller connector variants (x4, x8 PCIe) are not defined.

Gold Finger Plating Requirements

The minimum DC-XPI gold finger plating **must** be 30u" of gold over 50u" of nickel.

DC-XPI Pin Definition

The DC-XPI connector pinout is defined in the Table below.

The contact sequence for each pin is shown to indicate the order in which the pins make contact between the HPM and DC-XPI Card. The contact sequence **must** be followed for the PRSNT_ADPTR_N (pin B70) PRSNT_CMN (pin OA1) pins. Contact sequencing for other pins **may** be followed, but is not critical as the DC-XPI interface is not intended for hot-swapping. Gold finger dimensions on the I/O adapter for contact sequencing **should** follow the OCP NIC 3.0 specifications.

Table 1 : DC-XPI Pinout

Pin No.	Contact Sequence	Pin Name	Pin No.	Contact Sequence	Pin Name
B70	Second mate	PRSNT_ADPTR_N	**A70**	First mate	GND
B69	Second mate	UART_TX	**A69**	Second mate	USB2_DATp
B68	Second mate	UART_RX	**A68**	Second mate	USB2_DATn
B67	First mate	GND	**A67**	First mate	GND
B66	Second mate	PETp15	**A66**	Second mate	PERp15
B65	Second mate	PETn15	**A65**	Second mate	PERn15
B64	First mate	GND	**A64**	First mate	GND
B63	Second mate	PETp14	**A63**	Second mate	PERp14
B62	Second mate	PETn14	**A62**	Second mate	PERn14
B61	First mate	GND	**A61**	First mate	GND
B60	Second mate	PETp13	**A60**	Second mate	PERp13
B59	Second mate	PETn13	**A59**	Second mate	PERn13
B58	First mate	GND	**A58**	First mate	GND
B57	Second mate	PETp12	**A57**	Second mate	PERp12
B56	Second mate	PETn12	**A56**	Second mate	PERn12
B55	First mate	GND	**A55**	First mate	GND
B54	Second mate	PETp11	**A54**	Second mate	PERp11
B53	Second mate	PETn11	**A53**	Second mate	PERn11
B52	First mate	GND	**A52**	First mate	GND
B51	Second mate	PETp10	**A51**	Second mate	PERp10
B50	Second mate	PETn10	**A50**	Second mate	PERn10
B49	First mate	GND	**A49**	First mate	GND
B48	Second mate	PETp9	**A48**	Second mate	PERp9
B47	Second mate	PETn9	**A47**	Second mate	PERn9

B46	First mate	GND	**A46**	First mate	GND
B45	Second mate	PETp8	**A45**	Second mate	PERp8
B44	Second mate	PETn8	**A44**	Second mate	PERn8
B43	First mate	GND	**A43**	First mate	GND
KEY					
B42	Second mate	PRSNT_PERIPH_N	**A42**	Second mate	PWRBRK0_N
B41	First mate	GND	**A41**	First mate	GND
B40	Second mate	PETp7	**A40**	Second mate	PERp7
B39	Second mate	PETn7	**A39**	Second mate	PERn7
B38	First mate	GND	**A38**	First mate	GND
B37	Second mate	PETp6	**A37**	Second mate	PERp6
B36	Second mate	PETn6	**A36**	Second mate	PERn6
B35	First mate	GND	**A35**	First mate	GND
B34	Second mate	PETp5	**A34**	Second mate	PERp5
B33	Second mate	PETn5	**A33**	Second mate	PERn5
B32	First mate	GND	**A32**	First mate	GND
B31	Second mate	PETp4	**A31**	Second mate	PERp4
B30	Second mate	PETn4	**A30**	Second mate	PERn4
B29	First mate	GND	**A29**	First mate	GND
KEY					
B28	First mate	GND	**A28**	First mate	GND
B27	Second mate	PETp3	**A27**	Second mate	PERp3
B26	Second mate	PETn3	**A26**	Second mate	PERn3
B25	First mate	GND	**A25**	First mate	GND
B24	Second mate	PETp2	**A24**	Second mate	PERp2
B23	Second mate	PETn2	**A23**	Second mate	PERn2
B22	First mate	GND	**A22**	First mate	GND
B21	Second mate	PETp1	**A21**	Second mate	PERp1
B20	Second mate	PETn1	**A20**	Second mate	PERn1
B19	First mate	GND	**A19**	First mate	GND
B18	Second mate	PETp0	**A18**	Second mate	PERp0
B17	Second mate	PETn0	**A17**	Second mate	PERn0
B16	First mate	GND	**A16**	First mate	GND
B15	Second mate	REFCLKp	**A15**	Second mate	USB3.0_RXn
B14	Second mate	REFCLKn	**A14**	Second mate	USB3.0_RXp
B13	First mate	GND	**A13**	First mate	GND
B12	Second mate	RFU	**A12**	Second mate	USB3.0_TXn
B11	Second mate	RFU	**A11**	Second mate	USB3.0_TXp
B10	First mate	GND	**A10**	First mate	GND
B9	Second mate	+3.3V_AUX_EDGE	**A9**	Second mate	RST_ADPTR_N
B8	Second mate	PERST_N	**A8**	Second mate	SMDAT
B7	Second mate	IRQ_N	**A7**	Second mate	SMCLK

B6	Second mate	WAKE_N	**A6**	First mate	GND
B5	First mate	GND	**A5**	Second mate	RFU
B4	Second mate	+12V_EDGE	**A4**	Second mate	RFU
B3	Second mate	+12V_EDGE	**A3**	First mate	GND
B2	Second mate	+12V_EDGE	**A2**	First mate	GND
B1	Second mate	+12V_EDGE	**A1**	First mate	GND
KEY					
OB14	Second mate	+12V_EDGE	**OA14**	First mate	GND
OB13	Second mate	+12V_EDGE	**OA13**	First mate	GND
OB12	Second mate	+12V_EDGE	**OA12**	First mate	GND
OB11	Second mate	+12V_EDGE	**OA11**	First mate	GND
OB10	Second mate	+12V_EDGE	**OA10**	First mate	GND
OB9	Second mate	+12V_EDGE	**OA9**	First mate	GND
OB8	Second mate	+12V_EDGE	**OA8**	First mate	GND
OB7	Second mate	+12V_EDGE	**OA7**	First mate	GND
OB6	Second mate	+3V3_EDGE	**OA6**	First mate	GND
OB5	Second mate	+3V3_EDGE	**OA5**	First mate	GND
OB4	Second mate	+3V3_EDGE	**OA4**	First mate	GND
OB3	Second mate	+3V3_EDGE	**OA3**	First mate	GND
OB2	Second mate	+3V3_EDGE	**OA2**	First mate	GND
OB1	Second mate	+3V3_EDGE	**OA1**	Second mate	PRSNT_CMN

DC-XPI Base Pin Definition

DC-XPI Signal Descriptions

Power

The following table provides the required specifications for the power supply rails available at the DC-XPI interface. All three rails are required to be provided.

The currents described below can meet connector vendor requirements for <= 30°C temperature rise for the DC-XPI pinout and have been derated 20% per IEC 60512-5-2. The system designer must ensure an appropriate PCB layout to manage temperature excursions of the connector pins and PCB.

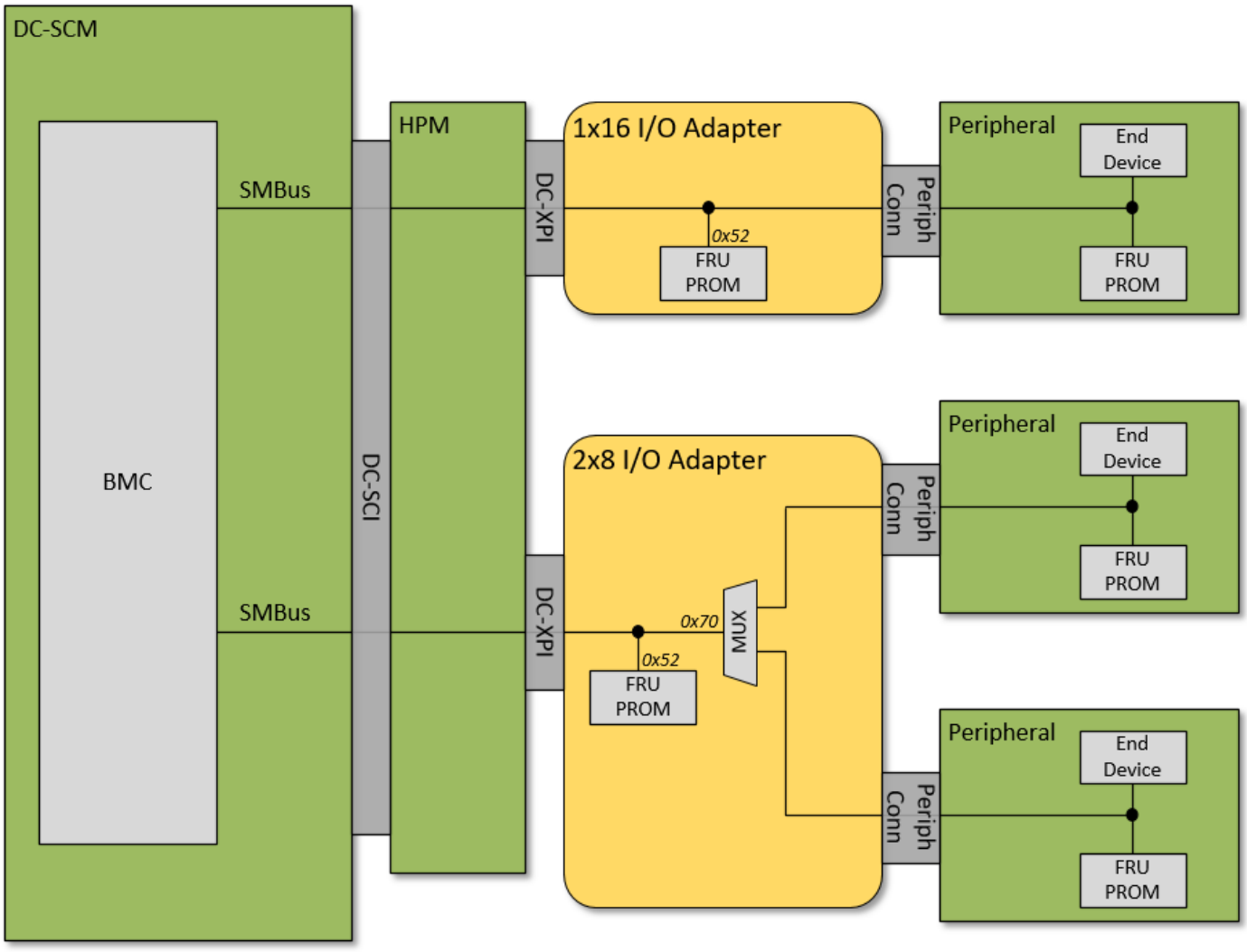
Power Rail	Nominal Voltage (V)	Tolerance	Minimum Voltage (V)	Current (A)	Min Power (W)
+3V3_EDGE	3.3	+/-5%	3.135	6.0	18.81
+3.3V_AUX_EDGE	3.3	+/-5%	3.135	1.0	3.14
+12V_EDGE	12.0	+/-5%	11.400	12.0	136.80
				TOTAL	**158.75**

Base Power Supply Specifications

Note: currents in this table equate to 1A per conductor.

Note: the DC-XPI tolerances have been set to account for additional drops on the I/O Adapter.

SMBus (SMDAT, SMCLK)



SMBus Example Block Diagram

The HPM **must** provide pullup resistors to the 3.3V STBY rail (consistent with the DC-SCM 1.0 specification). Components on the I/O Adapter that are attached to the bus and powered by non-STBY rails, must be appropriately electrically isolated.

The following guidance is provided for system implementations, but are not strictly required by this specification. All SMBus addresses are expressed in 7-bit (8-bit) notation:

- The I/O Adapter **may** have a FRU EEPROM and if present, **should** be located at address 0x52 (0xA4). The FRU EEPROM can be used to store vital product data such as inventory, bifurcation, topology, peripheral count, and other information.
- The FRU EEPROM **should** follow the Intel Platform Management FRU Information Storage Definition, rev 1.3.
- The I/O Adapter **should** provide a muxless path from BMC to the peripheral, so as to support multi-master transactions.
- Where SMBus muxing is required, e.g. for a multi-peripheral adapter, the mux **should** be located at address 0x70 (0xE0). Address 0x76 (0xEC) is also acceptable.

USB (USB2_DAT[pn], USB3_RX[pn], USB3_TX[pn])

DC-XPI provides USB2 and USB3 interfaces to the peripheral. This is generally intended for use as a high-speed OOB management link. The USB Host side is on the HPM/DC-SCM.

This is intended to be a single logical interface, where either USB2 or USB3 is used. That is, only a single USB host controller is expected to be provided by the DC-SCM (via the HBM) per DC-XPI interface.

Transmit and Receive directions here are defined with respect to the HPM.

Interrupt (IRQ_N)

An interrupt signal is provided with the intention of allowing the I/O adapter to interrupt the system BMC. An example usage would be: alerting the BMC of insertion of a new flash drive peripheral device. This signal could be used to carry an SMBus ALERT signal, but is not restricted to that usage.

PCIe (PE[TR][pn]0-15, REFCLK[pn], PERST_N)

DC-XPI supports up to a x16 PCIe interface using a common clock architecture.

DC-XPI does not support multi-host systems where the x16 link is divided amongst multiple root ports. This application would require (at least) multiple PERST_N signals from the hosts.

The I/O Adapter does not implement AC-coupling capacitors.

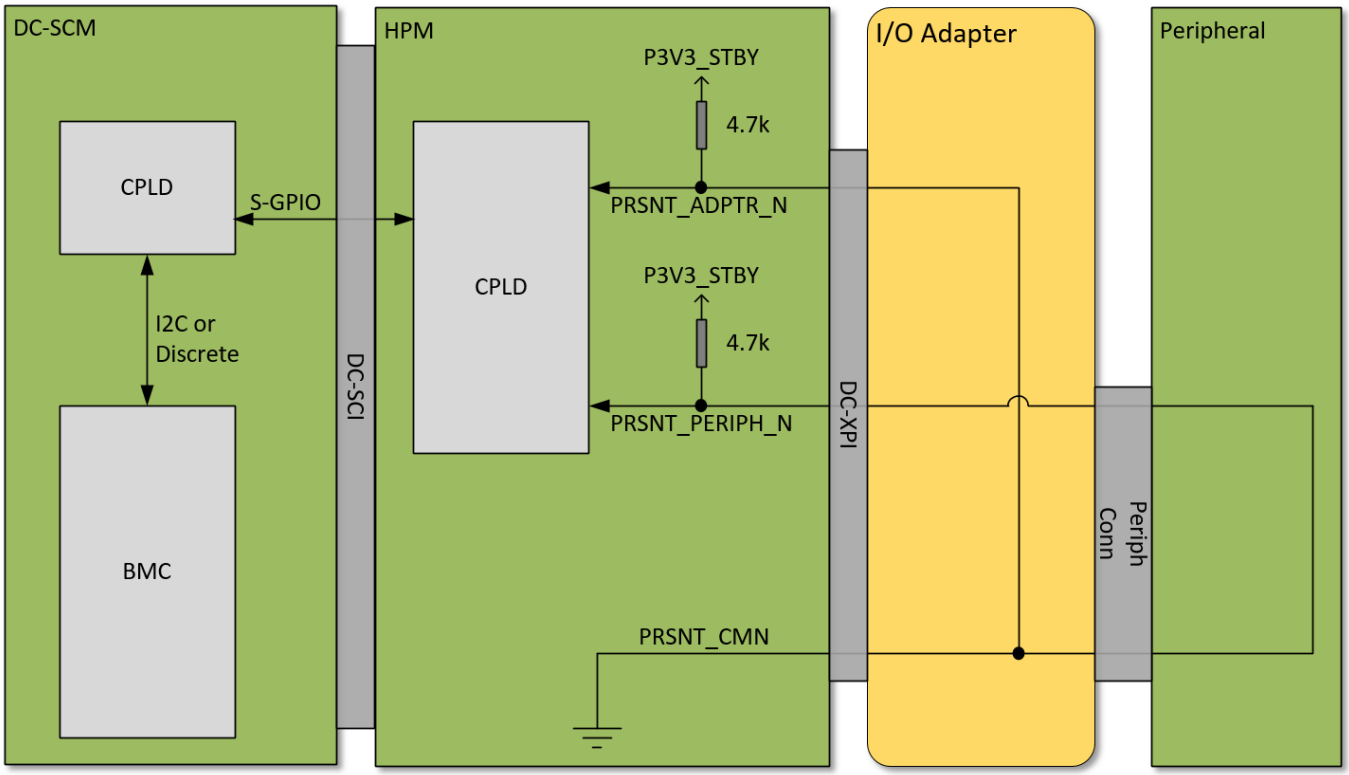
Transmit and Receive directions here are defined with respect to the HPM.

Presence Detection (PRSNT_ADPTR_N, PRSNT_PERIPH_N, PRSNT_CMN)

Three presence detection pins are defined on the DC-XPI interface. These pins are used to indicate presence of the I/O adapter (PRSNT_ADPTR_N) and the peripheral(s) (PRSNT_PERIPH_N).

The PRSNT_ADPTR_N and PRSNT_CMN pins are located on the extremities of the DC-XPI connector to ensure indication of full connector seating.

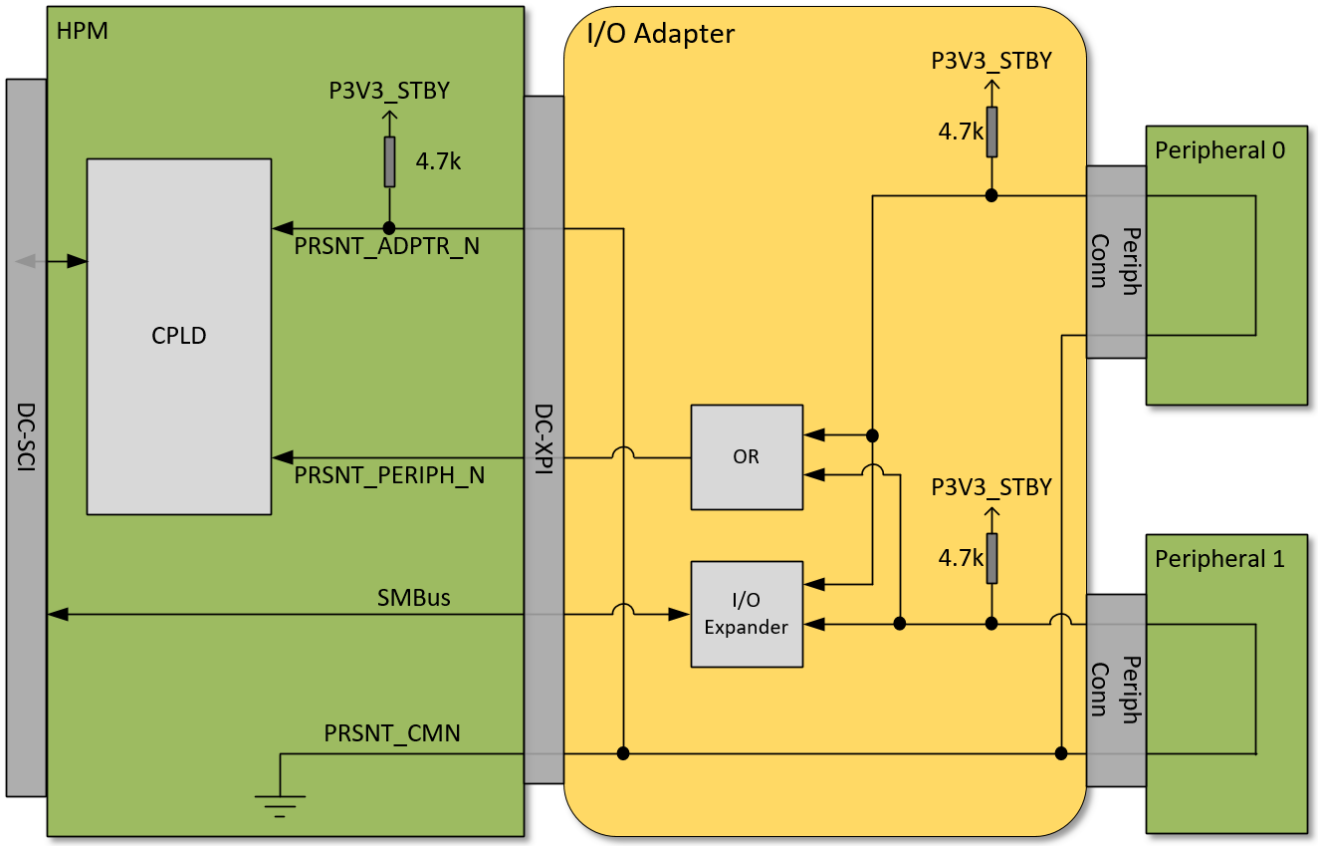
The following diagram is an example of presence detection with a single peripheral card attached to an I/O Adapter.



Single-Peripheral Presence Example Diagram

The following diagram is an example of presence detection with multiple plug-in peripherals attached to a single I/O Adapter. The DC-SCM is not shown for clarity. Note that the PRSNT_PERIPHIN_N signal is defined here as “all peripherals are present”. Upon detecting a de-asserted PRSNT_PERIPHIN_N signal, the BMC can query the I/O Adapter via SMBus to determine which peripheral(s) are not present.

In this scenario, the I/O Adapter FRU contains a “Peripheral Count” field, which the BMC reads as part of the inventory phase to determine how many peripherals the I/O Adapter supports (and whether it needs to read an I/O expander to determine status for multiple cards).



Multi-Peripheral Presence Example Diagram

Adapter Reset (RST_ADPTR_N)

This signal may be used to reset any stateful logic on the I/O adapter itself (e.g. an SMBus mux, an I/O expander, etc.). This signal must not reset any peripheral(s) attached to the I/O adapter.

UART (UART_TX, UART_RX)

The UART interface may be used for serial logs, serial console and debugging. The Transmit and Receive directions here are defined with respect to the HPM. Hardware flow control signals are not provided. Signaling level is 3.3 V, baud rates up to 115200 are supported.

WAKE (WAKE_N)

This signal may be used by a peripheral to wake the host on the HPM, e.g. Wake on LAN. The HPM must provide the appropriate pull-up resistor(s) for this signal.

WAKE_N signals from multiple DC-XPI connectors **may** be connected together to implement a wired-OR function.

Reserved for Future Use (RFU)

There are four pins on the DC-XPI interface that are reserved for future use. These pins **must** be left unconnected on both HPM and add-in card.

Bifurcation / Multiple Endpoints

If more than one PCIe endpoint is attached to an I/O Adapter, the I/O Adapter **must** provide the fanout for the following signals:

PRSNT_PERIPH_N

PERST (note that the peripherals are thus constrained to a single PERST reset domain)

PCIe clock (unless a separate reference clock scheme is being used)

SMBus (if used)

UART (if used)

USB (if used)

PWRBRK_N (if used)

Electrical Specification

The DC-XPI is not specified to support hot insertion or removal of I/O Adapters. In-rush current control **should** be provided on the HPM to protect the circuitry from damage due to I/O Adapter damaged connector pins, accidental removal, or installation in a powered system, etc.

The HPM **should** isolate multiple DC-XPI interfaces from each other so that a fault on one interface doesn't affect the operation of other interfaces. Examples may include power fusing (see below), I2C, clocks, resets, etc.

Fusing

The DC-XPI connector **should** be appropriately fused on the HPM to prevent damage to the HPM traces and connector in the case of a fault on either the I/O adapter or peripheral. This fusing also enhances fault isolation and repairability.

Additional fusing **may** be required on the I/O adapter for lower-power peripherals.

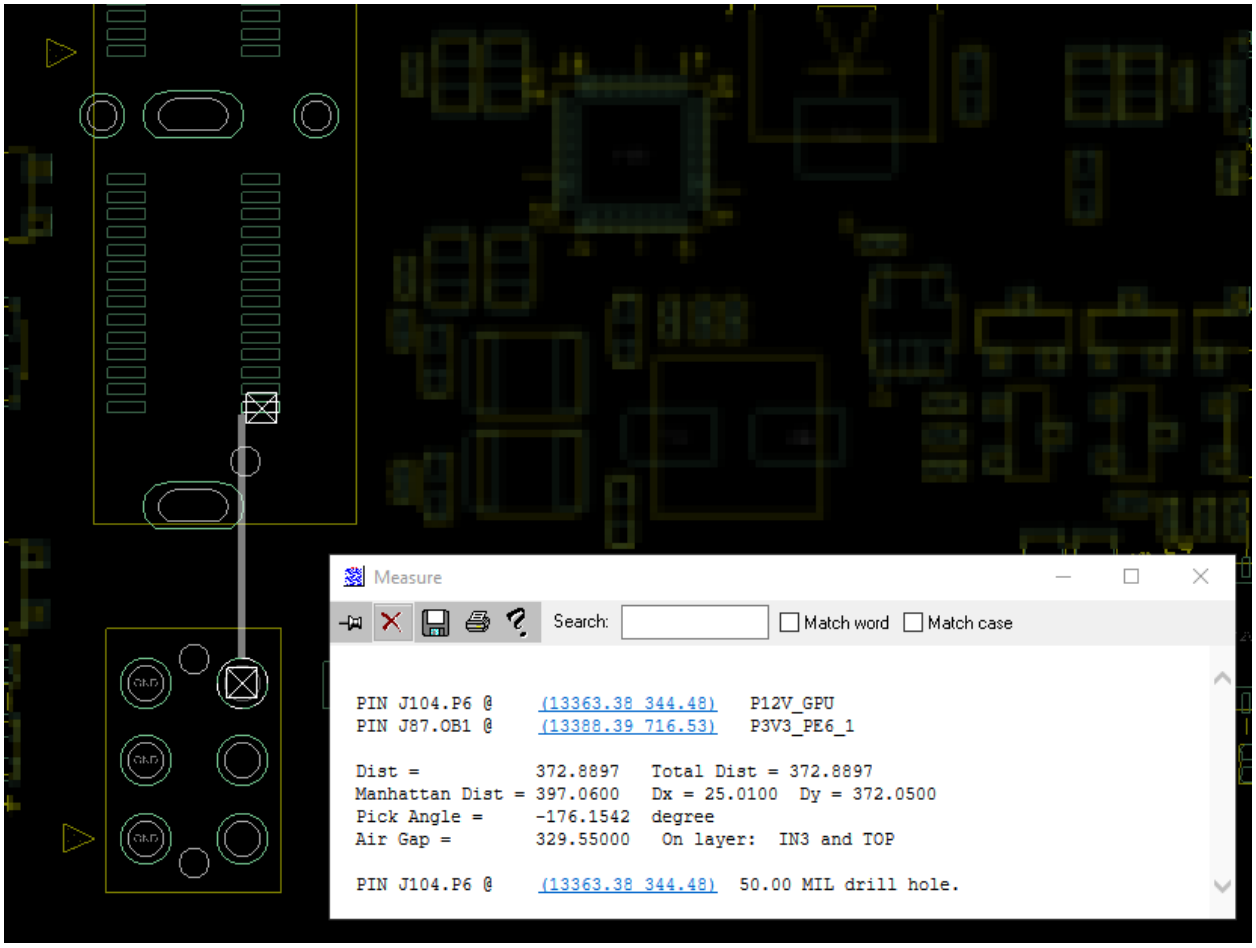
Appendix A – Optional High Power Expansion

If the peripheral(s) attached to a DC-XPI connector require more than 150W, a high-power expansion connector **may** be added to supplement the DC-XPI connector to provide up to 400W total.

A high power DC-XPI peripheral can draw up to 150W from the base DC-XPI connector and up to 250W additional power from the high power expansion connector.

Mechanical

The 4C+ and expansion connector **should** be mechanically located with respect to each other per the drawing below. This spacing allows for both riser-style and cabled I/O adapters to be used. In both riser and cabled applications, the I/O adapter can use either the 4C+ only or the 4C+ plus the power expansion connector.



Connector Definition

The high-power expansion connector leverages the contacts and footprint called out in the SFF-TA-1020 4C-HP connector, however in this specification the extra power only supports 12V and is implemented in a physically separate connector.

The contact sequence for each pin is shown to indicate the order in which the pins make contact between the HPM and DC-XPI Card. Contact sequencing for these pins **may** be followed, but is not critical as the DC-XPI interface is not intended for hot-swapping. Gold finger dimensions on the I/O adapter for contact sequencing **should** follow the OCP NIC 3.0 specifications.

Pin Definition

Pin No.	Contact Sequence	Pin Name	Pin No.	Contact Sequence	Pin Name
PB3	Second mate	+12V_EDGE_HP	**PA3**	First mate	GND
PB2	Second mate	+12V_EDGE_HP	**PA2**	First Mate	GND
PB1	Second mate	+12V_EDGE_HP	**PA1**	First Mate	GND

DC-XPI High Power Extension Pin Definition

Signal Descriptions

A system that supports a high-power expansion connector **must** deliver +12V_EDGE to the base connector and the additional +12V_EDGE_HP via the high power expansion connector from the same or different power supply rails.

Power

The following table provides the required specifications for the power supply rails available at the DC-XPI interface with high-power expansion. The three rails from the base specification are included for completeness.

The currents described below can meet connector vendor requirements for <= 30°C temperature rise for the DC-XPI pinout and have been derated 20% per IEC 60512-5-2. These currents are compatible with 30AWG cabled connections in the I/O Adapter (for both flat and bundled cable styles).

Power Rail	Nominal Voltage (V)	Tolerance	Minimum Voltage (V)	Current (A)	Min Power (W)
+3V3_EDGE	3.3	+/-5%	3.135	6.0	18.81
+3.3V_AUX_EDGE	3.3	+/-5%	3.135	1.0	3.14
+12V_EDGE	12.0	+/-5%	11.400	12.0	136.80
+12V_EDGE_HP	***12.0***	***+/-5%***	***11.400***	***25.0***	***285.00***
				TOTAL	**443.75**

Extended Power Supply Specifications

Fusing

A high-power expansion connector **should** have its own fuse on the HPM to prevent damage to the connector and traces.

Additional fusing **may** be required on the I/O adapter depending on the application.

Peripheral Power

I/O Adapters and plug-in peripherals must adhere to the following requirements:

+12V_EDGE and +12V_EDGE_HP **must** be treated as coming from independent system power supply rails.

+12V_EDGE and +12V_EDGE_HP **must** not be electrically shorted at any point on an I/O Adapter nor on a peripheral.

No specific power sequencing between the various rails can be assumed.

Note that this specification requires that the AIC & plugin treat the two rails as separate, similar to the way PCIe CEM treats auxiliary power inputs for cards >75W. This approach alleviates current sharing and fusing complexities at the expense of having to implement two VR circuits on a high-power I/O Adapter and/or peripheral device.

Appendix B - Acronyms

For the purposes of the DC-XPI specification, the following acronyms apply:

Acronym	Definition
AIC	Add-in Card
BMC	Baseboard Management Controller
CEM	PCI-Sig Card Electromechanical specification
DC-MIO	DatacenterReady - Modular I/O
DC-SCM	DatacenterReady - Secure Control Module
DC-SCI	DatacenterReady - Secure Control Interface
DC-XPI	Data CenterReady - eXtended Peripheral Interface
EDSFF	Enterprise and Datacenter SSD Form Factor
FRU	Field Replaceable Unit
HPM	Host Processor/Memory Module. This refers to any processing module to be managed by a DC-SCM. In the simplest terms, this is like today's motherboard with BMC and Security circuitry removed. However, this is not limited to standard processor architecture and can apply to any architecture utilizing management and security features.
I^2C	Inter-Integrated Circuit - two wire serial protocol
I3C	MIPI Alliance Improved Inter-Integrated Circuit – two wire serial protocol
I/O	Input / Output
LFF	Large Form Factor
NC-SI	Network Controller Sideband Interface
NIC	Network Interface Card
OCP	Open Compute Project
SFF	Small Form Factor

Appendix C – Comparison of Features

The following table is an overview comparison of the features supported by several of the existing PCIe peripheral interfaces. This table is for reference only and is included for documentation of the need for DC-XPI.

	PCIe AIC x16	EDSFF-4C PECFF-4C	PECFF-4C-HP-12V	OCP NIC 3.0-4C+ PECFF-4C+	DC-XPI r1.0	DC-XPI r1.0 + Pwr Block
Spec(s)	PCI-SIG CEM 4.0	SFF-TA-1002 SFF-TA-1009 SFF-TA-1021	SFF-TA-1021 SFF-TA-1020	OCP NIC 3.0	This Doc	This Doc
# of Pins	164p	140p	140p + Pwr	168p	168p	168p + Pwr Block
Connector(s) Total Length	3.50"	2.25"	3.14"	2.73"	2.73"	~ 3.23"
Card/Riser Supported	✓	✓	✓	✓	✓	✓
Cable Supported	---	✓	(cable for 4C?)	✓	✓	✓ (two cables)
Nominal Power Level Supported	see spec for details	70W	660W	80W	150W	400W
12V Current		6.6A	55A + 6.6A	6.6A	12A (TBC)	25A + 12A (TBC)
3V3 Current		---	---	(1.1A)	6A (TBC)	6A (TBC)
3V3_AUX Current		25mA	25mA	(1.1A)	1A (TBC)	1A (TBC)
PRSNT	see spec for details	✓	✓	4pins	✓	✓
Dual-level PRSNT		---	---	---	✓	✓
# REFCLKs		2	2	4	1	1
# PERSTs		2	2	4	1	1
SMBus		✓	✓	✓	✓	✓
WAKE		---	---	✓	✓	✓
JTAG		---	---	---	---	---
PWRBRK		---	---	✓	✓	✓
CLKREQ		✓	✓	---	---	---

USB2		---	---	✓		✓	✓
USB3		---	---	---		✓	✓
UART		---	---	---		✓	✓
Interrupt		---	---	---		✓	✓
I3C		---	---	---		---	---
Bifurcation		---	---	3pins		---	---
NCSI (RMII)		---	---	✓		---	---
DUALPORTEN		✓	✓	---		---	---
SGPIO		---	---	4pins		---	---
PWREN/GD		1pin	1pin	2pins		---	---
SLOTID		---	---	2pins		---	---
LED/ACTIVITY		1pin	1pin	---		---	---
MFG		1pin	1pin	---		---	---
		---	---	---		---	---
# RFU/RSVD		7	7	2		4	4

Comparison of Features

Table Legend:

	meets DC-XPI goals
	does not meet DC-XPI goals
---	not supported

Appendix D – Comparison of Pinouts

The following table is a comparison of the DC-XPI pinout vs. the OCP NIC pinout. It is included for reference only.

	168 Pin DC-XPI				168 Pin OCP NIC			
	CPU Side of the Connector							
Pin	Signal	Signal	Pin		Pin	Signal	Signal	Pin
B70	PRSNT_ADPTR_N	GND	A70		B70	PRSNTB3#	PWRBRK0#	A70
B69	UART_TX	USB2_DATp	A69		B69	RFU	USB_DATp	A69
B68	UART_RX	USB2_DATn	A68		B68	RFU	USB_DATn	A68
B67	GND	GND	A67		B67	GND	GND	A67
B66	PETp15	PERp15	A66		B66	PETp15	PERp15	A66
B65	PETn15	PERn15	A65		B65	PETn15	PERn15	A65
B64	GND	GND	A64		B64	GND	GND	A64
B63	PETp14	PERp14	A63		B63	PETp14	PERp14	A63
B62	PETn14	PERn14	A62		B62	PETn14	PERn14	A62
B61	GND	GND	A61		B61	GND	GND	A61
B60	PETp13	PERp13	A60		B60	PETp13	PERp13	A60
B59	PETn13	PERn13	A59		B59	PETn13	PERn13	A59
B58	GND	GND	A58		B58	GND	GND	A58
B57	PETp12	PERp12	A57		B57	PETp12	PERp12	A57
B56	PETn12	PERn12	A56		B56	PETn12	PERn12	A56
B55	GND	GND	A55		B55	GND	GND	A55
B54	PETp11	PERp11	A54		B54	PETp11	PERp11	A54
B53	PETn11	PERn11	A53		B53	PETn11	PERn11	A53
B52	GND	GND	A52		B52	GND	GND	A52

B51	PETp10	PERp10	A51	B51	PETp10	PERp10	A51
B50	PETn10	PERn10	A50	B50	PETn10	PERn10	A50
B49	GND	GND	A49	B49	GND	GND	A49
B48	PETp9	PERp9	A48	B48	PETp9	PERp9	A48
B47	PETn9	PERn9	A47	B47	PETn9	PERn9	A47
B46	GND	GND	A46	B46	GND	GND	A46
B45	PETp8	PERp8	A45	B45	PETp8	PERp8	A45
B44	PETn8	PERn8	A44	B44	PETn8	PERn8	A44
B43	GND	GND	A43	B43	GND	GND	A43
Key				Key			
B42	PRSNT_PERIPH_N	PWRBRK0_N	A42	B42	PRSNTB0#	PRSNTB1#	A42
B41	GND	GND	A41	B41	GND	GND	A41
B40	PETp7	PERp7	A40	B40	PETp7	PERp7	A40
B39	PETn7	PERn7	A39	B39	PETn7	PERn7	A39
B38	GND	GND	A38	B38	GND	GND	A38
B37	PETp6	PERp6	A37	B37	PETp6	PERp6	A37
B36	PETn6	PERn6	A36	B36	PETn6	PERn6	A36
B35	GND	GND	A35	B35	GND	GND	A35
B34	PETp5	PERp5	A34	B34	PETp5	PERp5	A34
B33	PETn5	PERn5	A33	B33	PETn5	PERn5	A33
B32	GND	GND	A32	B32	GND	GND	A32
B31	PETp4	PERp4	A31	B31	PETp4	PERp4	A31
B30	PETn4	PERn4	A30	B30	PETn4	PERn4	A30
B29	GND	GND	A29	B29	GND	GND	A29
Key				Key			
B28	GND	GND	A28	B28	GND	GND	A28
B27	PETp3	PERp3	A27	B27	PETp3	PERp3	A27

B26	PETn3	PERn3	A26	B26	PETn3	PERn3	A26
B25	GND	GND	A25	B25	GND	GND	A25
B24	PETp2	PERp2	A24	B24	PETp2	PERp2	A24
B23	PETn2	PERn2	A23	B23	PETn2	PERn2	A23
B22	GND	GND	A22	B22	GND	GND	A22
B21	PETp1	PERp1	A21	B21	PETp1	PERp1	A21
B20	PETn1	PERn1	A20	B20	PETn1	PERn1	A20
B19	GND	GND	A19	B19	GND	GND	A19
B18	PETp0	PERp0	A18	B18	PETp0	PERp0	A18
B17	PETn0	PERn0	A17	B17	PETn0	PERn0	A17
B16	GND	GND	A16	B16	GND	GND	A16
B15	REFCLKp	USB3.0_RXn	A15	B15	REFCLKp0	REFCLKp1	A15
B14	REFCLKn	USB3.0_RXp	A14	B14	REFCLKn0	REFCLKn1	A14
B13	GND	GND	A13	B13	GND	GND	A13
B12	RFU	USB3.0_TXn	A12	B12	AUX_PWR_EN	PRSNTB2#	A12
B11	RFU	USB3.0_TXp	A11	B11	+3.3V_EDGE	PERST1#	A11
B10	GND	GND	A10	B10	PERST0#	PRSNTA#	A10
B9	+3.3V_AUX_EDGE	RST_ADPTR_N	A9	B9	BIF2#	RST_ADPTR_N	A9
B8	PERST_N	SMDAT	A8	B8	BIF1#	SMDAT	A8
B7	IRQ_N	SMCLK	A7	B7	BIF0#	SMCLK	A7
B6	WAKE_N	GND	A6	B6	+12V_EDGE	GND	A6
B5	GND	RFU	A5	B5	+12V_EDGE	GND	A5
B4	+12V_EDGE	RFU	A4	B4	+12V_EDGE	GND	A4
B3	+12V_EDGE	GND	A3	B3	+12V_EDGE	GND	A3
B2	+12V_EDGE	GND	A2	B2	+12V_EDGE	GND	A2
B1	+12V_EDGE	GND	A1	B1	+12V_EDGE	GND	A1
Key				Key			

OB14	+12V_EDGE	GND	OA14		OB14	RBT_CRS_DV	RBT_CLK_IN	OA14
OB13	+12V_EDGE	GND	OA13		OB13	GND	GND	OA13
OB12	+12V_EDGE	GND	OA12		OB12	REFCLKp2	REFCLKp3	OA12
OB11	+12V_EDGE	GND	OA11		OB11	REFCLKn2	REFCLKn3	OA11
OB10	+12V_EDGE	GND	OA10		OB10	GND	GND	OA10
OB9	+12V_EDGE	GND	OA9		OB9	RBT_RXD0	RBT_TXD0	OA9
OB8	+12V_EDGE	GND	OA8		OB8	RBT_RXD1	RBT_TXD1	OA8
OB7	+12V_EDGE	GND	OA7		OB7	SLOT_ID0	RBT_TX_EN	OA7
OB6	+3V3_EDGE	GND	OA6		OB6	CLK	SLOT_ID1	OA6
OB5	+3V3_EDGE	GND	OA5		OB5	DATA_OUT	RBT_ARB_OUT	OA5
OB4	+3V3_EDGE	GND	OA4		OB4	DATA_IN	RBT_ARB_IN	OA4
OB3	+3V3_EDGE	GND	OA3		OB3	LD#	WAKE_N	OA3
OB2	+3V3_EDGE	GND	OA2		OB2	MAIN_PWR_EN	PERST3#	OA2
OB1	+3V3_EDGE	PRSNT_CMN_N	OA1		OB1	NIC_PWR_GOOD	PERST2#	OA1
Optional PWR BLOCK:								
PB3	+12V_EDGE_HP	GND	PA3					
PB2	+12V_EDGE_HP	GND	PA2					
PB1	+12V_EDGE_HP	GND	PA1					

Comparison of Pinouts

Appendix E – Peripheral Voltage Tolerances

The following table is a comparison of the voltage tolerances required by some potential peripheral standards. This table is included for reference only and was used to guide the DC-XPI interface tolerances.

Rail	PCIe AIC CEM rev4.0	U.2 Enterprise SSD FF 1.0a	EDSFF SFF-TA-1109 rev2.0
3.3V	+/-9%	n/a	n/a
3.3V_STBY	+/-9%	+/-15% (+10/-9% per some drive specs)	+5/-10%
12V	+/-8%	unspecified (+/-8% per some drive specs)	+10/-9%
12V_AUX	+5/-8%	n/a	n/a