

AT&T Open XGS-PON

NFV 4-Port Remote OLT Specification

Revision 1.1

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# Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| Revision | Date | Author | Description |
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# Scope

This document defines the technical specifications for the AT&T Open XGS-PON 4-port Remote OLT submitted to the Open Compute Project.

# Overview

This document describes the technical specifications of the Open XGS-PON 4-port Remote OLT designed by AT&T. The system is a physically Hardened outdoor unit that is self‐contained, and not part of a physical chassis system. However, this physical box is attached to a fabric (e.g. leaf and spine) that interconnects it to create large scale‐out virtual network elements[[1]](#footnote-1).

The Open XGS-PON 4-port Remote OLT is a cost optimized access design focused on NFV Infrastructure deployments which support 10Gb/10Gb PON access connectivity and provide **40Gb** uplinks to the ToR (Top of Rack) or Spine layer of the network.

The switch supports 4 x XFP XGS-PON links that each operate at 10Gb downstream (egress) and 10Gb upstream (ingress), 1x QSFP28 ports that operate as up to four 10Gb ports each. These 4 physical ports are designed to support 1‐1 active‐standby arrangement, where each lane in a primary port has a corresponding backup in a failover port. Other applications are also envisioned and described below.

The Open XGS-PON 4-port Remote vOLT is a PHY‐Less design with the XFP connections directly attaching to the XFI and SERDES interfaces of the Broadcom BCM68620 xPON SoC for OLT.

Applications of this design include some specific variations and considerations in order to address a broader market and set of collaborators for this project. Specifically, the set of variations considered include:

1. The simplified and cost‐optimized virtualized scale‐out OLT.
2. A small, simplified, self‐contained traditional OLT device that can be used in non‐NFVI environments.
3. The ability to synchronize and distribute timing from upstream toward ONUs.

The three variations are not mutually exclusive, and are now described in more detail.

# Virtual OLT

The first application embodies the virtual OLT. In this application the device is envisioned to be part of a NFVI deployment, where compute, storage, and other cloud infrastructure are part of the environment. In this environment, the Open XGS-PON 4-port Remote OLT connects to leaf or spine devices that aggregate traffic and also provide transport for management and control.

The low‐level management processes that might be typically performed by an embedded processor on a XGS-PON 4-port Remote OLT are performed outside the box, in a separate commodity server. This allows managing many OLT devices from a small number of commodity servers, and conserves compute and storage in the same way that performing aggregation in the ToR switch conserves aggregation typically performed on line cards to interface several XGS-PON PHY chips to a backplane or fabric. The arrangement also allows for an overall system design where there is no single point of failure that affects the entire Open XGS-PON 4-port Remote OLT and allows application of cloud application architecture to software that was previously hosted on embedded processors.

This system is described as a disaggregated or virtual OLT because the various software and hardware components that were once integrated into a single physical device have been separated and supported in a distributed way across NFV infrastructure. By doing this it becomes more likely to re‐use components among disparate networking functions and to independently scale resources and investments according the specific application of the technology.

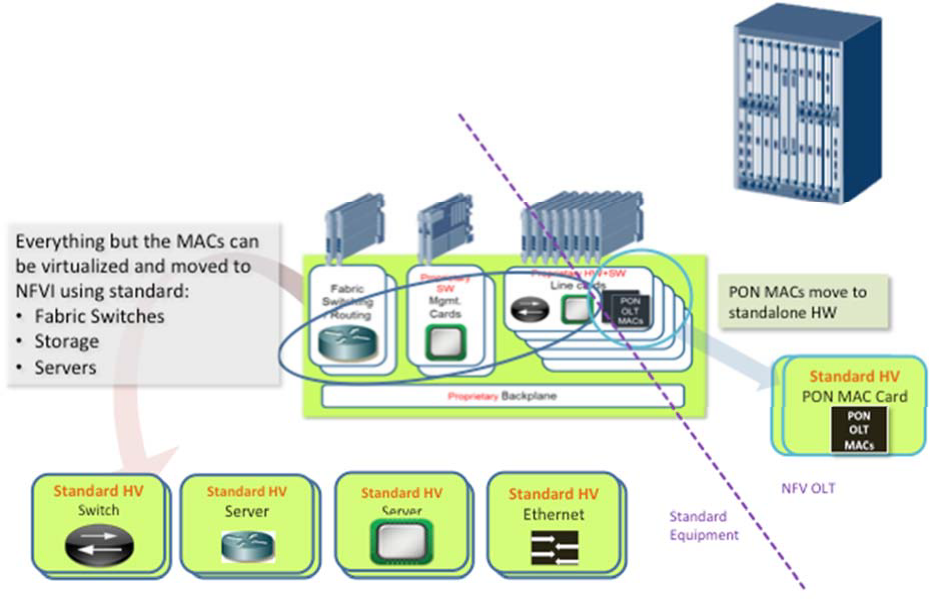


Figure 1 - Virtual OLT

Figure 1 shows the disaggregation of a typical OLT and the mapping of its functions to NFV infrastructure. The backplane or fabric of the OLT is mapped to the fabric of NFVI (ToR and EoR / leaf & spine switches). The interfaces to the fabric (what were card edge connectors) become simple Ethernet interfaces. The control and management functions are embodied in SDN control and Orchestration with a software stack that will be described shortly. Processing and configuration are mapped to compute and storage in NFVI. The figure shows that almost all the components in an OLT, those to the left of the dashed line, can be mapped to standard high‐volume (HV) components found in NFVI. The exception is in the XGS-PON PHY and MAC. Those are not typically found in NFVI and this specification describes a standard HV device that supports them.

In the Virtual OLT, the application of the AT&T Open XGS-PON 4-port Remote OLT is to facilitate attaching XGS-PON silicon to the fabric of NFVI – as shown in Figure 2.

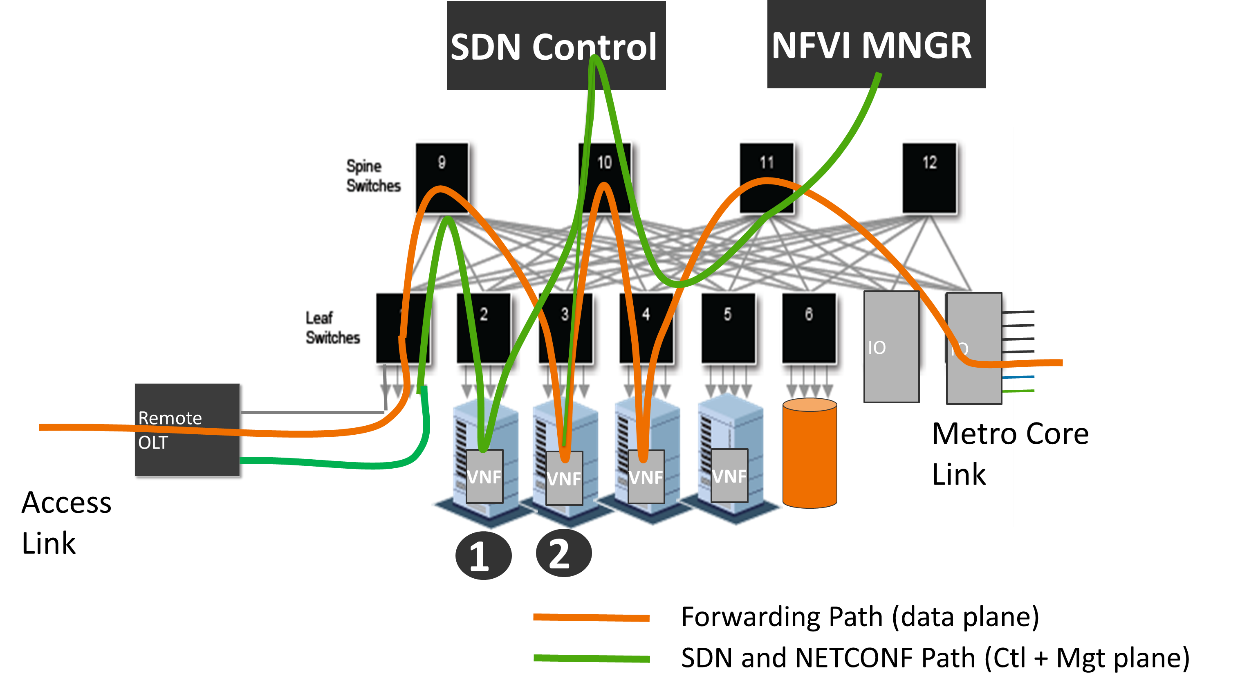


Figure 2 - Typical application of XGS-PON 4 Port Remote OLT

Figure 2 shows the Open XGS-PON 4-port Remote OLT attached to typical ToR (Leaf) switches in the lower left corner. Shown prominently at the top are processes that are run inside the compute VNFs at point 1 and 2. These processes provide the management and control plane functions that manage and control the overall system including the XGS-PON silicon within the Open XGS-PON 4-port Remote OLT.

The software used to support this system is partly shown in Figure 3. At the lowest level of the figure we find firmware and hardware drivers that are part of the software loaded and run on the BCM68620 SoC chip. That software is loaded on the chip and then subsequently configured and managed through a matching low‐level API along with an OMCI stack which is run on a commodity data center (DC) server. These elements are

colored blue because they are proprietary and specific to the BCM68620, and would need to be replaced to support other chips and PHY technologies.

The next layer up is shown in purple and represents open source software. The lowest layer of this software consumes OLT API calls and OMCI signaling and creates a homogenized abstraction of an OpenFlow controlled OLT – largely patterned after an Ethernet switch. This abstraction is then plugged into the southbound side of an OpenFlow agent and configuration management block, and that software comprises all the code to generically manage and control the Open XGS-PON 4-port Remote OLT.

The next layer in the software stack is an OpenFlow Controller and configuration. These might be combined or separate software. Finally, in green, we see the applications that embody the control plane and management applications for a number of access technologies and instances of each.

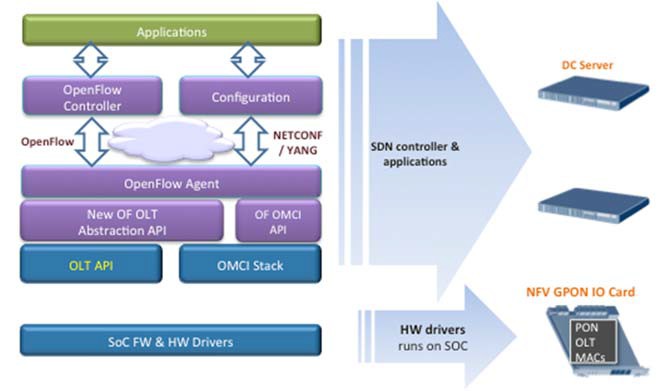


Figure 3 - Software stack for Open VOLT XGS-PON 4-port Remote OLT

To support this application, the Open XGS-PON 4-port Remote OLT minimizes the number of components populated on the system board and leverages external, scalable, available and re‐usable components instead.

This is the most basic and economic instantiation of this design. Management is performed through external processes and is communicated through a virtual LAN that isolates that traffic from customer traffic. Specifically, there is a need to support OOB (out of band management) LAN. The design also incorporates a baseboard management controller (BMC) to manage system resources.

# Mini OLT

The next application of this technology moves to the opposite extreme. In this case the Open XGS-PON 4-port Remote OLT is extended with Processing, Storage, and an internal PCIe communications to facilitate the device becoming a stand-alone OLT system. From a hardware perspective, the board is populated in addition to the components of the virtual OLT with a CPU and RAM, and Flash storage. This application is useful in one-off applications, in lab and development environments, and in places where NFVI isn’t available or desired. The software stack for this device can be identical to that used in the virtual OLT: where either part or even all the software shown in is hosted on the onboard CPU. However, it is also possible to optimize. For example, control and management applications could be written directly to the merchant silicon APIs. Obviously, hybrid approaches are also possible by making other software placement choices, and other software not shown above could also be run on the CPU. Note however, that this design has several single points of failure, and is not as robust from the perspective of availability as the virtual OLT.

# Timing

The next application covers a case for timing distribution. This application is largely independent of the previous ones. That is, regardless of whether there is an onboard software, processor and storage, there are situations when distributing timing is desired. The typical case for including timing distribution is where XGS-PON is used to provide backhaul for cell sites, but this is not a universal requirement for using GPON for cell site backhaul. In this application a Synchronization Management Unit is added to the system to facilitate SyncE and IEEE 1588 timing paths.

This overall design supports all the aforementioned use cases, and allows the omission or depopulation of various components as manufacturing options to source the device for the various use cases.

# XGS-PON Network

A 10 Gigabit Services PON (XGS-PON) network supports symmetrical 10G/10G communications to enable a variety of applications. Some key features include:

* Data rates of : ~10Gbps (9953Mbps) DS/~10Gbps (9953Mbps) US
* At least 128 ONTs (downstream PON endpoints) per PON Link
* ToD synchronization
* ONT power saving operation
* Optional downstream AES encryption for each port
* IPv6
* Dual-stack IPv4 and IPv6
* Symmetric bandwidth allocation

Figure 4 shows a typical XGS-PON Network.

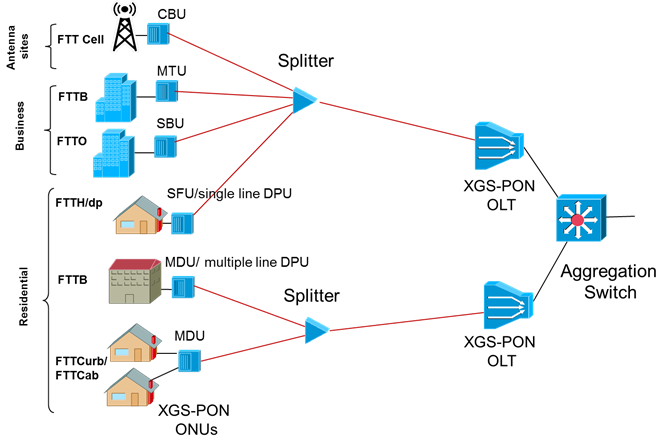


Figure 4 - XGS-PON Network

# System Overview

An overview of the system in terms of functional blocks is seen in Figure 5.



Figure 5 - Main system Block diagram

The block diagram in Figure 5 shows 2x BCM68620 devices connected to the QUX BCM88270 switch.

* The BMC (possibly FPGA) provides chassis management
* All main devices are managed either: inband from remote management software, or by the main CPU block using PCIe interface.
* The CPU block also provides optional for OOB LAN access/management.
* All the chassis devices are connected through an I2C network such as PSUs, Thermals, System LEDs
* The BMC provides multi master support, and Chassis Management arbitration.
* Each BCM68620 SoC is connecting directly to the PON XFP cage using the PON link physical connection and two 10G XFI links to the QUX device for the network uplink.
* Redundancy is managed by the QUX switching matrix.

The XGS-PON 4-port Remote vOLT system is a physical Hardened outdoor unit and consists of the following main HW modules:

## xPON SoC – Broadcom BCM68620

* The BCM68620 is a high-performance, single-chip, cost-effective OLT PON MAC SoC with support XGPON1, XGS-PON, NGPON2 and 10G-EPON.
* The SoC provides two ports of XGS-PON (10G/10G) links.
* The BCM68620 integrates NNI SerDes and MAC interfaces, ICF (Interconnect Function), PON MACs, and Burst mode PON SerDes interfaces.
* Supports external packet buffer for XGS-PON reassembly.
* Supports 800 MHz, 32-bit DDR3
* Size: 33 mm X 33 mm

## Host CPU

An open issue at the time of writing, is whether to have a modular host CPU, or whether to create a single design with a fixed selection.

* Using SoC processor, e.g. D-1500
* Memory: DRAM - 2GByte DDR3 72bit, NAND Flash + SDIO
* Management ports: 1000 Base-T Ethernet + UART
* Additional Interfaces: PCIe gen 2.0, SPI, I2C, GPIOs, IRQs

## BMC

An open issue at the time of writing, is whether to have a physical or logical BMC, or whether to make the BMC choice modular on a COM-Express.

* Serves for general ‘glue logic’ applications
  + For example: I2C control, LEDs, Interrupts + I/O expender, PS control, Power sequencing
* FPGA device (Reference PN): XC3S700AN-4FGG484C
* Number of IOs: 372
* Size: 23x23 mm
* Total ball count: 484

## Broadcom BCM88270 QUX - Switching & TM device

* The BCM88270 is a high-performance, single-chip, cost-effective switch and TM
* Performance - 120Gbps; 120Mpps
* OAM, 1588, SyncE Telecom DPLL
* 120Gbps- 28 x3.125G+ 8x10.3G SerDes
* TM - 32K queues, 32Mb on-chip buffering, Packet packing for improved burst absorption
* Max classification rules – can be the number of LLIDs/GEMs (Tunnel IDs) – 64K
* Size: 25x25 mm

# Physical Overview

## Dimensions

|  |  |  |
| --- | --- | --- |
|  | Inches | Millimeters |
| Length | 9.645 | 245 |
| Width | 11.81 | 300 |
| Height | 1.73 | 44 |
| Note: Width does not include mounting ears. | | |

## Panel LED Definitions

|  |  |  |
| --- | --- | --- |
| LED Name | Description | State |
| Diag | LED to indicate  system diagnostic test results | Green – Normal  Amber – Fault detected |
| LOC | LED to indicate Location of switch in Data Center | Blue Flashing – Set by management to locate switch  Off – Function not active |
| XFP LEDS | LED built into  XFP cage to indicate port status | On Green/Flashing – Port up with active ONTs .  Flashing indicates activity  On Amber – Port up with no active ONTs  Off – No Link/Port down |
| QSFP Break out  LEDs | Each QSFP28 has  four LEDs to indicate status of the individual  10G ports | On Green/Flashing – Individual 10G port has link at  10G. Flashing indicates activity  Off – No Link |
| OOB LED | LED to indicate  link status of  10/100/1000 management port | On Green/Flashing ‐ port has link  Off – No link |

### XFP Interface Module support

|  |  |
| --- | --- |
| 10Gb XGS-PON XFP Modules | Standard 10Gb XGS-PON XFP modules |

### QSFP Interface Module Support

|  |  |
| --- | --- |
| 40Gb QSFP Optical Modules | Standard 40Gb QSFP modules including but not limited to: 40GBASE-SR4, 40GBASE-LR4, 40GBASE-ER, AOC Cables |
| Direct Attach Copper (DAC) | Standard DAC cables including but not limited to: Passive cable up to 5m, Active cable up to 10m |

## Board placement

The below figure illustrates the board placement for the vOLT box. The placement consists of the following main elements:

### Front Panel

* PON Links: 4x XFP ports
* Uplink Ports:
  + Main active - 1x QSFP28

### LEDs

* QSFP28 LEDs
  + Two per XFP Module (Link, Activity)
  + Two per QSFP28 port (Link, Activity)
  + System and PSU LED indicators
* Console management port (RJ-45) – two stacked ports
* Reset button

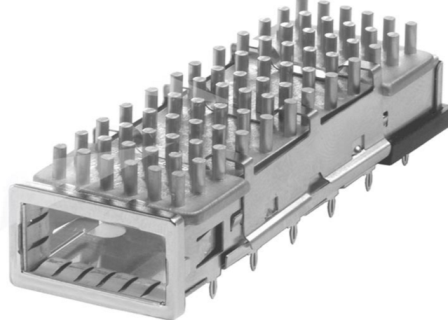


Figure 6 - Single XFP Module

### PCB Board Set

The XGS-PON 4-port Remote vOLT is composed of a single main PCB that contains all the main blocks and connectivity to front and rear panel connections.

### Power Supply Options

The XGS-PON 4-port Remote vOLT requires the support of two modes:

1. -48V DC line input
2. Pedestal power outlet

# PON Links

The XGS-PON 4-port Remote vOLT system is designed to support up to four PON links. The links will be using XFP modules.

Each BCM68620 device will be connecting to two XFP modules.

* Reference the ITUT standard G.9807.1

# Uplink

The XGS-PON 4-port Remote vOLT system is designed to support up to 4 links on the uplink side. All links will be connected directly from the BCM88270 QUX device to the single QSFP28 module placed in the front panel.

The dedicated links from the BCM88270 QUX device towards the QSFP28 module is configured to work in 10.3Gbit SERDES mode (XFI).

In case where uplink redundancy is required, it will be based on the QSFP28 module located on the front panel. Redundancy should be managed and controlled by the Host CPU application which will determine when and in which conditions the uplink redundancy should be active.

# General Specifications

## Software Support

The XGS-PON 4-port Remote vOLT supports a base software package composed of the following components:

## BMC support

AMI BMC or OpenBMC It’s an open work item to explore using these as a “virtual BMC”

## Open Network Linux (Used with D-1500 CPU)

See <http://opennetlinux.org/>for latest supported version

## Power Consumption

The total estimated system power consumption of the XGS-PON 4-port Remote vOLT is 58.0 Watts. This is based upon worst case power assumptions for traffic, optics used, and environmental conditions. Typical power consumption is ~60 Watts (Max.)

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Main Blocks | Qnt. | Typ. (W) | Max. (W) | Total Typ. (W) | Total Max. (W) |
| 2 x BCM68620,  4 x XGS-PON Optics, BCM88270 + DDRs | 1 |  |  | <34 | <39 |
| QSFP28 Module | 1 | 3.0 | 3.5 | 3.0 | 3.5 |
| FPGA | 1 | 1.1 | 1.3 | 1.1 | 1.3 |
| PCIe Switch | 1 | 1.0 | 1.2 | 1.0 | 1.2 |
| Timing (DPLL, clocks) | 1 | 0.4 | 0.5 | 0.4 | 0.5 |
| CPU + Memory | 1 | 3.0 | 3.5 | 3.0 | 3.5 |
|  |  |  |  | 42.0 | 48.3 |
| Power Supply efficiency | 1 | 6.3 | 9.7 | 6.3 | 9.7 |
|  |  |  |  |  |  |
| Total estimated Power |  |  |  | 48.2 | 58.0 |

## Environmental

* 0 to 70 Degrees C operating range
* ‐40 to 70 Degrees C storage temperate range
* Humidity 5% to 95% non‐condensing (operational and storage)
* Vibration – IEC 68‐2‐36, IEC 68‐2‐6
* Shock – IEC 68‐2‐29
* Acoustic Noise Level – Under 60dB in 40 degree C
* Altitude ‐ 15,000 (4572 meters) tested operational altitude

## Safety

 NRTL/ Canada

 CB (Issued by TUV/RH)

 China CCC

## Electromagnetic Compatibility

* CE
* EN55022 Class A
* EN55024
* EN61000‐3‐2
* EN61000‐3‐3
* FCC Title 47, Part 15, Subpart B Class A
* VCCI Class A
* CCC

## ROHS

Restriction of Hazardous Substances (6/6)

Compliance with Environmental procedure 020499‐00 primarily focused on Restriction of Hazardous substances (ROHS Directive 2002/95/EC) and Waste and Electrical and Electronic Equipment (WEEE Directive 2002/96/EC)

## Vibration and Shock

The motherboard meets shock and vibration requirements according to the following IEC specifications: IEC78-2-(\*) and IEC721-3-(\*) Standard & Levels.

## Prescribed Materials

### Disallowed Components

The following components are not used in the design of the motherboard:

* Components disallowed by the European Union's Restriction of Hazardous Substances
* Directive (RoHS 6)
* Trimmers and/or potentiometers
* Dip switches

### Capacitors and Inductors

The following limitations apply to the use of capacitors:

* Only aluminum organic polymer capacitors made by high quality manufacturers are used; they must be rated 105°C
* All capacitors have a predicted life of at least 50,000 hours at 45°C inlet air temperature, under worst conditions
* Tantalum capacitors are forbidden
* SMT ceramic capacitors with case size > 1206 are forbidden (size 1206 are still allowed)
* Ceramic material for SMT capacitors must be X7R or better material (COG or NP0 type should be used in critical portions of the motherboard)
* Only SMT inductors may be used. The use of through whole inductors is disallowed.

1. This type of system is described in ETSI NFV architecture, where it comprises the Infrastructure that supports Network Functions Virtualization – often called NFVI. Additionally, the open software beyond that described in this specification is collected and distributed as one of the use cases for the ONS2015 ‐ CORD project at ON.Labs. See <https://wiki.onosproject.org/display/ONOS/ONOS+Use+Cases> [↑](#footnote-ref-1)