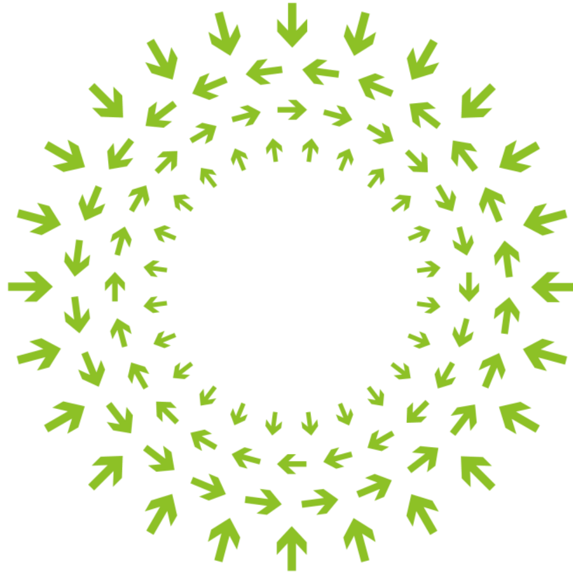

Open CloudServer OCS Tray Mezzanine Specification Version 2.0

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Revision History

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1 Summary

This specification, *Open CloudServer OCS Tray Mezzanine Version 2.0*, describes the physical and interface requirements for the Open CloudServer (OCS) tray mezzanine card. The mezzanine card will be installed on the tray backplane and will have a Peripheral Component Interconnect Express (PCIe) x16 Gen3 interface. This interface can either be used as one x16, two x8, or four x4 channels.

Note that this specification does not cover the functional or features requirements for the mezzanine cards that will be developed for this project.

There are two mechanical specifications for the mezzanine card:

- Model A provides a 17.5mm stack height and a 13mm top side height allowance.
- Model B provides a 15.5mm stack height and a 15mm top side height allowance.

Figure 1 shows Model A of the OCS tray mezzanine card.

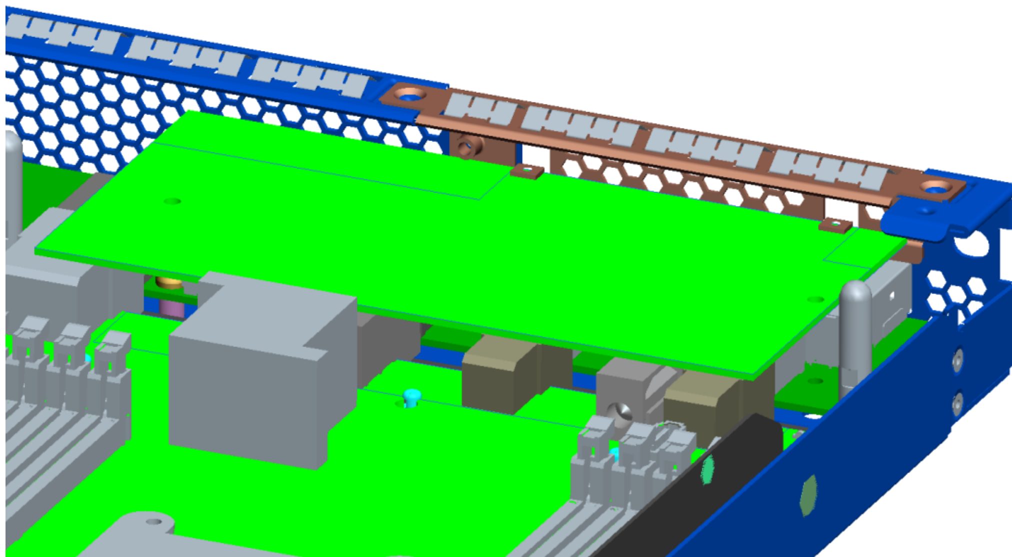

Figure 1: OCS tray mezzanine card Model A

Figure 2 shows Model B of the OCS tray mezzanine card.

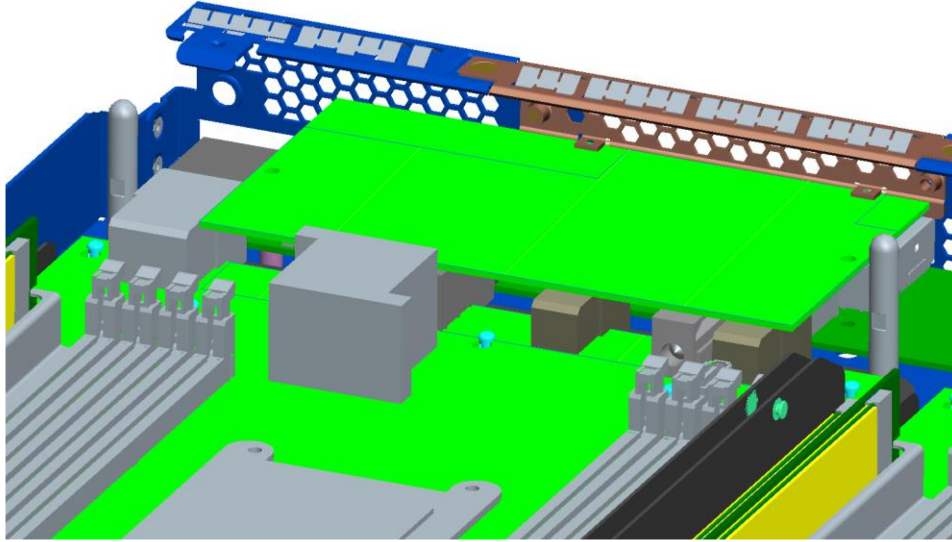

Figure 2: OCS tray mezzanine card Model B

2 Interface Connector

The connector interfaces between the tray mezzanine card and the tray backplane use the Samtec SEARAY solution. The tray backplane uses a Samtec SEAF (female) connector and the tray mezzanine card uses a Samtec SEAM (male) connector. Table 1 lists the manufacturing part numbers (MPNs) for Model A and Model B cards. Note that the mating tray backplane SEAF connector is fixed and will always be SEAF-20-06.5-S-08-2-A-K-TR; only the mezzanine card can vary.

Table 1: Connector manufacturing part numbers

Model	Manufacturer	Mezzanine card connector MPN	Mating (MB) connector MPN
A	Samtec	SEAM-20-11.0-S-08-2-A-K-TR (or equivalent)	SEAF-20-06.5-S-08-2-A-K-TR (or equivalent)
B	Samtec	SEAM-20-9.0-S-08-2-A-K-TR (or equivalent)	SEAF-20-06.5-S-08-2-A-K-TR (or equivalent)

Figure 3 shows an example of a stackup for a Model A card, with a 17.5mm stack height with a 6.5mm SEAF connector and an 11mm SEAM connector. In this configuration, it is expected that taller components would be placed on the top side of the printed circuit board (PCB). Note that this is an example; a different height SEAM can be used depending on the tray mezzanine back side keepout requirements and the required height to clear obstructions on the tray backplane. See Section 3 of this specification for more detailed information.

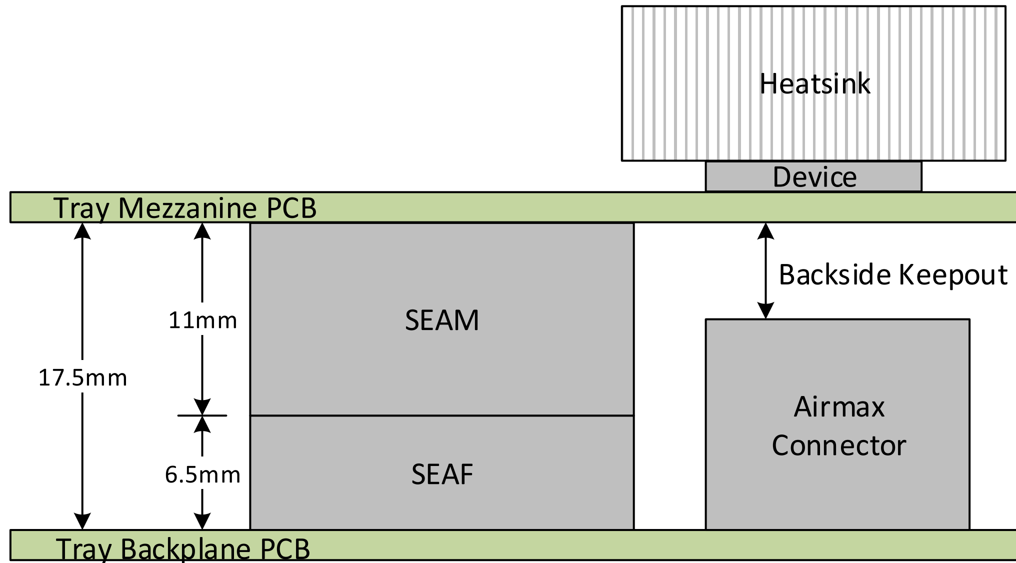

Figure 3: Model A connector stackup example

2.1 Signal Definitions

Table 2 defines the signals used in the tray backplane interface.

Table 2: Tray mezzanine connector signal definitions

Bus type	I/O	Logic	Description
PCIE_B2T_TX_DP/N[15:0]	I	Current-mode logic (CML)	PCIe Gen3 Transmit from blade to tray mezzanine card through tray backplane
PCIE_T2B_RX_DP/N[15:0]	O	CML	PCIe Gen3 Receive from tray mezzanine card to blade through tray backplane
CLK_100M_P/N[3:0]	I	CML	PCIe Gen3 Clock from blade to tray mezzanine card through tray backplane
PCIE_RESET_N[3:0]	I	3.3V	PCIe Reset from blade to tray mezzanine card through tray backplane
PCIE_WAKE_N	O	3.3V	PCIe Wake from blade to tray mezzanine card through tray backplane
PCIE_CFG_ID[1:0]	O	3.3V	PCIe Configuration ID from tray mezzanine card to blade through tray backplane Motherboard shall have 100k pull-up resistors on both pins

Bus type	I/O	Logic	Description
			Mezzanine card shall place 1k pull-down resistors for the desired configuration 00 = 1x16 bifurcation 01 = 2 x8 bifurcation 10 = 4 x4 bifurcation 11 = N/A
MEZZ_EN	I	3.3V	3.3V Power Enable from blade to tray mezzanine card through tray backplane
MEZZ_PRESENT_N	O	3.3V	Present signal from tray mezzanine card to blade through tray backplane Should be tied to GND on the tray mezzanine card
MEZZ_SCL	I	3.3V	I2C Clock from blade to tray mezzanine card through tray backplane
MEZZ_SDA	I/O	3.3V	I2C Data from blade to tray mezzanine card through tray backplane
P12_MEZZ	I	12V	12V Power from blade to tray mezzanine card through tray backplane Max power is 36W
Ground		0V	Ground pins

Table 3 shows how the reset and clock signals are mapped to support each of the bifurcation cases for PCIe to the tray mezzanine.

Table 3: PCIe bifurcation mapping

	1 x 16	2 x 8		4 x 4			
Signal name	**15:0**	**15:8**	**7:0**	**15:12**	**11:8**	**7:4**	**3:0**
PCIE_RESET_N[0]	X	X		X			
PCIE_RESET_N[1]			X		X		
PCIE_RESET_N[2]						X	
PCIE_RESET_N[3]							X
CLK_100M_P/N[0]	X	X		X			
CLK_100M_P/N[1]			X		X		
CLK_100M_P/N[2]						X	
CLK_100M_P/N[3]							X

2.2 Connector Pinout

Table 4 lists the pinout for the 160-pin connector on the tray mezzanine card that interfaces to the tray backplane.

Table 4: Tray mezzanine connector pinout

160	MEZZ_PRESENT_B1_N	PCIE_WAKE_B1_N	MEZZ_B1_SDA	MEZZ_B1_EN	MEZZ_B1_SCL	P12_MEZZ	P12_MEZZ	P12V_MEZZ	153
152	PCIE_RESET_B1_N<3>	PCIE_RESET_B1_N<1>	PCIE_RESET_B1_N<0>	PCIE_CFG_B1_ID0	PCIE_CFG_B1_ID1	GND	GND	P12V_MEZZ	145
144	CLK_100M_N<3>	PCIE_RESET_B1_N<2>	CLK_100M_N<2>	GND	CLK_100M_N<1>	GND	CLK_100M_N<0>	P12V_MEZZ	137
136	CLK_100M_P<3>	GND	CLK_100M_P<2>	GND	CLK_100M_P<1>	GND	CLK_100M_P<0>	GND	129
128	GND	PCIE_B2T_TX_DN<8>	GND	PCIE_B2T_TX_DN<0>	GND	PCIE_T2B_RX_DN<8>	GND	PCIE_T2B_RX_DN<0>	121
120	GND	PCIE_B2T_TX_DP<8>	GND	PCIE_B2T_TX_DP<0>	GND	PCIE_T2B_RX_DP<8>	GND	PCIE_T2B_RX_DP<0>	113
112	PCIE_B2T_TX_DN<9>	GND	PCIE_B2T_TX_DN<1>	GND	PCIE_T2B_RX_DN<9>	GND	PCIE_T2B_RX_DN<1>	GND	105
104	PCIE_B2T_TX_DP<9>	GND	PCIE_B2T_TX_DP<1>	GND	PCIE_T2B_RX_DP<9>	GND	PCIE_T2B_RX_DP<1>	GND	97
96	GND	PCIE_B2T_TX_DN<10>	GND	PCIE_B2T_TX_DN<2>	GND	PCIE_T2B_RX_DN<10>	GND	PCIE_T2B_RX_DN<2>	89
88	GND	PCIE_B2T_TX_DP<10>	GND	PCIE_B2T_TX_DP<2>	GND	PCIE_T2B_RX_DP<10>	GND	PCIE_T2B_RX_DP<2>	81
80	PCIE_B2T_TX_DN<11>	GND	PCIE_B2T_TX_DN<3>	GND	PCIE_T2B_RX_DN<11>	GND	PCIE_T2B_RX_DN<3>	GND	73
72	PCIE_B2T_TX_DP<11>	GND	PCIE_B2T_TX_DP<3>	GND	PCIE_T2B_RX_DP<11>	GND	PCIE_T2B_RX_DP<3>	GND	65
64	GND	PCIE_B2T_TX_DN<12>	GND	PCIE_B2T_TX_DN<4>	GND	PCIE_T2B_RX_DN<12>	GND	PCIE_T2B_RX_DN<4>	57
56	GND	PCIE_B2T_TX_DP<12>	GND	PCIE_B2T_TX_DP<4>	GND	PCIE_T2B_RX_DP<12>	GND	PCIE_T2B_RX_DP<4>	49
48	PCIE_B2T_TX_DN<13>	GND	PCIE_B2T_TX_DN<5>	GND	PCIE_T2B_RX_DN<13>	GND	PCIE_T2B_RX_DN<5>	GND	41
40	PCIE_B2T_TX_DP<13>	GND	PCIE_B2T_TX_DP<5>	GND	PCIE_T2B_RX_DP<13>	GND	PCIE_T2B_RX_DP<5>	GND	33
32	GND	PCIE_B2T_TX_DN<14>	GND	PCIE_B2T_TX_DN<6>	GND	PCIE_T2B_RX_DN<14>	GND	PCIE_T2B_RX_DN<6>	25
24	GND	PCIE_B2T_TX_DP<14>	GND	PCIE_B2T_TX_DP<6>	GND	PCIE_T2B_RX_DP<14>	GND	PCIE_T2B_RX_DP<6>	17
16	PCIE_B2T_TX_DN<15>	GND	PCIE_B2T_TX_DN<7>	GND	PCIE_T2B_RX_DN<15>	GND	PCIE_T2B_RX_DN<7>	GND	9
8	PCIE_B2T_TX_DP<15>	GND	PCIE_B2T_TX_DP<7>	GND	PCIE_T2B_RX_DP<15>	GND	PCIE_T2B_RX_DP<7>	GND	1

2.3 Power

The tray mezzanine accepts a conditioned 12V from the tray backplane through five pins on the SEAM connector. This makes it possible for an estimated 3A of 12V current (36W) to the mezzanine, assuming 50% derating at 95°C for the connector pins. Note that this describes the power capability only, and does not imply the supported thermal envelope.

3 Mechanical Control Outline

Figure 4 and Figure 5 show the mechanical control outline for Model A and Model B cards. Either model may be selected to develop a card.

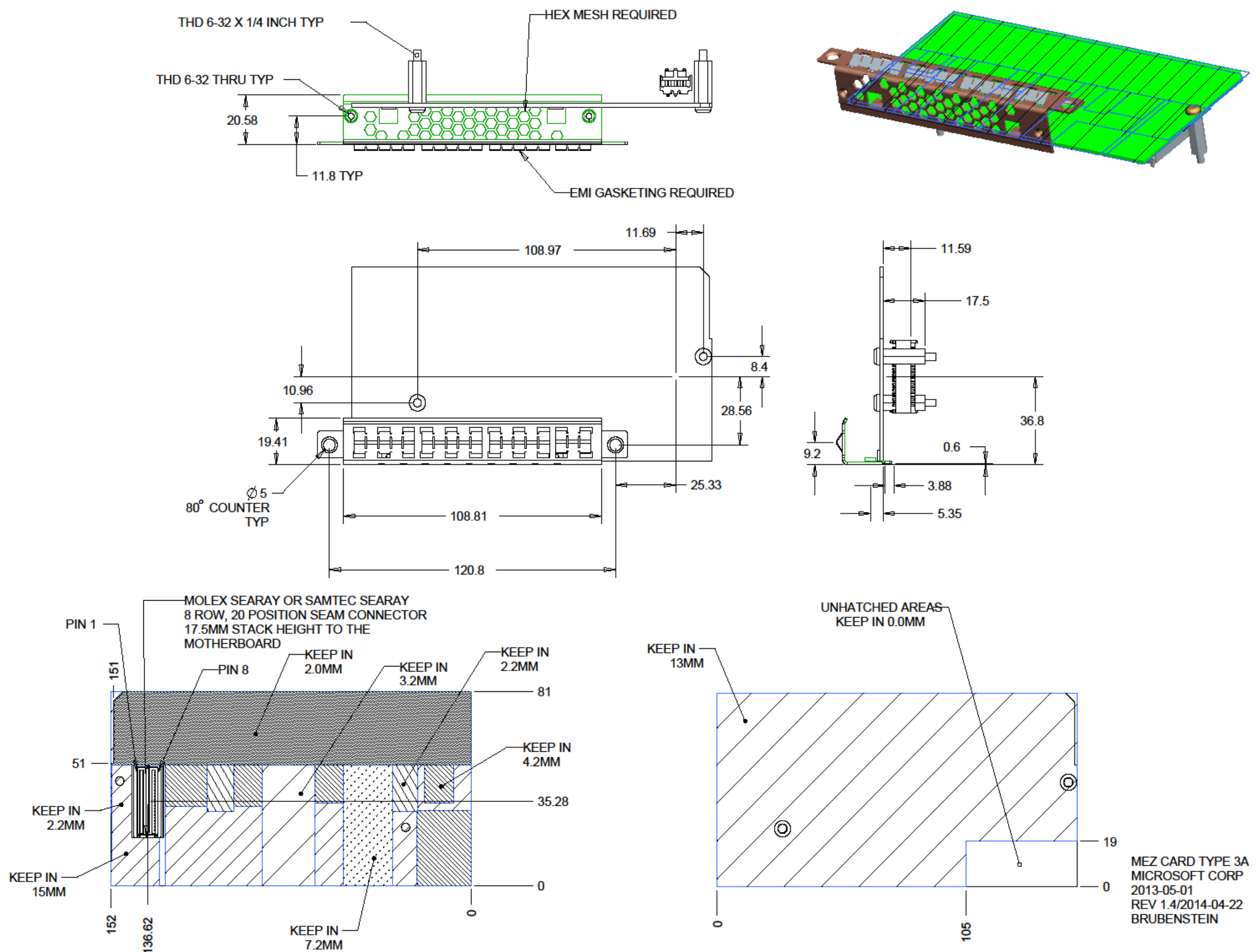

Figure 4: Drawing of Model A card

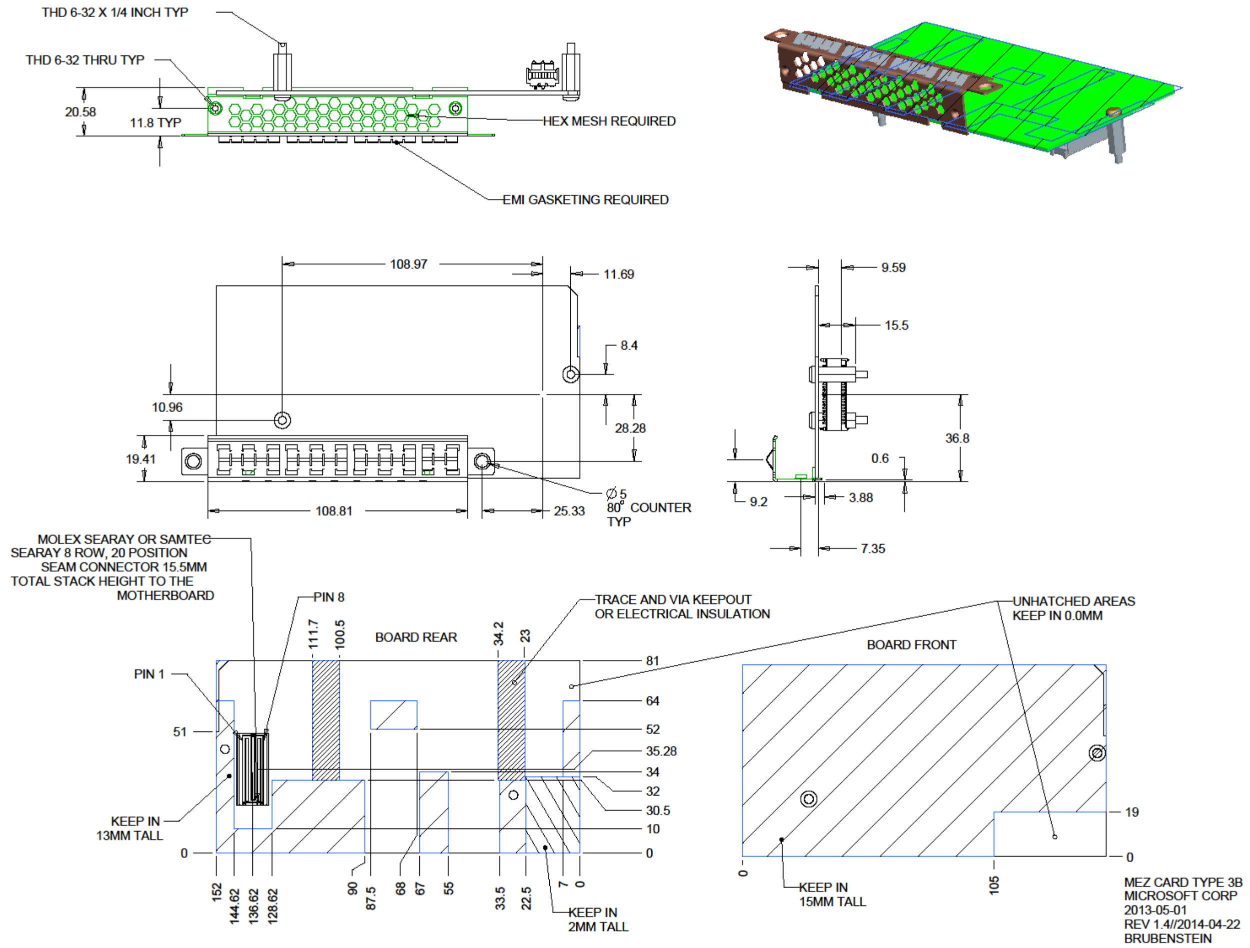

Figure 5: Drawing of Model B card

4 CAD Model Capture

Figure 6 and Figure 7 show views of Computer-Aided Design (CAD) captures of Model A and Model B cards plugged into side-by-side blades.

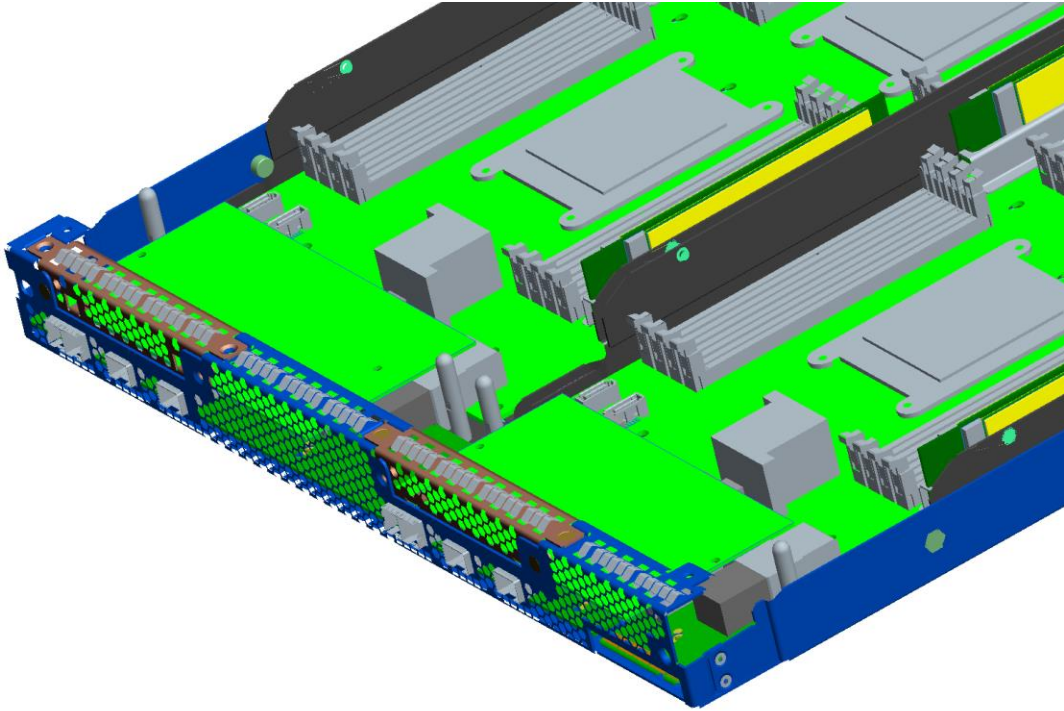

Figure 6: View from front of Model A and Model B plugged into side-by-side blades

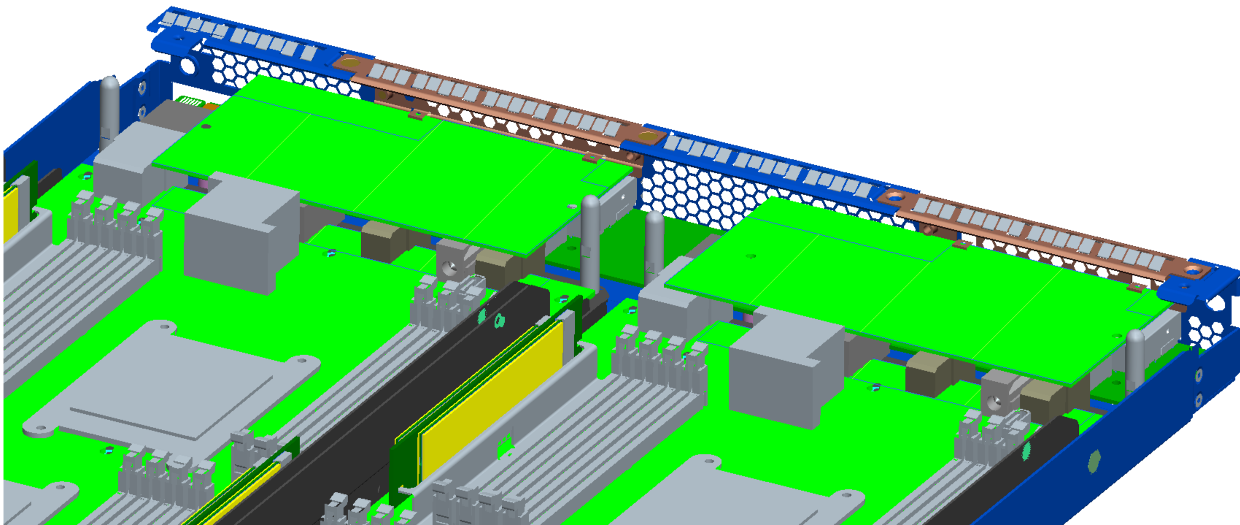

Figure 7: View from inside of Model A and Model B plugged into side-by-side blades

5 Thermal Specification

The mezzanine card is presented with an approaching airflow temperature of 70°C and a flow rate of 0.61m/s. No downstream airflow requirements are placed on the mezzanine card.

6 Standoffs and Screws for Assembly

The mezzanine card manufacturer is required to provide standoffs and screws to assemble the mezzanine card to the tray backplane board. The standoffs are to be provided loose in a bag and secured during assembly of the card to the tray backplane.