

CHASSIS MANAGEMENT BOARD

DVT

PCB Rev : D

PCB P/N:DAT6MTH3AD0

Date : 2012/10/23

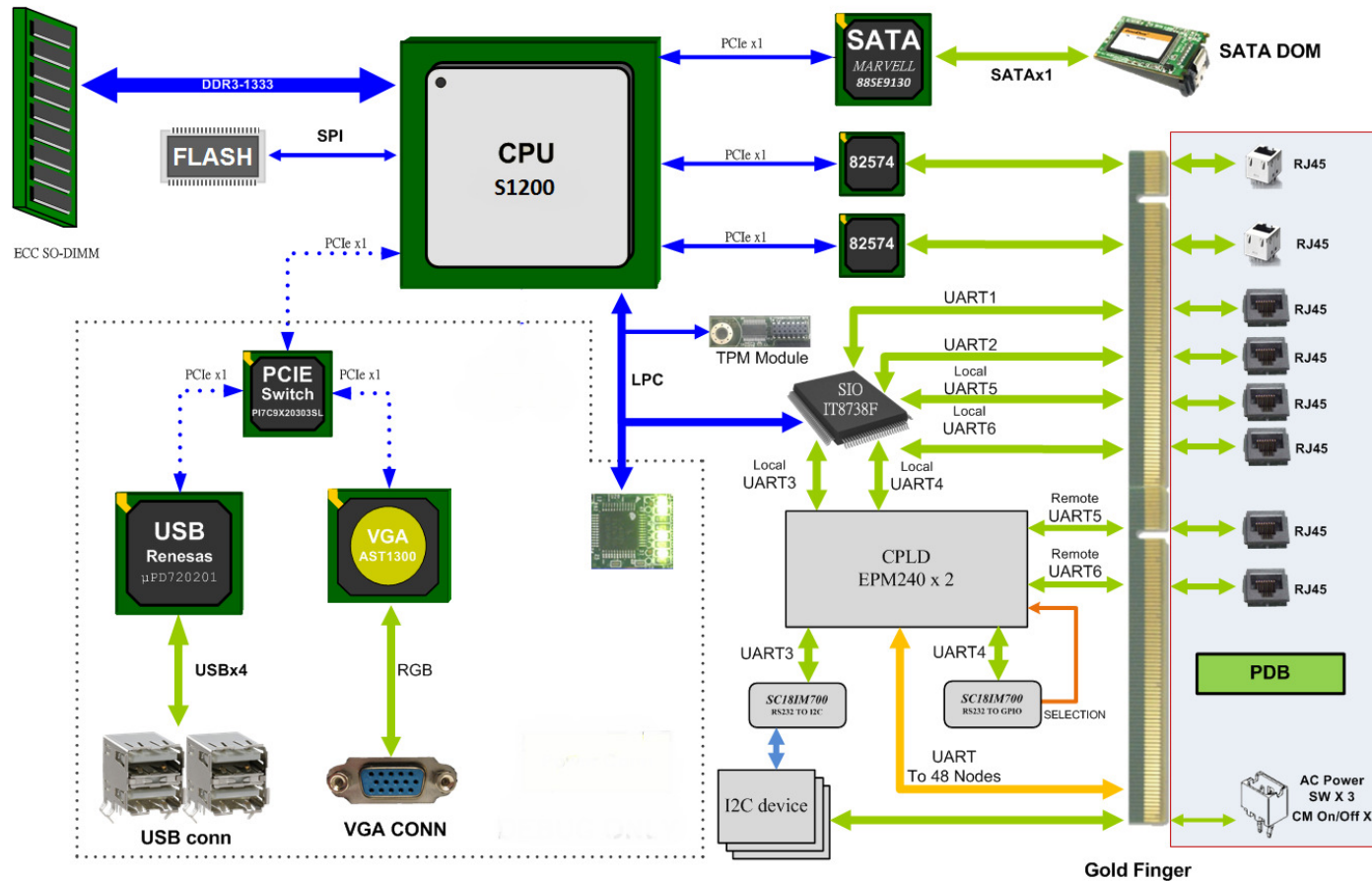


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|-----------------------------------------|-----------------|-------|---------|
| Cloud Server Infrastructure Engineering | | | |
| Title | | | |
| Chassis Manager Assembly V1 | | | |
| Size | Document Number | | |
| | Cover | | |
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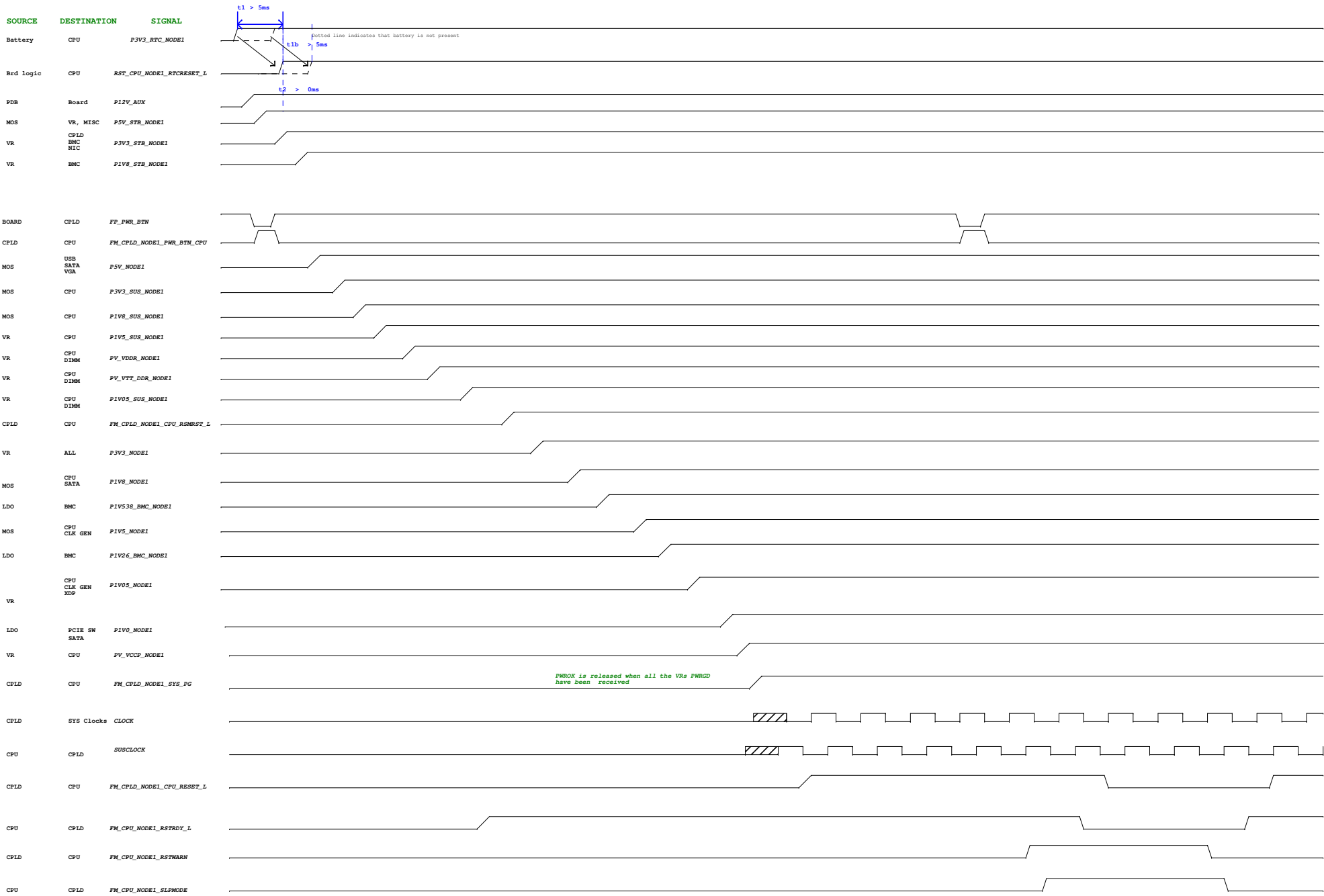
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| 14 | NODE1 CPU DDR3 INTERFACE | 57 | USB | | | | |
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| 24 | NODE1 CPU DECOUPLING | 67 | NODE1 CPLD (1) | | | | |
| 25 | BLANK | 68 | NODE1 CPLD (2) | | | | |
| 26 | NODE1 CPU TEMPERATURE ADC | 69 | NODE1 POWER_BUTTON | | | | |
| 27 | NODE1 SO-DIMM DIMM | 70 | LEVEL SHIT | | | | |
| 28 | BLANK | 71 | P5V_STB & P3V3_STB | | | | |
| 29 | BLANK | 72 | P1V05_SUS & P1V0_NODE1 | | | | |
| 30 | PCIE_SWITCH | 73 | P1V5_SUS & P1V8_SUS | | | | |
| 31 | BLANK | 74 | P1V8_STB & P1V538_BMC | | | | |
| 32 | NODE1 AST1300_DDRIII & I2C | 75 | P1V26_BMC | | | | |
| 33 | NODE1 AST1300_DDRIII MEMORY | 76 | P3V3_SUS | | | | |
| 34 | NODE1 AST1300_SPI_UART_MAC | 77 | P5V & P3V3 | | | | |
| 35 | NODE1 AST1300_GPIO_JTAG_MIS | 78 | P1V8 & P1V05 | | | | |
| 36 | NODE1 AST1300_POWER | 79 | P1V5 | | | | |
| 37 | NODE1 AST1300_HW STRAPPING | 80 | PV_VDDR & PV_VTT_DDR | | | | |
| 38 | BLANK | 81 | VCCP_CPU | | | | |
| 39 | BLANK | 82 | SCREW, HOLE, MISC | | | | |
| 40 | BLANK | 83 | SET2DIL | | | | |
| 41 | BLANK | 84 | BLANK | | | | |
| 42 | BLANK | 85 | BLANK | | | | |
| 43 | BLANK | | | | | | |



CM Block Diagram

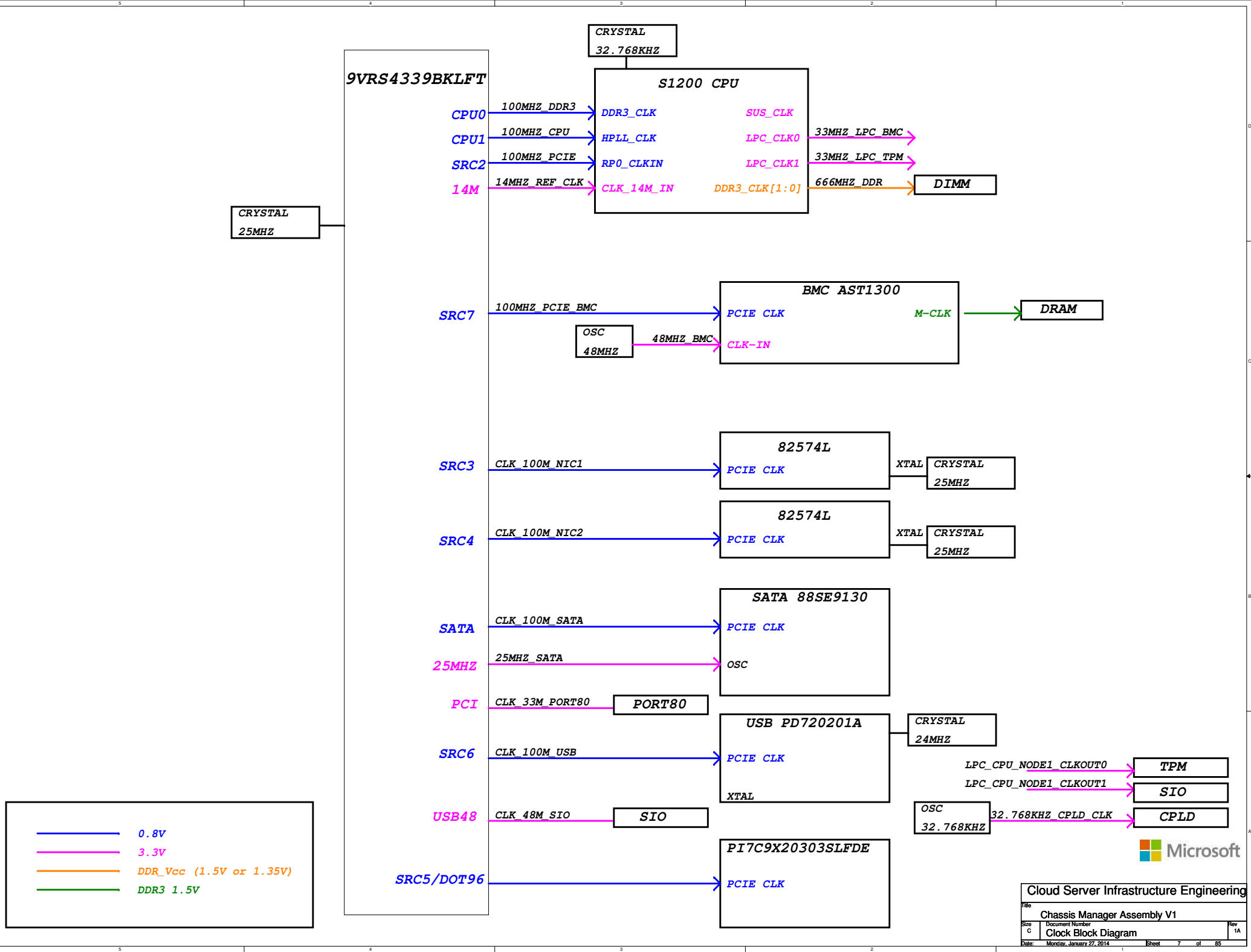


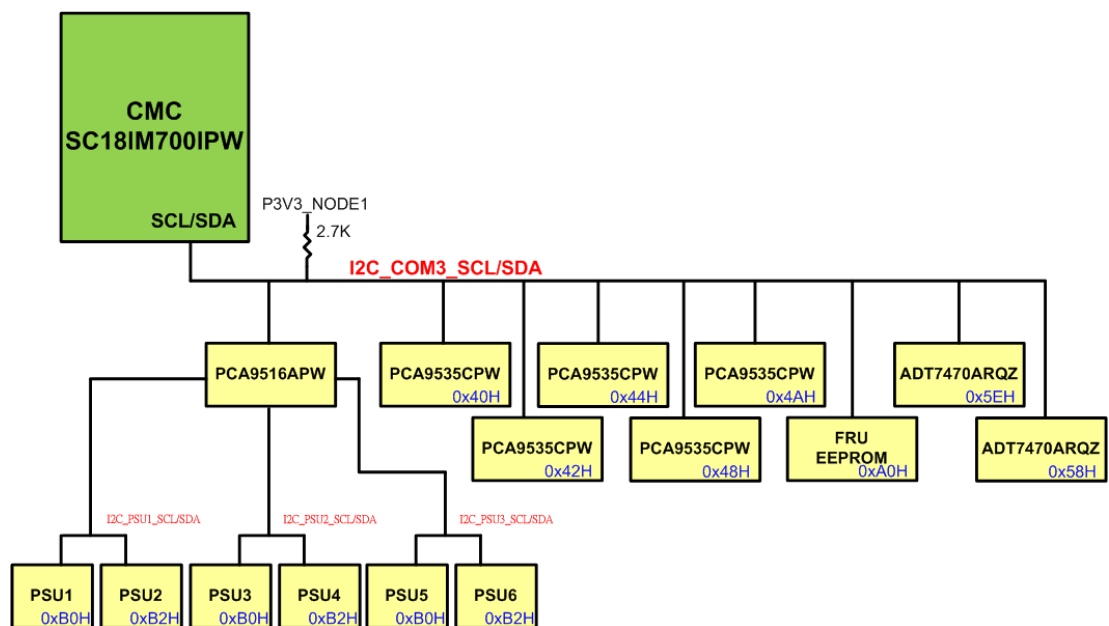
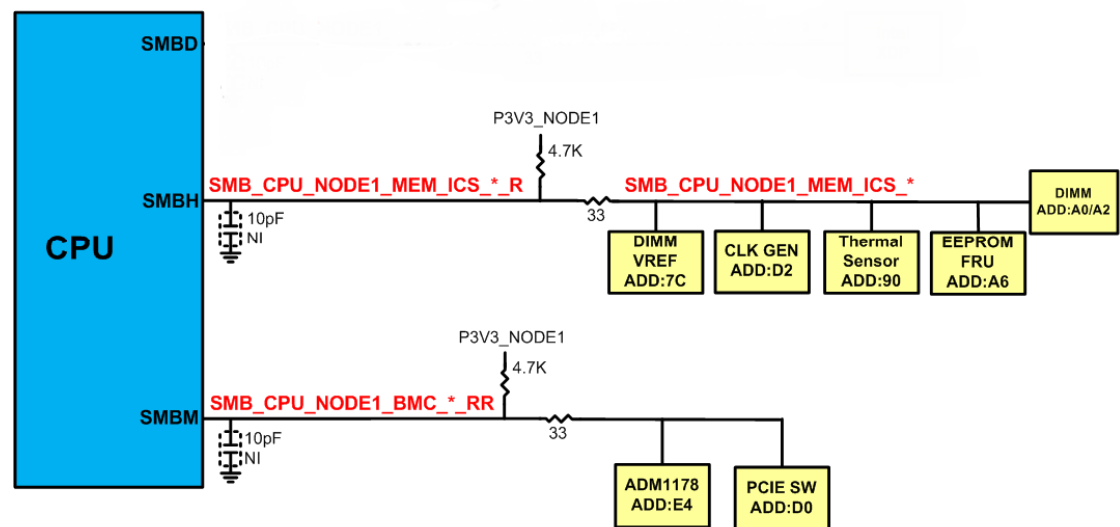
System Power Up/Down Sequence



| Layer | Lyr Type | Finished Cu Wt | Thickness(mils) | Tolerance | Er |
|-----------------|----------|--------------------|-----------------|-----------|-----|
| | | Soldermask | 0.65 | | 3.8 |
| 1 | TOP | 0.5 o.z. + plating | 1.9 | | |
| | | Prepreg | 2.70 | | 4.0 |
| 2 | GND1 | 1 oz | 1.2 | | |
| | | Core | 4.00 | | 4.1 |
| 3 | IN1 | 1 oz | 1.2 | | |
| | | Prepreg | 12.00 | | 4.0 |
| 4 | VCC1 | 1 oz | 1.20 | | |
| | | Core | 4.00 | | 4.1 |
| 5 | VCC2 | 1 oz | 1.20 | | |
| | | Prepreg | 4.00 | | 4.0 |
| 6 | GND2 | 1 oz | 1.20 | | |
| | | Core | 4.00 | | 4.1 |
| 7 | IN2 | 1 oz | 1.20 | | |
| | | Prepreg | 12.00 | | 4.0 |
| 8 | IN3 | 1 oz | 1.2 | | |
| | | Core | 4.00 | | 4.1 |
| 9 | GND3 | 1 oz | 1.2 | | |
| | | Prepreg | 2.70 | | 4.0 |
| 10 | BOT | 0.5 o.z. + plating | 1.9 | | |
| | | Soldermask | 0.65 | | 3.8 |
| Total Thickness | | | 64.10 | +/-10% | |







PWR_BTN_NODE1_L

FM_CPLD_NODE1_PWR_BTN_L

EPM240F100C5N

CPU

MAX809SEUR+

PWRGD_NODE1_P12V_PG

TPS54326
(P5V_STB_NODE1)

PWRGD_NODE1_P5V_STB_PG

TPS54326RGTR
(P3V3_STB_NODE1)

PWRGD_NODE1_P3V3_STB_PG

FM_CPLD_NODE1_P1V8_STB_EN

TPS54326RGTR
(P1V8_STB_NODE1)

PWRGD_NODE1_P1V8_STB_PG

FM_CPLD_NODE1_P1V538_BMC_EN

RT9018B-25GQW
(P1V538_BMC_NODE1)

PWRGD_NODE1_P1V538_BMC_PG

FM_CPLD_NODE1_P1V26_STB_EN

RT9018B-18GQW
(P1V26_BMC_NODE1)

PWRGD_NODE1_P1V26_STB_PG

FM_CPLD_NODE1_PVDDR_STB_EN

TPS51518RUKR
(PV_VDDR_NODE1)

PWRGD_NODE1_PVDDR_STB_PG

FM_CPLD_NODE1_PVTT_DDR_EN

TPS51200
(PV_VTT_DDR_NODE1)

PWRGD_NODE1_PVTT_DDR_PG

FM_CPLD_NODE1_P1V05_SUS_EN

RT9018B-25GQW
(P1V05_SUS_NODE1)

PWRGD_NODE1_P1V05_SUS_PG

FM_CPLD_NODE1_P1V5_SUS_EN

RT9018B-25GQW
(P1V5_SUS_NODE1)

PWRGD_NODE1_P1V05_SUS_PG

FM_CPLD_NODE1_P3V3_SUS_EN

AON7212
(P3V3_SUS_NODE1)

FM_CPLD_NODE1_P1V8_SUS_EN

AON7212
(P1V8_SUS_NODE1)

FM_CPLD_NODE1_P5V_EN

AON7212
(P5V_NODE1)

FM_CPLD_NODE1_P3V3_EN

TPS54326RGTR
(P3V3_NODE1)

PWRGD_NODE1_P3V3_PG

RST_CPU_NODE1_SRTCST_L

FM_CPLD_NODE1_CPU_RSMRST_L

FM_CPLD_NODE1_SYS_PG

FM_CPLD_NODE1_CPU_RESET_L

FM_CPU_NODE1_RSTRDY_L

FM_CPU_NODE1_RSTWARN

FM_CPU_NODE1_SLPMODE

FM_CPLD_NODE1_P1V8_EN

AON7212
(P1V8_NODE1)

FM_CPLD_NODE1_P1V5_EN

AON7212
(P1V5_NODE1)

FM_CPLD_NODE1_P1V0_EN

PWRGD_NODE1_P1V0_NODE1

RT9018B-25GQW
(P1V0_NODE1)

FM_CPLD_NODE1_PVCCP_EN

PWRGD_NODE1_PVCCP_PG

RT8167BGQW
(PV_VCCP_NODE1)

FM_CPLD_NODE1_P1V05_EN

PWRGD_N1_P1V05_PG

TPS51219RTER
(P1V05_NODE1)

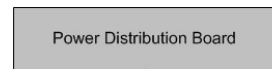


Cloud Server Infrastructure Engineering

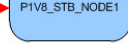
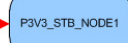
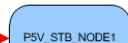
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| Chassis Manager Assembly V1 | | | |
| Size | Document Number | Rev | |
| C | Power Good / Reset Tree | 1A | |
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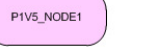
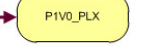
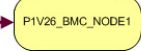
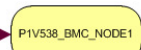
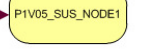
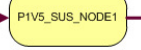
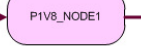
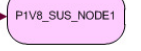
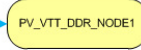
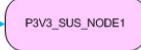
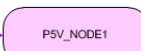
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| Cloud Server Infrastructure Engineering | | | |
| Title | | Chassis Manager Assembly V1 | |
| Size | Document Number | Rev | |
| C | Blank | 1A | |
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P12V_PDB



CM Board Power Block Diagram



Rev 0.2
2012/07/03



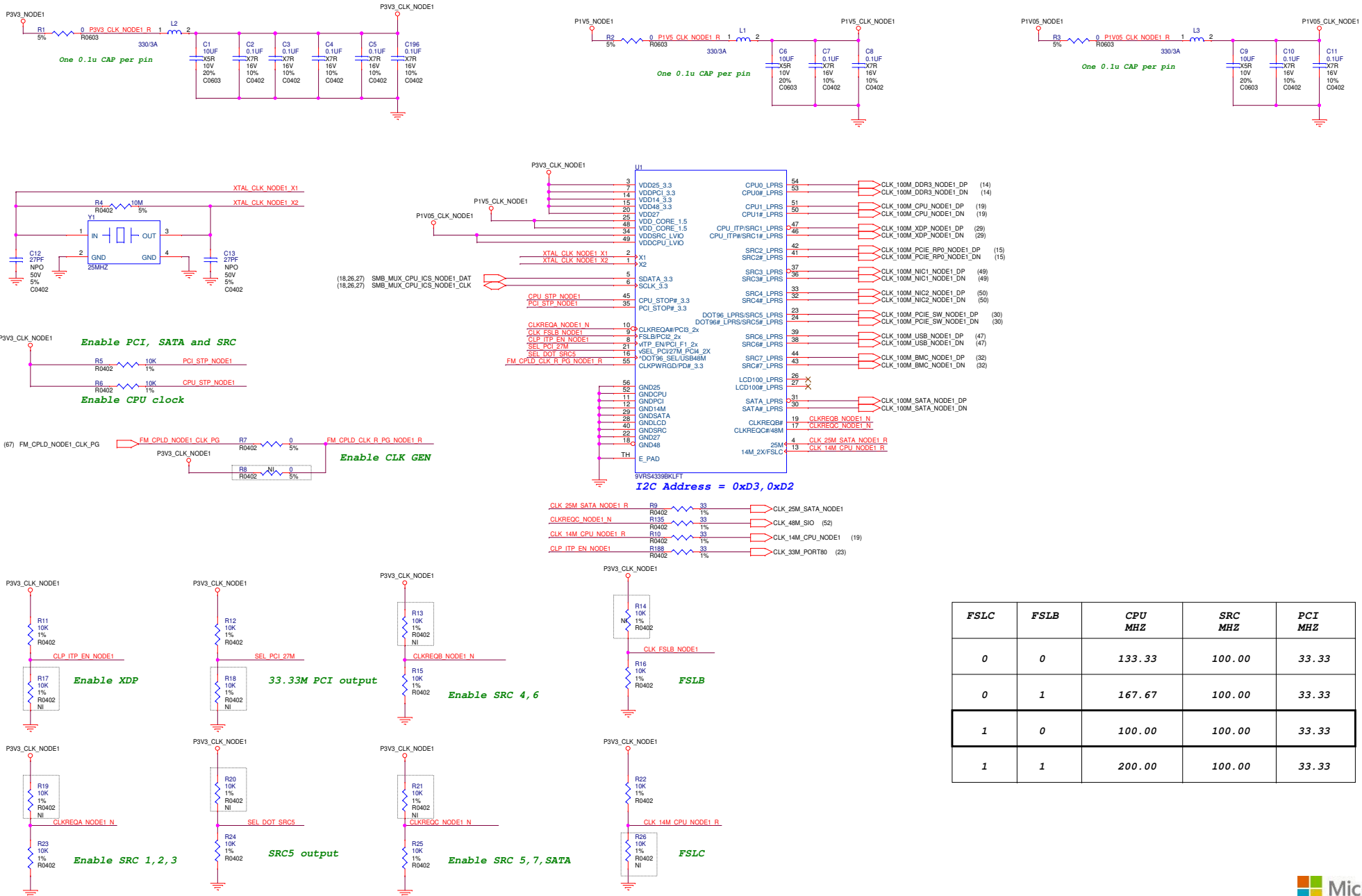
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| Cloud Server Infrastructure Engineering | | | |
| Chassis Manager Assembly V1 | | | |
| Size | Document Number | Rev 1A | |
| C | Power Topology | | |
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RJ-45 Port Pin-outs

| Signal | Console Port (DTE) | RJ-45 Rolled Cable | Adapter | Adapter | Signal |
|--------|--------------------|--------------------|----------|-----------|--------|
| | RJ-45 | RJ-45 Pin | DB-9 Pin | DB-25 Pin | |
| CTS | 1 | 8 | 7 | 4 | RTS |
| DTR | 2 | 7 | 4 | 20 | DSR |
| TxD | 3 | 6 | 3 | 2 | RxD |
| GND | 4 | 5 | 5 | 7 | GND |
| GND | 5 | 4 | 5 | 7 | GND |
| RxD | 6 | 3 | 2 | 3 | TxD |
| DSR | 7 | 2 | 6 | 8 | DTR |
| RTS | 8 | 1 | 8 | 5 | CTS |





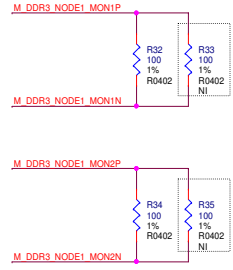
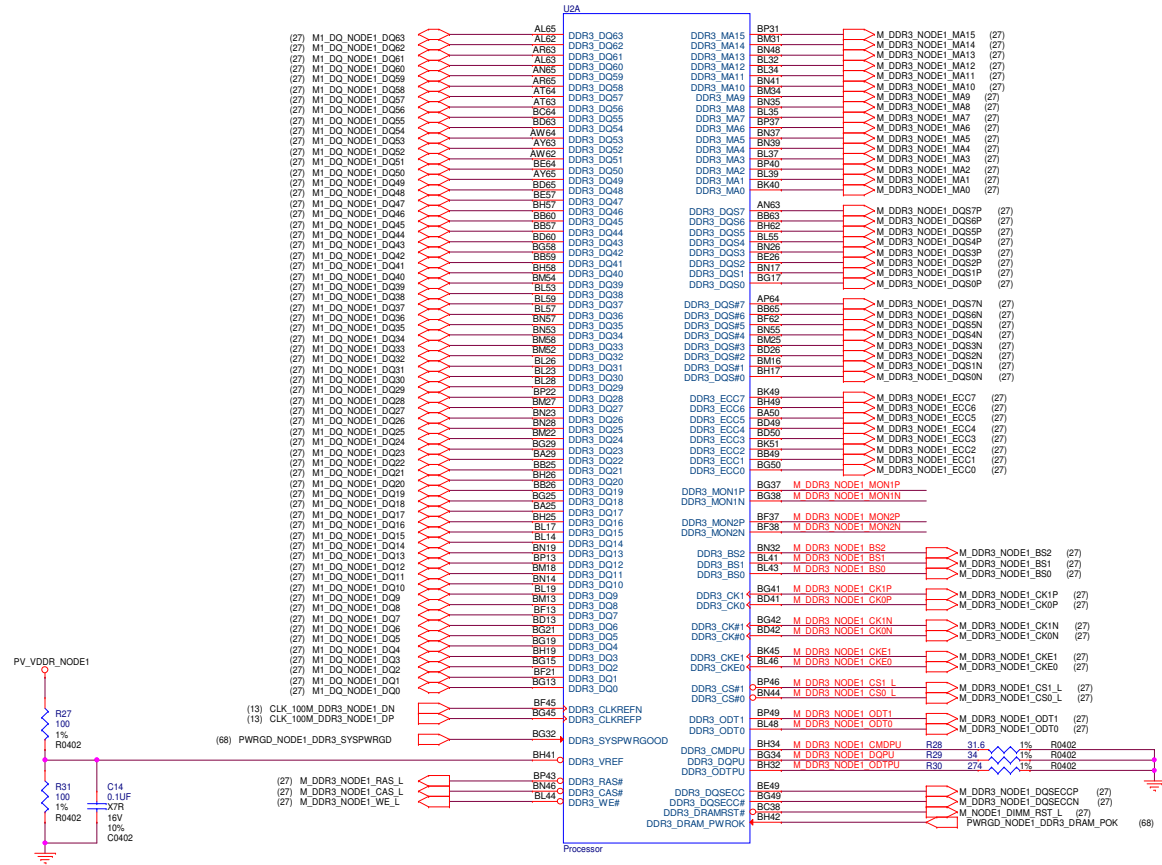
| FSLC | FSLB | CPU MHZ | SRC MHZ | PCI MHZ |
|------|------|---------|---------|---------|
| 0 | 0 | 133.33 | 100.00 | 33.33 |
| 0 | 1 | 167.67 | 100.00 | 33.33 |
| 1 | 0 | 100.00 | 100.00 | 33.33 |
| 1 | 1 | 200.00 | 100.00 | 33.33 |



Cloud Server Infrastructure Engineering

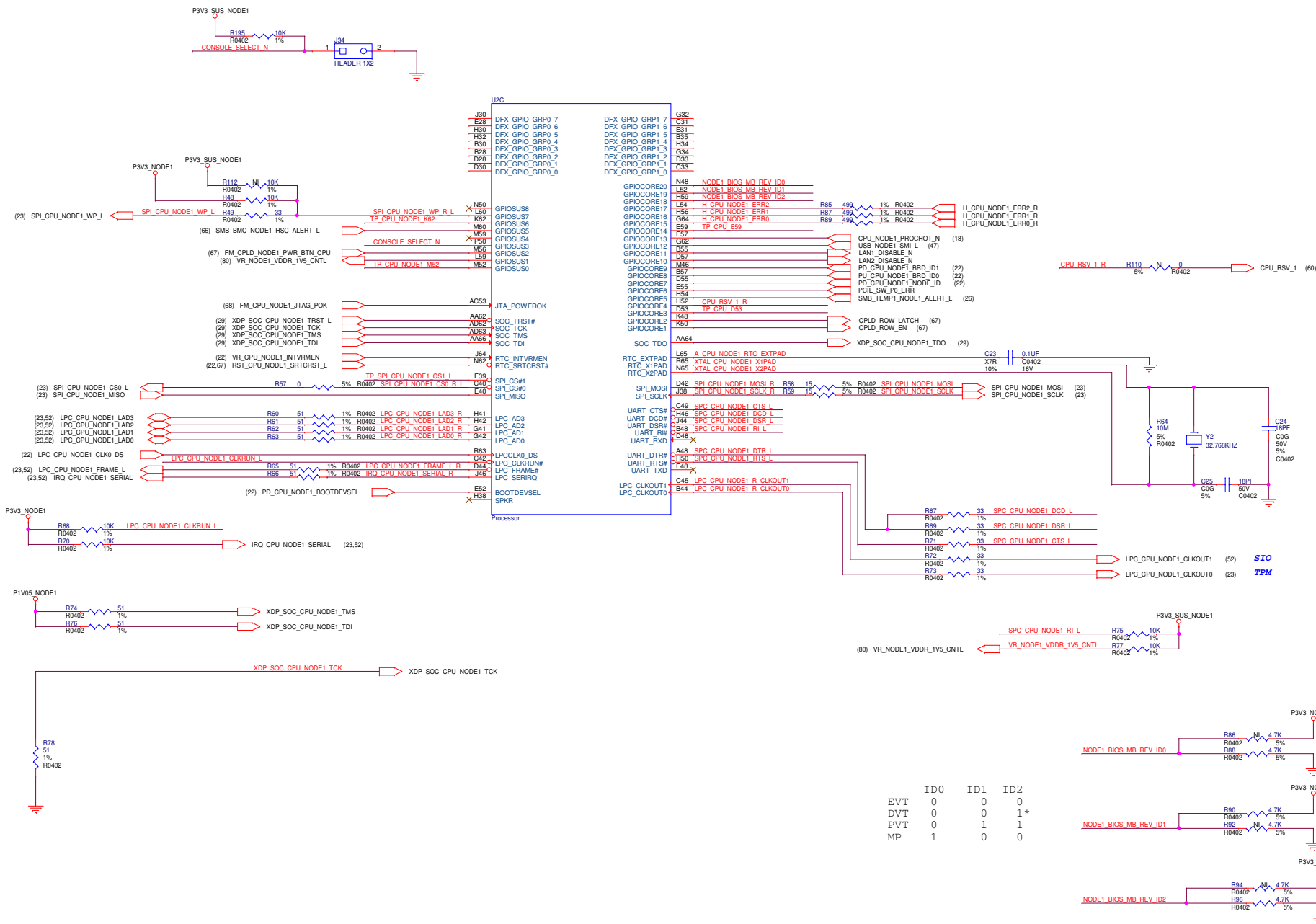
| Chassis Manager Assembly V1 | | |
|-----------------------------|-----------------|--------|
| Size | Document Number | Rev 1A |
| C | Clock Gen | |

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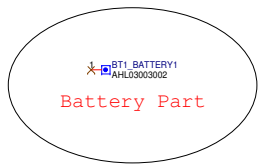
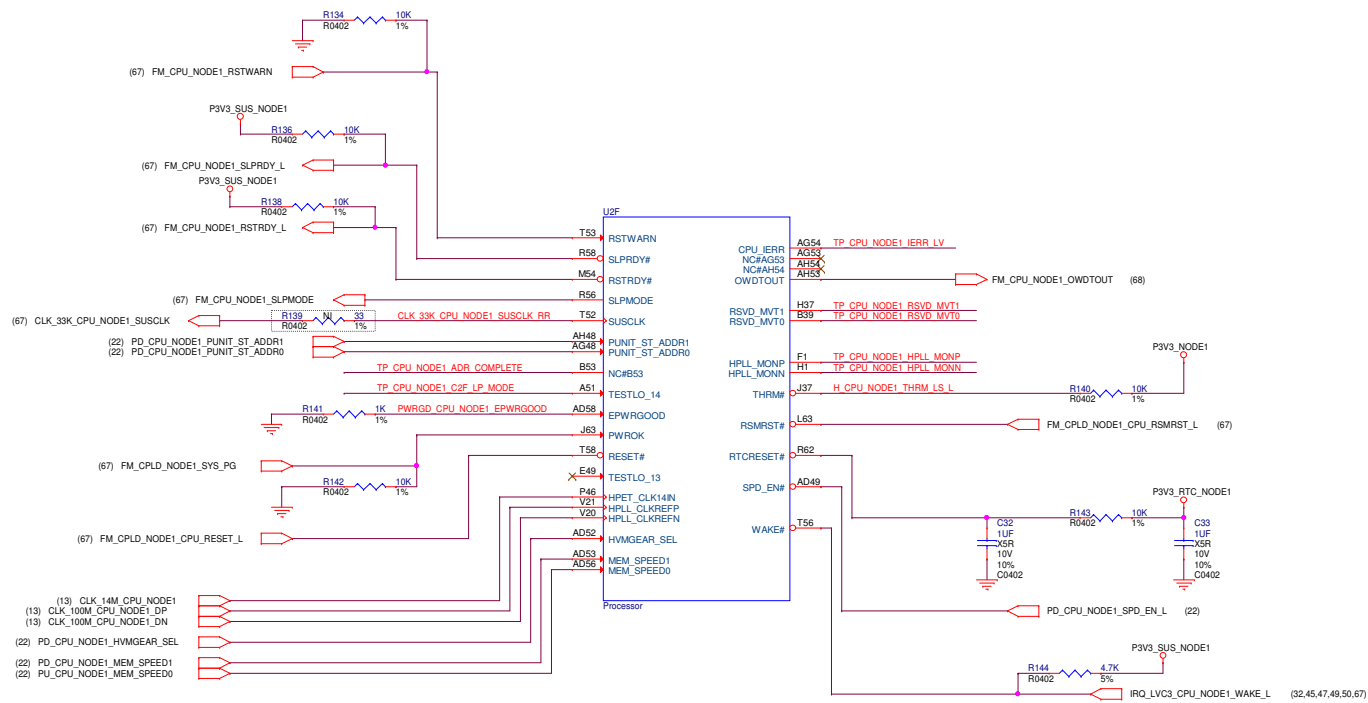
Cloud Server Infrastructure Engineering

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| Size | Document Number | Node1 CPU DDR3 Interface |
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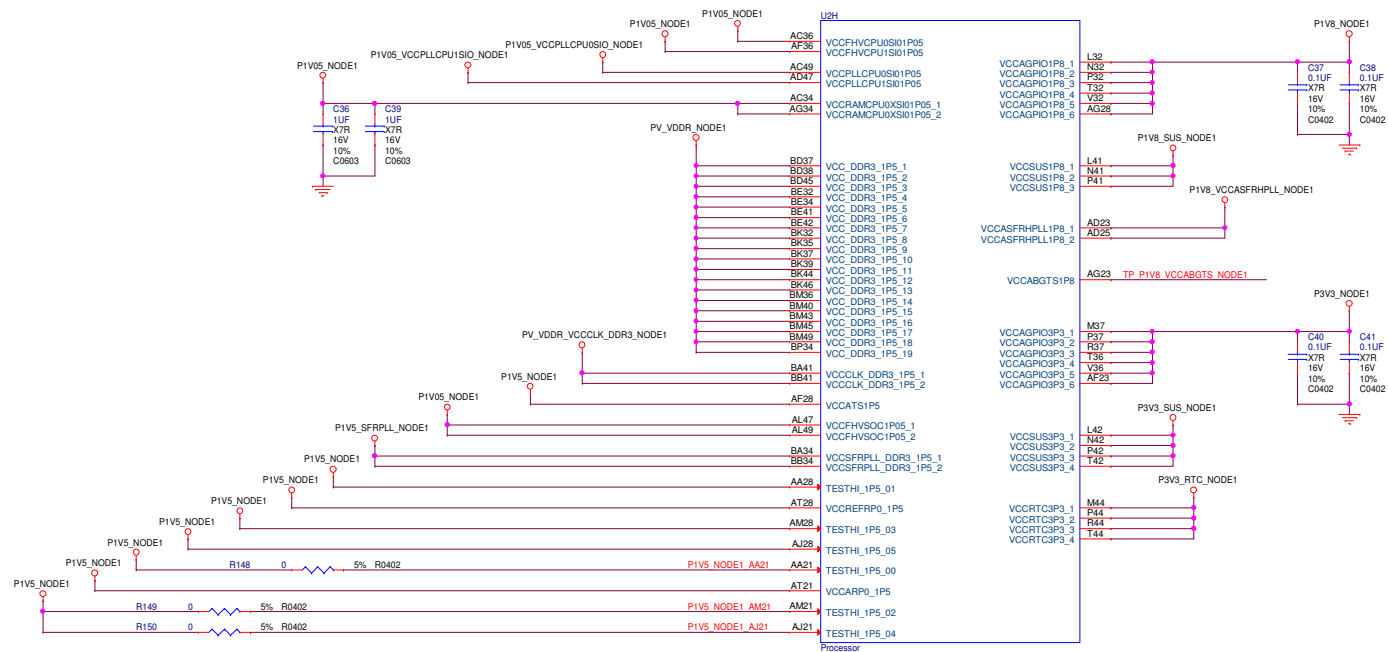
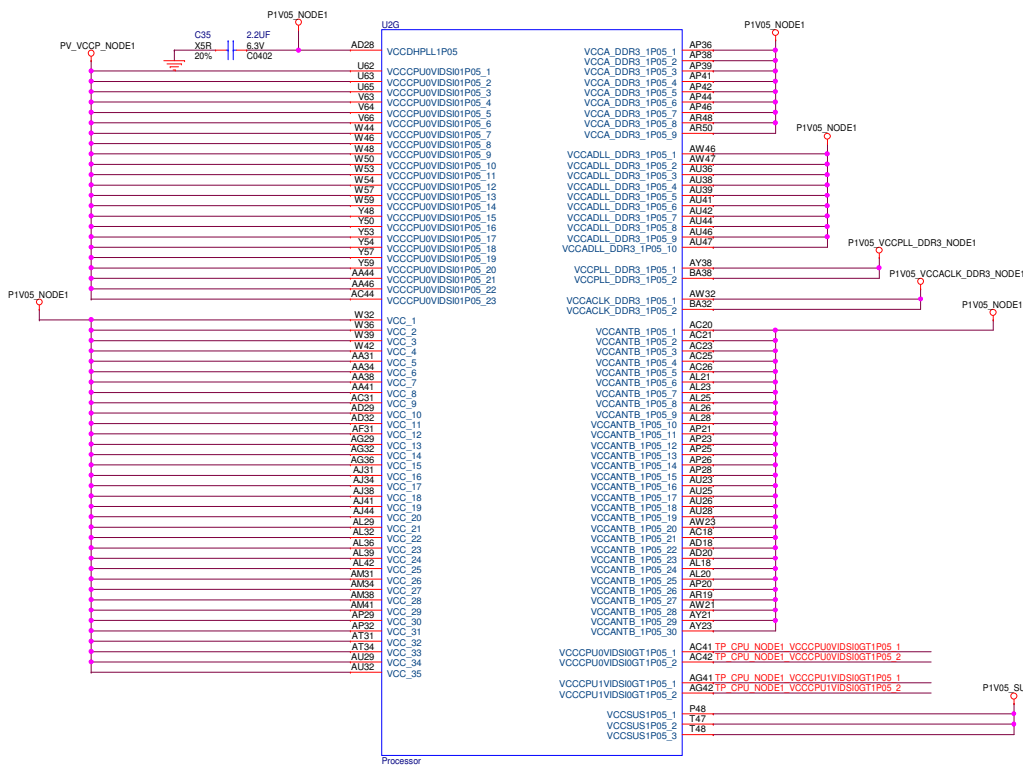


Cloud Server Infrastructure Engineering

| Chassis Manager Assembly V1 | | | Rev 1A |
|--------------------------------|-----------------|-------------------------|--------|
| Size C | Document Number | Node1 CPU GPIO LPC UART | |
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| Cloud Server Infrastructure Engineering | | | |
|-----------------------------------------|----------------------------|--------|----------|
| Chassis Manager Assembly V1 | | | |
| Size | Document Number | Rev 1A | |
| C | Node1 CPU Management Reset | | |
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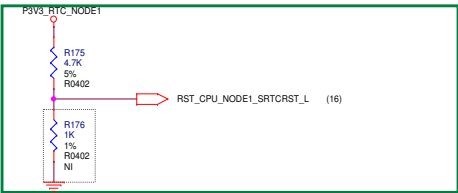
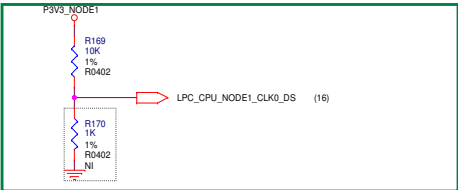
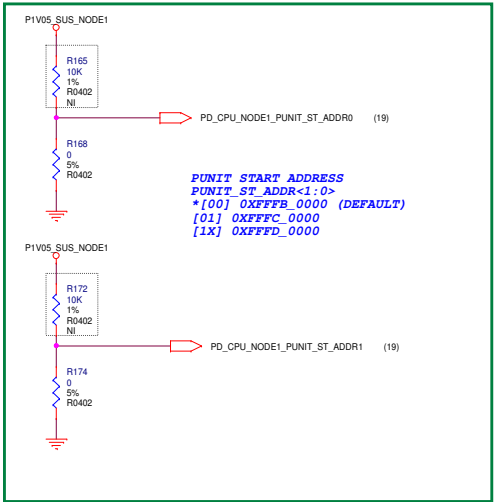
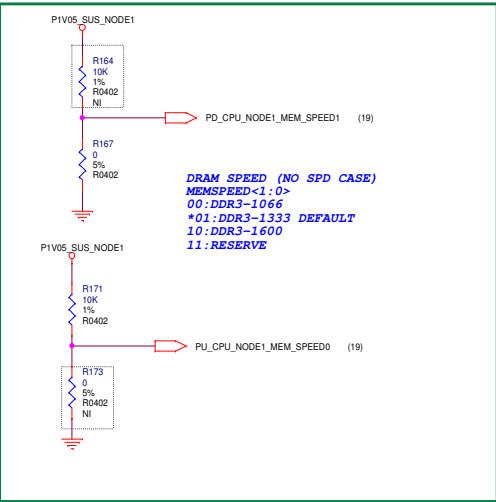
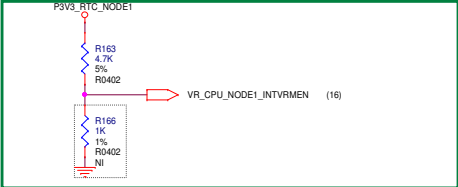
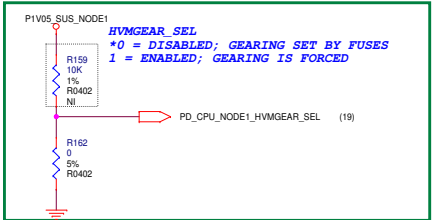
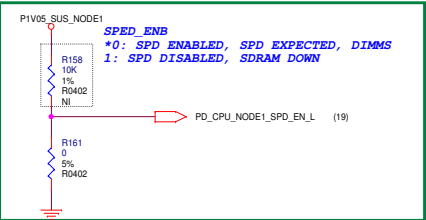
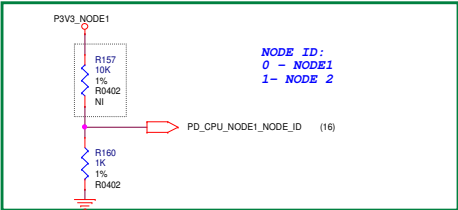
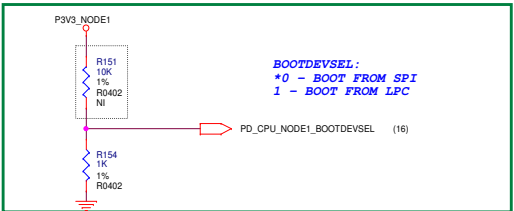
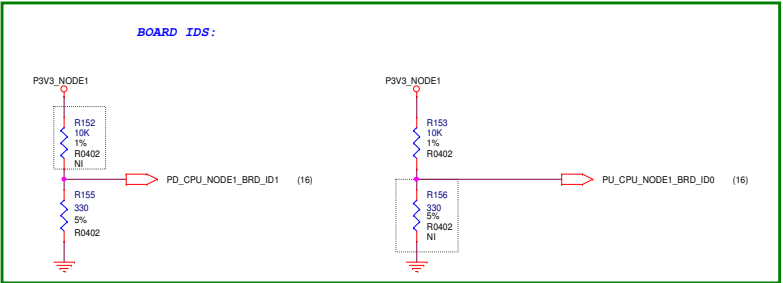
Title **Chassis Manager Assembly V1**

| | |
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| Size | Document Number |
| C | Node1 CPU Power Rails |

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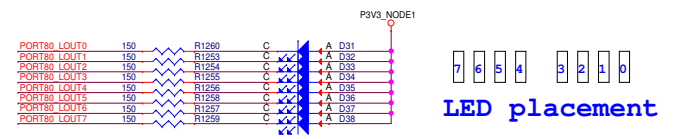
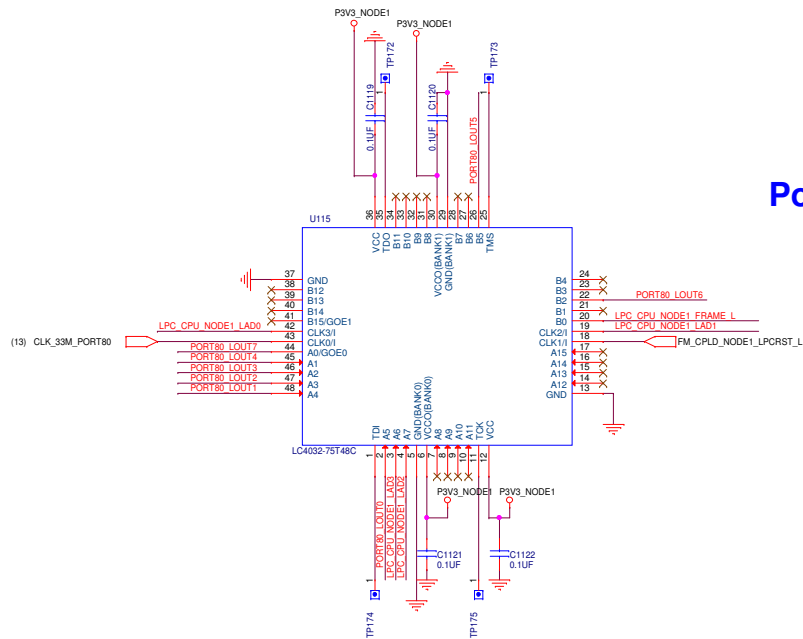
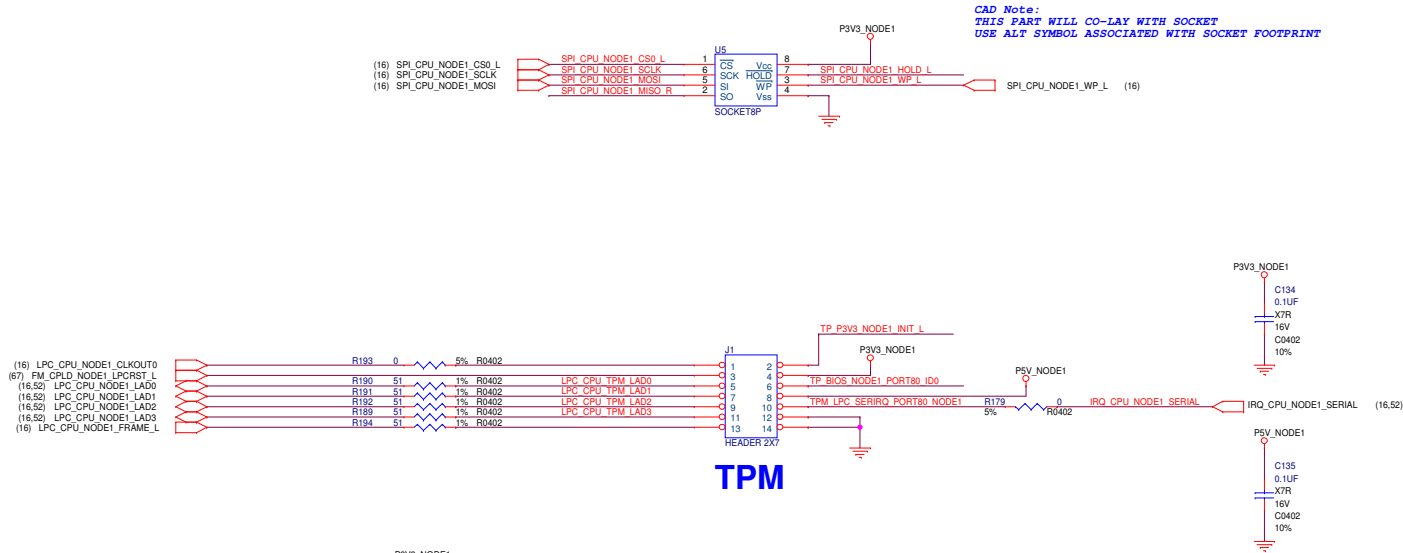
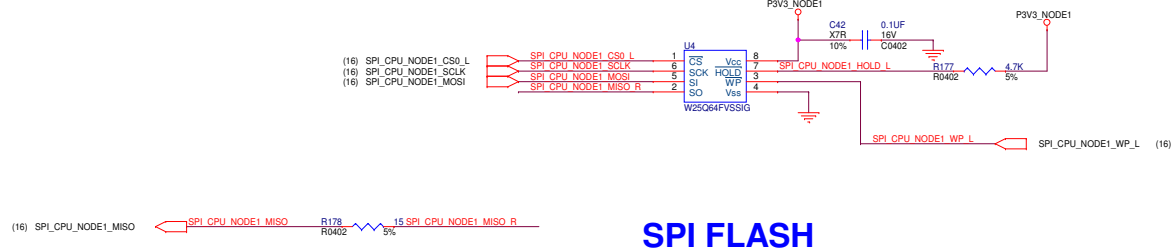
Rev
1A

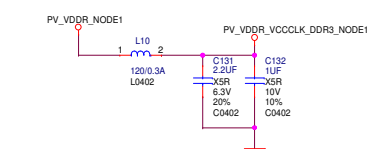
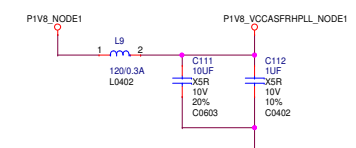
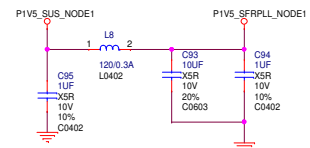
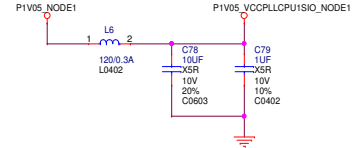
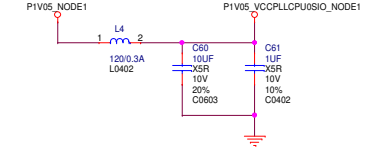
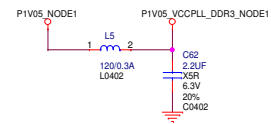
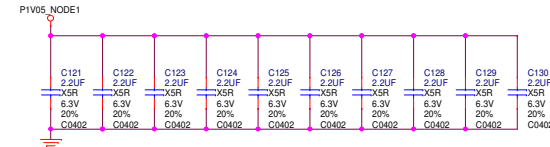
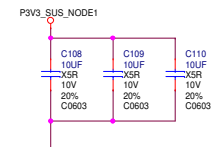
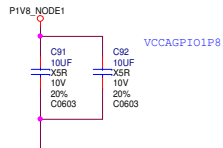
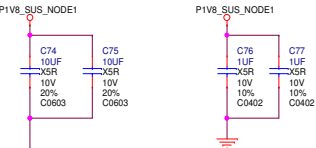
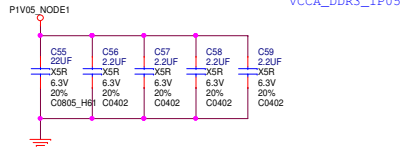
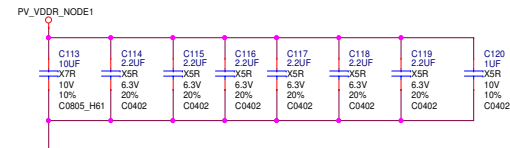
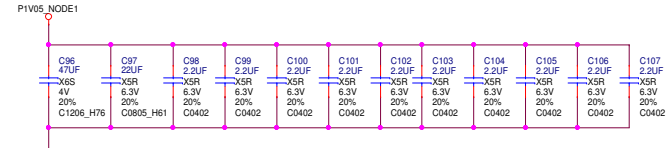
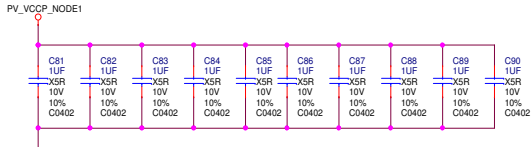
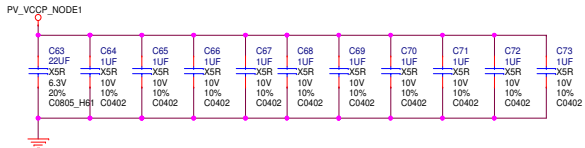
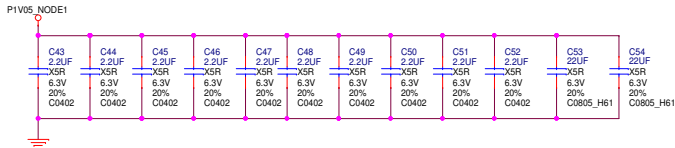




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| Chassis Manager Assembly V1 | | | Rev 1A |
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| Size C | Document Number | Node1 CPU Strapping | |
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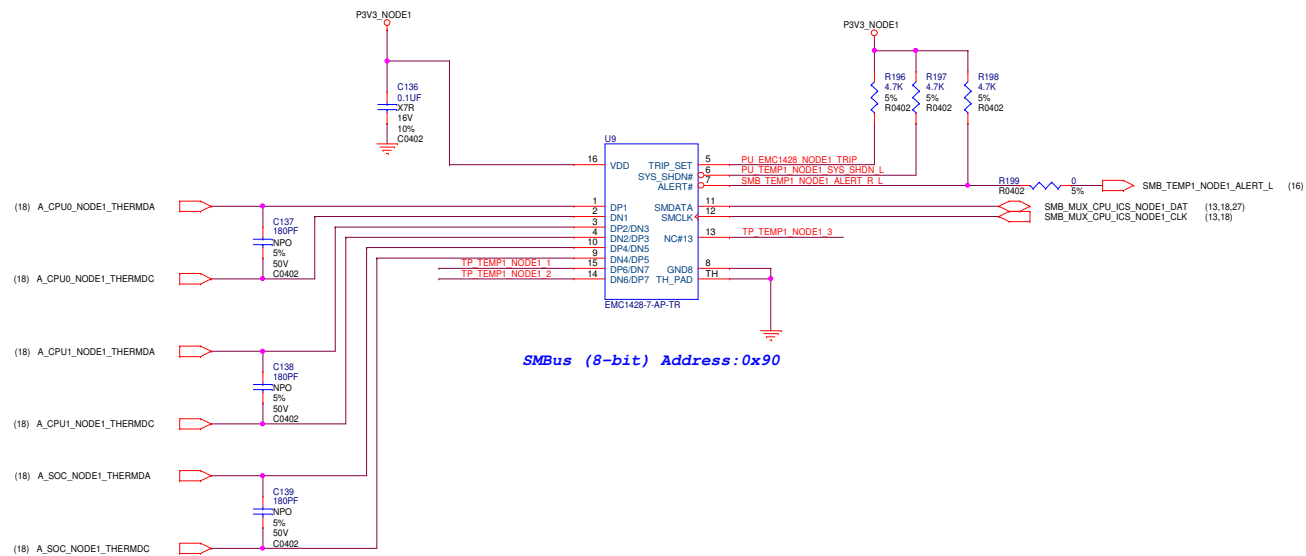
Cloud Server Infrastructure Engineering

| Chassis Manager Assembly V1 | | |
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| Size | Document Number | Rev |
| C | Node1 CPU Decoupling | 1A |
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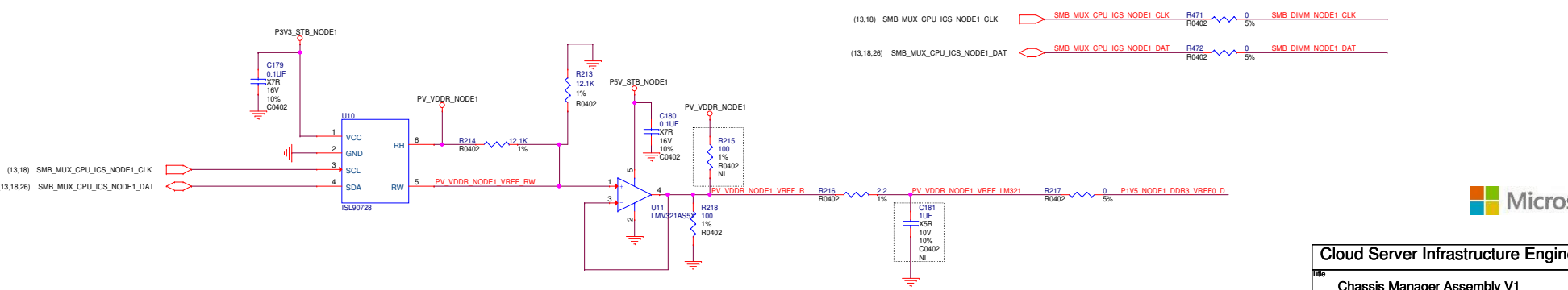
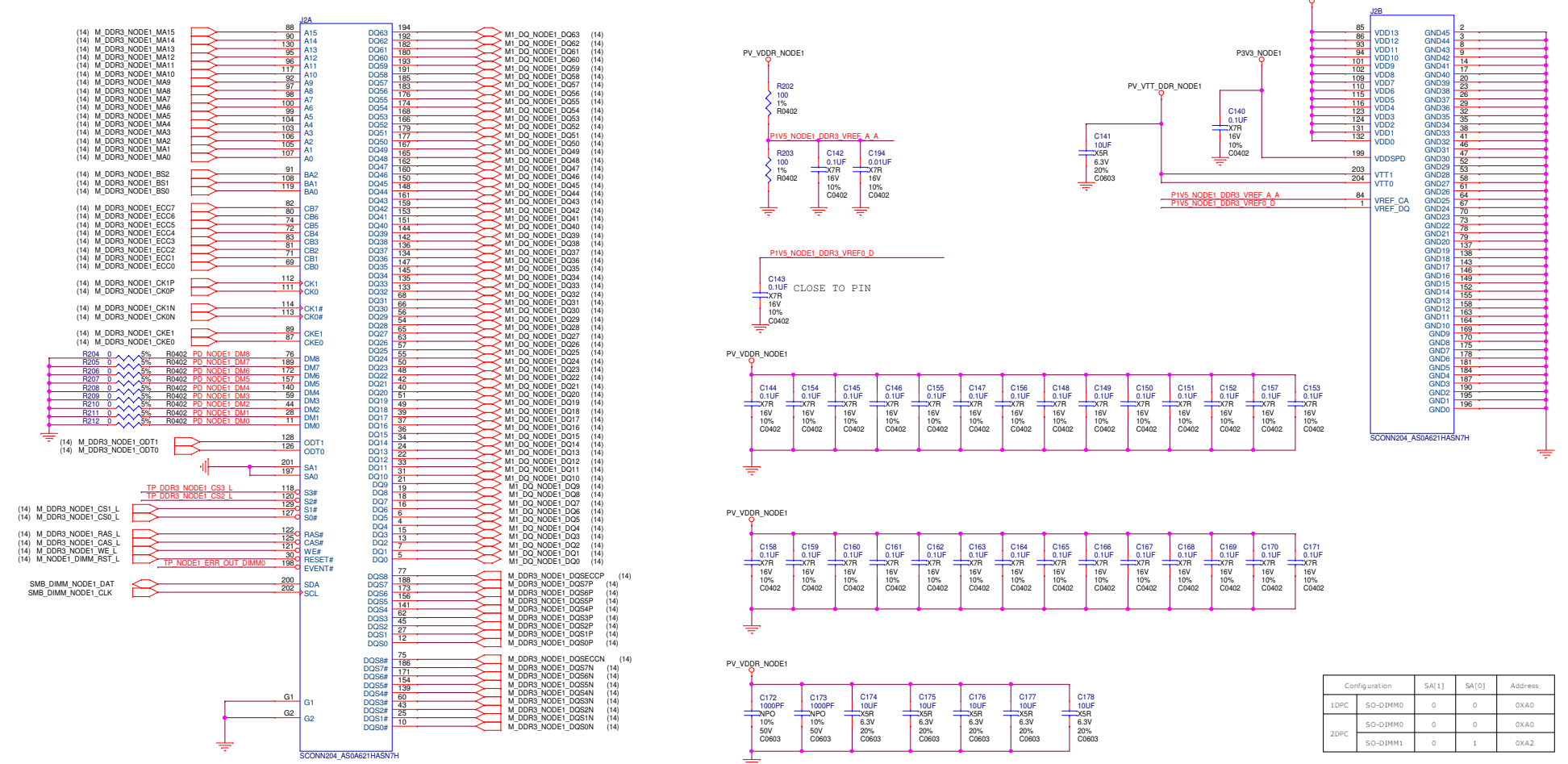


Cloud Server Infrastructure Engineering

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| Title | | Chassis Manager Assembly V1 | |
| Size | Document Number | Rev 1A | |
| C | Node1 CPU Temperature ADC | | |
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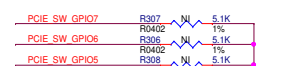
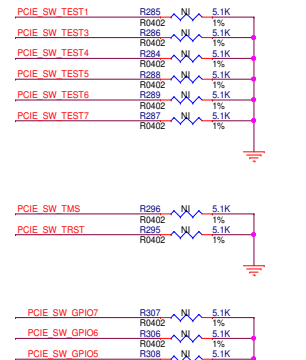
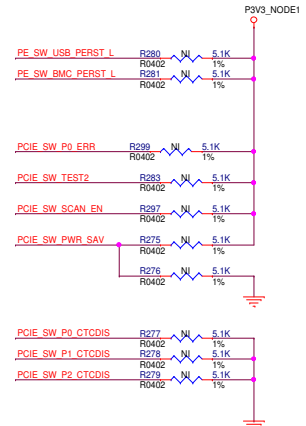
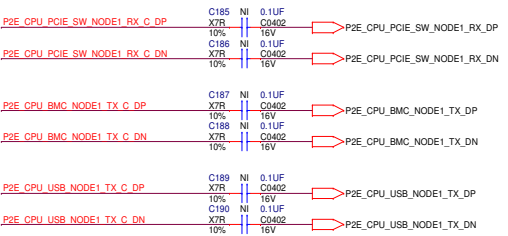
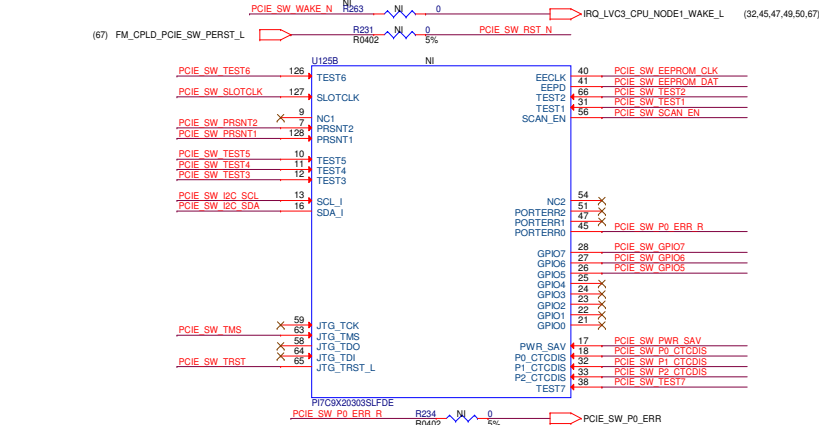
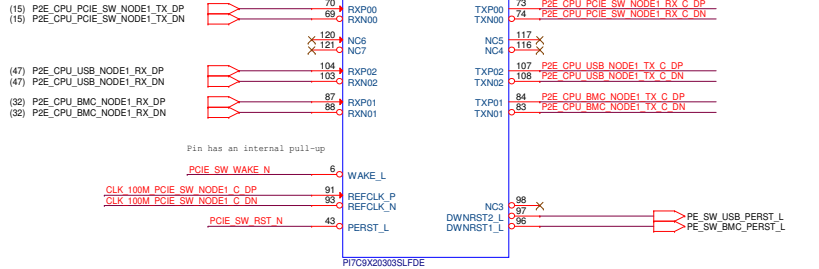
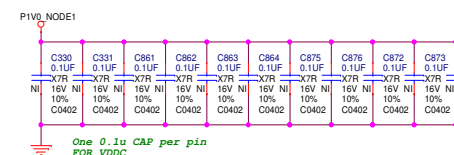
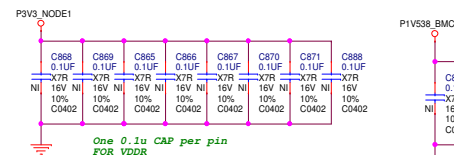
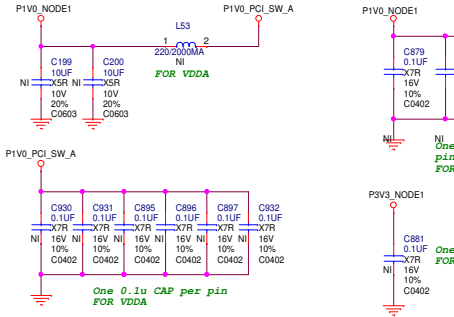
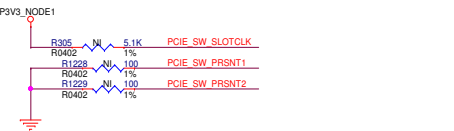
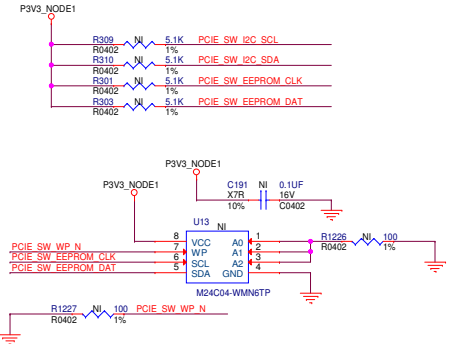
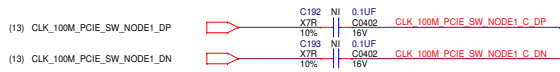
Cloud Server Infrastructure Engineering

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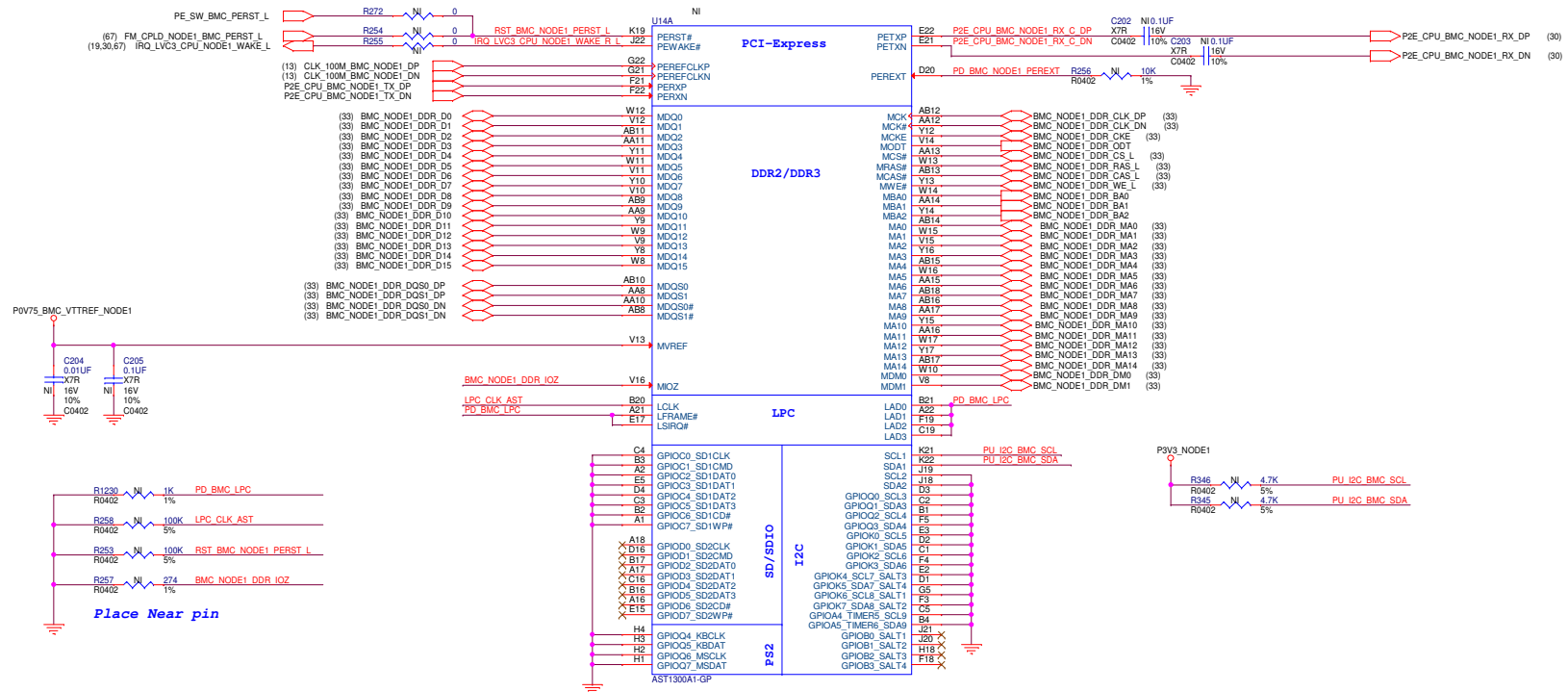
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| Size C | PCle Switch | |
| Date: Monday, January 27, 2014 | Sheet 30 | of 85 |

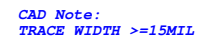
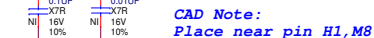
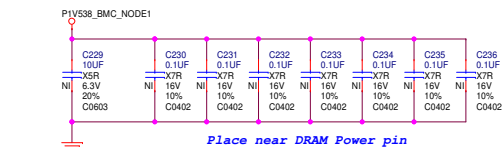


Cloud Server Infrastructure Engineering

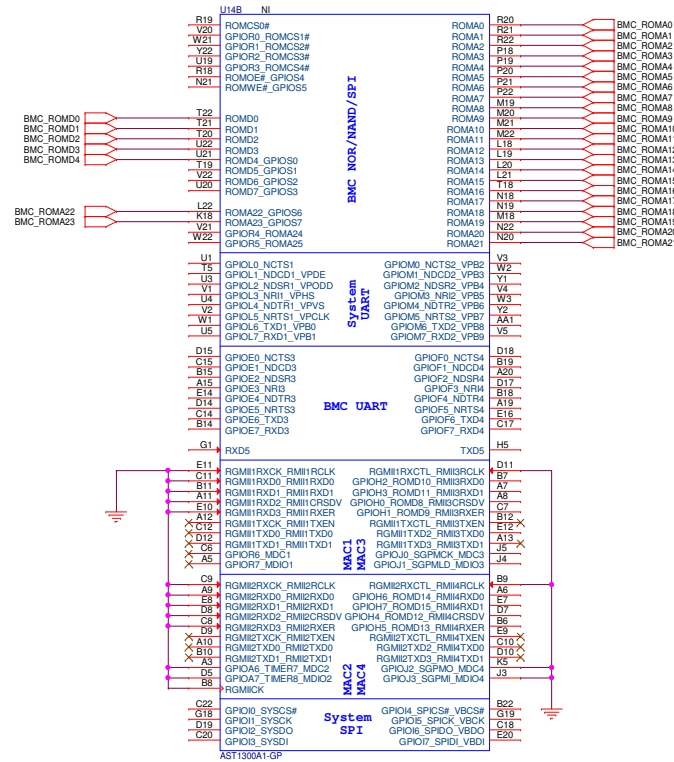
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| Title | | Chassis Manager Assembly V1 | |
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VGA OLN

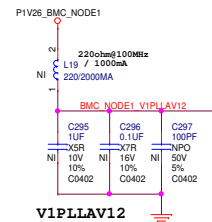
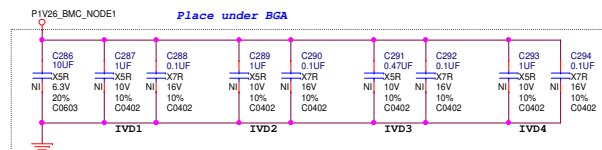
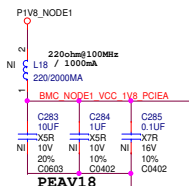
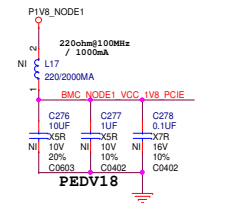
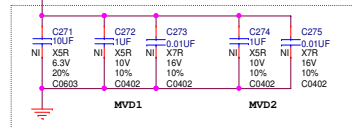
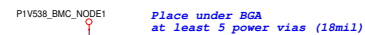
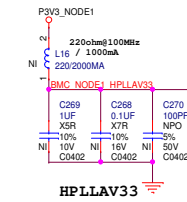
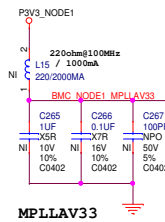
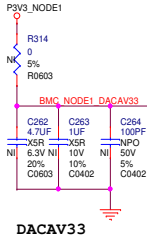
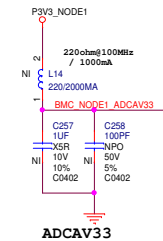
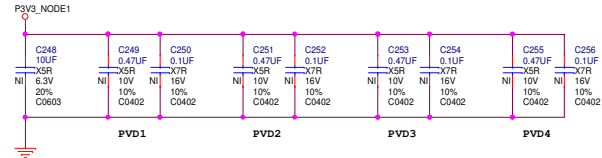
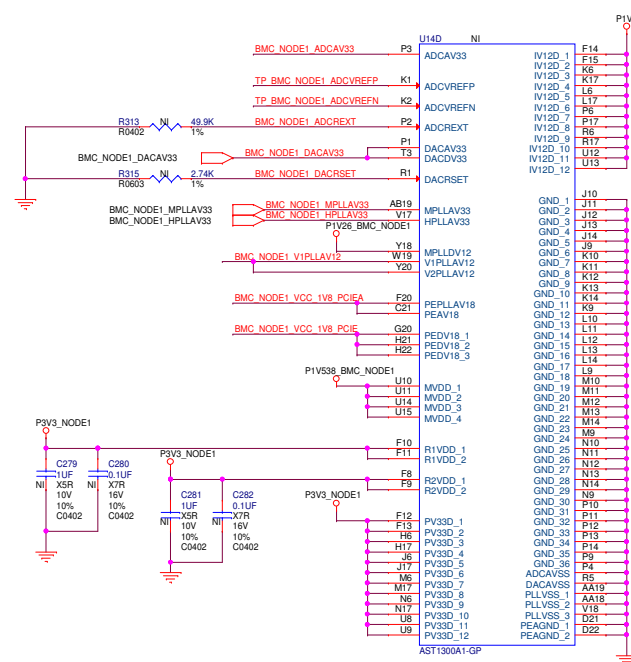


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| Chassis Manager Assembly V1 | | |
| Size | Document Number | Rev |
| C | Node1 AST1300 SPI UART MAC | 1A |
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AST1300_POWER

VGA OLNy





ROMA[1:0] : Coprocessor boot code s
 00 : Boot from NOR flash memory
 01 : Boot from NAND flash memory
 10 : Boot from SPI flash memory
 *11 : Disable CPU operation (Select)



ROMA[3:2] : VGA memory size selection
 00 : Select 8 MB VGA memory
 01 : Select 16 MB VGA memory
 10 : Select 32 MB VGA memory
 *11 : Select 64 MB VGA memory (Select)



ROMA[5] : Enable VGA BIOS ROM (depends on design)
 0 : No VGA BIOS ROM (for on-board application)
 1 : Enable VGA BIOS ROM (for add-on application)



ROMA[9:8] : H-PLL default clock frequency selection
 00 : Select 384 MHz
 01 : Select 360 MHz
 10 : Select 336 MHz (Select)
 11 : Select 408 MHz



ROMA[11:10] : CPU/AHB clock frequency ratio selection
 00 : Select CPU:AHB = 1:1
 01 : Select CPU:AHB = 2:1
 10 : Select CPU:AHB = 4:1 (Select)
 11 : Select CPU:AHB = 3:1



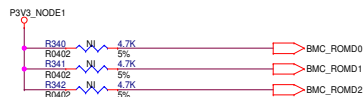
ROMA[15] : VGA Class Code selection
 0 : Select the Class Code for video device
 1 : Select the Class Code for VGA device (Select)



ROMA[19] : Disable MSI controller
 0 : Enable
 1 : Disable (Select)



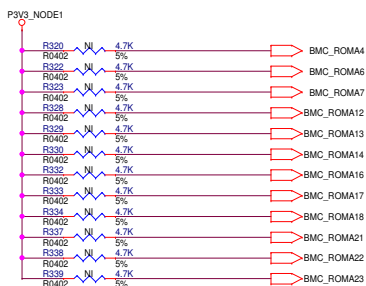
ROMA[20] : Disable LPC to decode SuperIO 0x2E/0x4E address
 0 : Enable address decoding
 1 : Disable address decoding (Select)



ROMD[2:0] : DRAM configuration setting
 000: DDR3 SDRAM with CL = 5, CWL = 5
 010: DDR3 SDRAM with CL = 6, CWL = 5 (Select)
 100: DDR3 SDRAM with CL = 7, CWL = 6
 110: DDR3 SDRAM with CL = 8, CWL = 6
 001: DDR2 SDRAM with CL = 4
 011: DDR2 SDRAM with CL = 5
 101: DDR2 SDRAM with CL = 6
 111: DDR2 SDRAM with CL = 7
 The DRAM configuration setting is defined for compliant VGA BIOS/Driver and BMC firmware default supported DRAM timing. The trapping setting must meet the DRAM speed bin used to get correct DRAM timing in initialization.



ROMD[4:3] : DRAM size setting
 00: 64 MBytes
 01: 128 MBytes (Select)
 10: 256 MBytes
 11: 512 MBytes

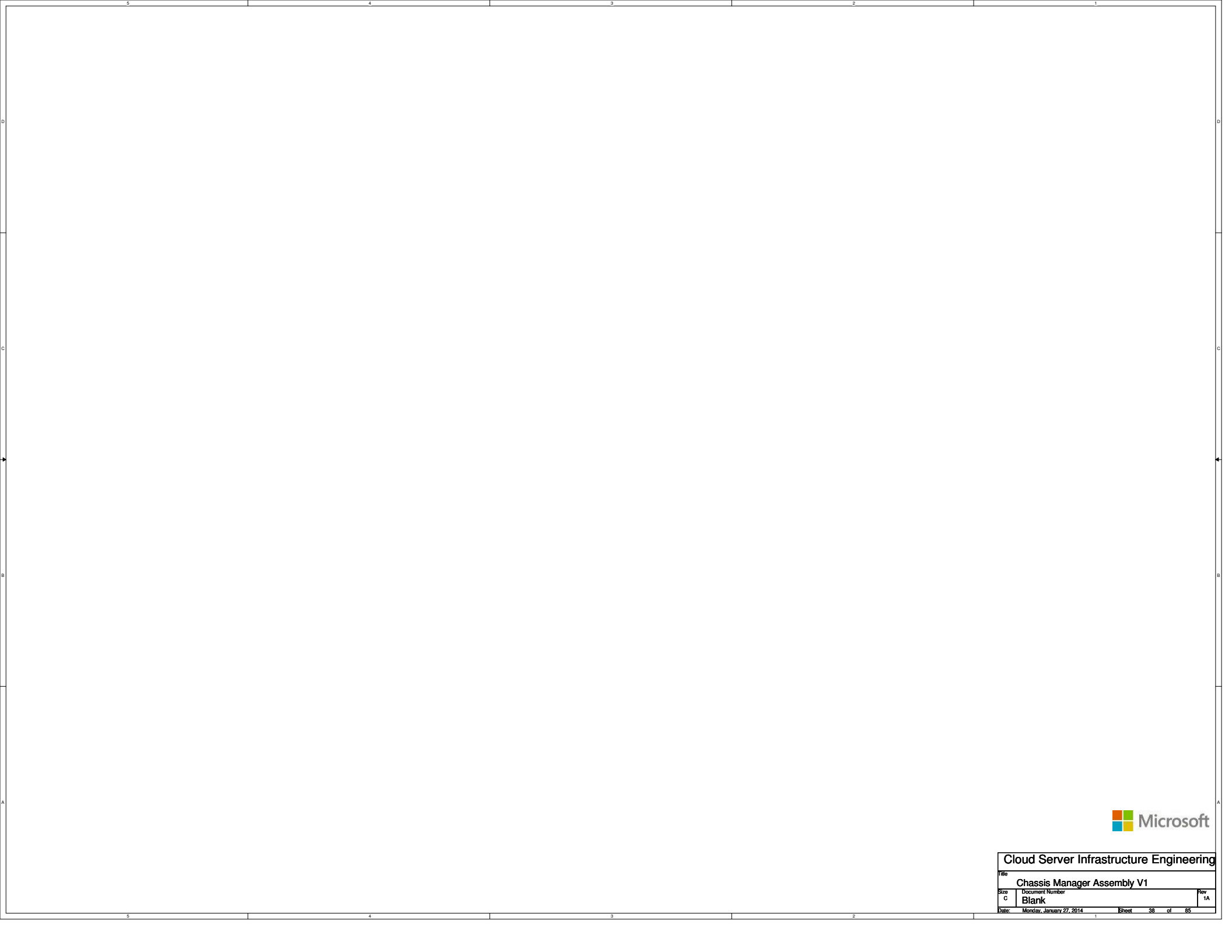


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Cloud Server Infrastructure Engineering

| Title | | |
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| Chassis Manager Assembly V1 | | |
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| C | Node1 AST1300 HW Strapping | 1A |
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Title
Chassis Manager Assembly V1

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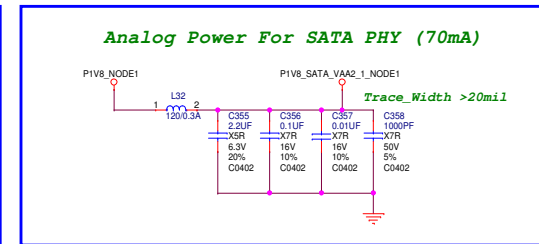
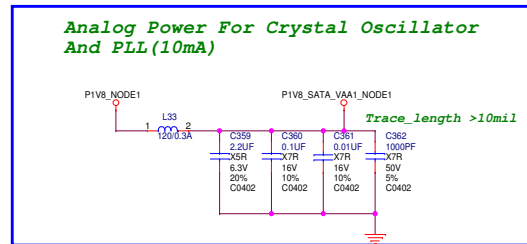
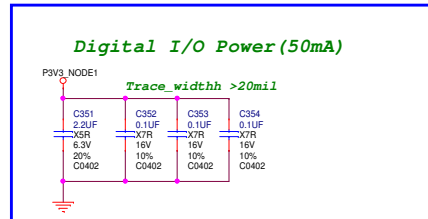
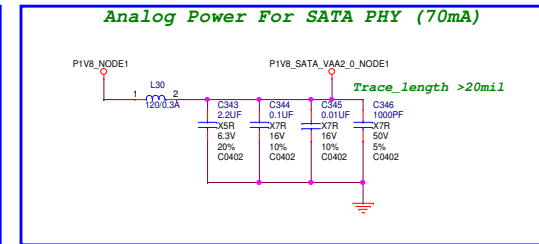
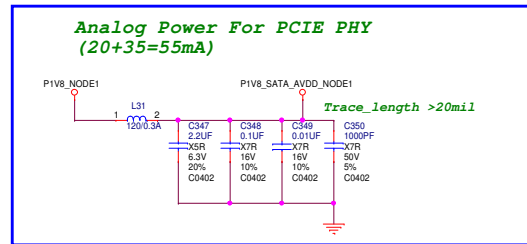
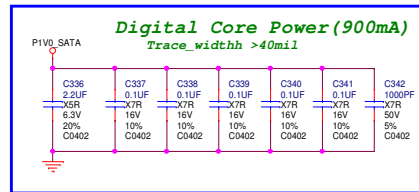
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| Title | | Chassis Manager Assembly V1 | |
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5.2 Recommended Operating Conditions

Table 5-2 defines the recommended operating conditions for the 88SE9130.
Table 5-2 Recommended Operating Conditions*

| Parameter | Symbol | Min | Typ | Max | Units |
|-----------------------------------------------------|----------------------|-------|------|------|-------|
| Analog Power for PCIe Phy Transmitter | AVDDT _{op} | 1.71 | 1.8 | 1.98 | V |
| Analog Power for PCIe Phy | AVDD _{op} | 1.71 | 1.8 | 1.98 | V |
| Analog Power for Crystal Oscillator and PLL | VAA1 _{op} | 1.71 | 1.8 | 1.98 | V |
| Analog Power for SATA Phy | VAA2_0 _{op} | 1.71 | 1.8 | 1.98 | V |
| Analog Power for SATA Phy | VAA2_1 _{op} | 1.71 | 1.8 | 1.98 | V |
| Digital Core Power | VDD _{op} | 0.98 | 1.0 | 1.10 | V |
| Digital I/O Power | VDDIO _{op} | 3.135 | 3.3 | 3.63 | V |
| Internal Bias Reference | ISET _{op} | 5.98 | 6.04 | 6.10 | KΩ |
| Ambient Operating Temperature, Advanced Commercial | | 0 | | 85 | °C |
| Ambient Operating Temperature, Industrial† | | -40 | | 85 | °C |
| Junction Operating Temperature, Advanced Commercial | | 0 | | 125 | °C |
| Junction Operating Temperature, Industrial† | | -20 | | 125 | °C |

* Estimated values are provided until characterization is complete.
† Engineering samples only. Estimated value provided until characterization is complete. Marvell does not have automotive or military qualification for industrial temperature versions of 88SE9130.



88SE9130 One-Lane PCI Express 2.0 to 3 or 6 Gbps SATA I/O Controller Preliminary Datasheet

5.3 Power Requirements

Table 5-3 defines the power requirements for the 88SE9130.
Table 5-3 Power Requirements*

| Parameter | Symbol | Min | Typ | Max | Units |
|---------------------------------------------|---------------------|-----|-----|-----|-------|
| Analog Power for PCIe Phy Transmitter | I _{AVDDT} | | | 20 | mA |
| Analog Power for PCIe Phy | I _{AVDD} | | | 35 | mA |
| Analog Power for Crystal Oscillator and PLL | I _{VAA1} | | | 10 | mA |
| Analog Power for SATA Phy | I _{VAA2_0} | | | 70 | mA |
| Analog Power for SATA Phy | I _{VAA2_1} | | | 70 | mA |
| Digital Core Power | I _{VDD} | | | 800 | mA |
| Digital I/O Power (3.3V)† | I _{VDDIO} | | | 50 | mA |

* Estimated values are provided until characterization is complete.
† The digital I/O power supply can be either 3.3V or 1.8V.

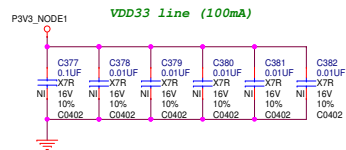
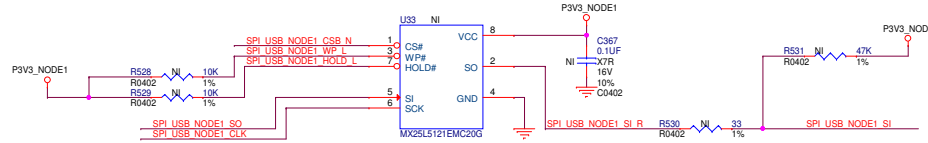
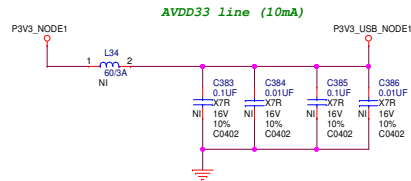
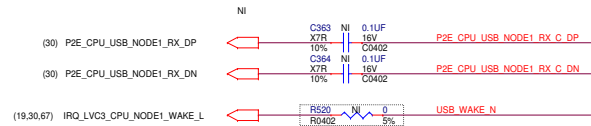
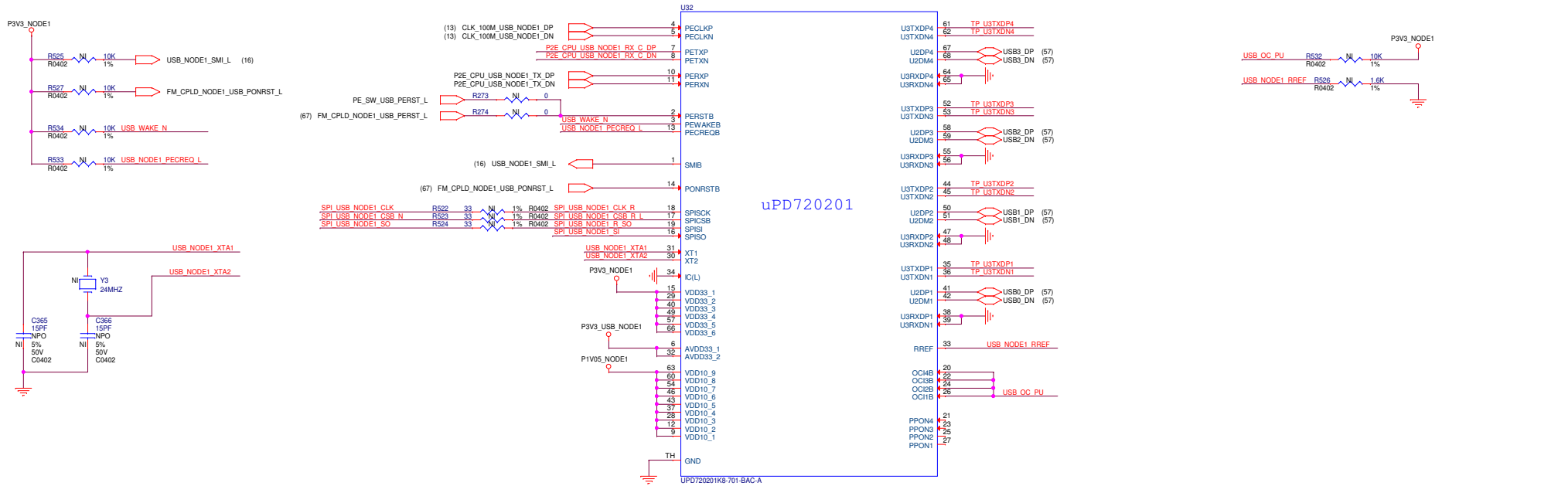
1.8V: 205mA
1.0V: 900mA
3.3V: 500mA

uter Inc * UNDER NDA# 12122816



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| C | Node1 HDD Controller 2 | | | | |
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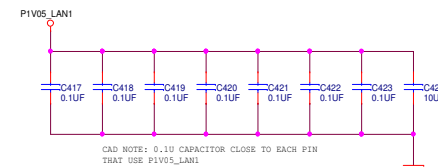
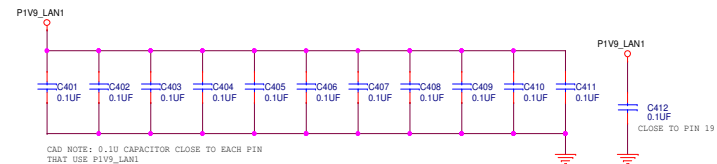
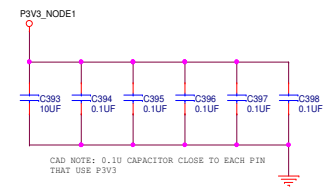
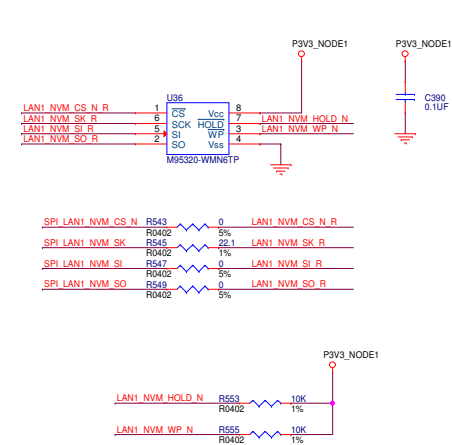
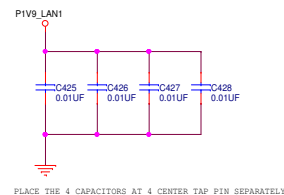
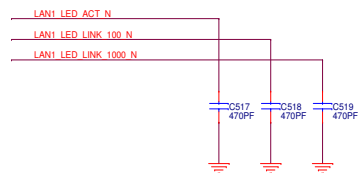
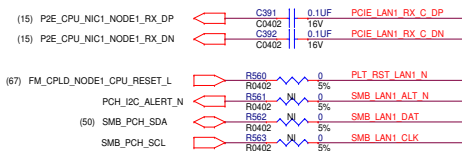
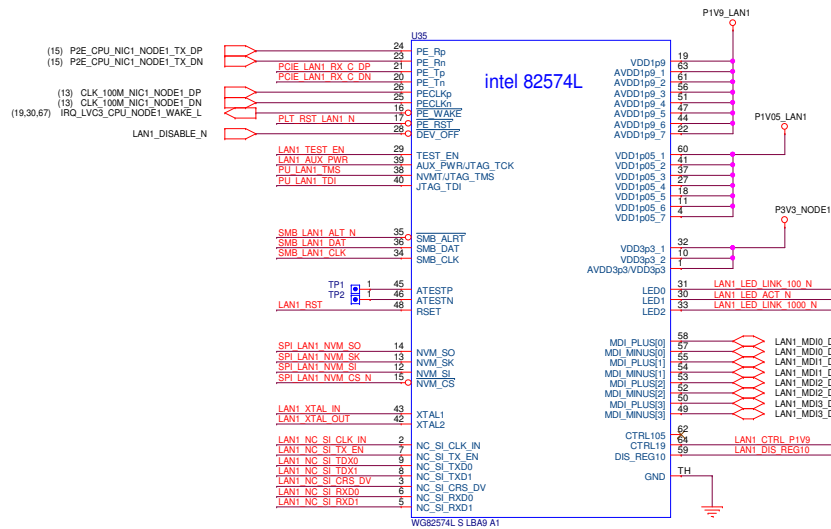
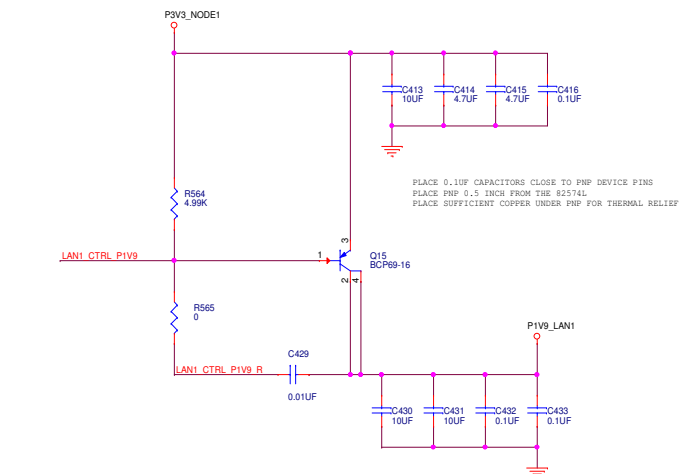


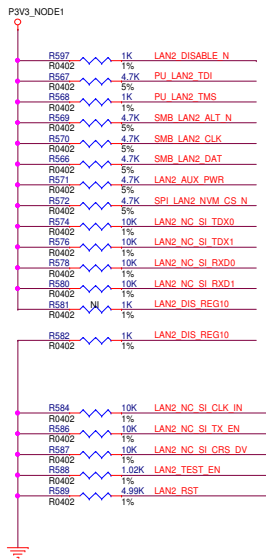
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| Chassis Manager Assembly V1 | | |
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| Size | Document Number | Rev 1A |
| C | Node1 USB Controller | |
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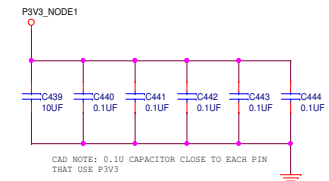
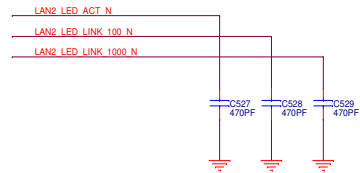
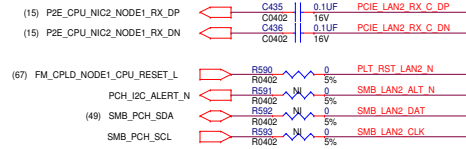
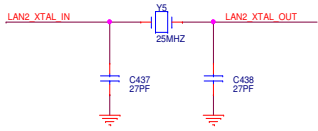
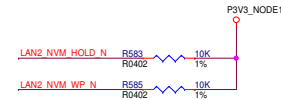
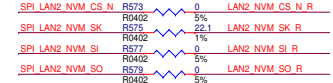
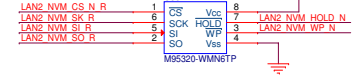
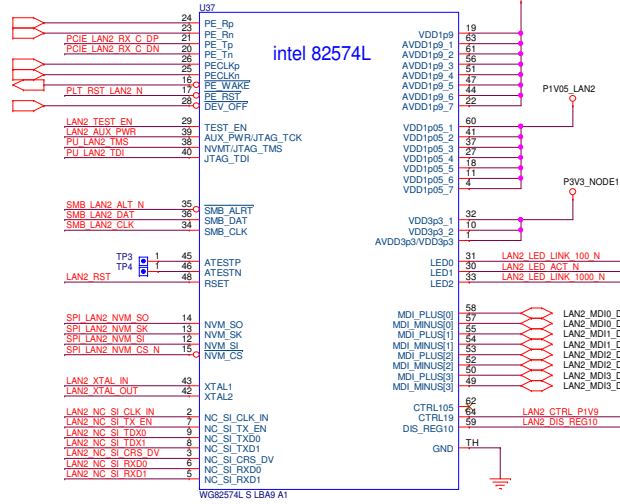
| Cloud Server Infrastructure Engineering | | | |
|-----------------------------------------|--------------------------|-----------------------------|----------|
| Title | | Chassis Manager Assembly V1 | |
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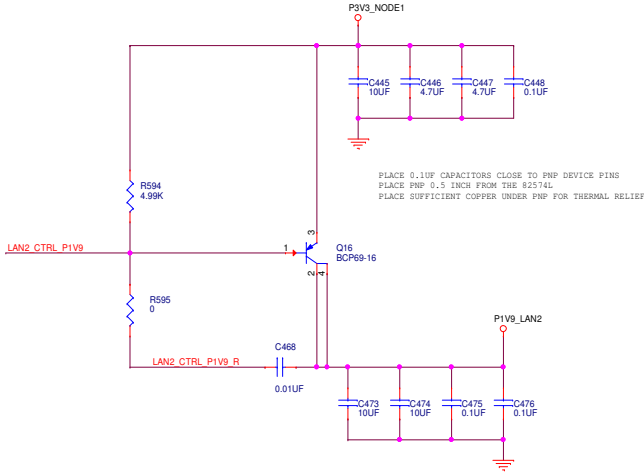


(15) P2E_CPU_NIC2_NODE1_TX_DP
(15) P2E_CPU_NIC2_NODE1_TX_DN
(13) CLK_100M_NIC2_NODE1_DP
(13) CLK_100M_NIC2_NODE1_DN
(19,30,67) IRQ_LVC3_CPU_NODE1_WAKE_L

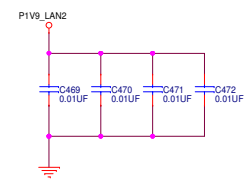
LAN2_DISABLE_N



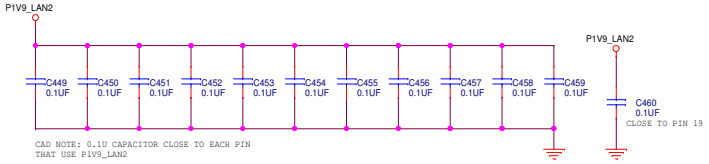
CAD NOTE: 0.1U CAPACITOR CLOSE TO EACH PIN THAT USE P3V3



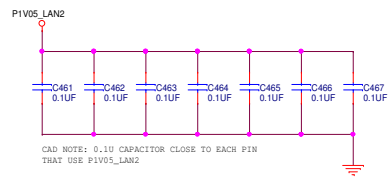
PLACE 0.1UF CAPACITORS CLOSE TO PNP DEVICE PINS
PLACE PNP 0.5 INCH FROM THE 82574L
PLACE SUFFICIENT COPPER UNDER PNP FOR THERMAL RELIEF



PLACE THE 4 CAPACITORS AT 4 CENTER TAP PIN SEPARATELY



CAD NOTE: 0.1U CAPACITOR CLOSE TO EACH PIN THAT USE P1V9_LAN2



CAD NOTE: 0.1U CAPACITOR CLOSE TO EACH PIN THAT USE P1V05_LAN2



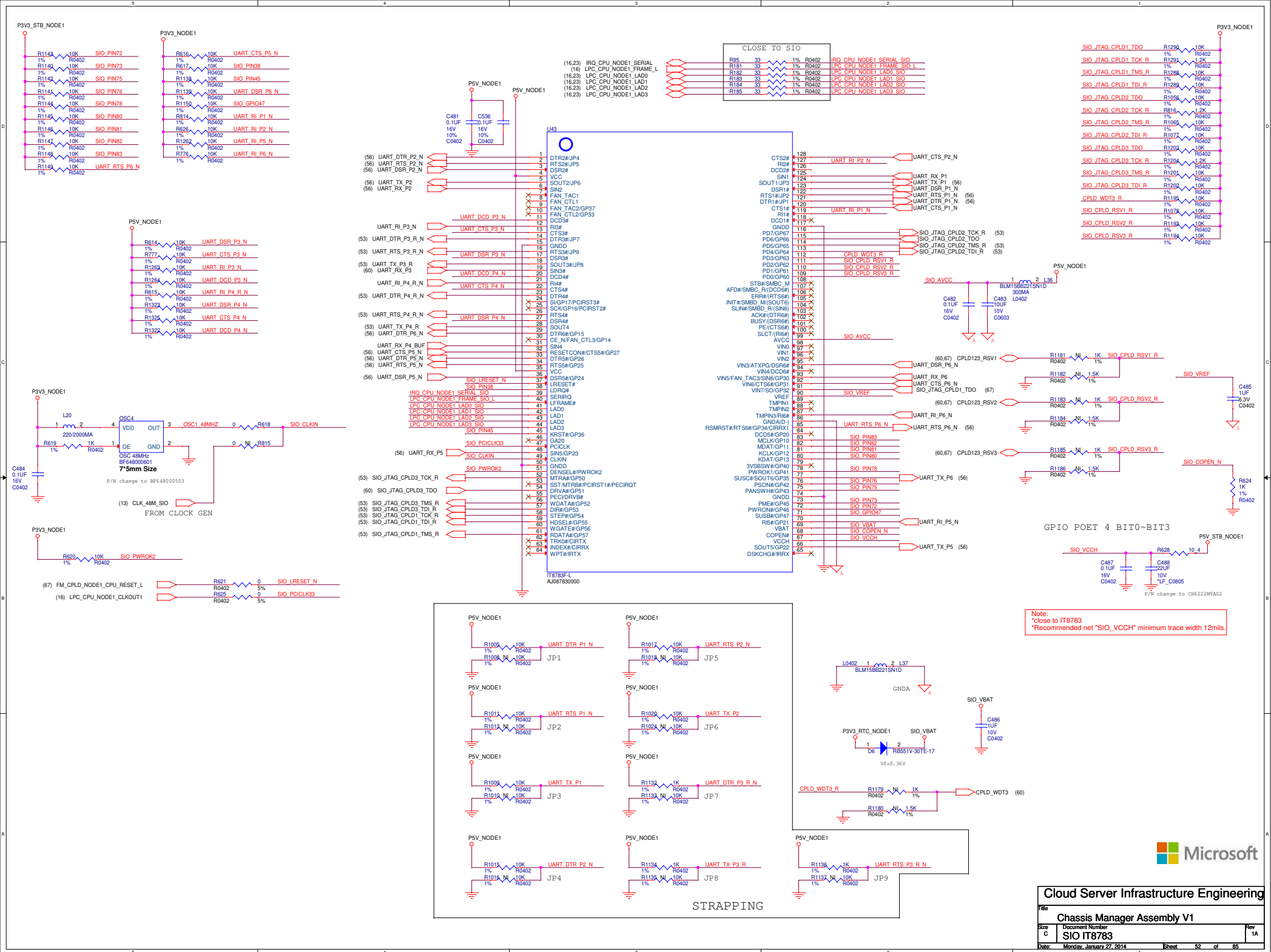
Cloud Server Infrastructure Engineering

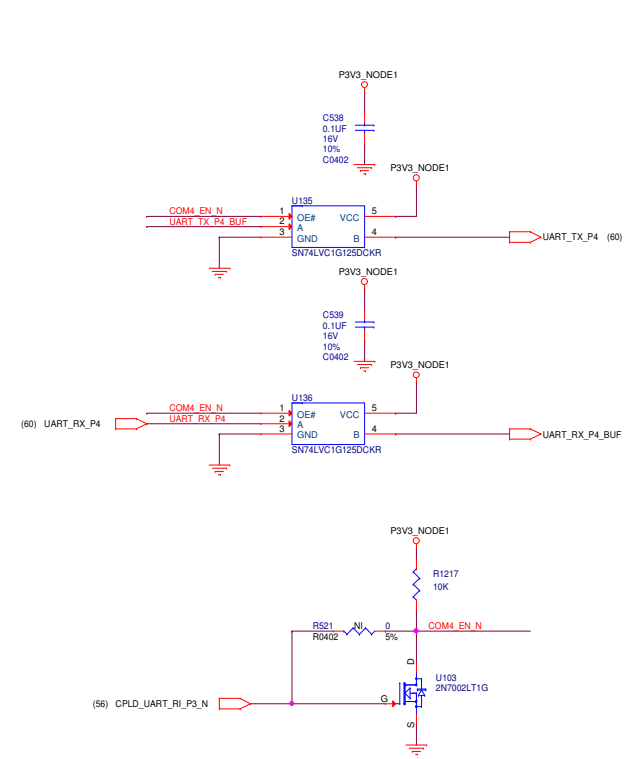
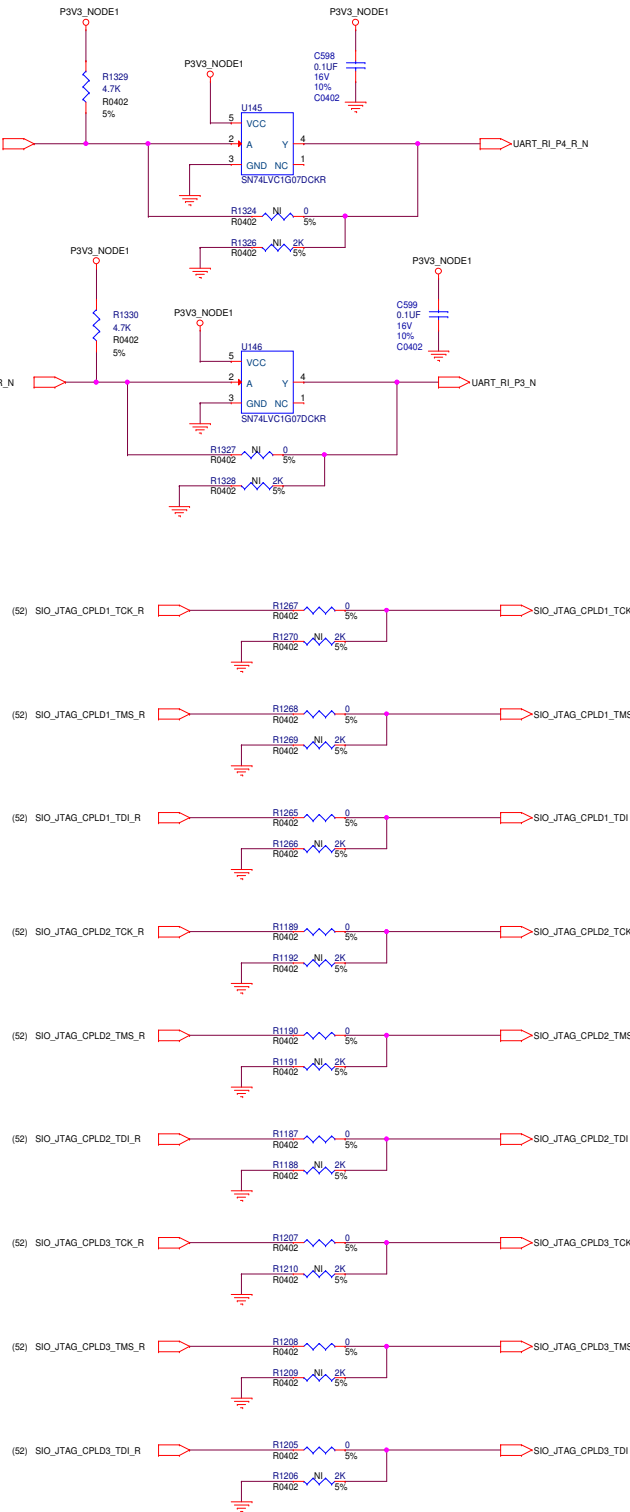
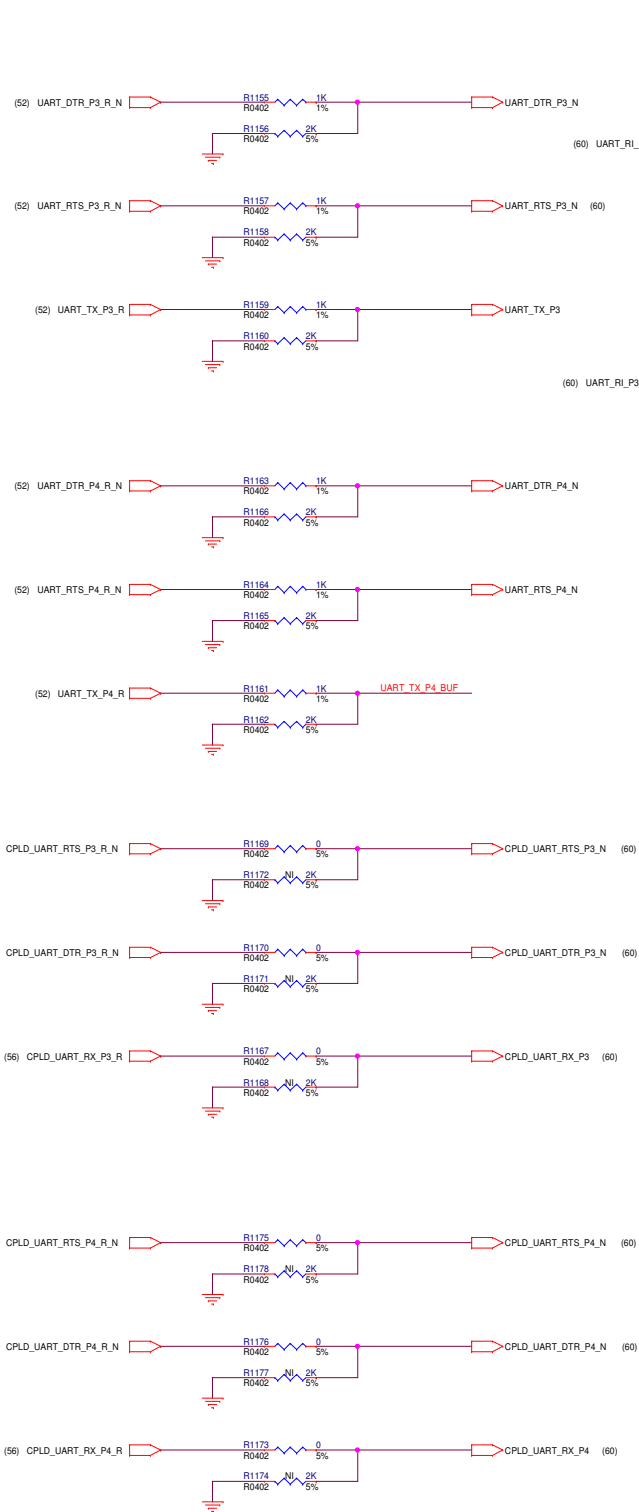
| Chassis Manager Assembly V1 | | | |
|-----------------------------|--------------------------------|--------|----------|
| File | Document Number | Rev 1A | |
| Size | Node1 82574 LAN 2 | | |
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| | | | |
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| Title | | Chassis Manager Assembly V1 | |
| Size | Document Number | Rev | |
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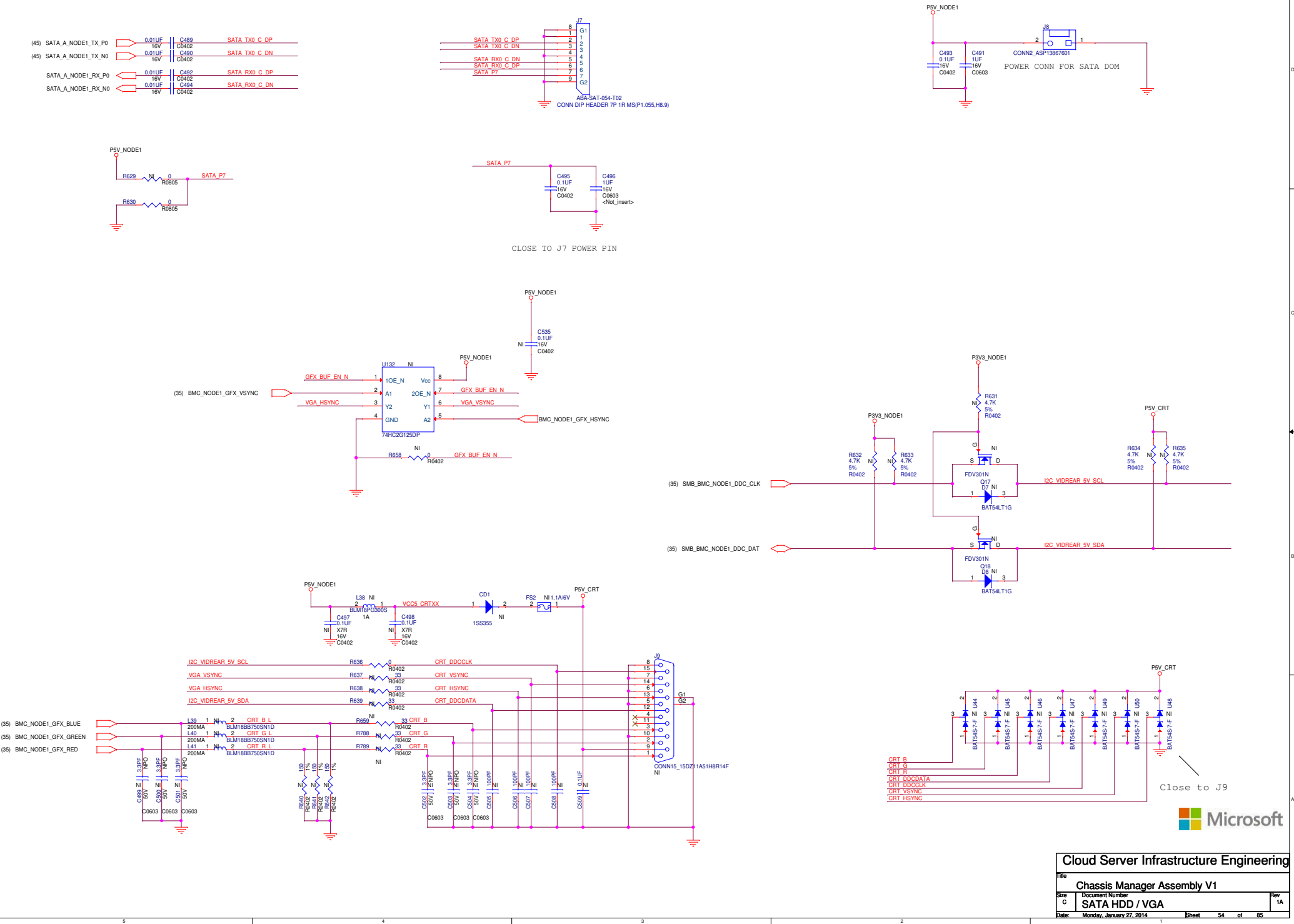


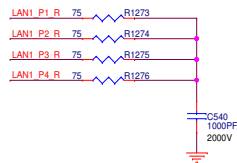
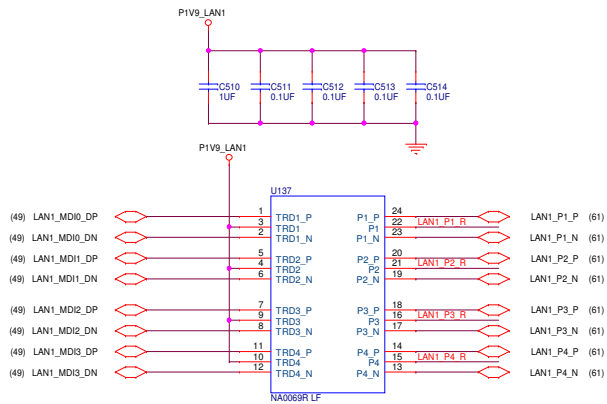


Cloud Server Infrastructure Engineering

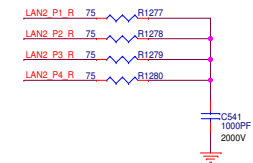
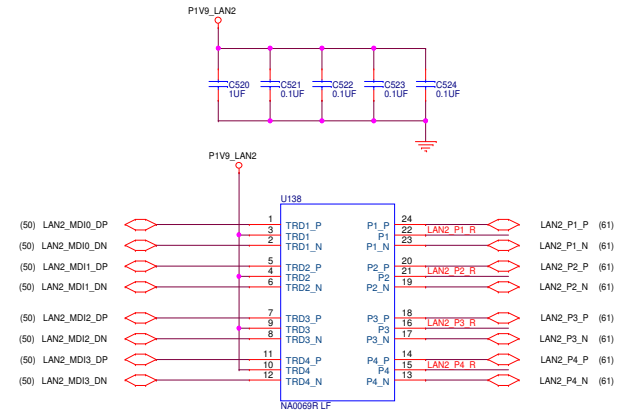
| Chassis Manager Assembly V1 | | |
|-----------------------------|--------------------------|----------------|
| Size | Document Number | Rev |
| C | Divider | 1A |
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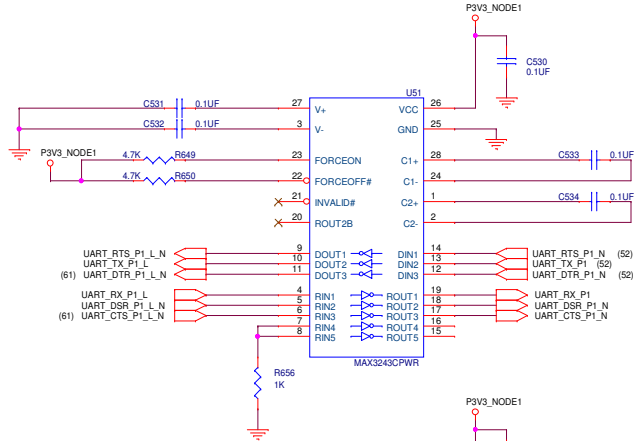
SATA DOM



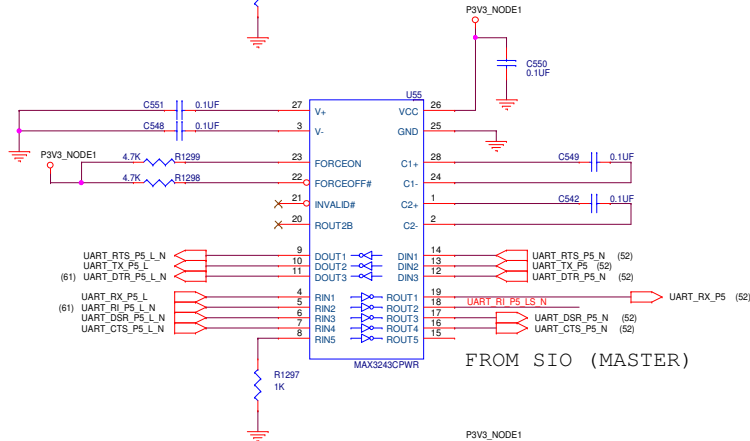


check pin define

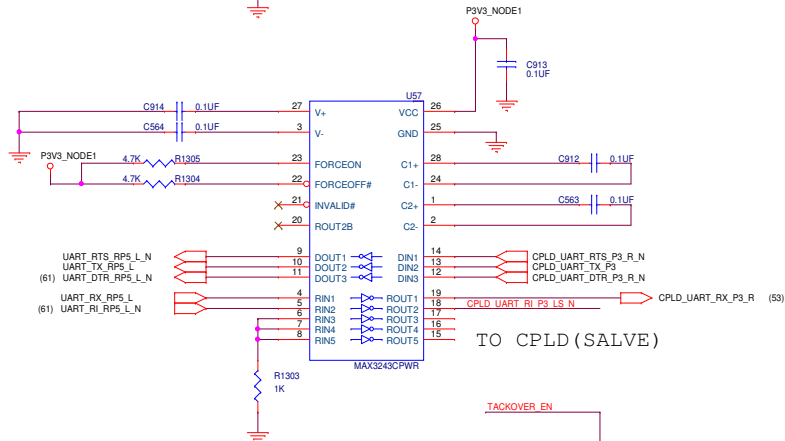




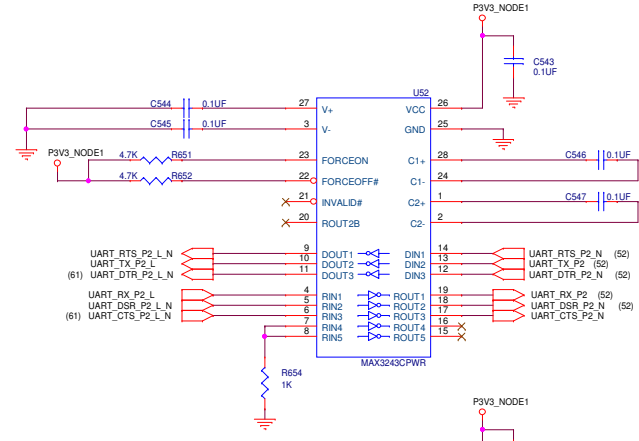
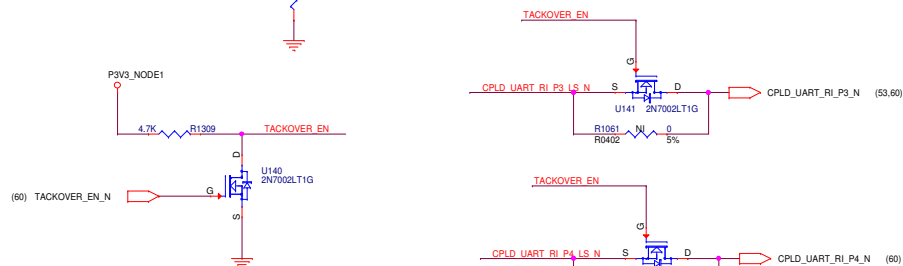
FROM SIO (MASTER)



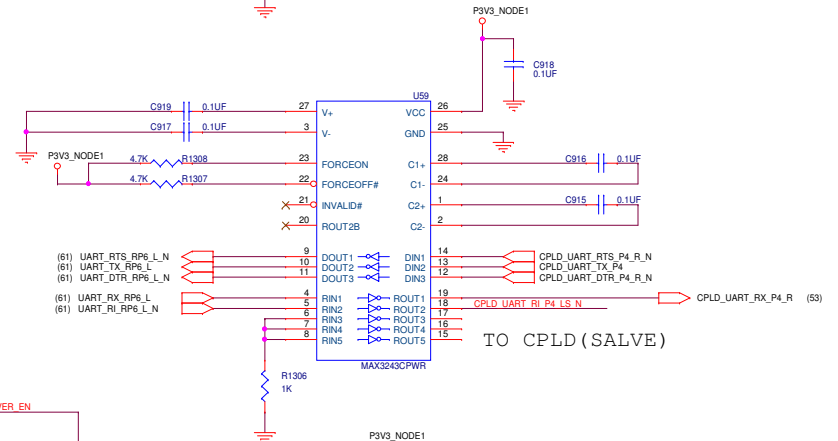
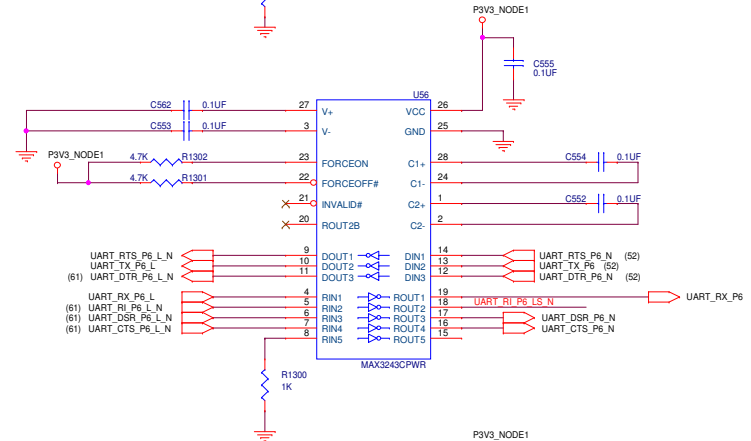
FROM SIO (MASTER)



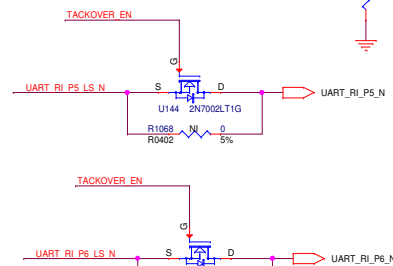
TO CPLD (SLAVE)



FROM SIO (MASTER)



TO CPLD (SLAVE)



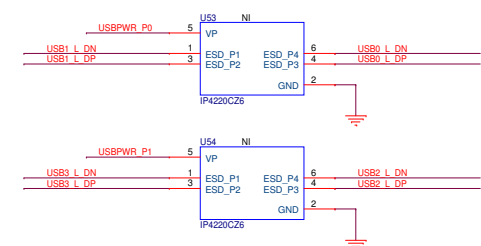
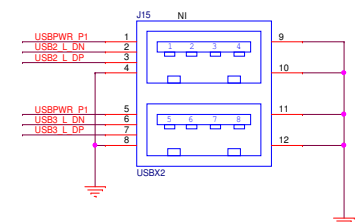
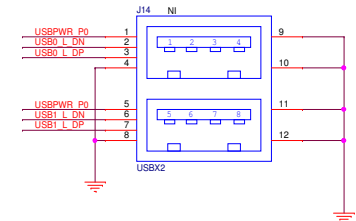
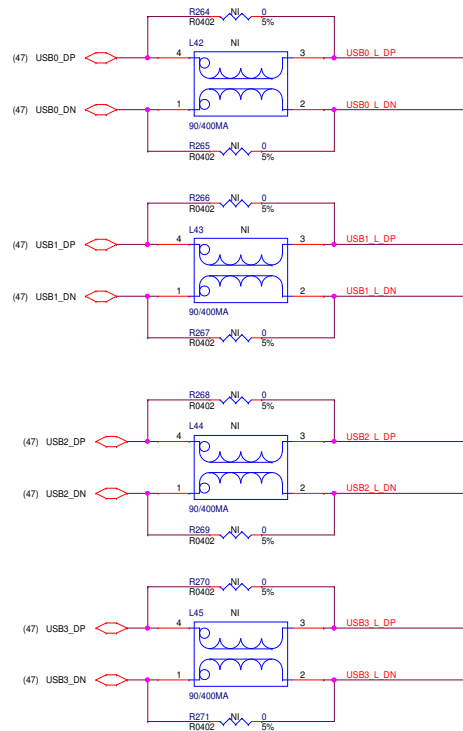
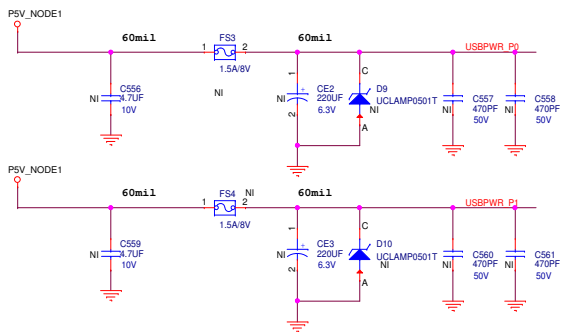
Cloud Server Infrastructure Engineering

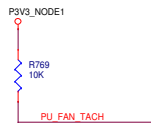
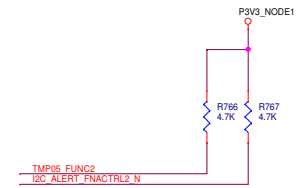
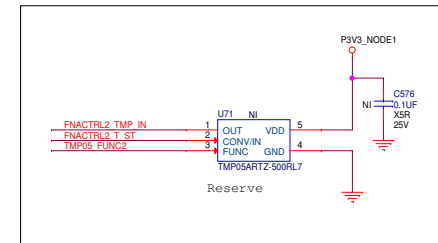
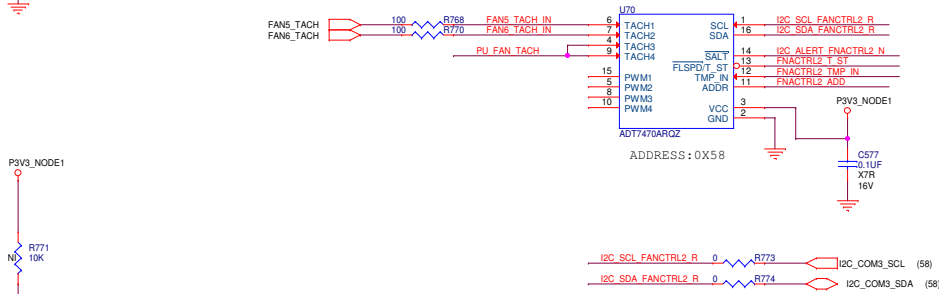
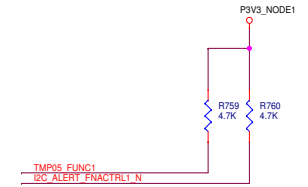
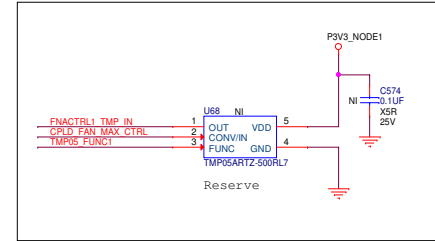
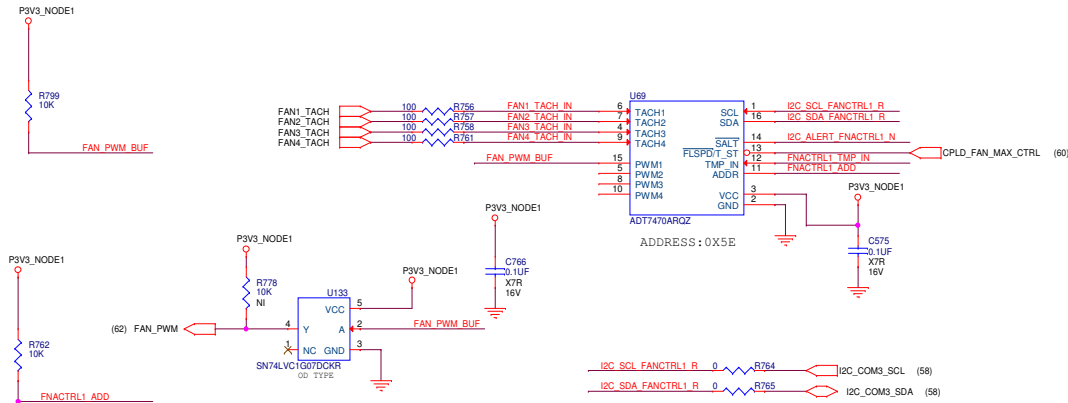
Chassis Manager Assembly V1

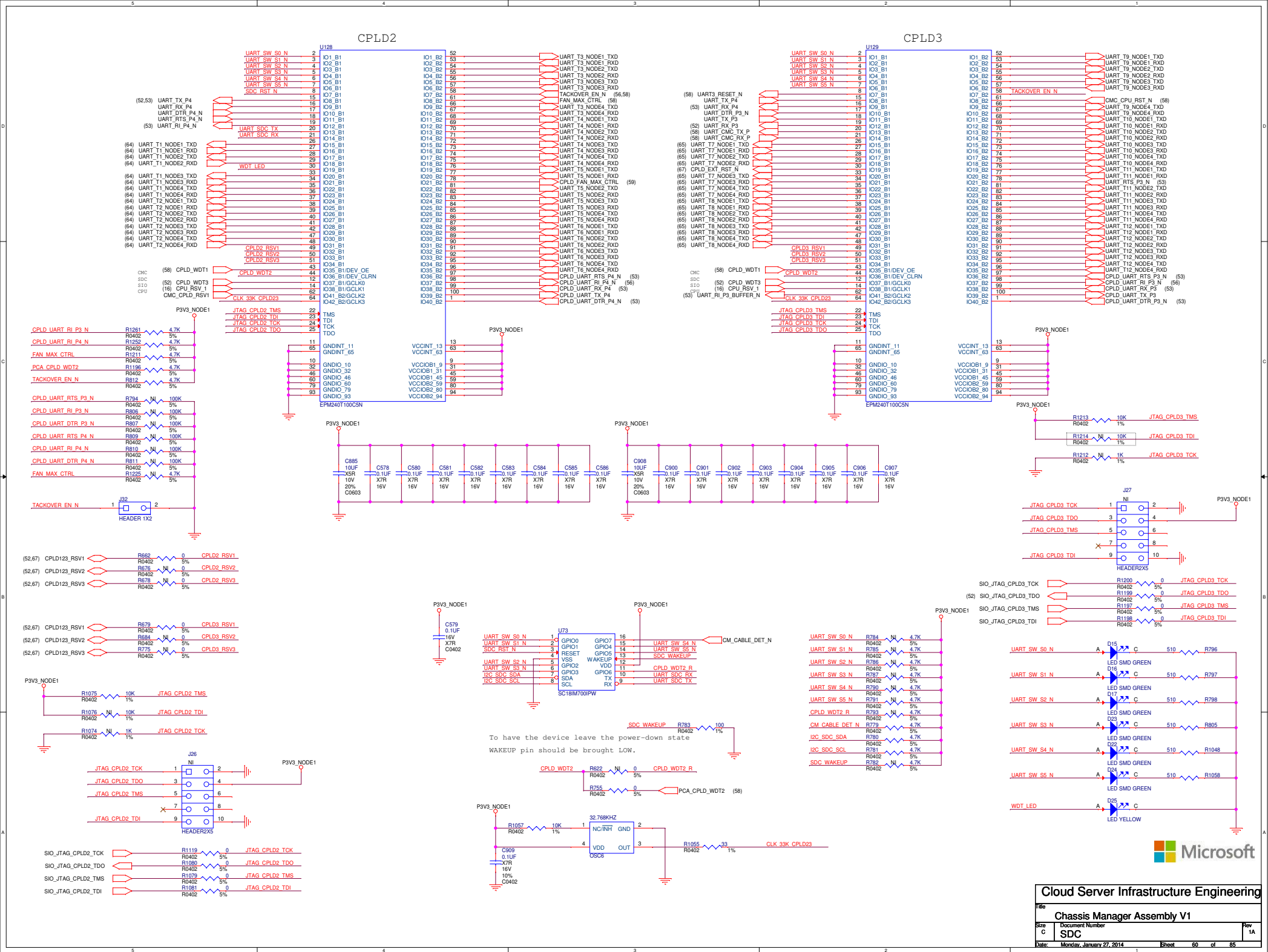
Document Number RS232 Driver/Receiver

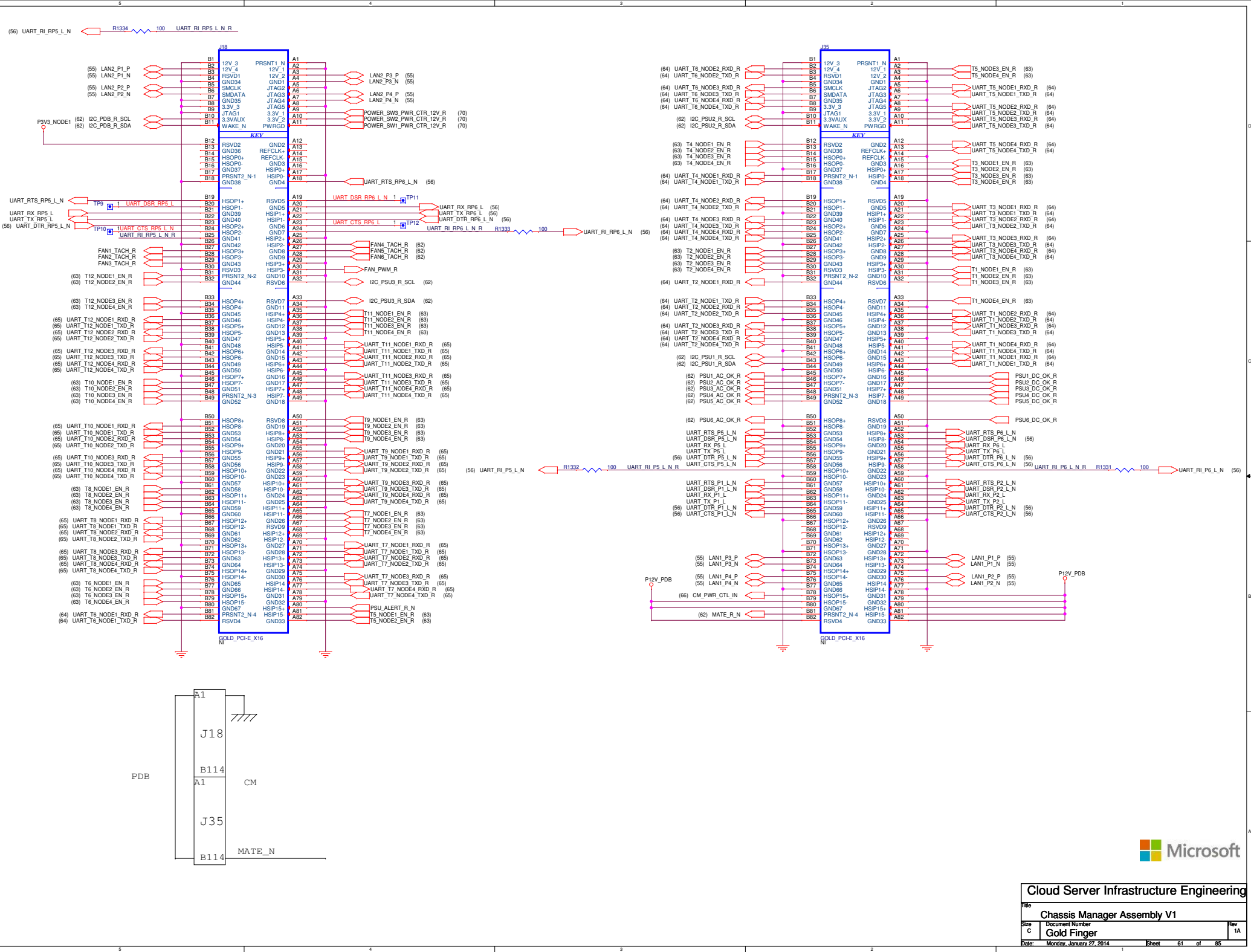
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Current limit =1.5~2A





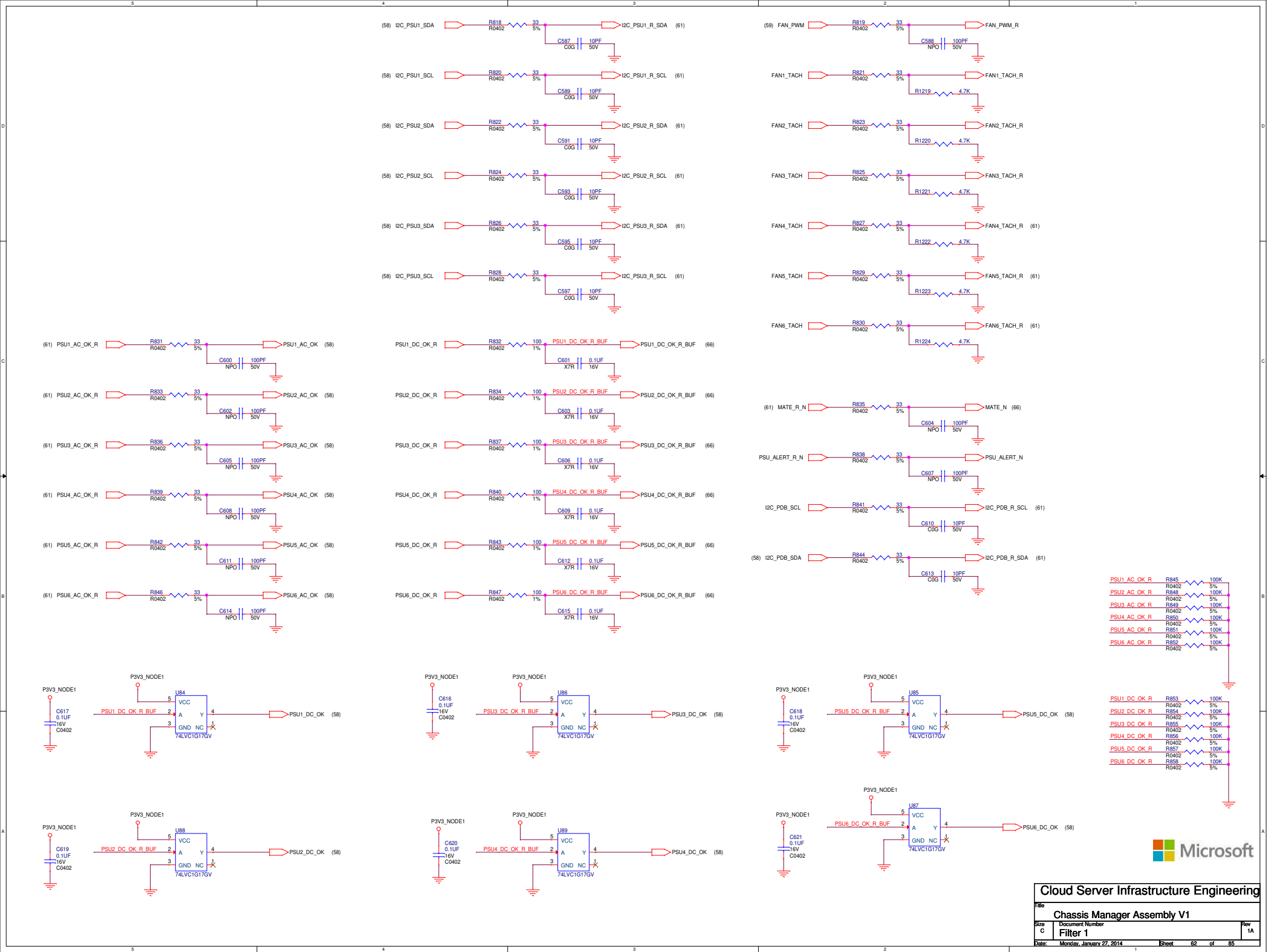




Cloud Server Infrastructure Engineering

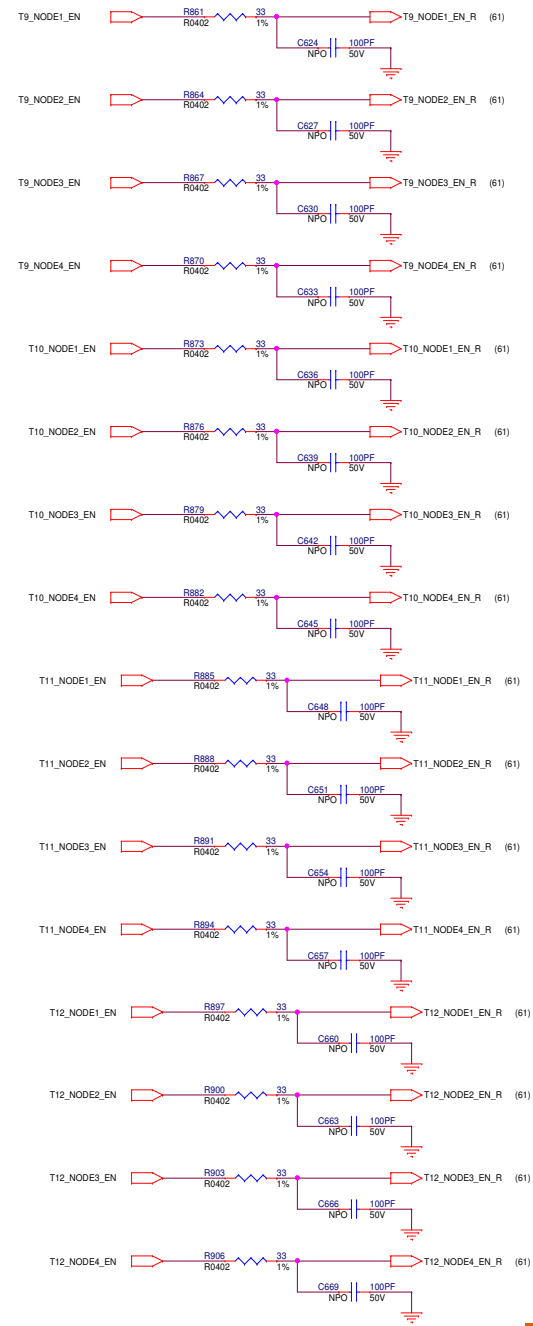
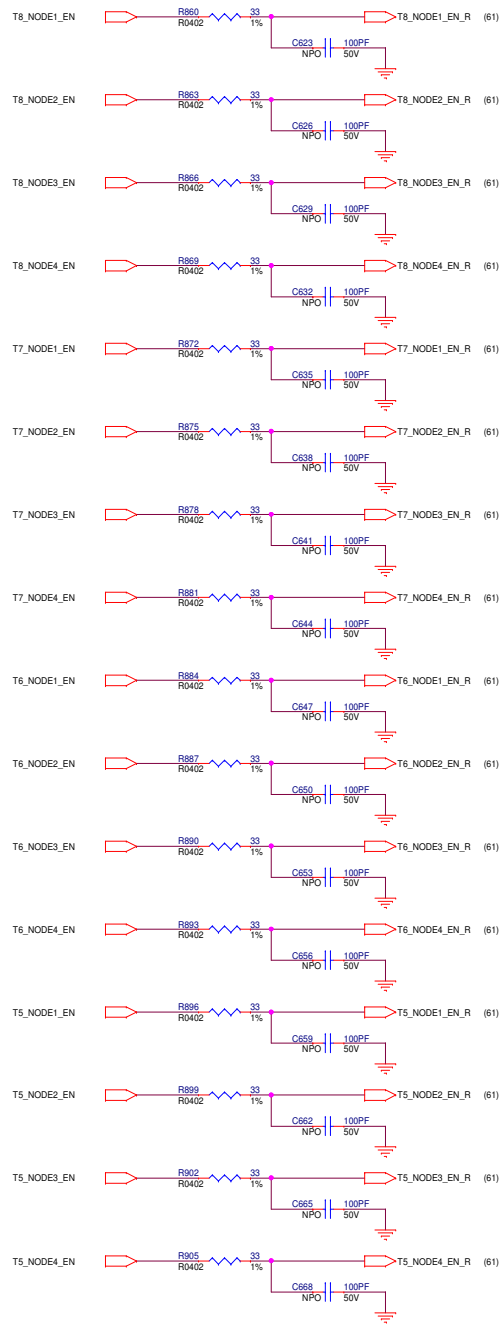
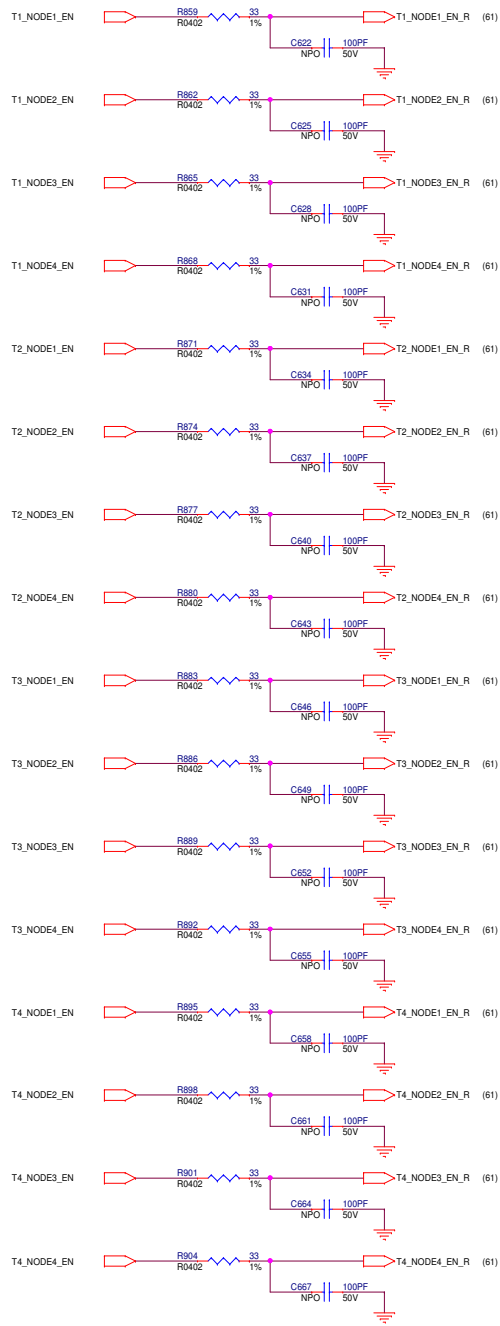
Chassis Manager Assembly V1

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|-------|--------------------------|----------------|
| C | Gold Finger | 1A |
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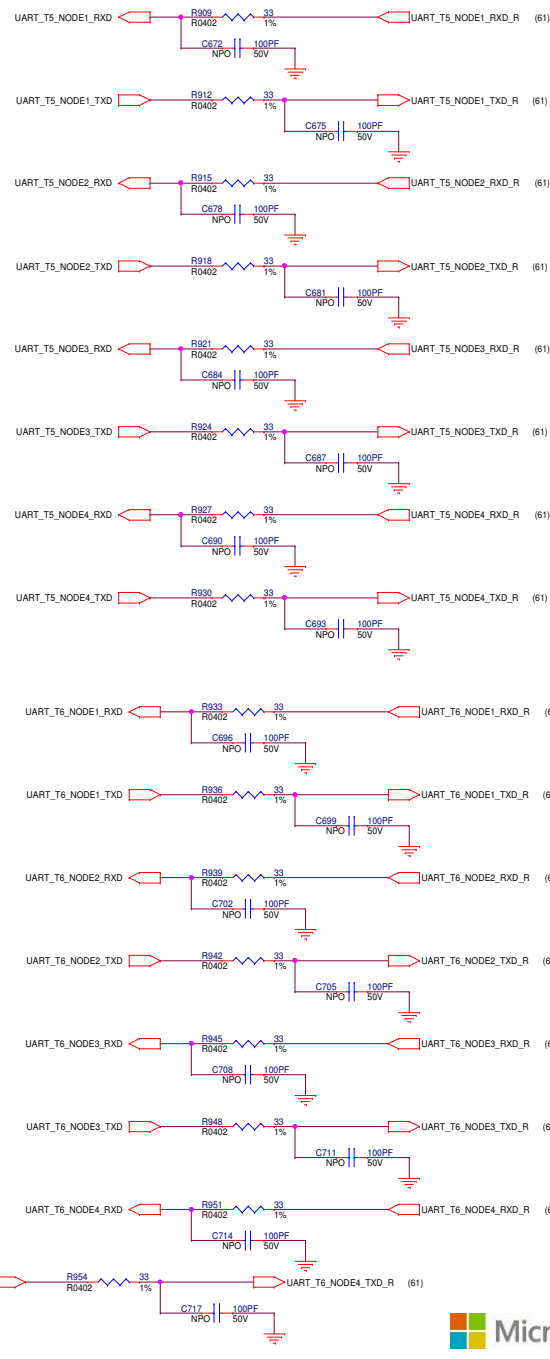
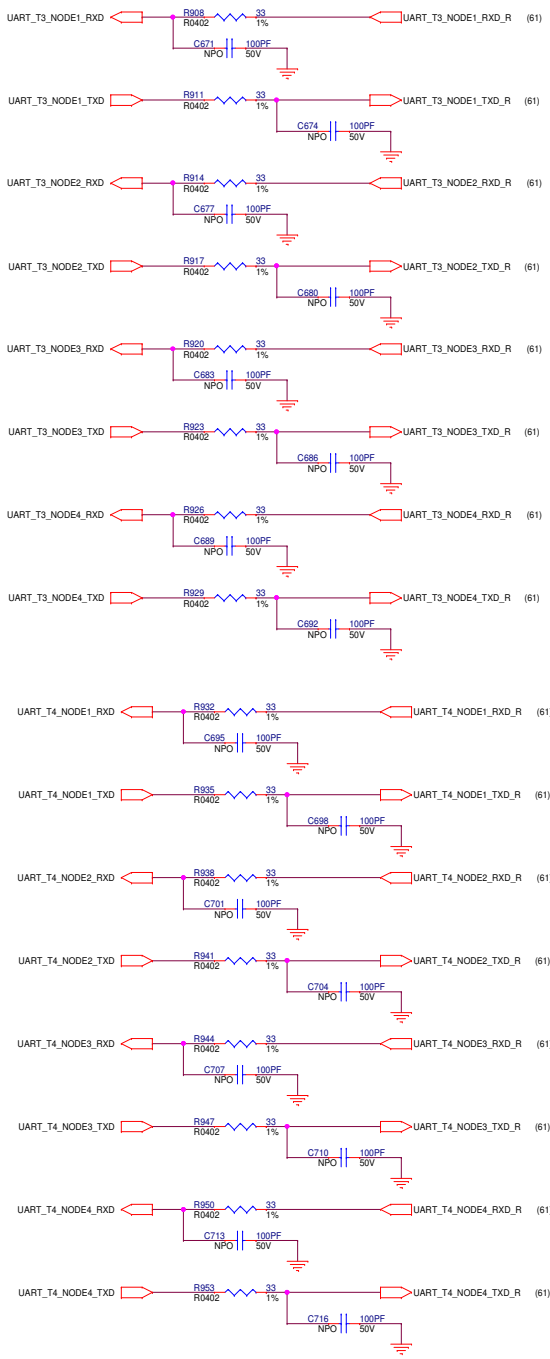
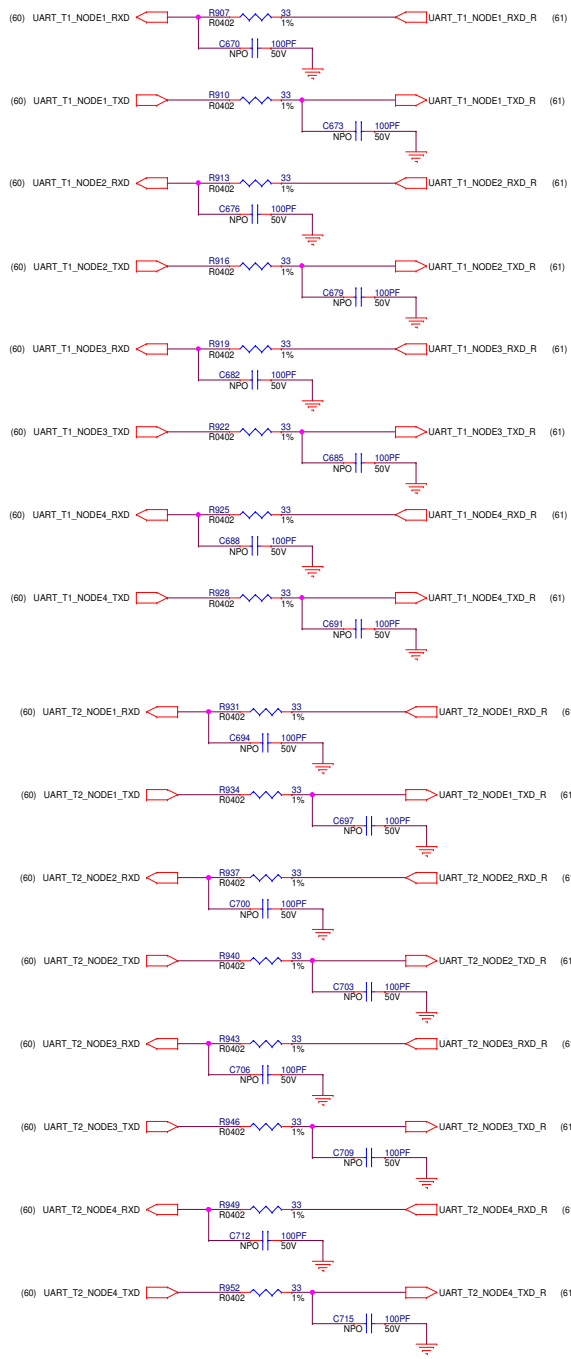
Cloud Server Infrastructure Engineering

| Chassis Manager Assembly V1 | | | Rev 1A |
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| File | Document Number | | |
| Size | Filter 1 | | |
| C | Monday, January 27, 2014 | Sheet | 62 of 65 |



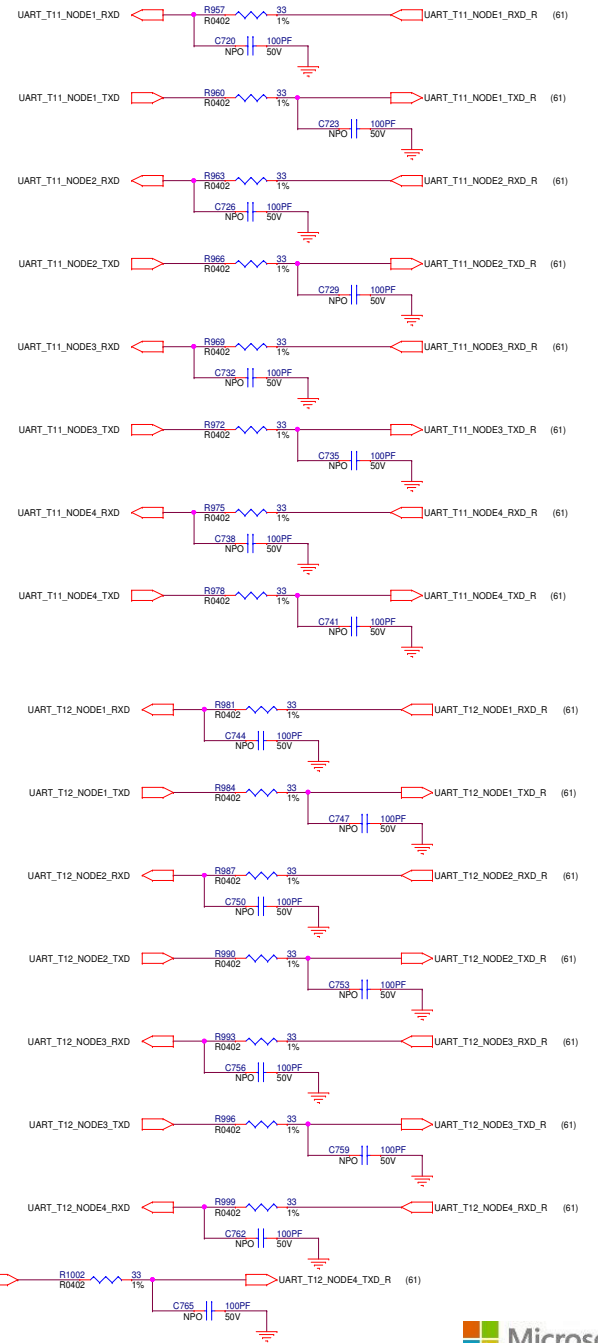
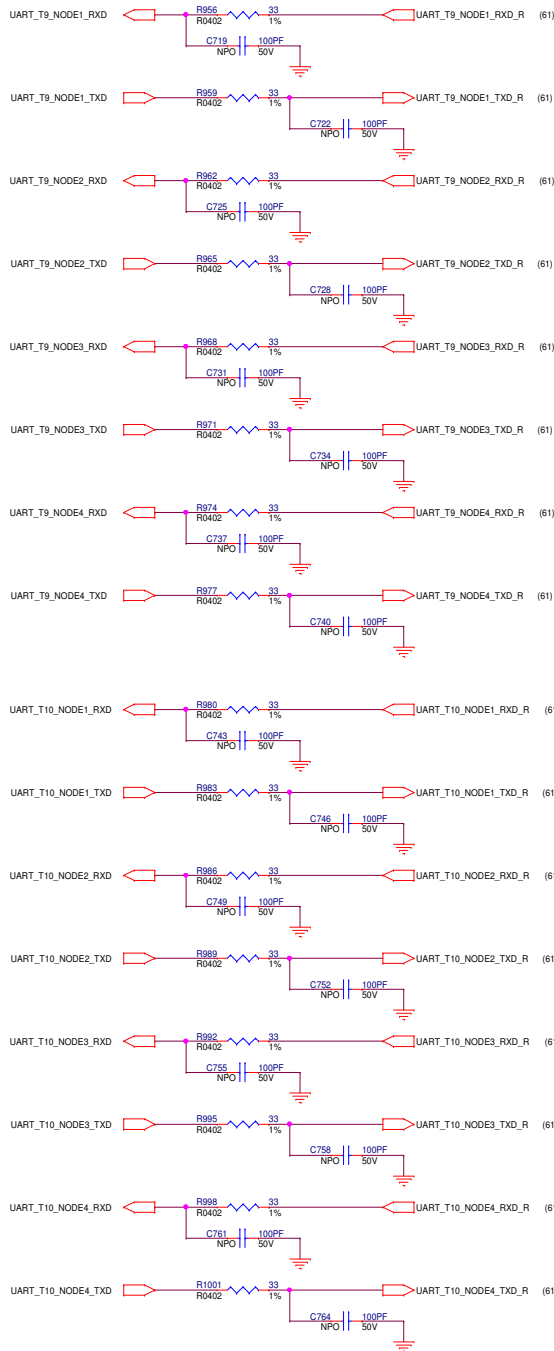
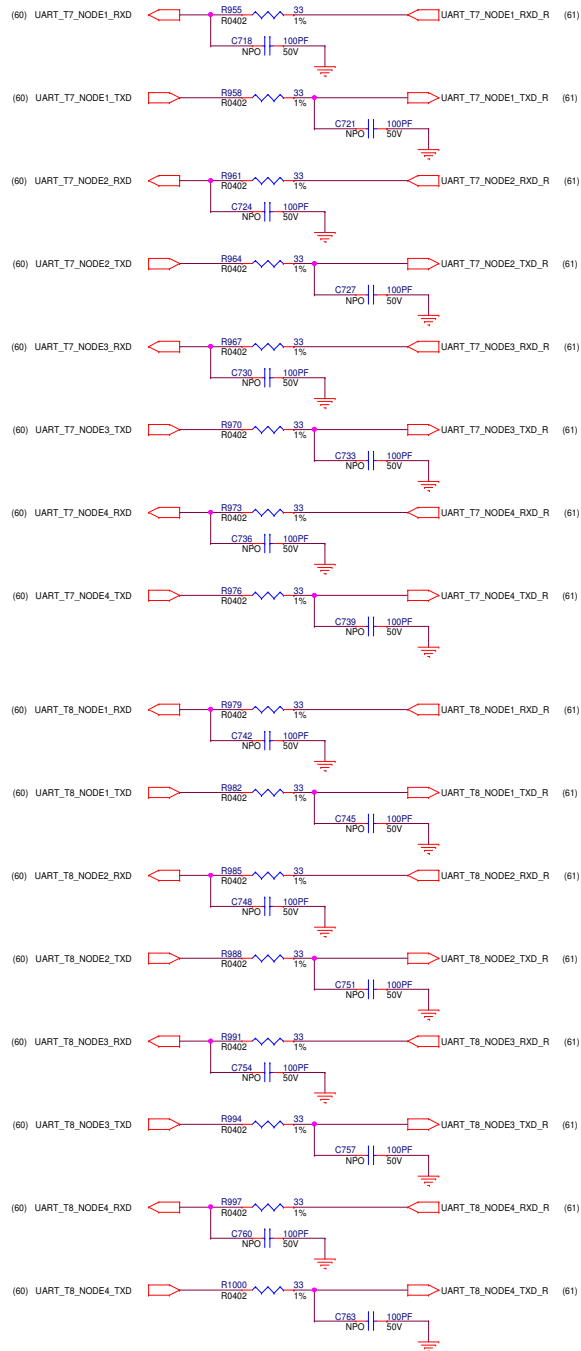
Cloud Server Infrastructure Engineering

| Chassis Manager Assembly V1 | | |
|--------------------------------|-----------------|--------|
| File | Document Number | Rev 1A |
| Size C | Filter 2 | |
| Date: Monday, January 27, 2014 | Sheet 63 | of 65 |



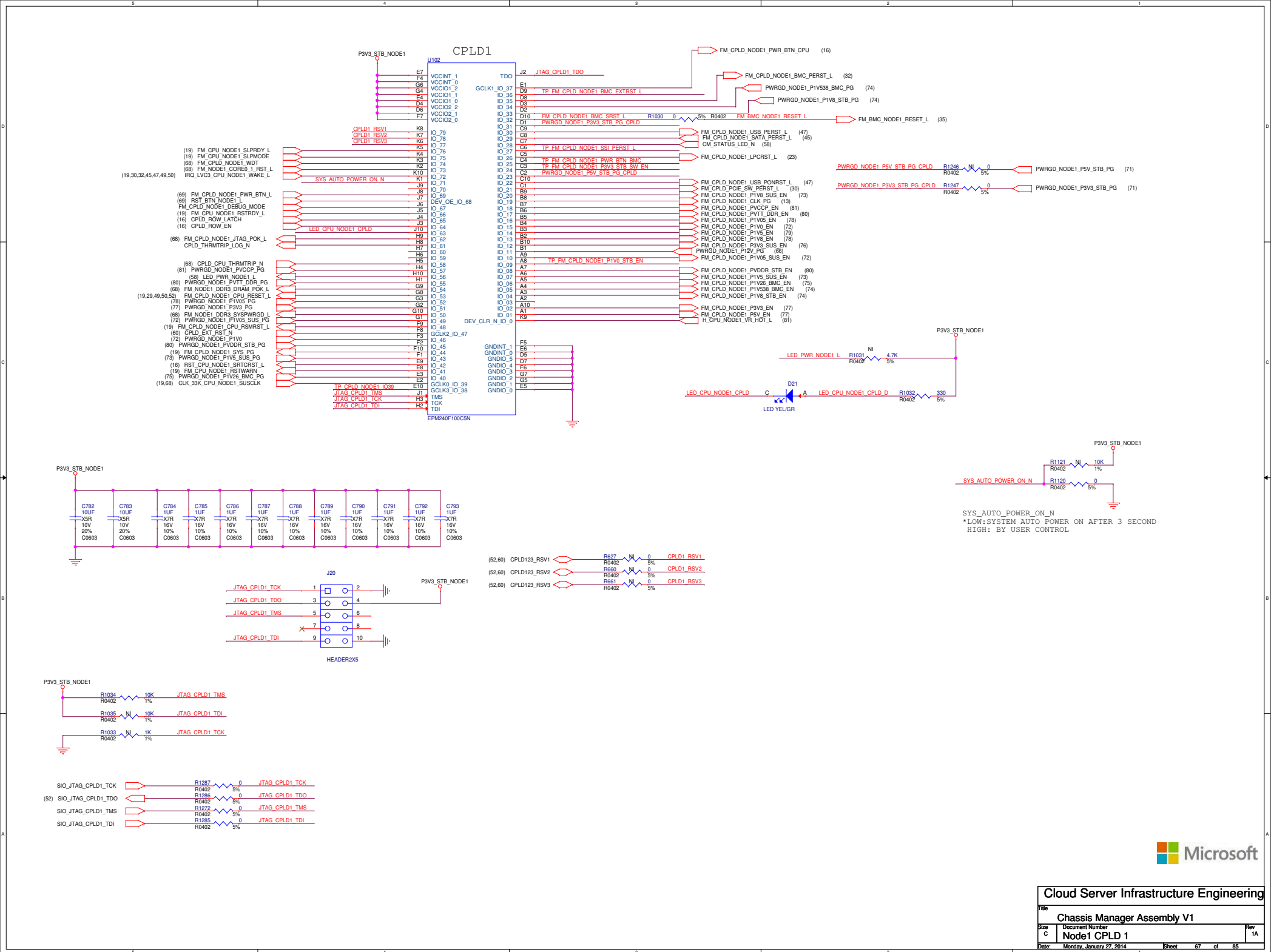
Cloud Server Infrastructure Engineering

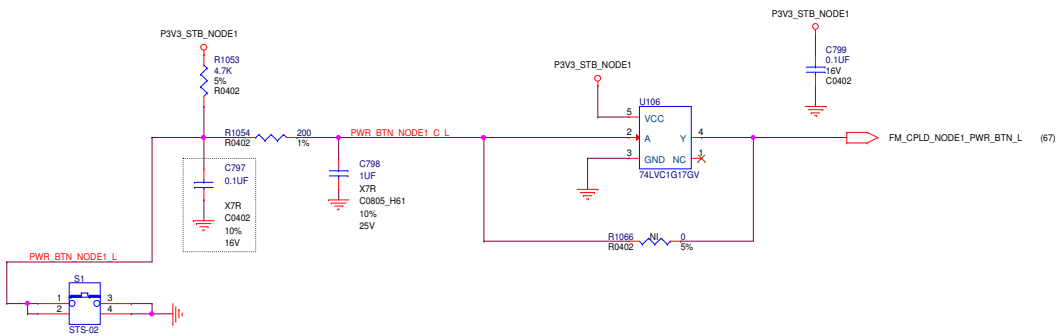
| Chassis Manager Assembly V1 | | |
|-----------------------------|--------------------------|----------------|
| Size | Document Number | Rev 1A |
| C | Filter 3 | |
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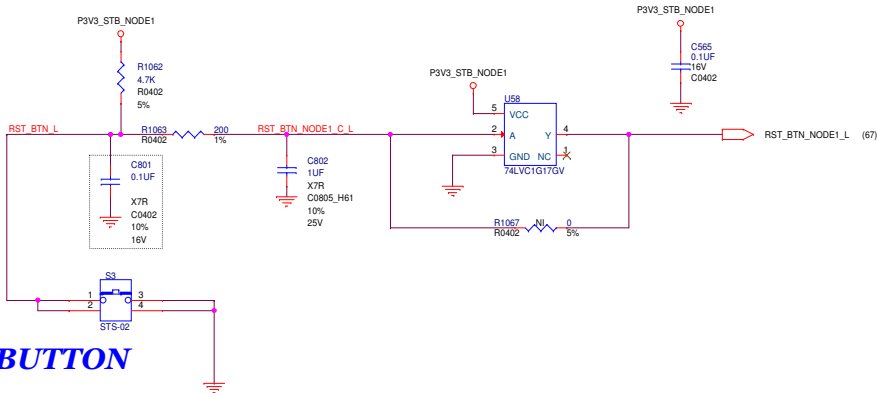
Cloud Server Infrastructure Engineering

| Chassis Manager Assembly V1 | | | Rev 1A |
|--------------------------------|-----------------|----|--------|
| File | Document Number | | |
| Size C | Filter 4 | | |
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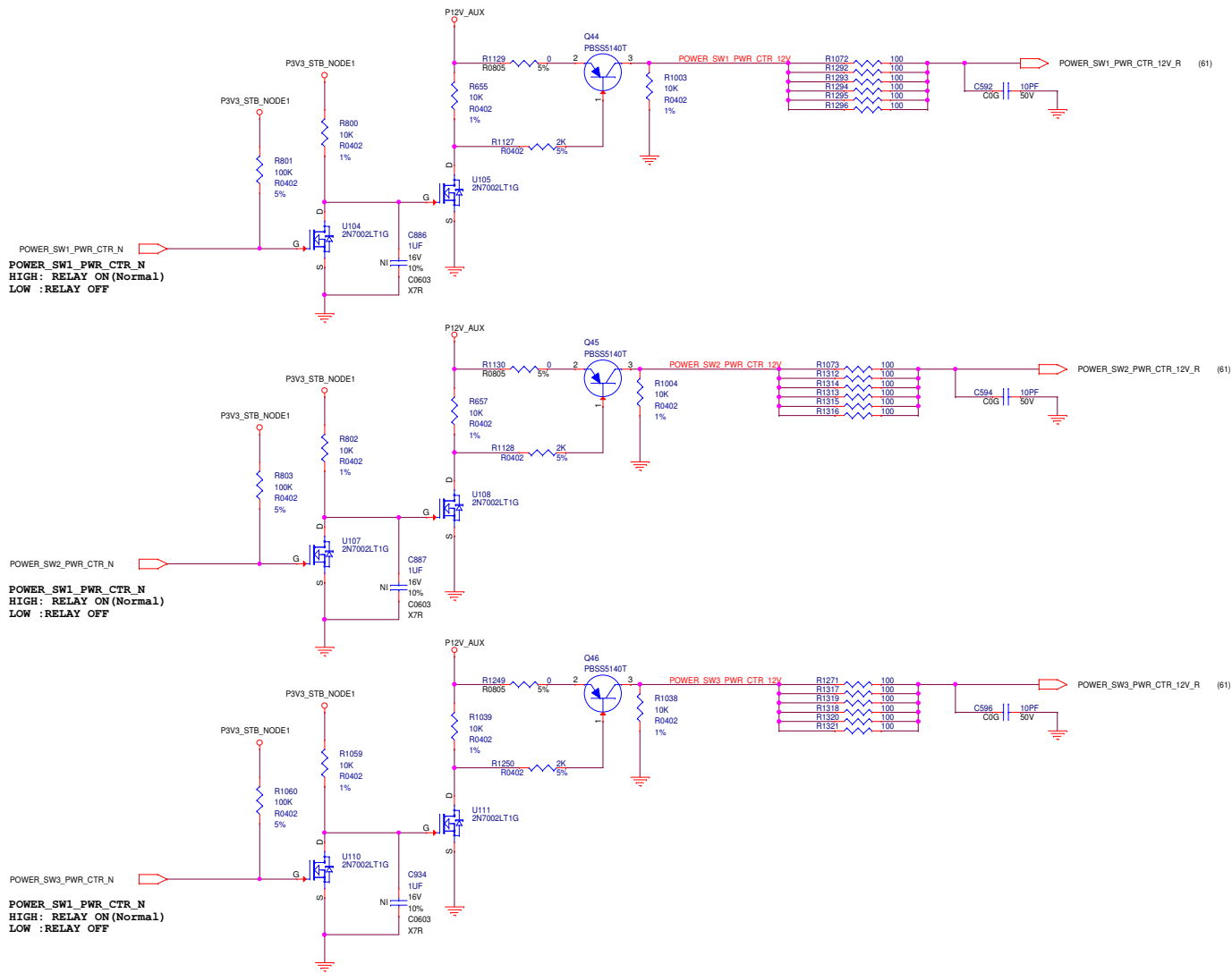


Power Button



RESET BUTTON





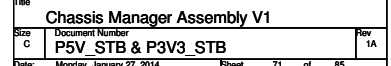
Cloud Server Infrastructure Engineering

| Chassis Manager Assembly V1 | | |
|-----------------------------|--------------------------|----------------|
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| C | Level Shift | 1A |
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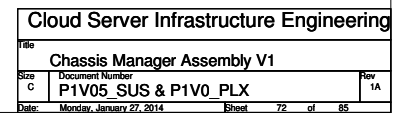
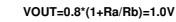
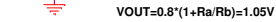
Output Voltage = 5V \pm 0.5% (DC \pm 1.5%)
Output Ripple & Noise < 50mV
Transient Tolerance = 500mV
TDC = 0.85 A
Max current = 0.95A
Over-Current Protection(IC Default*1.3) = 1.248A
Current Step = 0.95A
Slew Rate = 0.5A/us
Work frequency = 700KHZ
Efficiency > 80% @TDC

[illegible]

Output Voltage = 3.3V_I 0.5% (DC) 0.2%
Output Ripple & Noise < 50mV
Transient Tolerance = 330mV
TDC = 0.4A
Max current = 0.5A (budget=0.45A)
Over-Current Protection (IC Default*1.3)
= 0.65A
Current Step = 0.25A
Slew Rate = 0.5A/us
Work frequency = 700kHz
Efficiency > 80% @TDC

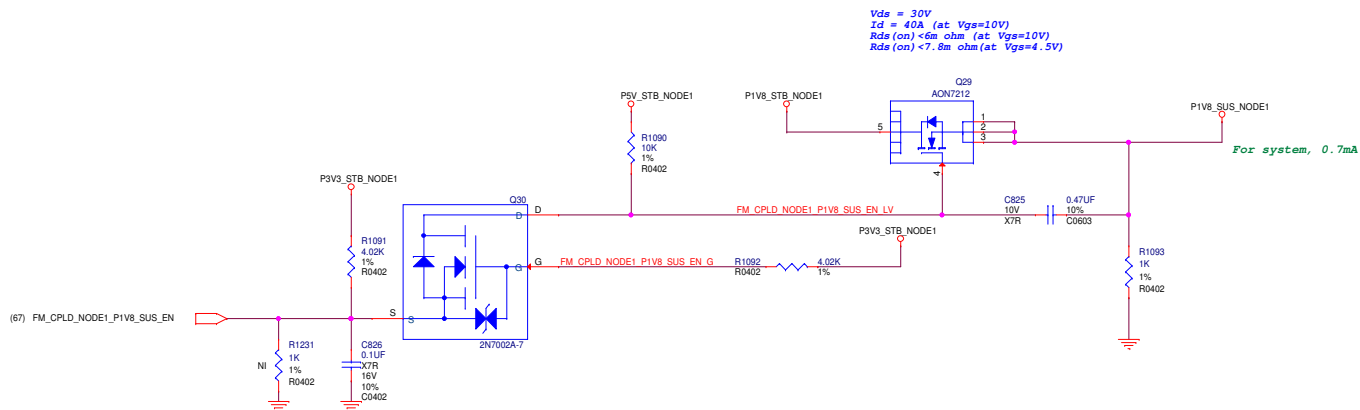
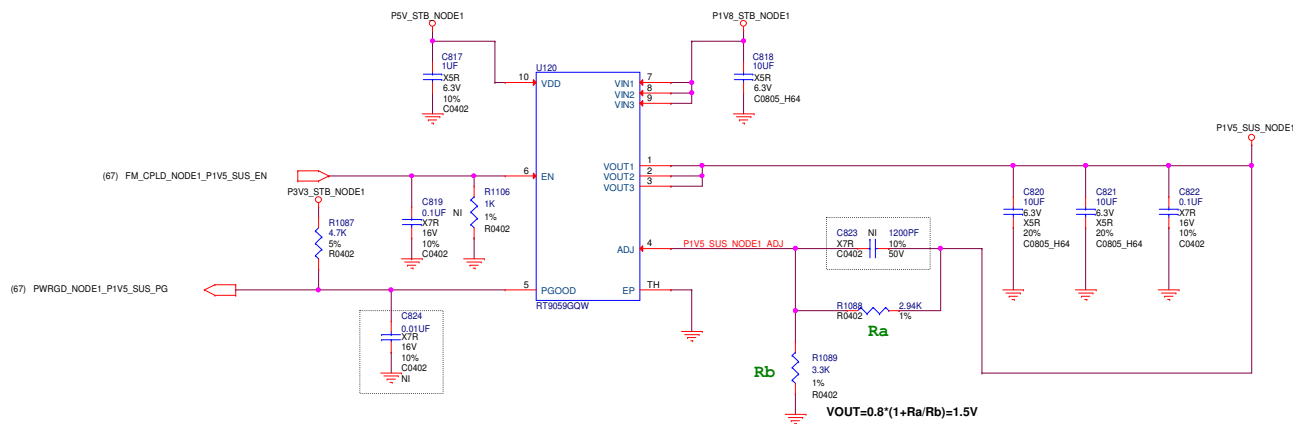
[illegible]

Output Voltage=1.05V+/-1.0%
AC TRANSIENT=+/-4.0%
TDC=0.84A
MAX CURRENT=0.84A
CURRENT STEP=0.42A
SLEW RATE=2.5A/US
PD=(1.8V-1.05V)*0.0003A=0.000225W



Design specification

Output Voltage=1.5V+/-1.0%
 AC TRANSIENT=+/-4.0%
 TDC=0.84A
 MAX CURRENT=0.84A
 CURRENT STEP=0.42A
 SLEW RATE=2.5A/US
 PD=(1.8V-1.5V)*0.189A=0.0567W



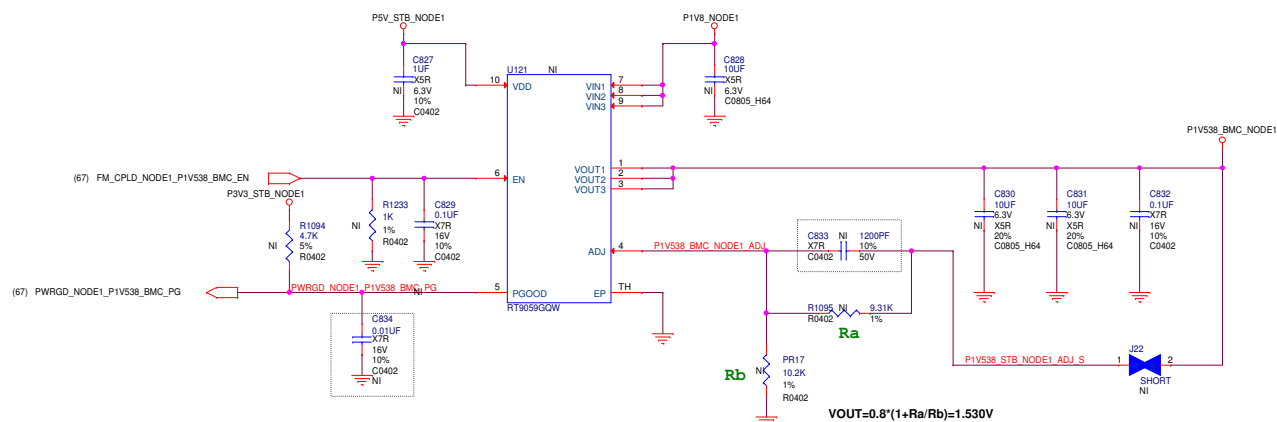
Cloud Server Infrastructure Engineering

| Chassis Manager Assembly V1 | | |
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| Size | Document Number | Rev 1A |
| C | P1V5 SUS & P1V8 SUS | |
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Output Voltage = $1.8V_{(\pm 2\%)}$ (DC= $\pm 1\%$)
Output Ripple & Noise = $< 18\text{ mV}$
Transient Tolerance = $108\text{mV}_{(\pm 3\%)}$
TDC = 2A
Max current = 2.4 A
Over-Current Protection(Max Current*1.3) = 0.91A
Current Step = 0.3A
Slew Rate = 2.5A/us
Work frequency = 700kHz
Efficiency > 80% @TDC

[illegible]

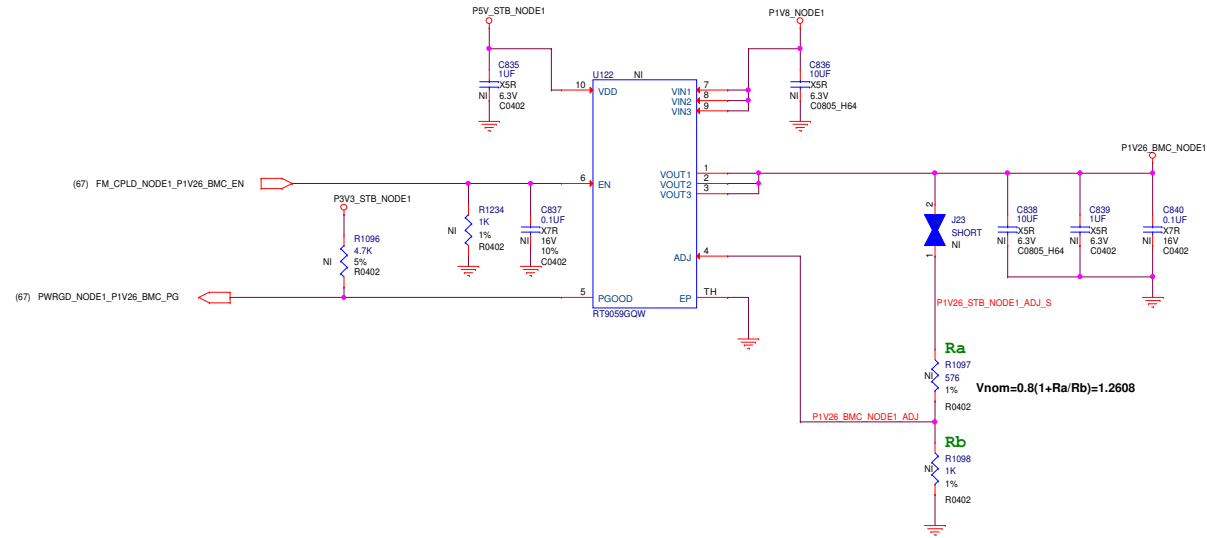
Output Voltage=1.53V+/-1.0%
AC TRANSIENT=+/-4.0%
TDC=0.44A
MAX CURRENT=0.84A
CURRENT STEP=0.832A
SLEW RATE=2.5A/US
PD=(1.8V-1.538V)*0.44A=0.119W



| | | |
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| C | P1V8_STB & P1V538_STB | 1A |
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Design specification

Output Voltage=1.26V+/-1.0%
AC TRANSIENT=+/-4.0%
TDC=0.84A
MAX CURRENT=0.84A
CURRENT STEP=0.42A
SLEW RATE=2.5A/US
PD=(1.8V-1.26V)*0.84A=0.45W

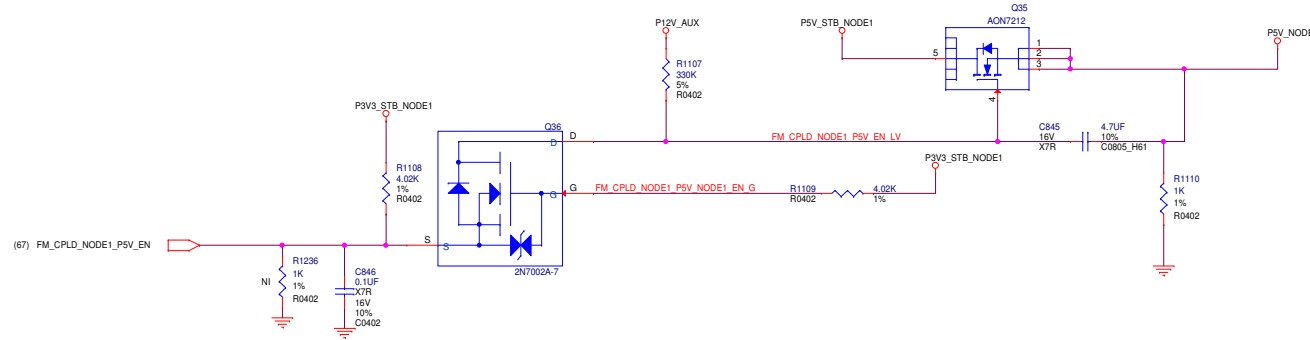


Cloud Server Infrastructure Engineering

| Title | | | |
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| C | P1V26_STB | 1A | |
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$V_{ds} = 30V$
 $I_d = 40A$ (at $V_{gs}=10V$)
 $R_{ds(on)} < 6m\ \Omega$ (at $V_{gs}=10V$)
 $R_{ds(on)} < 7.8m\ \Omega$ (at $V_{gs}=4.5V$)

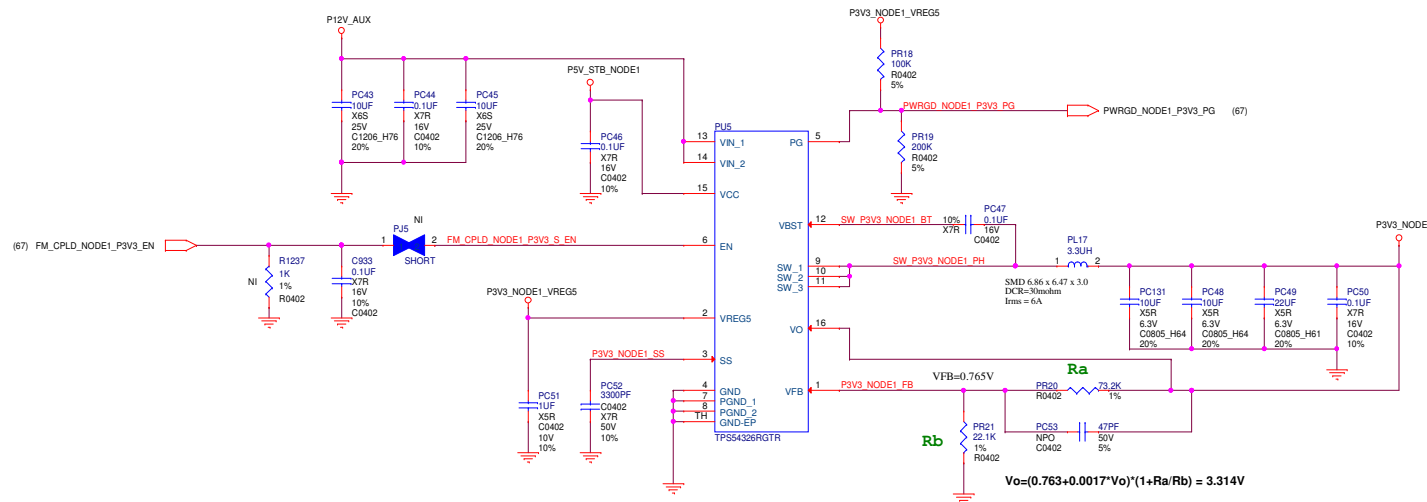
For system, 0.7A



Design specification

Output Voltage = $3.3V \pm 5\%$ (DC; $\pm 2\%$)
 Output Ripple & Noise < 50mV
 Transient Tolerance = 330mV
 TDC = 1.6A
 Max current = 2A (budget 1.914A)
 Over-Current Protection (IC Default * 1.3) = 2.6 A
 Current Step = 0.5A
 Slew Rate = 1A/us
 Work frequency = 700kHz
 Efficiency > 80% @TDC

2012.5.7 Modified by Kent



$$V_o = (0.763 + 0.0017 \cdot V_o) \cdot (1 + R_a/R_b) = 3.314V$$

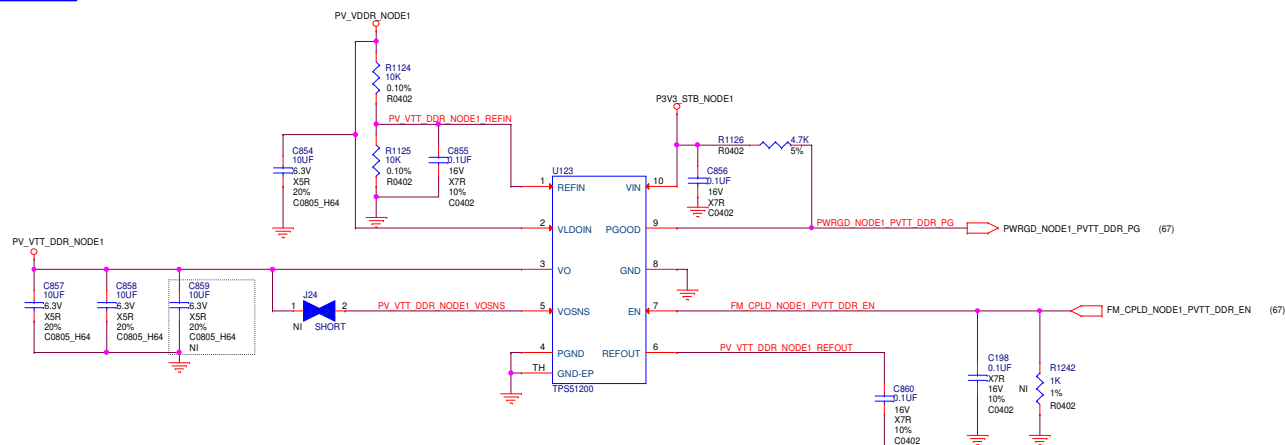
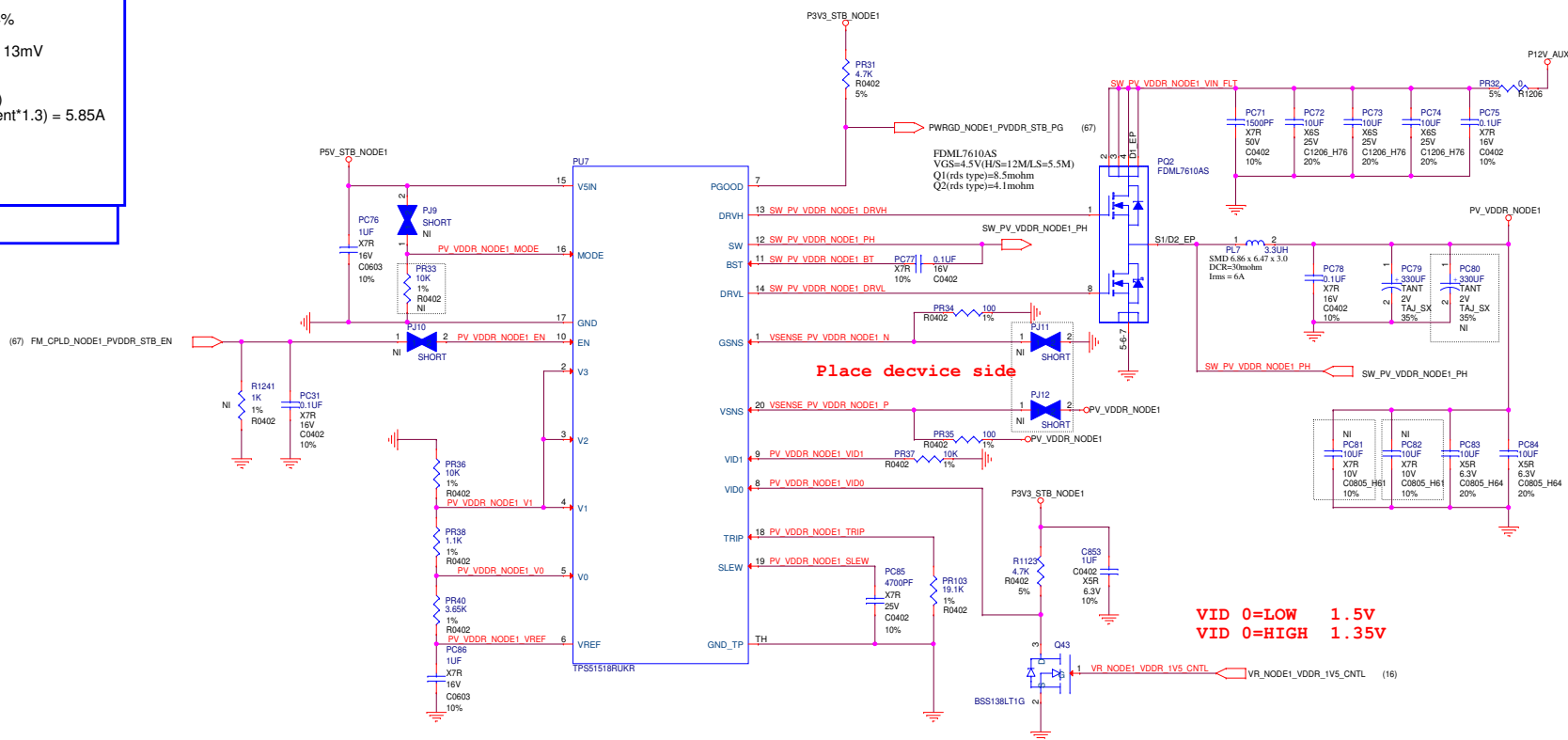


Cloud Server Infrastructure Engineering

| Chassis Manager Assembly V1 | | |
|--------------------------------|-----------------|--------|
| File | Document Number | Rev 1A |
| Size C | P5V & P3V3 | |
| Date: Monday, January 27, 2014 | Sheet 77 | of 85 |

Output Voltage = 1.5 OR 1.35V \pm 0.4%
(DC \pm 0.1.5%)
Output Ripple & Noise = <15mV or 13mV
Transient Tolerance = \pm 4%
TDC = 3.6A
Max current = 4.5 A (budget4.206A)
Over-Current Protection(Max Current \times 1.3) = 5.85A
Current Step = 3A
Slew Rate = 10A/us
Work frequency = 350kHz
Efficiency > 80% @TDC

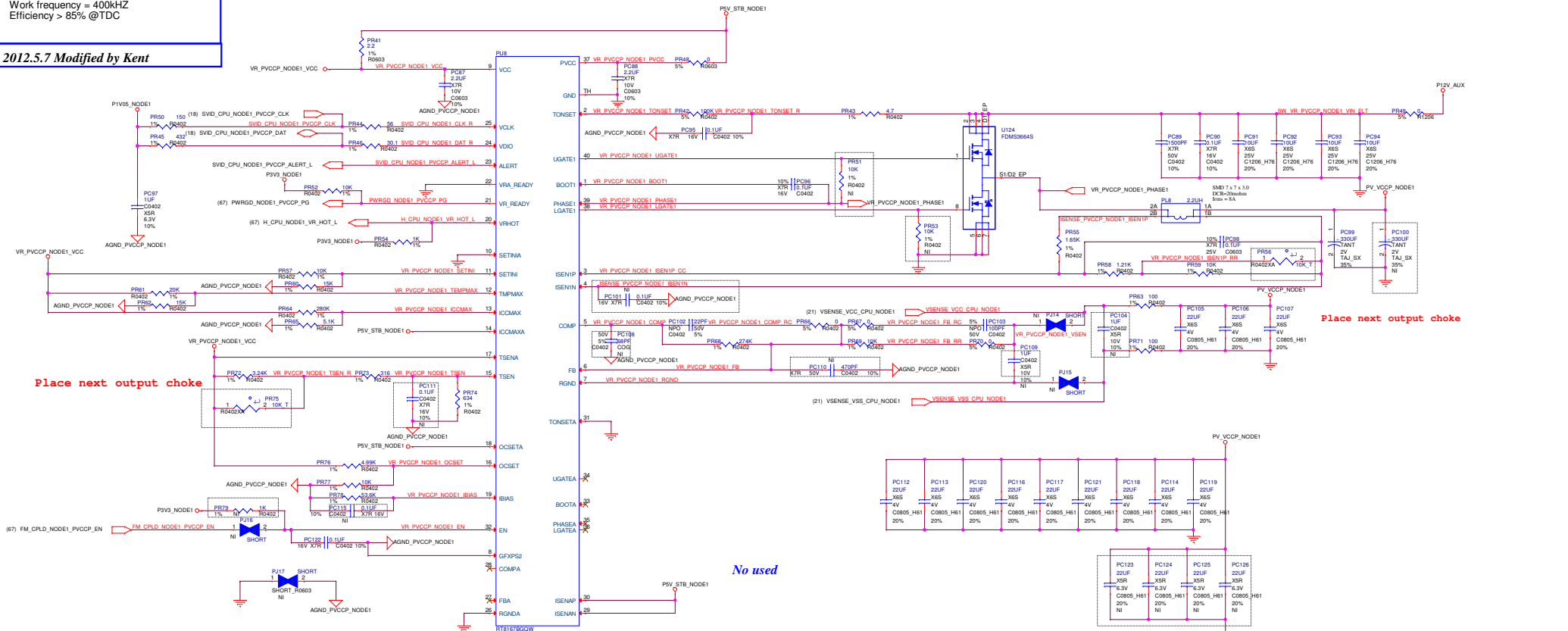
Output Voltage = 0.75V or 0.675 V \pm 5%
Output Ripple & Noise < 15mV or 13.5mV
Transient Tolerance = 75mV or 67.5mV
TDC = 0.4A
Max current = 0.4A
PD = (1.5V - 0.75V) \times 0.4A = 0.3W
or
PD = (1.35V - 0.675V) \times 0.4A = 0.27W

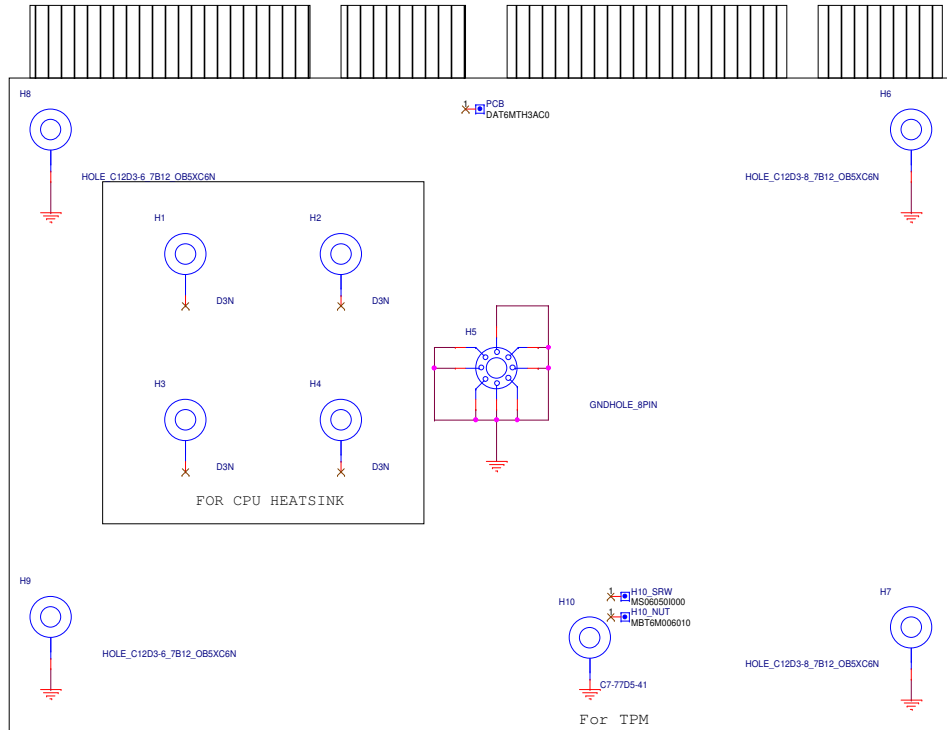


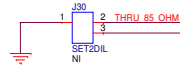
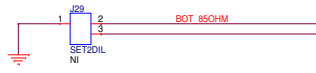
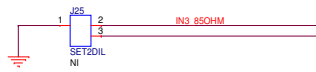
Design specification

- Output Voltage = $1.1V \pm 0.5\%$ (DC; $\pm 0.5\%$)
- Output Ripple & Noise < $22mV$ ($\pm 0.1\%$)
- Transient Tolerance = $77mV$ ($\pm 0.5\%$)
- TDC = 2.56A
- Max current = 3.2A (bouget 3.118)
- Over-Current Protection (IC Default* 1.3) = $4.16A$
- Current Step = 2A
- Slew Rate = 1A/us
- Work frequency = 400KHZ
- Efficiency > 85% @TDC

2012.5.7 Modified by Kent







THRU for EA measured reference.





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|-----------------------------------------|--------------------------|-----------------------------|----------|
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