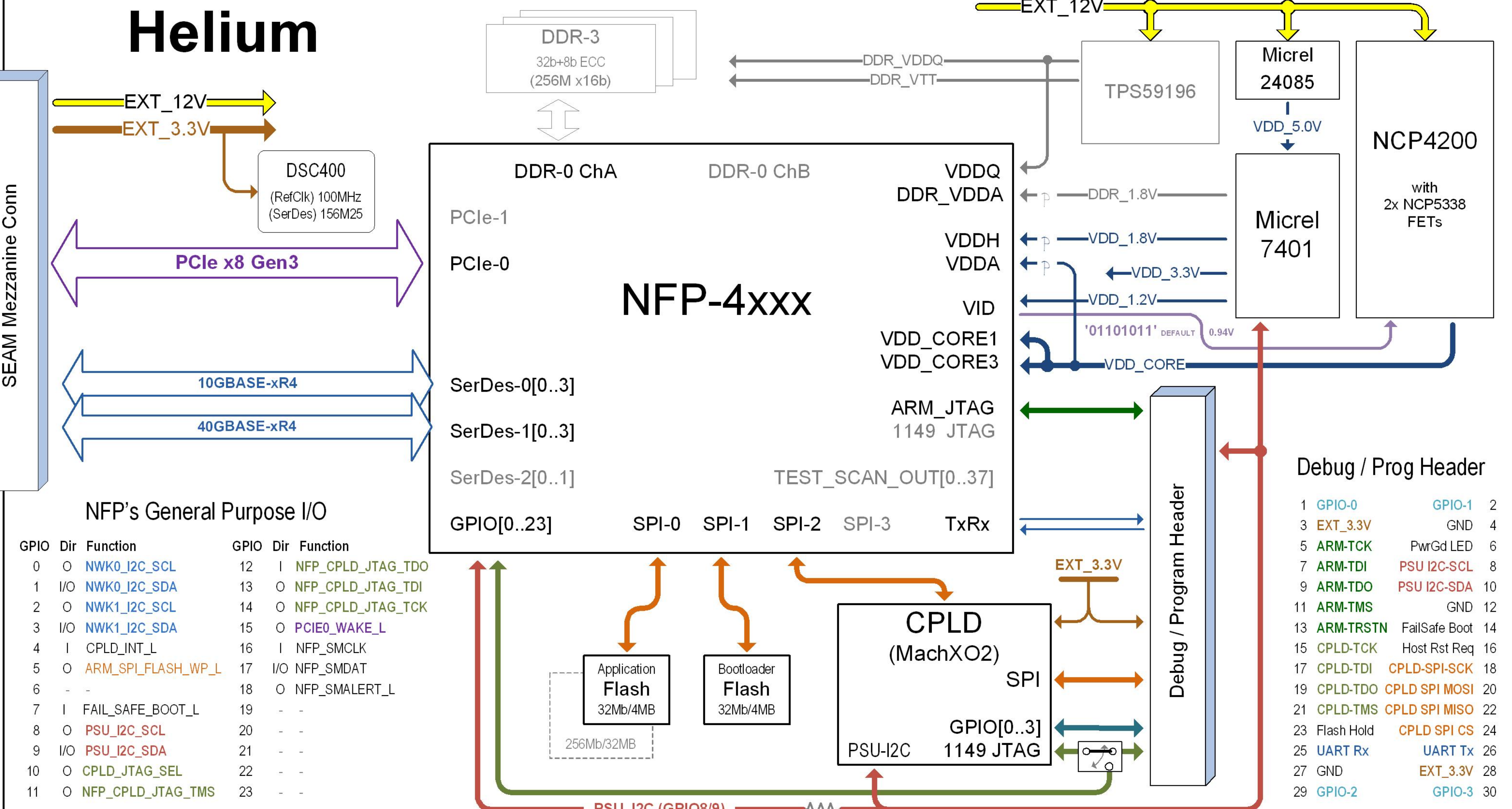
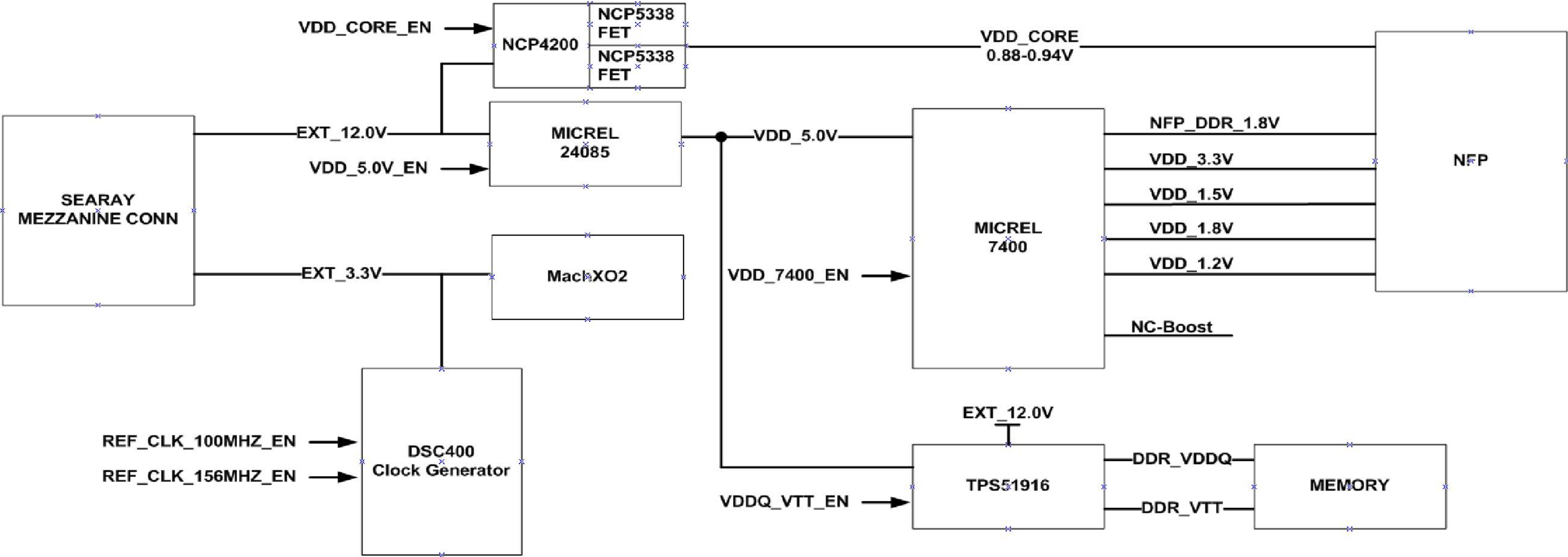


A		B		C		D																													
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REV	DESCRIPTION	DATE	APPROVED																																
	Initial Draft	20150202	KFP																																
01	Initial revision	20150520																																	

Block Diagram



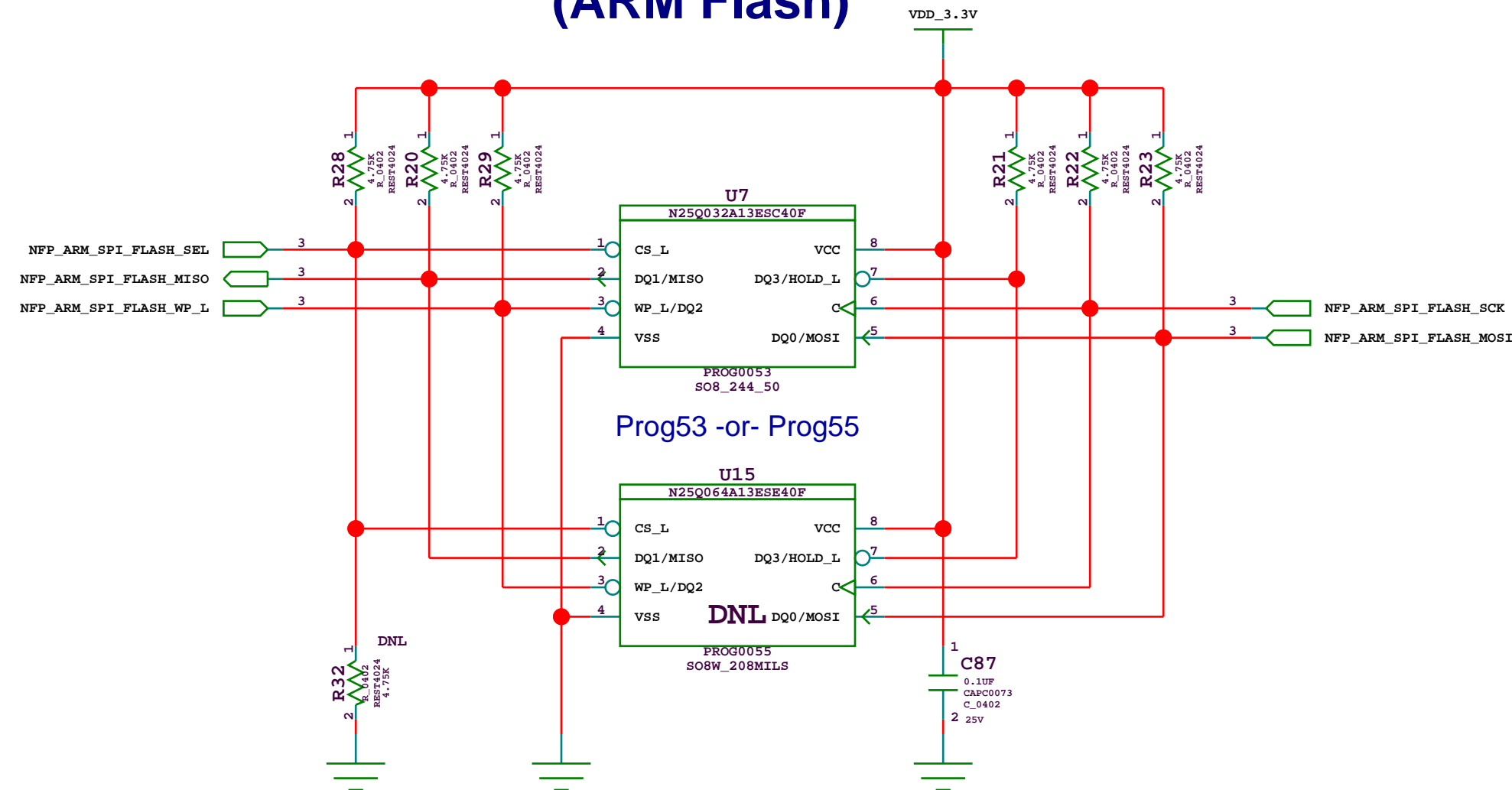
POWER DISTRIBUTION



			Voltage			Current		Power	
			Min	Typ	Max	Typ	Max	Typ	Max
PCIE_3V3			2.700	3.300	3.600	0.098A	0.168A	0.324W	0.555W
PCIE_12V0			0.000	12.000	0.000	2.797A	3.111A	33.56W	37.34W
	VDD_CORE		0.873	0.900	0.968	25.24A	28.39A	22.72W	25.55W
	VDD_FUSE		0.873	0.900	0.968	0.000A	0.000A	0.000W	0.000W
	VDD_CORE		0.873	0.900	0.968	23.44A	26.59A	21.10W	23.93W
	NFP_VDDA_SERDES012		0.873	0.900	0.968	1.100A	1.100A	0.990W	0.990W
	VDDA_PCIE0		0.873	0.900	0.968	0.700A	0.700A	0.630W	0.630W
	VDD_5V0		4.500	5.000	5.500	1.503A	1.540A	7.513W	7.701W
	VDD_1V2		1.140	1.200	1.260	0.100A	0.100A	0.120W	0.120W
	VDD_1V5		1.425	1.500	1.575	0.194A	0.194A	0.291W	0.291W
	VDD_1V8		1.746	1.800	1.854	1.428A	1.428A	2.571W	2.571W
	NFP_DDR_1V8		1.746	1.800	1.850	0.205A	0.205A	0.370W	0.370W
	VDD_3V3		3.135	3.300	3.465	1.108A	1.108A	3.657W	3.657W
	DDR_VDDQ		1.283	1.350	1.450	0.246A	0.501A	0.332W	0.676W

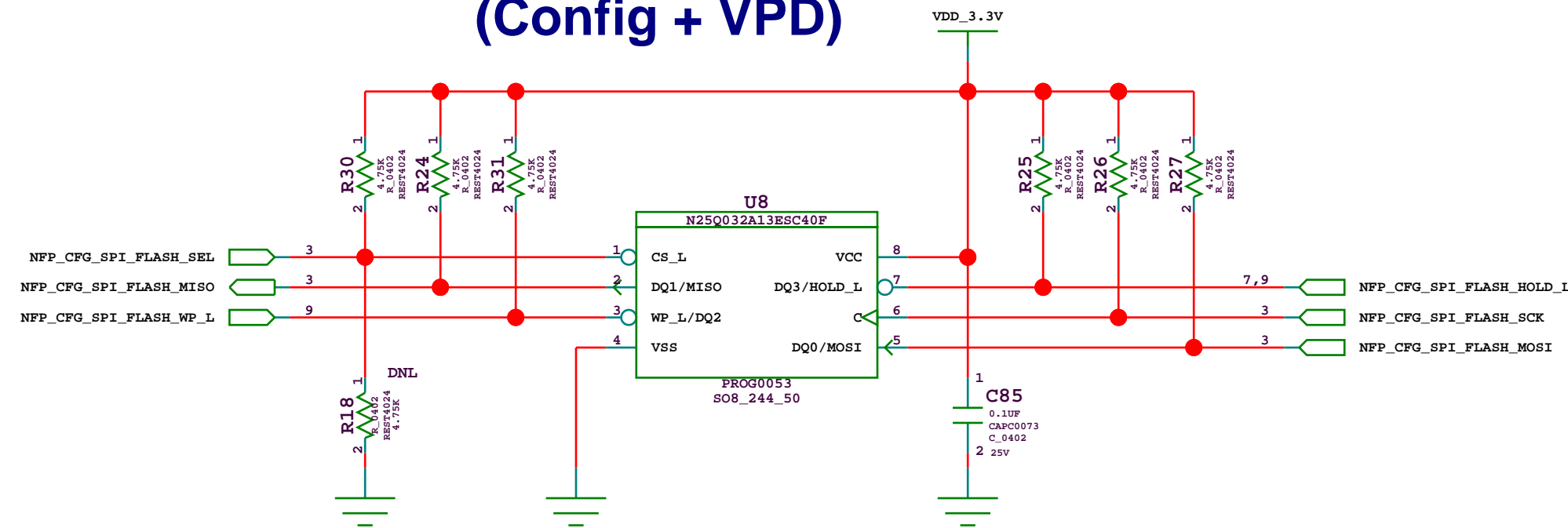
NFP - SPI Flash, Clock, Reset, GPIO

Application Flash [SPI-0] (ARM Flash)

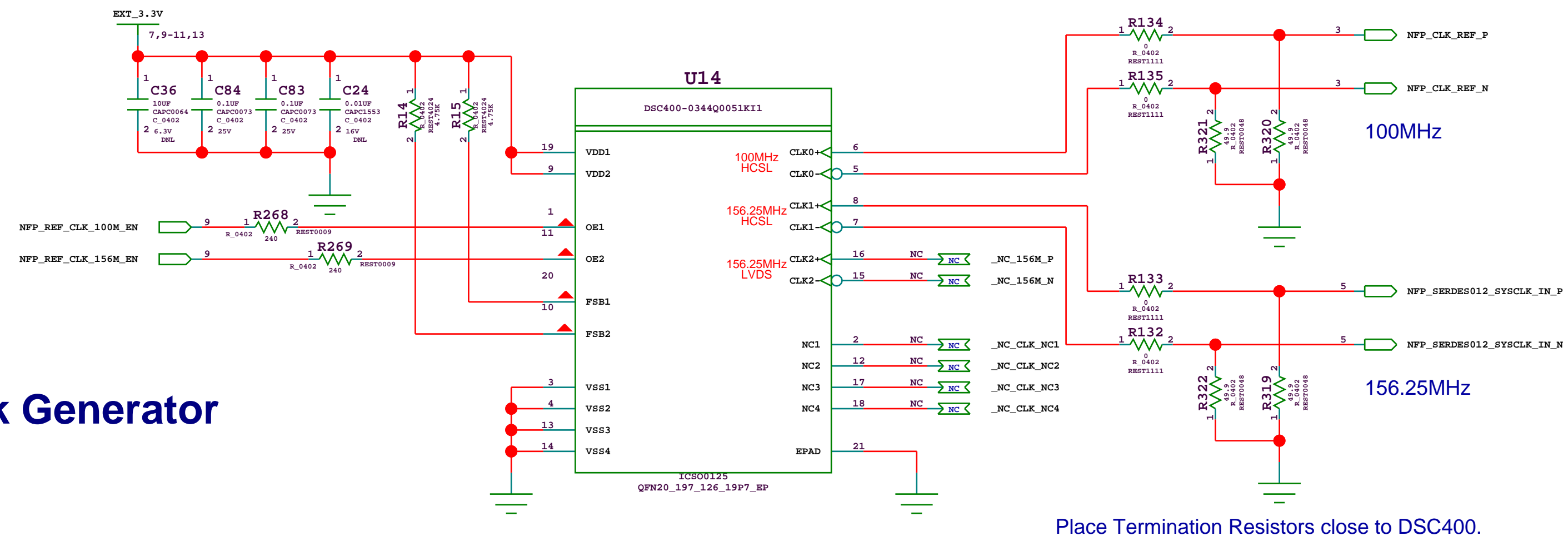


NOTE: Prog53 can overlap Prog55 (Only one loaded)

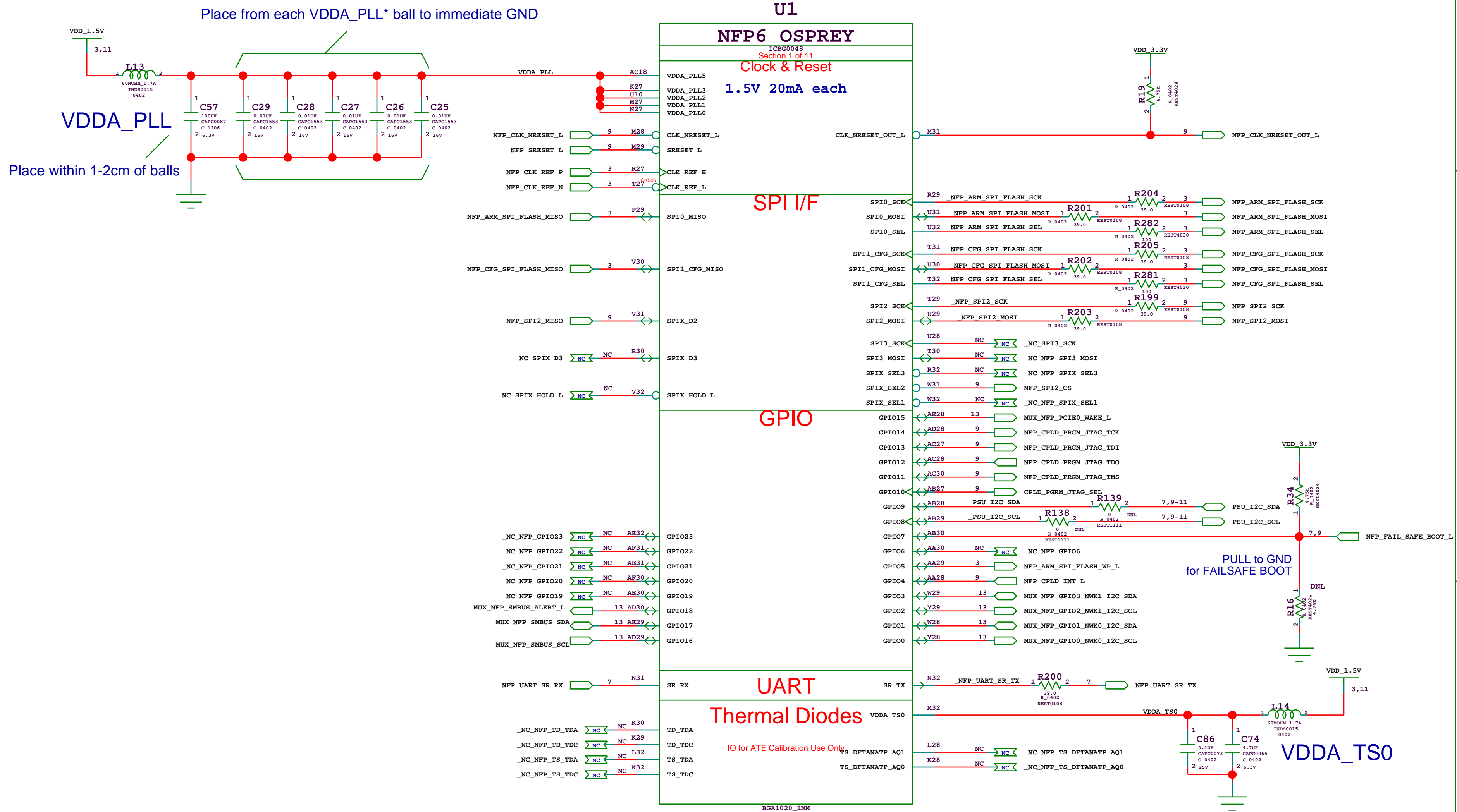
Bootloader and VPD Flash [SPI-1]



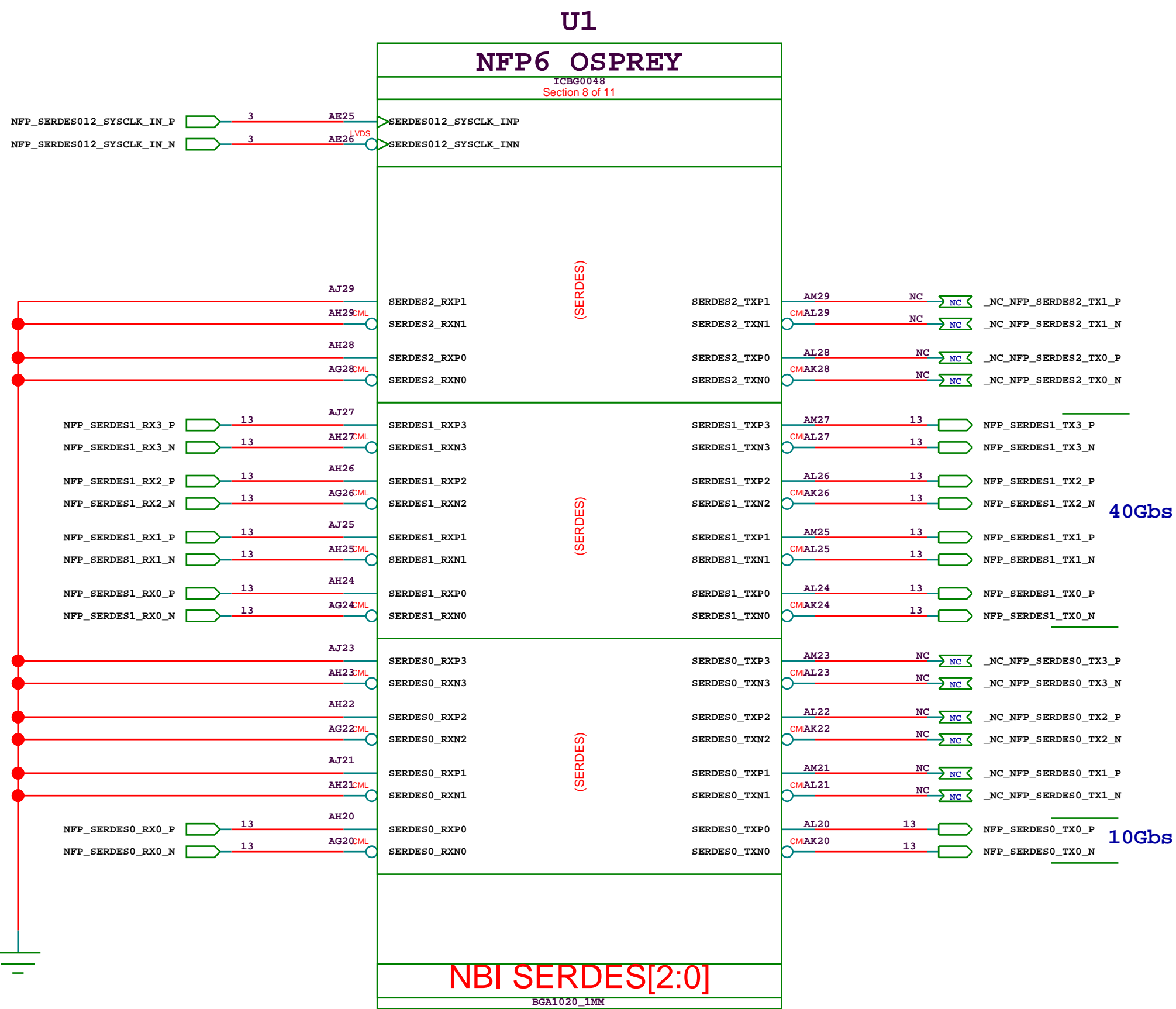
Clock Generator



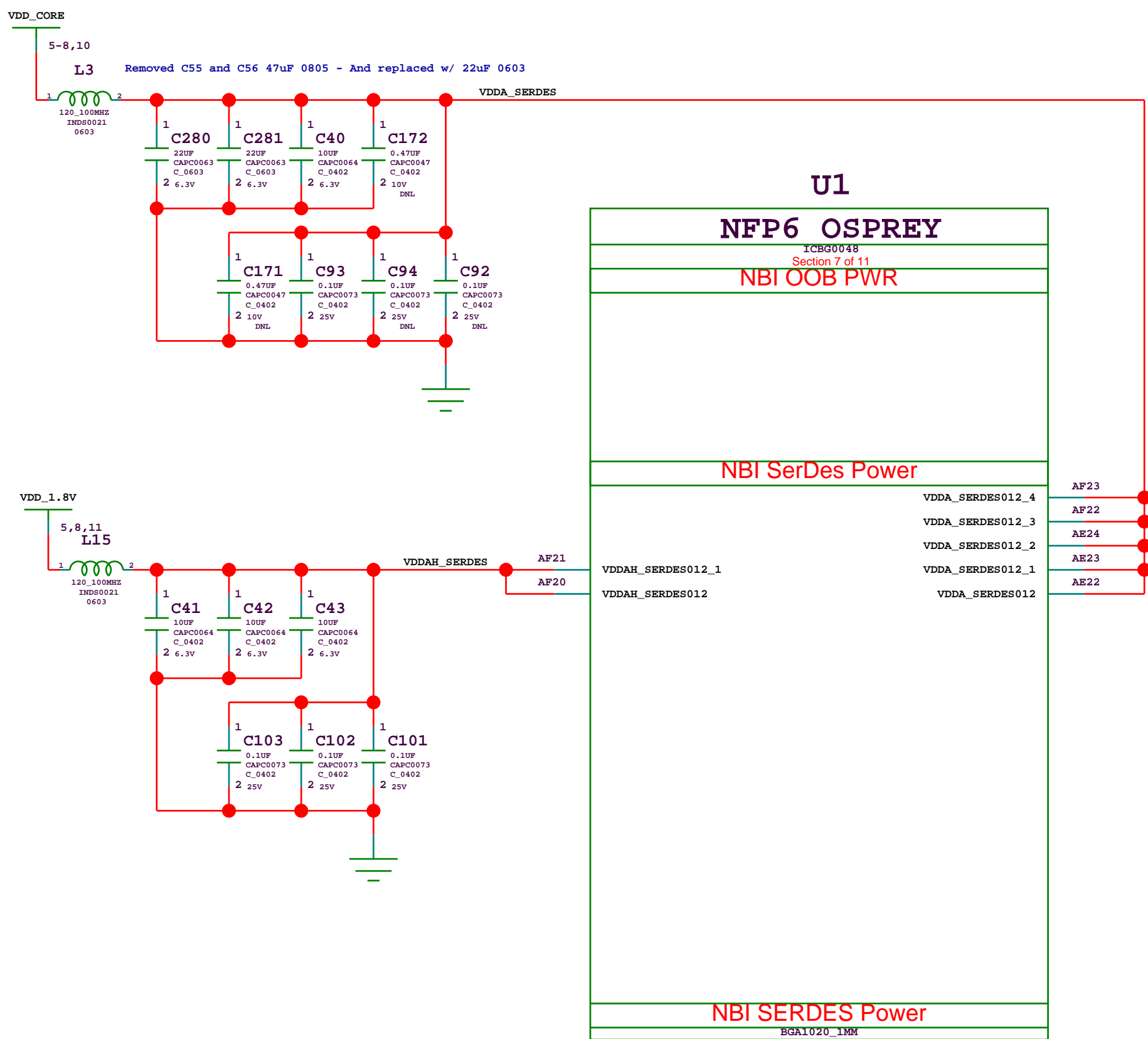
Place Termination Resistors close to DSC400



NFP - Network SerDes & PCIe[0:1] Interfaces

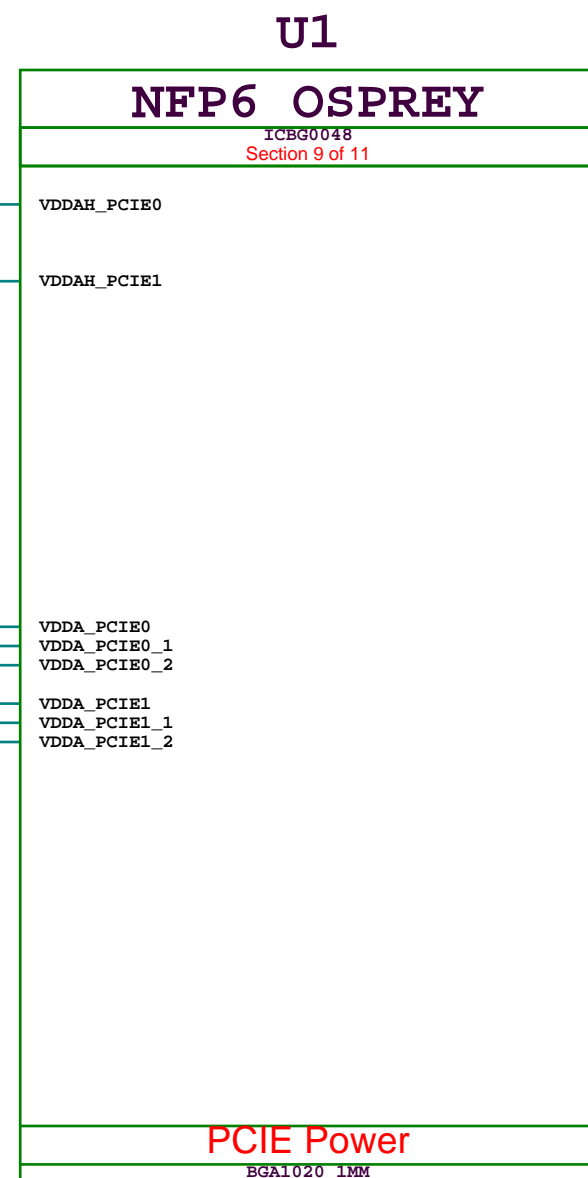


What do you do with RX Channels that not all are used?



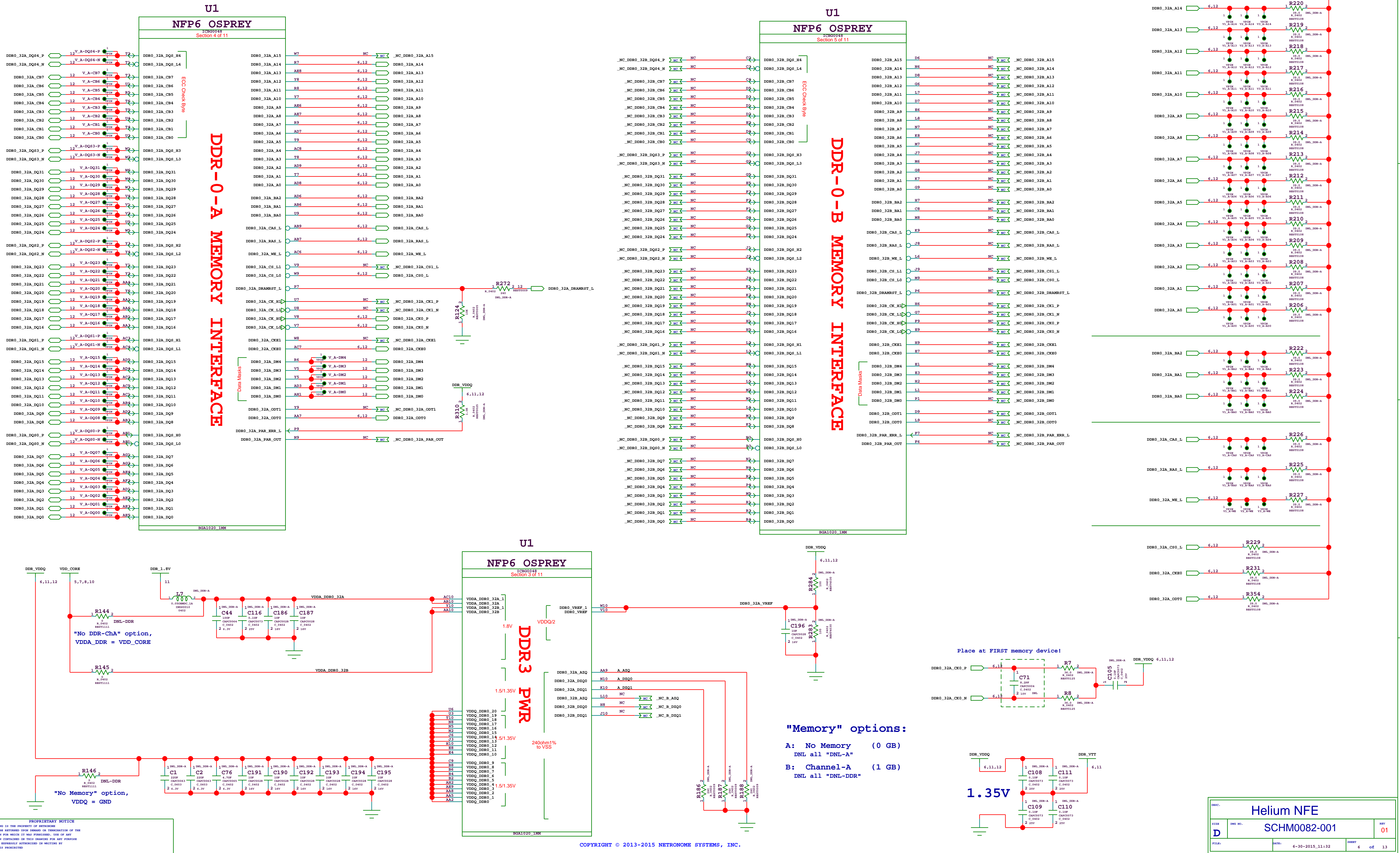
NOTE: Osprey is an "End Point", therefore signal naming convention seems backwards:

- NFP's Transmit: NFP_PCIEx_PER_P/N
- NFP's Receive: NFP_PCIEx_PET_P/N

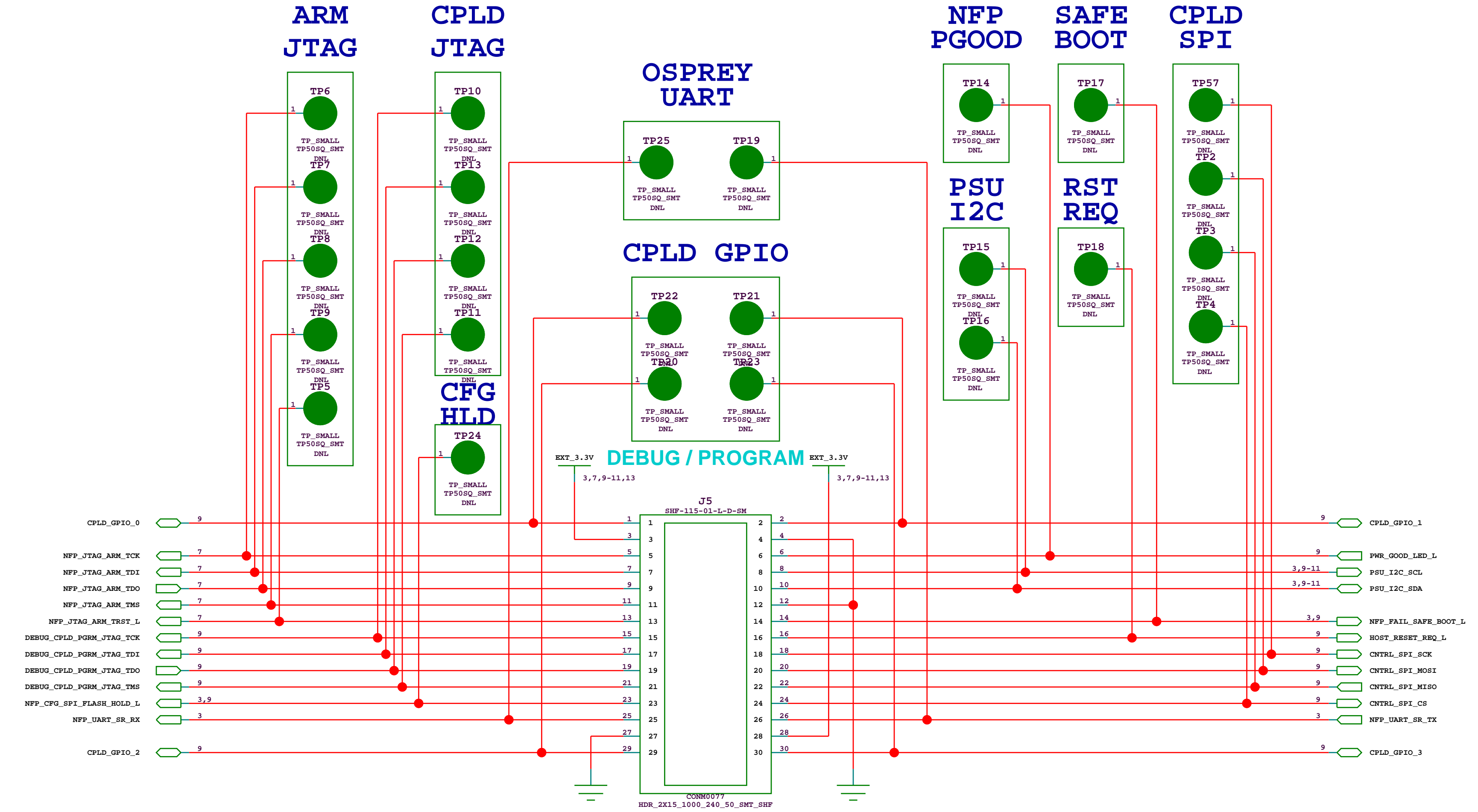
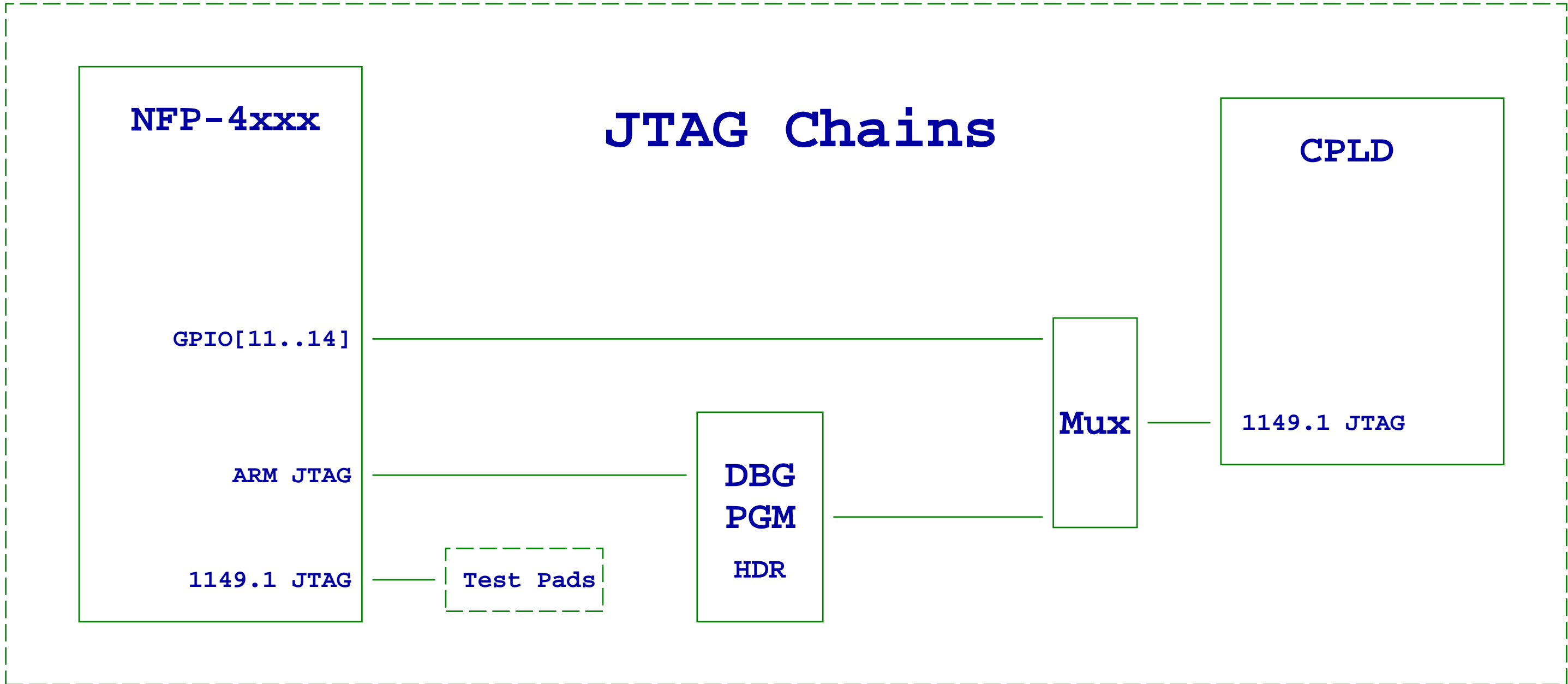
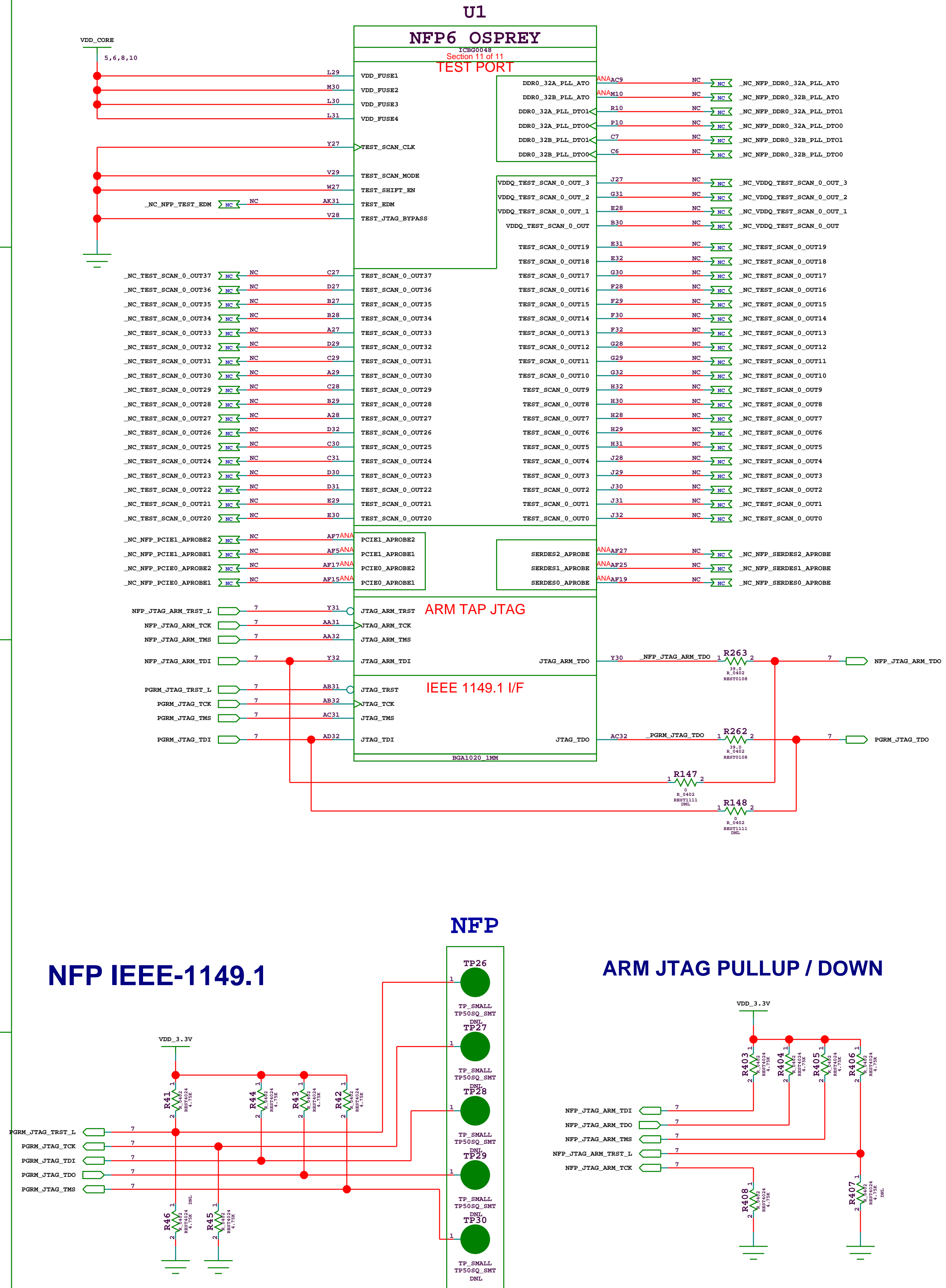


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NFP - DDR0_32A/B Block



NFP - Test / JTAG / Debug



NOTE: ALL TEST POINTS SHOULD BE PLACED ON THE BOTTOM SIDE OF THE BOARD EXCEPT TP14-16, TP20-23

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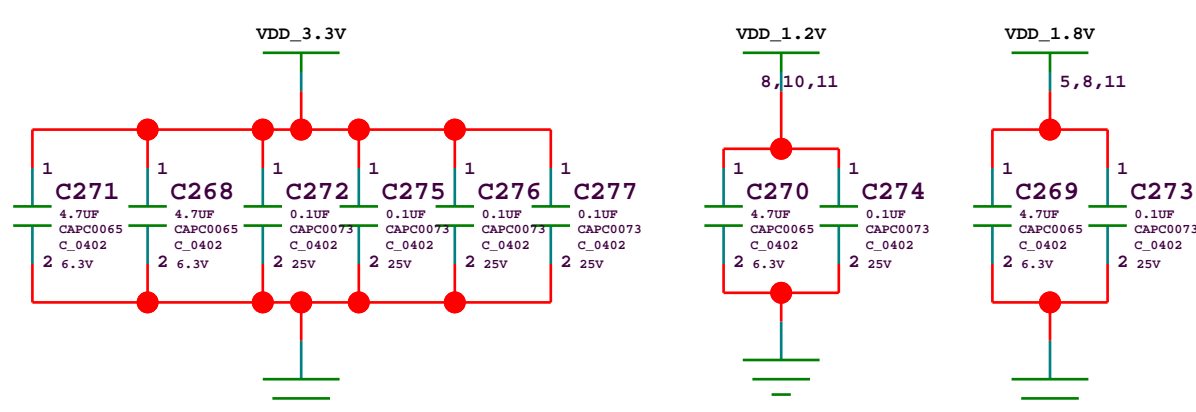
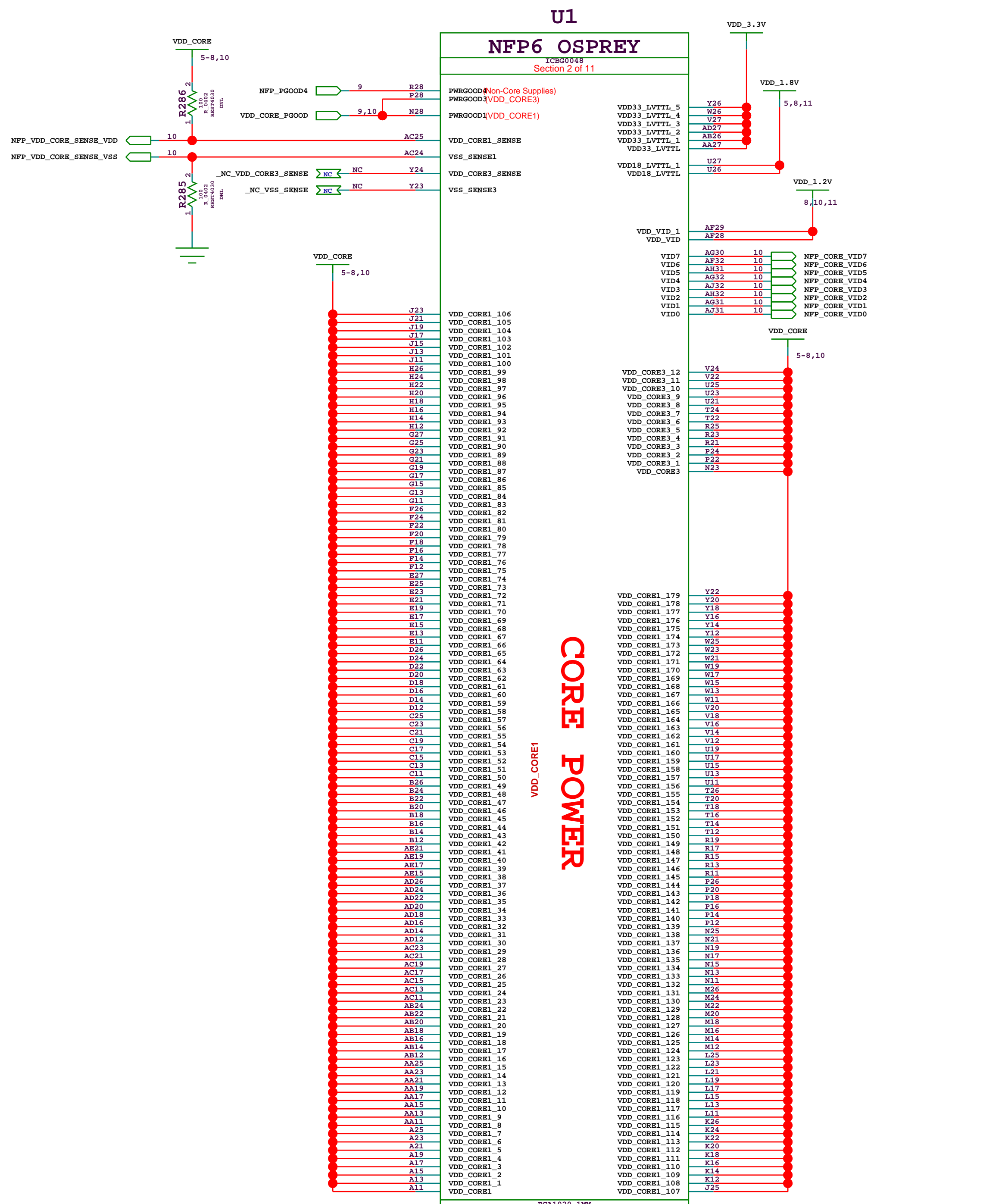
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DESC:	Helium NFE		
SIZE	DWG NO.	SCHM0082-001	REV 01
FILE:	DATE:	6-30-2015_11:32	SHEET 7 of 13

NFP - Power Block, Mounting Holes

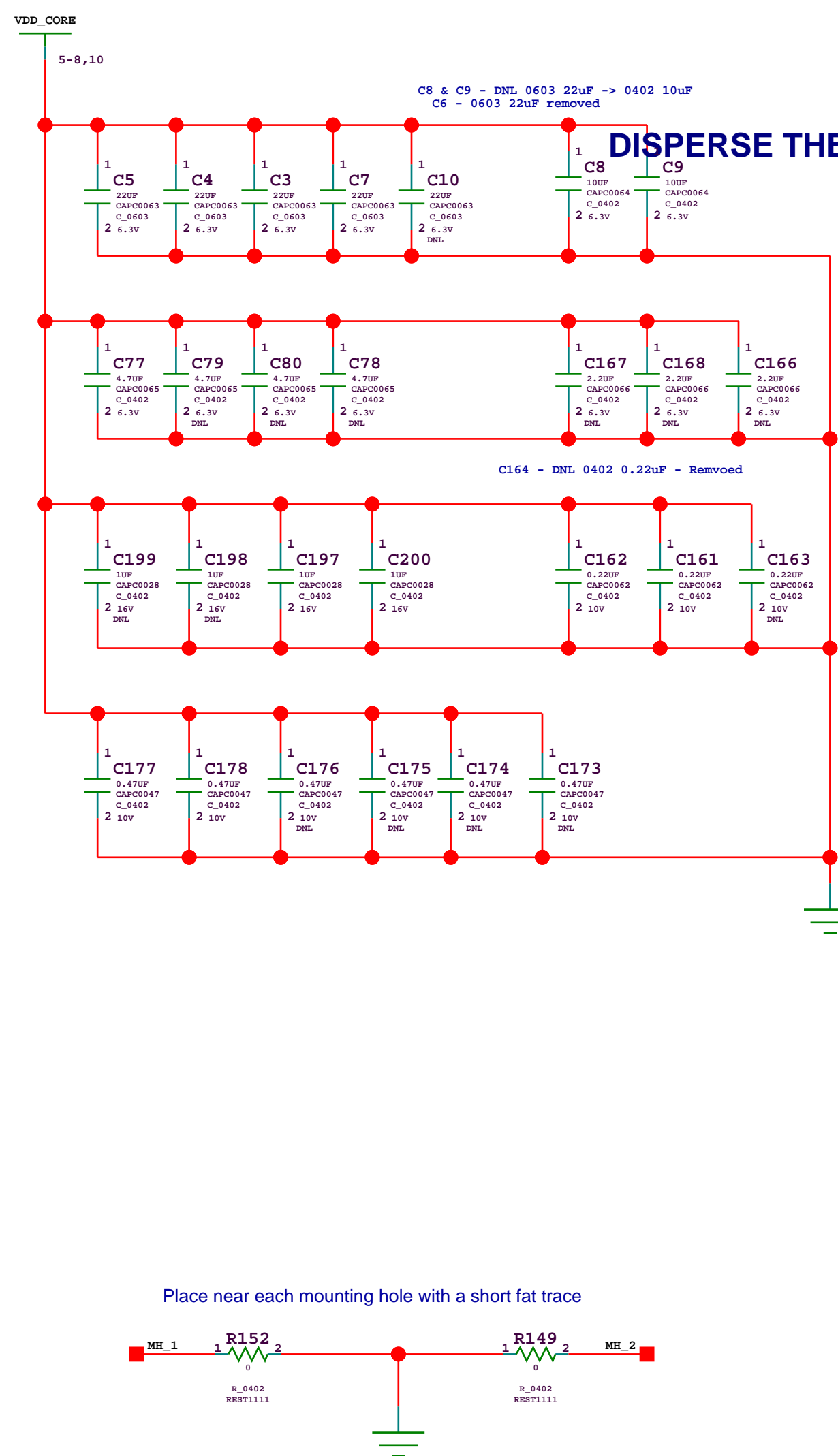
PLACE ON NFP_VDD_CORE & GND IN CENTER OF BGA FIELD

ROUTE NFP_VDD_CORE_SENSE_VDD/VSS as diff pair using 20mil traces from U1 core to UDPM1

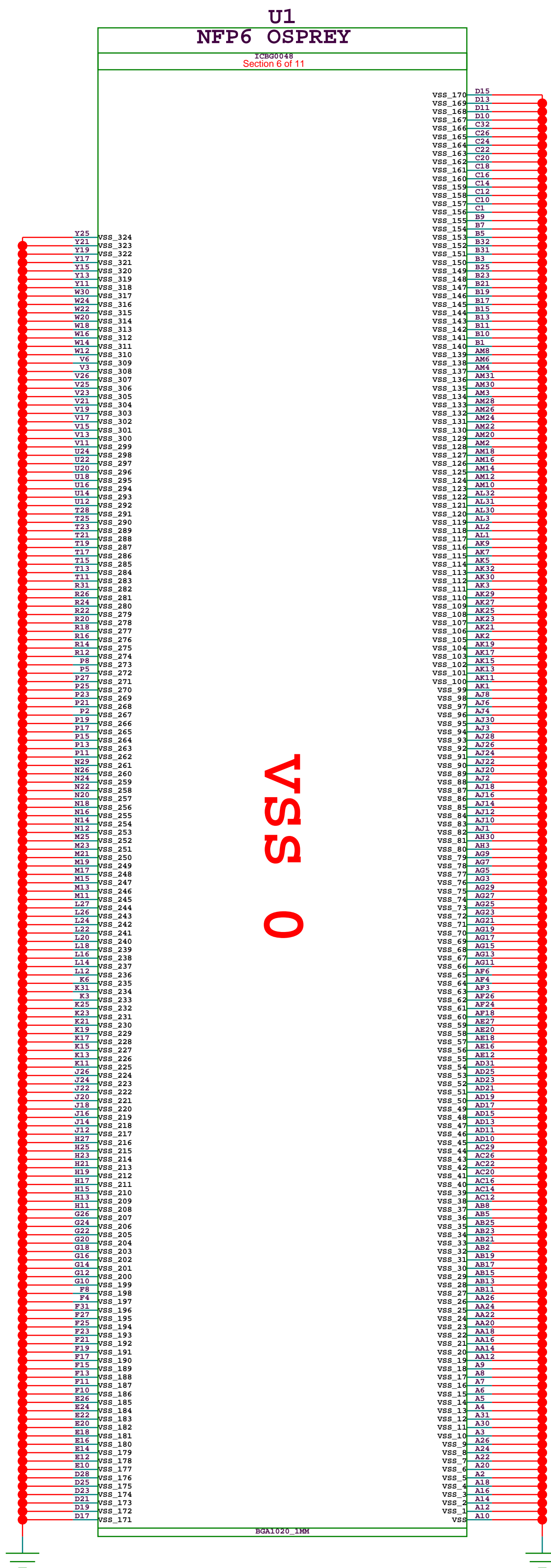


BYPASS CAPS

PLACE IN BGA FIELD



PLACE IN BGA FIELD



VS O

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DESC.			
Helium NFE			
SER	DMG NO.	SCHM0082-001	REV 01
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CPLD - NFE System Management

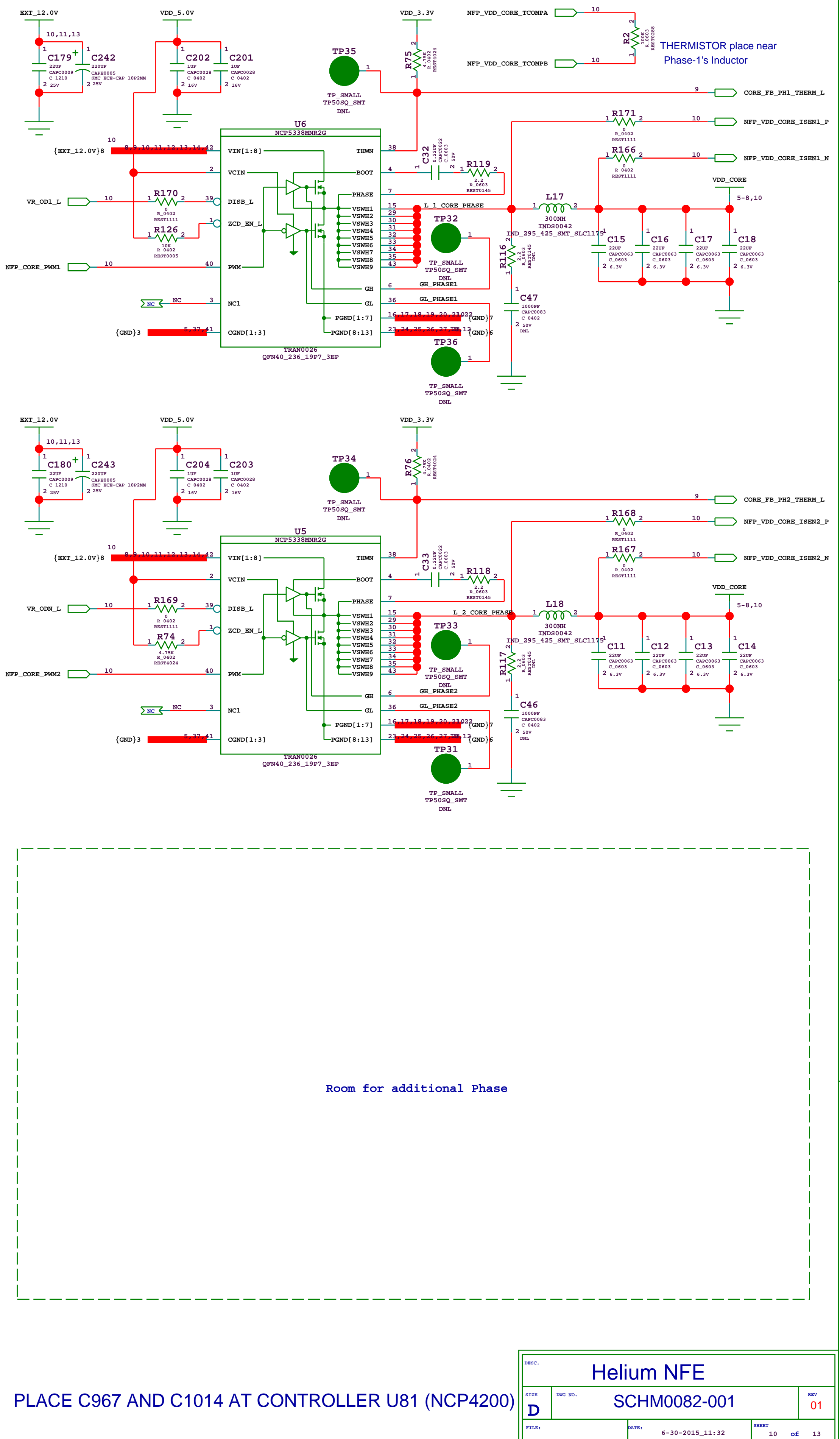
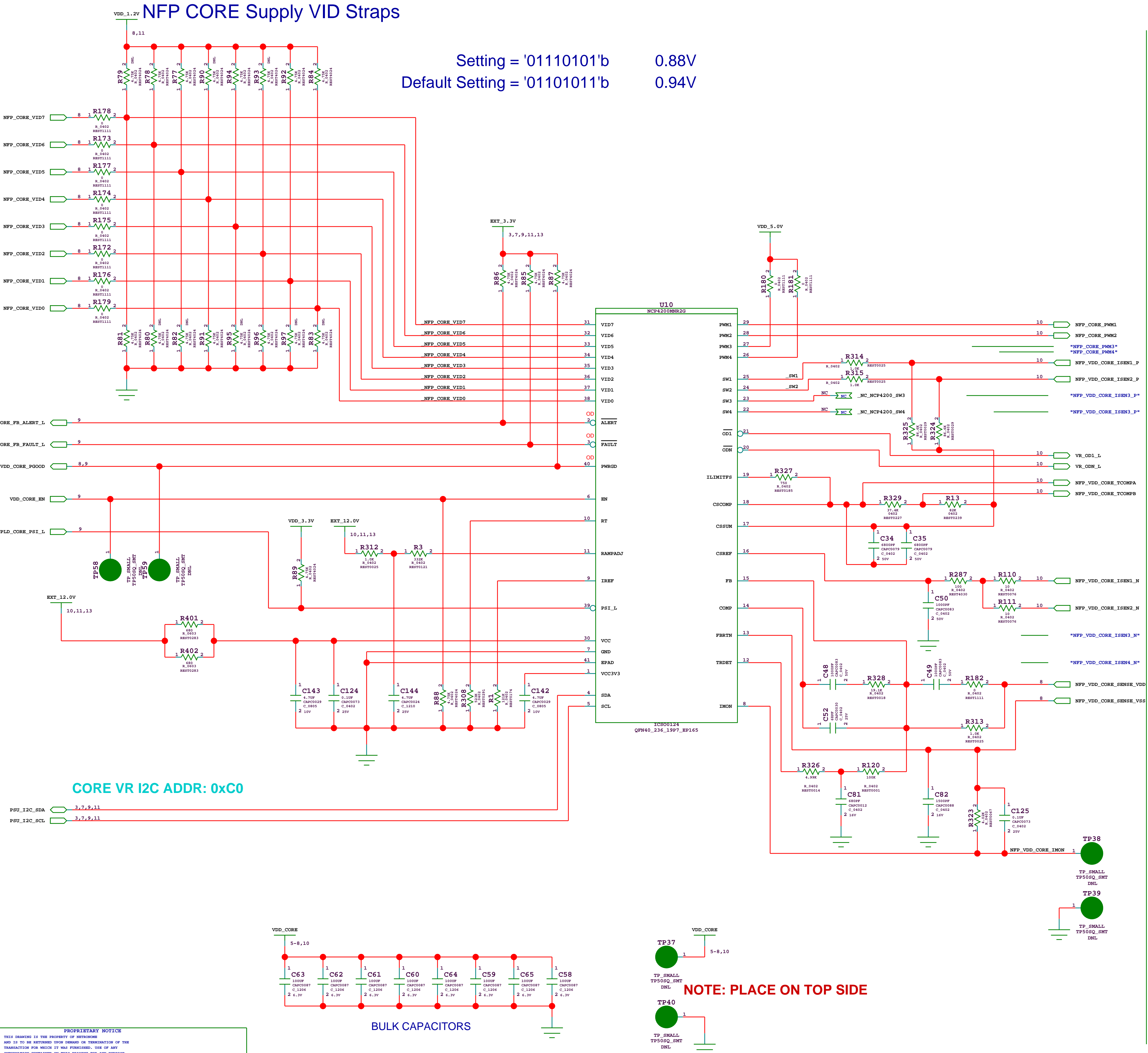


Power - NFP Core

NFP CORE Supply VID Straps

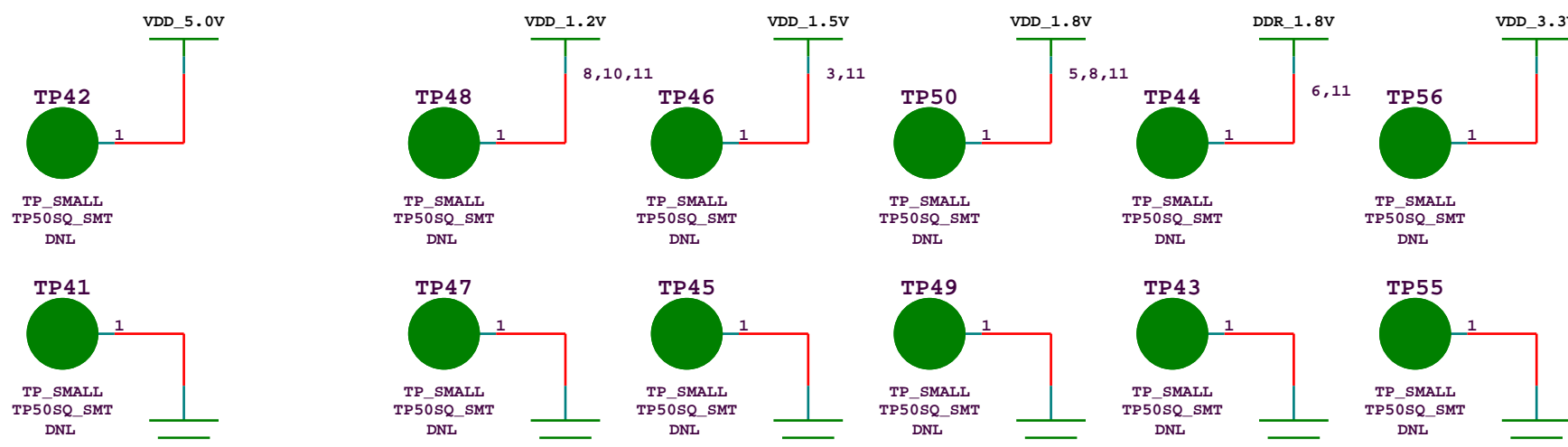
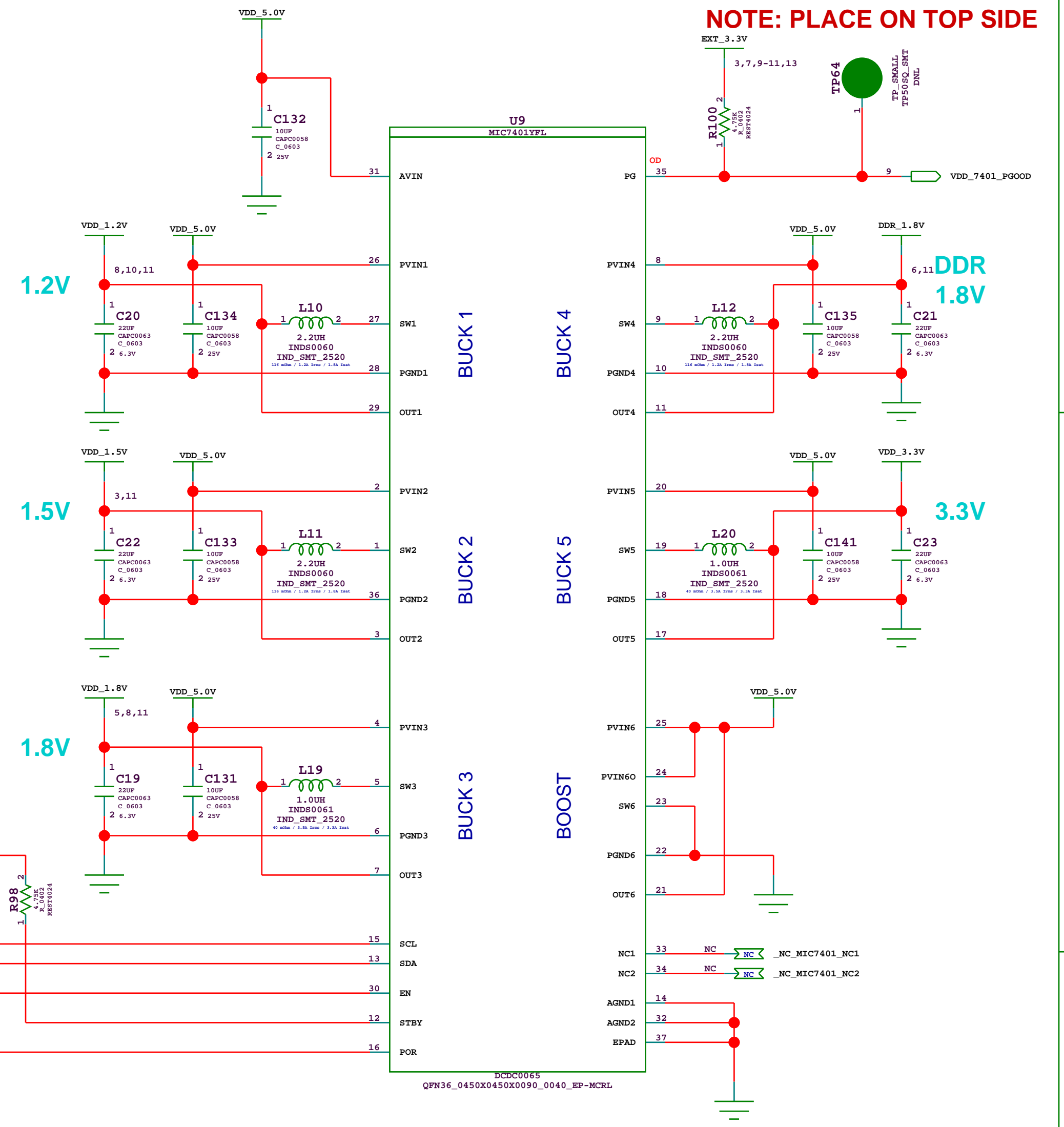
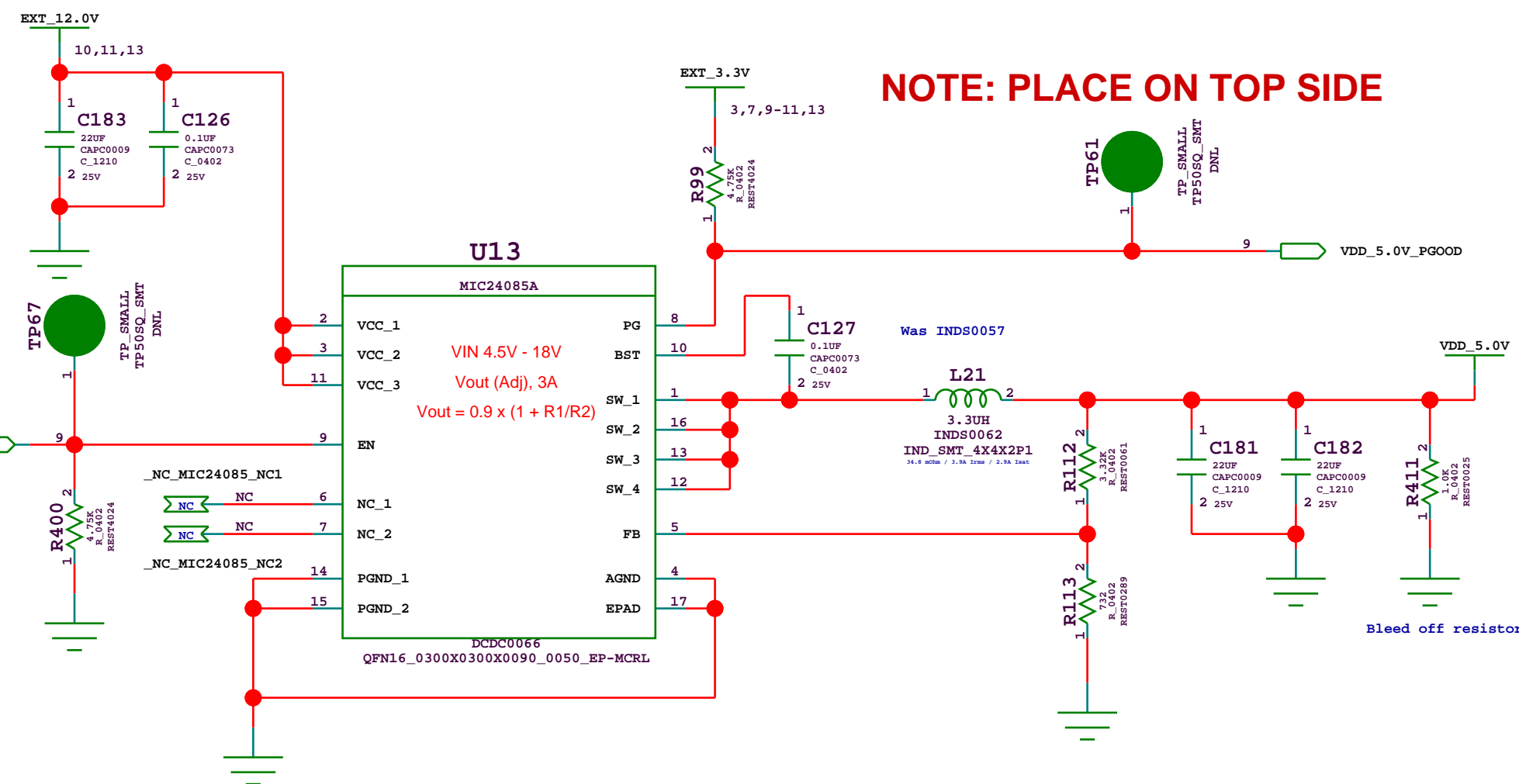
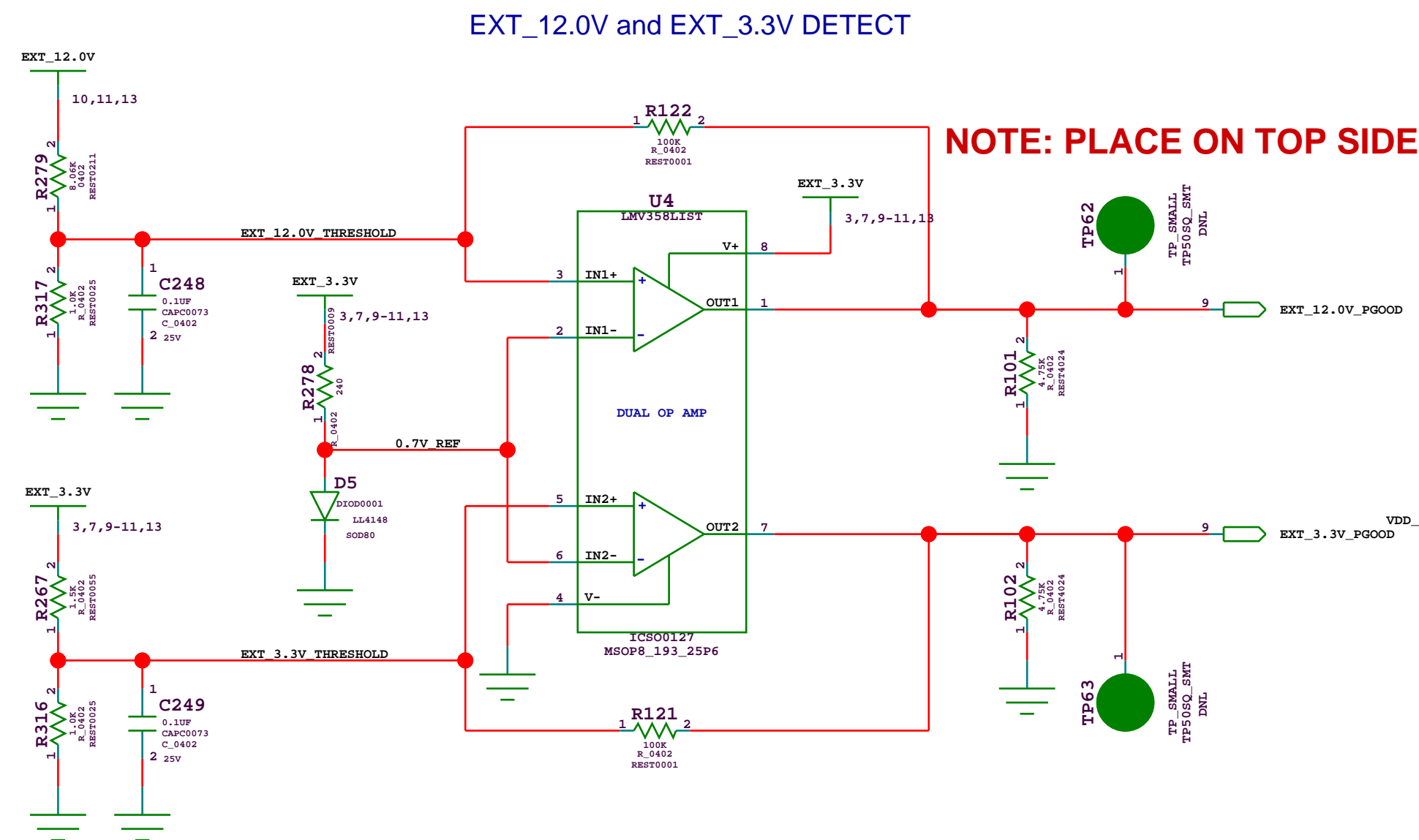
Setting = '01110101'b
Default Setting = '01101011'b

0.88V
0.94V

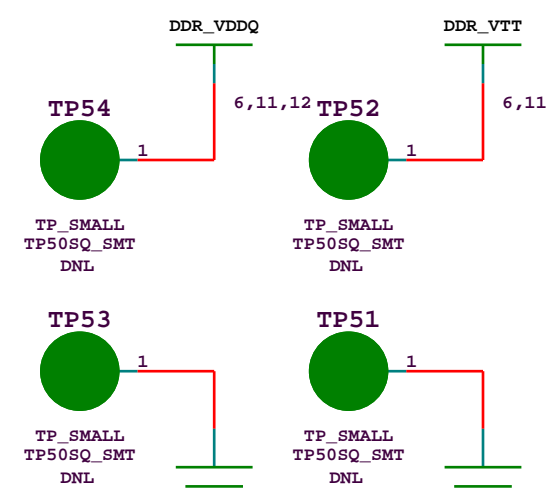
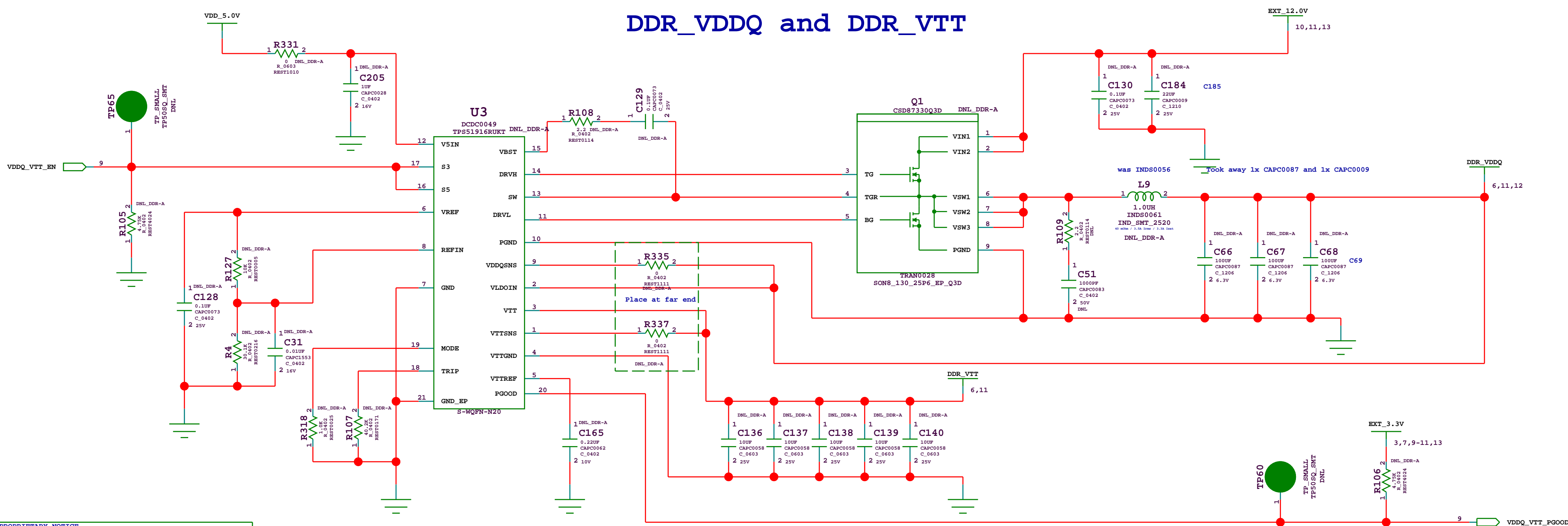


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Power - 5V, 3.3V, 1.8V, 1.5V, 1.2V, DDR



DDR_VDDQ and DDR_VTT



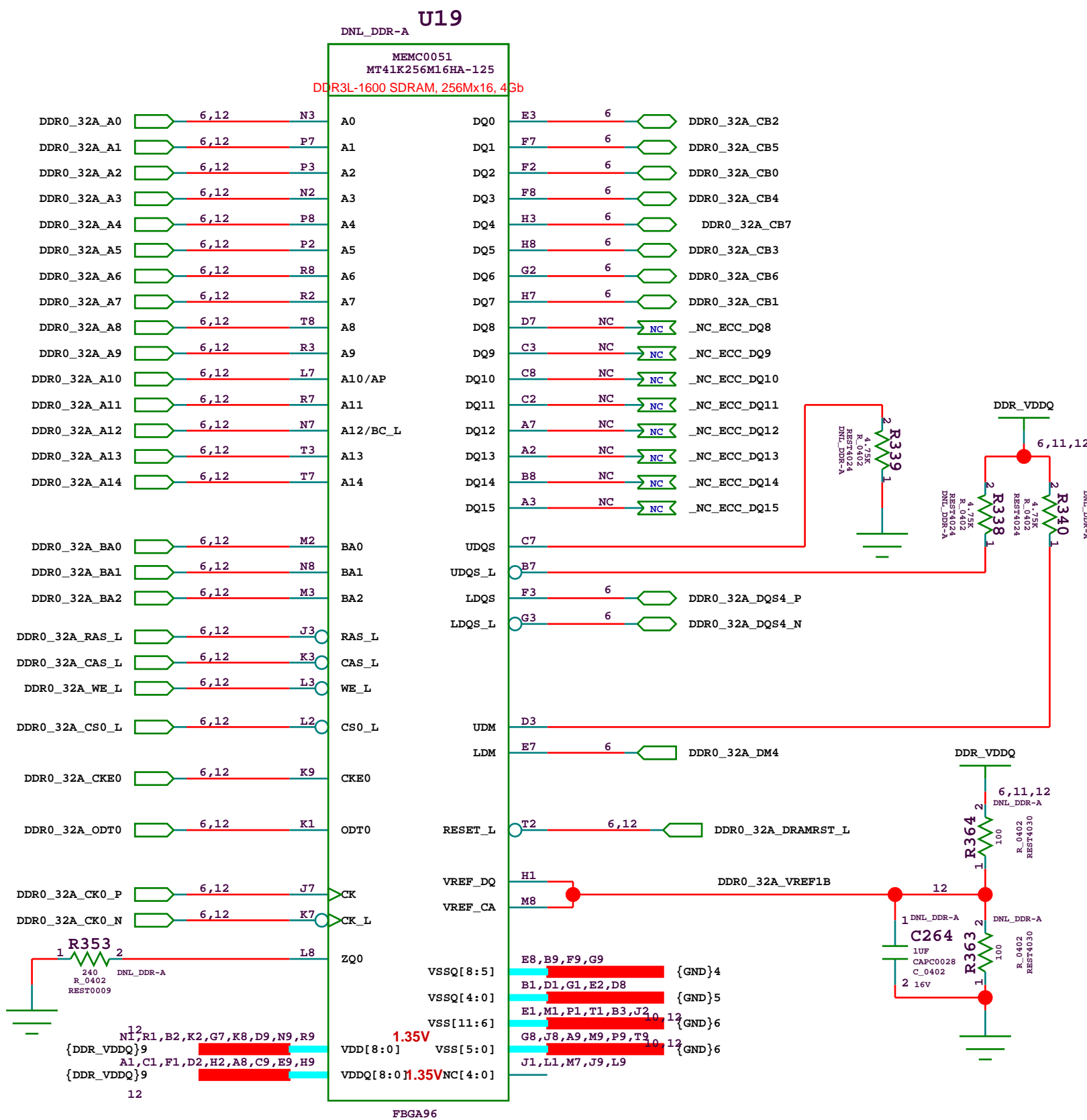
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SIZE		DMG NO.				REV	
D		SCHM0082-001				01	
FILE:		DATE:		SHEET			
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DDR-0

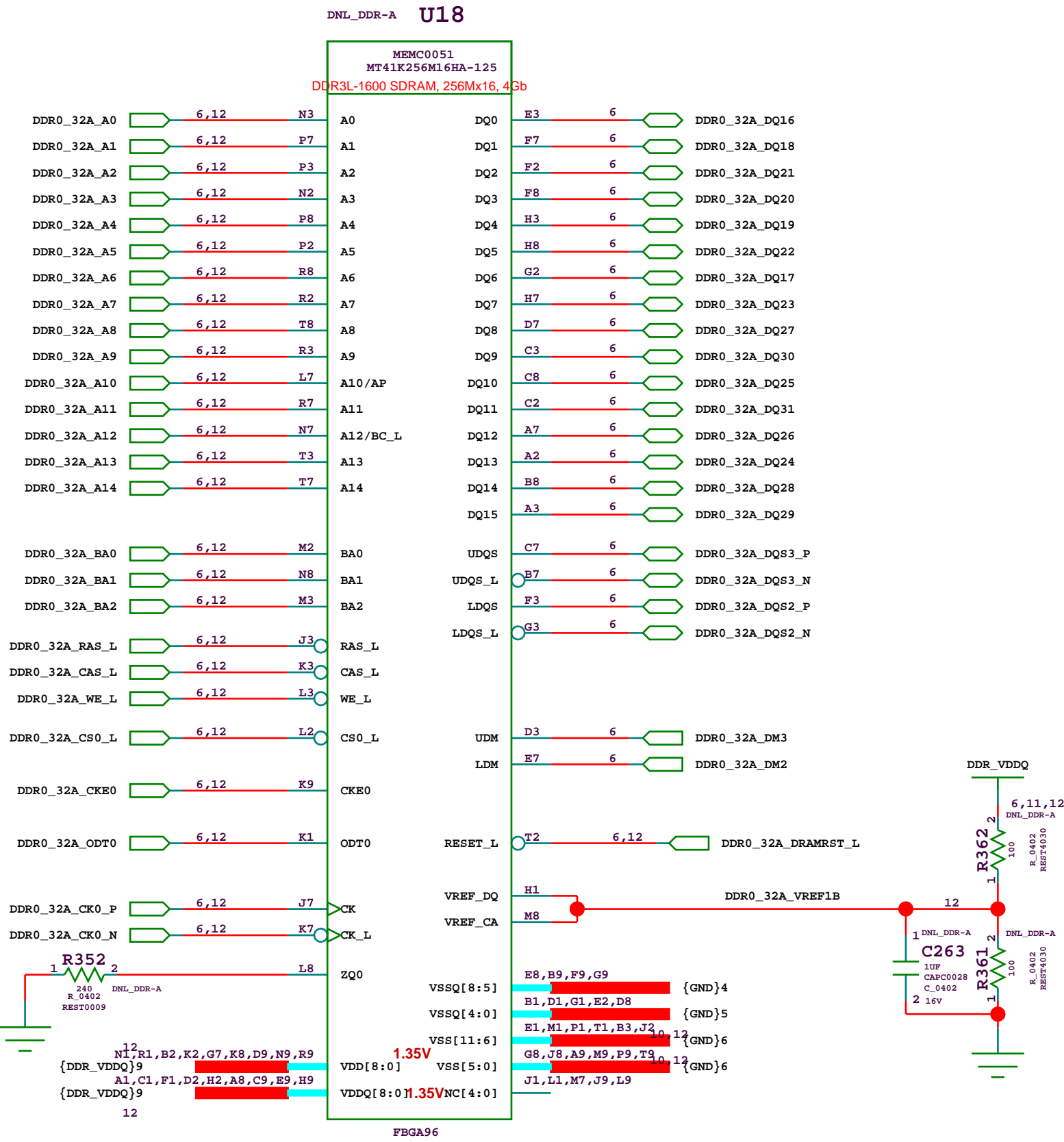
DDR3 - DDR-0 Channel A

Ch-A

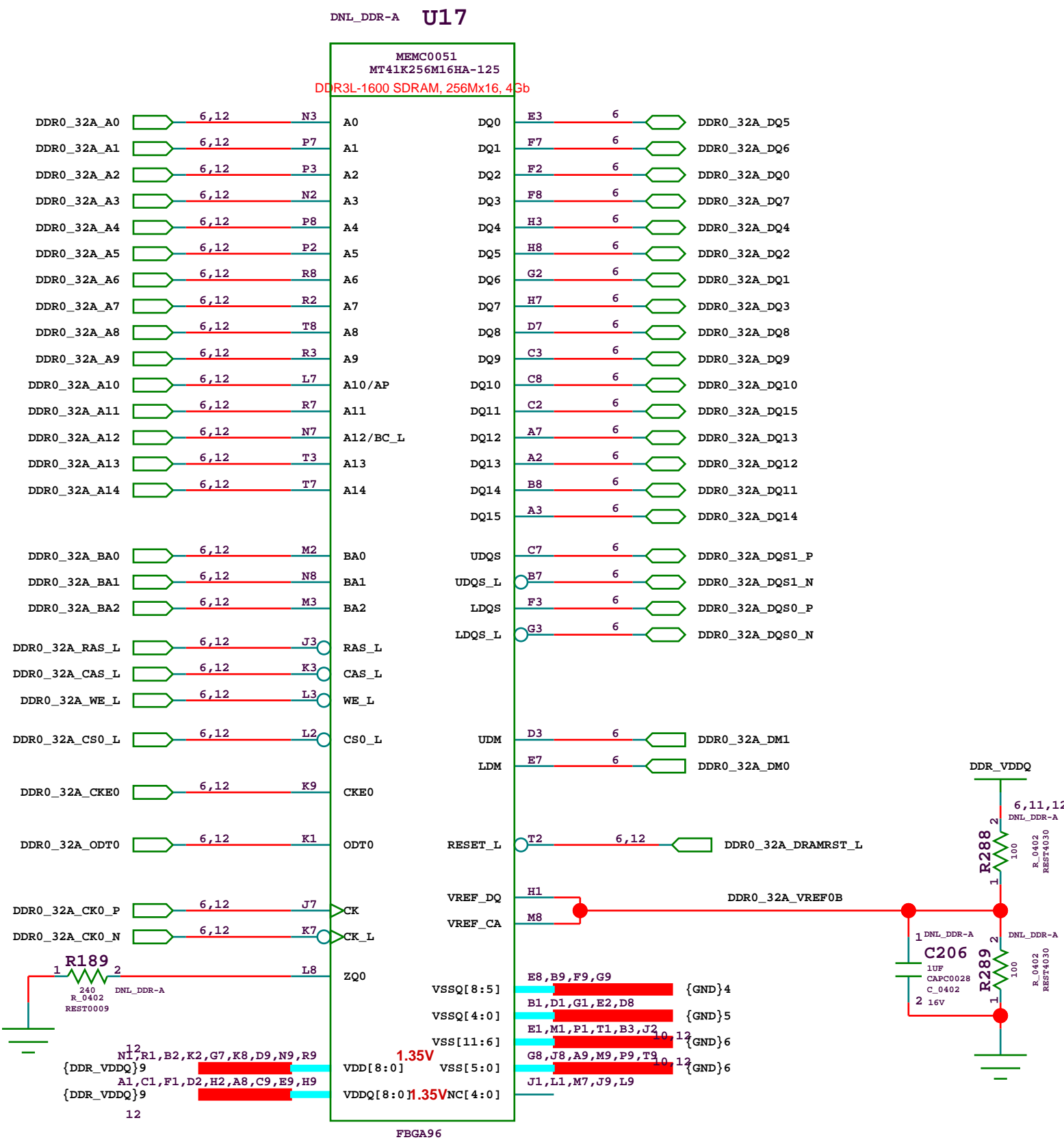
CB[7:0] - Bot
Device 2



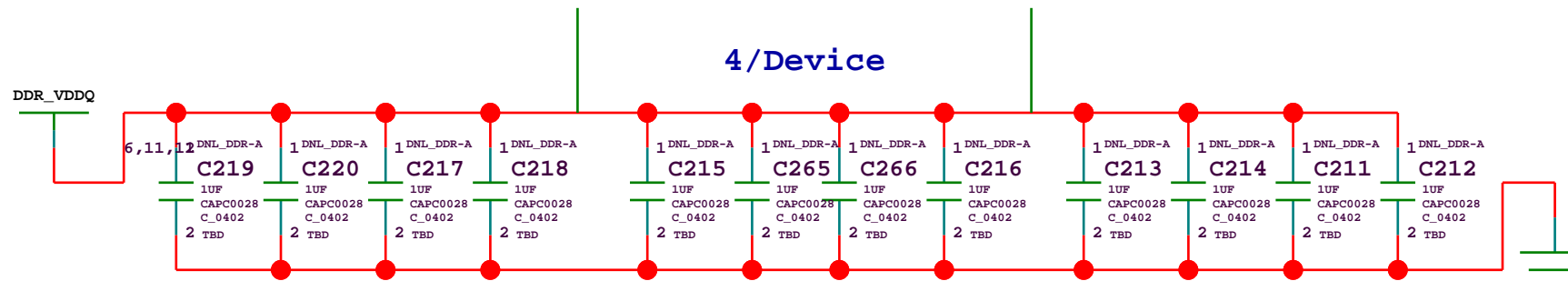
DQ[31:16]
Device 1



DQ[15:0]
Device 0



Single-ranked DDR3 Memory [CS0_L]

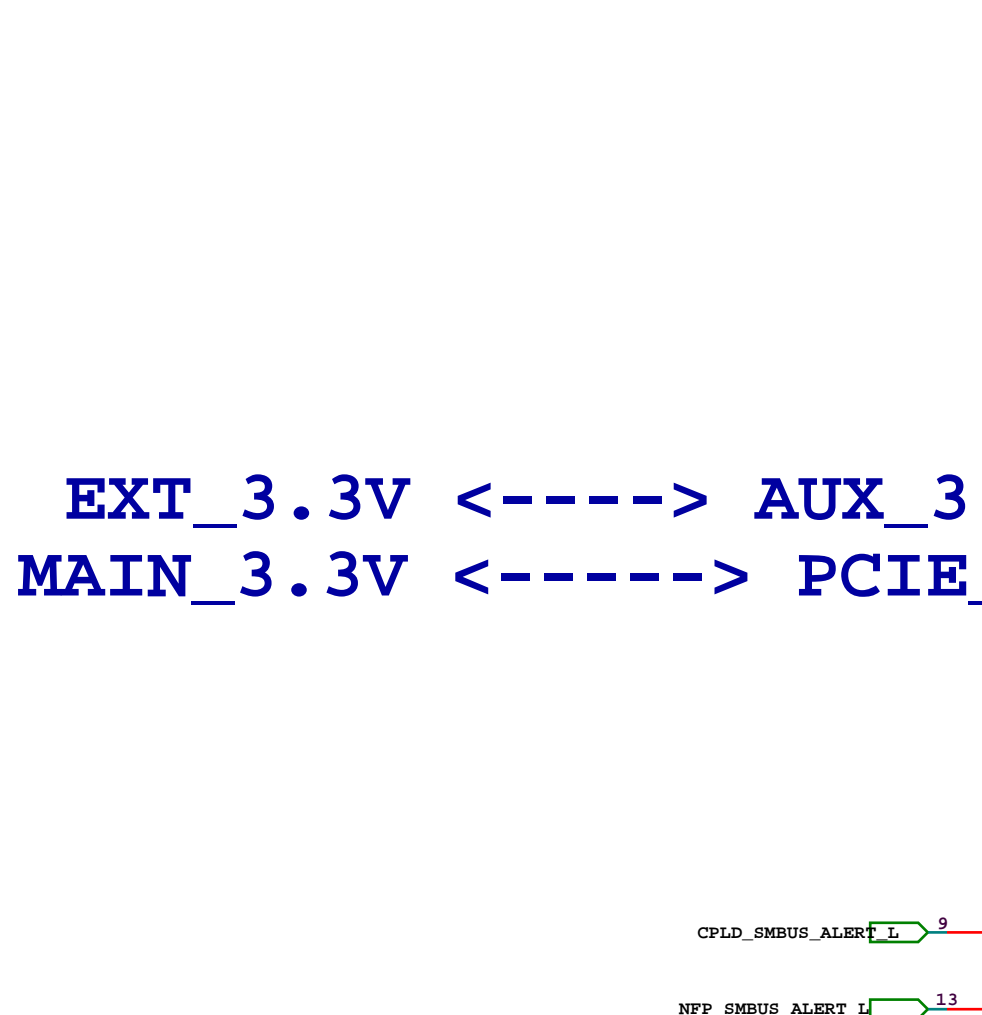
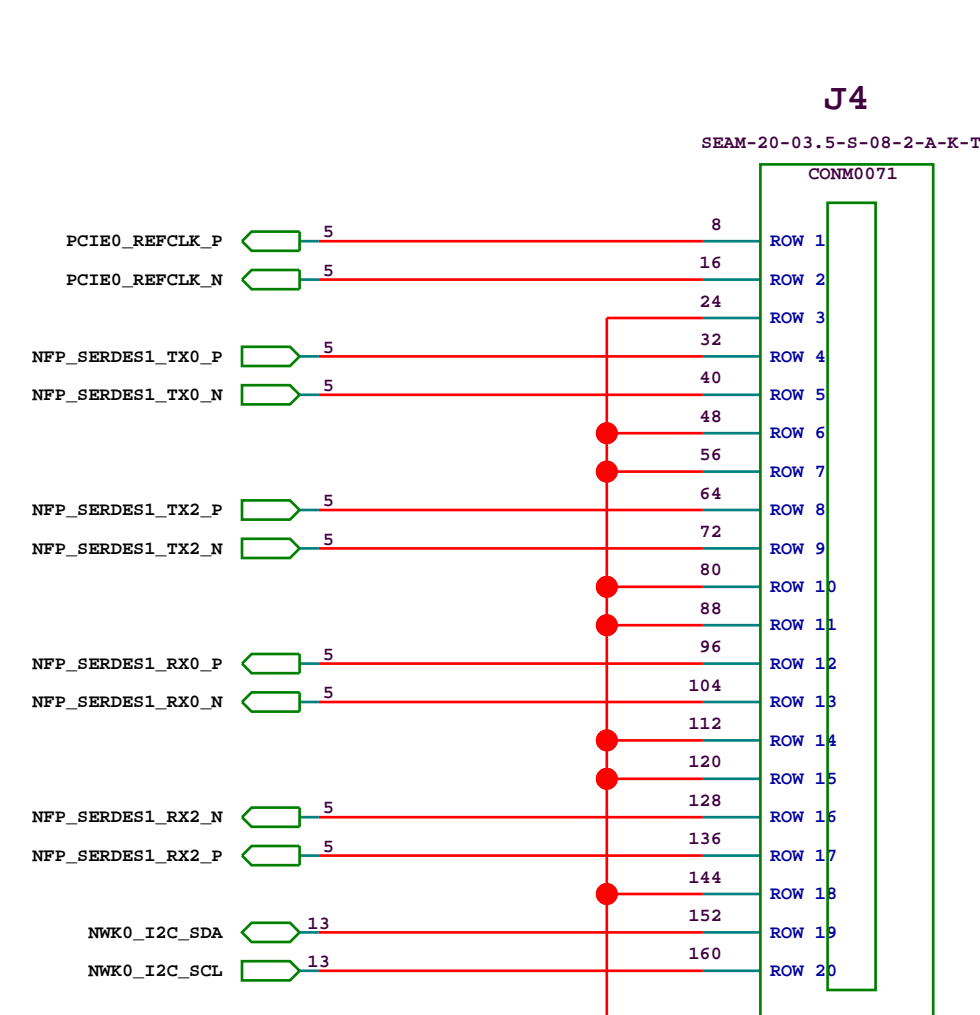
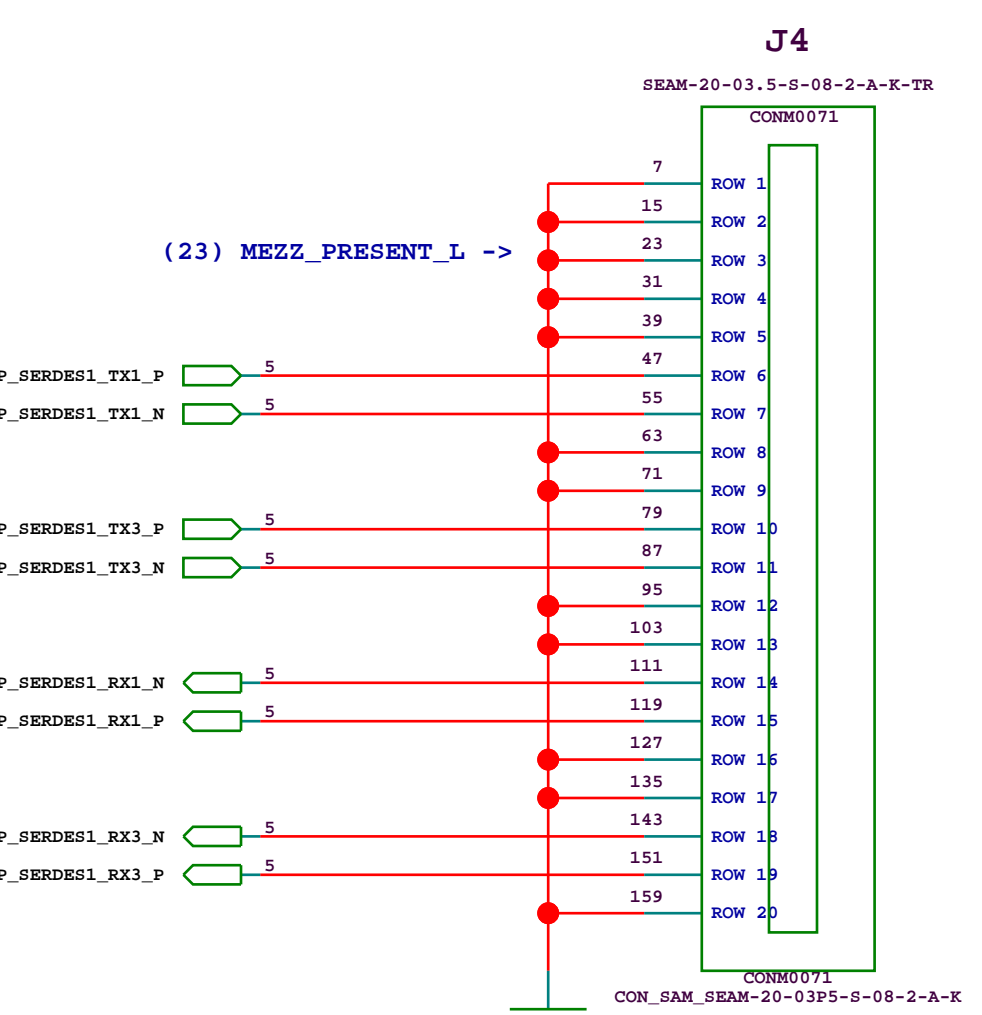
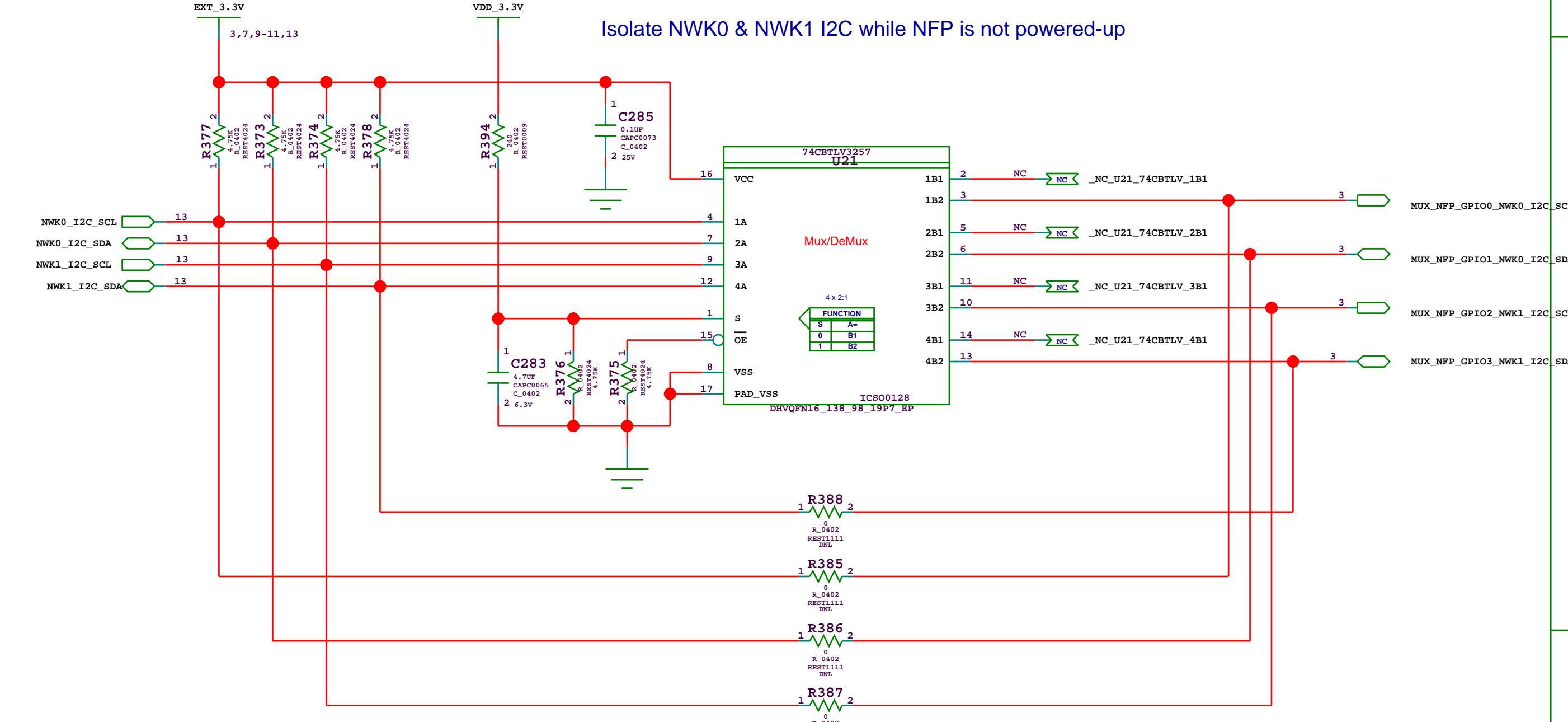
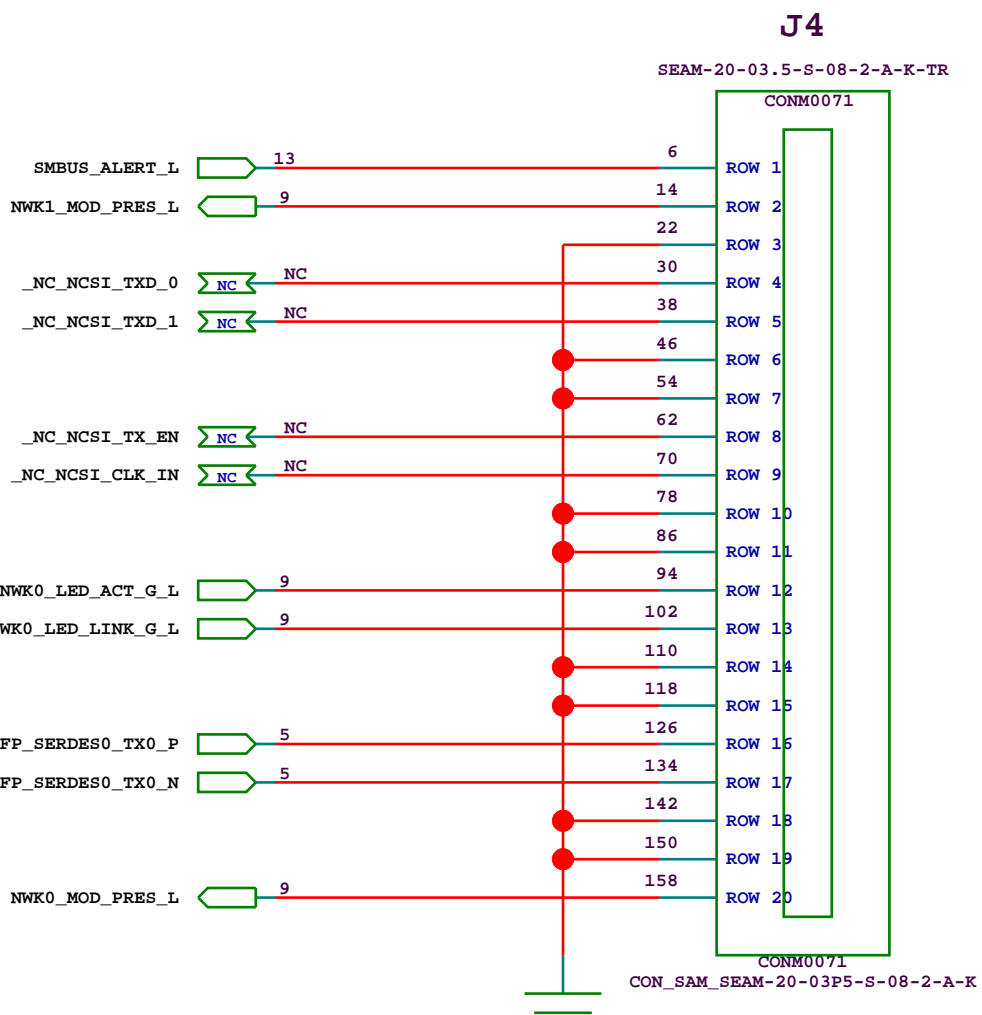
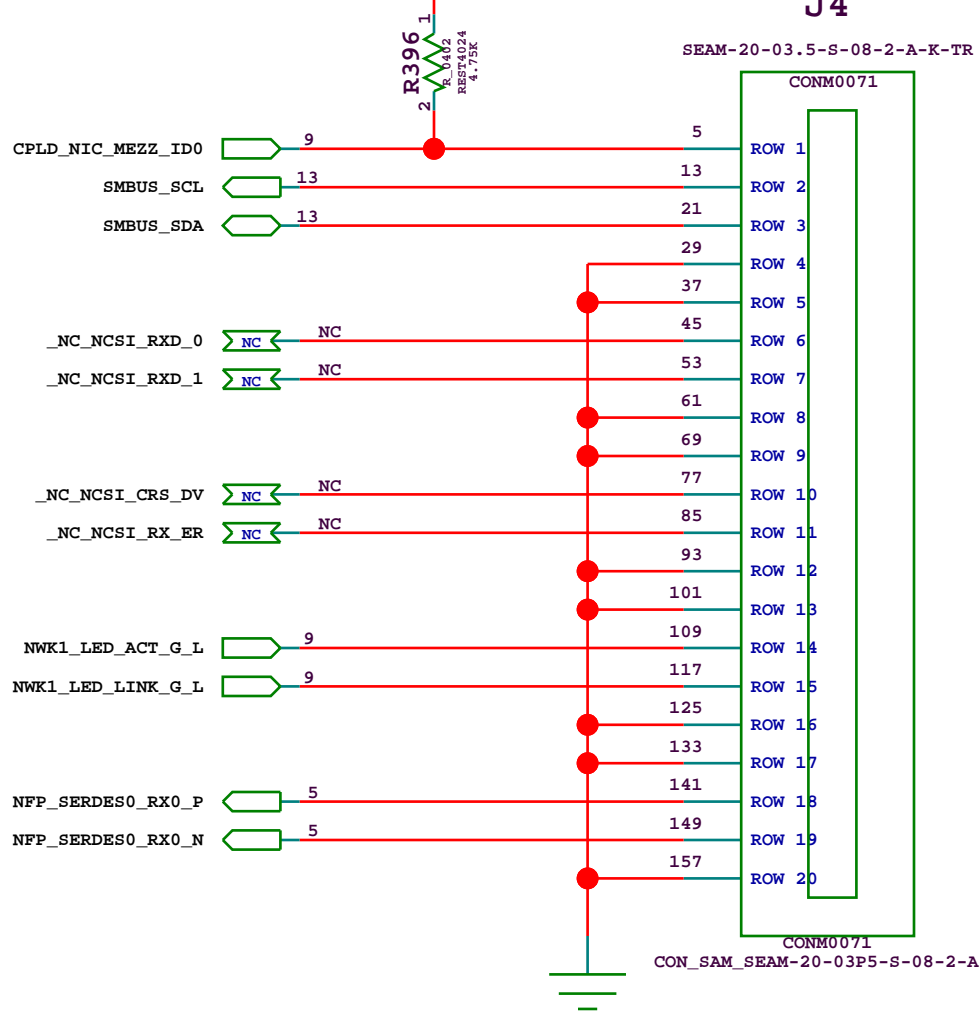
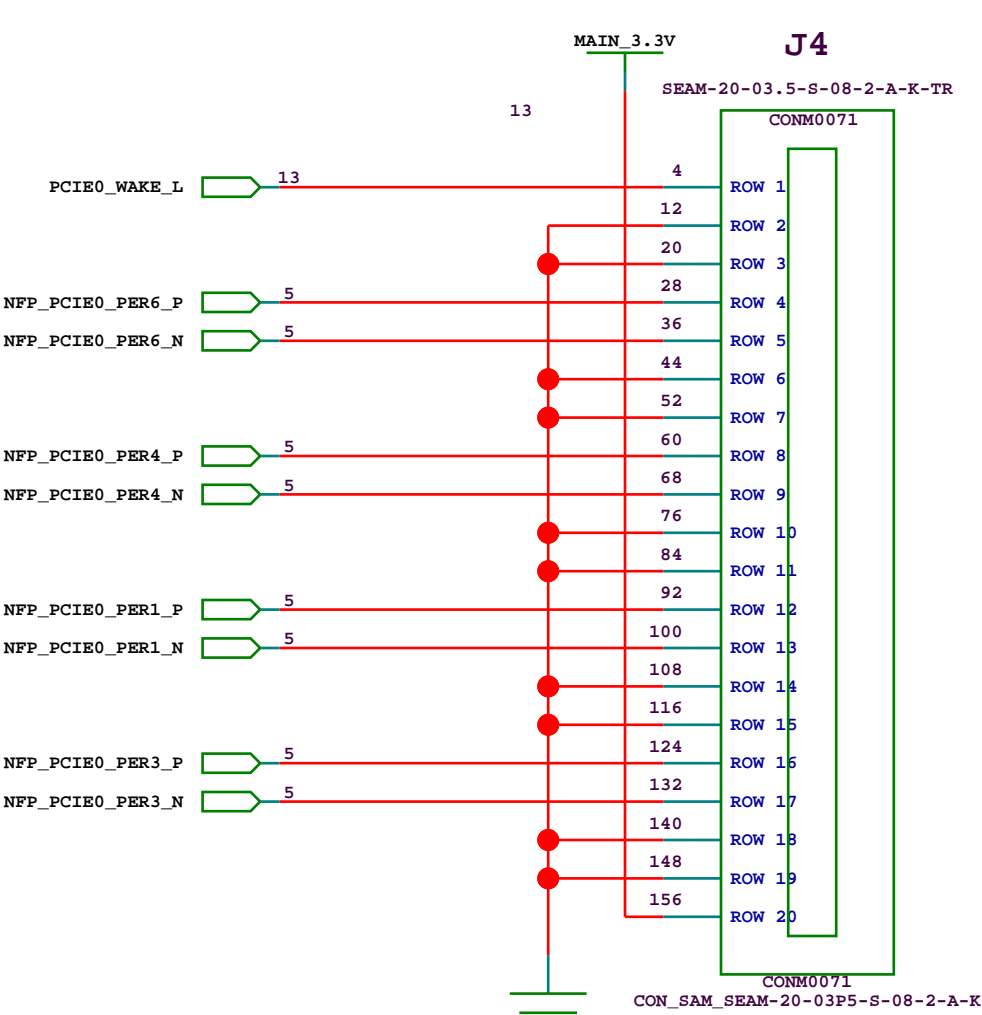
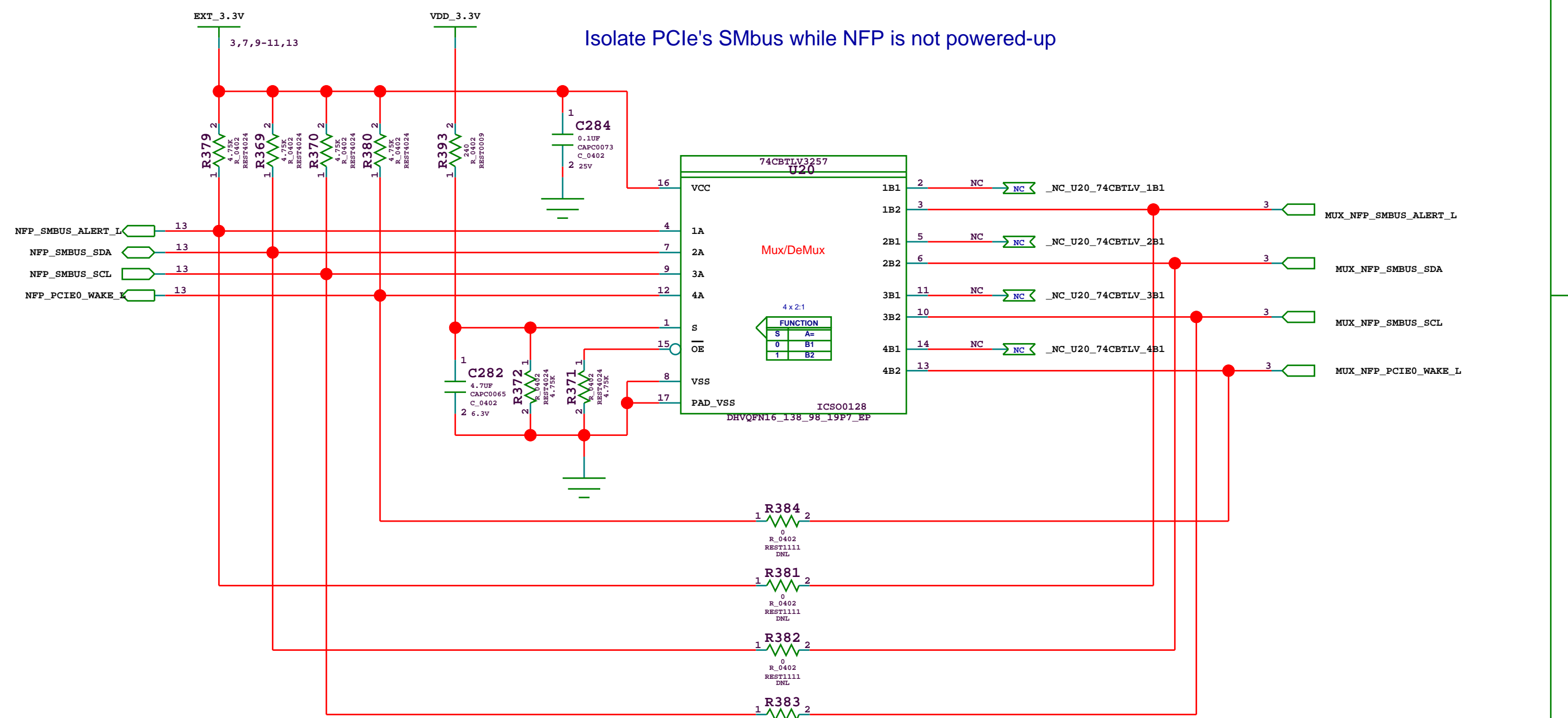
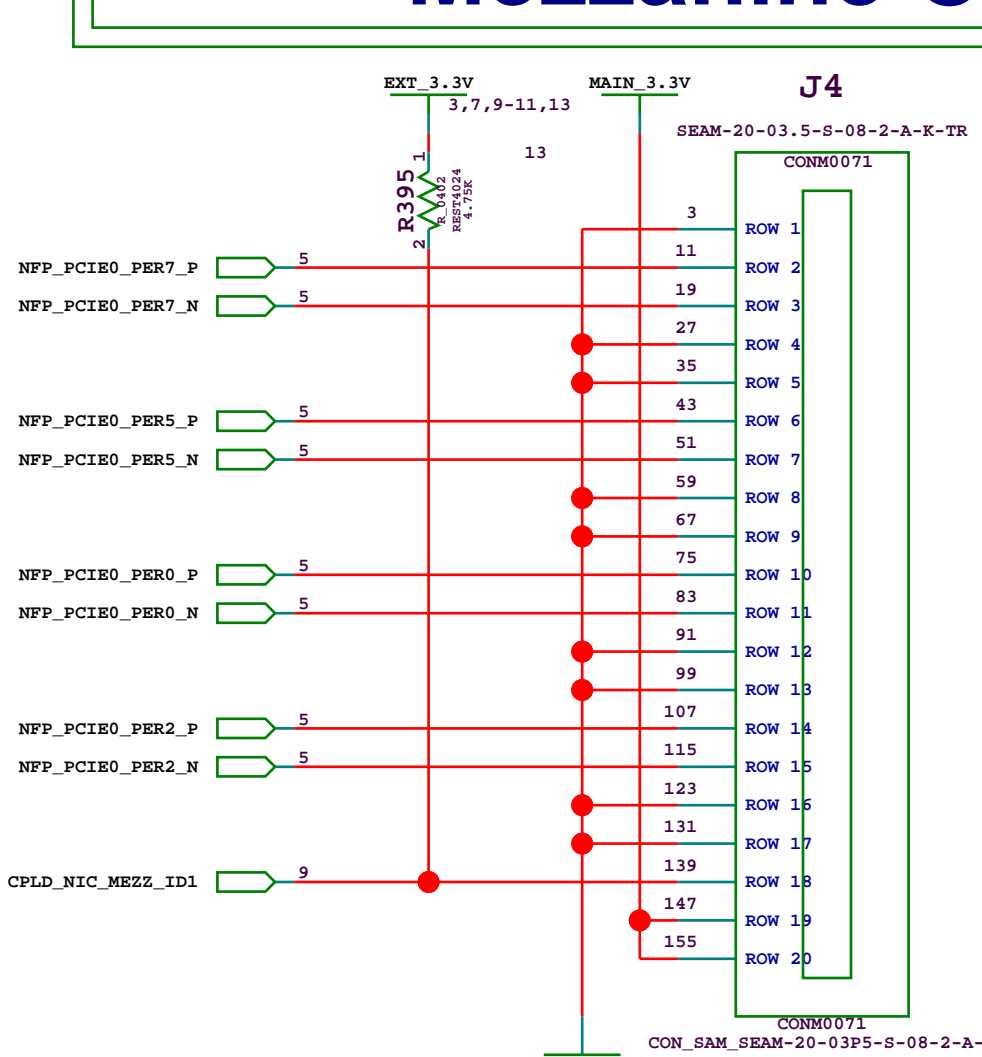
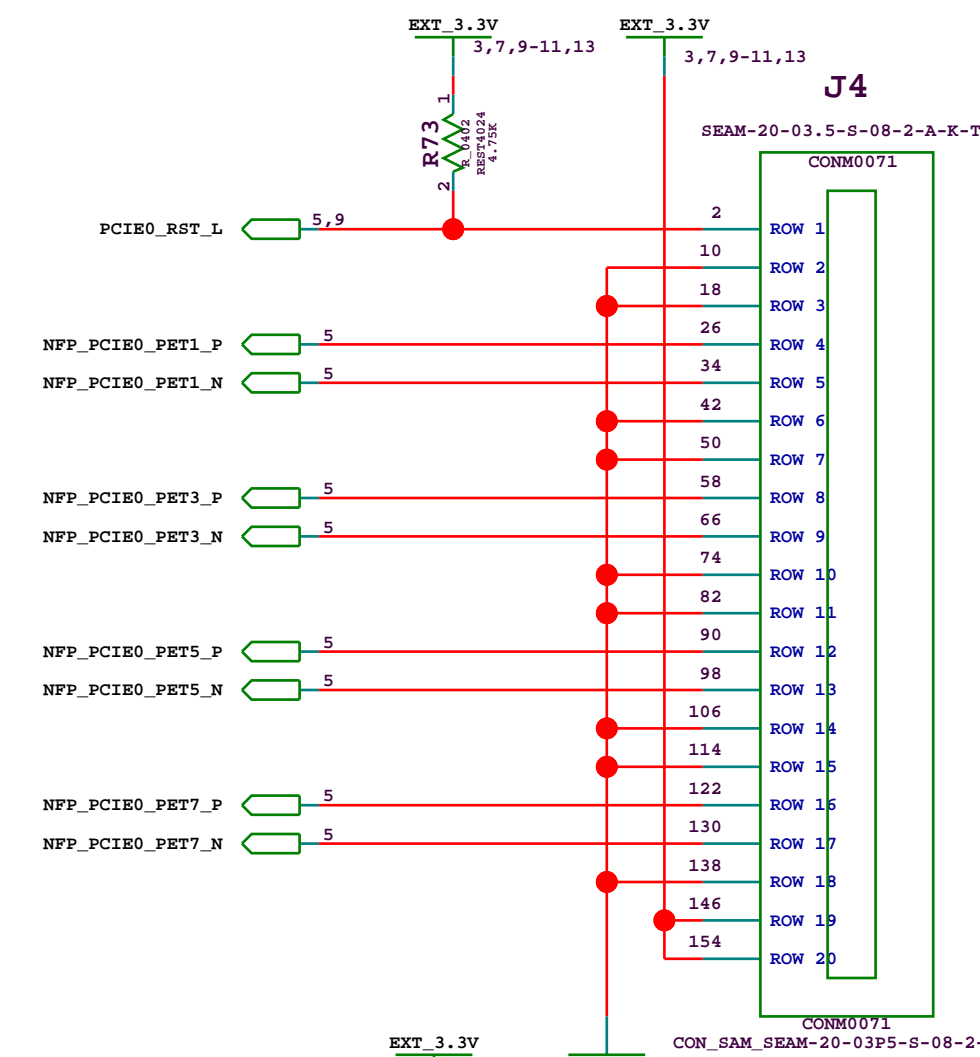
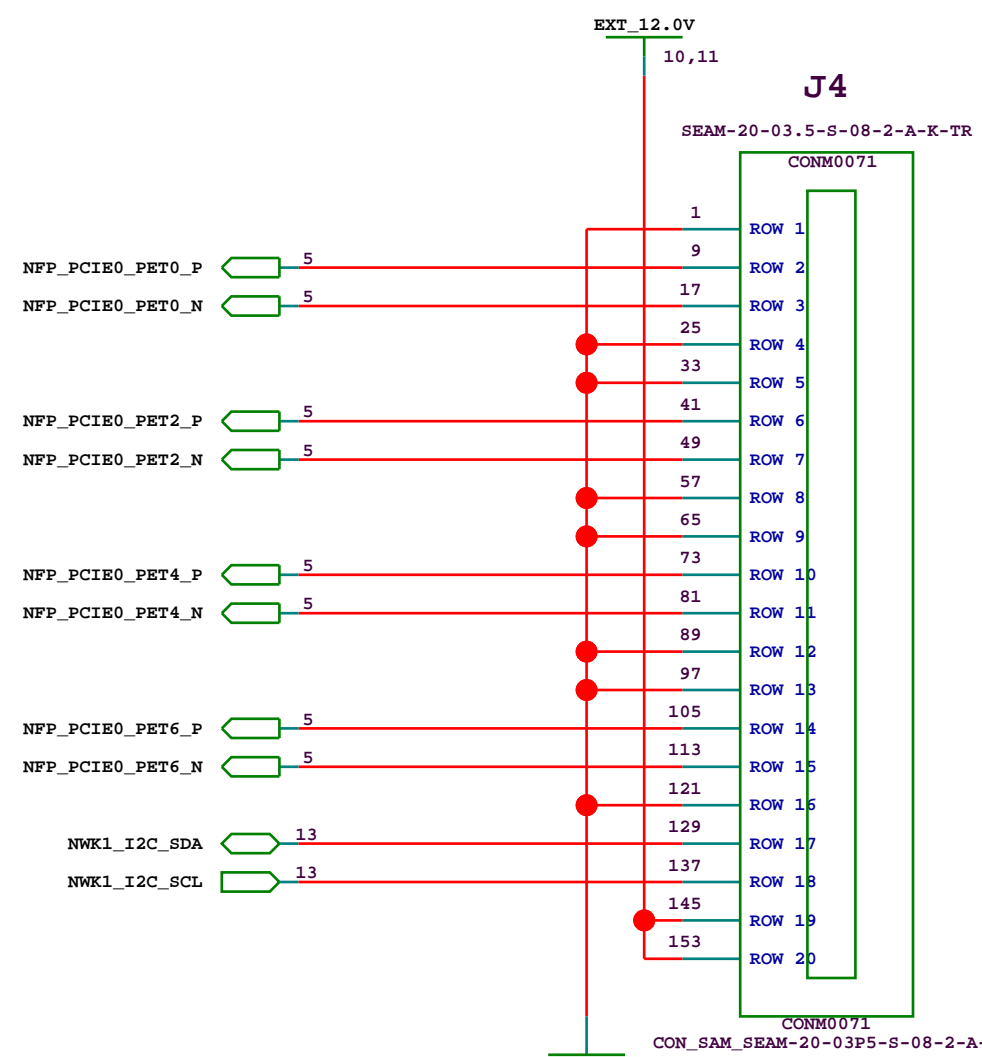


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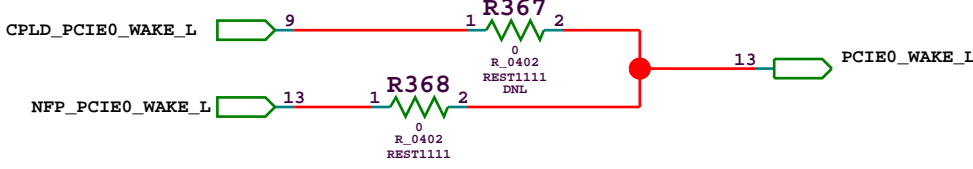
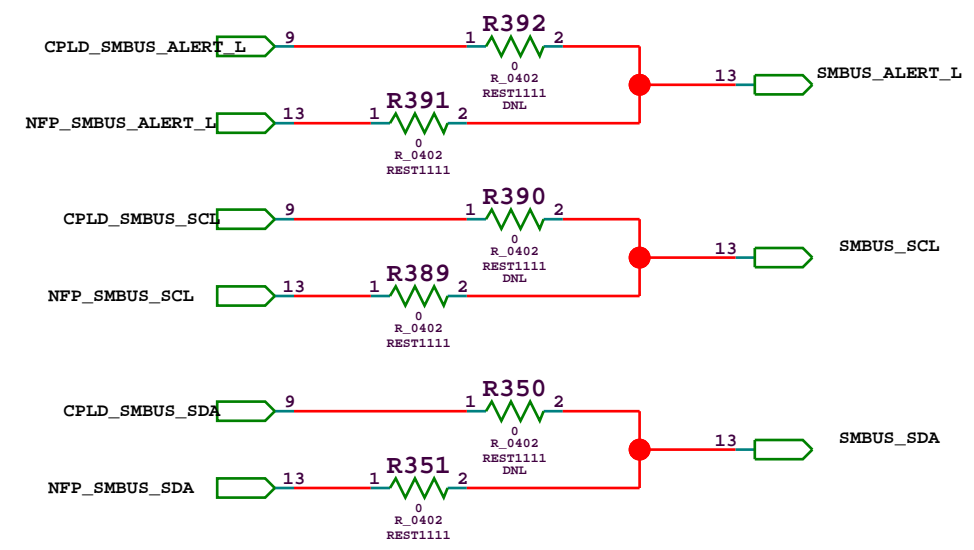
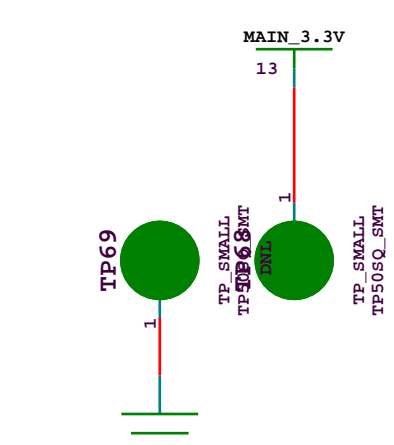
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Mezzanine Connector & Muxes



EXT_3.3V <-----> AUX_3.3V
MAIN_3.3V <-----> PCIE_3.3V



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D	SCHM0082-001	01
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	6-30-2015_11:132	13 of 13