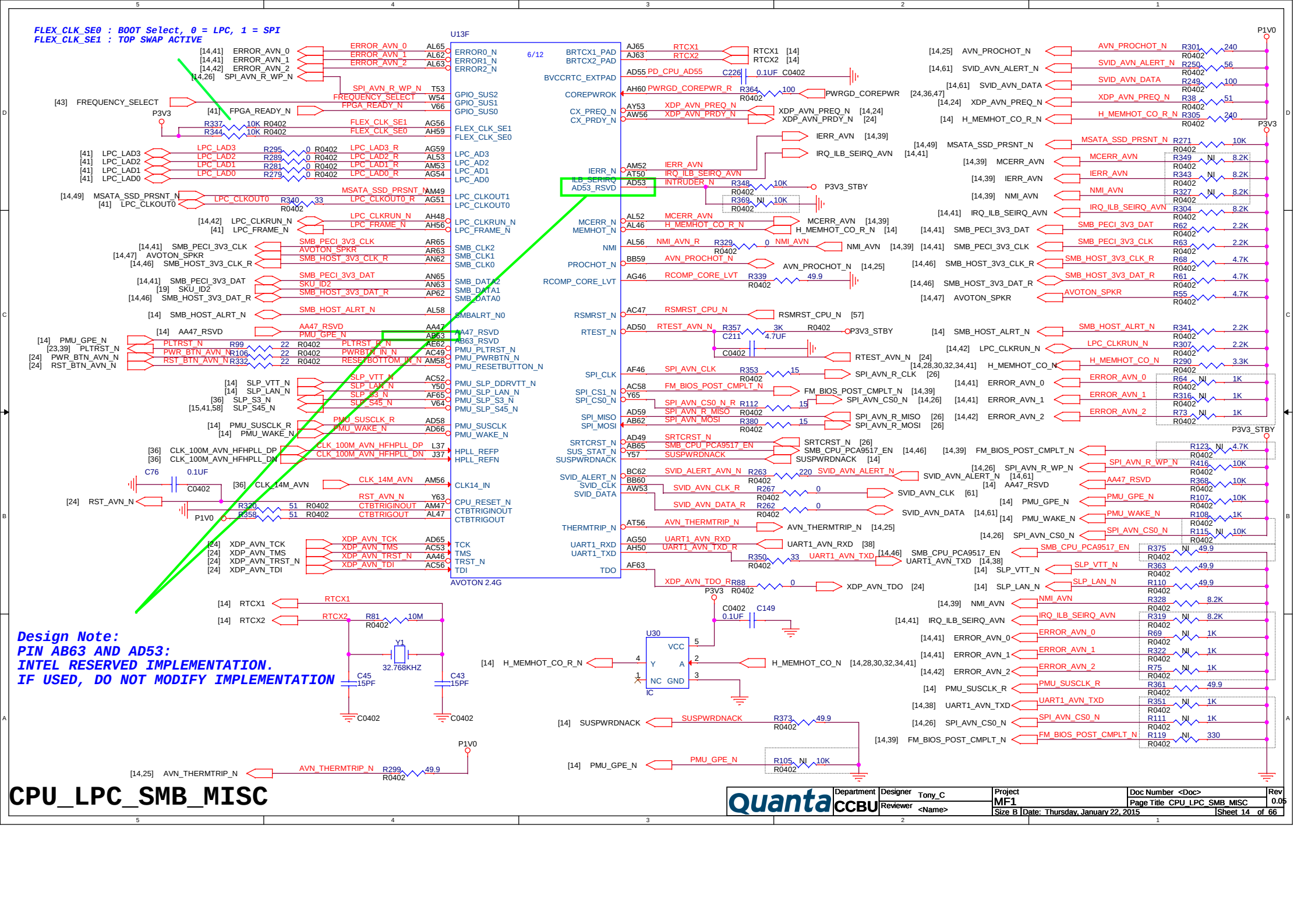
MF1 M/B

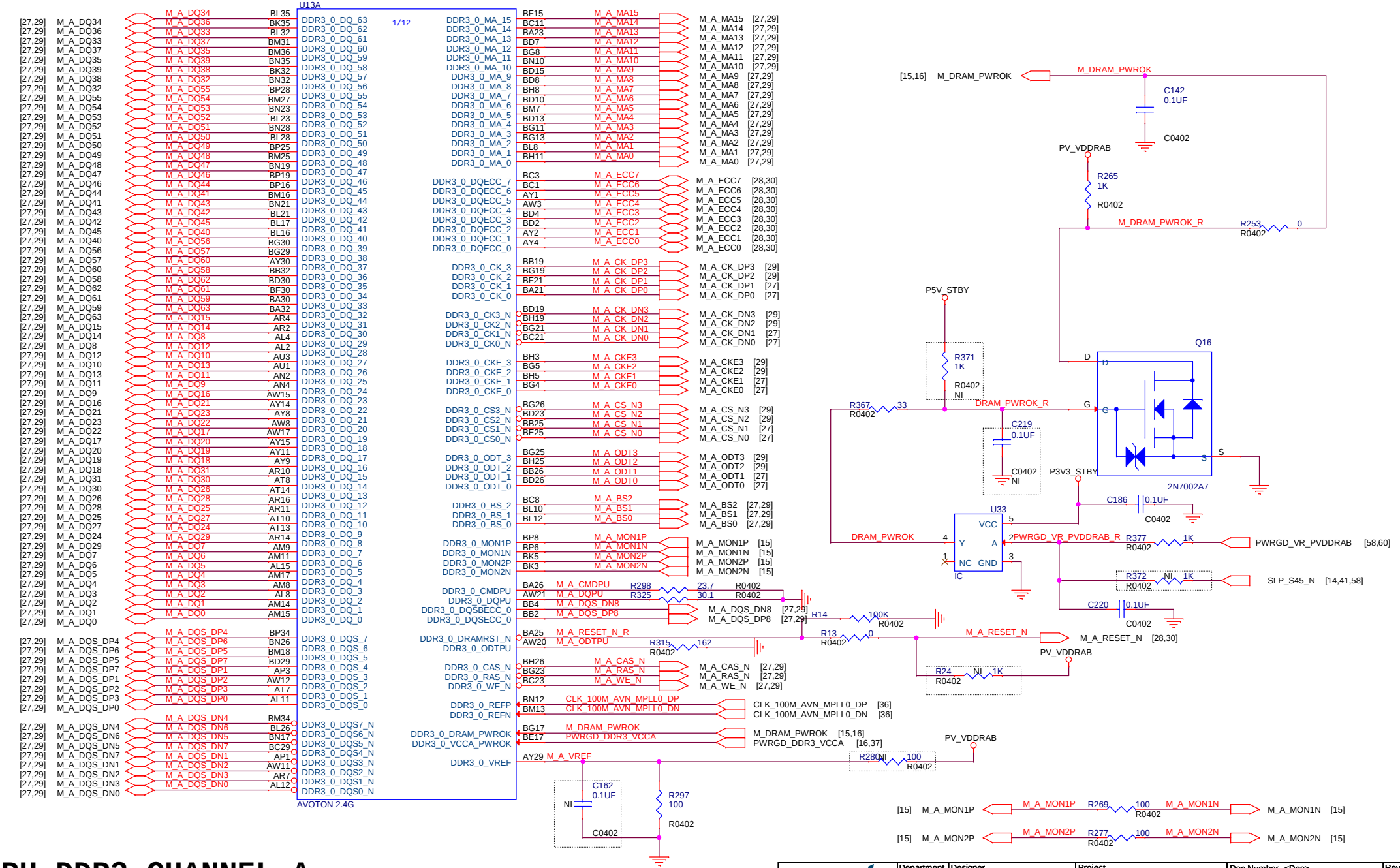
Avoton Micro-Server

PCB REV: C
PCBA REV: C2A
FAB: 3
SCH Rev:001
LAST UPDATE: 2015/01/22 2030

COVER PAGE

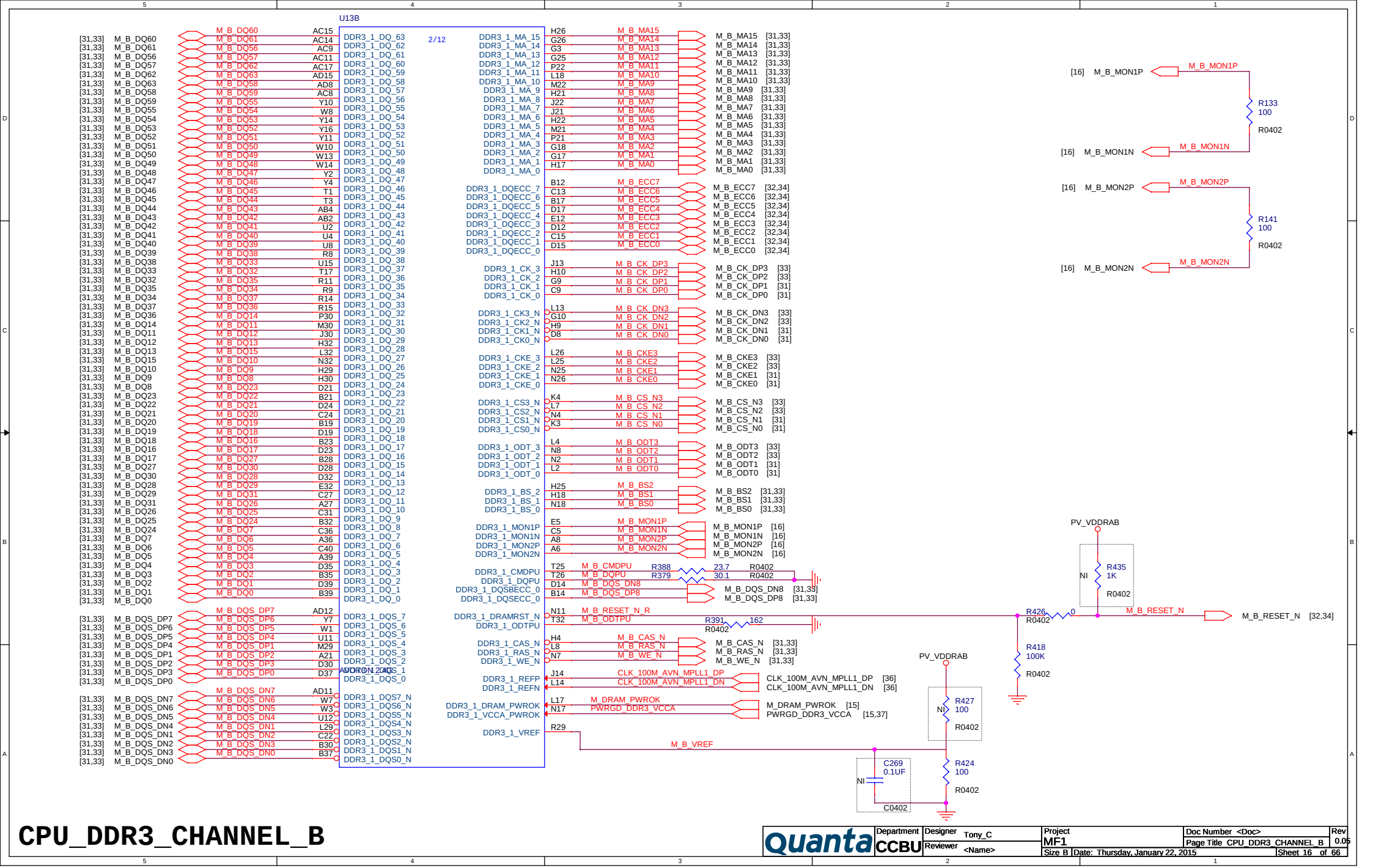
Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.5
		Reviewer <Name>		Page Title Cover Page	
			Size B Date: Thursday, January 22, 2015	Sheet 1 of 66	


FLEX_CLK_SE0 : BOOT Select, 0 = LPC, 1 = SPI
FLEX_CLK_SE1 : TOP SWAP ACTIVE
U13F
6/12
AVOTON 2.4G
Design Note:
PIN AB63 AND AD53:
INTEL RESERVED IMPLEMENTATION.
IF USED, DO NOT MODIFY IMPLEMENTATION
CPU_LPC_SMB_MISC
Quanta
Department CCBU
Designer Tony_C
Reviewer <Name>
Project MF1
Doc Number <Doc>
Page Title CPU_LPC_SMB_MISC
Rev 0.05
Size B
Date: Thursday, January 22, 2015
Sheet 14 of 66



CPU_DDR3_CHANNEL_A

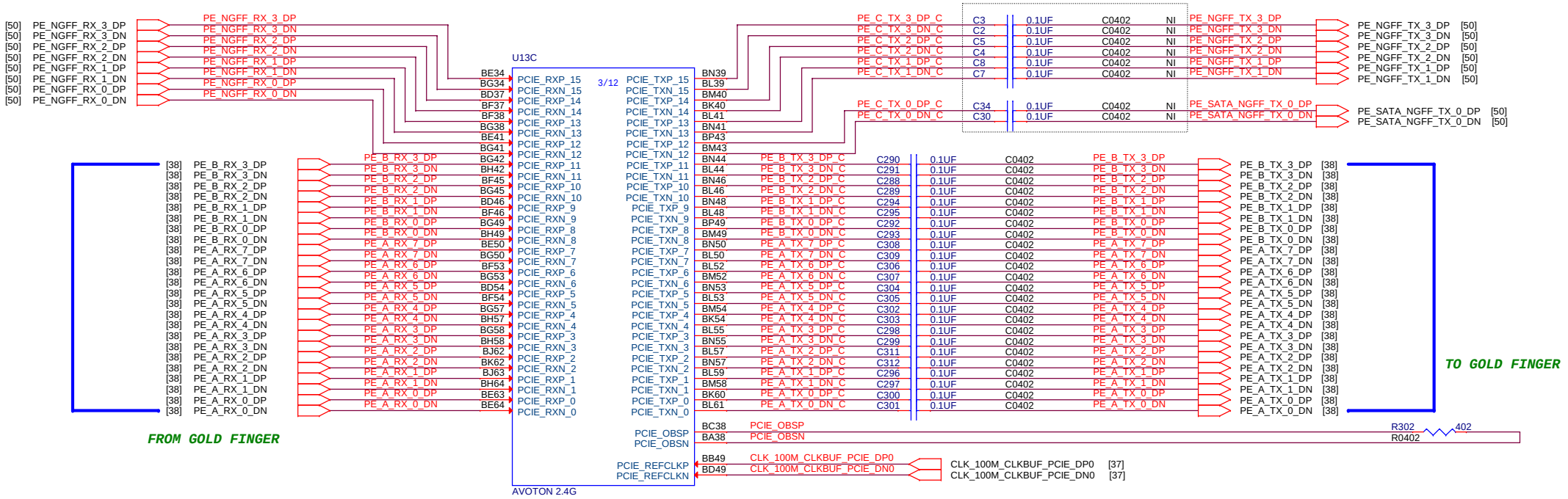
Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title CPU_DDR3_CHANNEL_A	
			Size B Date: Thursday, January 22, 2015	Sheet 15 of 66	



CPU_DDR3_CHANNEL_B

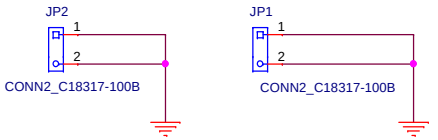
Quanta	Department CCBU	Designer Tony_C	Project MF1
		Reviewer <Name>	Size B Date: Thursday, January 22, 2015

Doc Number <Doc>	Rev 0.05
Page Title CPU_DDR3_CHANNEL_B	
Sheet 16 of 66	



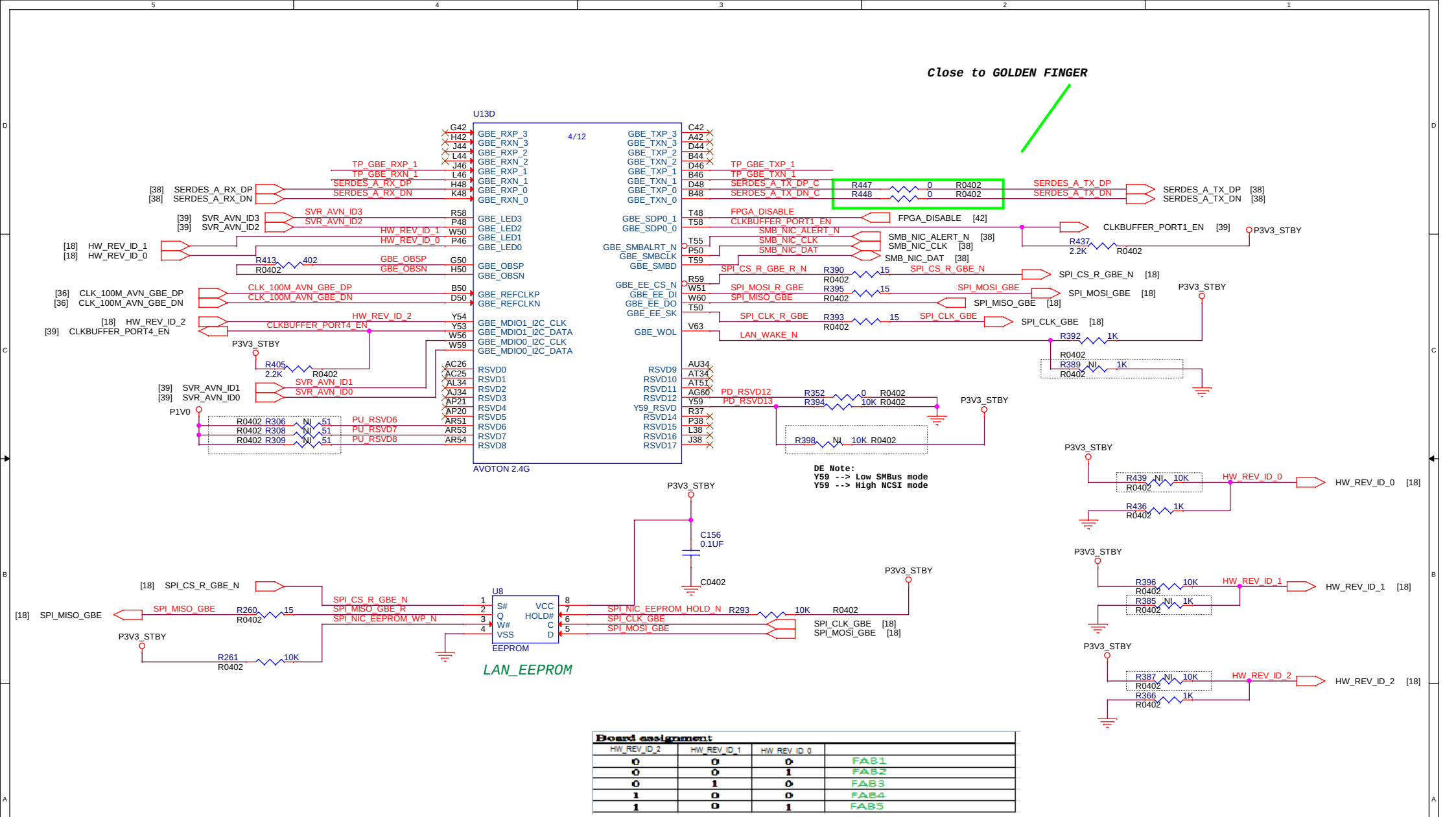
Bifurcation Control Register

Bifurcation Control 0 (BIFCTL0)	Lane Widths	Lane Numbers Assigned to Each Lane-Width Choice
000	x4 x4 x4 x4	Lanes 15:12 operate as x4 Lanes 11:8 operate as x4 Lanes 7:4 operate as x4 Lanes 3:0 operate as x4
001	x4 x4 x8	Lanes 15:12 operate as x4 Lanes 11:8 operate as x4 Lanes 7:0 operate as x8
010	x8 x4 x4	Lanes 15:8 operate as x8 Lanes 7:4 operate as x4 Lanes 3:0 operates as x4
011	x8 x8	Lanes 15:8 operate as x8 Lanes 7:0 operate as x8
100	x16	Lanes 15:0 operate as x16
101 - 111	Reserved	



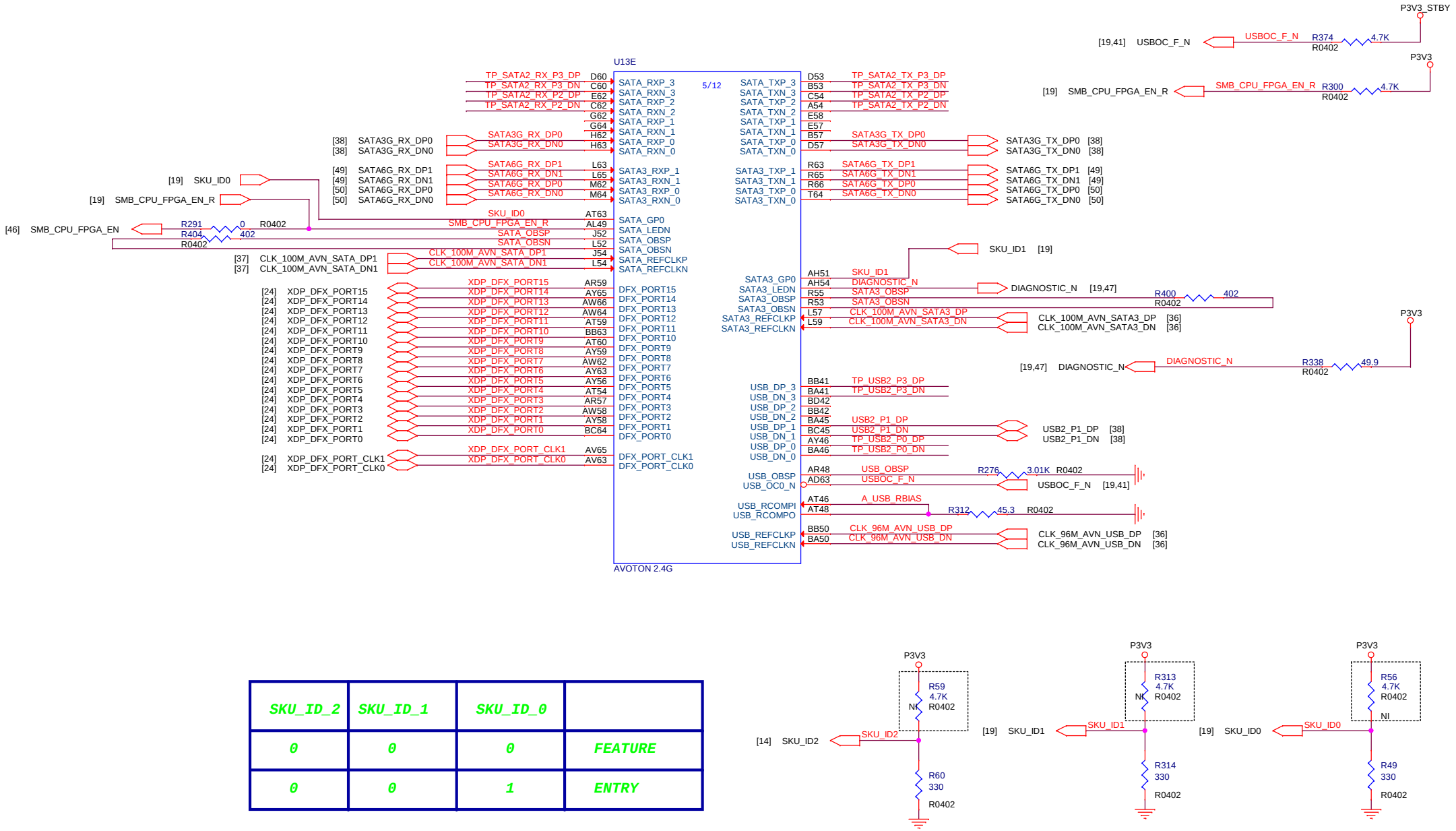
CPU_PCIE_GEN2

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title CPU_PCIE_GEN2	
			Size B Date: Thursday, January 22, 2015	Sheet 17 of 66	



CPU_GBE

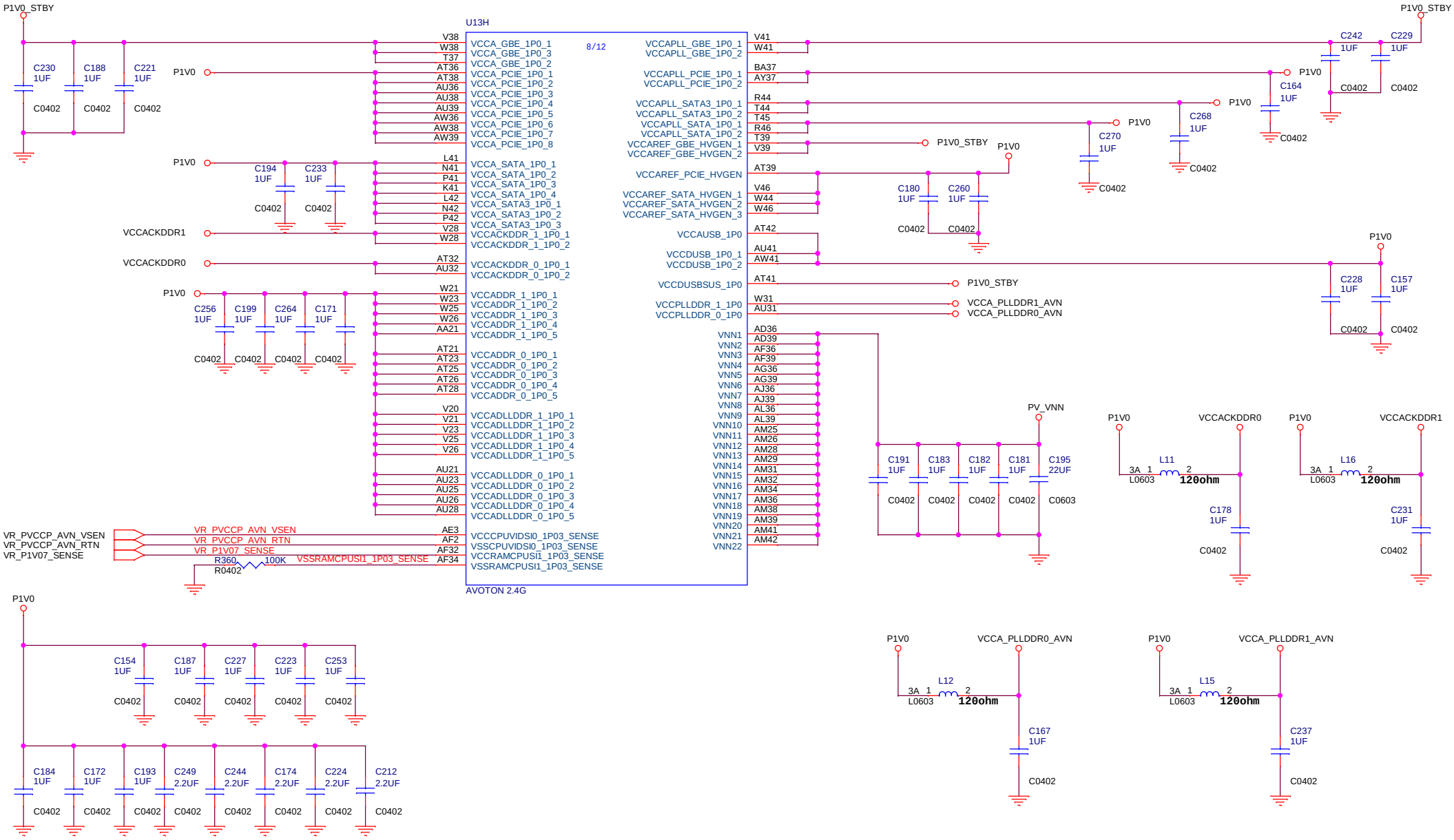
Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>	Size B Date: Thursday, January 22, 2015	Page Title CPU_GbE	Sheet 18 of 66

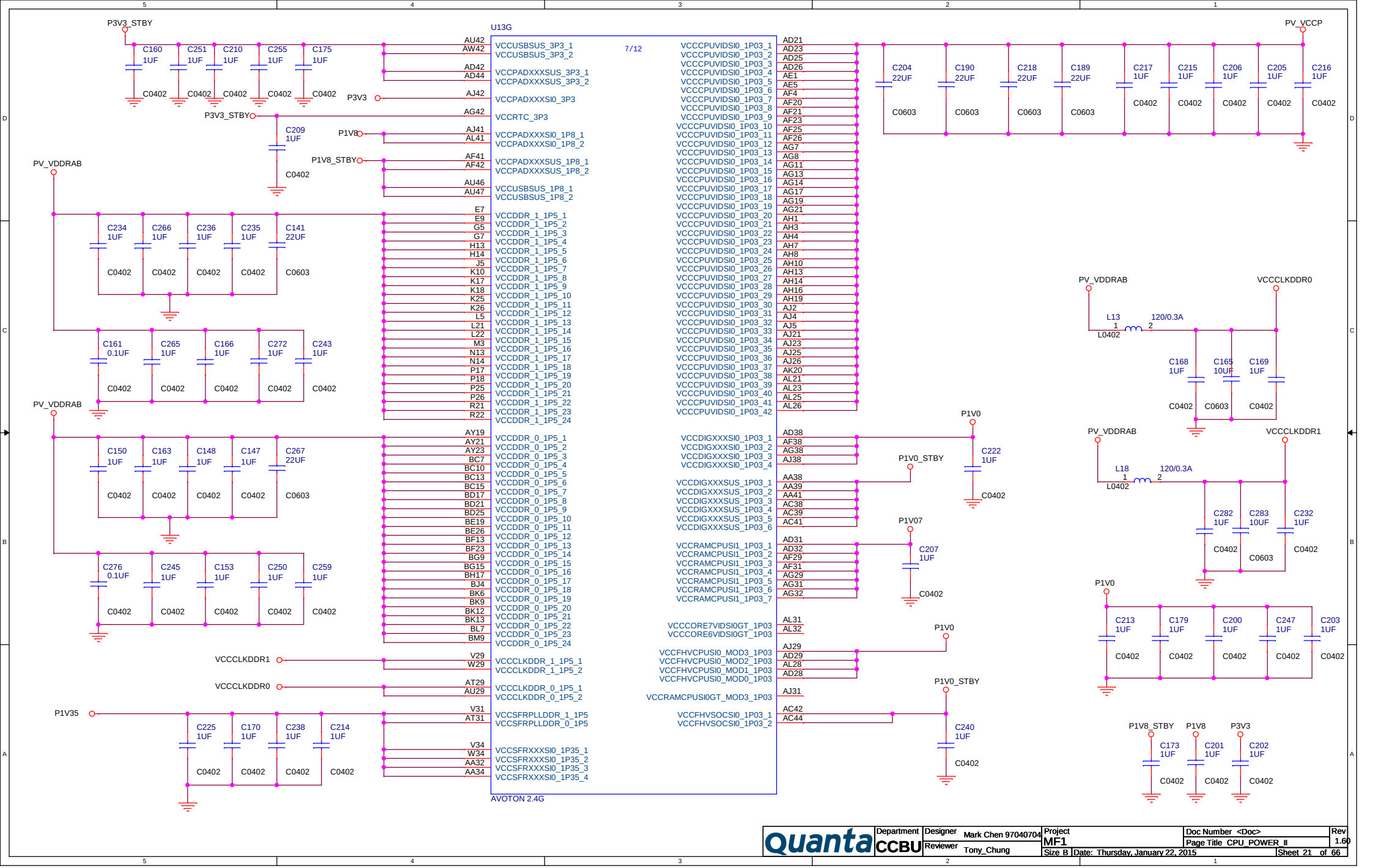


SKU_ID_2	SKU_ID_1	SKU_ID_0	
0	0	0	FEATURE
0	0	1	ENTRY

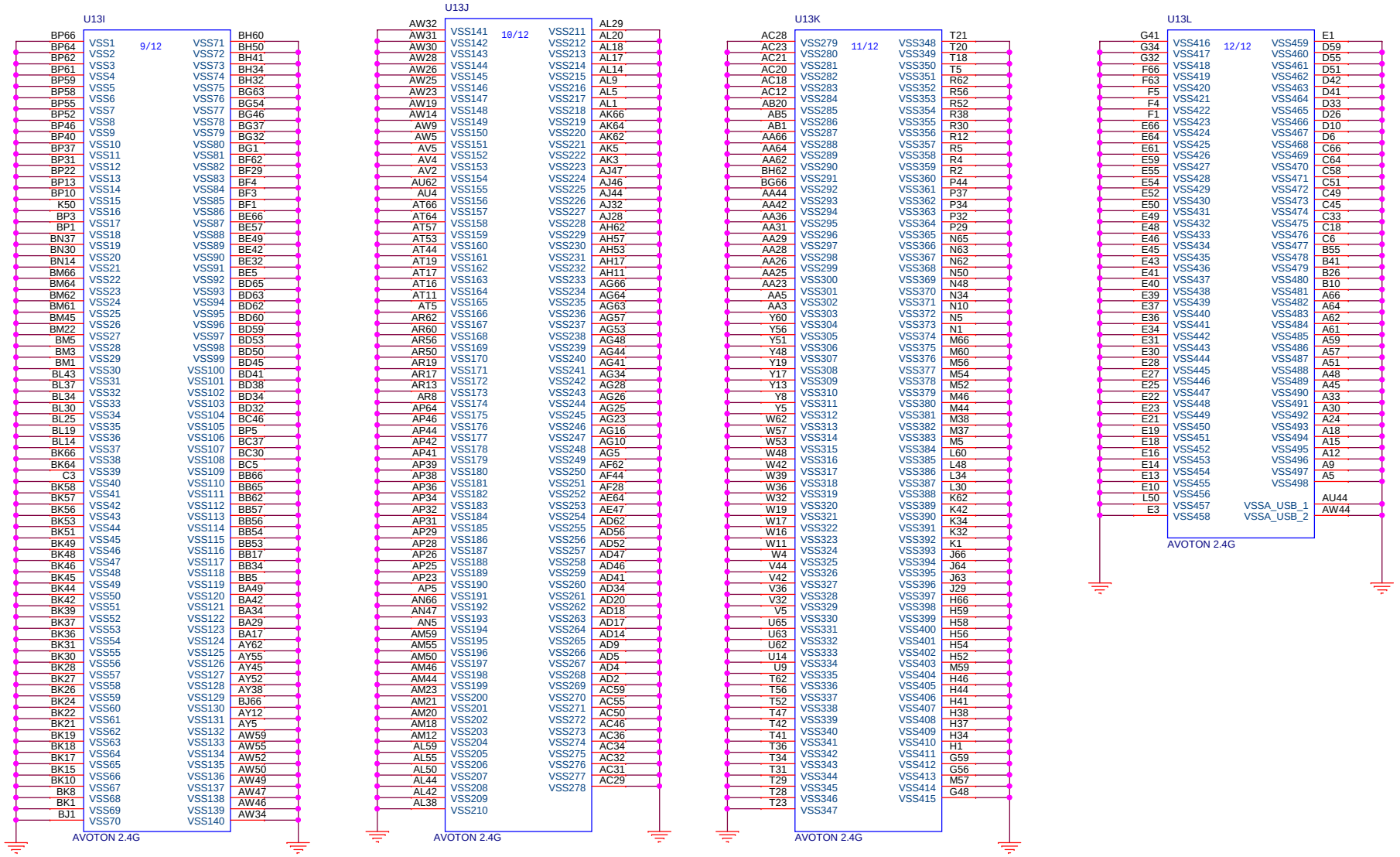
CPU_SATA_USB

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc> Rev 0.05
		Reviewer <Name>		Page Title CPU_SATA_USB
			Size B Date: Thursday, January 22, 2015	Sheet 19 of 66


U13H
8/12
AVOTON 2.4G
P1V0_STBY
P1V0
VCCACKDDR1
VCCACKDDR0
PV_VNN
VCCA_PLLDDR1_AVN
VCCA_PLLDDR0_AVN
[60] VR_PVCCP_AVN_VSEN
[60] VR_PVCCP_AVN_RTN
[63] VR_P1V07_SENSE
VR_PVCCP_AVN_VSEN
VR_PVCCP_AVN_RTN
VR_P1V07_SENSE
R360 100K R0402
VSSRAMCPUSI1_1P03_SENSE
120ohm
L0603
Quanta
Department CCBU
Designer Mark Chen 97040704
Reviewer Tony_Chung
Project MF1
Doc Number <Doc>
Page Title CPU_POWER_I
Rev 1.60
Size B Date: Thursday, January 22, 2015
Sheet 20 of 66

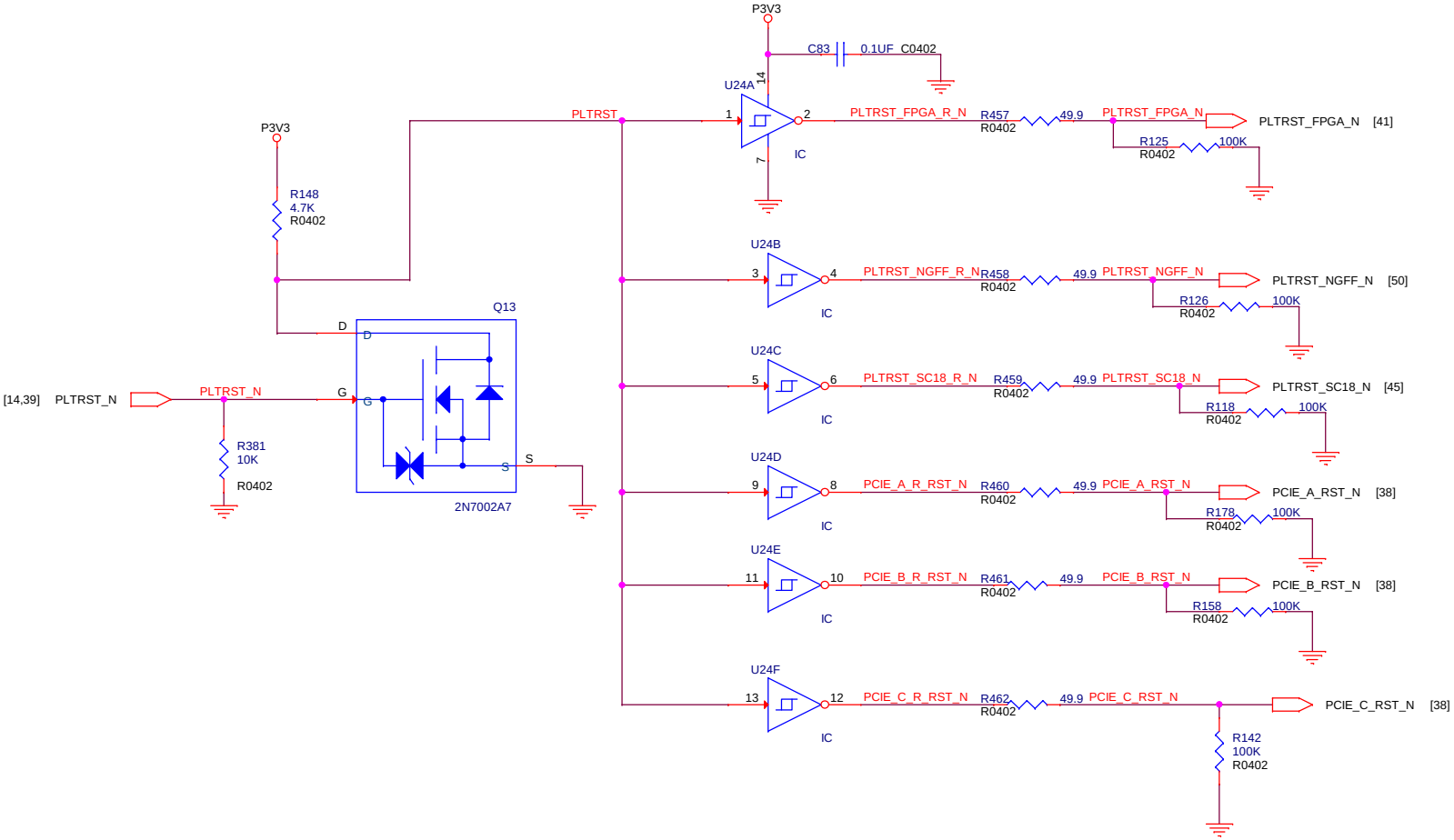


Quanta	Department CCBU	Designer Mark Chen 97040704	Project MF1	Doc Number <Doc>	Rev 1.60
		Reviewer Tony_Chung	Size B Date: Thursday, January 22, 2015	Page Title CPU_POWER_II	Sheet 21 of 66



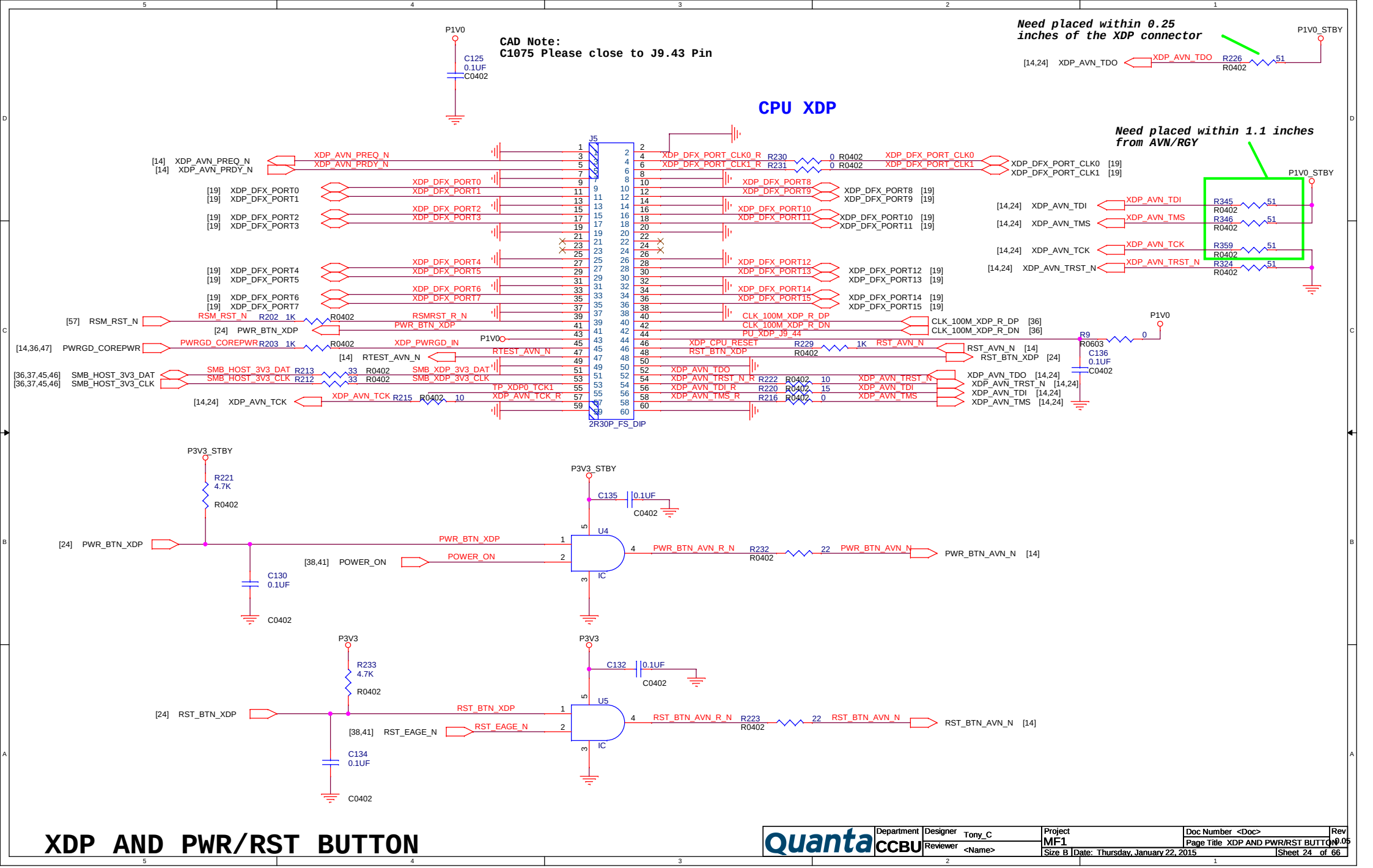
CPU_GND

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc> / Rev 0.05
		Reviewer <Name>		Page Title CPU_GND
			Size B Date: Thursday, January 22, 2015	Sheet 22 of 66



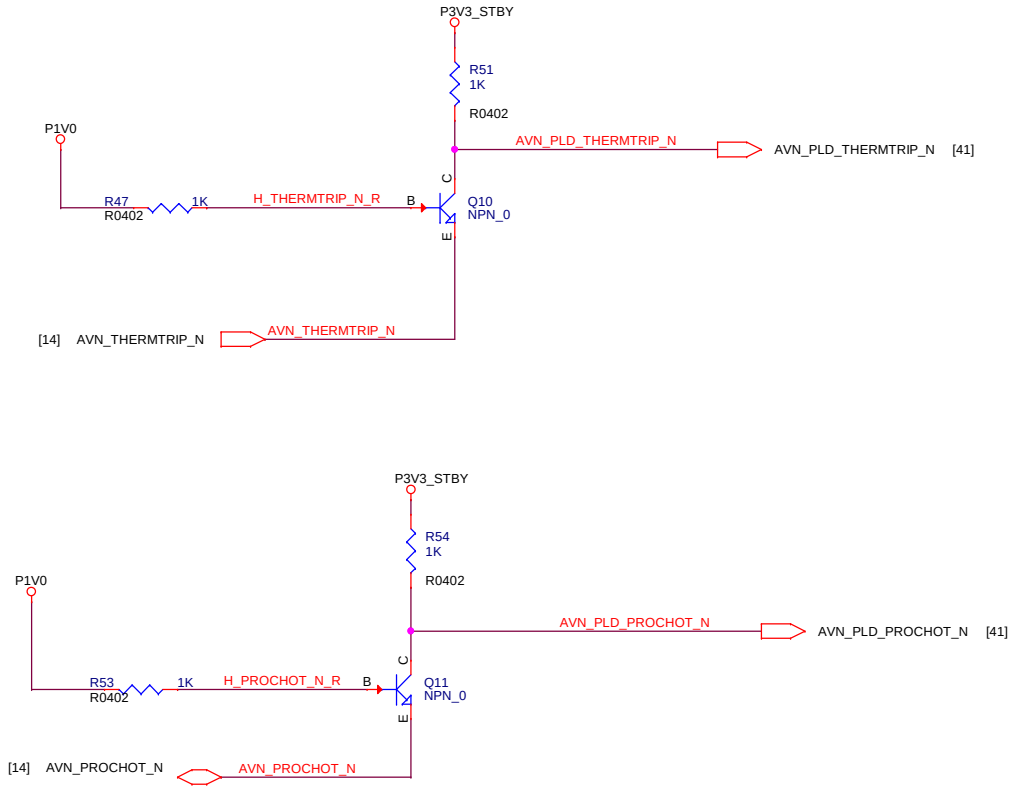
PLTRST_BUFFER

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title PLTRST_BUFFER	
			Size B Date: Thursday, January 22, 2015	Sheet 23 of 66	



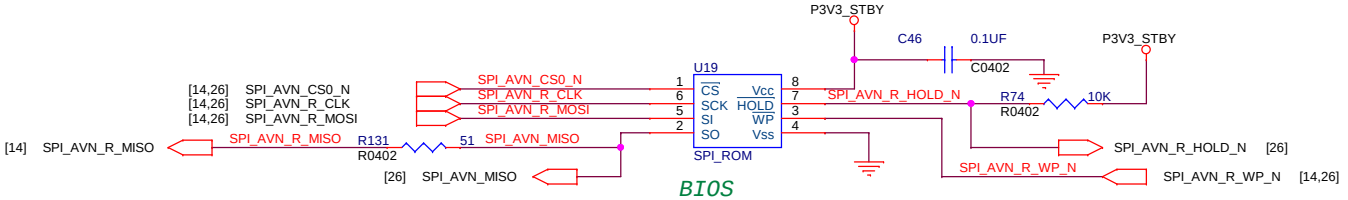
XDP AND PWR/RST BUTTON

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc> Rev 0.05
		Reviewer <Name>	Size B Date: Thursday, January 22, 2015	Page Title XDP AND PWR/RST BUTTON Sheet 24 of 66



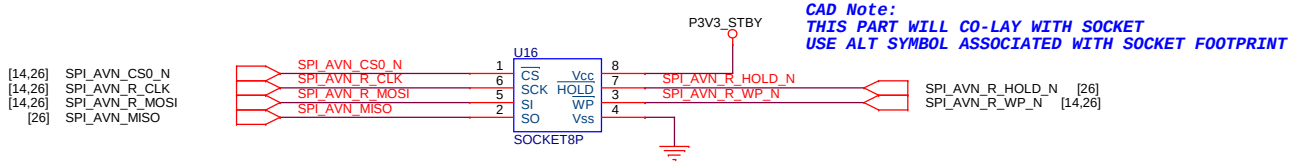
ERROR CNTL

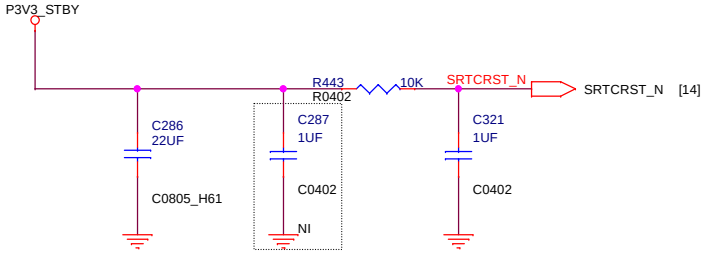
Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title ERROR CNTL	
			Size B Date: Thursday, January 22, 2015	Sheet 25 of 66	



BIOS

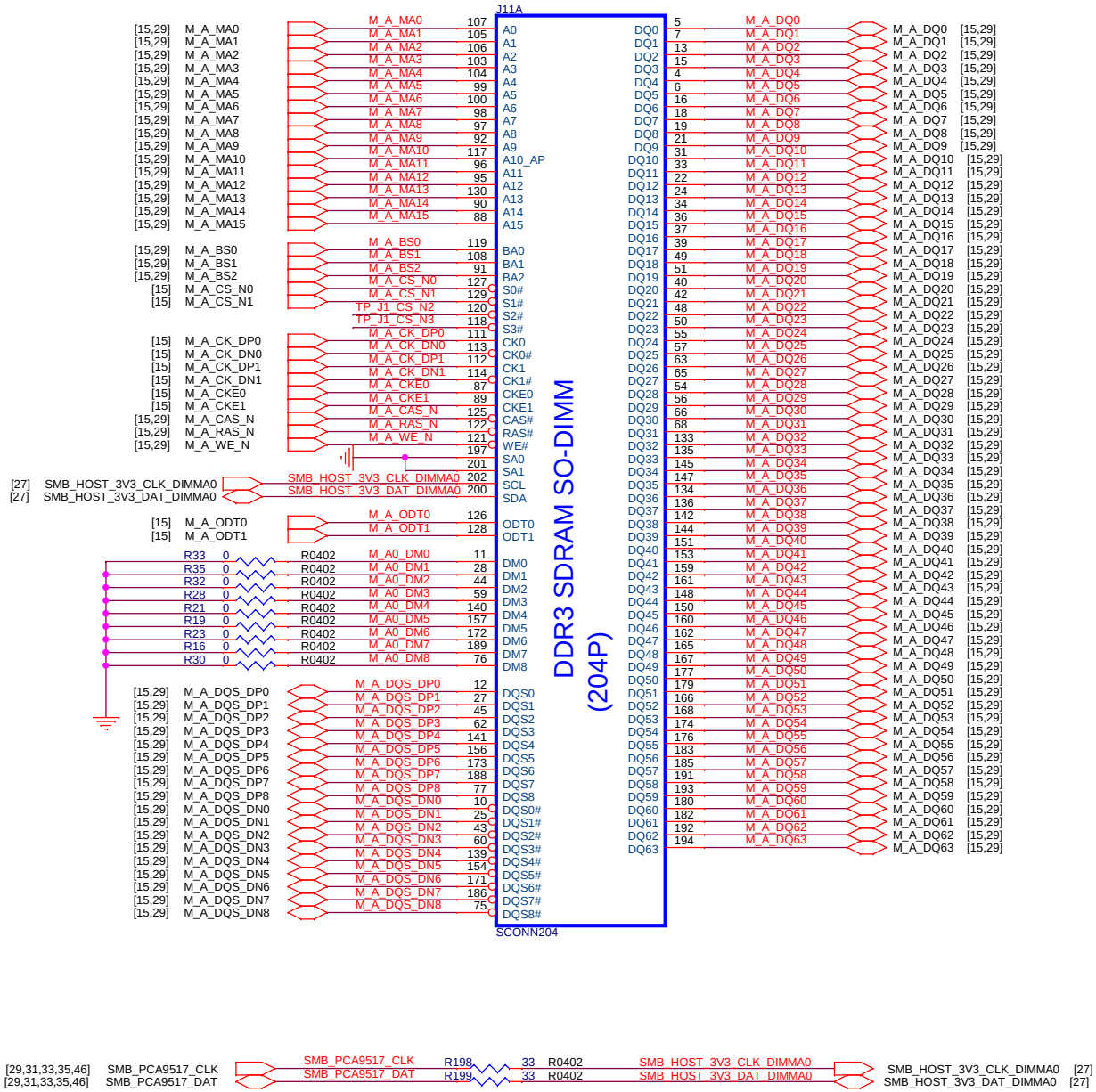
CAD Note:
THIS PART WILL CO-LAY WITH SOCKET
USE ALT SYMBOL ASSOCIATED WITH SOCKET FOOTPRINT





CPU SPI

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title CPU_SPI	
			Size B Date: Thursday, January 22, 2015	Sheet 26 of 66	

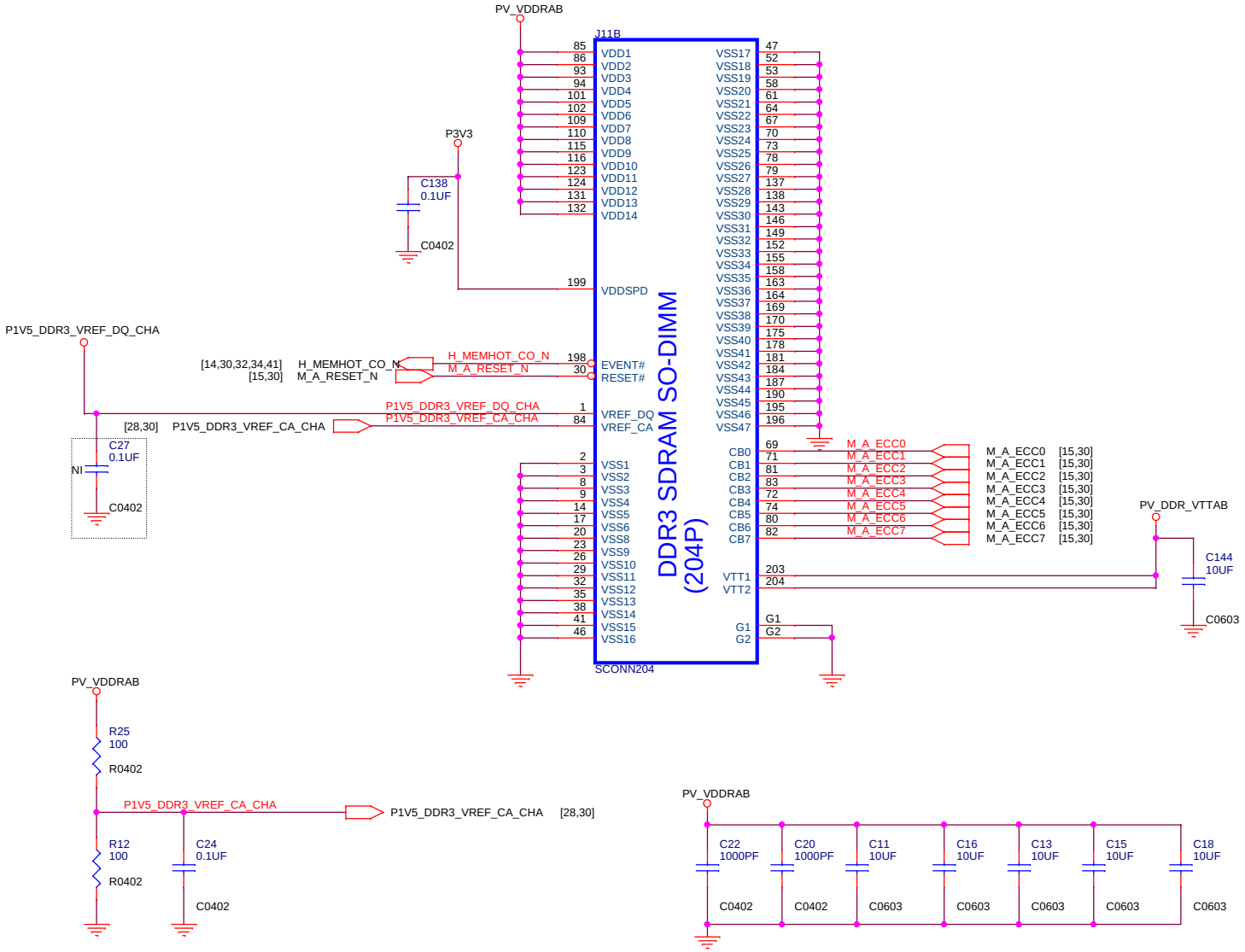


[29,31,33,35,46] SMB_PCA9517_CLK
[29,31,33,35,46] SMB_PCA9517_DAT
SMB_PCA9517_CLK R198 33 R0402 SMB_HOST_3V3_CLK_DIMMA0
SMB_PCA9517_DAT R199 33 R0402 SMB_HOST_3V3_DAT_DIMMA0
SMB_HOST_3V3_CLK_DIMMA0 [27]
SMB_HOST_3V3_DAT_DIMMA0 [27]

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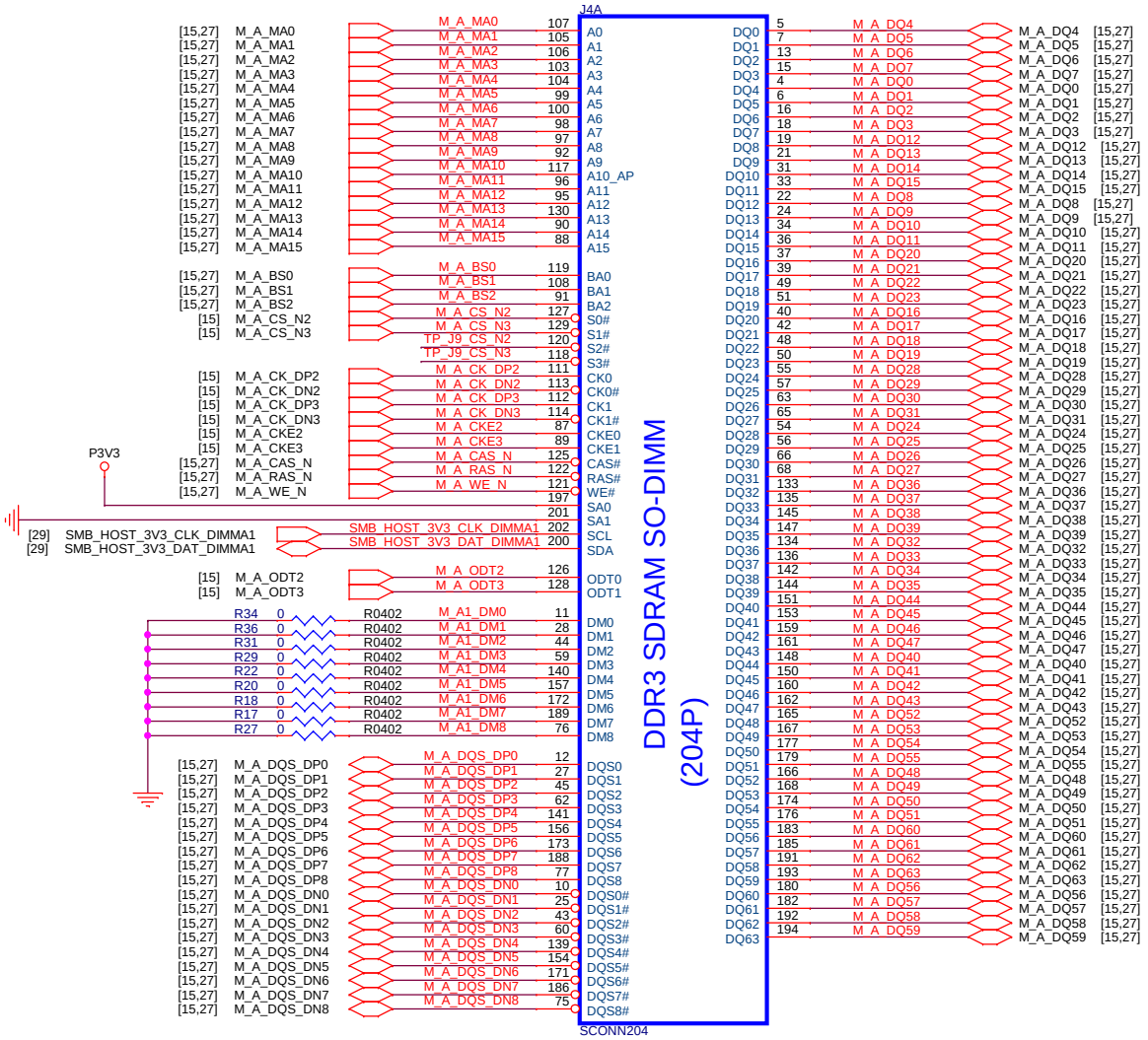
DDR3_SODIMM_CHA0_1

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc> Rev 0.57
		Reviewer Chih-Ta Chen 92081366	Size B Date: Thursday, January 22, 2015	Page Title DDR3_SODIMM_CHA0 Sheet 27 of 66



DDR3_SODIMM_CHA0_2

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title BLANK	
			Size B	Date: Thursday, January 22, 2015	Sheet 28 of 66

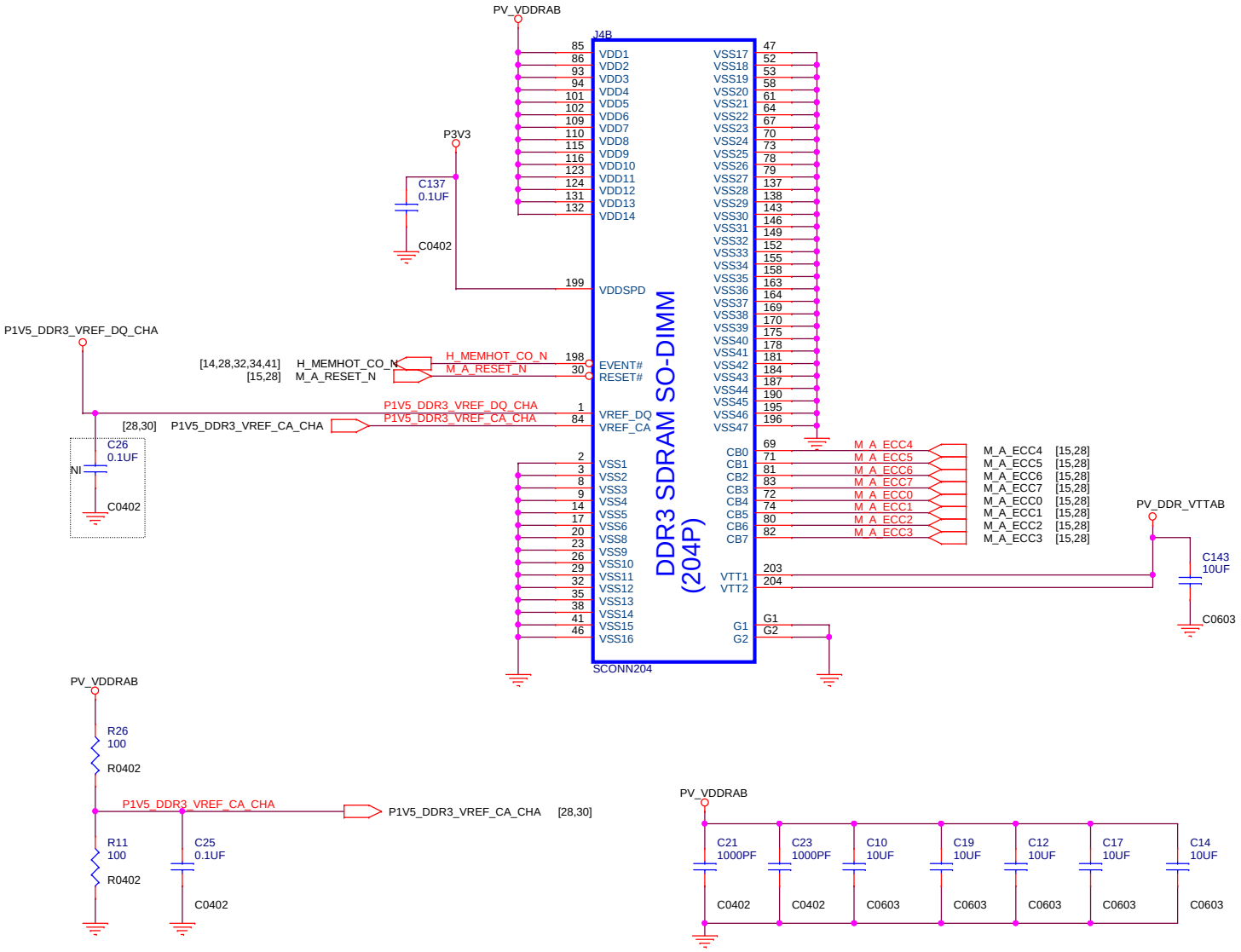


[27,31,33,35,46] SMB_PCA9517_CLK
[27,31,33,35,46] SMB_PCA9517_DAT
SMB_PCA9517_CLK R3 33 R0402 SMB_HOST_3V3_CLK_DIMMA1
SMB_PCA9517_DAT R7 33 R0402 SMB_HOST_3V3_DAT_DIMMA1
SMB_HOST_3V3_CLK_DIMMA1 [29]
SMB_HOST_3V3_DAT_DIMMA1 [29]

ADDRESS = 0xA2

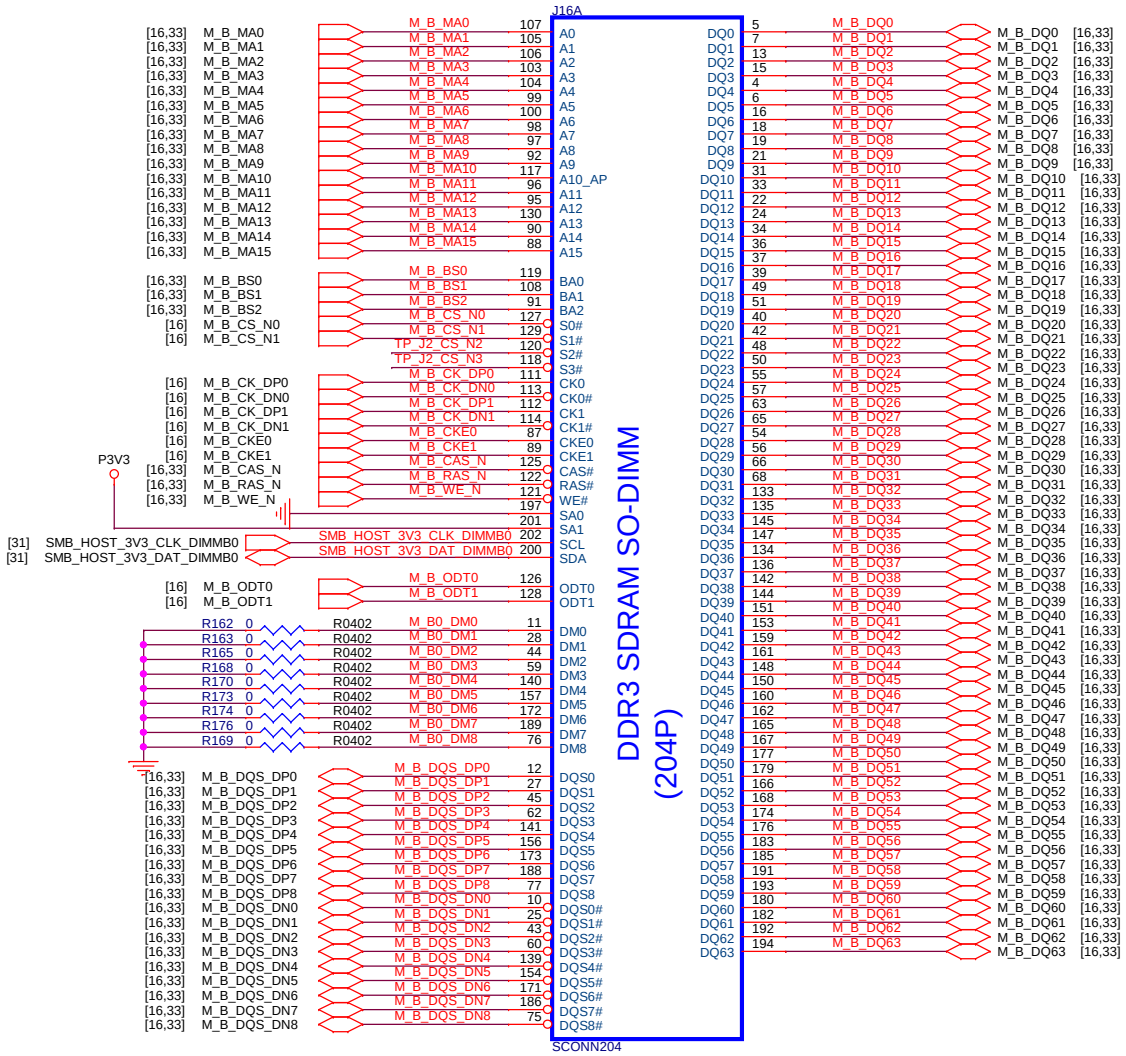
DDR3_SODIMM_CHA1_1

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc> Rev 0.57
		Reviewer Chih-Ta Chen 92081308		Page Title DDR3_SODIMM_CHA1
		Size B Date: Thursday, January 22, 2015		Sheet 29 of 66



DDR3_SODIMM_CHA1_2

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title BLANK	
			Size B	Date: Thursday, January 22, 2015	Sheet 30 of 66

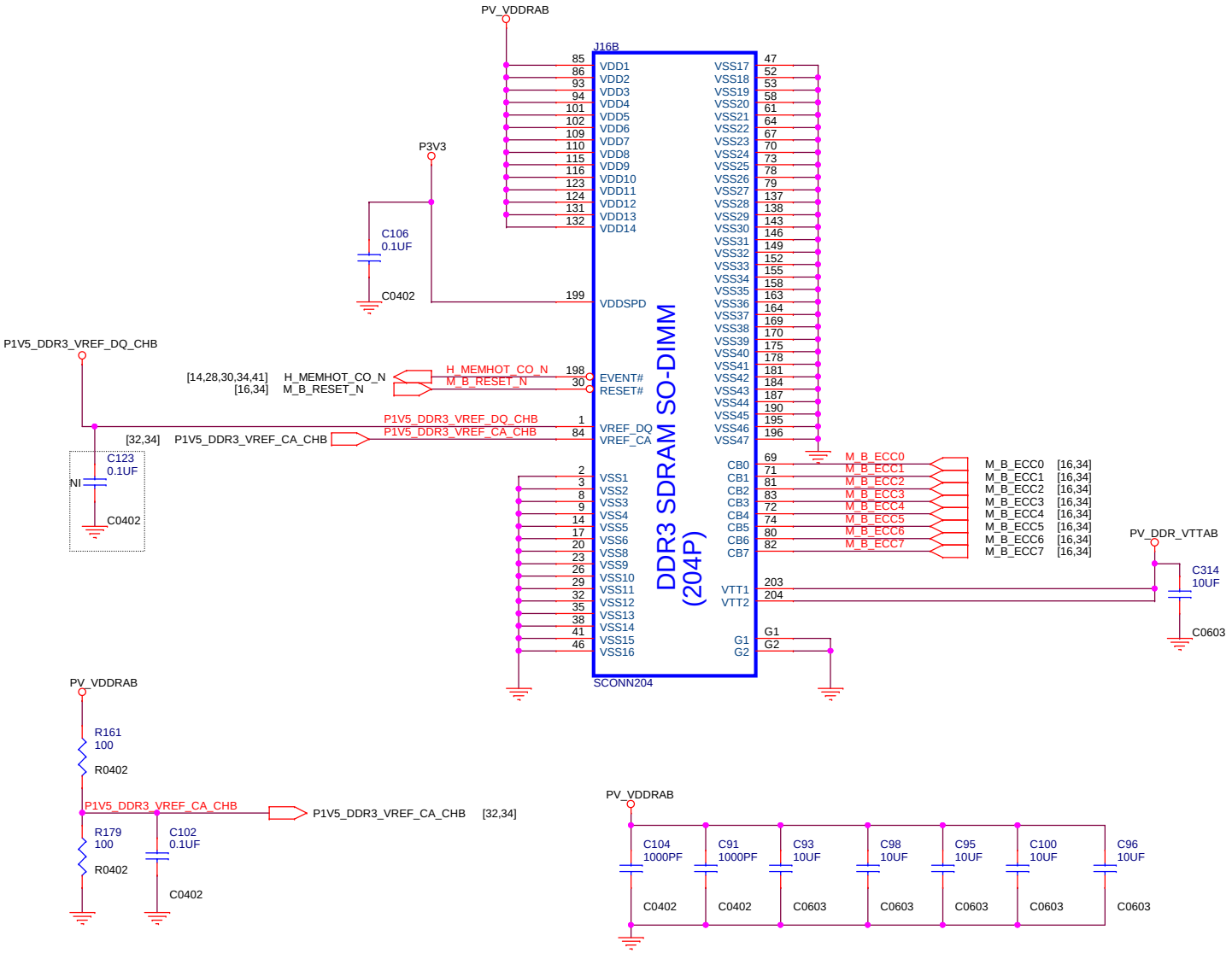


[27,29,33,35,46] SMB_PCA9517_CLK
[27,29,33,35,46] SMB_PCA9517_DAT
SMB_PCA9517_CLK SMB_PCA9517_DAT
R455 33 R0402
R454 33 R0402
SMB_HOST_3V3_CLK_DIMMB0 SMB_HOST_3V3_DAT_DIMMB0
SMB_HOST_3V3_CLK_DIMMB0 [31]
SMB_HOST_3V3_DAT_DIMMB0 [31]

ADDRESS = 0xA4

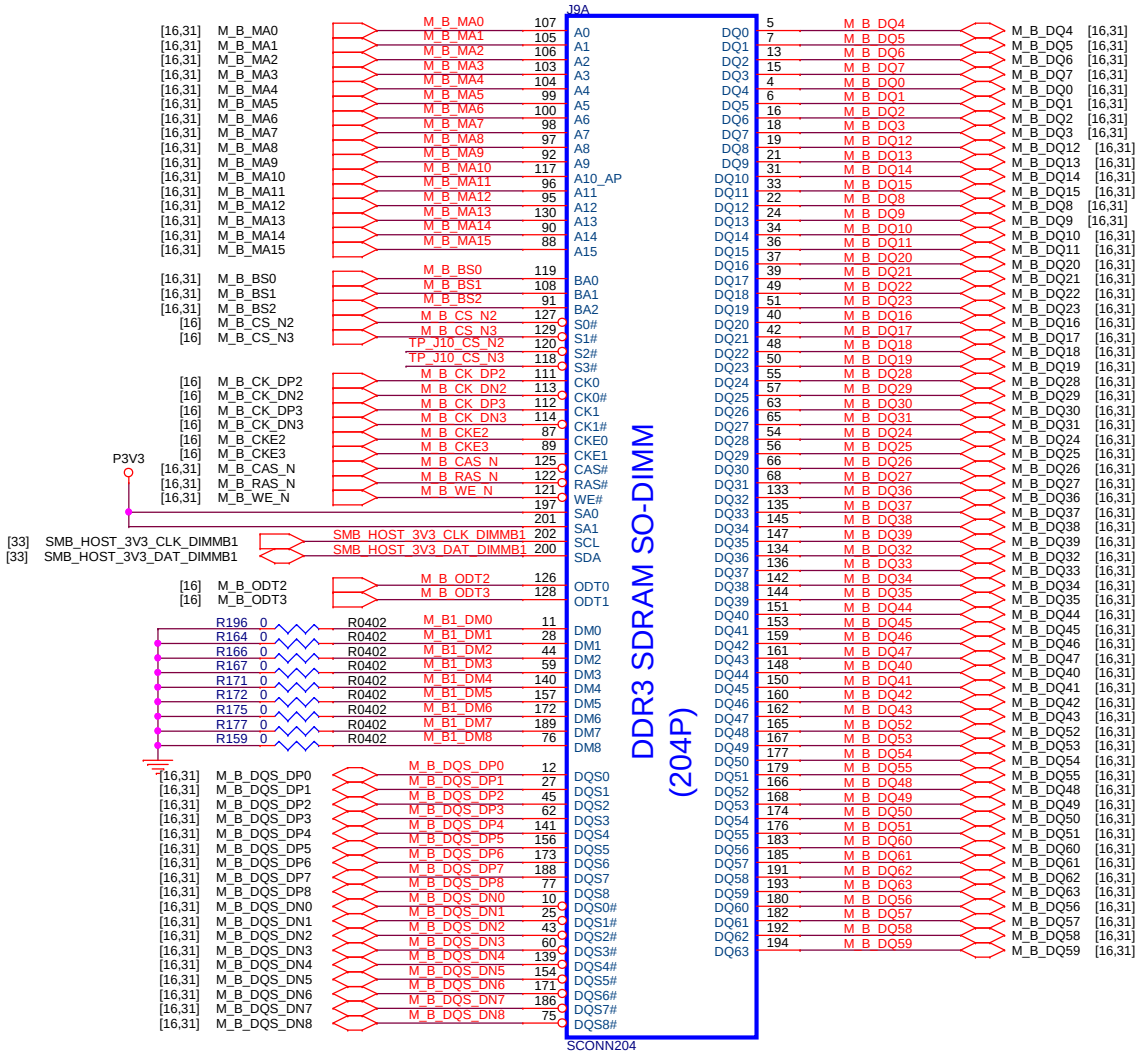
DDR3_SODIMM_CHB0_1

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc> / Rev 0.57
		Reviewer Chih-Ta Chen 92081366		Page Title DDR3_SODIMM_CHB0
			Size B Date: Thursday, January 22, 2015	Sheet 31 of 66



DDR3_SODIMM_CHB0_2

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>	Size B Date: Thursday, January 22, 2015	Page Title BLANK	Sheet 32 of 66

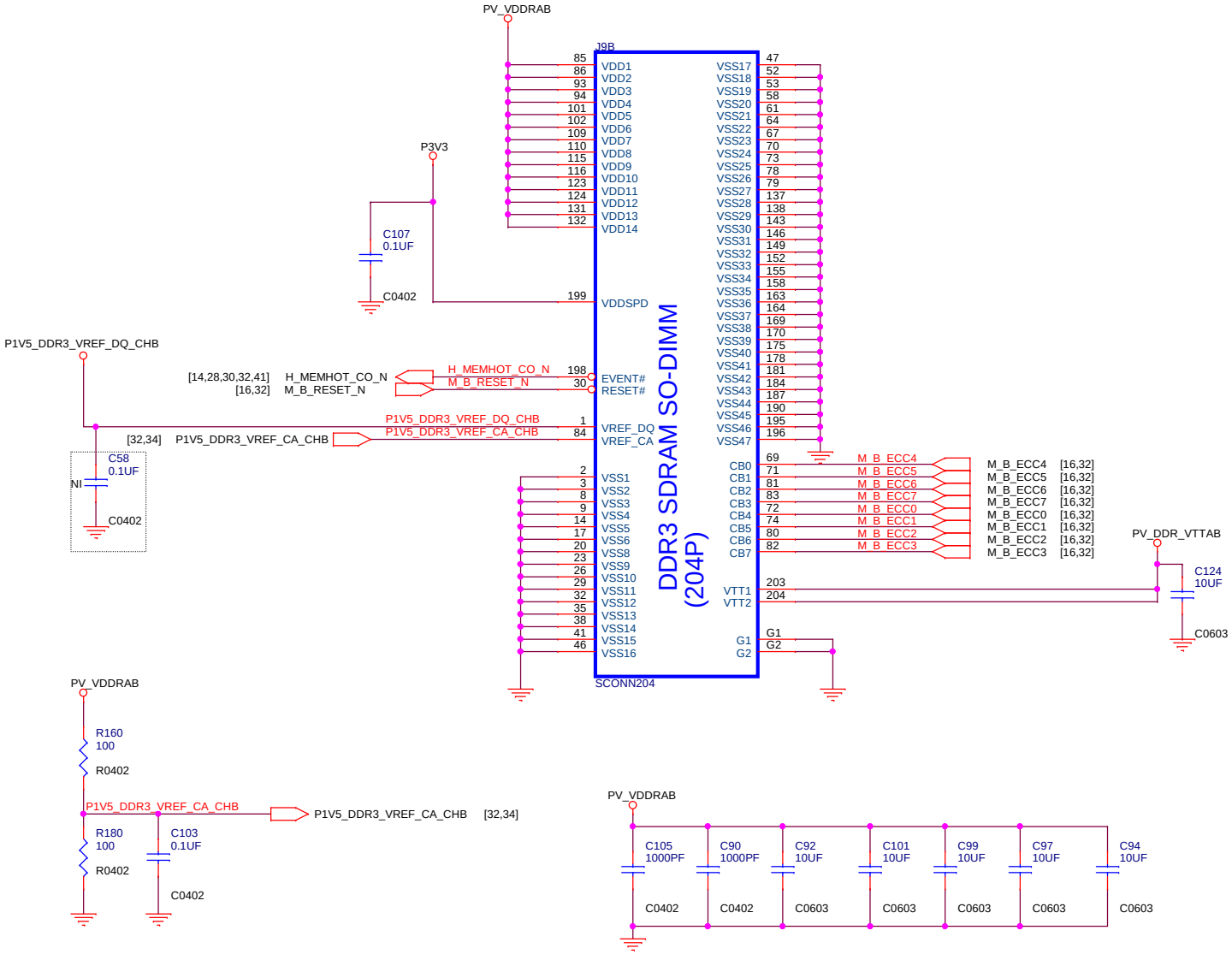


[27,29,31,35,46] SMB_PCA9517_CLK
[27,29,31,35,46] SMB_PCA9517_DAT
SMB_PCA9517_CLK R193 33 R0402 SMB_HOST_3V3_CLK_DIMMB1
SMB_PCA9517_DAT R192 33 R0402 SMB_HOST_3V3_DAT_DIMMB1
SMB_HOST_3V3_CLK_DIMMB1 [33]
SMB_HOST_3V3_DAT_DIMMB1 [33]

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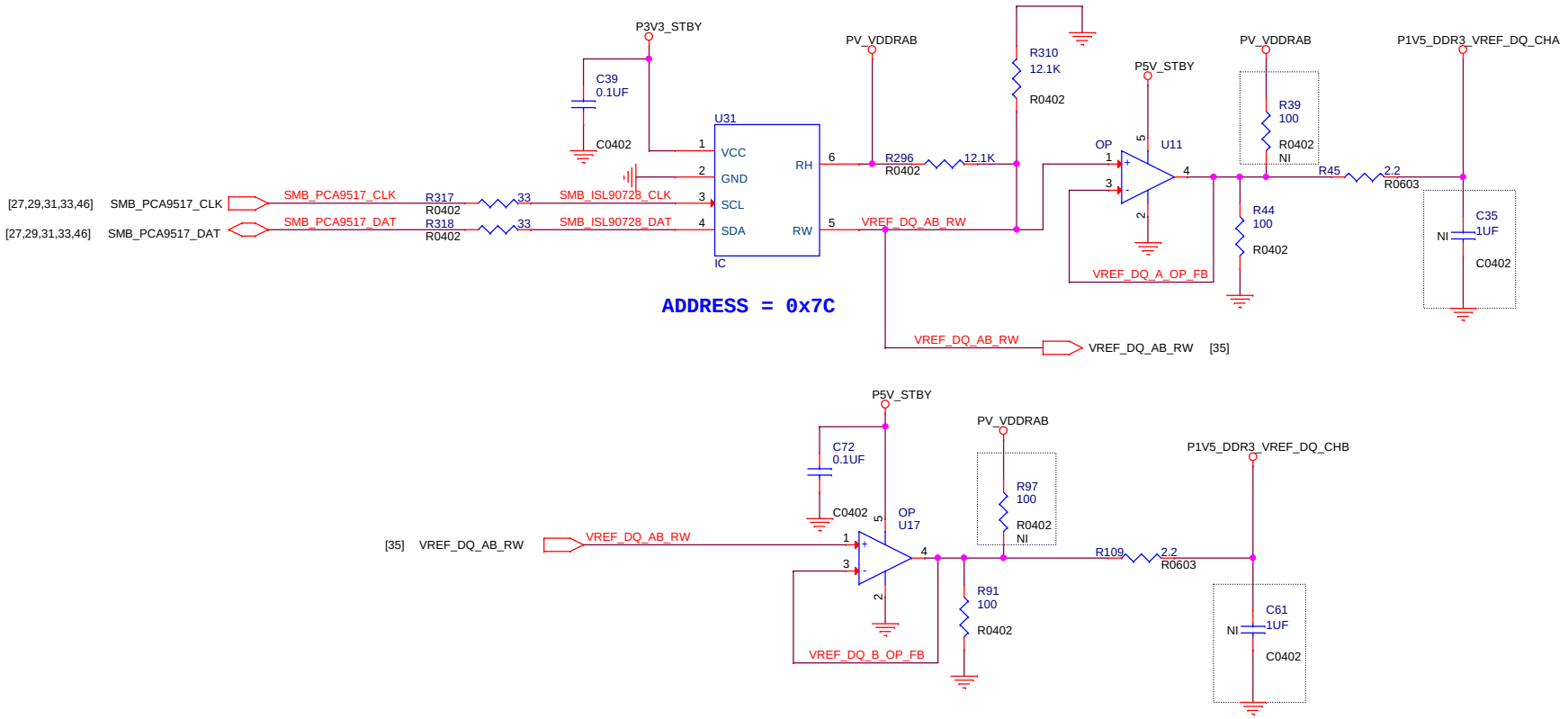
DDR3_SODIMM_CHB1_1

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc> / Page Title DDR3_SODIMM_CHB1 / Rev 0.57
		Reviewer Chih-Ta Chen 92081366	Size B Date: Thursday, January 22, 2015	Sheet 33 of 66



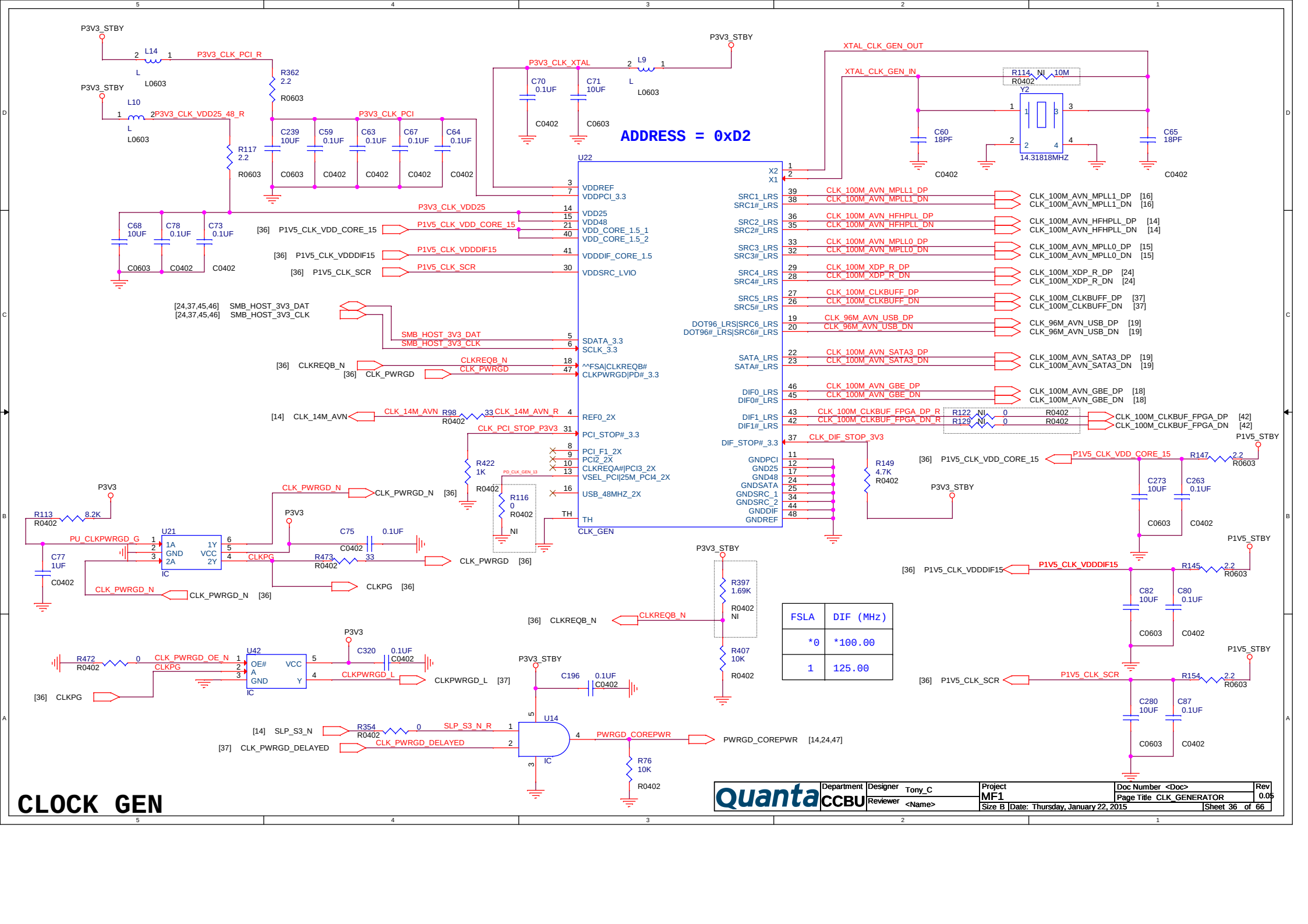
DDR3_SODIMM_CHB1_2

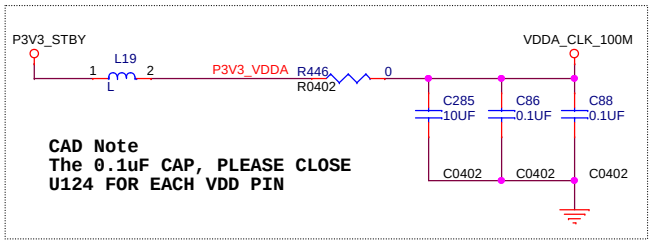
Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title BLANK	
			Size B	Date: Thursday, January 22, 2015	Sheet 34 of 66

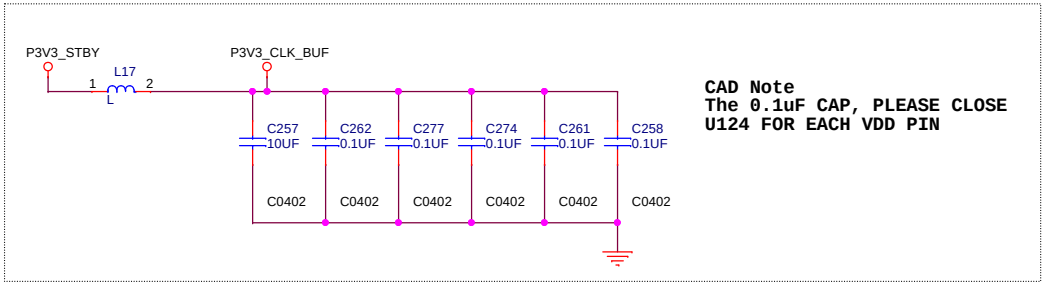


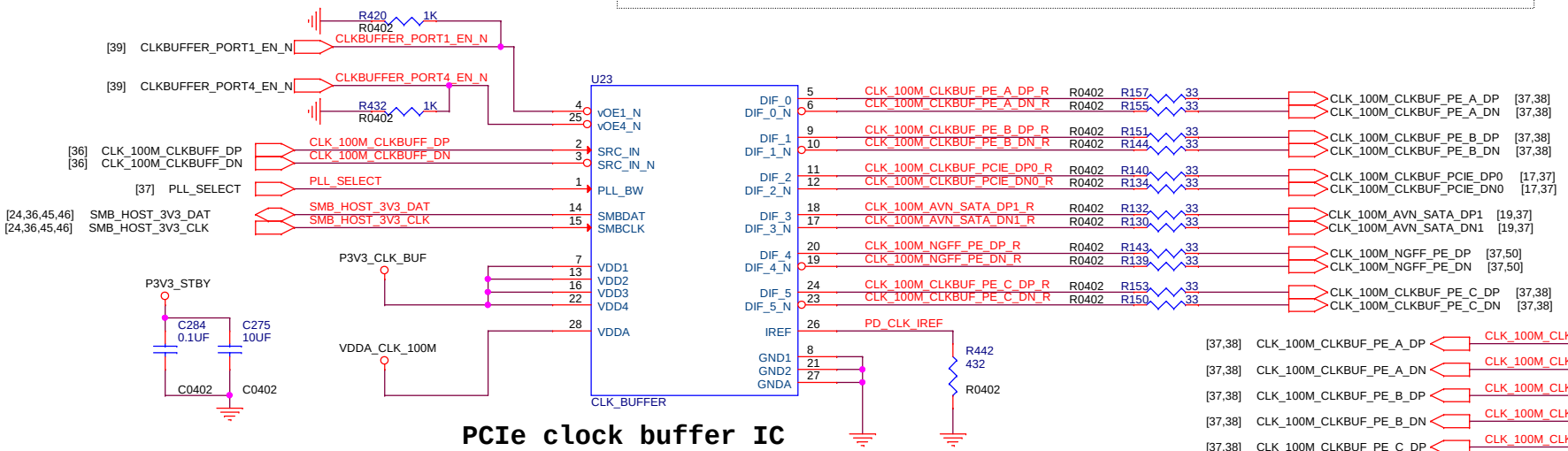
DIMM VREF

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title DIMM VREF	
			Size B Date: Thursday, January 22, 2015	Sheet 35 of 66	


ADDRESS = 0xD2
U22
U21
U42
U14
P3V3_STBY
P3V3
L14
L10
L9
L0603
R362 2.2
R0603
R117 2.2
P3V3_CLK_PCI_R
P3V3_CLK_VDD25_48_R
P3V3_CLK_PCI
P3V3_CLK_XTAL
C239 10UF
C59 0.1UF
C63 0.1UF
C67 0.1UF
C64 0.1UF
C70 0.1UF
C71 10UF
C0402
C0603
C68 10UF
C78 0.1UF
C73 0.1UF
P3V3_CLK_VDD25
P1V5_CLK_VDD_CORE_15
P1V5_CLK_VDDDIF15
P1V5_CLK_SCR
VDDREF
VDDPCI_3.3
VDD25
VDD48
VDD_CORE_1.5_1
VDD_CORE_1.5_2
VDDDIF_CORE_1.5
VDDSRC_LVIO
SMB_HOST_3V3_DAT
SMB_HOST_3V3_CLK
SDATA_3.3
SCLK_3.3
CLKREQB_N
CLK_PWRGD
^^FSA|CLKREQB#
CLKPWRGD|PD#_3.3
CLK_14M_AVN
CLK_14M_AVN_R
REF0_2X
CLK_PCI_STOP_P3V3
PCI_STOP#_3.3
PCI_F1_2X
PCI2_2X
CLKREQA#|PCI3_2X
VSEL_PCI|25M_PCI4_2X
USB_48MHZ_2X
TH
CLK_GEN
R422 1K
R116 0
PD_CLK_GEN_13
XTAL_CLK_GEN_OUT
XTAL_CLK_GEN_IN
R114 NI 10M
Y2
14.31818MHZ
C60 18PF
C65 18PF
X2
X1
SRC1_LRS
SRC1#_LRS
CLK_100M_AVN_MPLL1_DP
CLK_100M_AVN_MPLL1_DN
SRC2_LRS
SRC2#_LRS
CLK_100M_AVN_HFHPLL_DP
CLK_100M_AVN_HFHPLL_DN
SRC3_LRS
SRC3#_LRS
CLK_100M_AVN_MPLL0_DP
CLK_100M_AVN_MPLL0_DN
SRC4_LRS
SRC4#_LRS
CLK_100M_XDP_R_DP
CLK_100M_XDP_R_DN
SRC5_LRS
SRC5#_LRS
CLK_100M_CLKBUFF_DP
CLK_100M_CLKBUFF_DN
DOT96_LRS|SRC6_LRS
DOT96#_LRS|SRC6#_LRS
CLK_96M_AVN_USB_DP
CLK_96M_AVN_USB_DN
SATA_LRS
SATA#_LRS
CLK_100M_AVN_SATA3_DP
CLK_100M_AVN_SATA3_DN
DIF0_LRS
DIF0#_LRS
CLK_100M_AVN_GBE_DP
CLK_100M_AVN_GBE_DN
DIF1_LRS
DIF1#_LRS
CLK_100M_CLKBUF_FPGA_DP_R
CLK_100M_CLKBUF_FPGA_DN_R
R122 NI 0
R129 NI 0
CLK_100M_CLKBUF_FPGA_DP
CLK_100M_CLKBUF_FPGA_DN
DIF_STOP#_3.3
CLK_DIF_STOP_3V3
R149 4.7K
GNDPCI
GND25
GND48
GNDSATA
GNDSRC_1
GNDSRC_2
GNDDIF
GNDREF
P1V5_STBY
R147 2.2
C273 10UF
C263 0.1UF
R145 2.2
C82 10UF
C80 0.1UF
R154 2.2
C280 10UF
C87 0.1UF
R113 8.2K
PU_CLKPWRGD_G
C77 1UF
CLK_PWRGD_N
C75 0.1UF
R473 33
CLKPG
R472 0
CLK_PWRGD_OE_N
C320 0.1UF
CLKPWRGD_L
C196 0.1UF
R397 1.69K
R407 10K
R76 10K
R354 0
SLP_S3_N
SLP_S3_N_R
CLK_PWRGD_DELAYED
PWRGD_COREPWR
R0402
R0603
C0603
C0402
NI
IC
1A
1Y
GND
VCC
2A
2Y
OE#
A
VCC
Y
FSLA
DIF (MHz)
*0
*100.00
1
125.00
CLOCK GEN
Quanta
Department CCBU
Designer Tony_C
Reviewer <Name>
Project MF1
Doc Number <Doc>
Page Title CLK_GENERATOR
Rev 0.05
Size B
Date: Thursday, January 22, 2015
Sheet 36 of 66







TO Gold finger

TO Gold finger

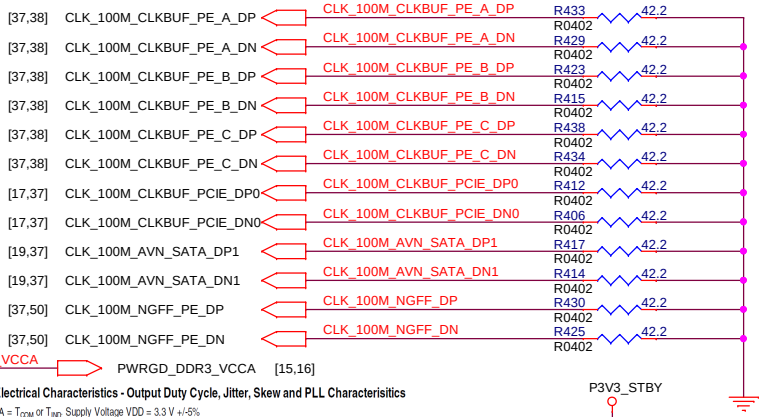
TO CPU

TO CPU

TO NGFF

TO Gold finger

PCIe clock buffer IC
SMB address: D4/D5



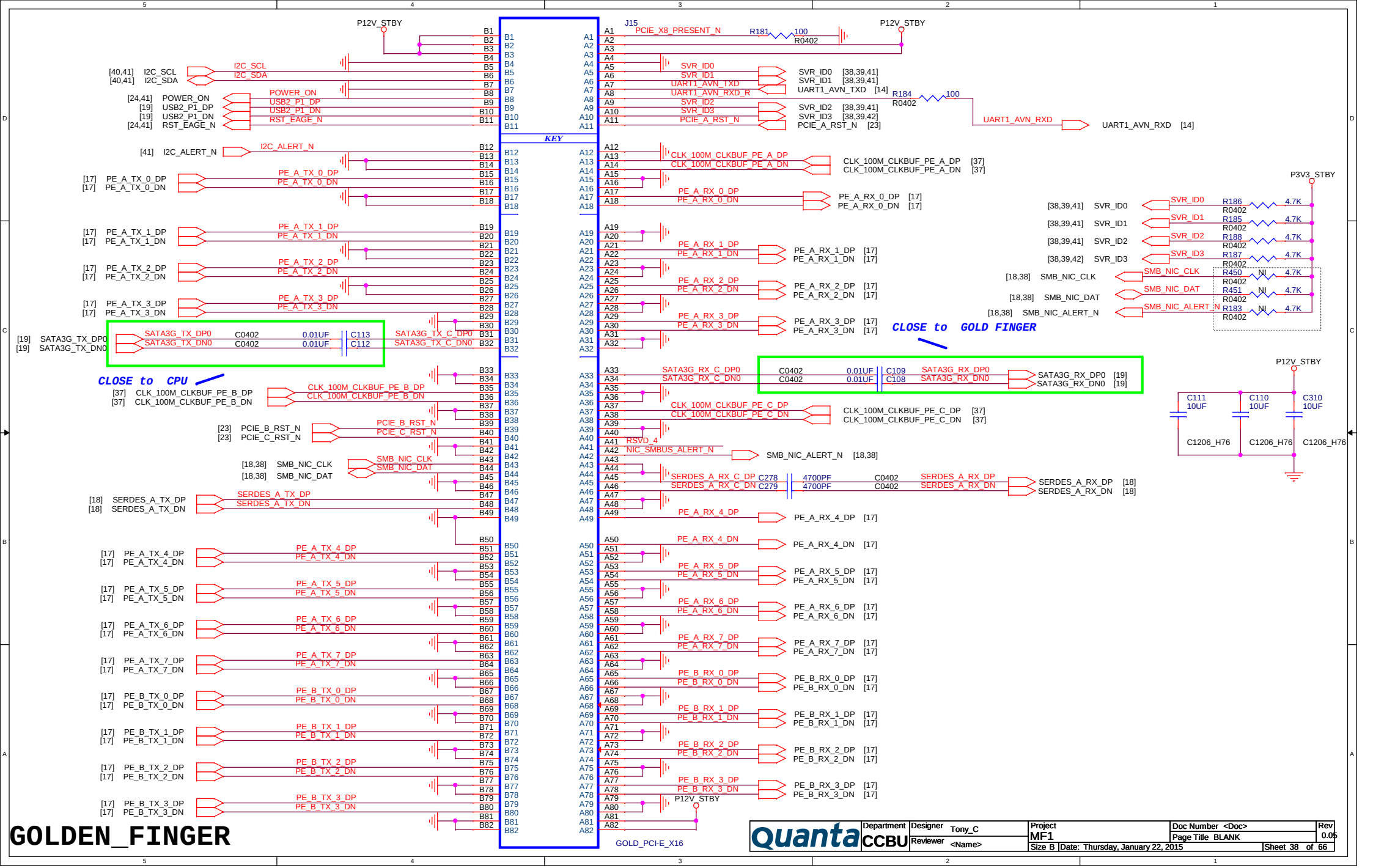
Electrical Characteristics - Output Duty Cycle, Jitter, Skew and PLL Characterisitics

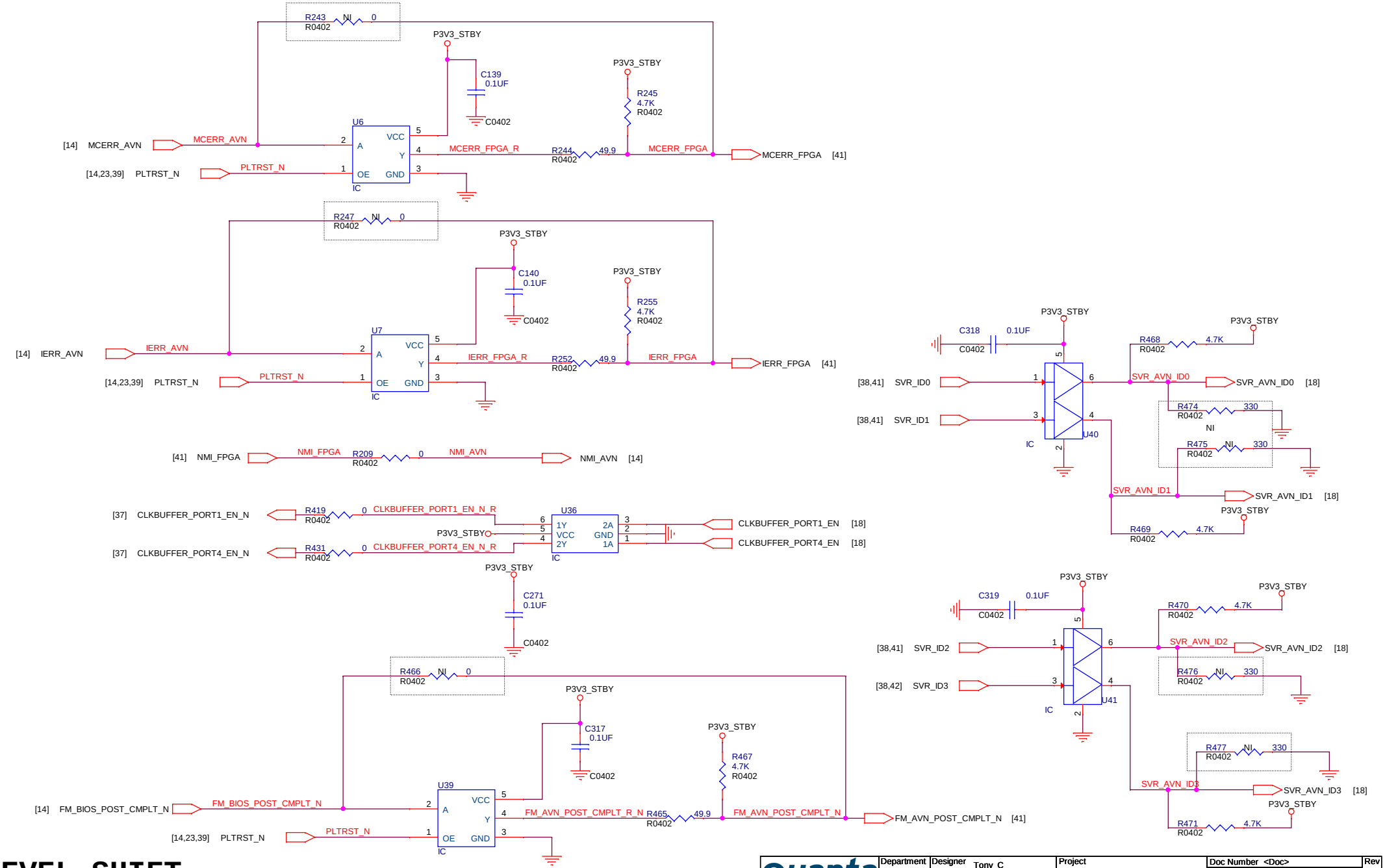
TA = T_{COM} or T_{IND}, Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PLL Bandwidth	BW	-3dB point in High BW Mode	2	2.3	4	MHz	1
		-3dB point in Low BW Mode	0.4	0.5	1	MHz	1

CLOCK BUFFER

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc> Rev 0.05
		Reviewer <Name>	Size B Date: Thursday, January 22, 2015	Page Title Clock Buffer Sheet 37 of 66


GOLDEN_FINGER
P12V_STBY
P3V3_STBY
KEY
J15
PCIE_X8_PRESENT_N
R181 100 R0402
R184 100 R0402
UART1_AVN_RXD
CLOSE to CPU
CLOSE to GOLD FINGER
SATA3G_TX_DP0
SATA3G_TX_DN0
SATA3G_TX_C_DP0
SATA3G_TX_C_DN0
C0402 0.01UF C113
C0402 0.01UF C112
SATA3G_RX_C_DP0
SATA3G_RX_C_DN0
C0402 0.01UF C109
C0402 0.01UF C108
SATA3G_RX_DP0
SATA3G_RX_DN0
CLK_100M_CLKBUF_PE_B_DP
CLK_100M_CLKBUF_PE_B_DN
CLK_100M_CLKBUF_PE_A_DP
CLK_100M_CLKBUF_PE_A_DN
CLK_100M_CLKBUF_PE_C_DP
CLK_100M_CLKBUF_PE_C_DN
PCIE_B_RST_N
PCIE_C_RST_N
SMB_NIC_CLK
SMB_NIC_DAT
SMB_NIC_ALERT_N
SERDES_A_TX_DP
SERDES_A_TX_DN
SERDES_A_RX_C_DP
SERDES_A_RX_C_DN
C278 4700PF C0402 SERDES_A_RX_DP
C279 4700PF C0402 SERDES_A_RX_DN
SERDES_A_RX_DP
SERDES_A_RX_DN
I2C_SCL
I2C_SDA
I2C_ALERT_N
POWER_ON
USB2_P1_DP
USB2_P1_DN
RST_EAGE_N
SVR_ID0
SVR_ID1
SVR_ID2
SVR_ID3
UART1_AVN_TXD
UART1_AVN_RXD_R
PCIE_A_RST_N
RSVD_4
NIC_SMBUS_ALERT_N
PE_A_TX_0_DP
PE_A_TX_0_DN
PE_A_TX_1_DP
PE_A_TX_1_DN
PE_A_TX_2_DP
PE_A_TX_2_DN
PE_A_TX_3_DP
PE_A_TX_3_DN
PE_A_TX_4_DP
PE_A_TX_4_DN
PE_A_TX_5_DP
PE_A_TX_5_DN
PE_A_TX_6_DP
PE_A_TX_6_DN
PE_A_TX_7_DP
PE_A_TX_7_DN
PE_B_TX_0_DP
PE_B_TX_0_DN
PE_B_TX_1_DP
PE_B_TX_1_DN
PE_B_TX_2_DP
PE_B_TX_2_DN
PE_B_TX_3_DP
PE_B_TX_3_DN
PE_A_RX_0_DP
PE_A_RX_0_DN
PE_A_RX_1_DP
PE_A_RX_1_DN
PE_A_RX_2_DP
PE_A_RX_2_DN
PE_A_RX_3_DP
PE_A_RX_3_DN
PE_A_RX_4_DP
PE_A_RX_4_DN
PE_A_RX_5_DP
PE_A_RX_5_DN
PE_A_RX_6_DP
PE_A_RX_6_DN
PE_A_RX_7_DP
PE_A_RX_7_DN
PE_B_RX_0_DP
PE_B_RX_0_DN
PE_B_RX_1_DP
PE_B_RX_1_DN
PE_B_RX_2_DP
PE_B_RX_2_DN
PE_B_RX_3_DP
PE_B_RX_3_DN
R186 4.7K R0402
R185 4.7K R0402
R188 4.7K R0402
R187 4.7K R0402
R450 NI 4.7K R0402
R451 NI 4.7K R0402
R183 NI 4.7K R0402
C111 10UF C1206_H76
C110 10UF C1206_H76
C310 10UF C1206_H76
GOLD_PCI-E_X16
Quanta
Department CCBU
Designer Tony_C
Reviewer <Name>
Project MF1
Doc Number <Doc>
Page Title BLANK
Rev 0.05
Size B Date: Thursday, January 22, 2015
Sheet 38 of 66

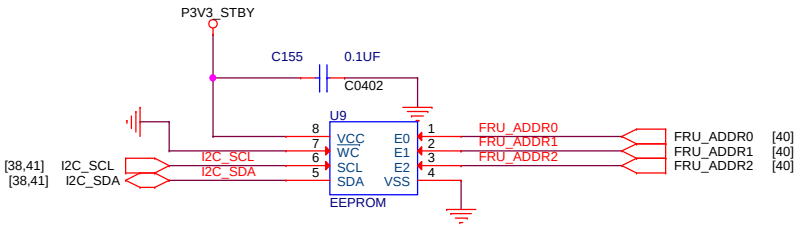


LEVEL_SHIFT

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title LEVEL_SHIFT	
			Size B Date: Thursday, January 22, 2015	Sheet 39 of 66	

SMBus (8-bit) Address:0xA2

FRU



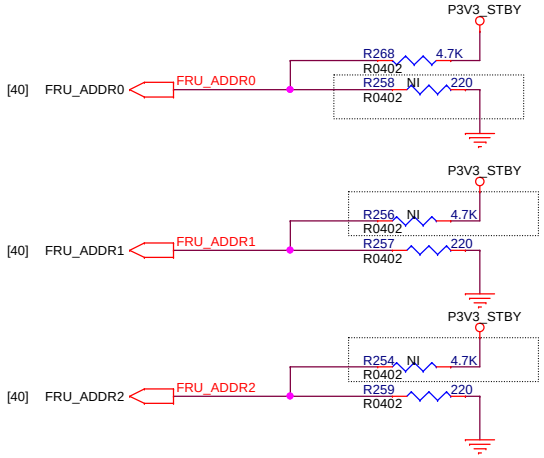


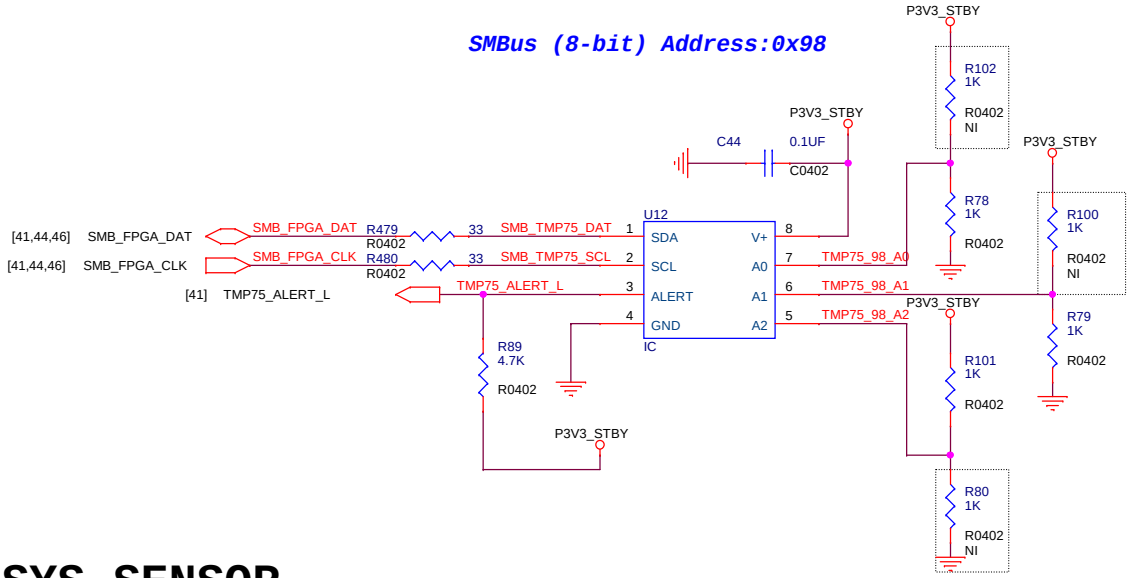
Table 2. Device Select Code

	Device Type Identifier[1]				Chip Enable Address[2]			$\overline{RW}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device Select Code	1	0	1	0	E2	E1	E0	$\overline{RW}$

Note: 1. The most significant bit, b7, is sent first.
2. E0, E1 and E2 are compared against the respective external pins on the memory device.

FRU address

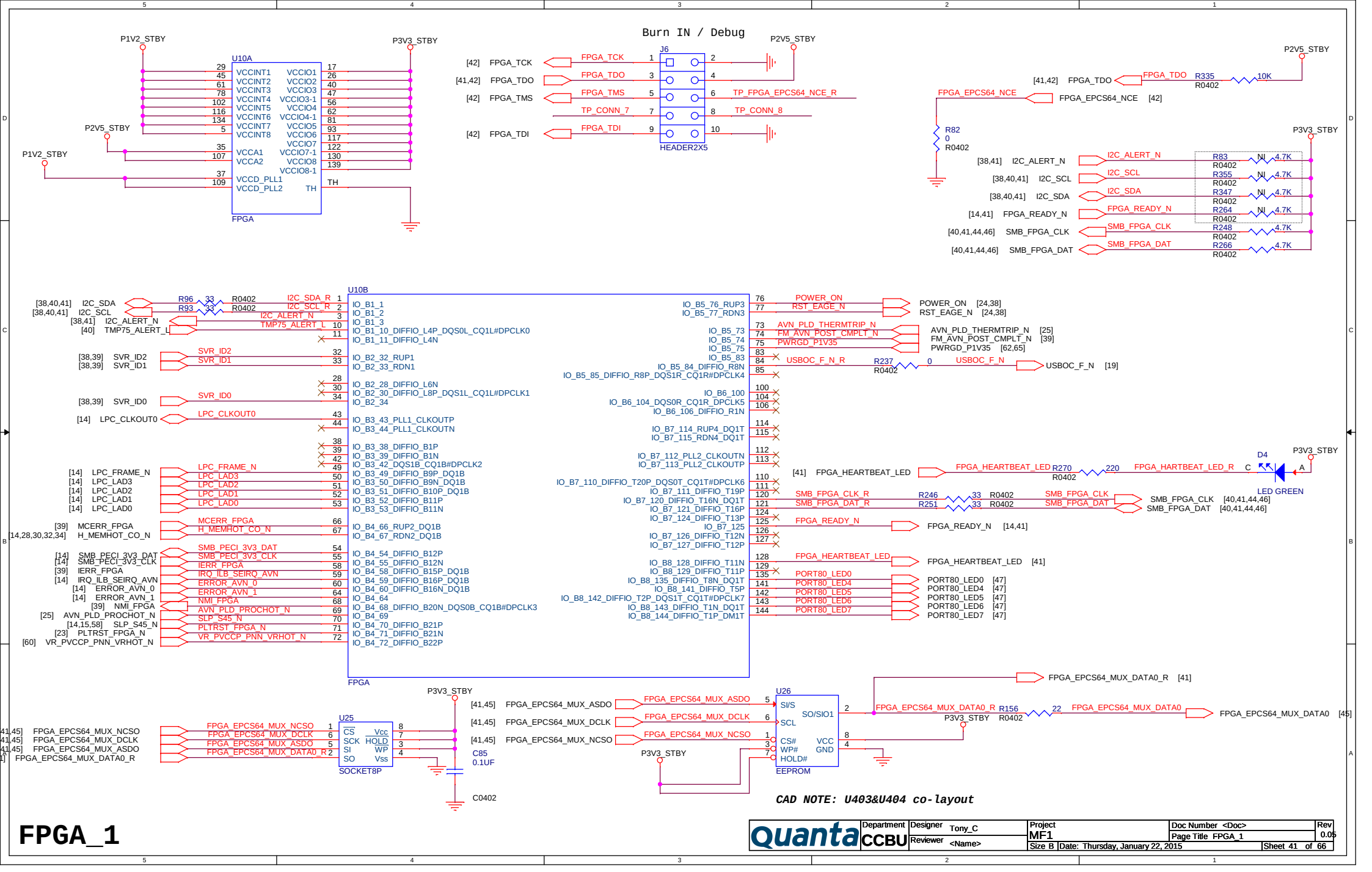
SMBus (8-bit) Address:0x98



A2	A1	A0	SLAVE ADDRESS
0	0	0	1001000
0	0	1	1001001
0	1	0	1001010
0	1	1	1001011
1	0	0	1001100
1	0	1	1001101
1	1	0	1001110
1	1	1	1001111

Table 12. Address Pins and Slave Addresses for the TMP75

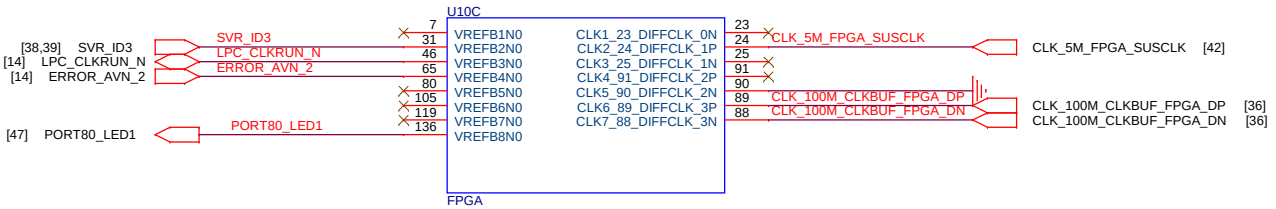
SYS_SENSOR



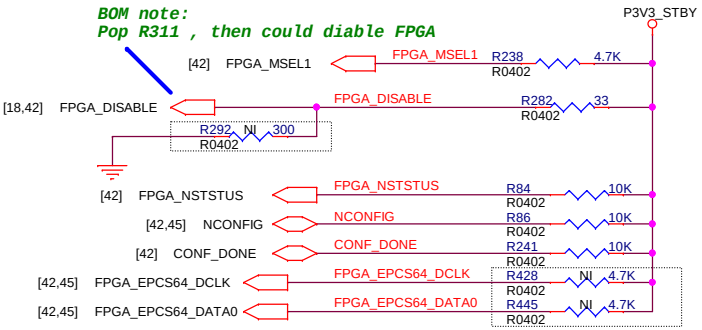
FPGA_1

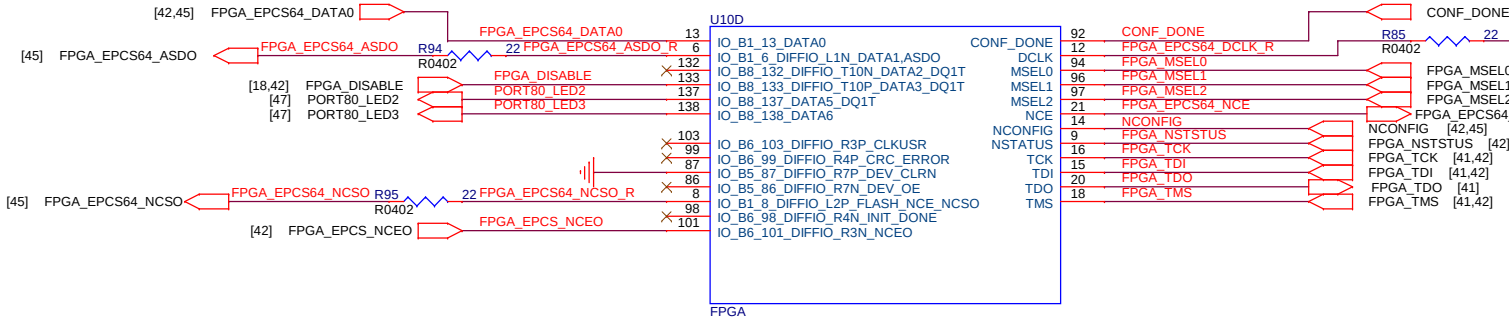
Quanta	Department CCBU	Designer Tony_C	Project MF1
		Reviewer <Name>	Doc Number <Doc>
			Page Title FPGA_1
		Size B Date: Thursday, January 22, 2015	Sheet 41 of 66

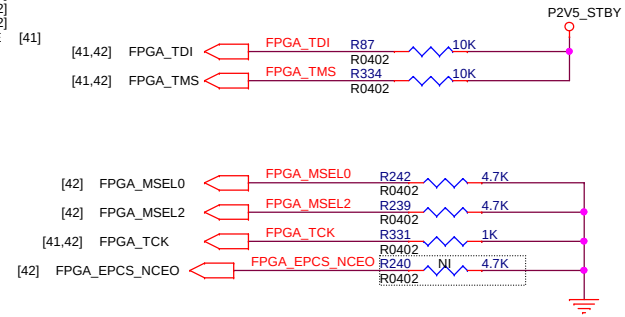
Rev 0.05



BOM note:
Pop R311 , then could diable FPGA







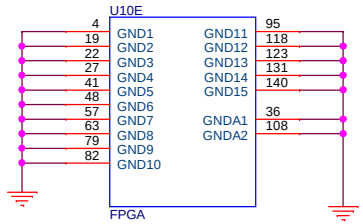
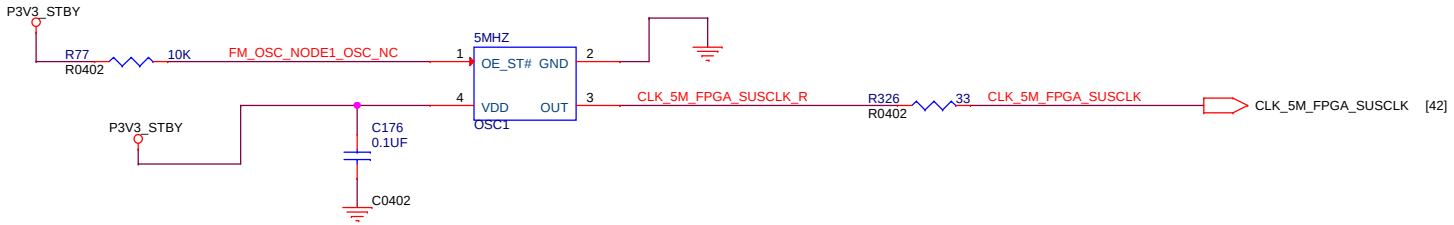


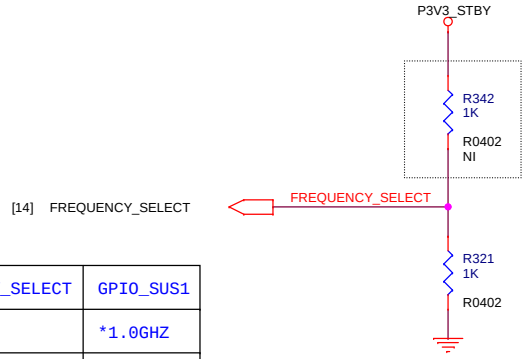
Table 8–5. Configuration Schemes for Cyclone IV E Devices

Configuration Scheme	MSEL3	MSEL2	MSEL1	MSEL0	POR Delay	Configuration Voltage Standard (V) *(1)*
AS	1	1	0	1	Fast	3.3
	0	1	0	0	Fast	3.0, 2.5
	0	0	1	0	Standard	3.3
	0	0	1	1	Standard	3.0, 2.5



FPGA_2

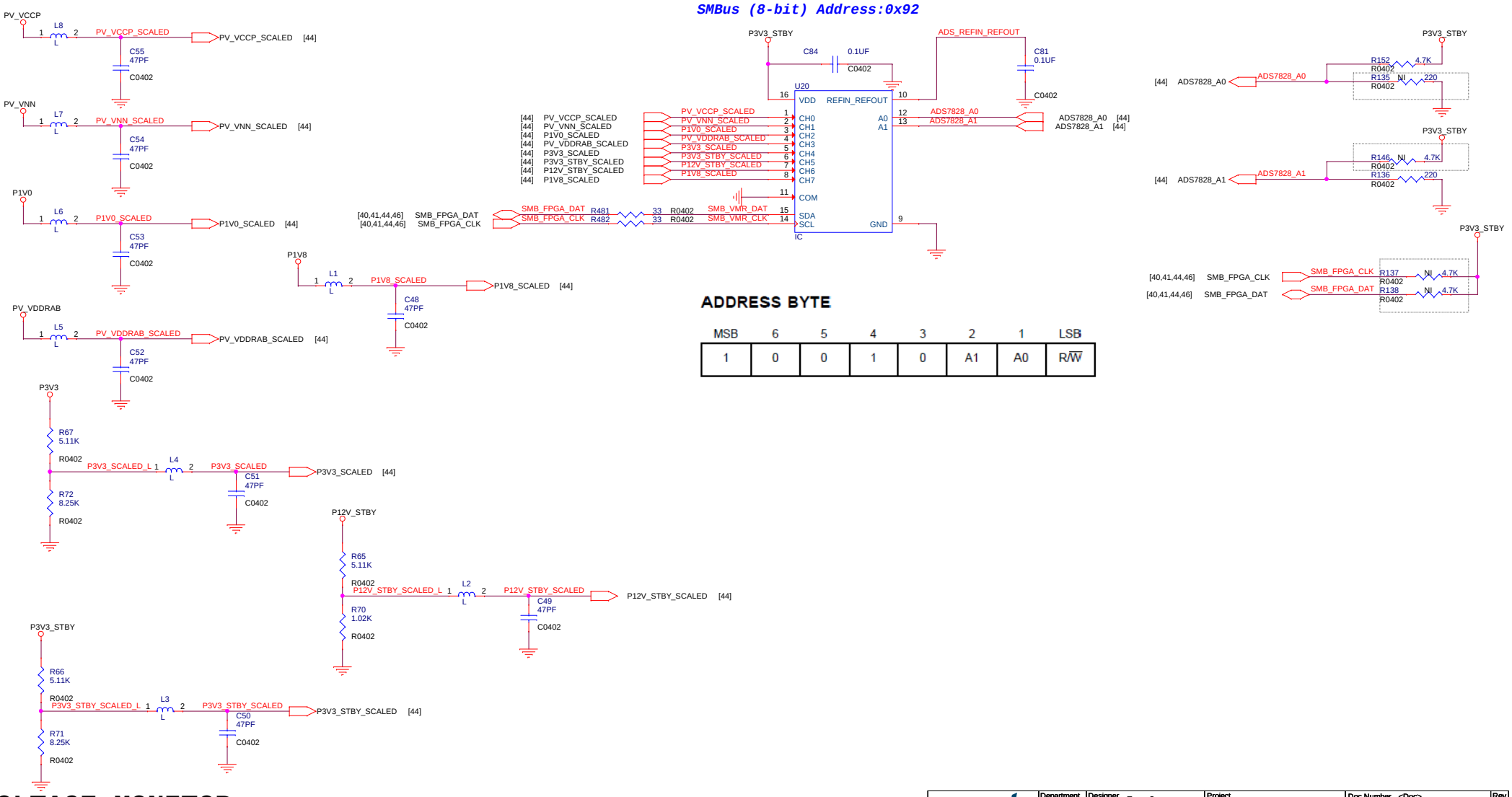
Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>	Size B Date: Thursday, January 22, 2015	Page Title FPGA_2	Sheet 42 of 66



FREQUENCY_SELECT	GPIO_SUS1
*0	*1.0GHZ
1	2.5GHZ

CPU_LAN_FREQUENCY_SWITCH

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.0
		Reviewer <Name>	Size B Date: Thursday, January 22, 2015	Page Title CPU_LAN_FREQUENCY_SWITCH	Sheet 43 of 66

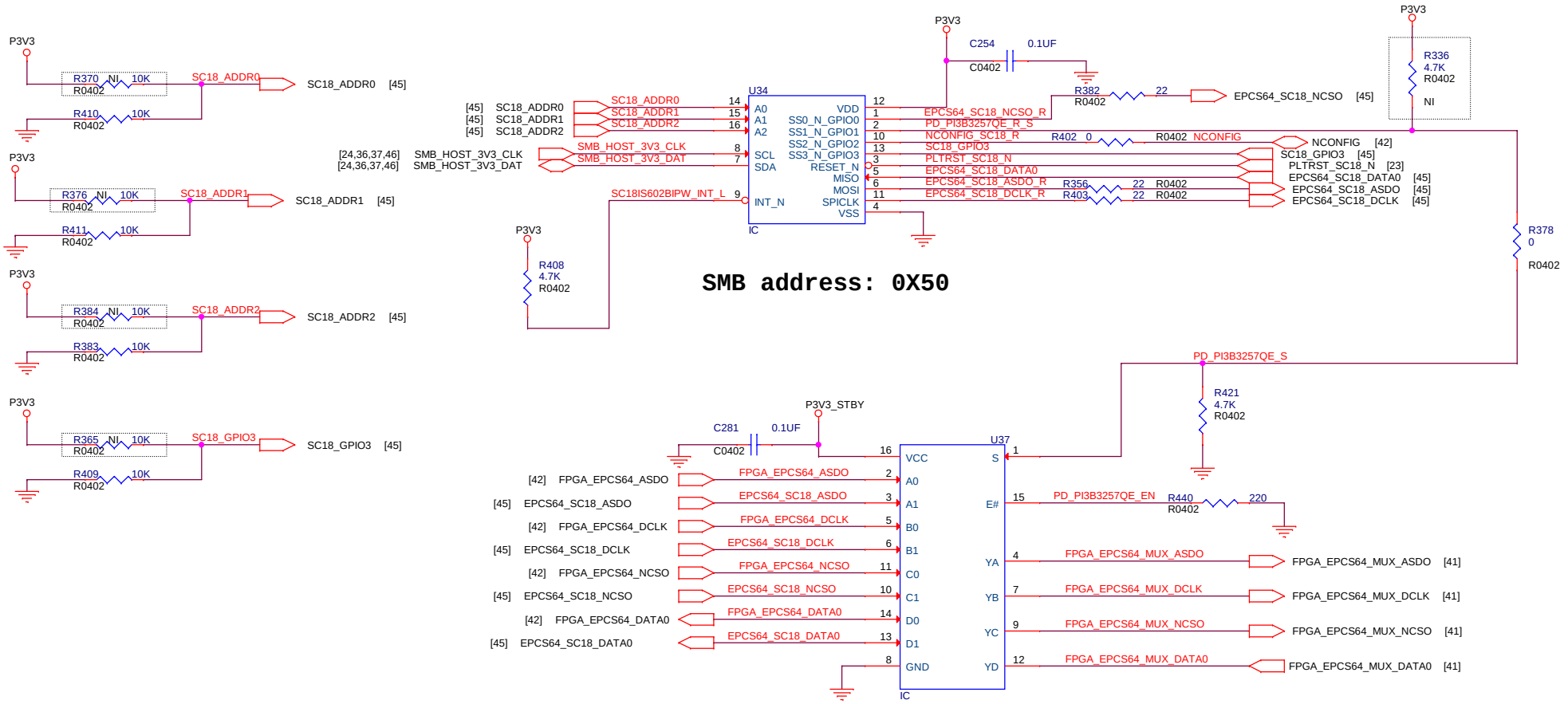


ADDRESS BYTE

MSB	6	5	4	3	2	1	LSB
1	0	0	1	0	A1	A0	R/$\overline{W}$

VOLTAGE MONITOR

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title VOLTAGE MONITOR	
			Size Custom Date: Thursday, January 22, 2015		Sheet 44 of 66



Truth Table[1]

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

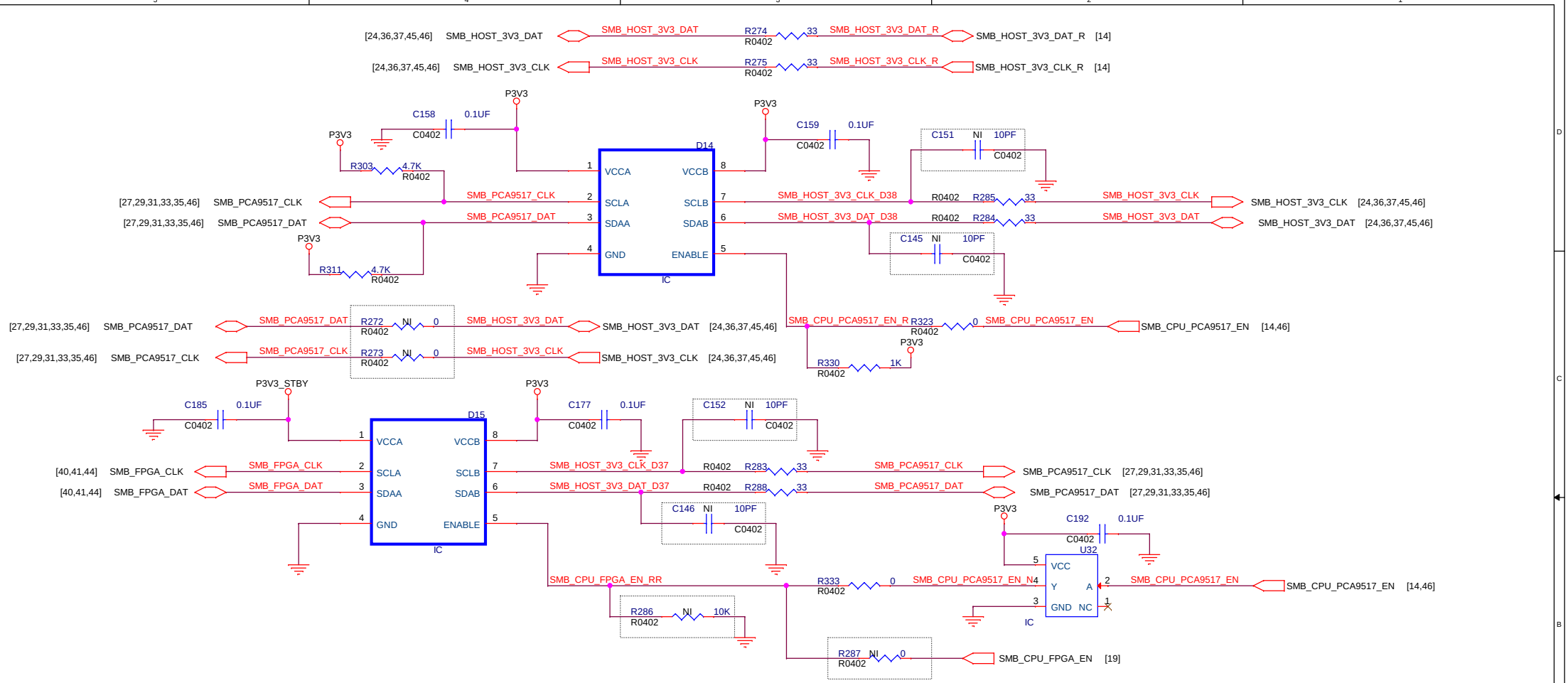
Note:
1. H = High Voltage Level, L = Low Voltage Level

Pin Description

Pin Name	Description
IAn-IDn	Data Inputs
S	Select Inputs
$\overline{E}$	Enable
YA-YD	Data Outputs
GND	Ground
Vcc	Power
NC	No Connect

I2C-BUS TO SPI BRIDGE

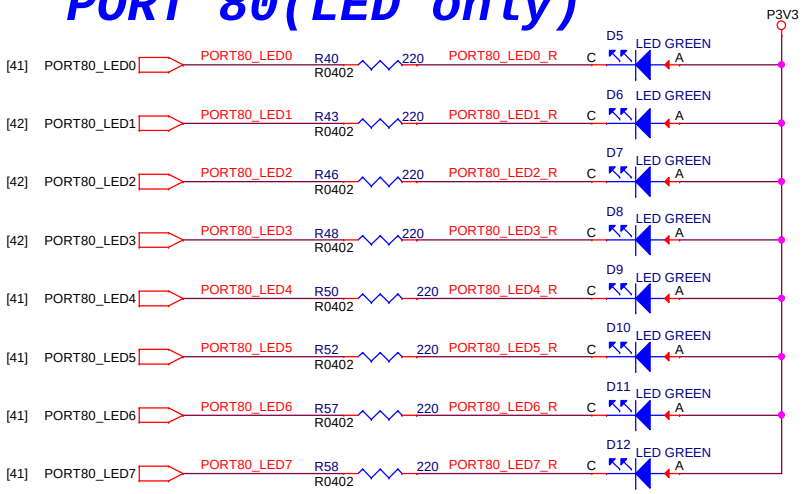
Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title I2C-BUS TO SPI BRIDGE	
			Size B Date: Thursday, January 22, 2015	Sheet 45 of 66	



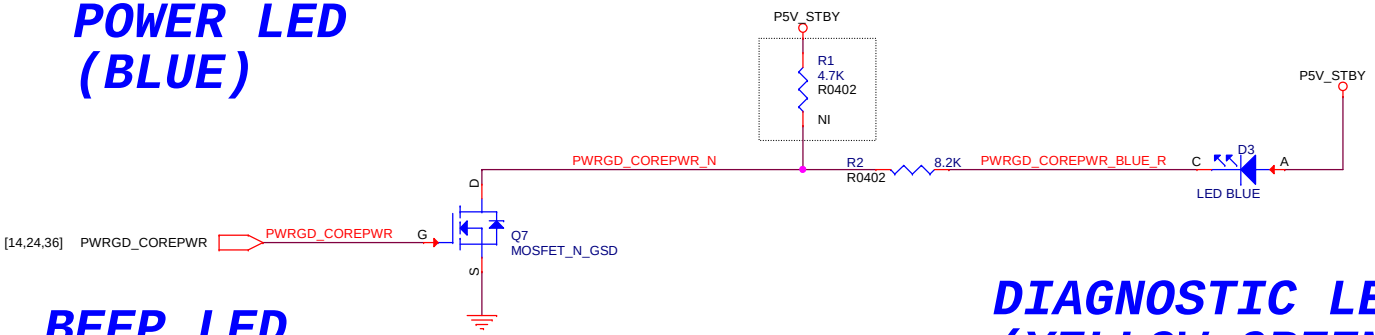
SMBUS ISOLATOR

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title SMBUS ISOLATOR	
			Size B Date: Thursday, January 22, 2015	Sheet 46 of 66	

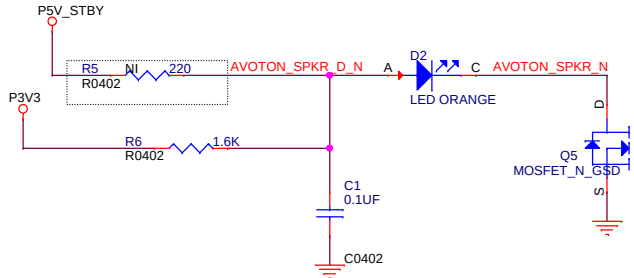
PORT 80(LED only)



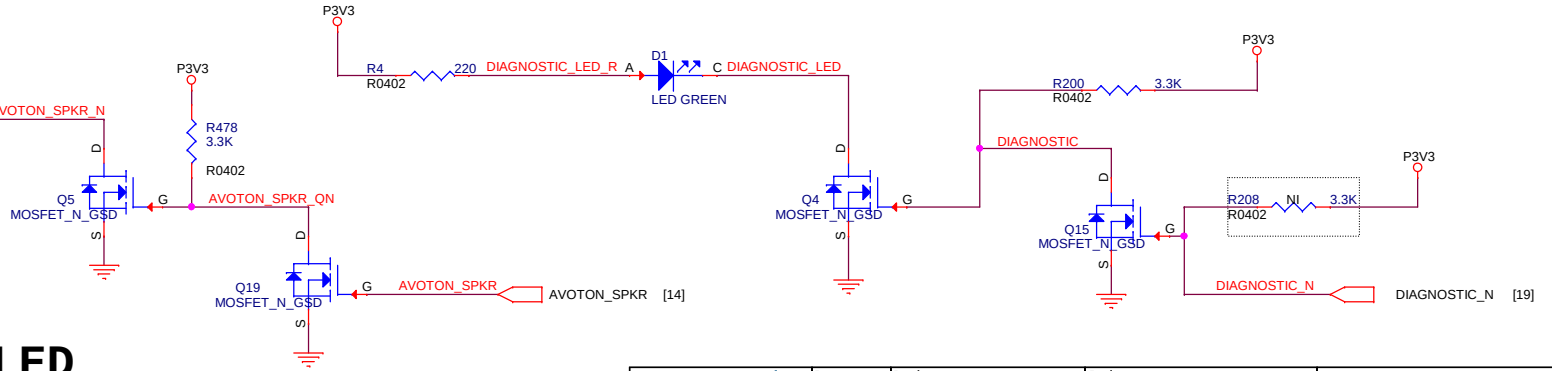
POWER LED (BLUE)



BEEP LED (Orange)



DIAGNOSTIC LED (YELLOW-GREEN)

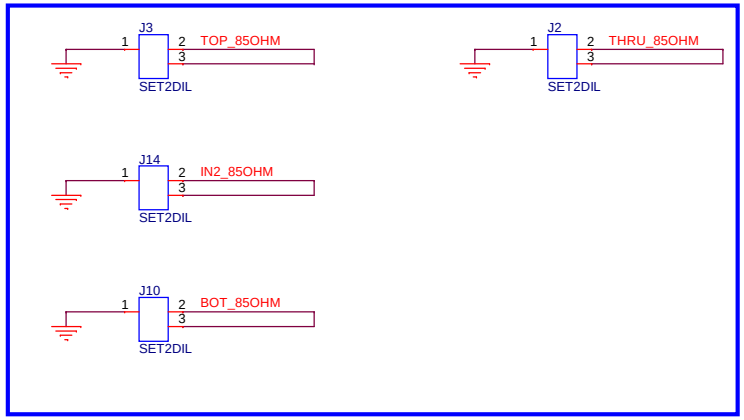


PWR/ BEEP/ PORT 80 LED

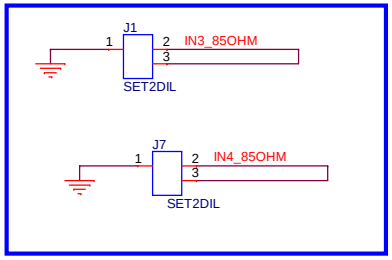
Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title PWR/ BEEP/ PORT 80 LED	
			Size B Date: Thursday, January 22, 2015		Sheet 47 of 66

SET2DEL

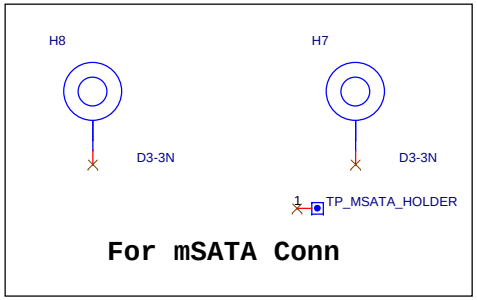
GND1



GND2

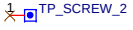


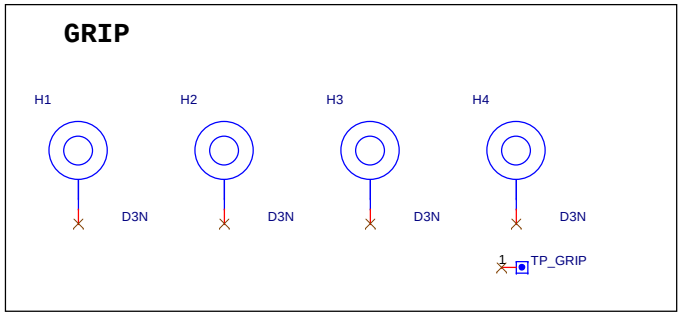
Screw Hole

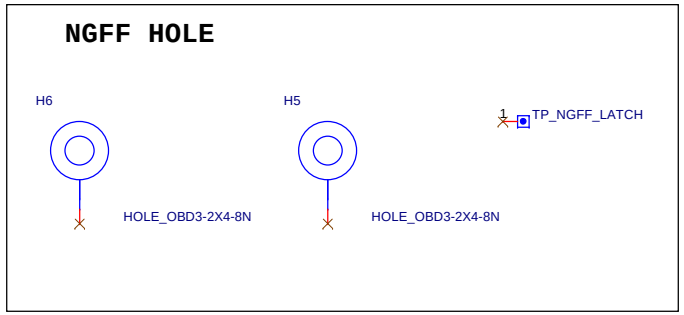








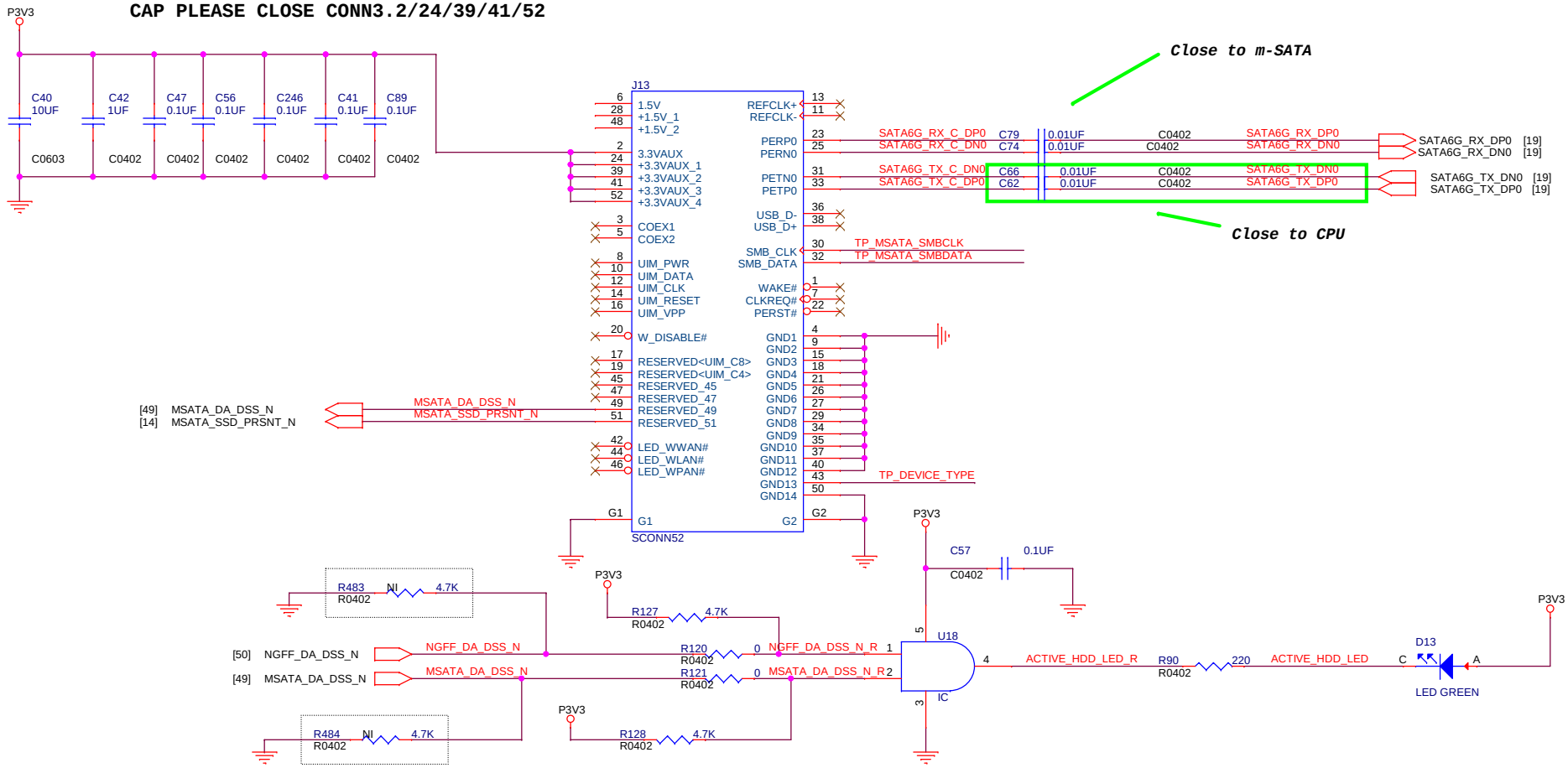




SCREW/TP

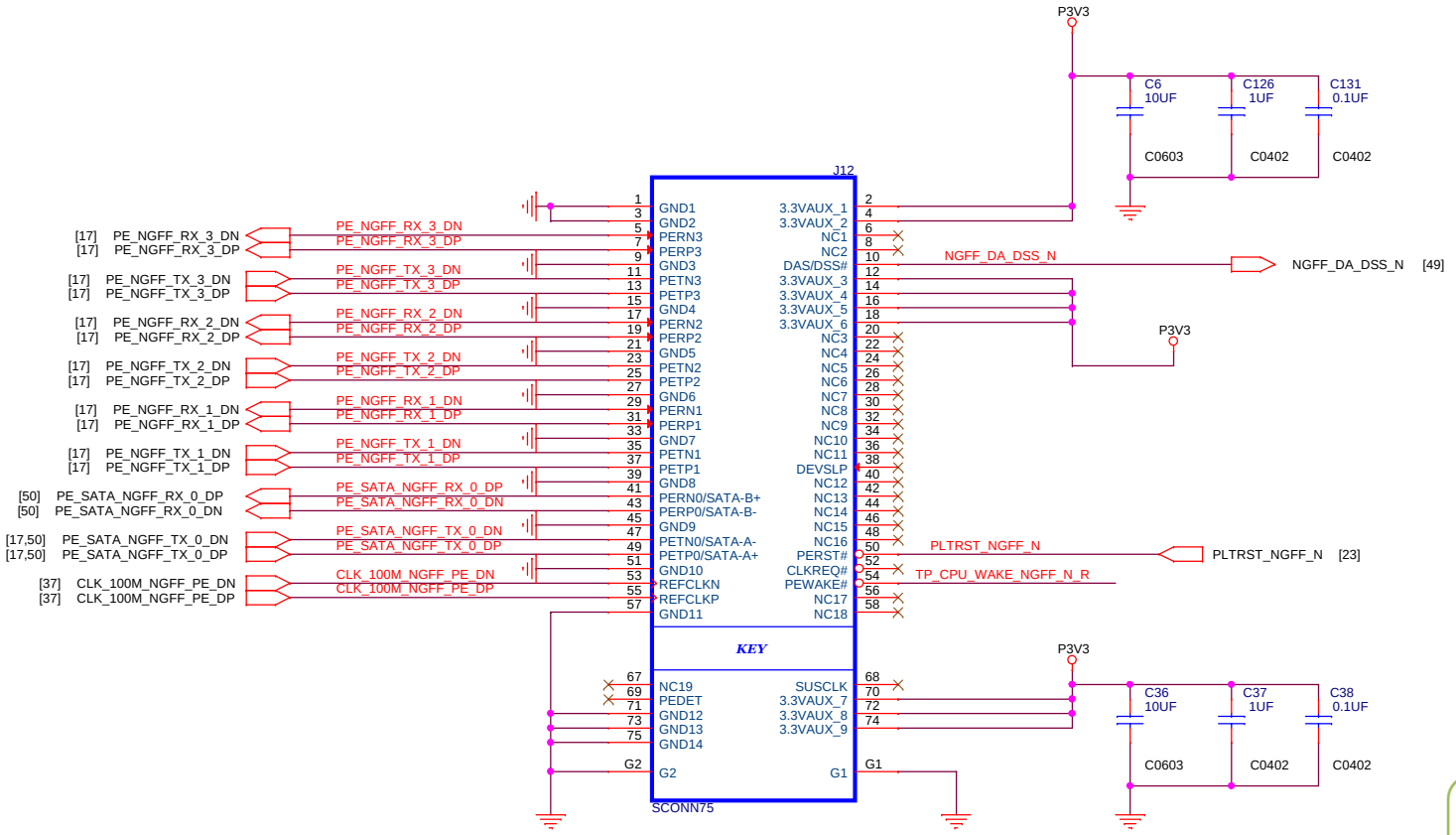
Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title SCREW/TP	
			Size B Date: Thursday, January 22, 2015		Sheet 48 of 66

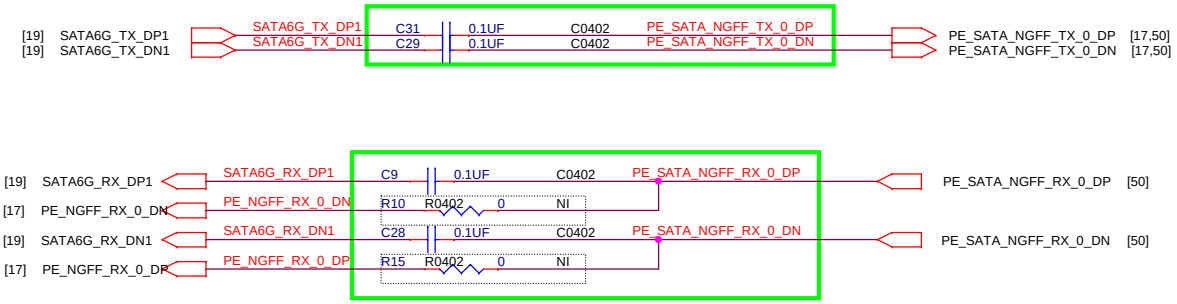
CAD Note
CAP PLEASE CLOSE CONN3.2/24/39/41/52

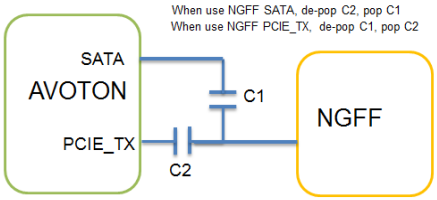


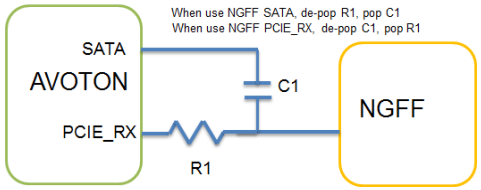
mSATA CONN

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title mSATA CONN	
			Size B Date: Thursday, January 22, 2015	Sheet 49 of 66	





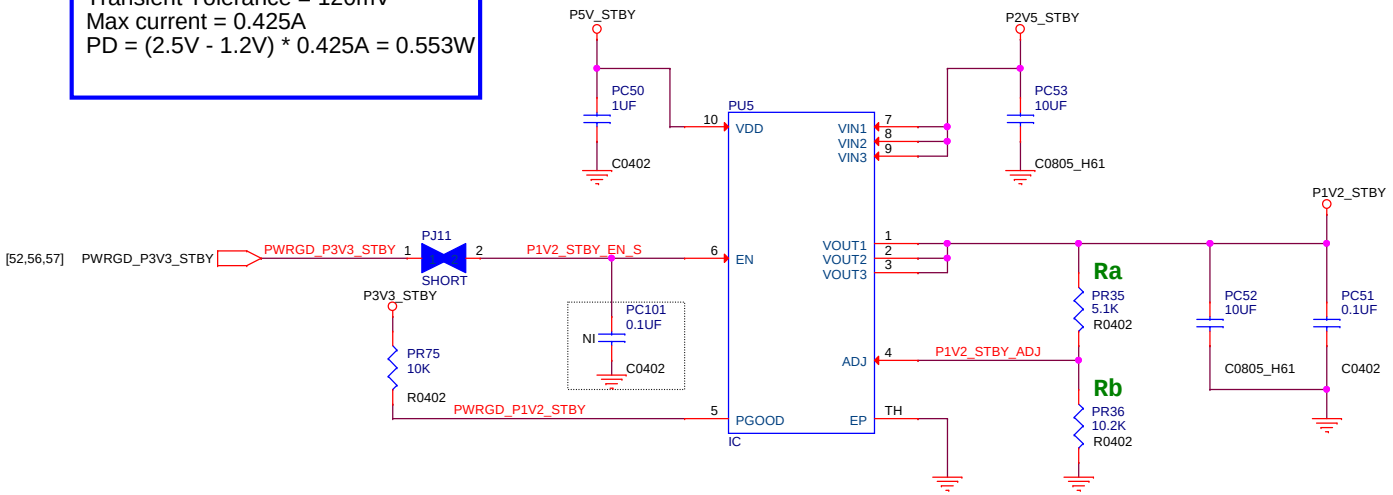




NGFF PCIEx4

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title NGFF PCIEx4	
			Size B Date: Thursday, January 22, 2015		Sheet 50 of 66

Output Voltage = 1.2V+/-5%
Output Ripple & Noise < 30mV
Transient Tolerance = 120mV
Max current = 0.425A
PD = (2.5V - 1.2V) * 0.425A = 0.553W

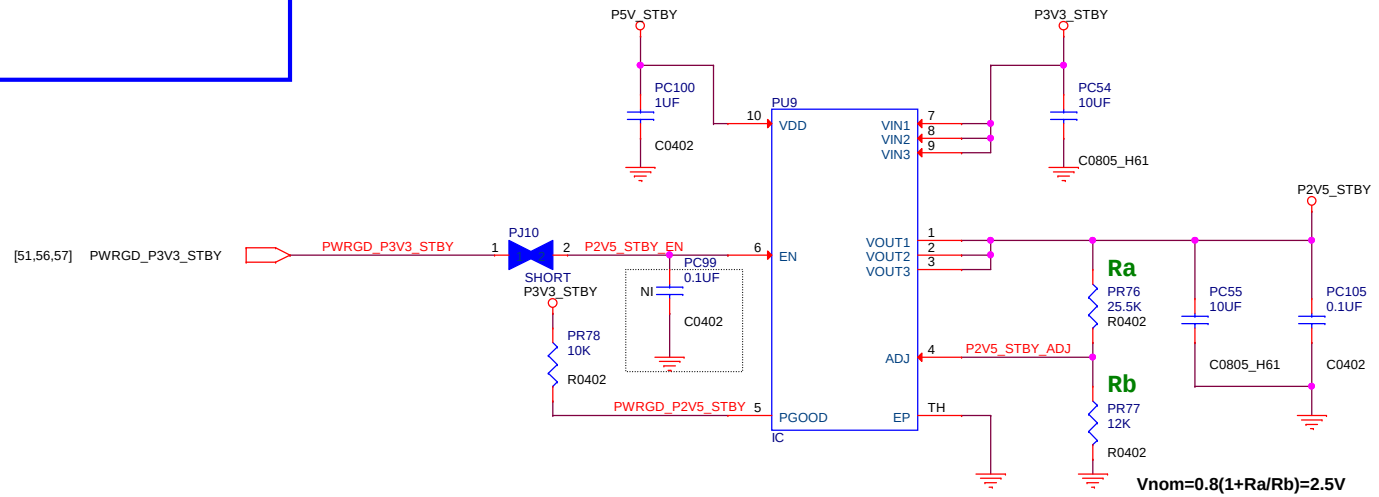


Vnom=0.8(1+Ra/Rb)=1.2 V

P1V2_STBY

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title P1V2_STBY	
			Size B Date: Thursday, January 22, 2015	Sheet 51 of 66	

Output Voltage = 2.5V+/-5%
Output Ripple & Noise < 30mV
Transient Tolerance = 250mV
Max current = 0.525A
PD = (3.3V - 2.5V) * 0.525A = 0.42W

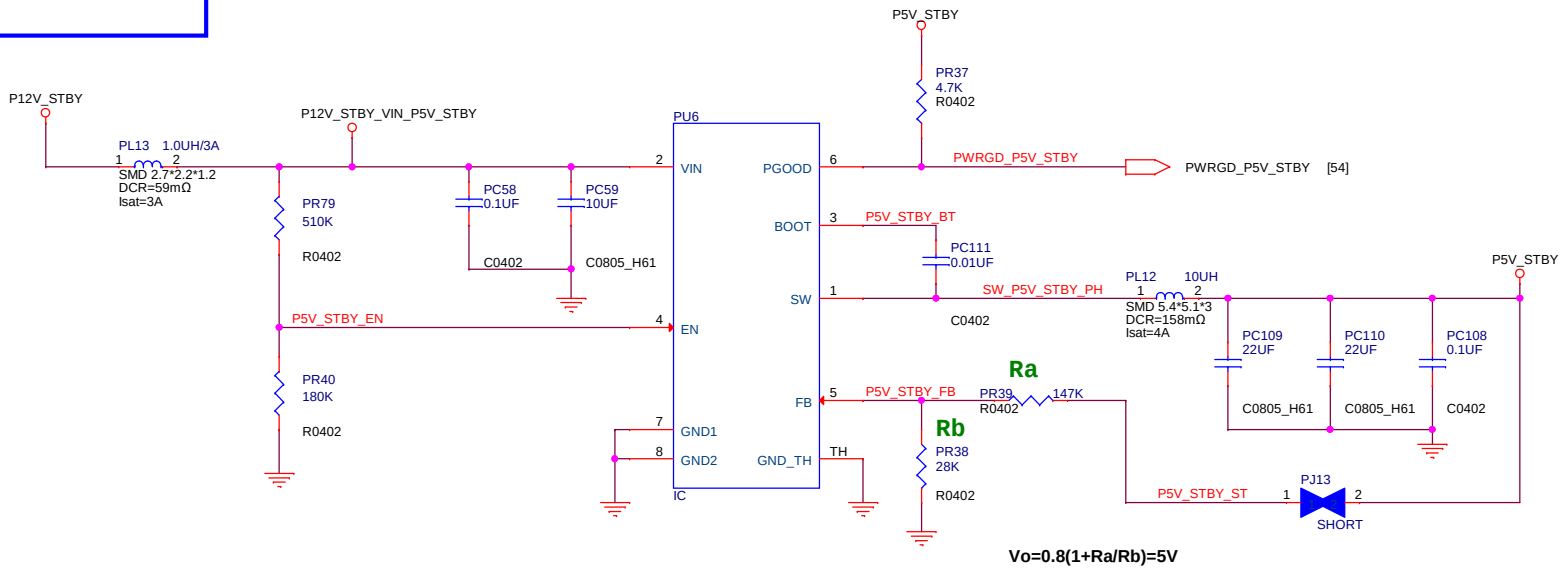


P2V5_STBY

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title P2V5_STBY	
			Size B Date: Thursday, January 22, 2015	Sheet 52 of 66	

Design specification

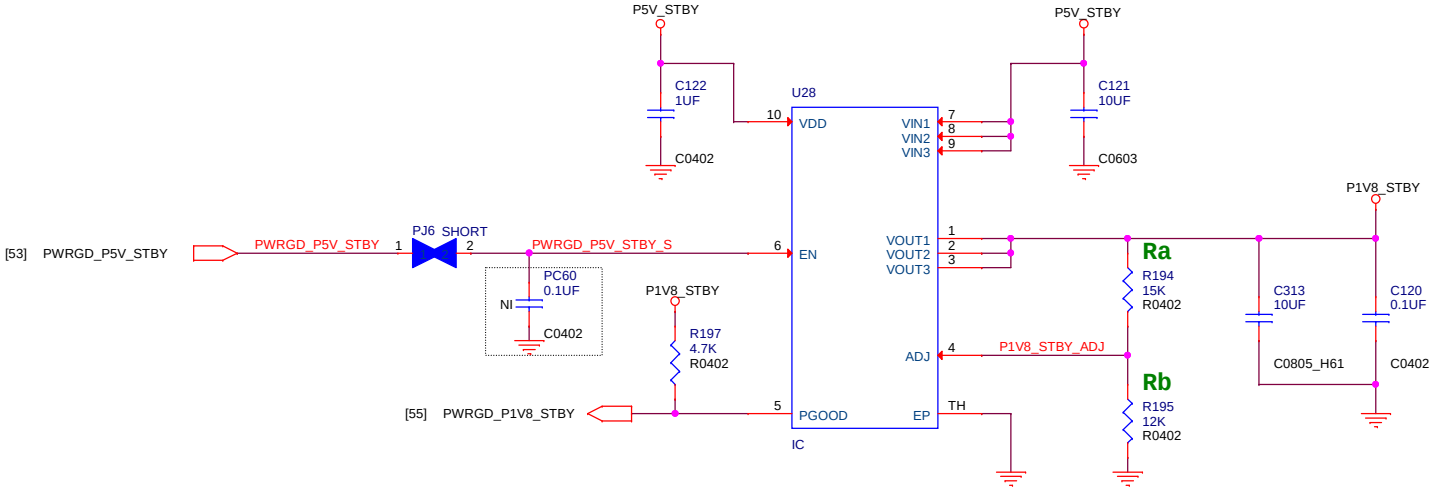
Output Voltage = 5V±5%
Output Ripple & Noise < 50mV
Transient Tolerance = 500mV
TDC = 0.5A
Max current = 0.7A
Over-Current Protection(IC Rating) = 2.6A
Current Step = 0.2A
Slew Rate = 2.5A/us
Work frequency = 800KHZ
Efficiency > 85% @TDC



P5V_STBY

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title P5V STBY	
			Size B	Date: Thursday, January 22, 2015	Sheet 53 of 66

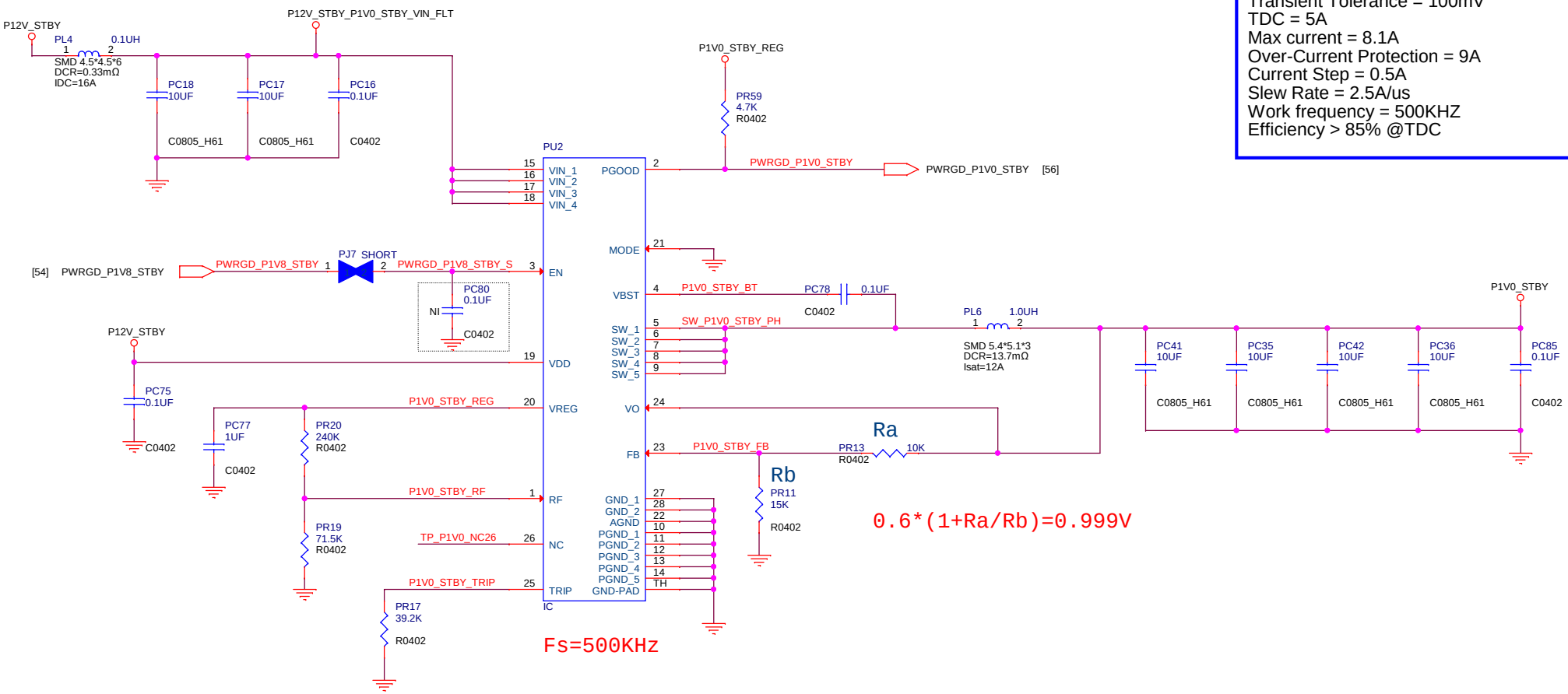
Output Voltage = 1.8V+/-5%
Output Ripple & Noise < 30mV
Transient Tolerance = 180mV
Max current = 0.15A
PD = (5.0V - 1.8V) * 0.15A = 0.48W



VOUT=0.8*(Ra+Rb)/Rb=1.8V

P1V8_STBY

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title P1V8 STBY	
			Size B Date: Thursday, January 22, 2015	Sheet 54 of 66	



Design specification

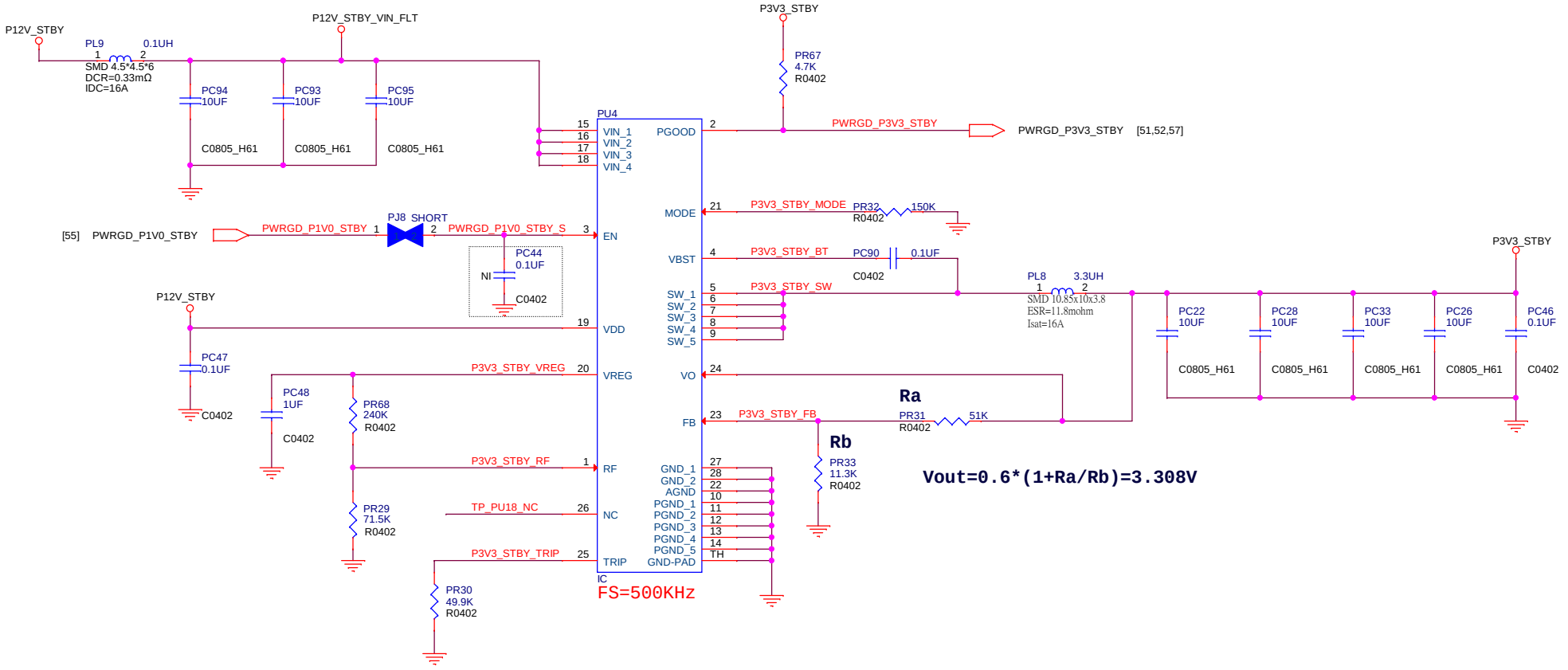
Output Voltage = 1.0V±5%
Output Ripple & Noise < 50mV
Transient Tolerance = 100mV
TDC = 5A
Max current = 8.1A
Over-Current Protection = 9A
Current Step = 0.5A
Slew Rate = 2.5A/us
Work frequency = 500KHZ
Efficiency > 85% @TDC

P1V0_STBY

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title P1V0 STBY	
			Size B	Date: Thursday, January 22, 2015	Sheet 55 of 66

Design specification

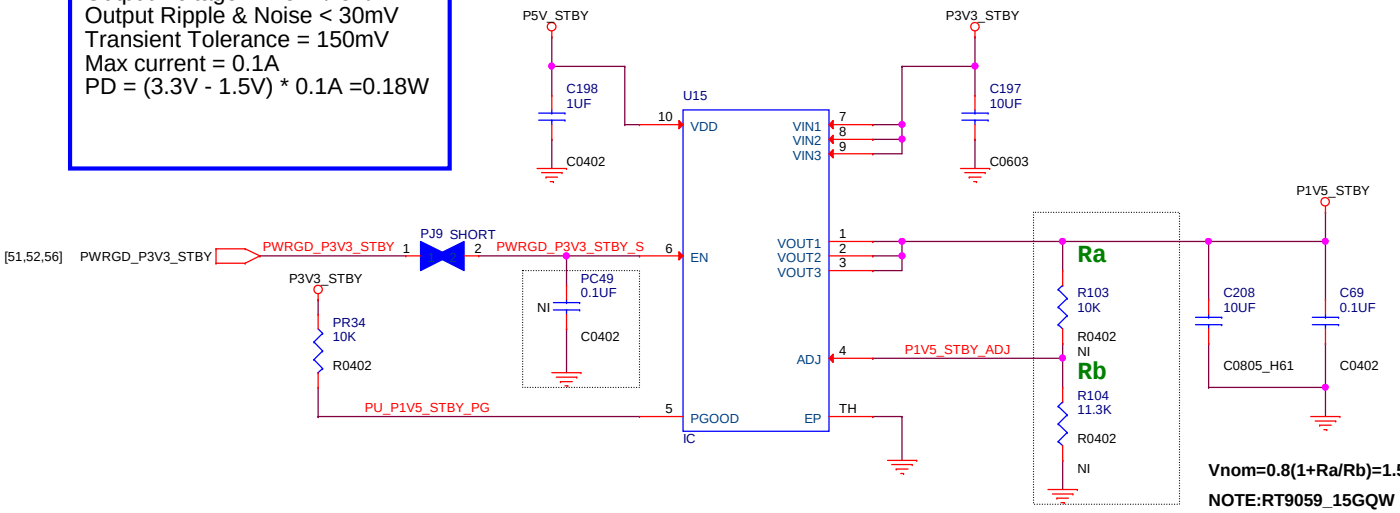
Output Voltage = 3.3V±5%
Output Ripple & Noise < 30mV
Transient Tolerance = 330mV
TDC = 7A
Max current = 8A
Over-Current Protection(Max current * 1.4) = 11.2A
Current Step = 3.5A
Slew Rate = 2.5A/us
Work frequency = 500KHZ
Efficiency > 85% @TDC



P3V3_STBY

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title P3V3 STBY	
			Size B Date: Thursday, January 22, 2015	Sheet 56 of 66	

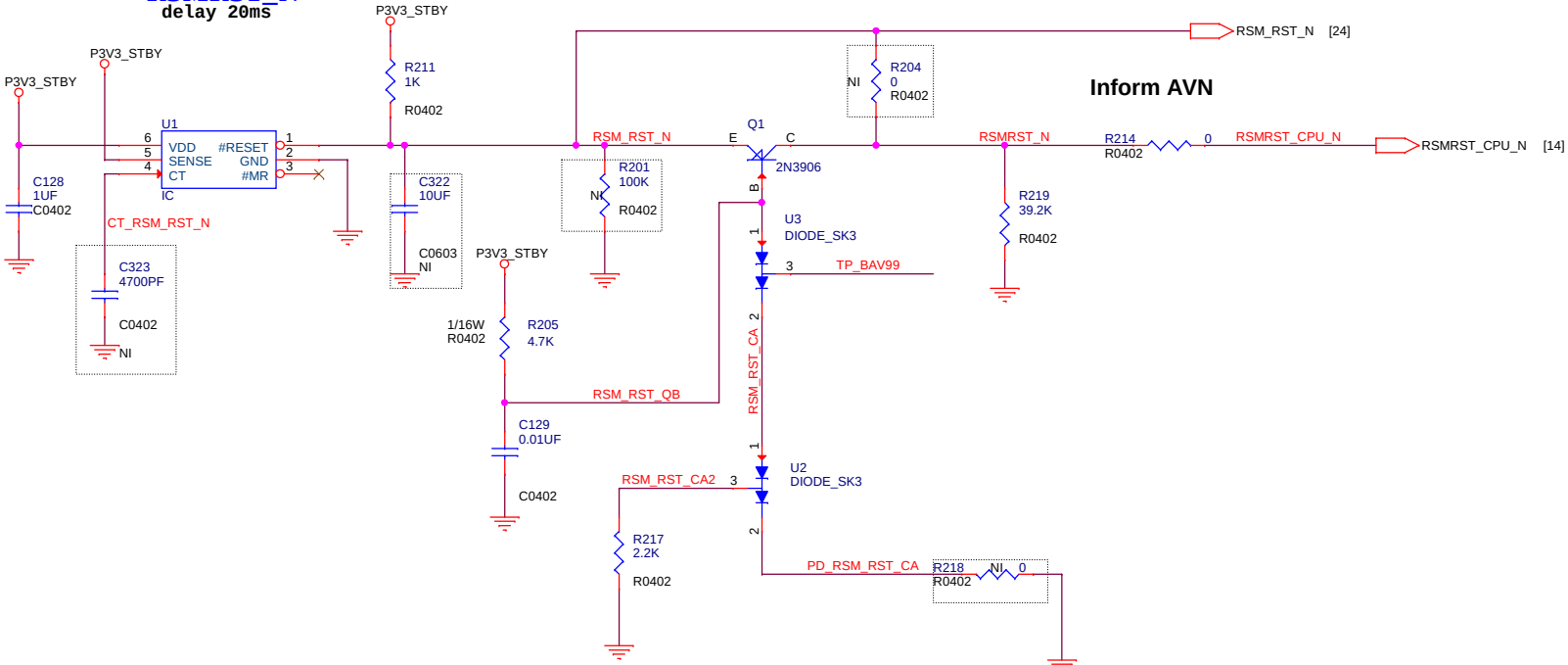
Output Voltage = 1.5V+/-5%
Output Ripple & Noise < 30mV
Transient Tolerance = 150mV
Max current = 0.1A
PD = (3.3V - 1.5V) * 0.1A =0.18W



Vnom=0.8(1+Ra/Rb)=1.508V

NOTE:RT9059_15GQW FIX OUTPUT VOLTAGE AT 1.5V

RSMRST_N
delay 20ms

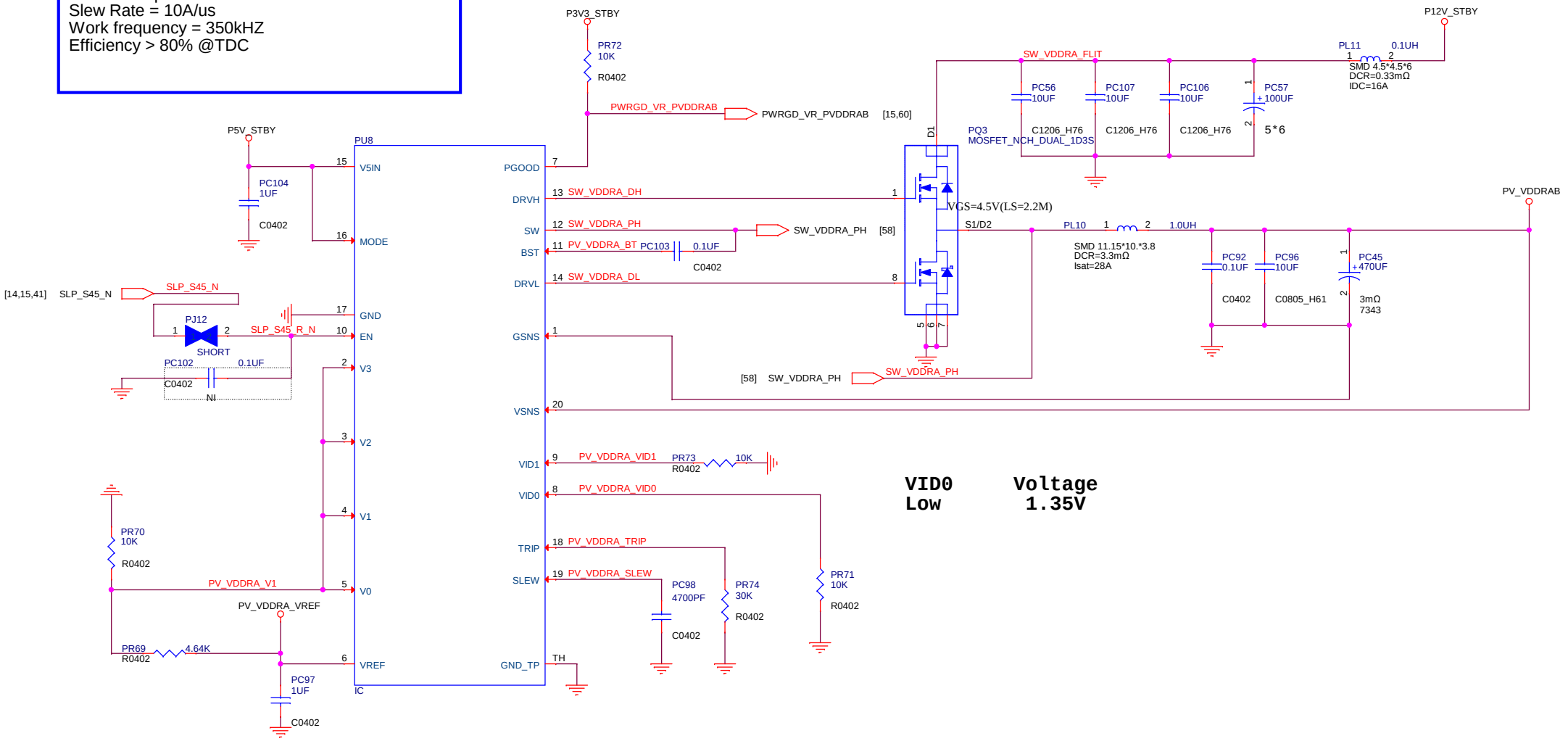


P1V5_STBY & RSMRST

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title P1V5_STBY&RSMRST	
			Size B Date: Thursday, January 22, 2015	Sheet 57 of 66	

Design specification

Output Voltage = 1.35V±4% (DC=±1.5%)
Output Ripple & Noise = <15mV or 13mV
Transient Tolerance = +/-4%
TDC =19.3 A
Max current = 22.3A
Over-Current Protection = 25.6A
Current Step = 9.6A
Slew Rate = 10A/us
Work frequency = 350kHZ
Efficiency > 80% @TDC

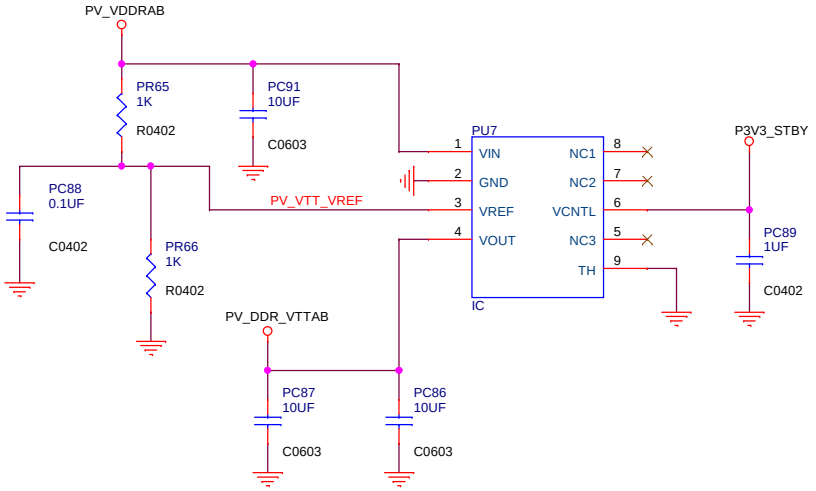


VID0	Voltage
Low	1.35V

VDDRAB

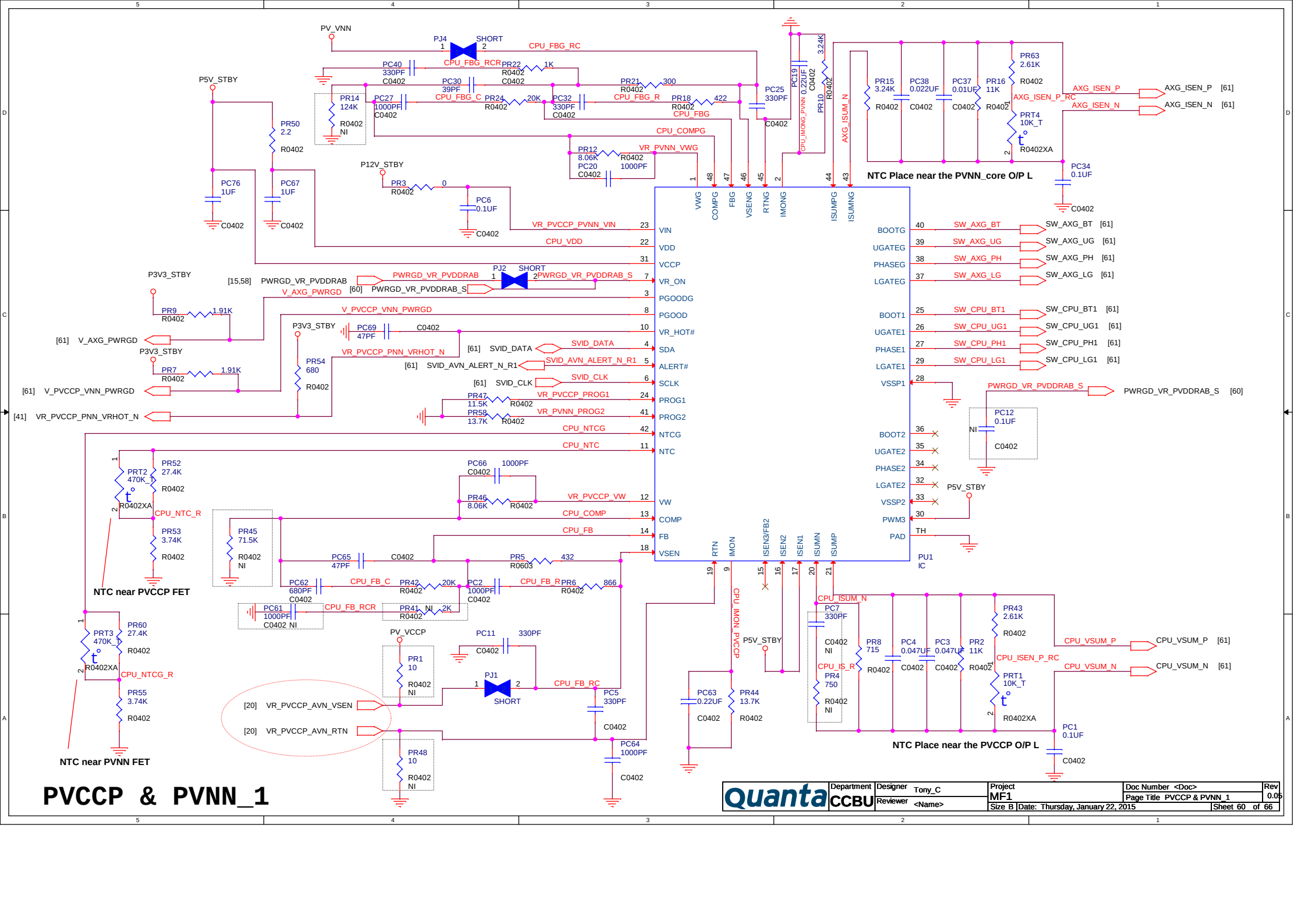
Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title VDDRAB	
			Size B Date: Thursday, January 22, 2015		Sheet 58 of 66

Output Voltage = 0.75V+/-5%
Output Ripple & Noise < 30mV
Transient Tolerance = 75mV
Max current = 0.1A
PD = (1.5V - 0.75V) * 0.1A = 0.075W



VTTAB

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title VTTAB	
			Size B Date: Thursday, January 22, 2015		Sheet 59 of 66


PV_VNN
PJ4
SHORT
CPU_FBG_RC
CPU_FBG_RCR
PC40 330PF C0402
PR22 1K R0402 C0402
P5V_STBY
PR21 300 R0402
PR14 124K R0402 NI
PC27 1000PF C0402
CPU_FBG_C
PR24 20K R0402
PC32 330PF C0402
CPU_FBG_R
PR18 422 R0402
CPU_FBG
PC25 330PF C0402
PC19 0.22UF C0402
CPU_IMONG_PVNN
3.24K R0402
AXG_ISUM_N
PR15 3.24K R0402
PC38 0.022UF C0402
PC37 0.01UF C0402
PR16 11K R0402
PR63 2.61K R0402
PRT4 10K_T R0402XA
AXG_ISEN_P
AXG_ISEN_P_RC
AXG_ISEN_N
AXG_ISEN_P [61]
AXG_ISEN_N [61]
PR50 2.2 R0402
PC76 1UF C0402
PC67 1UF C0402
CPU_COMPG
PR12 8.06K R0402
VR_PVNN_VWG
PC20 C0402 1000PF
P12V_STBY
PR3 R0402 0
PC6 0.1UF C0402
NTC Place near the PVNN_core O/P L
PC34 0.1UF C0402
VWG
COMPG
FBG
VSENG
RTNG
IMONG
ISUMPG
ISUMNG
VR_PVCCP_PVNN_VIN
CPU_VDD
P3V3_STBY
[15,58] PWRGD_VR_PVDDRAB
PJ2 SHORT
PWRGD_VR_PVDDRAB_S
[60] PWRGD_VR_PVDDRAB_S
V_AXG_PWRGD
PR9 1.91K R0402
[61] V_AXG_PWRGD
V_PVCCP_VNN_PWRGD
PC69 47PF C0402
VR_PVCCP_PNN_VRHOT_N
PR7 1.91K R0402
[61] V_PVCCP_VNN_PWRGD
PR54 680 R0402
[41] VR_PVCCP_PNN_VRHOT_N
[61] SVID_DATA
SVID_AVN_ALERT_N_R1
SVID_CLK
PR47 11.5K R0402
PR58 13.7K R0402
VR_PVCCP_PROG1
VR_PVNN_PROG2
CPU_NTCG
CPU_NTC
VIN
VDD
VCCP
VR_ON
PGOODG
PGOOD
VR_HOT#
SDA
ALERT#
SCLK
PROG1
PROG2
NTCG
NTC
VW
COMP
FB
VSEN
RTN
IMON
ISEN3/FB2
ISEN2
ISEN1
ISUMN
ISUMP
PU1
IC
BOOTG
UGATEG
PHASEG
LGATEG
BOOT1
UGATE1
PHASE1
LGATE1
VSSP1
BOOT2
UGATE2
PHASE2
LGATE2
VSSP2
PWM3
PAD
SW_AXG_BT
SW_AXG_UG
SW_AXG_PH
SW_AXG_LG
SW_CPU_BT1
SW_CPU_UG1
SW_CPU_PH1
SW_CPU_LG1
PWRGD_VR_PVDDRAB_S [60]
PC12 0.1UF NI C0402
P5V_STBY
PRT2 470K_T R0402XA
PR52 27.4K R0402
CPU_NTC_R
PR53 3.74K R0402
PR45 71.5K R0402 NI
NTC near PVCCP FET
PC66 1000PF C0402
PR46 8.06K R0402
VR_PVCCP_VW
CPU_COMP
CPU_FB
PC65 47PF C0402
PR5 432 R0603
PC62 680PF C0402
CPU_FB_C
PR42 20K R0402
PC2 1000PF C0402
CPU_FB_R
PR6 866 R0402
PC61 1000PF C0402 NI
CPU_FB_RCR
PR41 NI 2K R0402
PRT3 470K_T R0402XA
PR60 27.4K R0402
CPU_NTCG_R
PR55 3.74K R0402
NTC near PVNN FET
PV_VCCP
PR1 10 R0402 NI
PC11 330PF C0402
PJ1 SHORT
CPU_FB_RC
[20] VR_PVCCP_AVN_VSEN
[20] VR_PVCCP_AVN_RTN
PR48 10 R0402 NI
PC5 330PF C0402
PC64 1000PF C0402
CPU_IMON_PVCCP
PC63 0.22UF C0402
PR44 13.7K R0402
CPU_ISUM_N
PC7 330PF C0402 NI
CPU_IS_R
PR4 750 R0402 NI
PR8 715 R0402
PC4 0.047UF C0402
PC3 0.047UF C0402
PR2 11K R0402
PR43 2.61K R0402
PRT1 10K_T R0402XA
CPU_ISEN_P_RC
CPU_VSUM_P
CPU_VSUM_N
CPU_VSUM_P [61]
CPU_VSUM_N [61]
NTC Place near the PVCCP O/P L
PC1 0.1UF C0402
PVCCP & PVNN_1
Quanta
Department CCBU
Designer Tony_C
Reviewer <Name>
Project MF1
Doc Number <Doc>
Page Title PVCCP & PVNN_1
Rev 0.05
Size B
Date: Thursday, January 22, 2015
Sheet 60 of 66

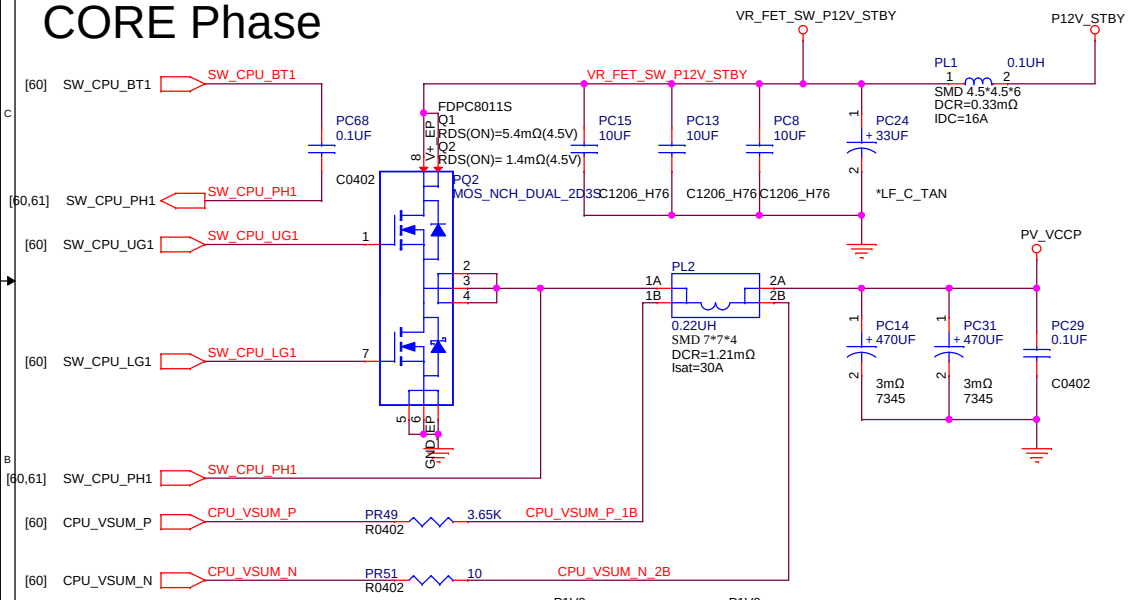
Vcore Design specification

VR12 Avoton Platform
Output Voltage = SVID[7:0] = 0.65~1.3V (VR12)
Output Ripple & Noise < +- 4.5mV
Total TOB = +-54mV
TDC = 11A
Max current = 23.2A
Over-Current Protection(Max Current*120%) = 28A
Current Step = 13A
Slew Rate = 100A/ns
Work frequency = 300kHZ
Load-Line = 0mΩ
Efficiency > 85% @TDC

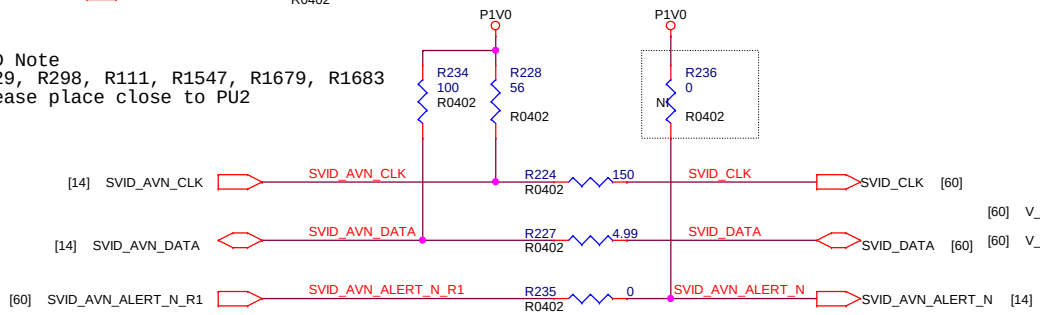
AXG Design specification

VR12 Edisonville Platform
Output Voltage = SVID[7:0] = 0.65~1.3V (VR12)
Output Ripple & Noise < +- 4.5mV
Total TOB = 19mV
TDC = 1A
Max current = 2.2A
Over-Current Protection(Max Current*200%) = 4.5A
Current Step = 1.3A
Slew Rate = 50A/ns
Work frequency = 300kHZ
Load-Line = 0mΩ
Efficiency > 85% @TDC

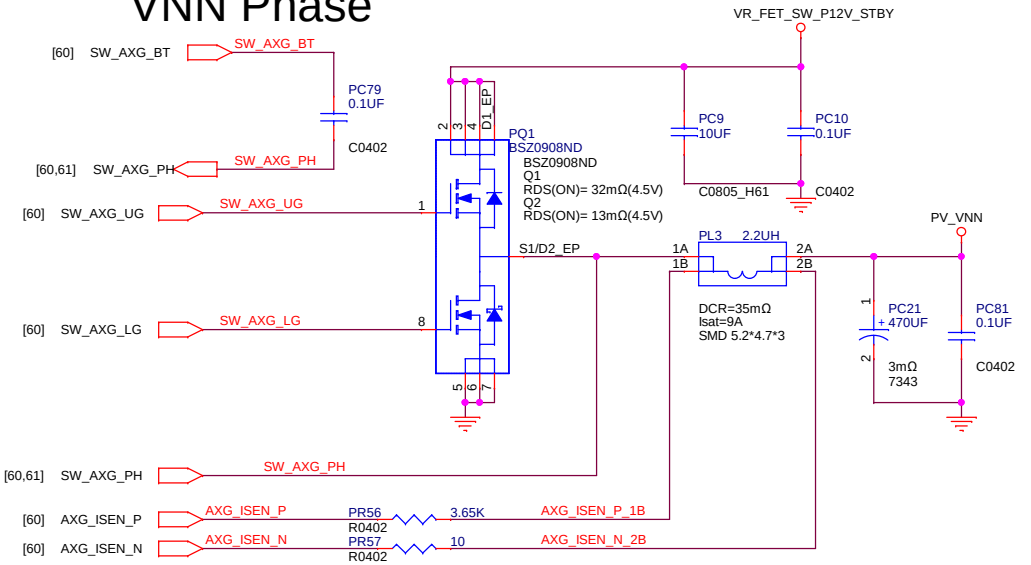
CORE Phase

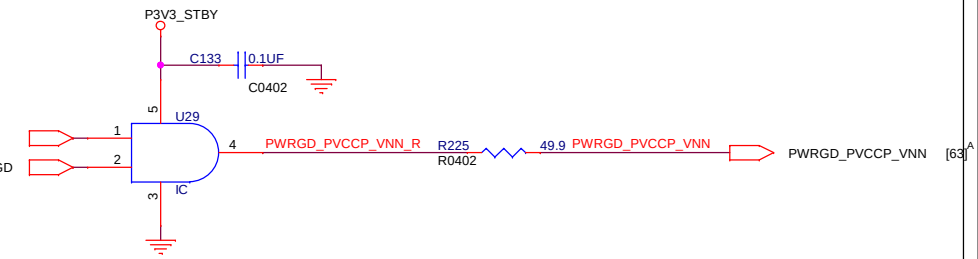


CAD Note
R929, R298, R111, R1547, R1679, R1683
Please place close to PU2



VNN Phase

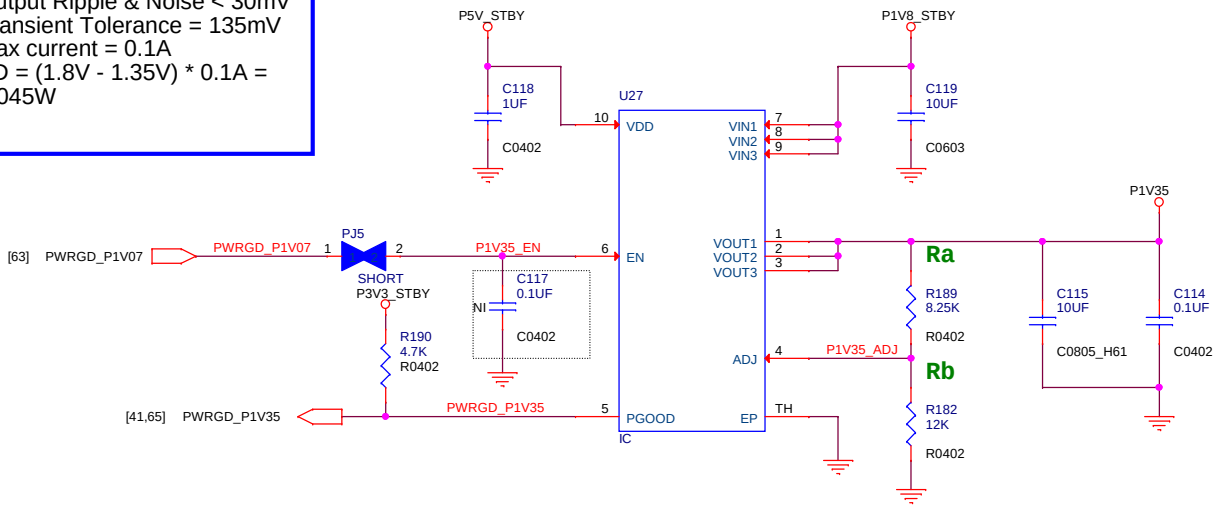




PVCCP & PVNN_2

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title PVCCP & PVNN_2	
			Size B Date: Thursday, January 22, 2015	Sheet 61 of 66	

Output Voltage = 1.35V+/-5%
Output Ripple & Noise < 30mV
Transient Tolerance = 135mV
Max current = 0.1A
PD = (1.8V - 1.35V) * 0.1A = 0.045W



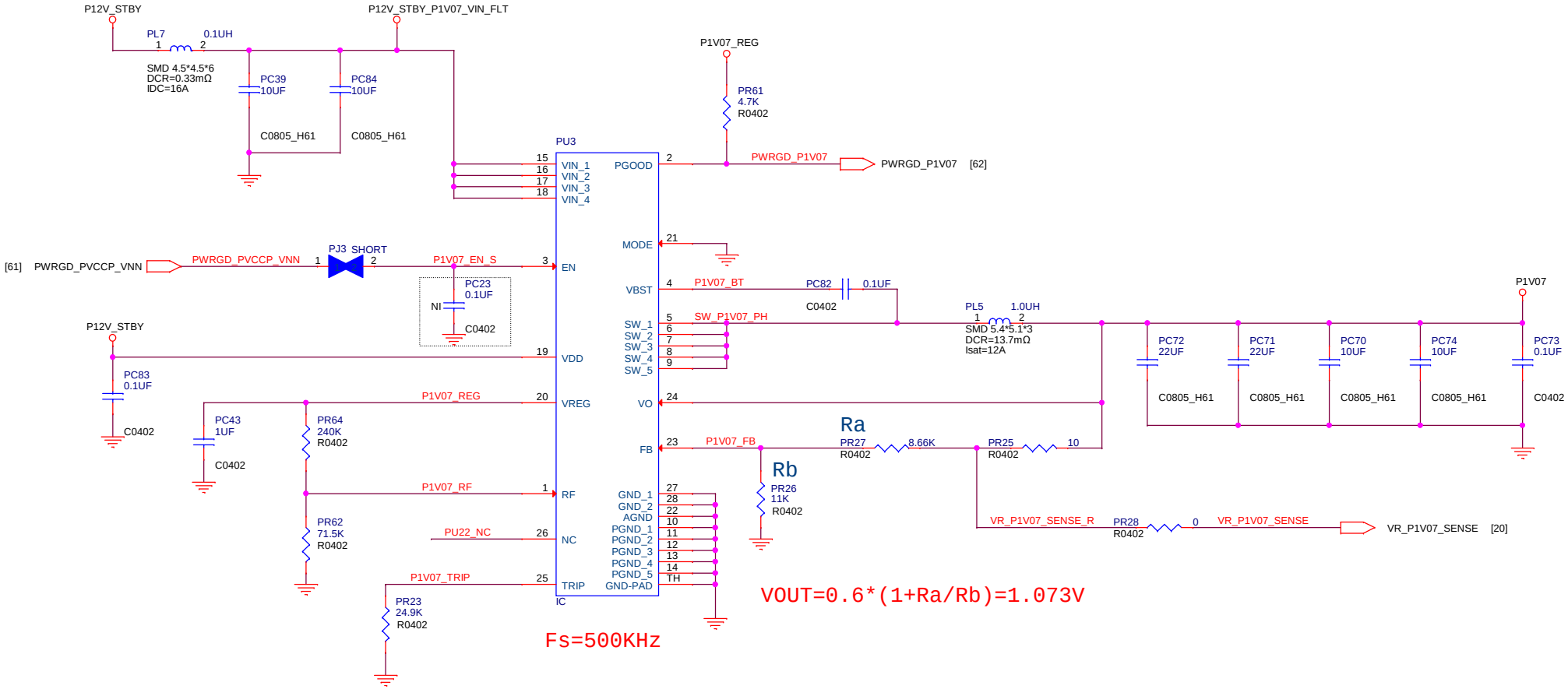
Vnom=0.8(1+Ra/Rb)=1.35V

P1V35

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title P1V35	
			Size B Date: Thursday, January 22, 2015		Sheet 62 of 66

Design specification

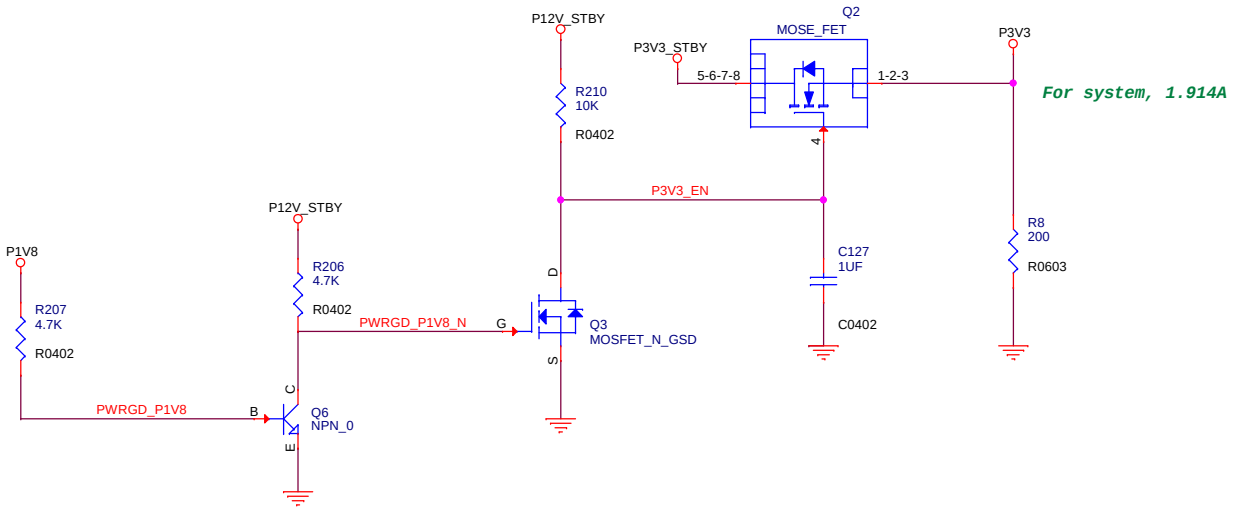
Output Voltage = 1.07V±5%
Output Ripple & Noise < 50mV
Transient Tolerance = 107mV
TDC = 2.5A
Max current = 2.8A
Over-Current Protection(Max Rating × 1.3) =3.7A
Current Step = 1.4A
Slew Rate = 2.5A/us
Work frequency = 500KHZ
Efficiency > 85% @TDC



P1V07

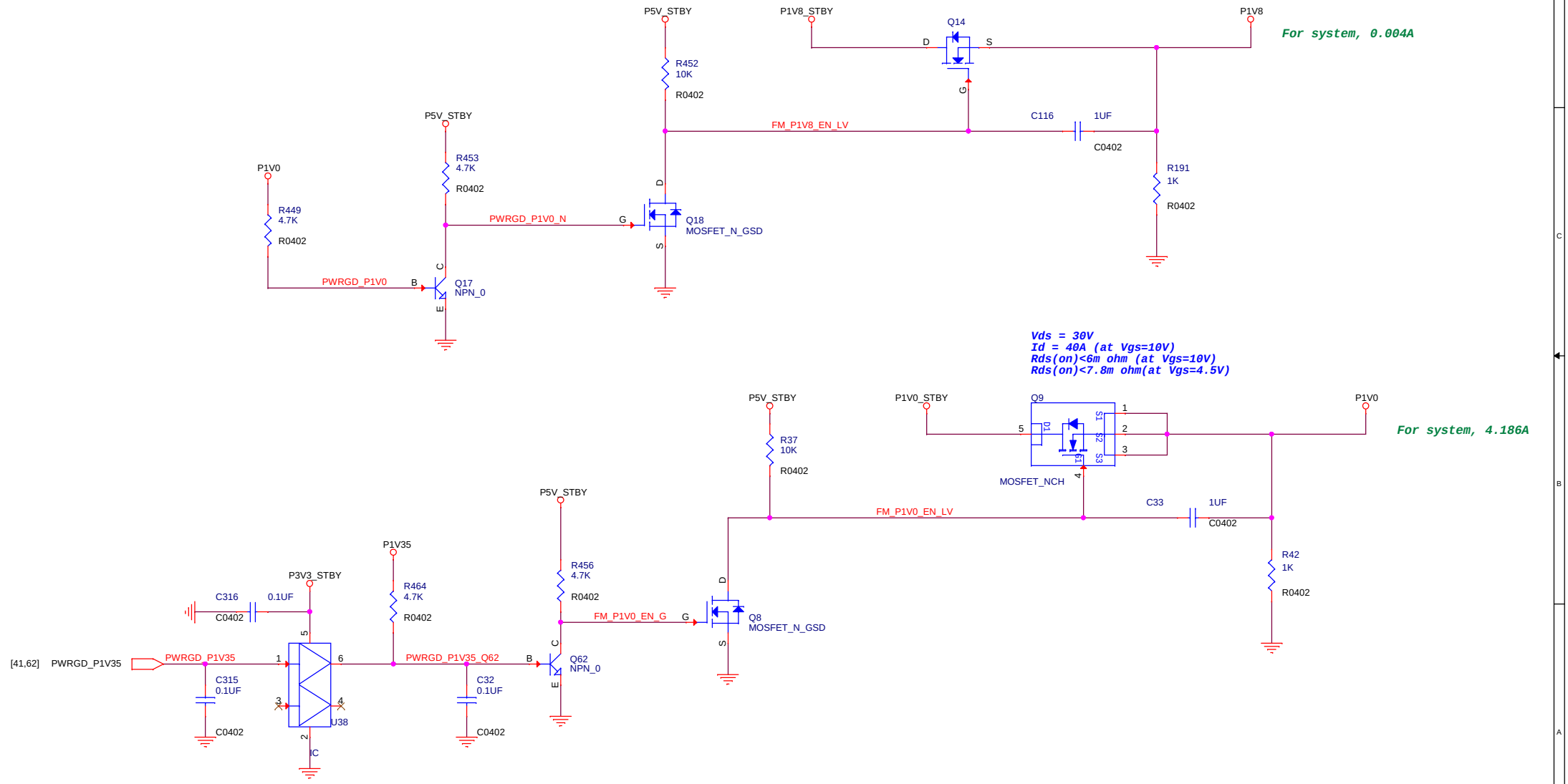
Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title P1V07	
			Size B Date: Thursday, January 22, 2015	Sheet 63 of 66	

Vds = 25V
Id = 40A (at Vgs=10V)
Rds(on)=8.1m ohm (at Vgs=4.5V)
Rds(on)=6.0 m ohm(at Vgs=10.0V)



P3V3

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title P3V3	
			Size B	Date: Thursday, January 22, 2015	Sheet 64 of 66



P1V0_P1V8

Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title P1V0_P1V8	
			Size B Date: Thursday, January 22, 2015		Sheet 65 of 66

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Quanta	Department CCBU	Designer Tony_C	Project MF1	Doc Number <Doc>	Rev 0.05
		Reviewer <Name>		Page Title BLANK	
			Size B	Date: Thursday, January 22, 2015	Sheet 66 of 66