ASE GROUP

ODSA

Enabling Heterogenous Integration

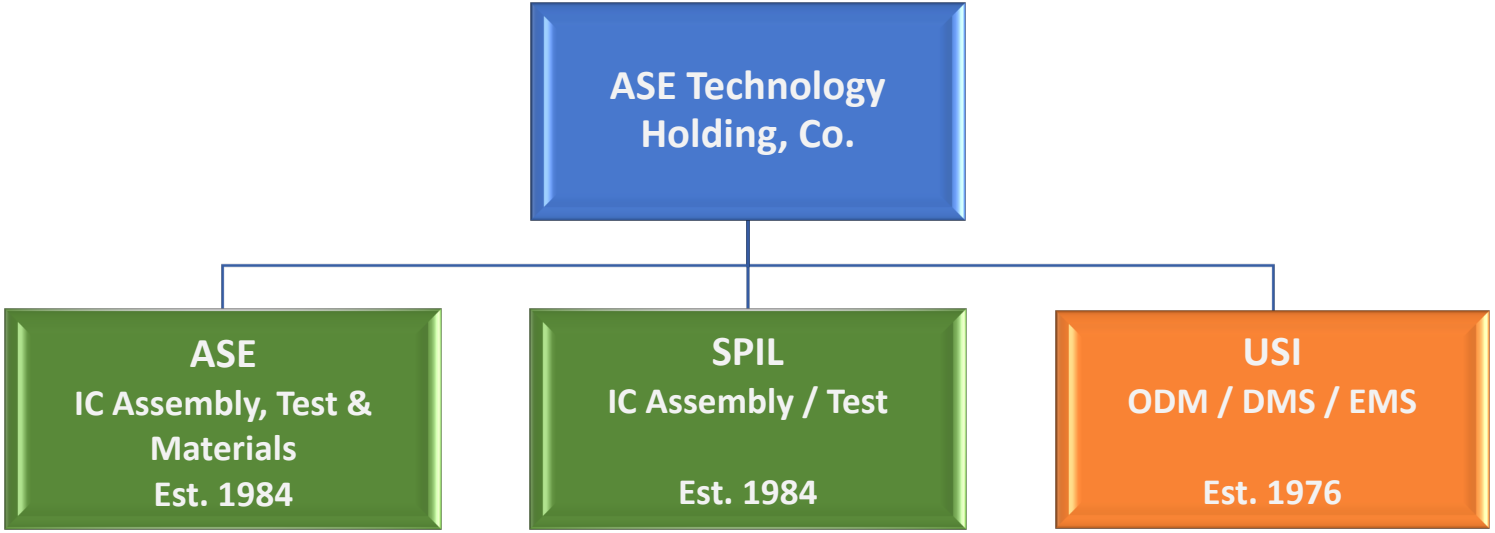
Eelco Bergman
OCP Global Forum 2020
ODSA Workgroup

March 4-5, 2020

ASE Introduction

© ASE Group. All rights reserved.

Organization



2019 Revenue: $8.13B

2019 Revenue: $5.37B

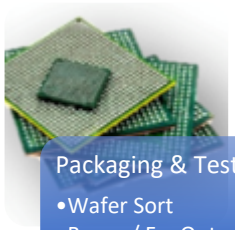
© ASE Group. All rights reserved.

Providing Complete Value Chain Solution

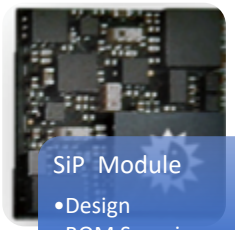
Integrating OSAT and EMS

Semiconductor Design
- Engineering test services

Wafer Fabrication
- IDM
- Wafer Foundry



Packaging & Test
- Wafer Sort
- Bump / FanOut
- Assembly
- Final Test



SiP Module
- Design
- BOM Sourcing
- Assembly
- Module Test
- FAE support

PCBA / System
- Design
- BOM Sourcing
- Assembly
- System Test
- Logistics

ASE Group Services

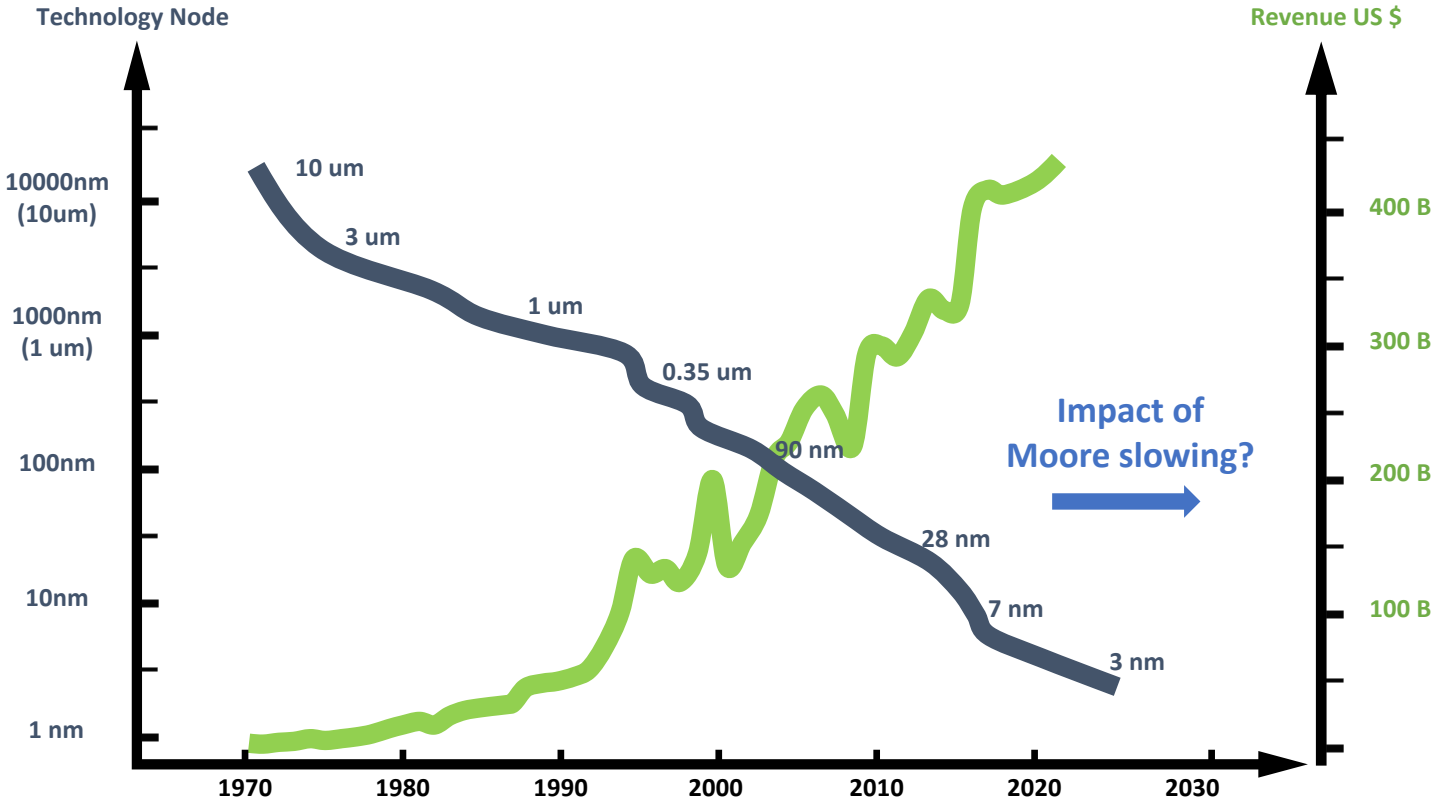
ASE GROUP ASE GROUP ASE GROUP USI USI

© ASE Group. All rights reserved.

Packaging Market Drivers

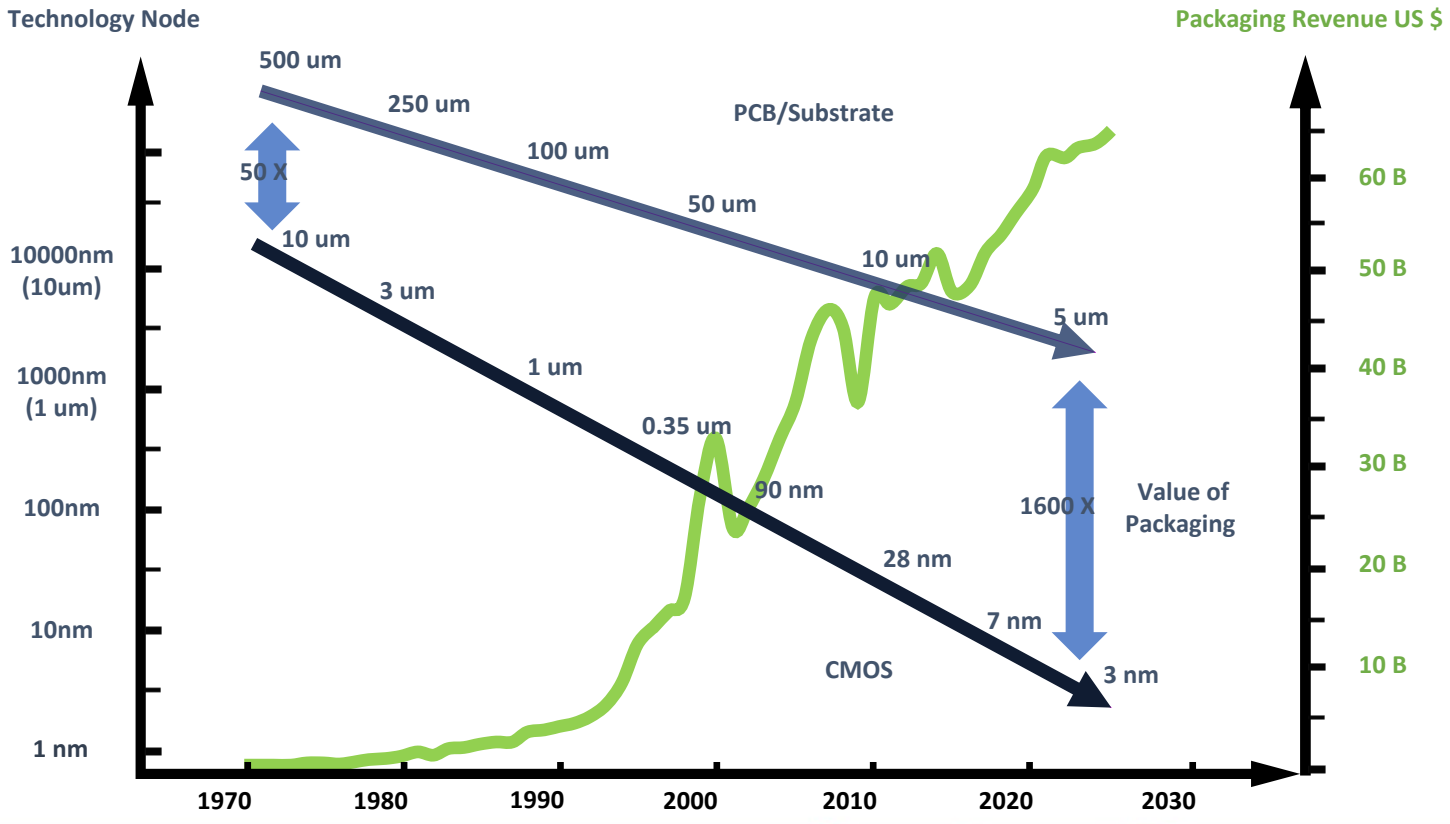
© ASE Group. All rights reserved.

Semiconductor Revenue vs. Process Generation



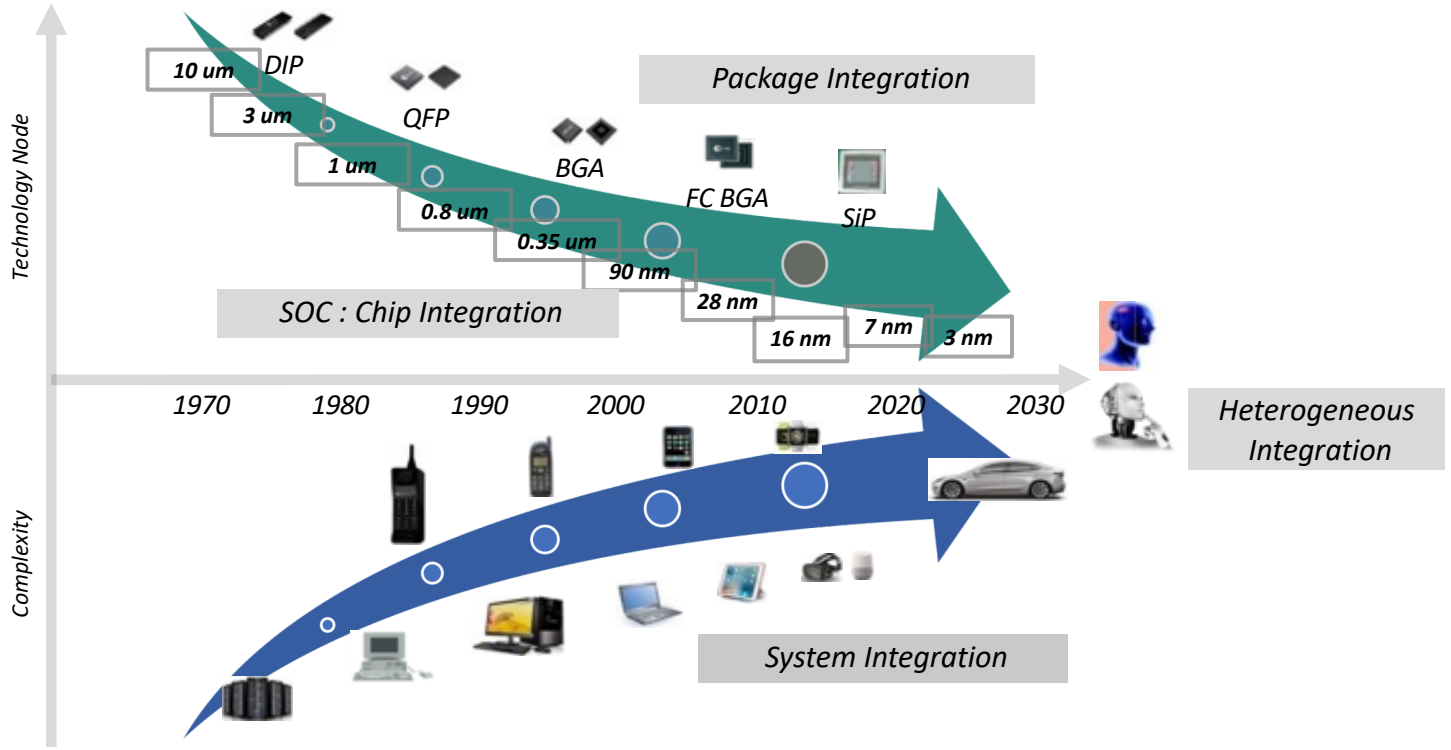
© ASE Group. All rights reserved.

Value of Semiconductor Packaging is Increasing



© ASE Group. All rights reserved.

Chip & System Integration Convergence



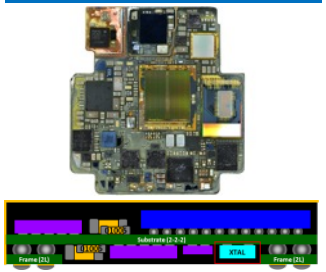
© ASE Group. All rights reserved.

Silicon Integration Packaging Solutions

© ASE Group. All rights reserved.

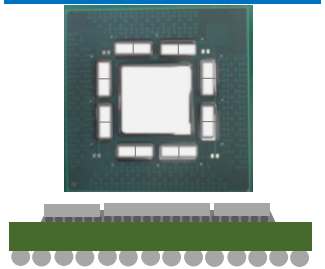
Silicon Integration Solutions

SiP



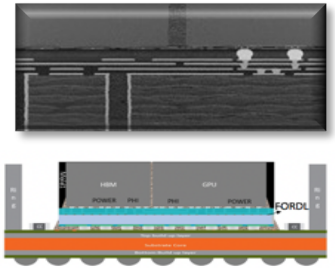
- PCB/Substrate interconnect
- Low/med density D2D
- > 25um line/space
- > 200um bump pitch
- > 50um comp spacing
- Bare/packaged parts
- Chip last process

Flip Chip MCM



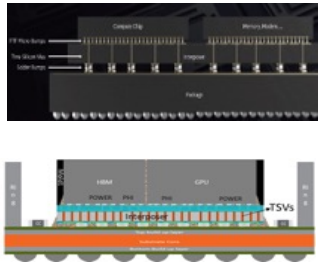
- Substrate interconnect
- Low/med density D2D
- > 10um line/space
- > 125um bump pitch
- > 50um D2D spacing
- Chip last process

FanOut/RDL



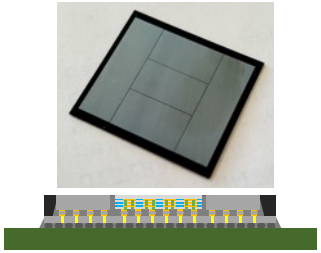
- RDL interconnect
- Med/high density D2D
- > 1um line/space
- > 40um bump pitch
- 100um D2D spacing
- Chip first/last
- FC to organic subs.
- No TSV – lower loss

2.5D TSV



- Si interconnect
- High density D2D
- < 0.5um line/space
- > 40um bump pitch
- > 50um D2D spacing
- Chip first/last
- High bandwidth
- Added Si layer
- Power limited

3D IC



Development

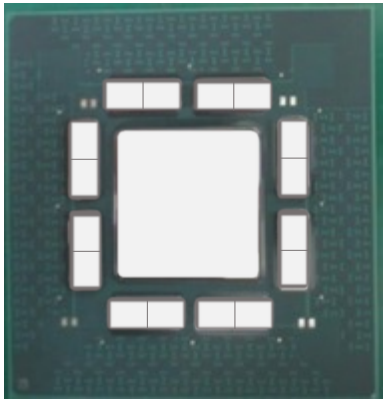
- Si interconnect
- High density D2D
- Foundry line/space
- < 10um bump pitch
- High bandwidth
- Shortest interconnect
- Direct or hybrid bond
- Custom die designs

Increasing Bandwidth & Cost

© ASE Group. All rights reserved.

Flip Chip / MCM

- Substrate based interconnect, > 10/10um line/space
- Multi-layer routing – 2/4 lyr core with build up layers
- Low to medium interconnect density (100's to 1,000)
- Package size: < 80x80mm (prod), < 120x120mm (dev)
- D2D spacing capability: 60um
- Benefits
  - Supports homo/heterogenous die partitioning
  - Enables IP reuse with advanced wafer node devices
  - Reduced SoC design and validation time
  - Enable multiple sources for 'standard' IP blocks / devices
  - Smaller SoC die size – increased yield
  - Lower bump/die stress – increased reliability

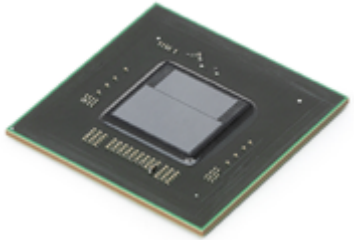


SoC + 16 chiplets
60um die to die spacing min

© ASE Group. All rights reserved.

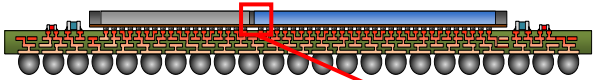
FanOut / FOCoS

- RDL based interconnect, 2/2um line/space
- Multi-layer routing (3-4 lyrs.)
- Medium to high interconnect density (1000's to 10,000)
- Large FO area (1200-1600mm2)
- Stacked vias (10um hole/15um land)
- Chip first or chip last process
- Benefits
  - Die size, yield and cost optimization
  - Process node / functionality optimization
  - Integration of digital/analog SoCs
  - Short, high density interconnect
  - No TSV - Lower cost alternative to 2.5D
  - Increased reliability vs. MCM



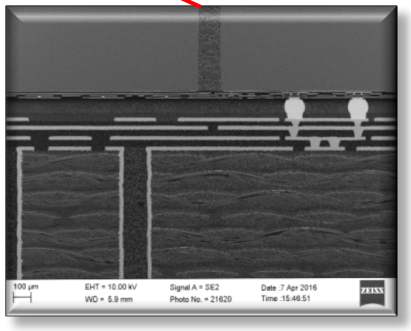
Fan Out Compound Die

Fan Out Hybrid BGA Package



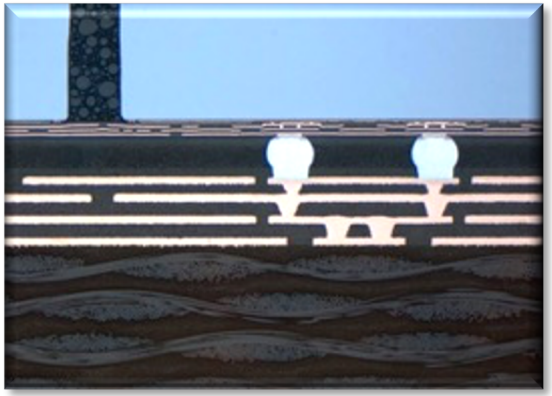
Stacked Via

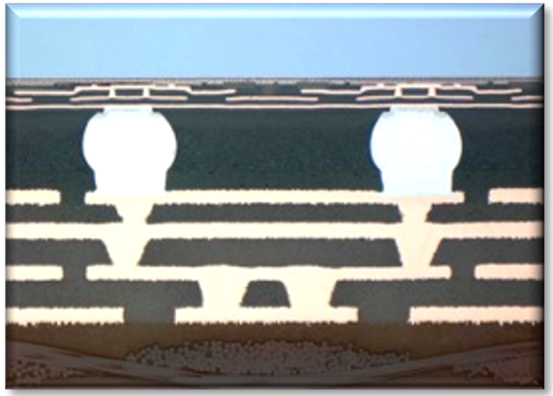
2/2 µm
Lines/Spaces

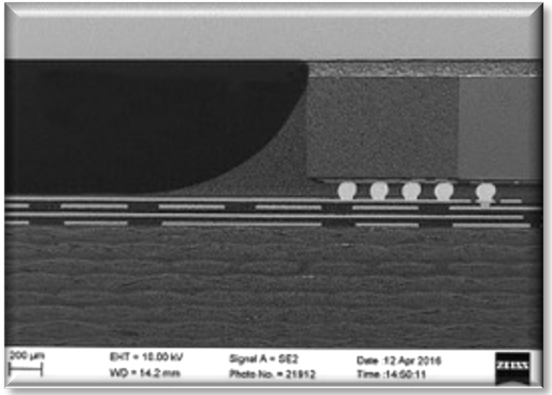


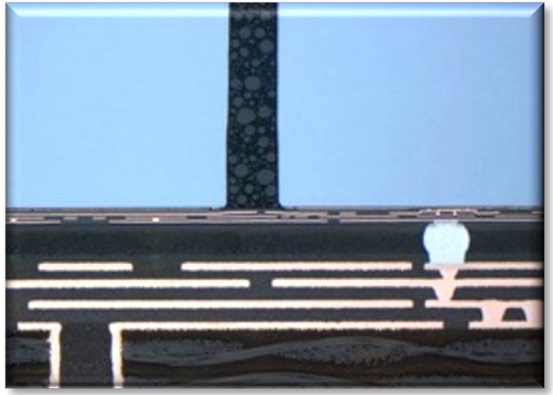
© ASE Group. All rights reserved.

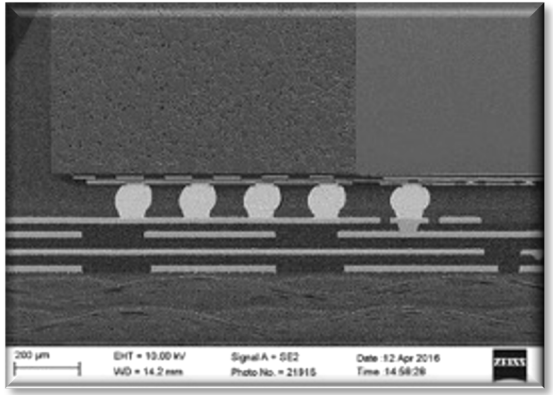
FOCoS Chip First Production Cross Sections





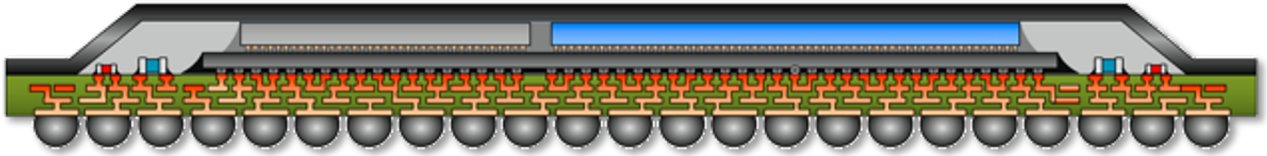




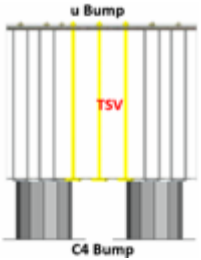


© ASE Group. All rights reserved.

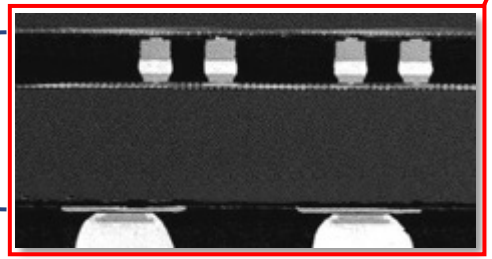
2.5D TSV Replacement Opportunity

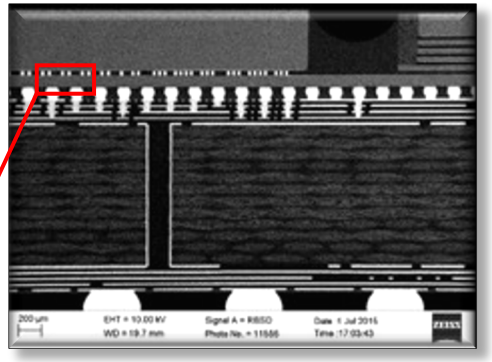


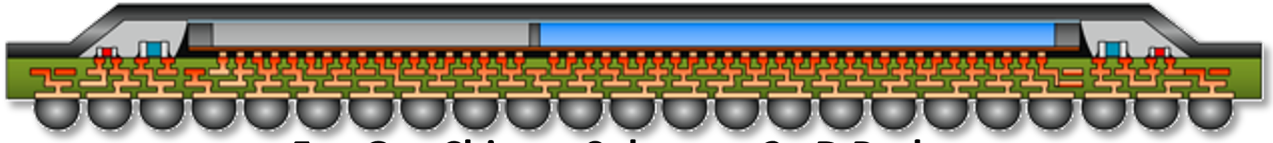
2.5D Interposer Package



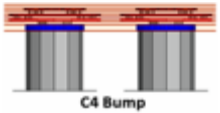
3D
Interposer
Interconnection



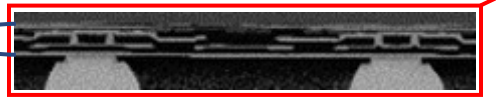


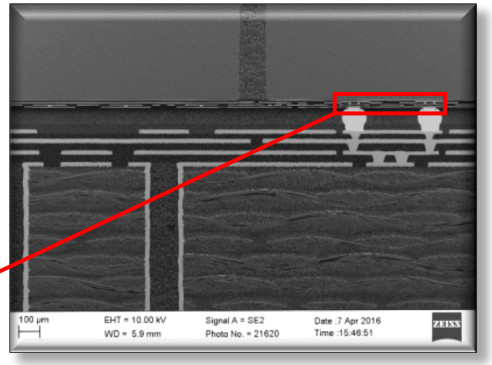


Fan Out Chip on Substrate 2.xD Package



3D
Fan Out
Interconnection

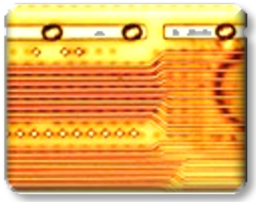
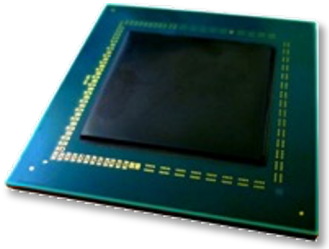
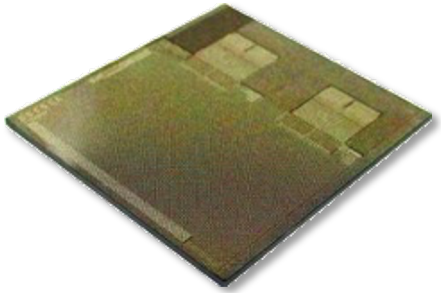
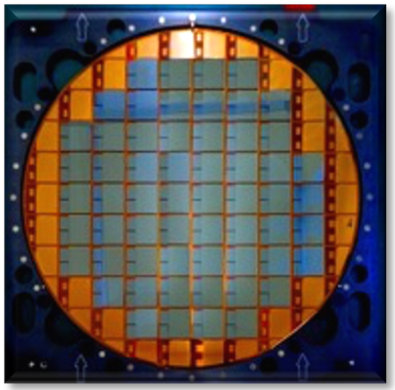




© ASE Group. All rights reserved.

FOCoS Chip Last With HBM

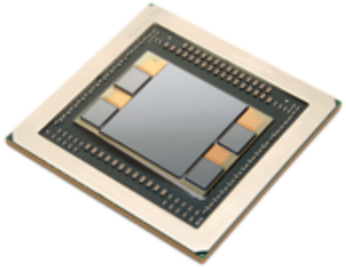
- Chip Last Construction
- 3,496 RDL traces to HBMs
- >15,500 C4 Bumps on Fan Out Composite Die
- 6 Metal Layers
  - 4 RDL layers
  - 2 layers with 2µm/2µm L/S
  - 1 UBM Layer
  - 1 C4 Layer

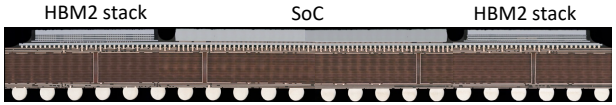





© ASE Group. All rights reserved.

2.5D TSV

- Silicon based interconnect, < 0.5/0.5um line/space
- High interconnect density (10,000's to 100,000)
- > 40um microbump pitch
- Supports:
  - Die partitioning
  - Memory integration
  - Optics integration (optical bench)
- Benefits
  - Silicon interconnect performance
  - High bandwidth interface enablement
  - Reduced power
  - Si on Si first level interconnect
  - System board size reduction

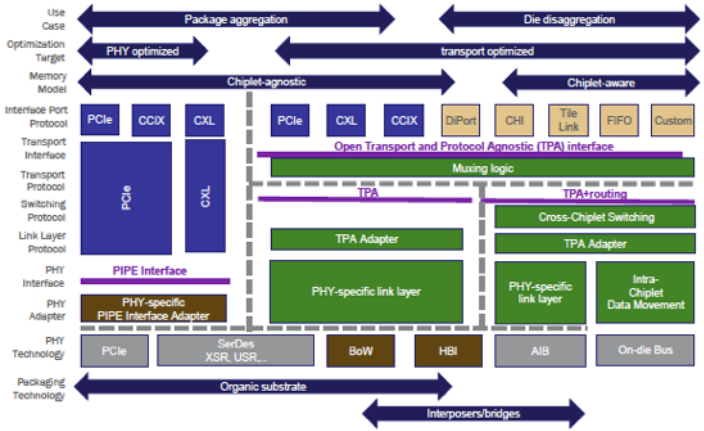




© ASE Group. All rights reserved.

ASE - ODSA Engagement Objectives

- Respond to increased need for heterogeneous die integration
  - Disaggregation of complex die
  - Shrink system board into package
- Drive cost reduction & scaling
  - Reduce design & development time
  - Decrease customization
  - Engage supply chain
- Enable mass adoption
  - Develop package level interface design guidelines
  - Establish interface design libraries
  - Enable design & simulation tool integration

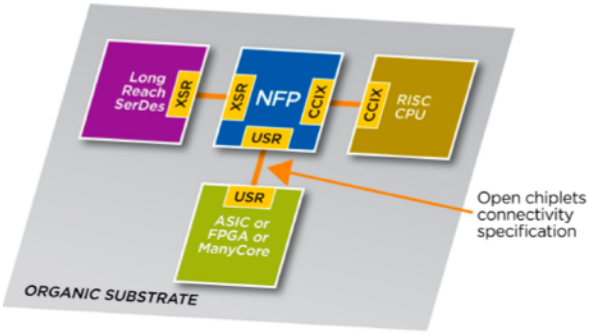


Open interface for chiplet communication

© ASE Group. All rights reserved.

Next Steps / Call to Action

- Establish working group under/as part of ODSA CDX to focus on package interface design rules & layout
- Members to include:
  - ODSA BoW & OpenHBI interface architecture developers
  - Other / 3rd party interface architecture developers (AIB, XSR/USR, etc.)
  - EDA tool & library suppliers
  - Package substrate design/simulation service providers (OSAT and/or independent)
- Assess feasibility of establishing physical interface layout / pin out standards (eg. DDRx, HBM, AIB)
- Identify critical interface layout requirements and develop 'PRD' specification per interface
- Establish design guidelines and develop interface design libraries
  - Organic substrate interconnect (> 10um line/space)
  - Redistribution layer interconnect (> 1um line/space)
  - Silicon substrate (2.5D) interconnect (< 0.5um line/space)
- Demonstrate virtual chiplet integration design flow



© ASE Group. All rights reserved.

Thank You

www.aseglobal.com

© ASE Group. All rights reserved.