ES200 2U Edge Server

Revision 0.2

Authors:

Daniel Huang, HW Engineer, Wiwynn Corporation

Robert Yang, ME Engineer, Wiwynn Corporation

Tommy Yeh, Thermal Engineer, Wiwynn Corporation

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Revision history

Revision	Editor	Description
V0.1 (July 31, 2020)	Daniel Huang	First draft release version
V0.2 (October 30, 2020)	Jackie Lee	Increase Appendix section

Contents

2   Introduction

ES200 is an Edge server with 2U short-depth (450mm) chassis design, compatible in EIA-19" rack mount, for CSP/Telco to deploy their Edge applications. The Wiwynn ES200 targets to build a common design for the 2U family which brings storage and I/O bays flexibility to switch by configurations.

3   Production Architecture Overview

ES200 Edge Server main characteristics and features are listed below:

Table 1: Server Feature List

Board Name	Edge Server Mother Board
Form Factor	Width: 438mm (17.2") x Depth: 450mm (17.7"), Height: 2U tall
Mother Board dimension	W 309.8mm x D 363.6mm, 12 layers, 2.36mm, 16 DIMMs
CPU	2S 3rd Gen Intel Xeon scalable processor
Chipset	Intel PCH C621A
Memory	**DIMM Sockets**: total 16 sockets, CH A/B/C/D/E/F/G/H 1DPC; (CH B; J2/J10 Support Intel DCPMM) **DIMM Types:** DDR4 RDIMM, 1.2V **DIMM Capacities:** 16GB, 32GB
PCIe Expansion Slot	**Type:** CPU1 native PCIe Gen4 **Port PE0 ABCD:** x16 PCIe link to sliver riser connector **Port PE1 AB:** x8 PCIe link to sliver riser connector **Port PE2 ABCD:** x16 PCIe link to OCP 3.0 connector **Port PE3 AB:** x8 PCIe link to sliver riser connector **DMI:** PCIe link x4 to PCH **Type:** CPU2 native PCIe Gen4 **Port PE0 ABCD:** x16 PCIe link to OCP 3.0 connector **Port PE1 CD:** x8 PCIe link to sliver connector **Port PE2 AB:** x8 PCIe link to sliver connector **Port PE2 CD:** x8 PCIe link to sliver connector **Port PE3 AB:** x8 PCIe link to sliver riser connector **Type:** PCH PCIe link x1 to BMC PCIe link x4 to M.2 connector

Front Side IO	One USB 3.0 port
	One USB 2.0 port on front IO board
	One VGA port (D-sub)
	One RJ45
	Power button with LED include identification function
	Reset button
	UID button with LED
Network	LOM: No
Video	ASPEED AST2500 16MB DDR4 video memory
Fan	**2U Fans:** Four pluggable 8038 fans
ACPI	ACPI compliance, S0, S5 support. (* No S1 and S3 supports)
Power-Supply	1600 Watts AC to DC power supply
TPM	TPM 2.0
2U PCIe Expansion	**Option#1**
	(1) Two OCP 3.0 slots PCIe x16
	(2) Two Riser card connectivity
	(1) Two PCIe x16 normal card-edge connectors for two x16 electrical
	(2) One PCIe x8 normal card-edge connectors
	(3) Six U.2/PCIe connectors
	(4) One M.2 connector
	Option#2
	(1) Two OCP 3.0 slots PCIe x16
	(2) Two Riser card connectivity
	(1) Two PCIe x16 normal card-edge connectors for one x16, one x8 electrical
	(2) One PCIe x8 normal card-edge connectors
	(3) Eight EDSFF E1.S connectors
	(4) One M.2 connector
Environmental	Operating temperature: -5°C to 55°C
	Non-operating temperature -40°C to 70°C
	Operating relative humidity 10% to 90% RH
	Non-operating relative humidity 5% to 95%RH

3.1   Server Board Block Diagram
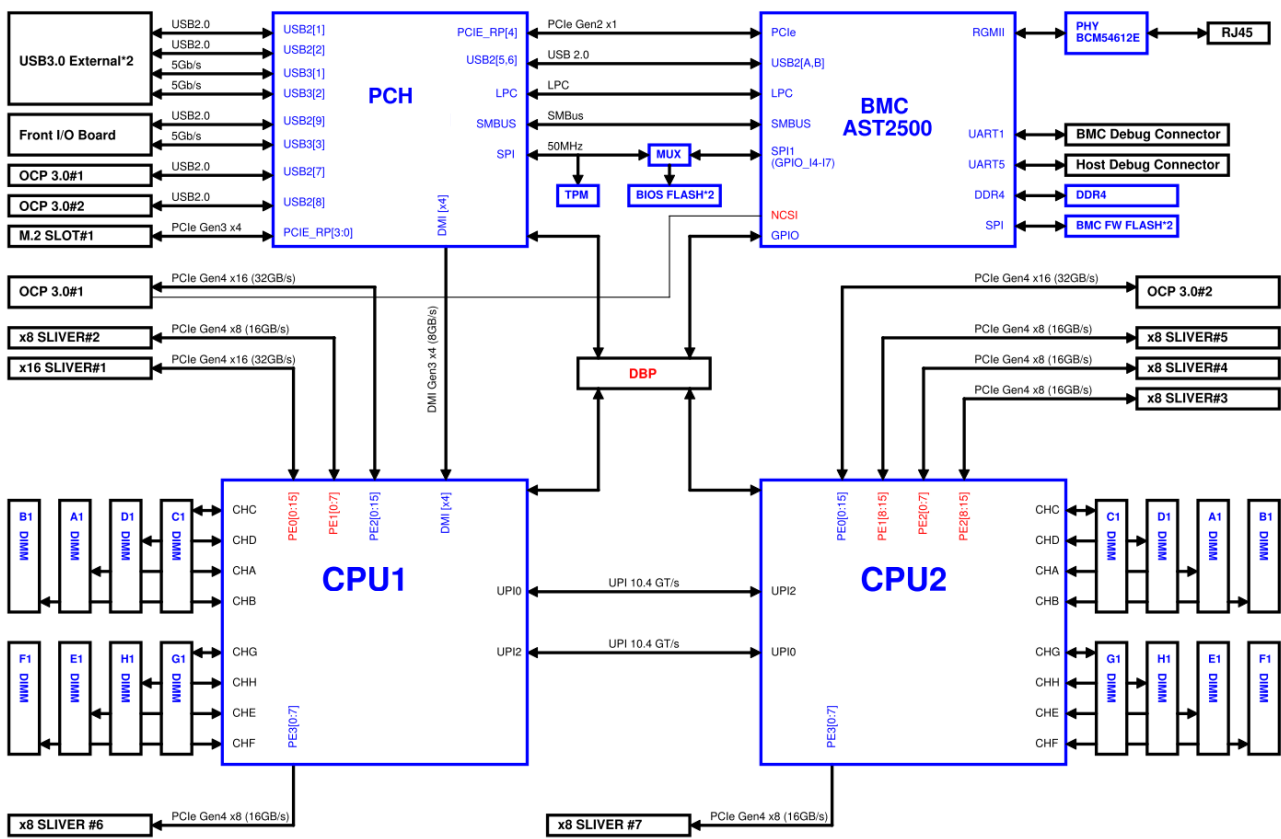

Figure 1: Server Board Block Diagram

3.2   Server Board

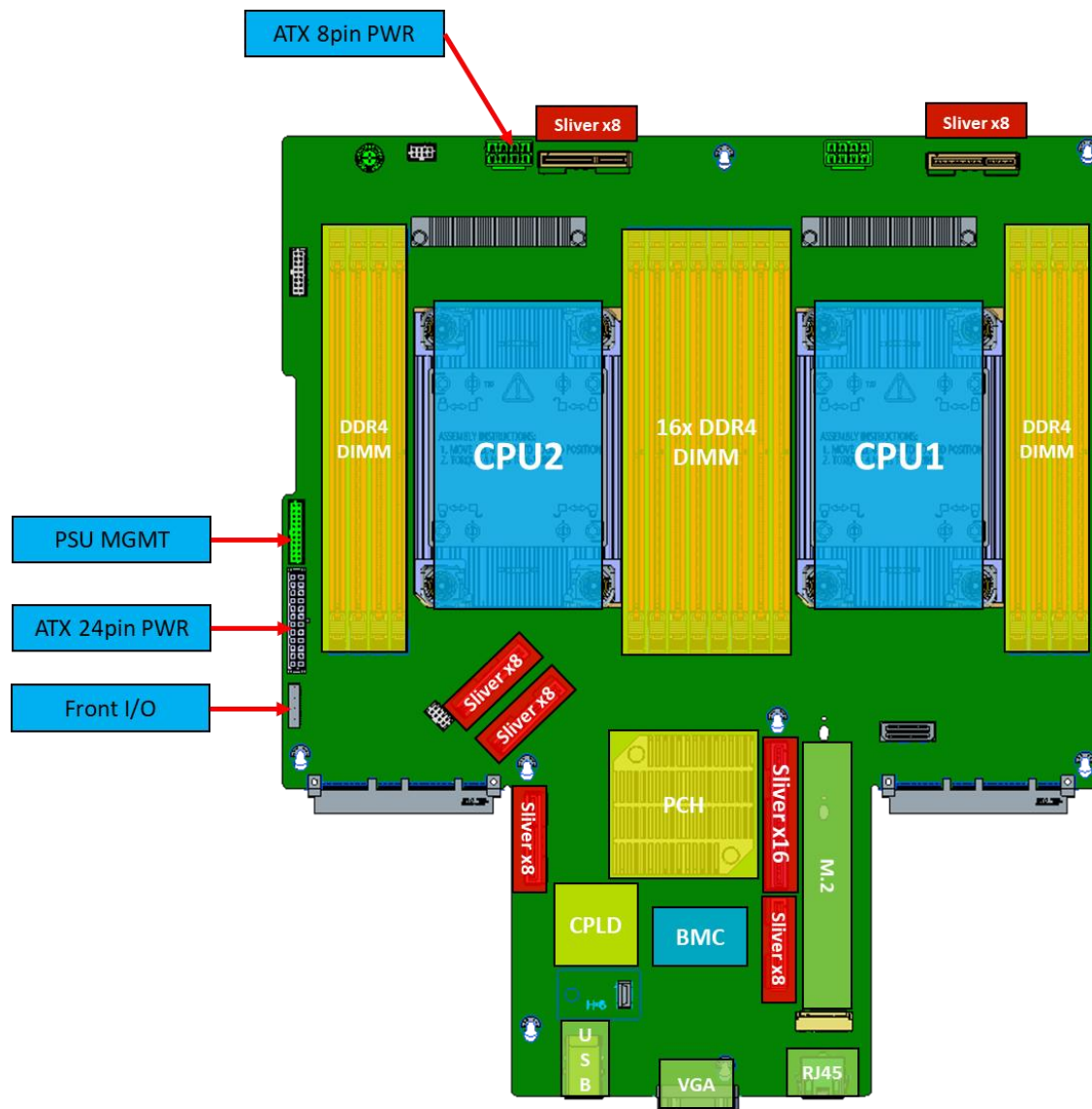### 3.2.1   Server Board Placement

Figure 2: Server Board Placement

3.2.2 Server Board Dimensions

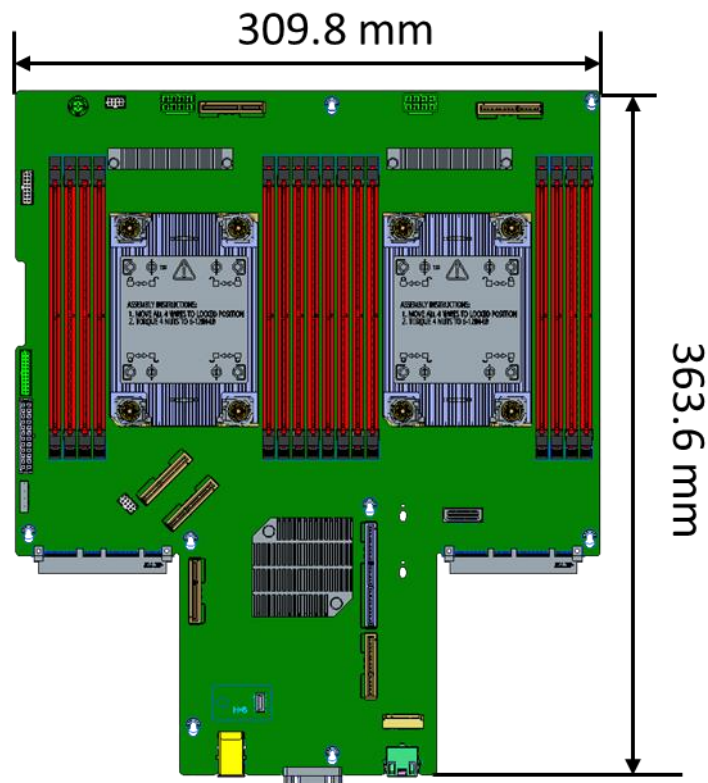Server Board dimensions are 309.8mm (W) x 363.6mm (L).

Figure 3: Server Board Dimensions

3.2.3 Processor

ES200 leverage 3rd Gen Intel Xeon scalable processor which is the next generation of 64-bit, multi-core server processor.

3.2.4 PCH

ES200 leverage the PCH which is the same one used in the Intel Skylake or Cascade Lake processors with a refresh version.

3.2.5   Memory

ES200 server board design supports eight DIMM slots per processor. Part of the DIMM slots also supports Intel DCPMM. Here is the population table for a processor.

	Slot 0	Slot 1	Slot 2	Slot 3	Slot 4	Slot 5	Slot 6	Slot 7
Config1	DRAM	DRAM/DCPMM	DRAM	DRAM	DRAM	DRAM	DRAM	DRAM

The DIMM identifiers on the silkscreen is indexed from J1 to J16 in ES200 server board DCPMM can only be populated on J2 and J10 locations (please refer to the following picture).he J6 and J14, must be depopulated with any DIMM, when J2 and J10 are populated with DCPMM.
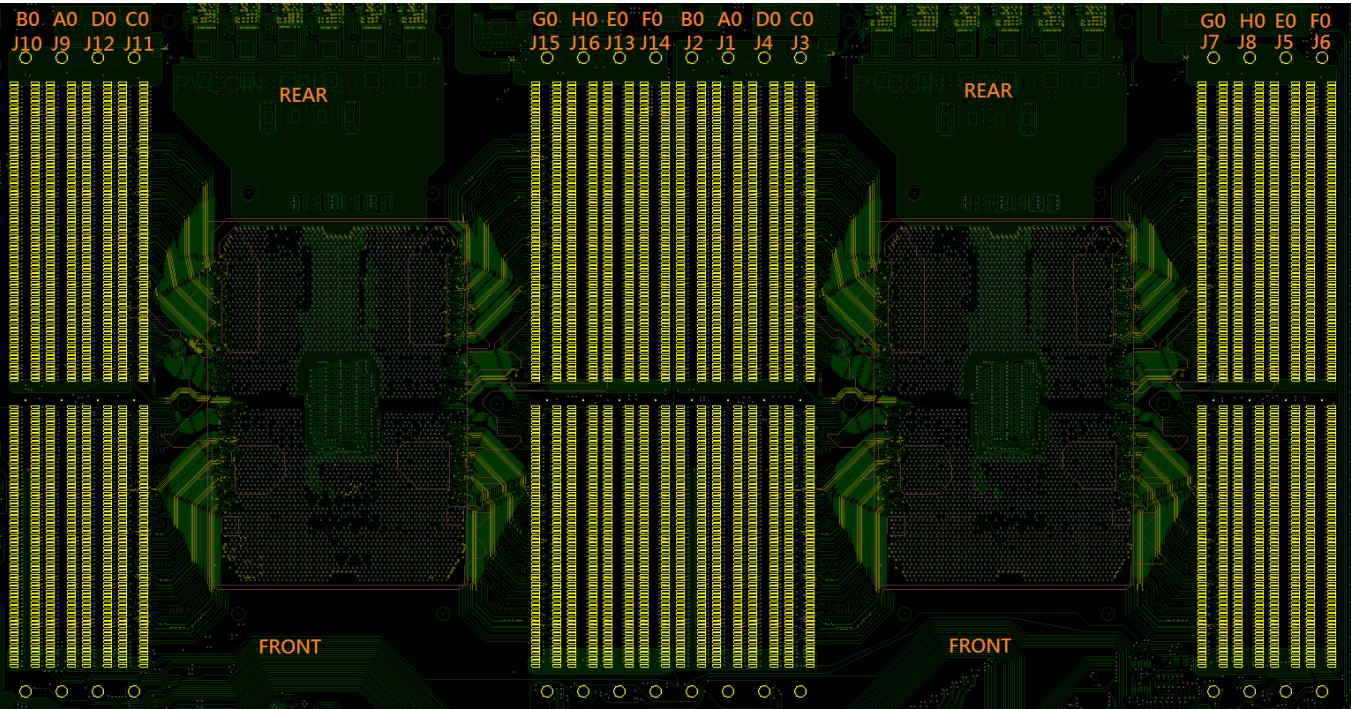

Figure 4: Server Board DDR Physical Slots

3.2.6   PCIE Lanes

CPU1 PCIE Port0

CPU1 PCIE P0 ABCD PCIE x 16 lanes are connecting to 140-pin riser slot

CPU1 PCIE Port1

CPU1 PCIE P1 AB PCIE x 8 lanes are connecting to 84-pin riser slot.

CPU1 PCIE Port2

CPU1 PCIE P2 ABCD PCIE x 16 lanes are connecting to OCP 3.0 connector.

CPU1 PCIE Port3

CPU1 PCIE P3 AB PCIE x 8 lanes are connecting to 84-pin sliver connector.

CPU2 PCIE Port0

CPU2 PCIE P0 ABCD PCIE x 16 lanes are connecting to OCP 3.0 connector.

CPU2 PCIE Port1

CPU2 PCIE P1 CD PCIE x 8 lanes are connecting to 84-pin sliver connector.

CPU2 PCIE Port2

CPU2 PCIE P2 AB PCIE x 8 lanes are connecting to 84-pin sliver connector.

CPU2 PCIE Port2

CPU2 PCIE P2 CD PCIE x 8 lanes are connecting to 84-pin sliver connector.

CPU2 PCIE Port3

CPU1 PCIE P3 AB PCIE x 8 lanes are connecting to 84-pin sliver connector.

3.2.7   SATA

There is no SATA port support in ES200 edge server.

3.2.8   USB

The ES200 Edge Server USB port distribution is as follows:

*   ASPEED BMC AST2500 consumes two USB 2.0 ports (one 1.1 and one 2.0)

*   Two USB3.0 ports in front side

*   One USB 2.0 port in the front IO board

The USB ports on the products are not required to be powered from STBY.

3.2.9   AST2500

The Server's Board Management Controller (**AST2500**) is a highly integrated single-chip solution, integrating several devices typically found on servers.

VGA Display Controller

- Fully IBM VGA compliant

- Maximum Display resolution: 1920x1200 32bpp@60Hz (reduced blanking)

- Support widescreen resolutions:

  - WXGA : 1280x800 32/16bpp @60Hz

  - WXGA+ : 1440x900 32/16bpp @60Hz

  - WSXGA+ : 1680x1050 32/16bpp @60Hz

  - FullHD+ : 1920x1080 32/16bpp @60Hz

DDR3L/DDR4 SDRAM Controller

- Support external 16-bit DDR3L/DDR4 SDRAM data bus width

- Maximum memory clock frequency

  - DDR3L: 800MHz (DDR3-1600)

  - DDR4: 800MHz (DDR4-1600)

GPIO Controller

- Directly connected to APB bus

- Support up to 228 GPIO pins, which are 29 sets

- Each GPIO set can be programmed to accept command from ARM, LPC(SIO), or Coprocessor.

- Programmable output mode: Push-Pull or Open-Drain

- Some GPIOs support Schmitt type input buffer for noise immunity

- 4 out of the 228 GPIO pins are with 16mA driving strength, others are 8mA driving strength

- 16 out of the 228 GPIO pins can support 1.8V mode.

- Support 8 sets of GPIO pass through (1 GPIO IN -- > 1 GPIO OUT) pin with internal switch control that is useful for some button function control.

3.2.10   TPM

In ES200 Edge Server the PCH supports TPM specification 2.0 implemented with a TPM header on the server board. It supports SPI interface TPM 2.0 module.

3.2.11   UART

ES200 Edge Server provides Host and BMC UART interfaces for development purpose.

3.2.12   Power connector for Accelerator Card

ES200 Edge Server can support two FHFL DW accelerator cards. The accelerator card needs external 12V power feed via cable. There is an 8-pin power connector on the PDB (power distribution board) that offers 12V power feed for the accelerator. The power feed capacity of the power connector is 336W (max. current is 28A).

3.2.13   Thermal Design

3.2.13.1   Thermal Solution for 2U System

CPU Heat Sink

- Dimension=113*78*24.7mm^3 (1U) for Full-Length PCIe AIC application,

  113*78*64mm^3 (2U) or Half-Length PCIe AIC application
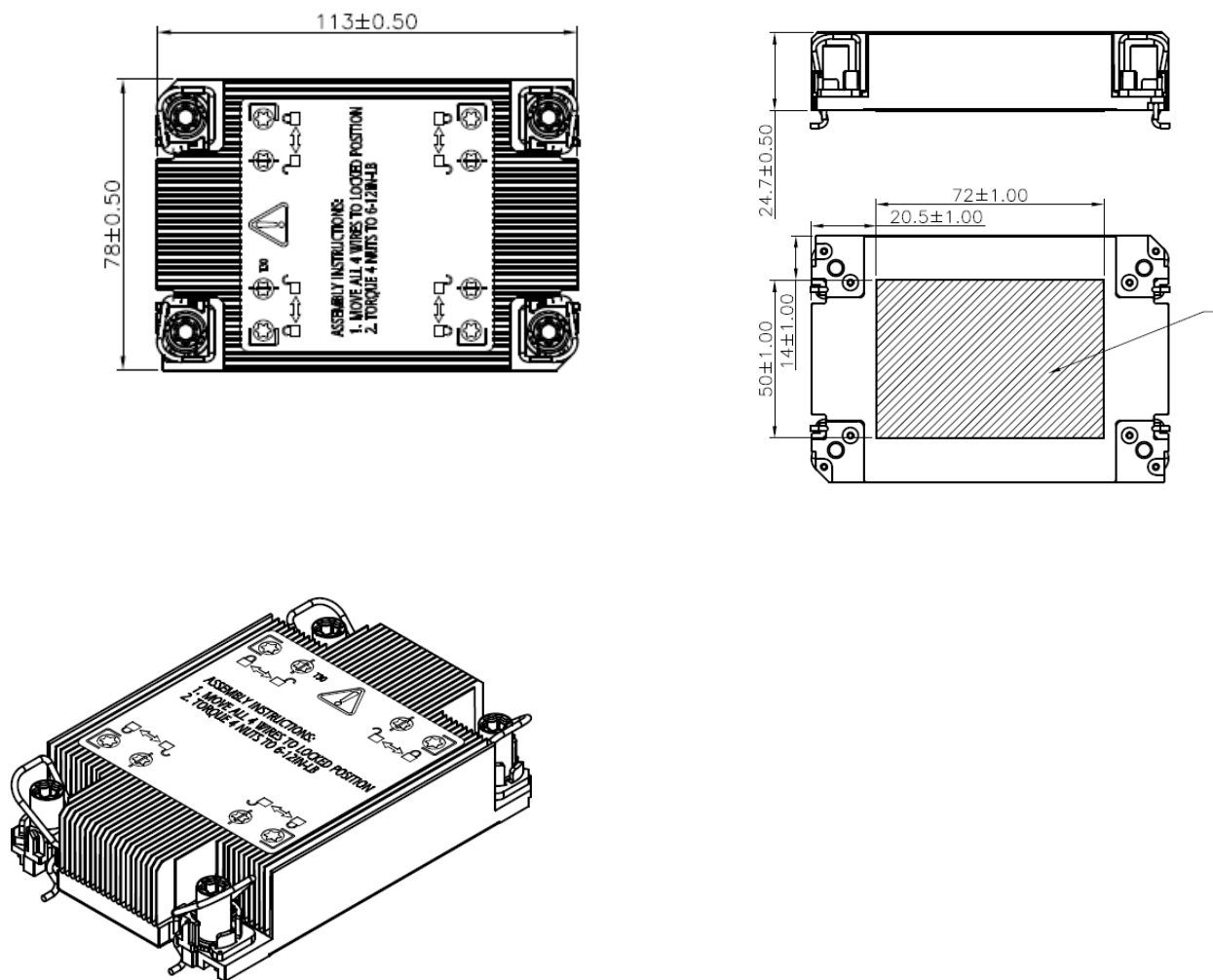
- Material=Al base + Cu block + Al Fin+ Heat pipe
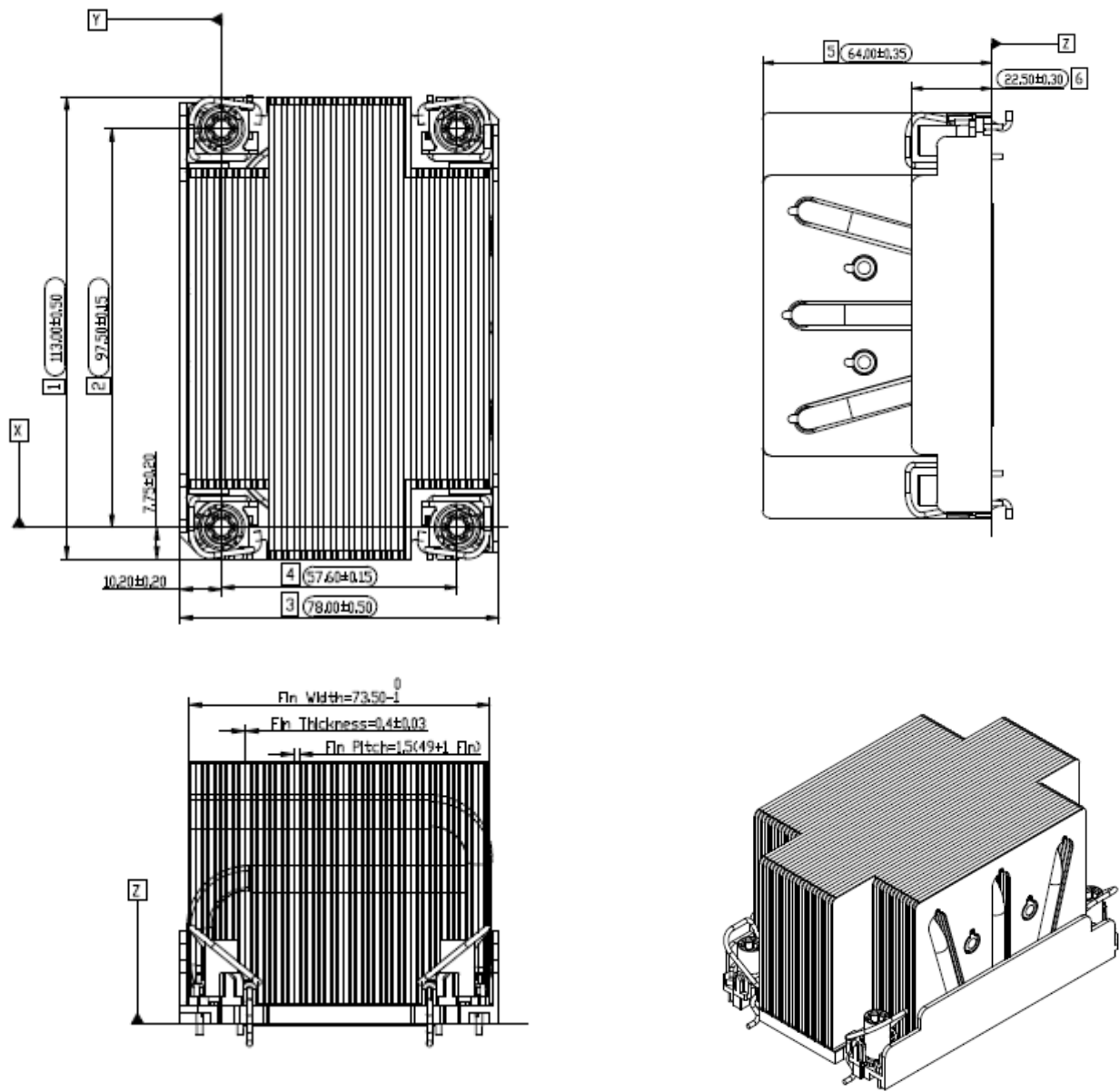

Figure 5: CPU Heat Sink Solution 1

Figure 6: CPU Heat Sink Solution 2

Fan x4

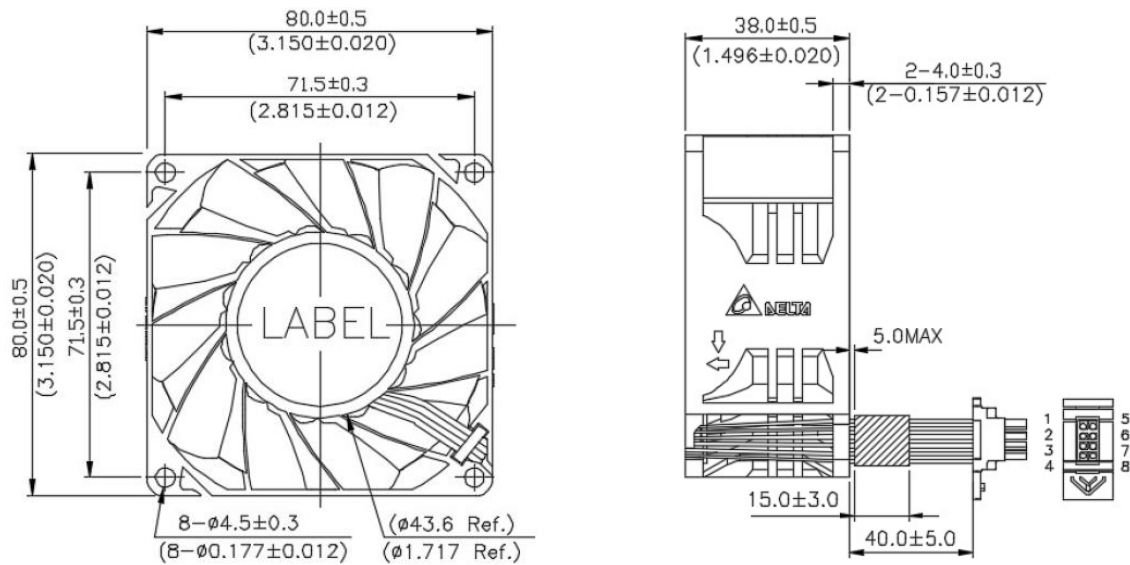- Dimensions=8038 (single rotor)

- Voltage=12 V

- PWM Frequency= 25 KHz

Figure 7: Fan Dimensions

4   Chassis Spec

4.1   2U System Overview

2U chassis can support the following configurations:

PSU
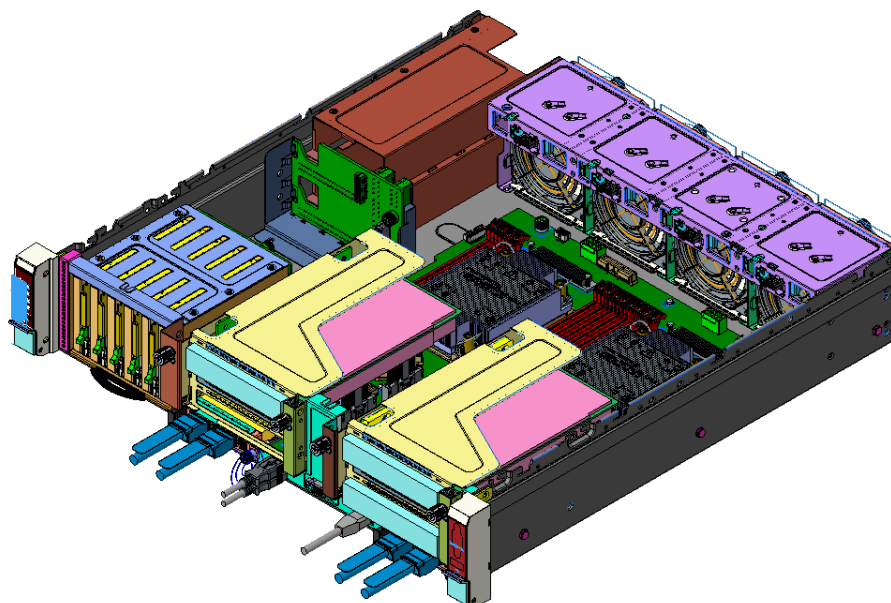
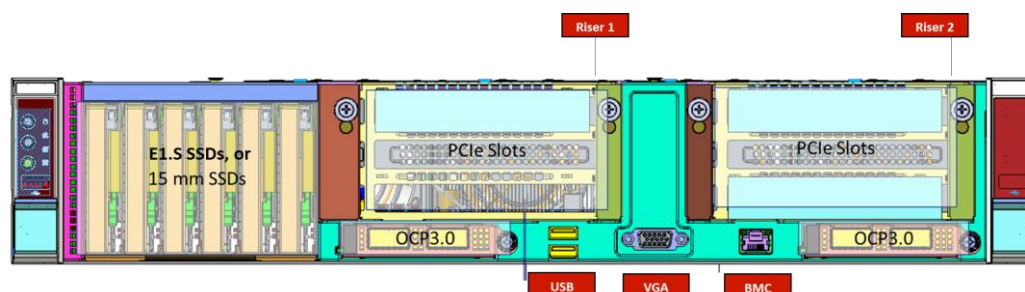- 1+1 redundant PSU

- AC/DC PSU.

Figure 8: 2U System Overview

Figure 9: System Front View

4.1.1   2U Chassis Dimensions

2U chassis dimensions are 438mm (W) x 451.1mm (D) x 87 mm (H).
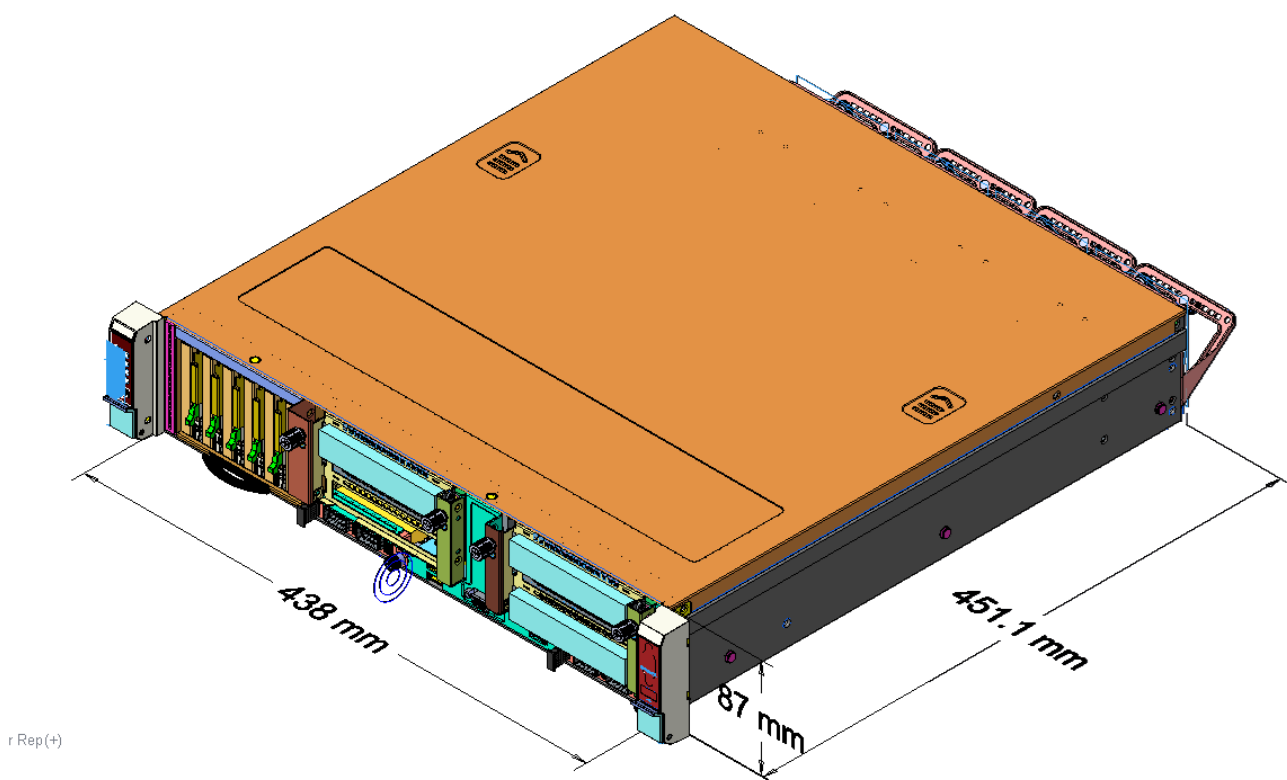

Figure 10: 2U Chassis Dimensions

5   Appendix

5.1   User Guidance

In the industry, there is a known vulnerability, [CVE-2019-6260](), when using ASPEED AST2500.
There are some approaches to mitigate:
  a.   Designers can refer to AST_usrGuide_QuickRef for CVE-2019-6260 to fine tune the firmware.
  b.   Designers can use another BMC chip to replace ASPEED AST2500 in the derivative designs.

5.2   Wiwynn actions to Aspeed QuickRef

According to CVE-2019-6260, ASPEED AST2400 and AST2500 Baseband Management Controller (BMC) hardware and firmware implement Advanced High-performance Bus (AHB) bridges, which allow arbitrary read and write access to the BMC's physical address space from the host.
The LPC, PCIe and UART AHB bridges are all explicitly features of ASPEED's designs for recovering BMC FW during firmware development or to allow the host to drive the BMC hardware even without any firmware on BMC.
The CVE applies to the Eight (8) specific cases of iLPC2AHB bridge Pt I, iLPC2AHB bridge Pt II, PCIe VGA P2A bridge, DMA from/to arbitrary BMC memory via X-DMA, UART-based SoC Debug interface, LPC2AHB bridge, PCIe BMC P2A bridge, and Watchdog setup.

●   iLPC2AHB bridge Pt I
[Suggested Mitigation of CVE] Can be disabled by configuring a bit in the BMC's LPC controller.
Wiwynn would disable the AST2500 L2A bridge in the firmware.

●   iLPC2AHB bridge Pt II
[Suggested Mitigation of CVE] Disable Super I/O decoding on the LPC bus (0x2E/0x4E decode).
Decoding is controlled via hardware strapping and can be turned off at runtime,
however disabling Super I/O decoding also removes the host's ability to configure SUARTs, System wakeups, GPIOs and the BMC/Host mailbox

After disabling Super I/O function, it would impact POSTCode, COM1/2 and SOL functions.
Wiwynn would disable L2A bridge and Super I/O function as the default setting, yet it will be configurable when needed.

●   PCIe VGA P2A bridge
[Suggested Mitigation of CVE] Can be disabled or filter writes to coarse-grained regions of the AHB by configuring bits in the System Control Unit
Wiwynn would disable the AST2500 PCI2AHB bridge in the firmware.

●   DMA from/to arbitrary BMC memory via X-DMA
[Suggested Mitigation of CVE] X-DMA accesses are configured to remap into VGA reserved memory in u-boot
Wiwynn would block the AST2500 X-DMA access in the firmware.

●   UART-based SoC Debug interface
[Suggested Mitigation of CVE] Can be disabled by configuring a bit in the System Control Unit.
Wiwynn would disable the AST2500 U2A function in the firmware.

- LPC2AHB bridge

[Suggested Mitigation of CVE] Don't enable the feature.
Wiwynn would disable the AST2500 LPC_2_SPI function in the firmware.

- PCIe BMC P2A bridge

[Suggested Mitigation of CVE] Don't enable the feature.
Wiwynn would disable the AST2500 PCI BMC device in the firmware

- Watchdog setup

[Suggested Mitigation of CVE] State: Required system function, always available
Wiwynn would only trigger Watchdog Timer in the "SOC Reset" mode