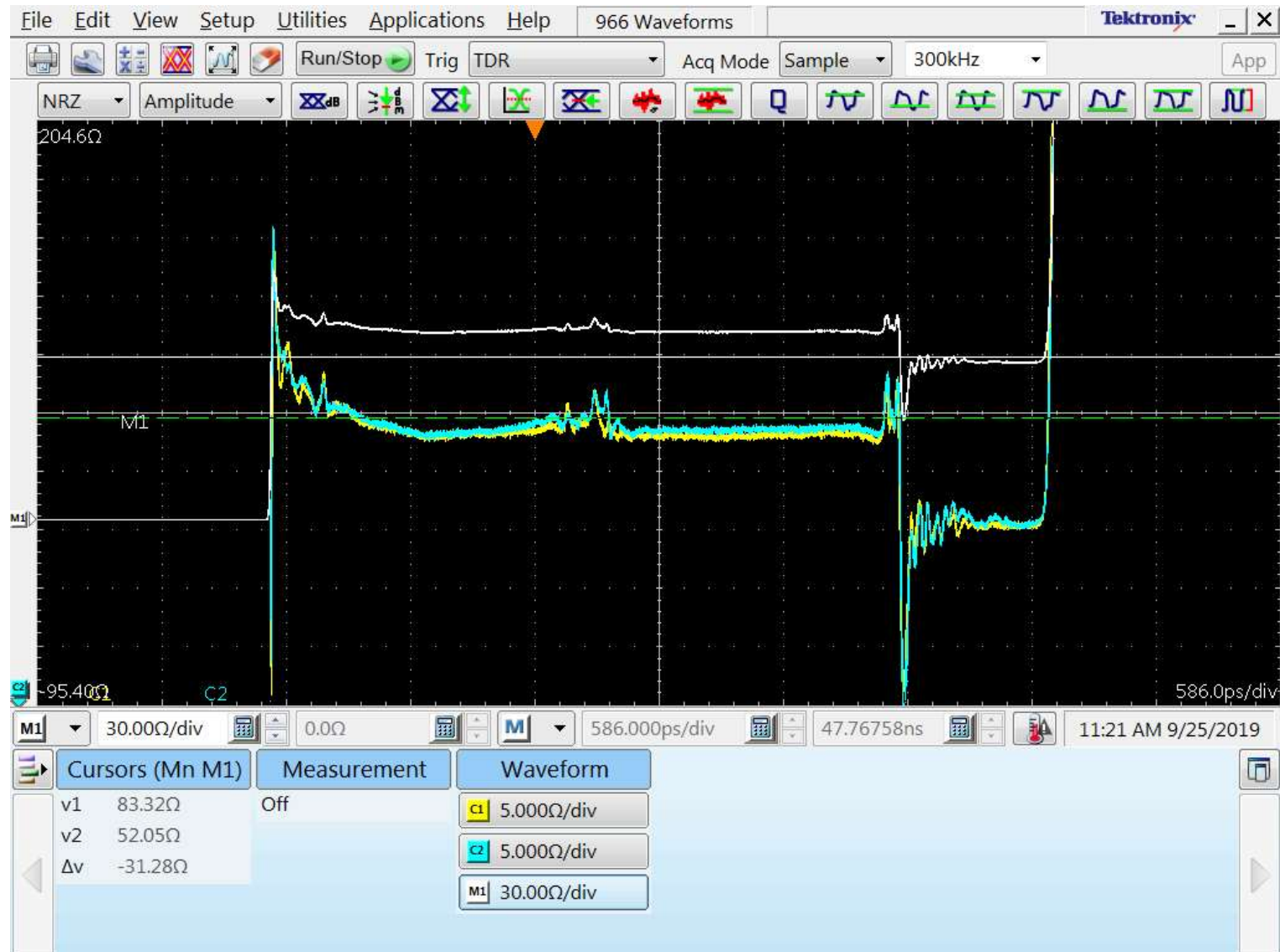# OCP CLB
Impedance Analysis

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Hewlett Packard Enterprise

TDR - OCP CLB RX00

TDR - OCP CLB TX00

TDR – PCIe G4 CLB RX00

TDR – PCIe G4 CLB TX00

Why there is BIG impedance drop on OCP CLB?

OCP CLB Stackup

- Cross section information from the board file

CLB_Gen4/ftcmkx03.brd

Design Cross Section

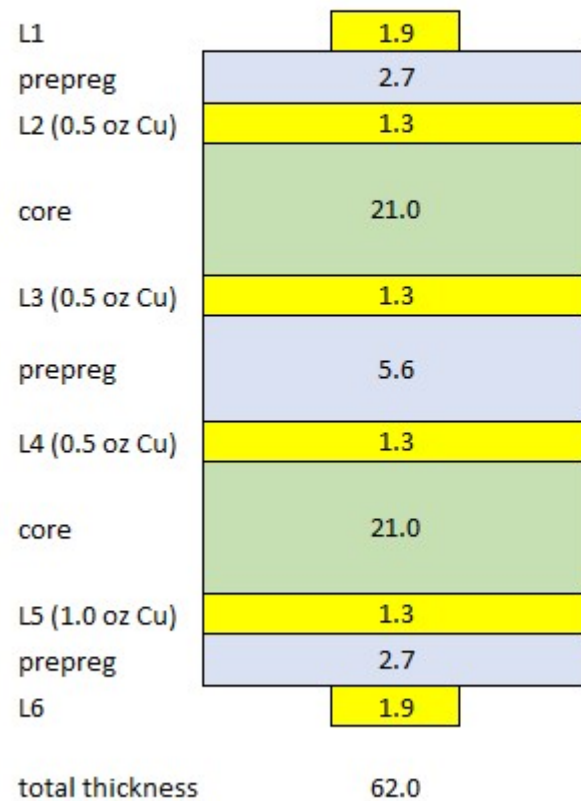| Subclass Name	Type	Material	Thickness (MIL)	Tol +	Tol -	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent
	SURFACE	AIR				0	1	0
TOP	CONDUCTOR	COPPER	1.900000	0	0	595900	4.5	0
	DIELECTRIC	FR-4	2.700000	0	0	0	4.5	0.035
GND	PLANE	COPPER	1.300000	0	0	595900	4.5	0.035
	DIELECTRIC	FR-4	21.000000	0	0	0	4.5	0.035
VCC	PLANE	COPPER	1.300000	0	0	595900	4.5	0.035
	DIELECTRIC	FR-4	5.600000	0	0	0	4.5	0.035
GD2	PLANE	COPPER	1.300000	0	0	595900	4.5	0.035
	DIELECTRIC	FR-4	21.000000	0	0	0	4.5	0.035
GD3	PLANE	COPPER	1.300000	0	0	595900	4.5	0.035
	DIELECTRIC	FR-4	2.700000	0	0	0	4.5	0.035
BOTTOM	CONDUCTOR	COPPER	1.900000	0	0	595900	4.5	0
	SURFACE	AIR				0	1	0

Total Thickness: 62 MIL

PCIe CLB

6.3.5.1 Test Fixture Requirements

A test fixture for connector S-parameter measurement must be designed and built to the following:
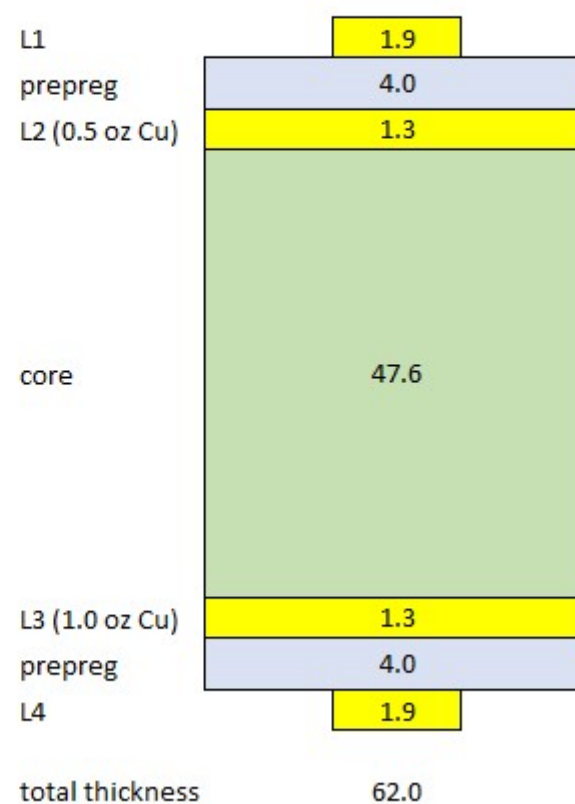
- The test fixture used for measuring S-parameters will comprise a baseboard and mating Add-in Card fabricated from the same PCB panel. The total thickness of the boards, measured across the Add-in Card edge fingers, must be 1.57 mm (062 mil).

- The PCB test fixture must be an FR-4 based material, or of a lower loss material with a relative permittivity of 3.6 or greater. Dielectric loss factor is not specified.

- The test PCB must have a microstrip structure; the microstrip's dielectric thickness or stackup are recommended to be approximately 0.102 mm (4 mil).

- The interconnect traces on all boards must be routed uncoupled (single ended) where possible. Some method of mitigating fiber weave effects must be applied. This can include off-axis routing or board rotation on the PCB panel.
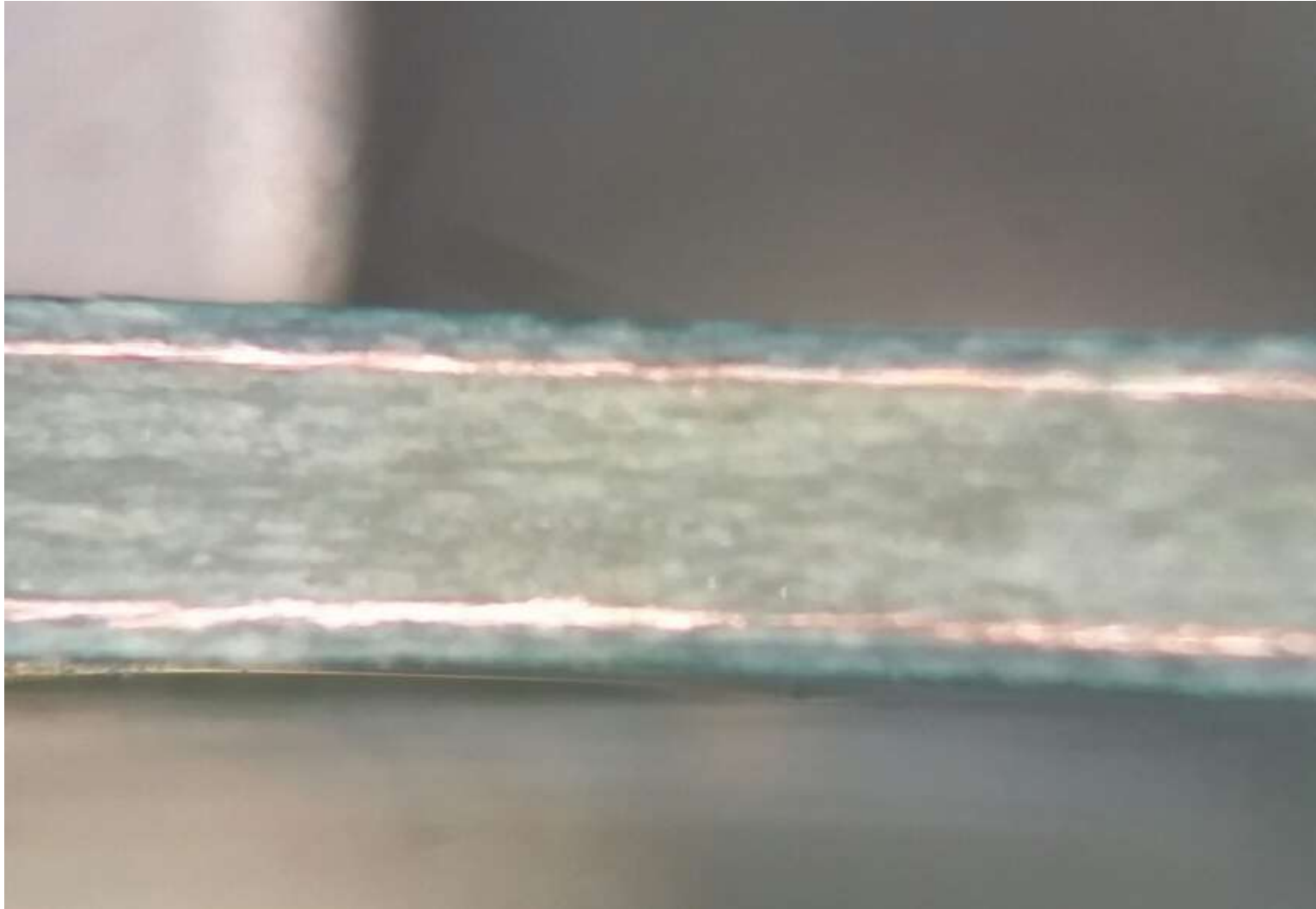
OCP vs PCIe CLB stackup

OCP

Layer	Thickness
L1	1.9
prepreg	2.7
L2 (0.5 oz Cu)	1.3
core	21.0
L3 (0.5 oz Cu)	1.3
prepreg	5.6
L4 (0.5 oz Cu)	1.3
core	21.0
L5 (1.0 oz Cu)	1.3
prepreg	2.7
L6	1.9
total thickness	62.0

PCIe

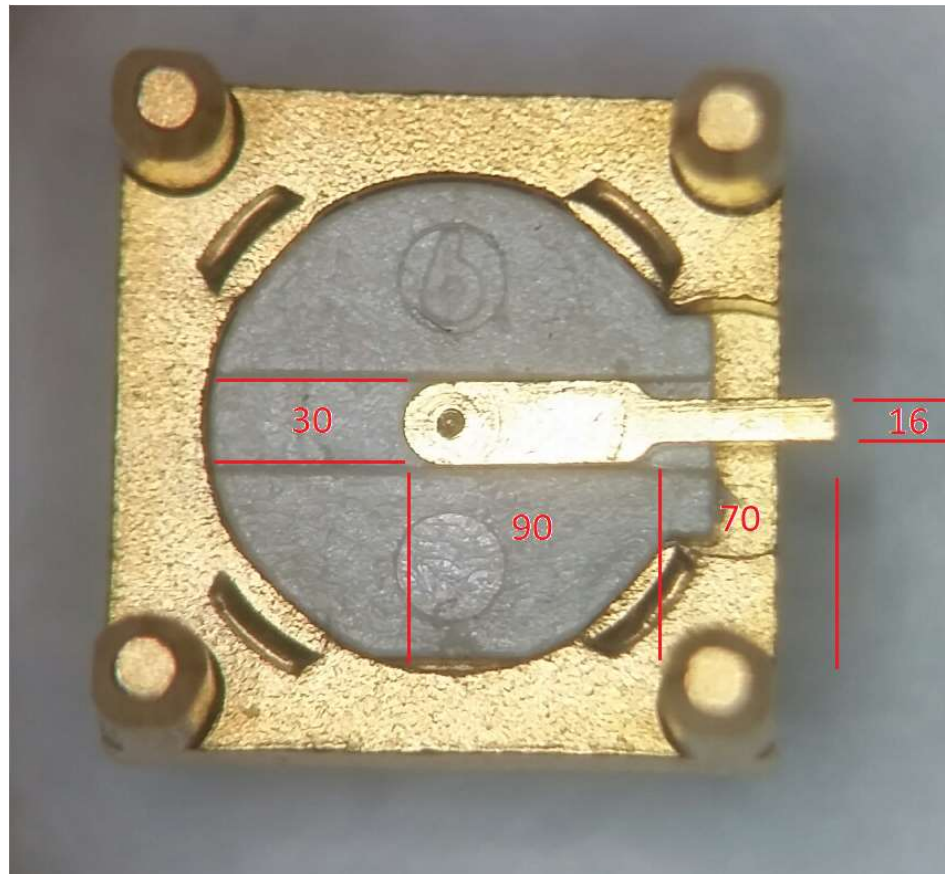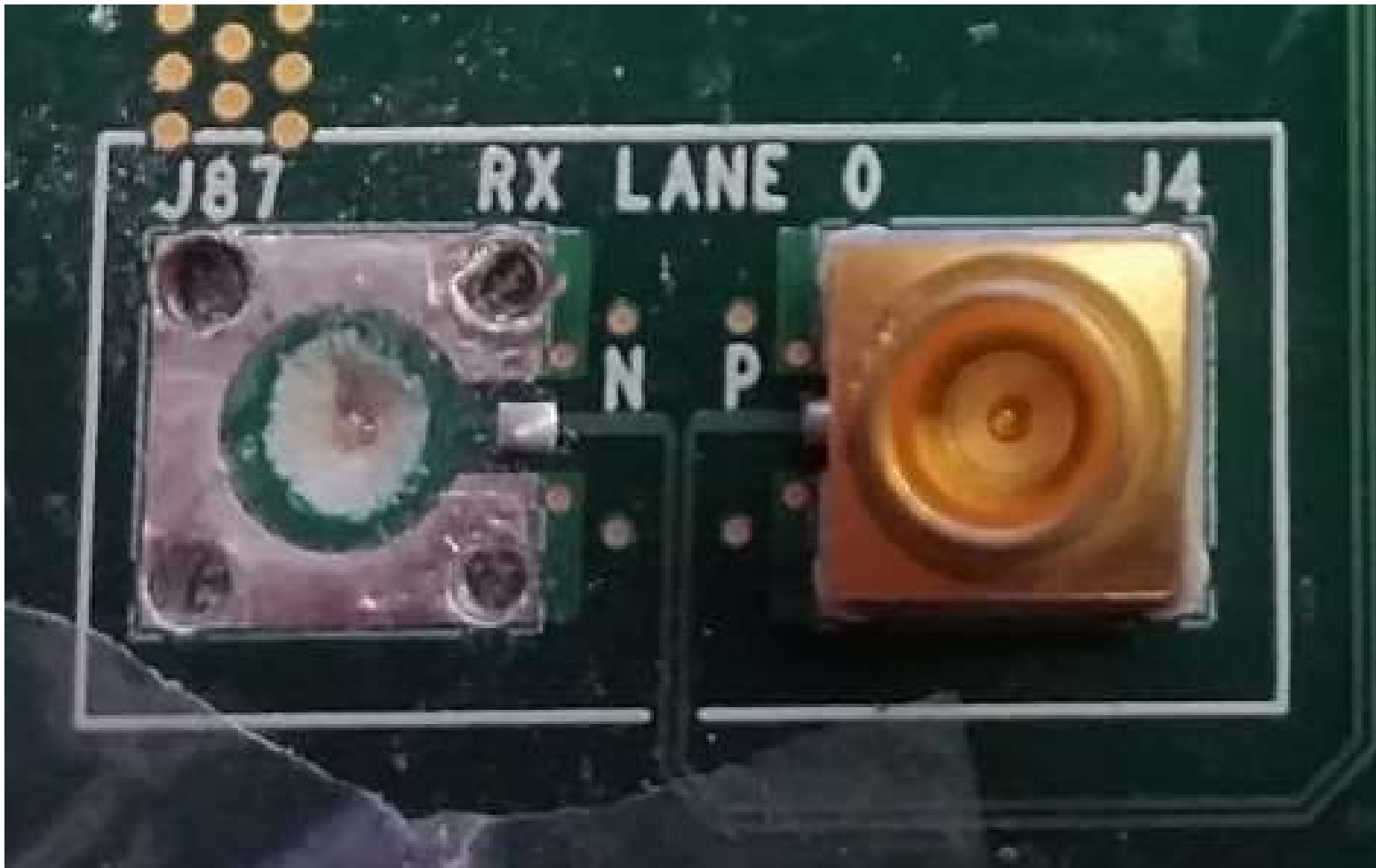| Layer	Thickness
L1	1.9
prepreg	4.0
L2 (0.5 oz Cu)	1.3
core	47.6
L3 (1.0 oz Cu)	1.3
prepreg	4.0
L4	1.9
total thickness	62.0

PCI-SIG Gen4 CLB X-section

SMP Header

- 30 mil wide metal on the SMP header creates large capacitance from L2 and thus causes significant impedance drop
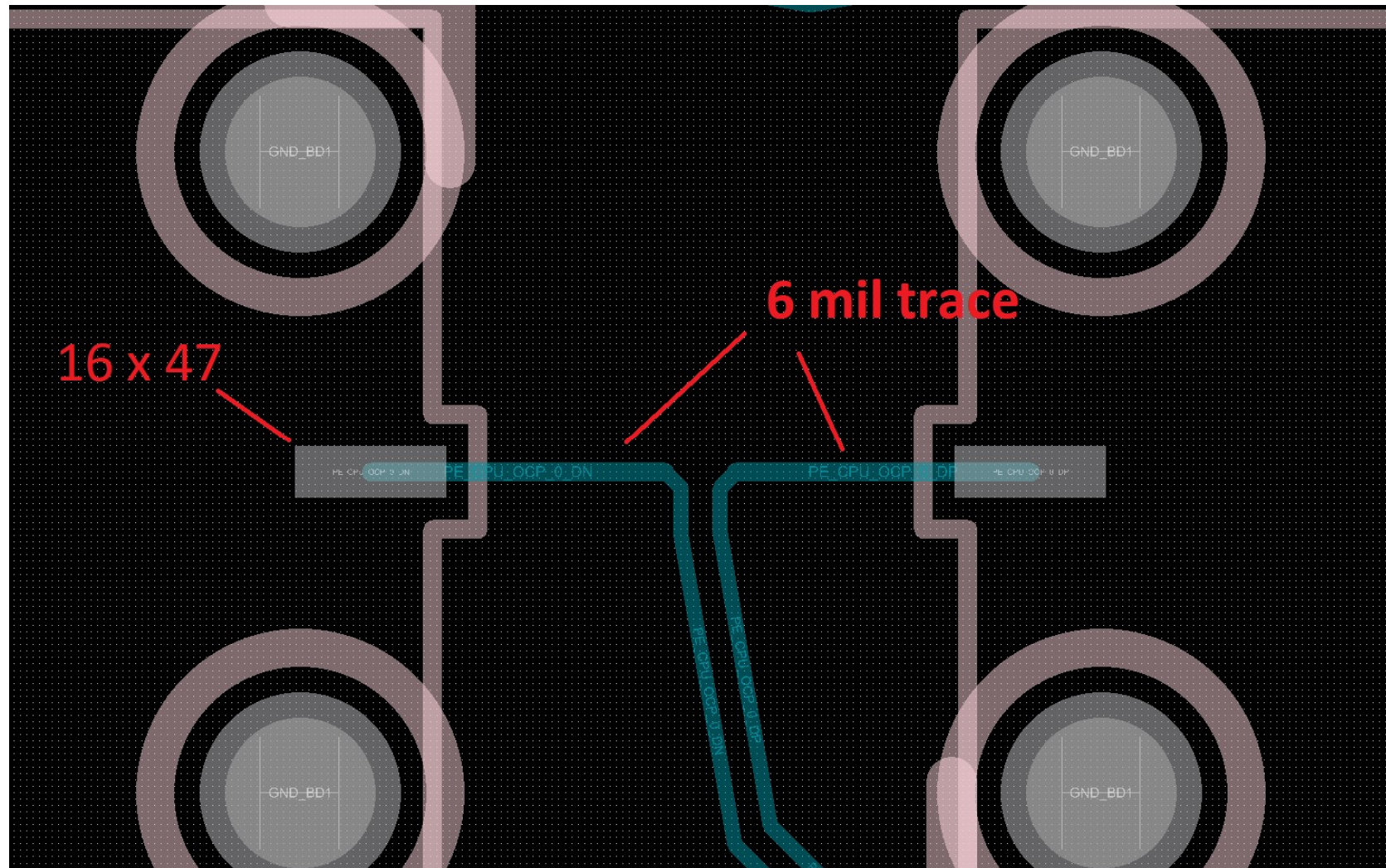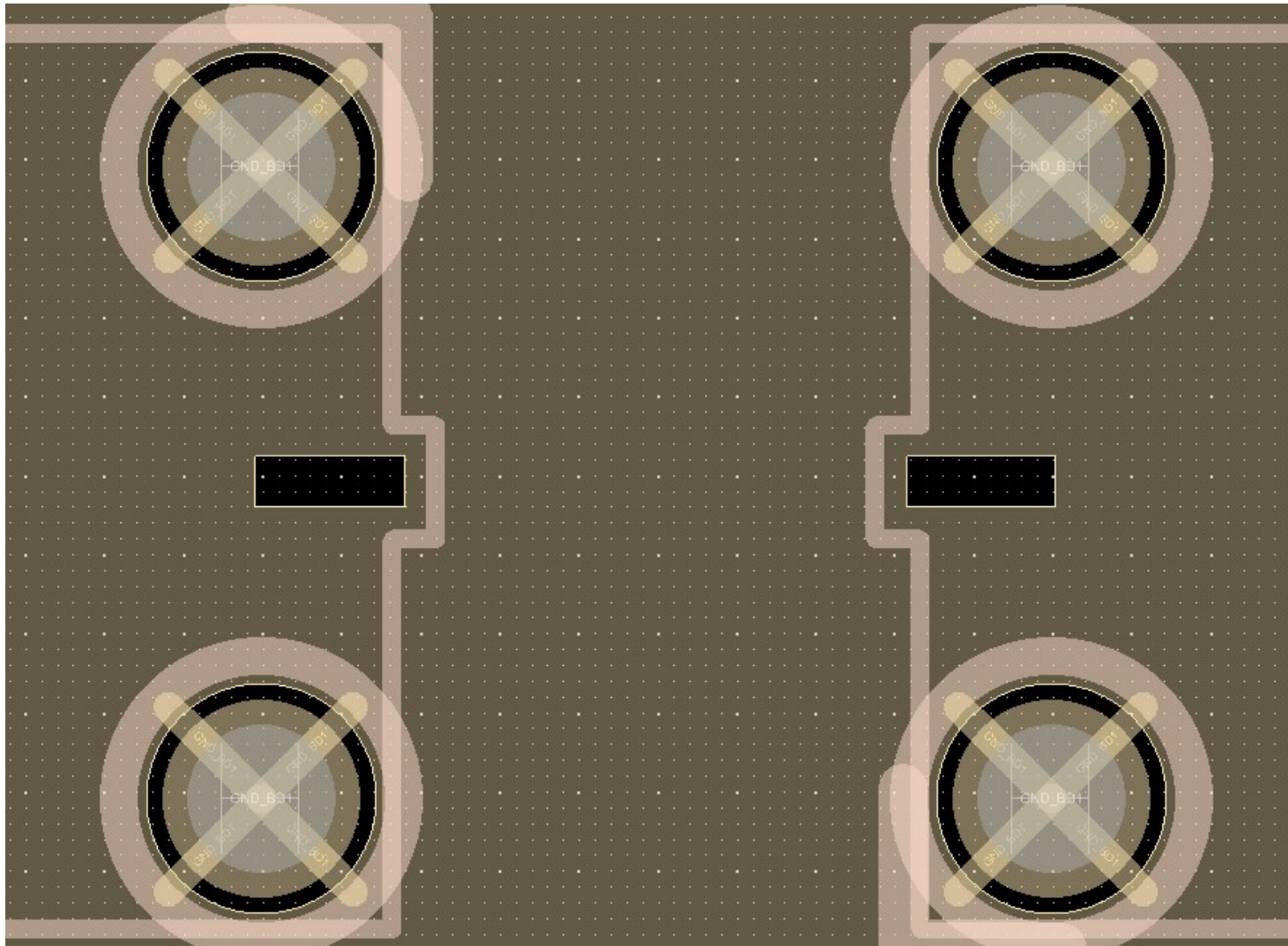
How does PCI-SIG CLB get around?

- Create void underneath the header on L2

OCP CLB – L1

OCP CLB – L2 & L3

Impedance Simulation Results

Layer	Thickness
L1	1.9
prepreg	2.7
L2 (0.5 oz Cu)	1.3
core	21.0
L3 (0.5 oz Cu)	1.3
prepreg	5.6
L4 (0.5 oz Cu)	1.3
core	21.0
L5 (1.0 oz Cu)	1.3
prepreg	2.7
L6	1.9
total thickness	62.0

Z0

13 impedance if L2 is reference

37 impedance if L3 is reference (void on L2)

40 impedance if L4 is reference (void on L2 & L3)

43 impedance if L5 is reference (void on L2, L3 & L4)

Recommendation

- Create void underneath the SMP header on L2, L3 & L4