Partial Width, Density Optimized HPM Form (M-DNO) Factor Base Specification

Part of the

Datacenter – Modular Hardware Systems (DC-MHS) Rev 1.0 Family

Version 0.9

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1.2. Acknowledgements

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2. Version Table

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Date	Version #	Description
4/21/2022	0.7	• Initial Public Release
6/22/2022	0.8	• Added Specification Compliance Table • Separated hole dimensioning to separate drawings • Added required pad size and recommended KOZs for all holes throughout document • Adjusted fixed riser connector positioning • Updated approach in Primary Side Component Height section • Added start of “zone” approach to PIC connector placement • Various text clarifications / edits • Various drawing updates and fixes
8/24/2022	0.9	• Rewrite of secondary side stackup, board thickness, board pan etc. (10.3, 10.4) • Removed Type 1 (many) • Changed certain values for Type 3 to TBD (many) • Placed all mounting hole information in one place (10.2) • Changed “mid-board” mounting holes from required to HPM Designer preference for all board types (10.2) • Removed secondary side keep out features for other board type hole locations (10.4) • Modified type 4 board outline in custom zone area (10.1) • Shifted HPM retention hole location (10.5) • Updated dimension scheme for recommended riser connectors, simplified verbiage for riser requirements (10.9) • Updated dimension scheme for PICPWR connectors (10.1.6) • Aligned PICPWR location optional / required characteristics across all board types (11.1) • Added PDB Management Connector (10.8) • Miscellaneous image and text cleanup throughout document (see change bars) • Added updated approach to primary side component height restrictions (10.12) • Added 1016 as a recommended option on far side (12.1) • Updated bottom side KOZ for board retention hole to align with FLW update (10.5) • Removed cable enablement section (added note to primary side KOZ section) • Added 2x3 PICPWR option, additional cleanup in power section (11.x) • Added adapted HPM chapter, moved note from power chapter to new chapter (13.x) • Simplified Ch 9 (removed board type goals) • Added tolerance table and custom tolerance for type 2/3 width (10,10.1) • Increased resolution of all figures • Additional Tweaks to NearIO verbiage to try and clarify intent (10.9) • Added required handle hole geometry (10.6) • Added Platform Custom Zone section with content TBD (10.13) • Added SFF number for riser connectors (12.1) • Scrubbed compliance table, added note not final until 1.0 (4) • Updated PIC connector locations (10.8) • Added example of re-purposing required mounting hole for Handle hole geometry

3. Scope

This document defines technical specifications for the Density Optimized Form Factors used in Open Compute Project Data Center Modular Hardware System.

Any supplier seeking OCP recognition for a hardware product based on this spec must be 100% compliant with any and all features or requirements described in this specification.

3.1. Items Not In Scope of Specification

- Compute Core (CPU/Memory/Voltage Regulators/SMP routing between CPUs)
- JTAG/Debug connectors for the Compute Core
- CPU, Memory, Heatsink, Liquid and any other thermal solutions
- Reliability requirements and design-in details
- BOM Population requirements
- Cooling System Connections (Fans, etc).

3.2. Typical OCP Sections Not Applicable

This is a Base specification, requiring other MHS specifications to fully define a design. The following typical Sections of an OCP specification are not included because they are not applicable to this specification.

- Rack Compatibility (Discussed in Section 8)
- Physical Spec
- Thermal Design
- Rear Side Power, I/O, Expansion
- Onboard Power System
- Environmental Regulations/Requirements
- Prescribed Materials
- Software Support
- System Firmware
- Hardware Management (Leverages OCP DC-SCM V2)
- Security

4. Specification Compliance Table

(Not Final for .9, Subsequent Section Requirements supersede this until 1.0 Release.)

The following table is intended summarize the list of attributes and requirements for a design to be MHS – DNO Spec Compliant. It specifies only required attributes for compliance and does not list optional attributes.

Table 1. Specification Compliance Summary Table

Item	Requirement	Document Reference
	Mechanical	**Chapter 10**
1	Defined Board Outline	Section 10.1, Figure 4 - Figure 6
2	All required mounting holes with associated pads and KOZ	Section 10.2, Figure 7- Figure 10
3	Unique alignment hole and slot with associated pad and KOZ	Section 10.2, Figure 7- Figure 10
4	Board Thickness <= 3.18mm	Section 10.3
5	Board Assembly Thickness <= 5.86mm	Section 10.4 & 10.3
6	Secondary side chassis hook keep out zones	Section 10.4, Figure 17 - Figure 19
7	1.6mm Secondary side universal component height restriction	Section 10.4, Figure 12
8	HPM Secondary side support 1.78mm +/- 0.10mm thick	Section 10.4 & 10.3, Figure 14
9	HPM to Chassis Retention hole and associated KOZs	Section 10.5, Figure 20
10	Far Side hole for board handling with defined geometry	Section 10.6, Figure 21 & Figure 22
11	Specified Location for OCP NIC 3.0 Co-Planar Connector	Section 10.7, Figure 23
12	Specified Location for DC-SCM Co-Planar Connector	Section 10.7, Figure 23
13	Primary control panel connector placed within specified zone	Section 10.8, Figure 24 & Figure 25
14	Intrusion switch header placed within specified zone	Section 10.8, Figure 24 & Figure 25
15	Host USB connector placed within specified zone	Section 10.8, Figure 24 & Figure 25
16	PDB Management connector placed within specified zone	Section 10.8, Figure 24 & Figure 25
17	Any implemented board to board riser connectors placed in specific defined location	Section 10.9.2, Figure 27 & Figure 28
18	2 (Type 2,3) or 3 (Type 4) I/O Retention Holes and KOZs	Section 10.9.2, Section 10.11, Figure 28 & Figure 29
19	All non-exempt soldered components adhere to Primary Side component height restrictions	Section 10.12, Figure 30 & Figure 31
	Power	**Chapter 11**
20	Far side Ingress / Egress Power Zone with at least 1 2x6 + 12SB PICPWR connector in specified location(s)	Section 11.1.1, Section 11.1.6, Figure 35
21	If implemented, Near side Ingress / Egress Power Zone with 2x3+6S or 2x6+12S PICPWR connector(s) in specified zone	Section 11.1.1, Section 11.1.6, Figure 35
22	Each implemented riser location connector is PICPWR compliant	Section 11.1.2, M-PIC
23	HPM delivers at least 87W to each implemented riser location	Section 11.1.2
24	HPM delivers power as defined in OCP DC-SCM 2.0 specification to DC-SCM connector	Section 11.1.3, OCP DC-SCM R2.0
25	HPM delivers power as defined in OCP NIC 3.0 specification to DC-SCM connector	Section 11.1.4, OCP NIC R3.0
26	HPM power shapes have a max 30C T-rise	Section 11.2
27	At maximum load, HPM voltage drop between primary power ingress and egress connectors is <= 1%	Section 11.2
	Electrical (I/O System)	**Chapter 0**
28	All HSIO connectors (near and far) are M-XIO compliant	Section 12.1, M-XIO
29	Internal USB follows M-PIC specification	Section 12.2, M-PIC
30	Intrusion Switch follows M-PIC specification	Section 12.3, M-PIC
31	If implemented, boot storage peripheral follows M-PIC specification	Section 12.4, M-PIC
32	Primary control panel follows M-PIC specification	Section 12.5, M-PIC
33	If implemented, secondary control panel follows M-PIC specification	Section 12.5, M-PIC
34	PDB Management Connector follows M-PIC specification	Section 12.6, M-PIC

5. Overview

The objective of this specification is to outline the requirements of a family of partial width, **D**e**N**sity **O**ptimized Host Processor Module (HPM) form factors within the OCP **M**odular hardware system group of specifications (**M-DNO** for short). This M-DNO specification embodies design considerations for CPU, DIMMs, and other server processor related features commonly used by the industry today but is not limited to only those functions. For instance, an FPGA array being placed within the Compute Area of the HPM is allowable per this specification. The HPM is designed with standard 19” rack, also known as compliant with EIA - 310-E and larger 21” racks in mind but is not limited to only those solutions. This specification considers both monolithic and multi-node / “blade” based system architectures in its definition.

The goals and successes of this specification are defined by allowing multiple generations of Compute Core (CPU/Memory) designs implemented to the specification to enable reuse of chassis and system level components over multiple generations and HPMs. Implementing to this specification and design methodology should result in reduced design investment, reduced validation investment, broader product portfolios and faster development cycle times due to enhanced reuse and leverage opportunity for each HPM designed.

This specification shall define attributes and design requirements that are common and critical to the use and deployment of Enterprise and Cloud solutions and may also apply to EDGE optimized service provider products. Examples of these attributes are mechanical form factor, placement guidance of common subsystems and placement guidance of HPM Power and Input-Output (IO) connections.

6. References

DC-MHS Family of Specifications

The **D**ata **C**enter – **M**odular **H**ardware **S**ystem (DC-MHS) family of specifications are written to enable interoperability between key elements of datacenter and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks. At the time of this publication there are the following specification workstreams:

- **M-FLW** (**M**odular Hardware System **F**u**l**l **W**idth Specification) – Host Processor Module (HPM) form factor specification optimized for using the full width of a Standard EIA-310 Rack mountable server. The specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-DNO** (**M**odular Hardware System Partial Width **D**e**n**sity **O**ptimized Specification) – Host Processor Module (HPM) specification targeted to partial width (i.e. ½ width or ¾ width) form factors. Such form factors are often depth challenged and found not only in enterprise applications but also in Telecommunications, Cloud and Edge Deployments. While the EIA-310 Rack implementation is chosen as a key test case for use, the specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-CRPS** (**M**odular Hardware System **C**ommon **R**edundant **P**ower **S**upply Specification) – Specifies the power supply solutions and signaling expected to be utilized by DC-MHS compatible systems.
- **M-PIC** (**M**odular Hardware System **P**latform **I**nfrastructure **C**onnectivity Specification) – Specifies common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems. Examples include power management, control panel and cooling amongst others.
- **M-XIO** (**M**odular Hardware System E**x**tensible **I**/**O**) – Specifies the highspeed connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers with peripheral subsystems such as PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.
- **M-PESTI** (**M**odular Hardware System **Pe**ripheral **S**ideband **T**unneling **I**nterface) – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (e.g., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination.

To access additional DC-MHS specifications please visit the OCP Server Project Wiki - Working

Additional References

This specification also relies on the following Open Compute Project specifications

1. OCP Server Network Interface Card (NIC) 3.0 – Specifies NIC card form factors targeting a broad ecosystem of NIC solutions and system use cases.
   Mezz (NIC) » Open Compute Project

2. OCP Datacenter Secure Control Module (DC-SCM) 2.0 – Specifies an SCM designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center.
   Hardware Management/Hardware Management Module - OpenCompute

7. Terminology

Standardized Term	Meaning	Alternative Terms
Shall	Indicates a requirement for spec compliance	Must
DC-SCM	Datacenter Secure Control Module v2 as defined by OCP DC-SCM 2.0 spec	SCM
PCB	Printed Circuit Board	PCBA
HPM (Host Processor Module)	PCB or PCBA form-factor being defined by this spec	Motherboard, board
Chassis-Board Bracket	Bracket that attaches to an HPM assembly, that enables a variety of board outlines and hole locations to change over time, and still fit within same chassis base.	Board Pan
Near	Board location or zone, related to section of board closer to the datum	
Far	Board location or zone, opposite of location of datum	
Platform	Complete system including HPM, power, peripherals, etc	
Compute Core	Elements of board design that are critical to processor and memory support, inclusive of CPU and Memory sockets. Examples are Voltage Regulators, High Speed IO routing, High speed trace routing between multiple processors, high speed trace routing between processors and memory, etc	
IO	Input Output, commonly referring to high speed connections to a CPU socket.	
PCIe	Peripheral Component Interconnect Express	
CXL	Compute Express Link	
HSIO	High Speed IO, commonly referring to PCIe routing, PCIe connectors, CXL routing/connectors, etc.	
OCP	Open Compute Project	
OEM	Original Equipment Manufacturer	Enterprise
CSP	Cloud Service Provider	
½ Width HPM	210mm wide HPM, enables systems with 2 HPMs side by side in 19” Rack	
¾ Width HPM	295mm wide HPM, enables systems with HPM adjacent to 2xM-CRPS PSUs	
Platform Custom Zone	Area of system board where space is allotted for Platform designers to implement custom features.	

Platform Infrastructure Connectivity Specification	Refer to Section 6 (References)	M-PIC
Full Width Specification	Refer to Section 6 (References)	M-FLW
Common Redundant Power Supply Specification	Refer to Section 6 (References)	M-CRPS, CRPS PSU
Extensible I/O Specification	Refer to Section 6 (References)	M-XIO
KOZ	Keep Out Zone, a design term for PCB designs that defines area of a board design where no components may be placed, usually to enable mechanical attachments or mechanical features.	
KIZ	Keep In Zone, a design term for PCB designs that define a zone with a height restriction (such as a volume), which the components selected for that part of the board design must comply with the height restriction of that zone.	
Compliant HPM	An HPM which meets every item listed in the M-DNO specification compliance table.	
Adapted HPM	An HPM that utilizes a Compliant HPM as a construct, with a specific set of repeatable modifications which form the adaptation.	
HPM Designer	The person or organization designing an HPM (whether compliant or adapted) which implements the M-DNO specification.	
System Designer	The person or organization designing a system which incorporates M-DNO HPMs (whether compliant or adapted) into the system design.	

8. Background & Assumptions

M-DNO targets a wide variety of 1 and 2 socket platforms including multi-node and monolithic (one HPM per chassis) systems for use in Enterprise, Cloud, and EDGE applications. In these applications the range of targeted chassis can be extremely varied, as can the location of the HPM within the chassis. Monolithic systems are typically, but not limited to, 1RU or 2RU designs. Multi-node systems on the other hand are expected to have a broad application set from 2U (e.g. 4 ½ Width HPMs) to 5U (e.g. 8-12 ½ Width HPMs in vertical orientation) chassis and beyond. Rear and Front service models (including articulating chassis with removable cover) are also considered.

When considering representative system depth targets, the most common environments were distilled into the following categories:

1. **Standard Depth Rack / Solution**
   - ~1070mm+ deep with a single ½ width (210mm) or ¾ width (295mm) HPM
   - ~1070mm+ deep with two ½ width (210mm) HPMs
2. **Mid Depth Rack / Solution**
   - ~430mm to 570mm deep with a single ½ width (210mm) or ¾ width (295mm) HPM
3. **Short Depth Rack / Solution**
   - ~350mm to ~430mm deep with a single ½ width (210mm) HPM

This specification shall focus on products targeted to these primary environments. **Section 0** illustrates design scenarios for each of these solutions providing the reader a clearer understanding of each category. This specification does not in any way prohibit alternate environments.

8.1. Common Industry Platform Features Considered

Mechanical

- Chassis installation within minimum EIA-310-E racks (but not limited to)
- PCIe Riser Connector fixed placement
- PCIe Cable route considerations
- Any additional fixed connector placement

I/O

- PCIe (Version 3.0, 4.0, 5.0, and future) Card configurations typically offered by Enterprise OEMs/CSPs/CoSPs.
- In 1U offerings with PCIe CEM based I/O, only Half-Length PCIe cards (167.6mm) are considered. This does not prevent Three-Quarter Length (254mm) cards, but support for Three-Quarter Length cards would restrict Compute Core placement (not defined).
- Use of Open Compute peripherals connectors on the HPM
  - OCP NIC v3.0
  - DC-SCM v2.0
  - *Note: While each HPM outline requires 1 connector of each type, a system* is not limited to 1 device of each type; configurations with 0 or >1 OCP NIC v3 / DC-SCM v2.0 are possible, but outside the scope of this specification

Power

- HPM supplied power to each fixed riser locations
- HPM Power Ingress and Egress connector placement for a variety of power layouts (PSUs with Cabled PDB, blind mate to bus bar, multi-node backplane, etc.)
- Considerations for Power Delivery to important chassis subsystems.

Thermal

- Thermal Design considerations including keep-out zone to enable thermal solutions that extend beyond the CPU and Memory sockets.

8.2. Architecture Specific Assumptions

Mechanical / Systems

- M-DNO based systems
    - Do not direct plug PSUs into the HPM but instead leverage Power Distribution Boards (PDB) or other system / rack level power infrastructure
    - Use remote fan designs in air cooled platforms (there is no HPM spec provision for Fan connectors on the HPM)
    - Support riser based I/O cards, cable based I/O cards or a mix of both
    - Leverage a variety of front and rear service models of I/O, PSU, HPM, etc.
- Systems designed for larger HPM Types may support use of smaller Types in a common chassis or sled with minimal changes (e.g. cables, riser quantities, standoff locations)
- Multi-node chassis designs leverage static rails with overall inner chassis opening width of 443mm (in 19” rack)
- Monolithic chassis designs leverage slide rails with overall inner chassis width of 431mm (in 19” rack)
- ¾ Width HPM must accommodate 2x 60mm M-CRPS PSUs within chassis opening described above (431mm)

I/O

- All M-DNO HPM Types enable (but do not require systems to leverage) use of “off the shelf” OCP NIC V3.0
- Mid / Standard Depth systems will *typically* leverage Coplanar OCP NIC layouts
- Short Depth systems will often require alternate implementation such as “floating” the OCP NIC (or no-pop)
- PCIe CEM based I/O will be the predominant use case for consideration but alternate form factors are not prohibited

DC-SCM

- All M-DNO HPM Types enable (but do not require systems to leverage) use of “off the shelf” DC-SCM 2.0
- Mid / Standard Depth systems will *typically* leverage Coplanar DC-SCM
- Short Depth systems will often require alternate implementation such as “floating” DC-SCM

9. HPM Layout Concepts & Definitions

A Note on Board Types:

The M-DNO specification workgroup studied various board configurations, sizes, and system intercepts. As the details matured, changes to the board types defined in draft releases were made for Version 1.0.

- "Type 1" was removed due to lack of clear industry use cases
- "Type 3" is included, however, certain details have been left as "TBD" to allow the workgroup additional time to further study the intended use cases. Included details should be considered directional and may change in a future M-DNO release.
- The initial type referencing by number was not reset for V1.0

In Summary, this specification will provide full detail on Type 2 and Type 4, as well as directional detail on Type 3.

To achieve the goals outlined in **Section 8**, this M-DNO specification defines three different HPM board "Types". Note that the M-DNO specification does NOT mandate CPU / DIMM quantities or define a specific area for CPU and Memory.

Figure 1: M-DNO Board Type Layout Overview

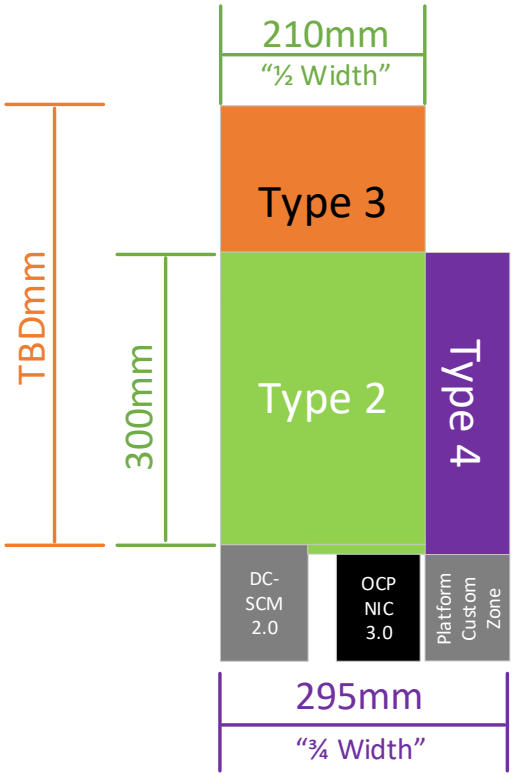
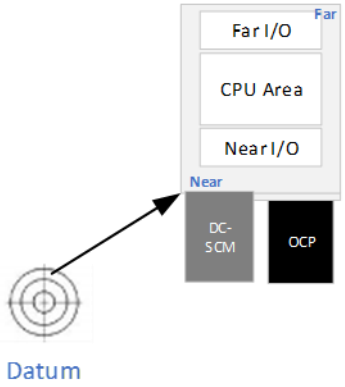


Figure 1 provides a dimensional overview of the three board types, additional definitions and concepts are described below:

1. Due to the wide array of potential HPM and Chassis configurations, this specification defines a **Near** <<Element>> as the <<Element>> closer to the Datum (0,0 reference) and **Far** <<Element>> as the <<Element>> further from the Datum, examples for <<Element>> include:
    a. Corner
    b. Edge
    c. I/O Zone

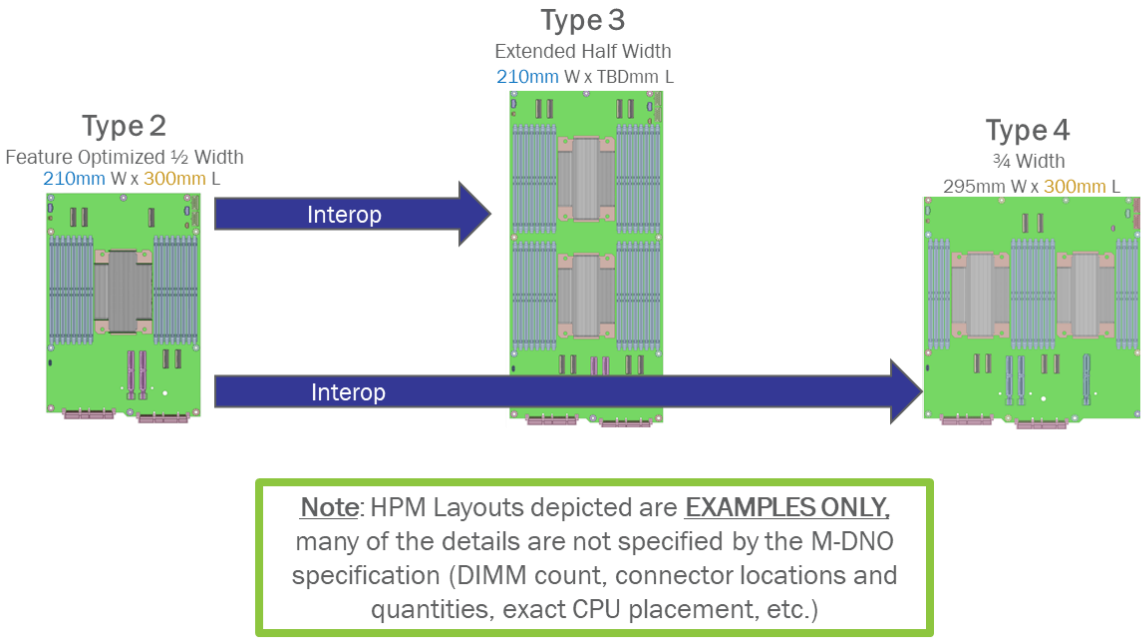
    An example of Near and Far terminology usage is shown in **Figure 2**.

Figure 2: Near and Far Terminology Example



2. The location of the DC-SCM and OCP NIC connector on the HPM shall be common across all types relative to the Datum (0,0)
3. "½ Width" refers to the common 210mm HPM width shared by Type 2 and 3
4. "¾ Width" refers to the 295mm HPM width used in Type 4
5. "Full Width" HPMs are outside the scope of this specification and are defined by the M-FLW specification
6. HPMs narrower than ½ Width are also outside the scope of this specification due to the inability of supporting common DCSCM 2.0 and OCP NIC 3.0 connector locations as described in #2. The DC-MHS workgroup may consider narrower HPM designs in the future.
7. The goal of this specification is to provide HPM Interoperability of smaller M-DNO HPM Types in systems designed for larger M-DNO HPM Types with minimal modifications (e.g. board pan or I/O cable changes), as depicted in **Figure 3**:
    a. Type 2 HPMs can be easily leveraged into systems which support Type 3 HPMs
    b. Type 2 HPMs can be easily leveraged into systems which support Type 4 HPMs
    c. These goals do NOT apply between M-DNO and M-FLW HPMs

Figure 3: M-DNO Type Interop Goals



Note: HPM Layouts depicted are EXAMPLES ONLY, many of the details are not specified by the M-DNO specification (DIMM count, connector locations and quantities, exact CPU placement, etc.)

10. Mechanical

In addition to the drawings and details within this document, DFX/CAD files will be provided for further detail.

Unless otherwise specified all units are in mm.

Unless otherwise specified, PCB dimensions shown in this specification shall comply to the following table. Note: This table is preliminary for V0.9 and subject to change for V1.0.

Table 2: Standard Tolerances (preliminary)

Dimension Type	Tolerance, unless otherwise specified
Drilled hole (origin) to round fiducial	+/- 0.076mm (+/- 0.003 inch)
Drilled hole (origin) to profiled card edge	+/- 0.254mm (+/- 0.010 inch)
Drilled hole (origin) to drilled hole	+/- 0.127mm (+/- 0.005 inch)
Profiled card edge to profiled card edge	+/- 0.127mm (+/- 0.005 inch)
Feature of size (hole diameter, slot width, etc.)	+/- 0.100mm (+/- 0.004 inch)
PCB thickness	+/- 10% of nominal

10.1. HPM Outlines

There are 3 M-DNO HPM Type Outlines defined as described in **Section 9**.

The M-DNO Type 2,3 and 4 Outlines are defined in **Figure 4** - **Figure 6** below.

Note that **Figure 4** and **Figure 5** contain unique tolerances when dimensioning the HPM width. These asymmetric width tolerances allow the HPM designer to optionally choose to set the nominal total width slightly narrower if desired for chassis compatibility goals.

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Figure 4: Type 2 HPM Outline

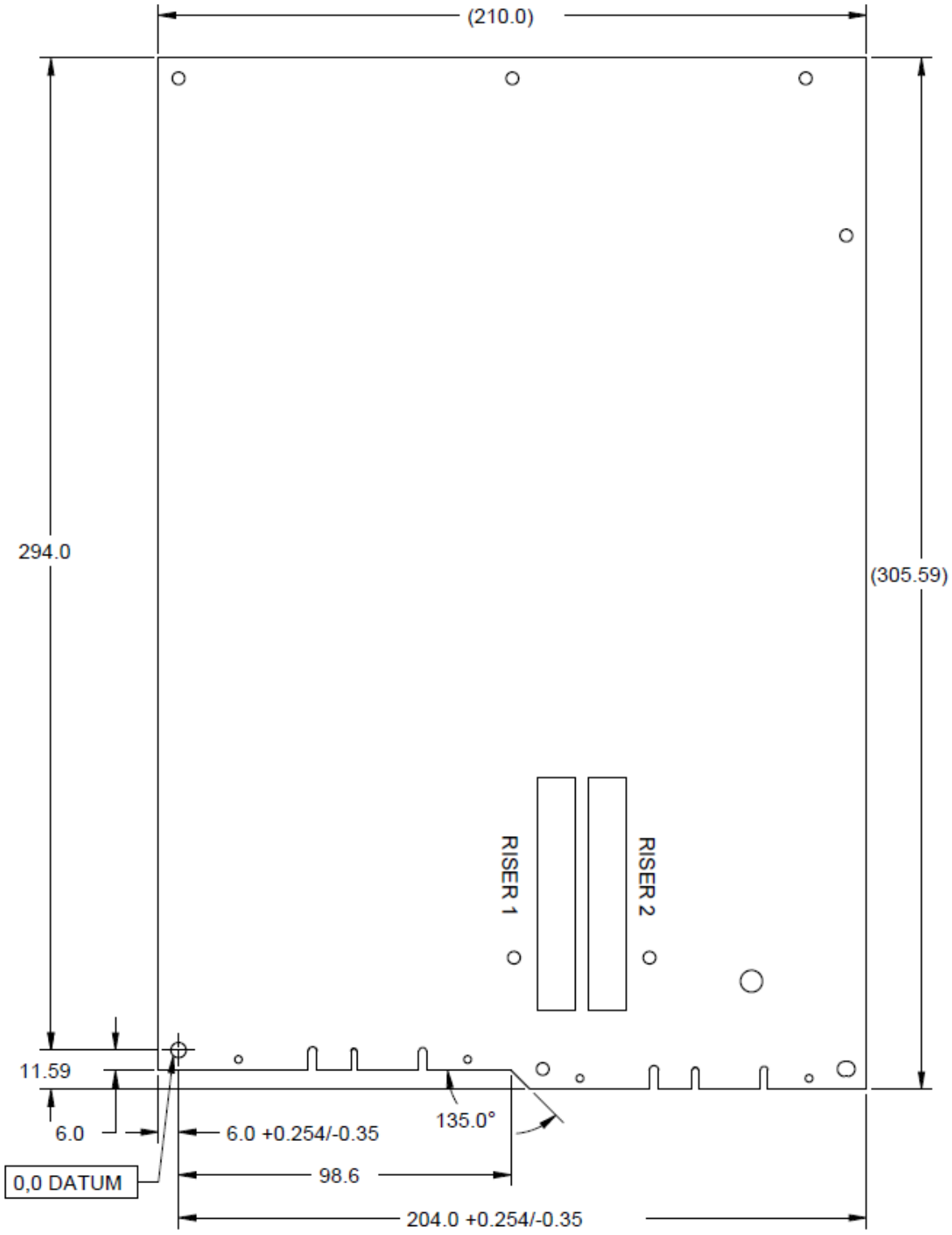


Figure 5: Type 3 HPM Outline

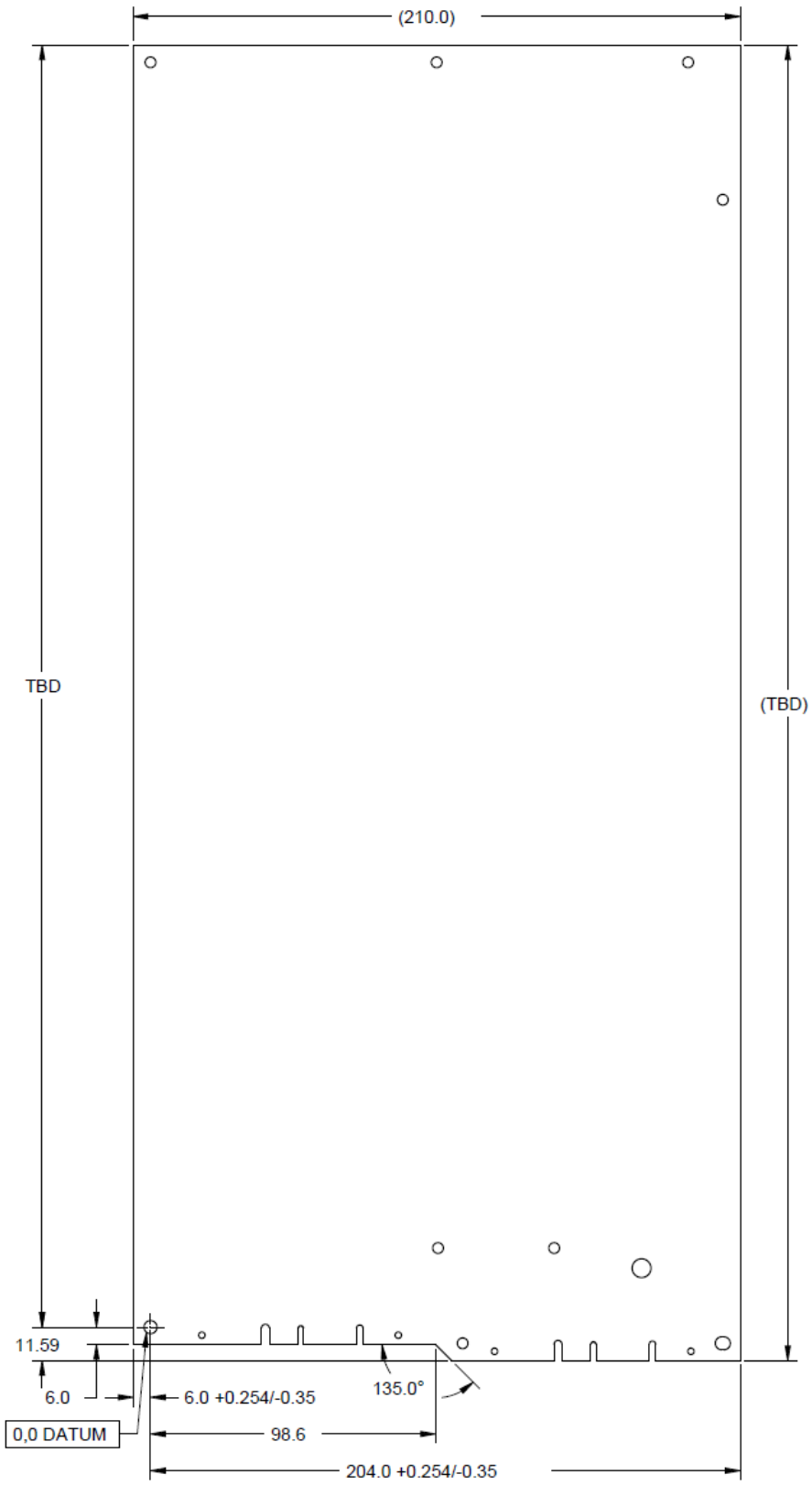
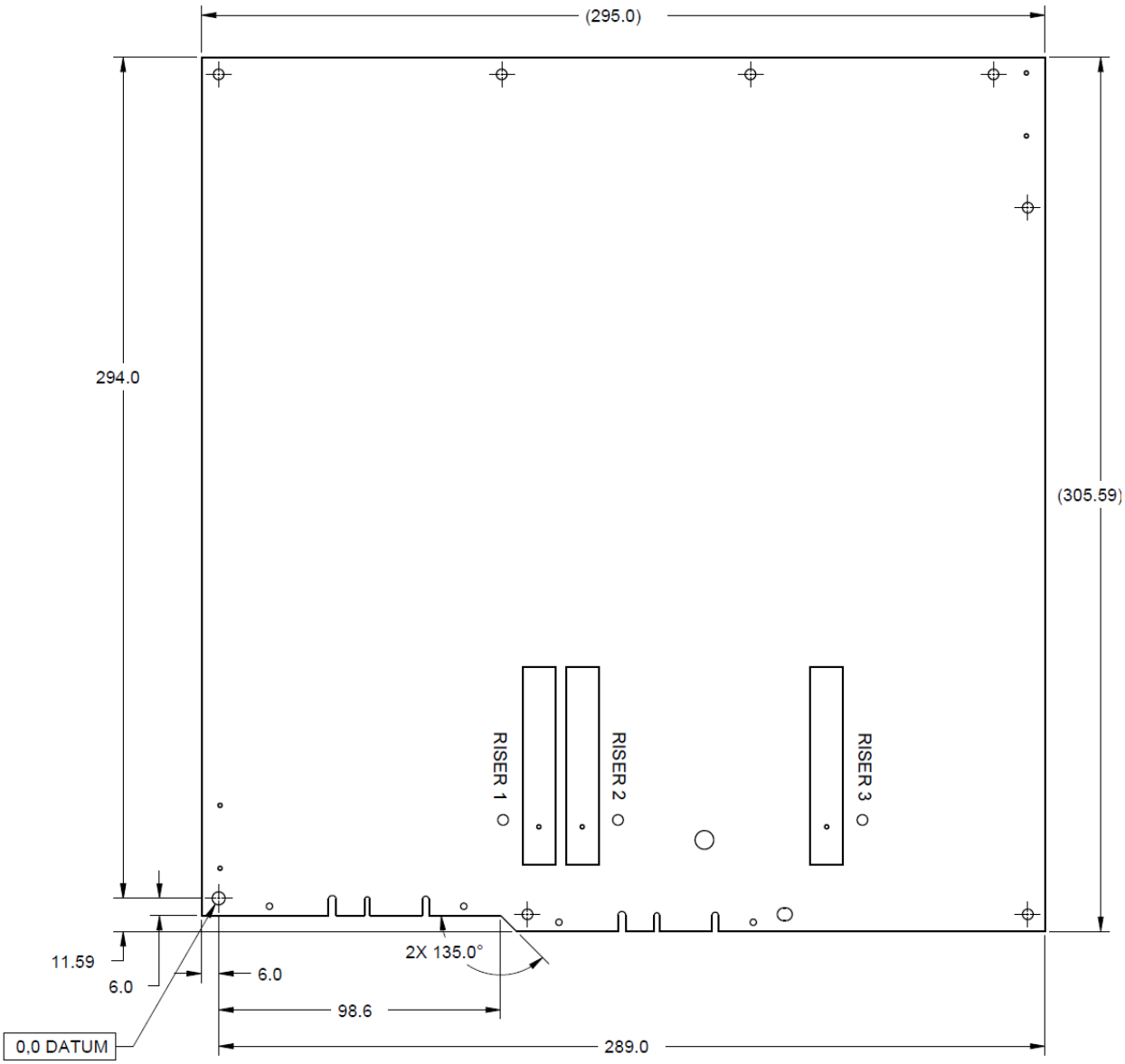


Figure 6: Type 4 HPM Outline



10.2. Board Datum and Mounting Hole Information

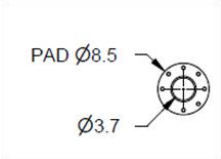
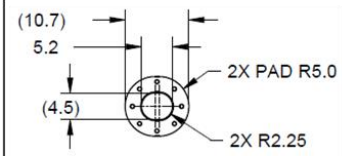
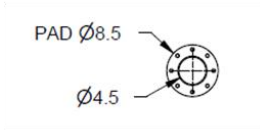
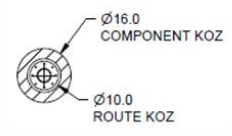
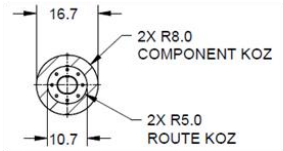
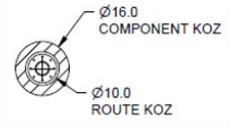
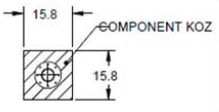
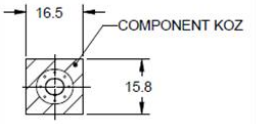
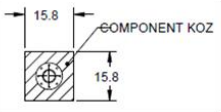
All M-DNO board types leverage a common datum location at the center of the mounting hole in the near corner of the board where the DC-SCM 2.0 connector resides. This allows for fixed elements (riser connectors, peripheral connectors, …) to have a common reference across all board types.

Detailed hole information common to all board types is provided in **Figure 7**.

All holes shall adhere to the specified size, ground pad dimensions, component KOZ and route KOZ.

The component KOZ is intended to keep small components at risk of damage away from the hardware and assembly tools. If a component is larger than 10mm in any dimension (i.e. a DIMM connector), it is considered more robust, and may encroach on the Component KOZ's.

Figure 7: Hole Detail Reference

	DETAIL A Standard Mounting Holes	DETAIL B Unique Alignment Slot	DETAIL C Unique Alignment Hole
Hole and Pad Sizes			
Top Side KOZs			
Bottom Side KOZs			

A set of required board mounting hole locations are specified for the 3 M-DNO HPM Types in **Figure 8-Figure 10**. All dimensioned holes are required.

It is expected that HPM designers will add additional mounting holes based on their HPM layout. All additional holes should adhere to Standard Mounting Hole requirements (Detail A in **Figure 7**).

It is recommended that HPM designers include a hole adjacent to the Far power zone, an example is depicted but not dimensioned.

Implementors Note:

The PCB Datum hole (Detail C) is defined such that a collared standoff with tight tolerance fit can be used to control X-Y tolerances in HPM mounting. Additionally, a slotted hole (Detail B) is defined to control rotation around the datum, by allowing, as an example, a collared standoff to be used with tight fit to the top/bottom edge of the slot.

All other mounting holes follow standard mounting hole guidance (Detail A). These mounting holes are expected to have clearance fits to screw hardware.

A design should follow good engineering practices in consideration of Platform Shock and Vibration requirements. Shock and Vibration requirements are not in scope of this specification.

Figure 8: Type 2 Mounting Holes

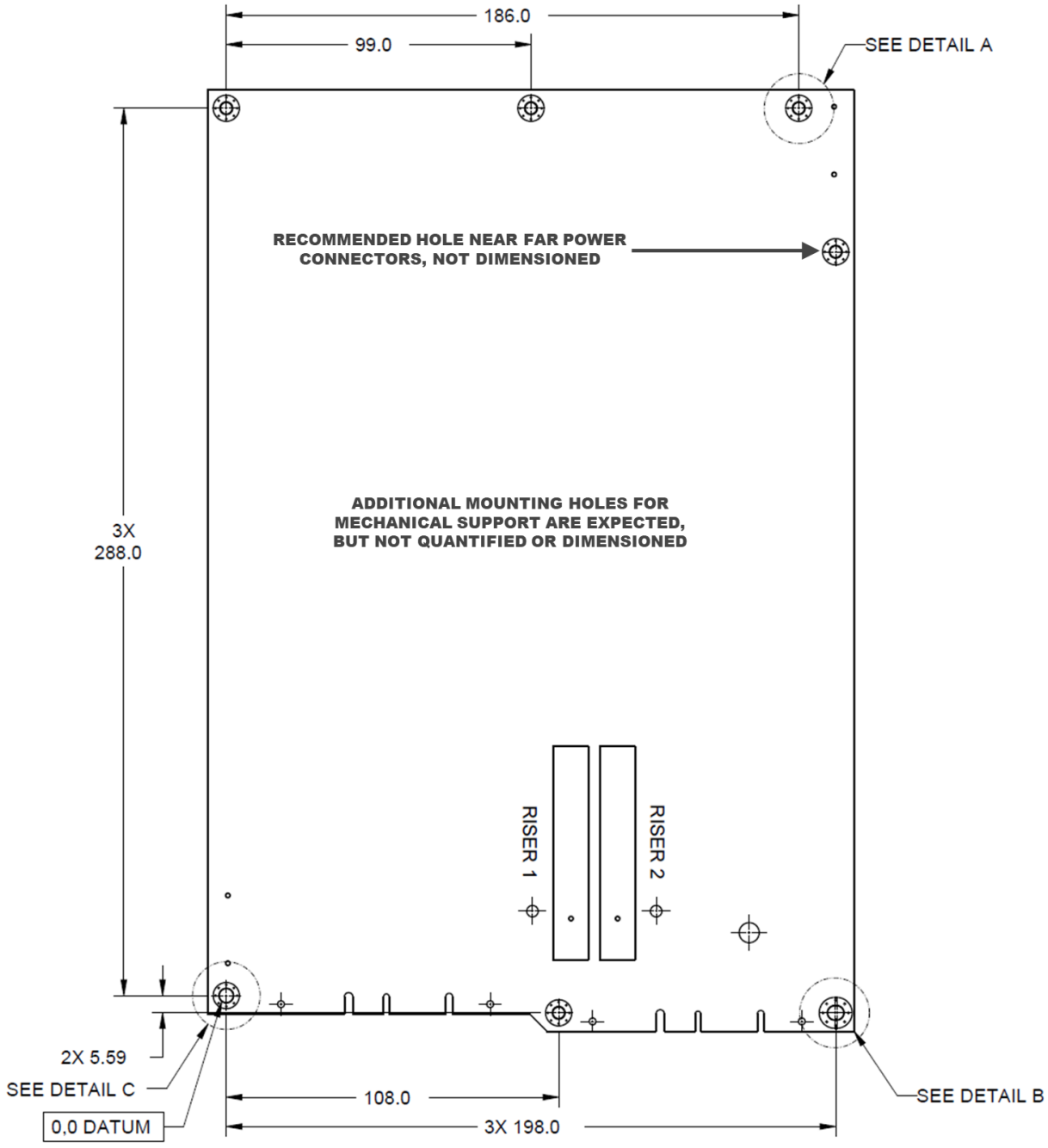


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Figure 9: Type 3 Mounting Holes

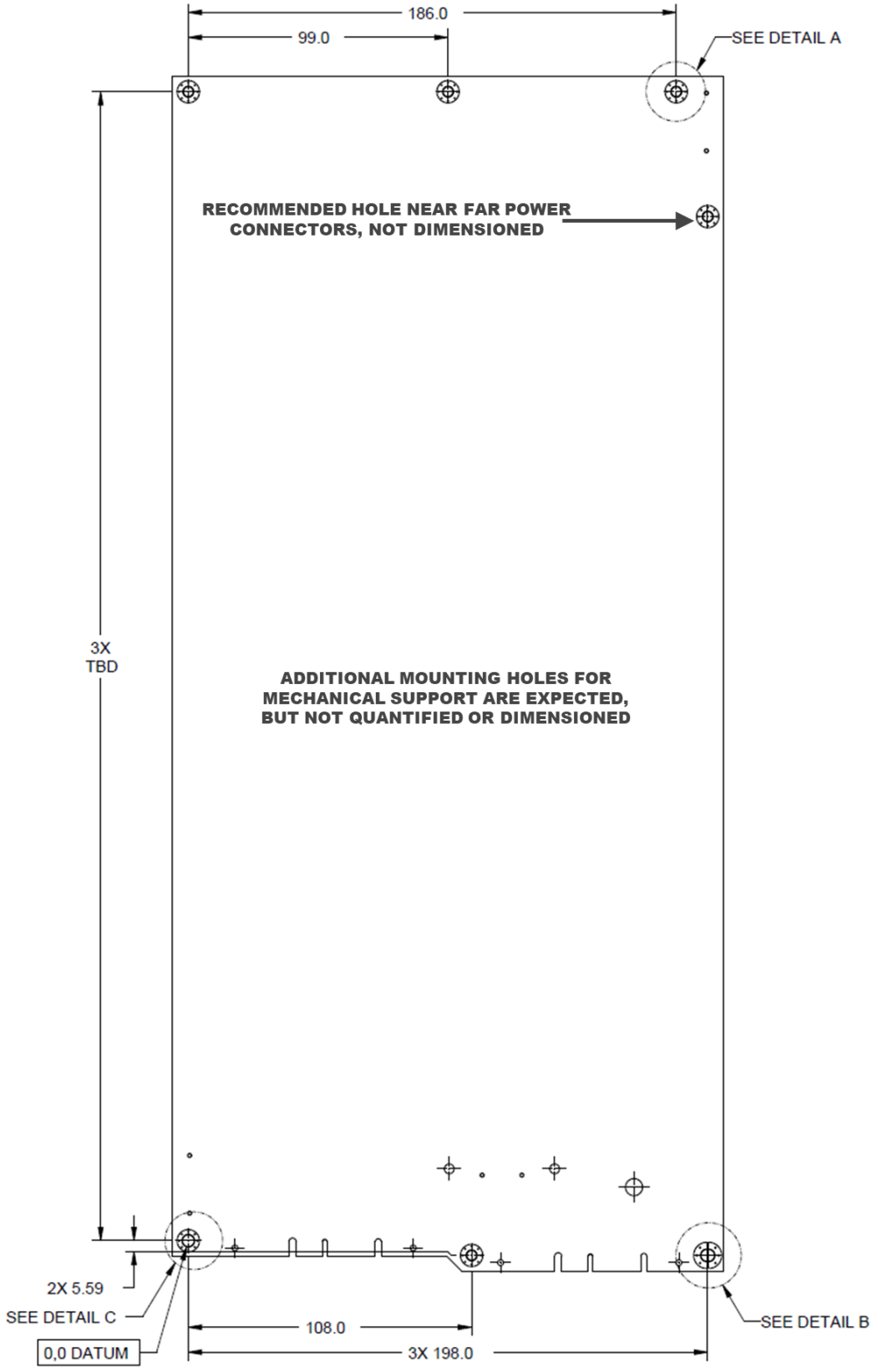
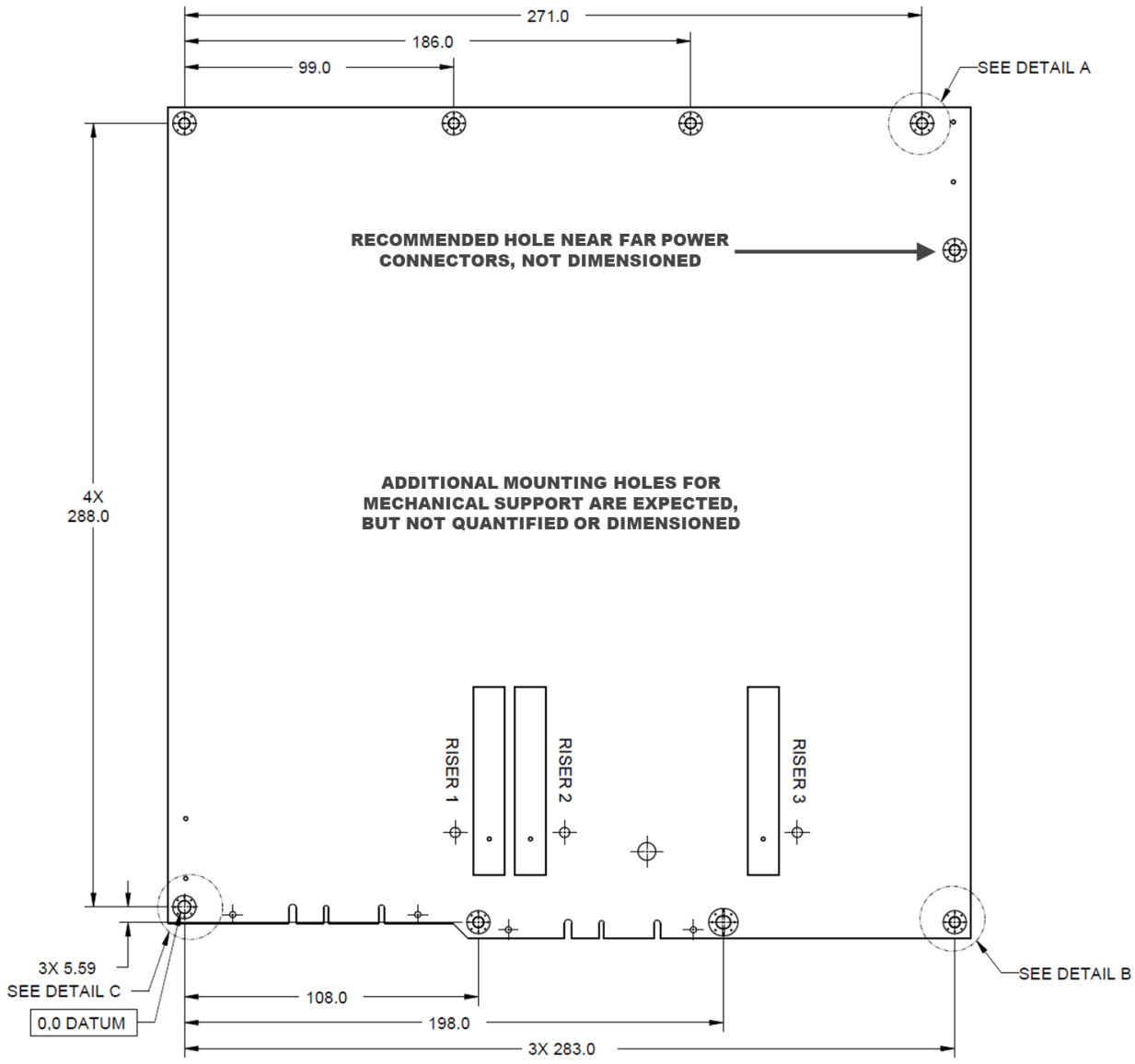


Figure 10: Type 4 Mounting Holes



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10.3. Board Thickness

The maximum board thickness allowed is 3.18mm nominal, assuming +10% max tolerance.

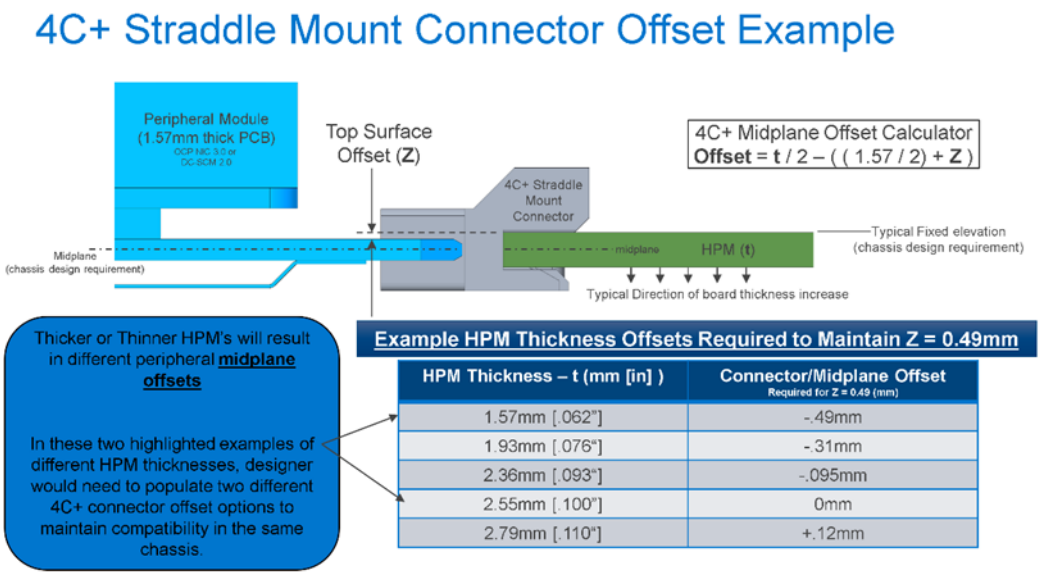
Implementors Note:

Designers should consider that variations in HPM thickness combined with 4C+ connector selection may result in variation of the vertical offset locations of OCP NIC V3 and DC SCM 2.0 peripherals relative to fixed chassis openings and the primary surface of the HPM. There are common connectors in the industry which will result in varying offset locations.

The diagram below demonstrates how selecting the variance of midplane offset within the 4C+ connector can enable a common resulting peripheral offset relative to the primary surface for varying HPM thickness (example offset Z = 0.49).

Note, the host thickness examples shown are common at the time of this specification being published, however, alternate thicknesses may become common in the future.

Designers should consult with vendors of SFF-TA-1002 4C+ to determine best options for their chassis application.



10.4. Assembly Thickness & Secondary Side Zones

The maximum overall thickness of the board assembly, including any insulators and backing plates, is 5.86mm.

These thicknesses are critical to ensure a consistent maximum height for system components (e.g. Riser solutions) across M-DNO HPMs.

There are four distinct Zones on the secondary side of the HPM as depicted in **Figure 11**. Each zone serves a unique purpose.

Figure 11: Secondary Side Zone Definitions

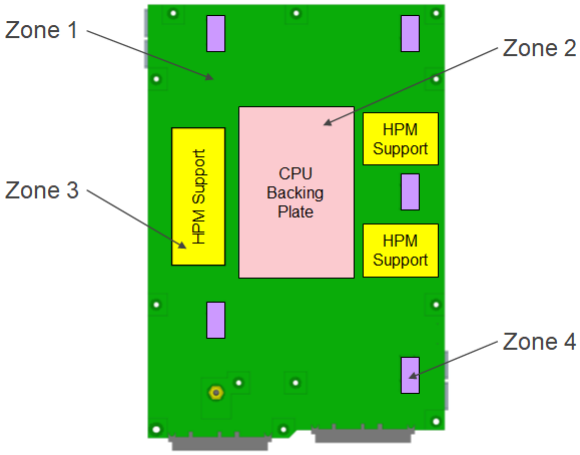


Table 3 details an **example** scenario stack-up based on the Critical MAX HPM assembly thickness.

Table 3: Max Thickness Example Z-Height Stack-Up, Per Zone

		Zone 1	Zone 2	Zone 3	Zone 4	
Item	**Description**	**Z Value (mm)**	**Z Value (mm)**	**Z Value (mm)**	**Z Value (mm)**	**Notes**
A	HPM	3.18	3.18	3.18	3.18	MAX Thickness (w/o Added tolerance, Assumes secondary mounting)
B	Secondary Component Z	1.60			0	MAX Height
C	CPU Backing Plate		2.60			MAX Thickness Backplate for MAX Thickness HPM, Hole in Pan/Tray
D	HPM Secondary Support			1.78		HPM Support Thickness +/- 0.10mm, must exceed secondary Component Z
E	Gap	0.28	0.08	0.10	0.58	Zone 2 & Zone 3 gap is small because contact is permissible/desired
F	Board Pan	0.80		0.80		
G	Chassis Hook				2.10	MAX Height from Inside Surface of Chassis
	TOTAL	5.86	5.86	5.86	5.86	

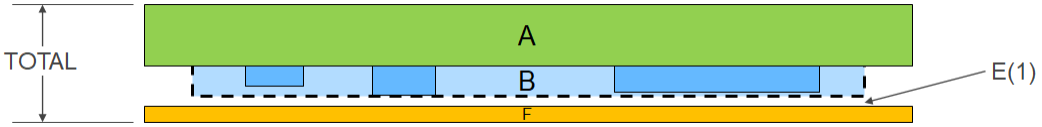
Note that the “total Z” value across the 4 zones must always be equivalent (5.86mm shown for example only).

Note that while the above scenario describes a board pan, the same maximum thicknesses apply to a chassis with no board pan (e.g. a sled based solution).

10.4.1. Secondary Side Components (Zone 1)

There is a required universal secondary side component height restriction of 1.6mm for all board types represented by area ‘B’ in **Figure 12** (refer to **Table 3** for all item descriptions).

Figure 12: Secondary Side Components (Zone 1)

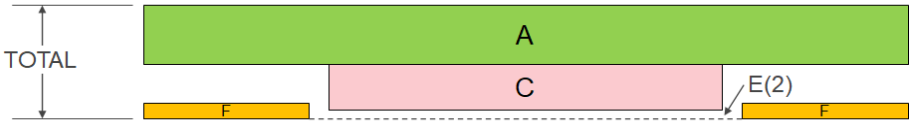


10.4.2. CPU Backing Plate Example (Zone 2)

Most server HPM designs need to support CPU backing plates or stiffeners placed under the CPU as part of the CPU Socket design.

Backing plates are assumed to be allowed to protrude into cuts in the Chassis-to-Board bracketry and / or HPM sled as represented by area 'C' in **Figure 13** (refer to **Table 3** for all item descriptions).

Figure 13: CPU Backing Plate (Zone 2)



10.4.3. HPM Secondary Support (Zone 3)

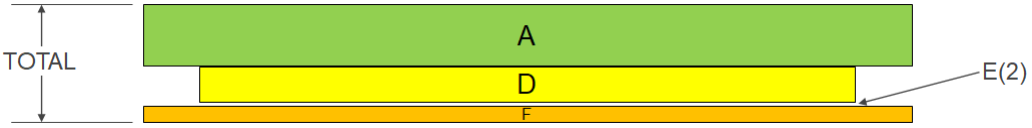
To ensure maximum flexibility of HPM primary side layouts, secondary supports need to be incorporated under the DIMM Sockets and / or any other area of the HPM needing extra vertical compression support. These supports help prevent the board from flexing during assembly, when downward forces are applied to the HPM from the primary side.

HPM Secondary Supports shall be 1.78mm +/- 0.10mm thick. They are designed to be close to the board pan or chassis, and provide a vertical deflection stop for the HPM. The materials used and methods for support are the choice of the HPM Designer.

This support height creates a common reference surface that Chassis Designers can rely on that is taller than the Secondary Component Z-Height MAX of 1.6mm.

Secondary supports are represented by area 'D' in **Figure 14** (refer to **Table 3** for all item descriptions).

Figure 14: HPM Secondary Support (Zone 3)



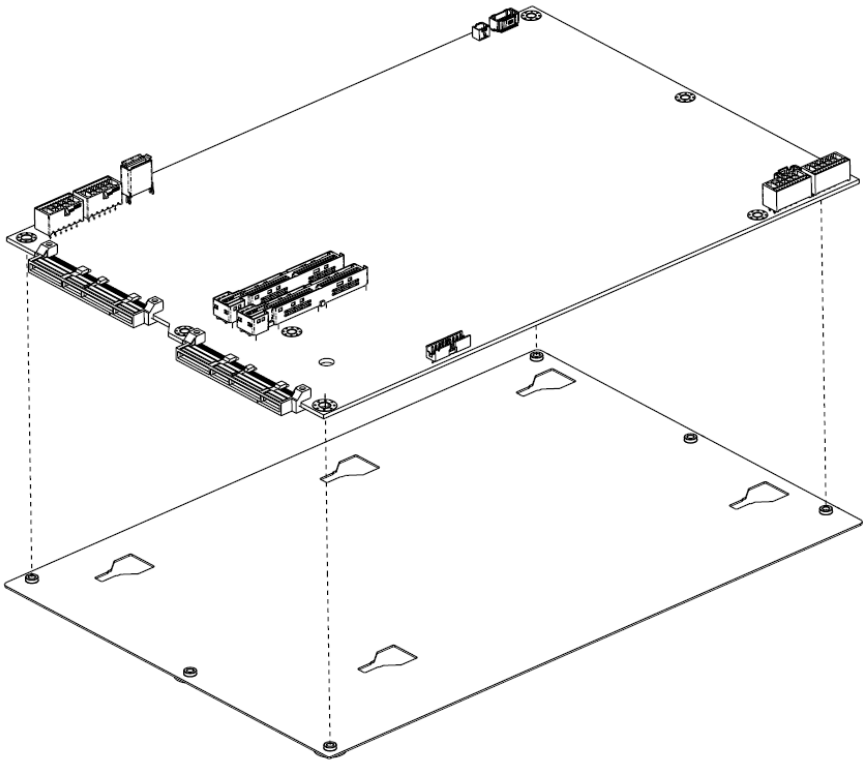
Implementors Note:

If an HPM Designer and a Chassis Designer agree to transfer this responsibility for HPM Support, and the HPM Designer provides all the appropriate PCB Keepouts and Guidance necessary to relocate these supports into the Chassis Design, then it will be permissible to remove these supplemental supports from the finished HPM PCB Assembly.

10.4.4. Chassis Hook Keepouts (Zone 4)

M-DNO HPMs shall allow for a Chassis-to-Board Bracket (Board Pan) which enables different board layouts (and mounting hole locations) between HPM Types and Compute Core designs, while maintaining compatibility to a common chassis. An example Board Pan is shown in **Figure 15**. These board pans typically require a Chassis Hook feature that intrudes into the Secondary Side Component space, resulting in a Chassis Hook Keepout on the HPM.

Figure 15: Example of Chassis-to-Board Bracket (Board Pan)



Implementors Note:

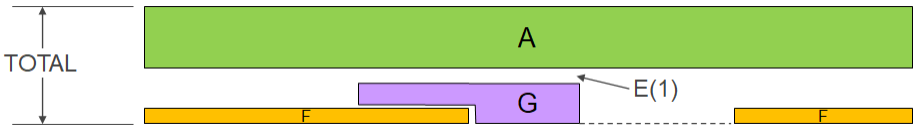
While most monolithic server designs benefit from a Board Pan, it is NOT expected that all systems supporting M-DNO HPMs will require a Board Pan. Specifically, sled-based designs common in multi-node systems typically do not require a board pan.

M-DNO HPMs shall support required locations for chassis hook features that interface between the chassis base and the Chassis-to-Board Bracket; these hook features are represented by area 'G' in **Figure 16** (refer to **Table 3** for all item descriptions).

A supporting chassis base must provide hook geometry to interface the cutouts on the Chassis to Board Bracket.

The geometry of the Board Bracket is not specified.

Figure 16: Chassis Hook Keepouts (Zone 4)



The zero-height secondary side keep out zones for Board Pan support are defined in **Figure 17-Figure 19**.

Connectors and/or sockets may be placed over the Chassis Hook Keepouts on the Primary Side of the HPM. The maximum length of a connector's Alignment Post or Retention Barb for such connectors is 3.20mm MAX.

This length guidance is for Non-Conductive Alignment Posts or Grounded Retention Barbs. Through Hole leads for Power and Signal pins are not permitted in the Chassis Hook Keepout Zones.

Implementors Note:

Alignment Posts and Retention Barbs of connectors that protrude through the HPM can impact an HPM design's ability to be compliant with the Chassis Hook Keepout Zones.

The HPM Designer should choose connector variants with Alignment and Retention features that do not protrude through the secondary side of the HPM to avoid any potential collision with Chassis Hooks during system assembly.

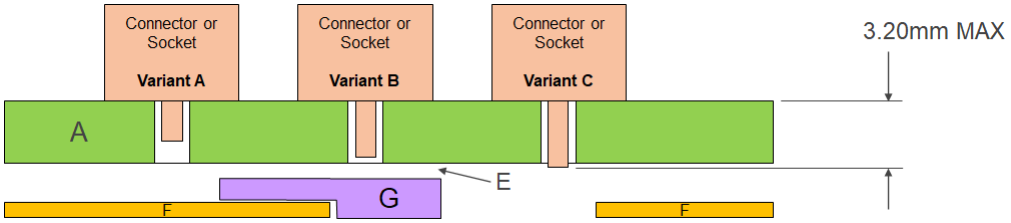


Figure 17: Type 2 HPM Secondary Side Chassis Hook Locations

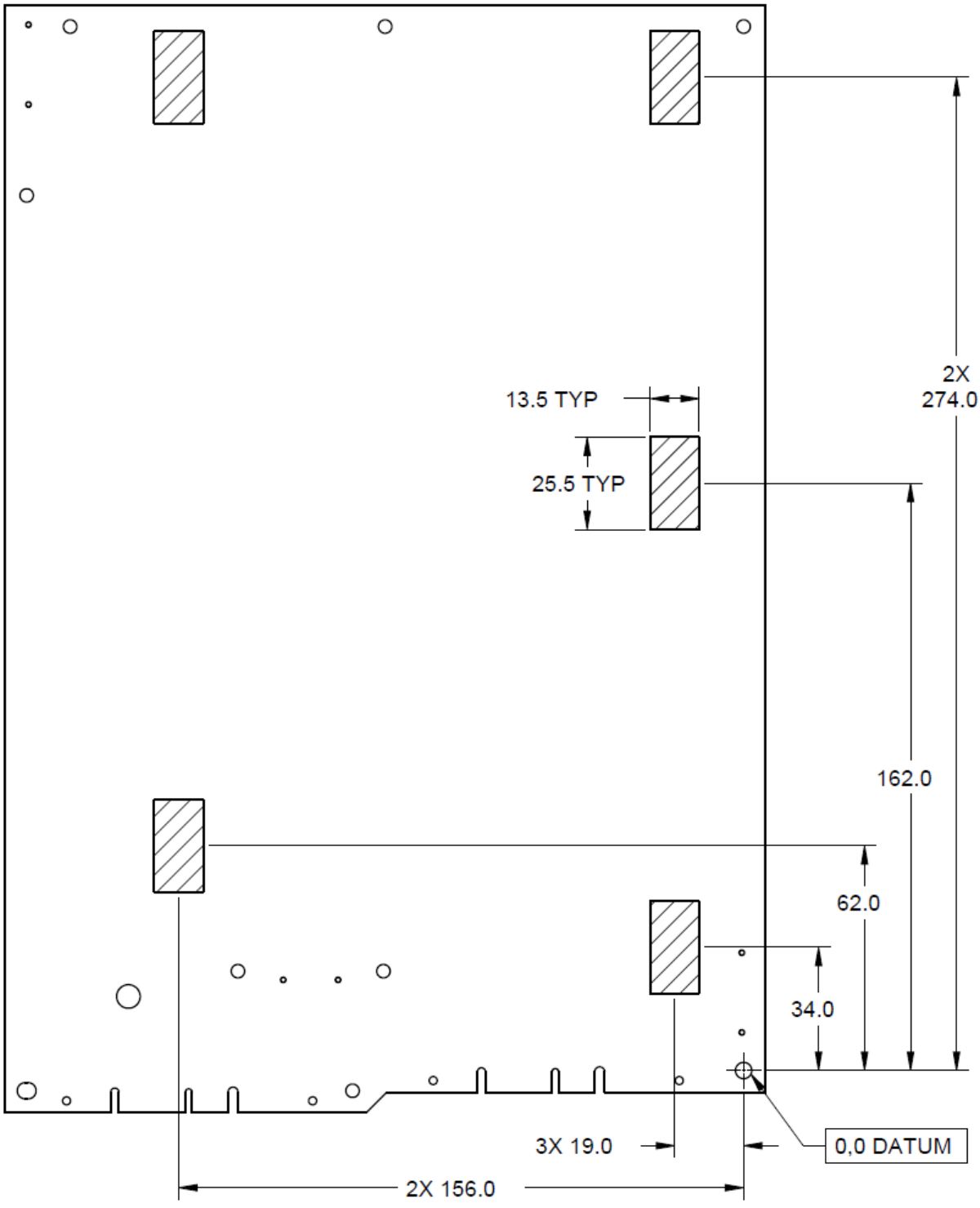


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Figure 18: Type 3 HPM Secondary Side Chassis Hook Locations

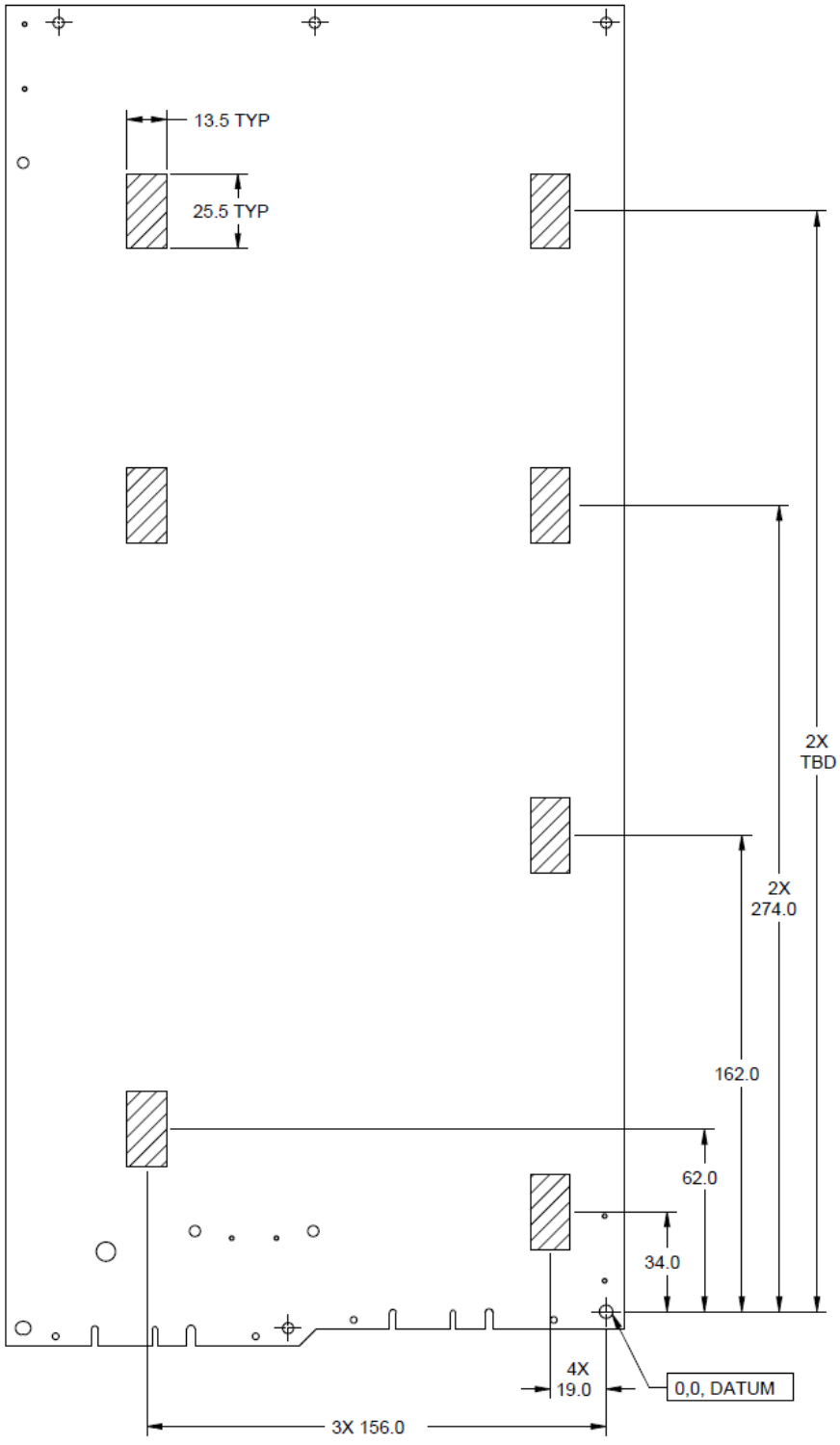
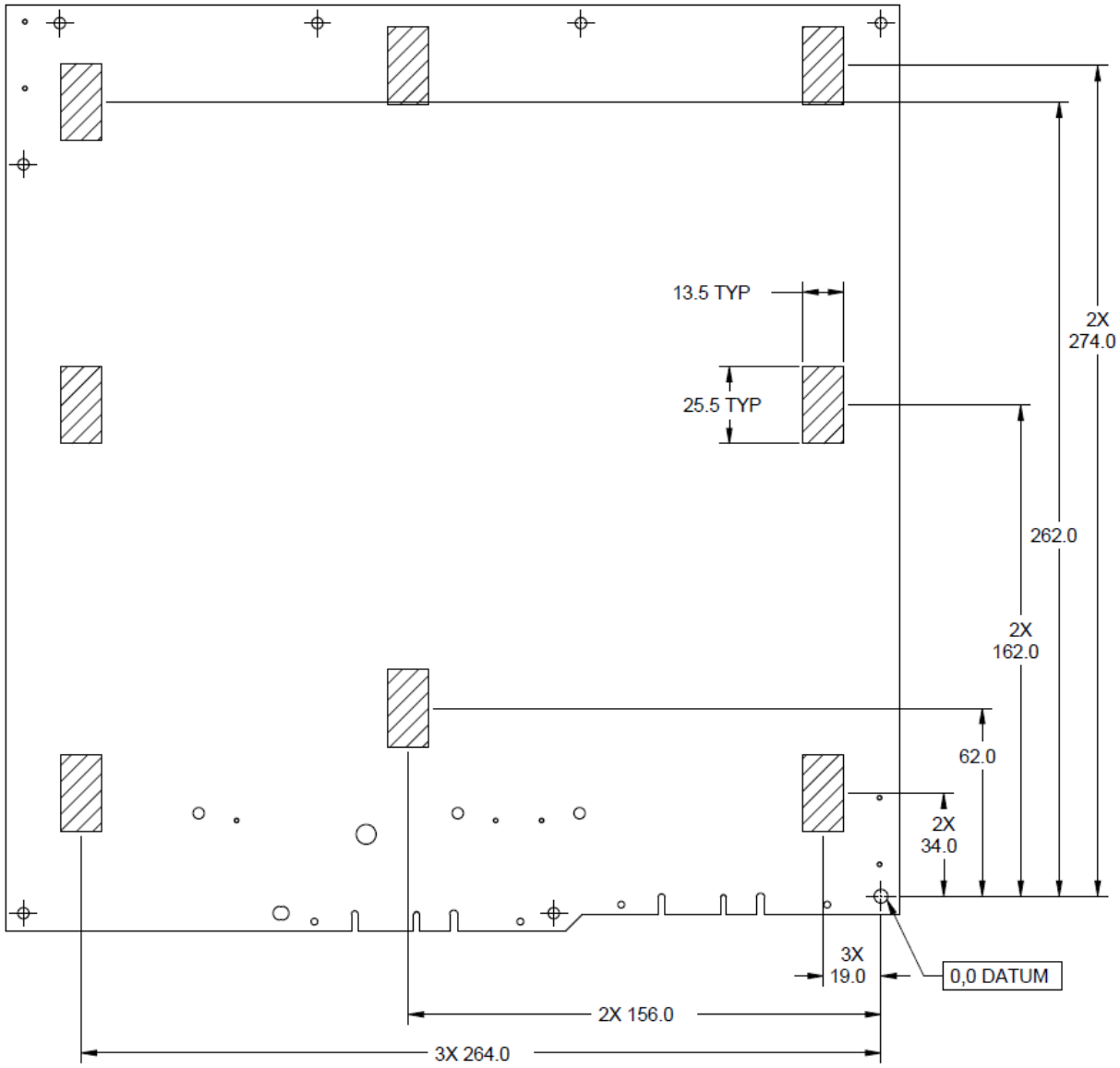


Figure 19: Type 4 HPM Secondary Side Chassis Hook Locations



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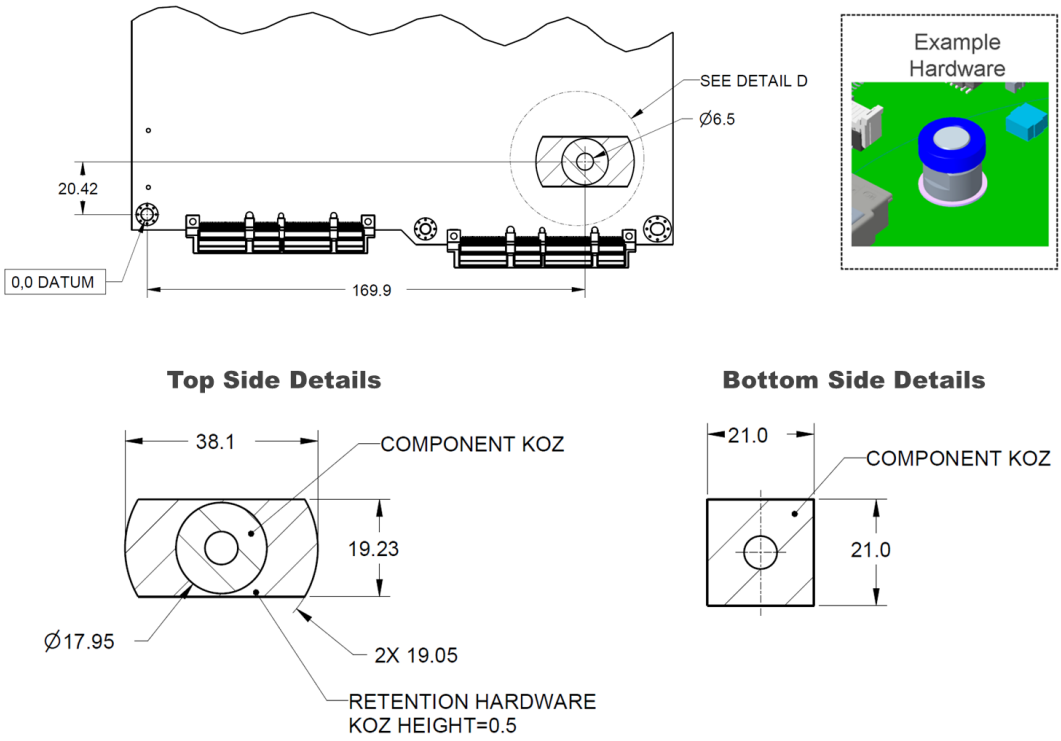
10.5. HPM to Chassis Retention Mounting

The HPM and Chassis-to-Board Bracket assembly requires retention to the chassis base. There shall be a hole required for motherboard retention to the chassis. The hole is sized for common retention methods such as plungers, thumbscrews, etc. Required Primary / Secondary
570 side KOZs and height restrictions around this hole are also depicted in **Figure 20.**

Note: The M-DNO workgroup is considering reducing the size or height restriction of the top side detail shown in **Figure 20** in the V1.0 release.in order to ease board placements.

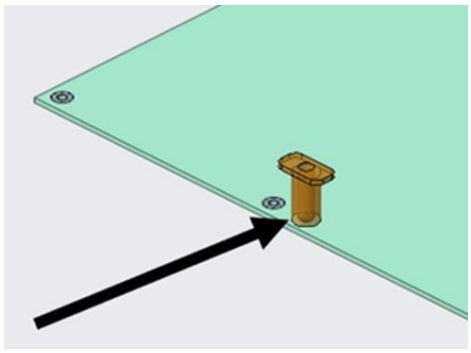
Figure 20: HPM Assembly to Chassis Retention Enablement



10.6. HPM Handle Hole

The HPM shall require a hole interface to a mechanical handle. This handle solution may be implemented with, but is not limited to, a plastic handle. An example is shown in **Figure 21**.

Figure 21: Example Board Handling Feature



Implementors Note:

While the hole is required, HPM and / or System designers may choose to not utilize hardware in the hole location and instead provide alternate solutions to assist in board handling. As an example, if the hole location is not accessible when large thermal solutions are installed the designer may instead choose to provide a handling feature / touch point not tied to the HPM itself.

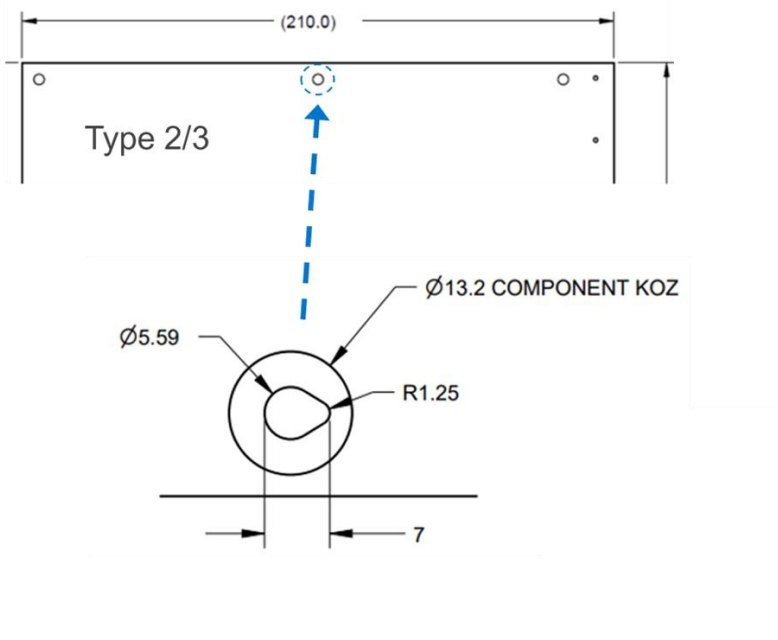
The hole location shall be near the Far side edge of the HPM. HPM Designers may choose to either:

1. Replace a required mid-board mounting hole along the Far Side edge (1 hole choice on Type 2 / Type 3, 2 hole choices on Type 4) with the board handle hole. **Figure 22** demonstrates this using a Type 2/3 board for example purposes.
   OR
2. Add an additional hole near the Far Side Edge with consideration for Compute Core Details such as cabling for HSIO.

The Board Handle hole may also be considered a mounting hole for structural purposes. For example, a designer does NOT need to place a board mounting hole in close proximity to the Board Handle Hole.

The board handle hole shall follow the required dimensions and KOZ in **Figure 22**.

Figure 22: Geometry and KOZ for HPM Handle Hole and Optional Placement Location



10.7. Common Peripheral Location Requirements

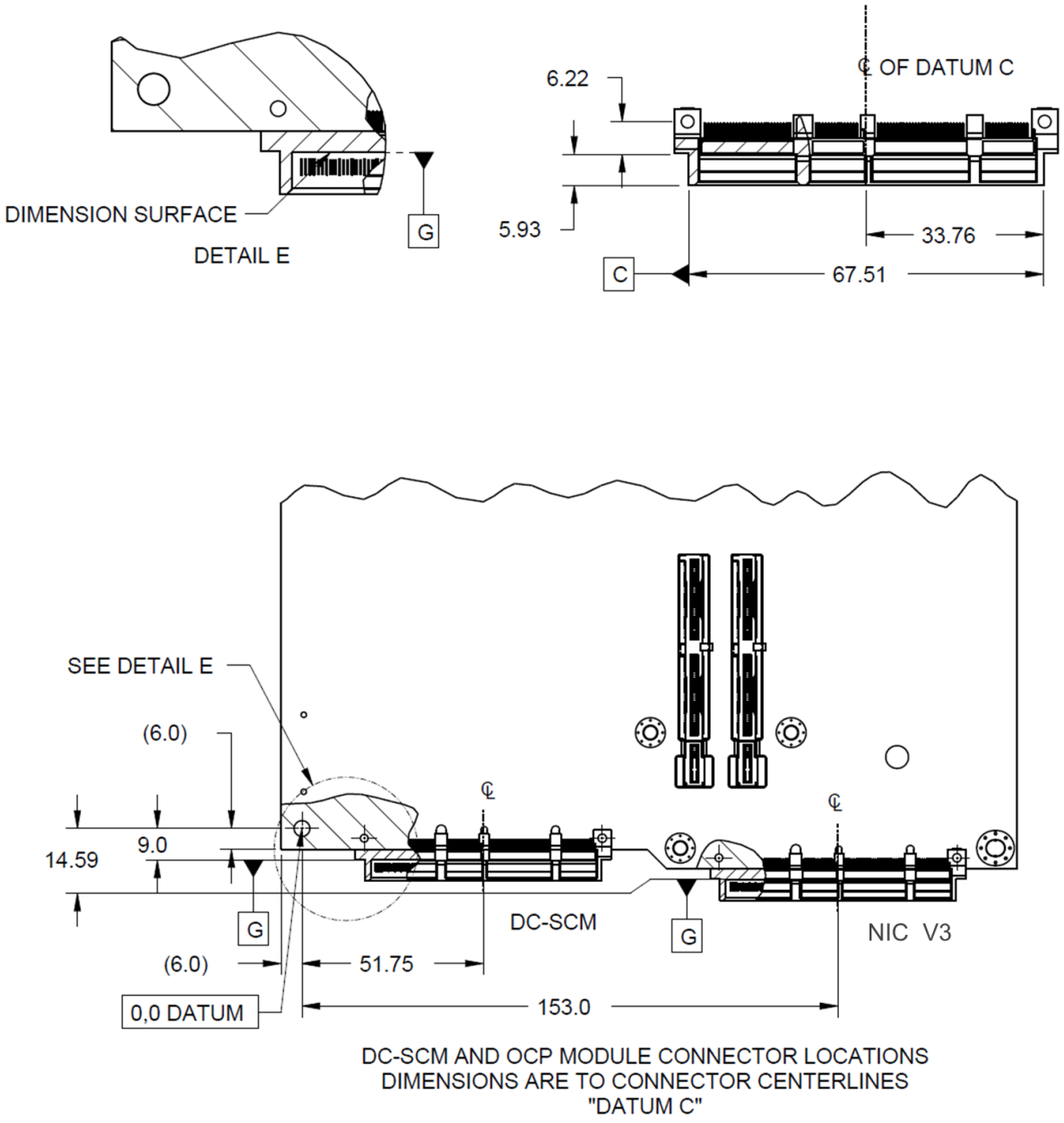
This specification defines fixed placement for certain peripheral connectors to maximize reuse across designs.

These fixed peripheral subsystem connectors are:

- OCP NIC 3.0
- DC-SCM 2.0

The location of each of the connectors is defined in **Figure 23**.

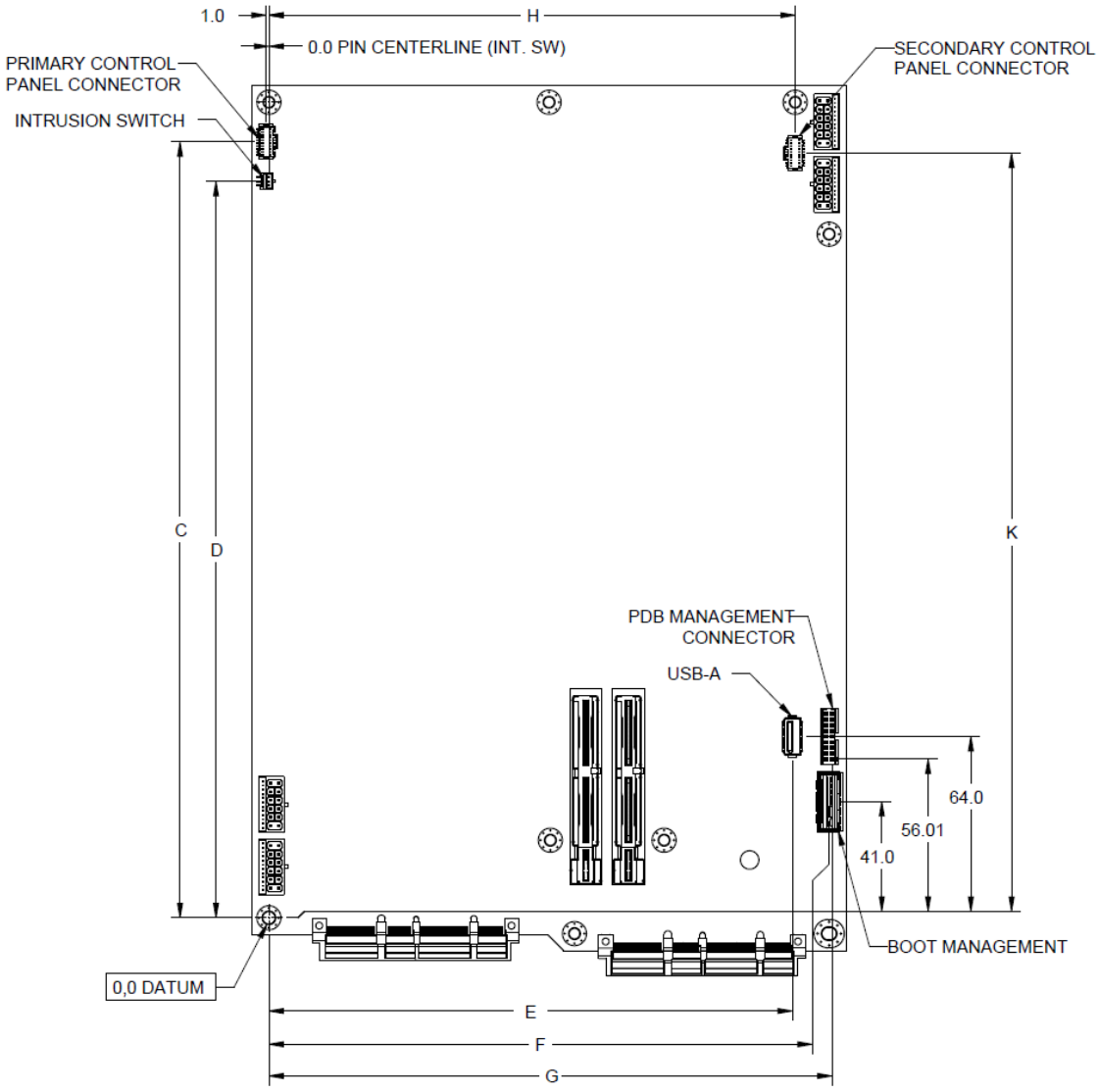
Figure 23: Locations of OCP NIC 3.0 and DC-SCM 2.0



DC-SCM AND OCP MODULE CONNECTOR LOCATIONS
DIMENSIONS ARE TO CONNECTOR CENTERLINES
"DATUM C"

10.8. Platform Infrastructure Connector Placement

610 ***Figure 24: Platform Infrastructure Connector Recommended Placements***



MISCELLANEOUS CONNECTORS							
	DIMENSION						
	C	D	E	F	G	H	K
TYPE	MID	MID	MID	MID	PIN 1	MID	MID
2	274	260	185	198	200	186	270
3	TBD	TBD	185	198	200	186	TBD
4	274	260	270	283	285	285	270

Figure 24 depicts the recommended location of the miscellaneous connectors defined in the M-PIC specification which are relevant to M-DNO HPMs. Additional information on these connectors is available in Section 12.2 – Section 12.6 of this document.

615 Note that a Type 2 board is represented but applicable dimensions are provided for all board types. These dimensions are intended to provide recommended connector locations that are consistent relative to the nearest board corner across all board types.

To ease board layouts while maintaining interoperability, placement zones are specified in **Figure 25** and **Figure 26** that connectors may move within if they cannot be placed in the recommended location. Placement of these connectors shall always be within the specified zone.

Figure 25: Intrusion, Control Panel, USB and PDB Management Placement Zones

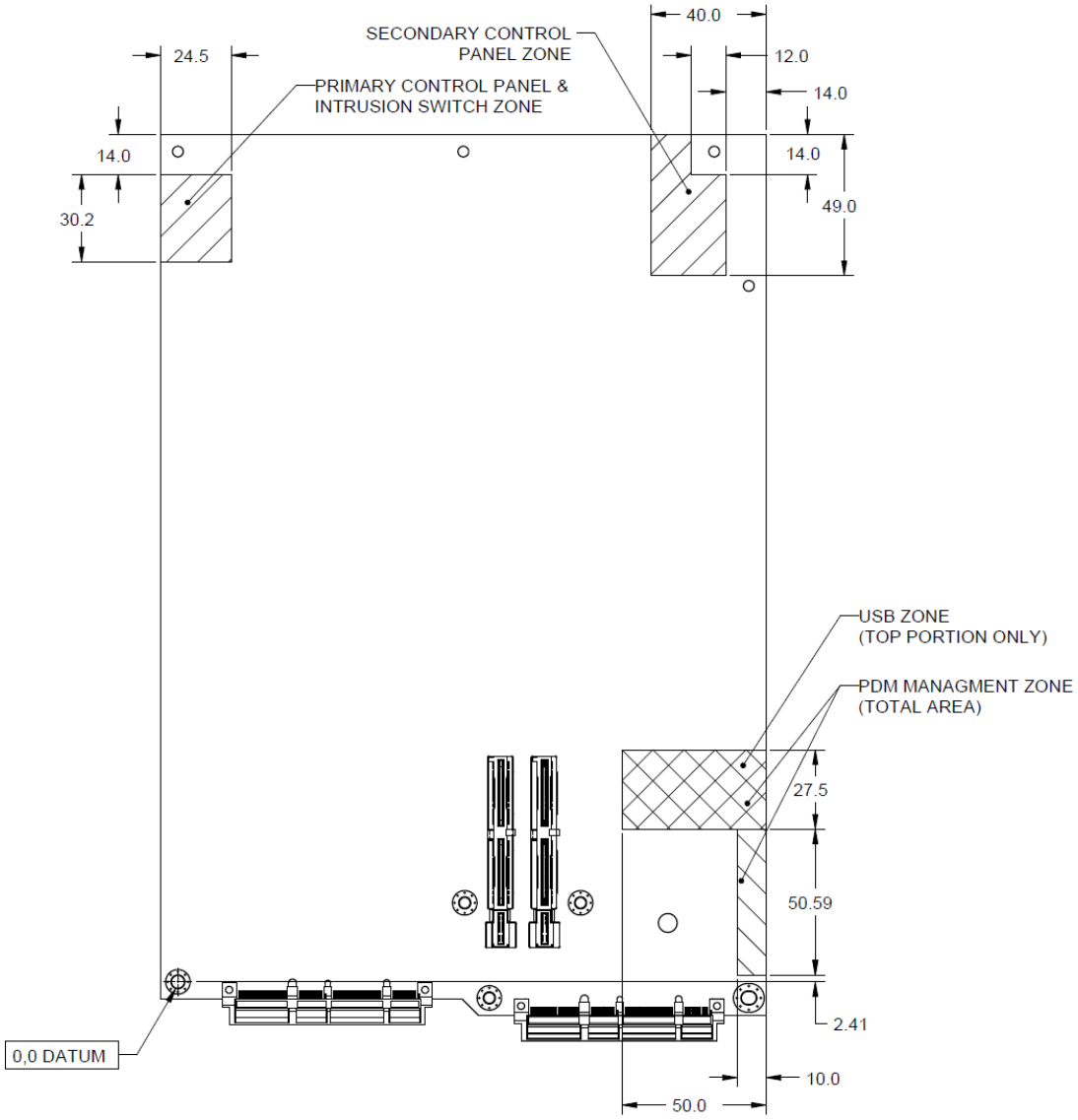
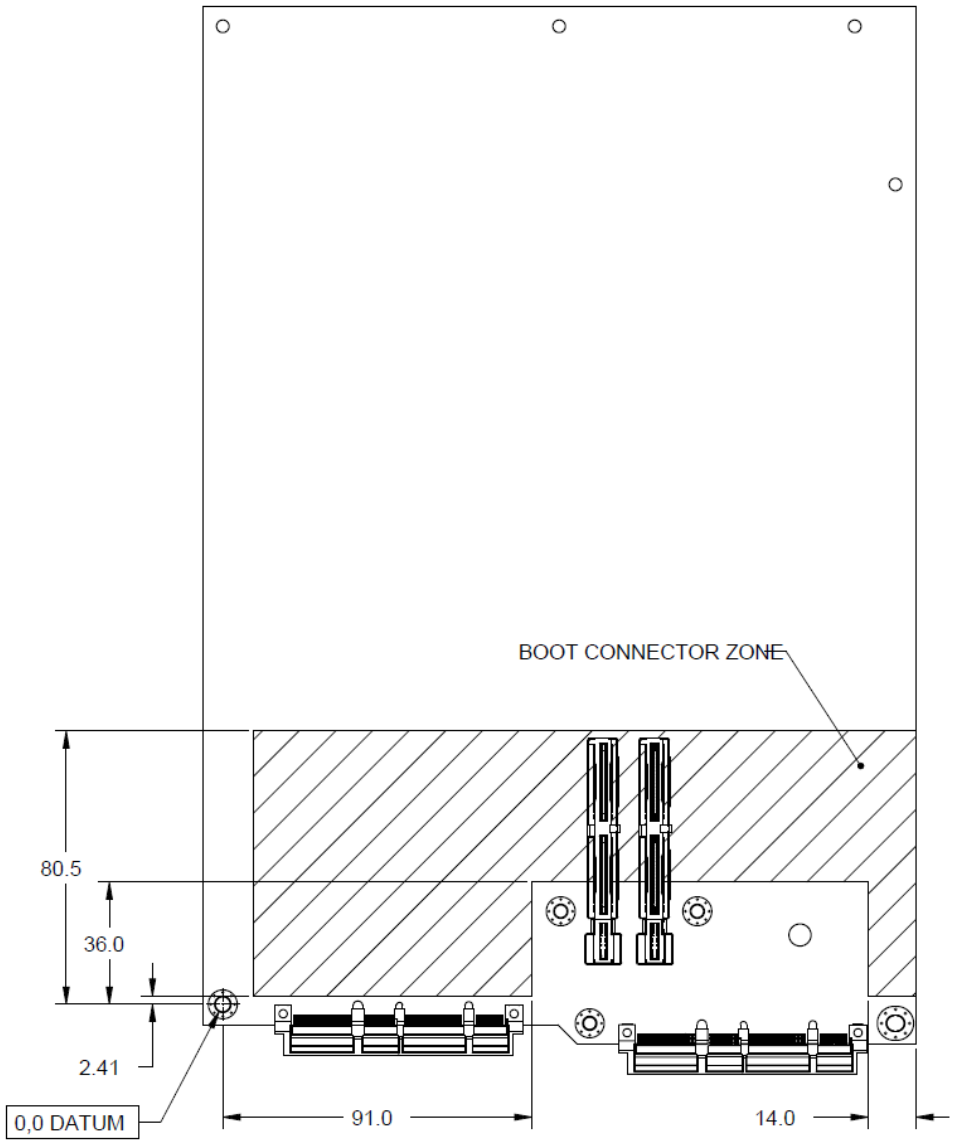


Figure 26: Boot Placement Zones



10.9. Near IO Connector Placement

The M-DNO specification defines multiple HPM Type outlines which support different fixed riser configurations. In addition to any fixed riser implementation(s), cabled high speed I/O (HSIO) connectors may also be placed on the near side of the HPM.

10.9.1. Cabled Near IO Connectors

If cabled HSIO connectors are implemented, it is recommended to use the connector(s) defined in **Section 12.1** with signaling defined by the M-XIO specification.

10.9.2. **Fixed Riser Connectors**

To enable chassis and I/O subsystem reuse, three fixed riser locations are defined

- ½ Width M-DNO HPM Types (2/3) support Riser locations 1 and 2
- ¾ Width Types (4) also support Riser location 3.
- Implementation of each riser location is **optional** across all M-DNO board Types.
- HPMs which implement fixed risers shall do so in any / all of the three specified locations
- Utilization of the connector described in **Section 12.1** is strongly recommended

Figure 27 dimensions the recommended riser connector in the appropriate (required) locations

While utilization of the recommended connector is encouraged, alternate riser connectors are permitted but shall adhere to the following rules as dimensioned in **Figure 28** and summarized in **Table 4**:

1. Connector locations are fixed horizontally (X – direction)
    a. The 'X' dimensions in **Figure 28** indicate riser centerlines. If a chosen connector centerline is offset from the riser centerline, the designer shall adjust the connector location to accomplish the defined Riser centerline.
2. Connector locations are fixed vertically (Y – direction)
    a. The dimensioned locations in **Figure 28** represent riser connector 'Y' length keep in zones
    b. Riser connectors shall not exceed the specified keep in zone
    c. The riser connector shall be oriented such that it touches the near edge within the keep in zone (11.65mm reference from datum)

Note: Requirement 2c is intended to force a fixed placement for a given riser connector across HPMs from different designers to enable reuse of risers and other system elements.

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Figure 27: Required Riser Locations with Recommended Connector

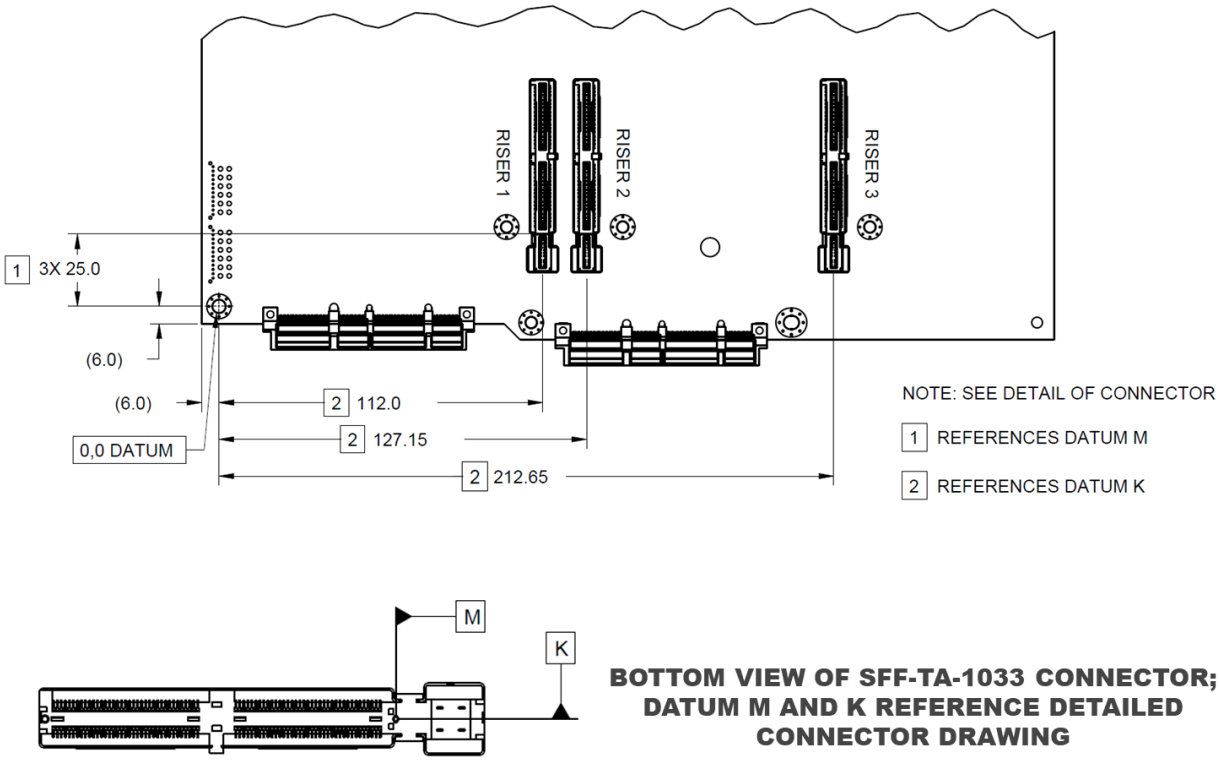


Figure 28: Fixed Riser Location and Numbering

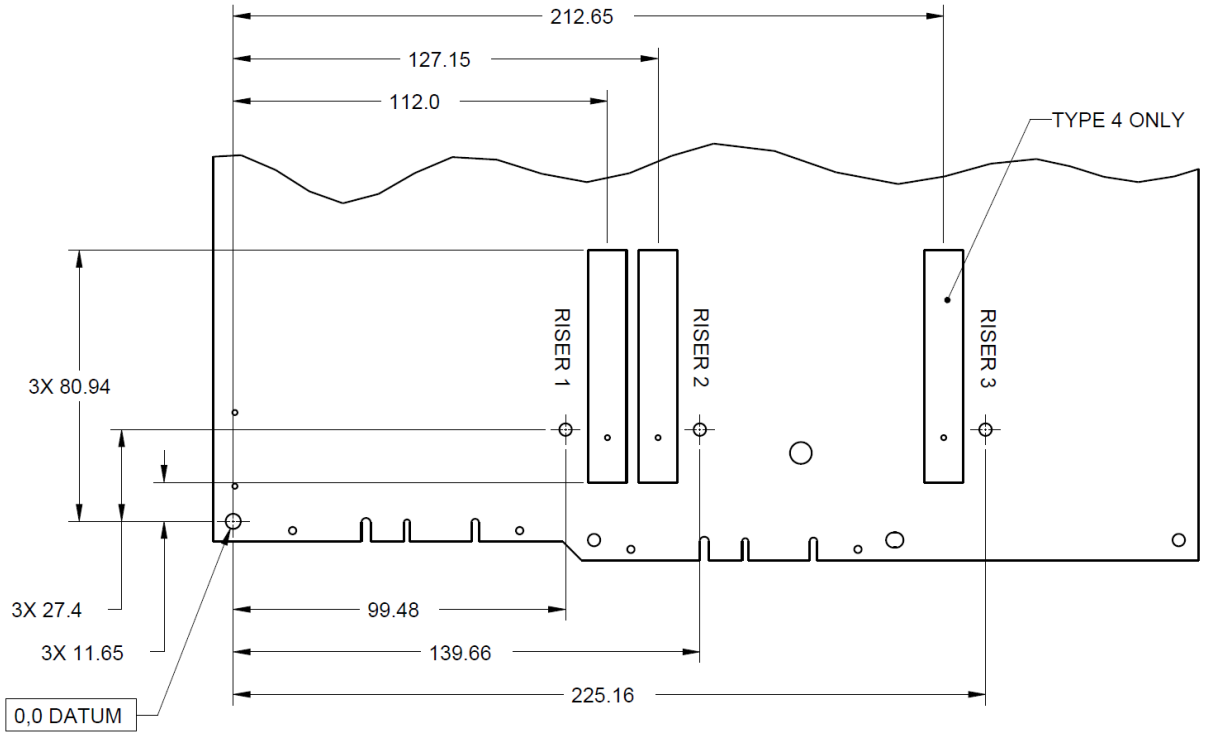


Table 4:Near IO Riser Attribute Requirements

Item	Requirement
Connector Choice	Strongly recommended
X-dimension location	Required for each implemented riser location, regardless of connector choice
Y-dimension location	Required for each implemented riser location, regardless of connector choice
Retention hole X-Y location	Required, regardless of whether the riser is implemented or not

10.10. Far Side IO Connector Placement

IO connector locations on the Far side of the HPM are not specified because they are all assumed to be cable-only connections and will not have major dependencies to chassis or subsystem reuse compatibility. The designer is free to choose/place these however they wish while respecting component height restrictions and other specified elements such as the Ingress / Egress power zone. It is recommended that high speed connectors placed on the Far Side leverage connector(s) described in **Section 12.1**.

10.11. Mounting Hole Requirements for IO Module Retention

There are required holes associated with each Near IO fixed riser location **regardless of whether the riser connector is implemented**. The intent of requiring these holes is to always make retention holes available to system designers (including systems with cable based I/O).

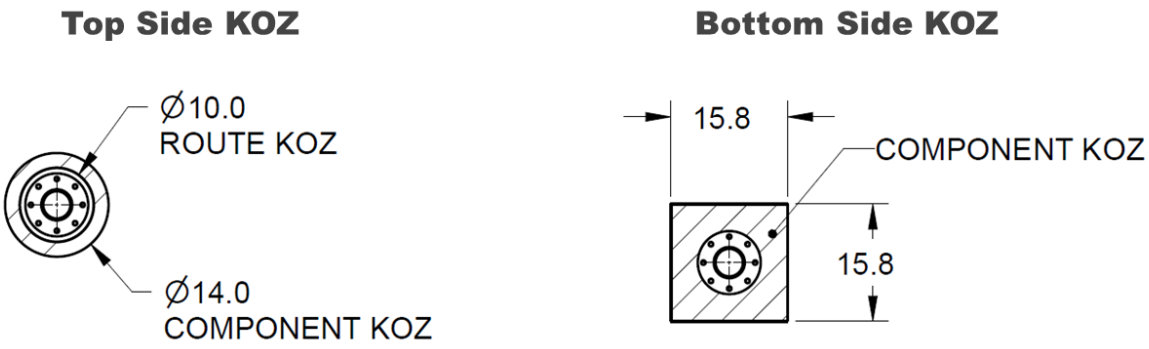
These holes are intended to be used for mechanical module retention (such as PCIe Risers, or other modules that require mechanical retention in the HPM area). There is one associated hole per defined riser location as shown in **Figure 28**.

- The retention holes associated with Riser 1 & Riser 2 are required on all M-DNO HPMs
- The retention hole associated with Riser 3 is required on all M-DNO Type 4 HPMs

Hole and pad dimensions follow standard mounting hole requirements as defined under Detail A of **Figure 7**.

Recommended KOZs around the holes are shown in **Figure 29** (note that there is a slight top side deviation from standard mounting holes).

Figure 29: IO Module Retention Hole KOZs



Chassis designers may choose the hardware and utilization method for riser retention. The hole location was selected to minimize impact of signal routing to the fixed riser locations as well as be accessible when cards are installed**.**

10.12. Primary Side Component Height Restrictions and KOZs

All M-DNO board types shall adhere to a common approach of three different component height restriction zones as shown in **Figure 30 and Figure 31**.

- The 12mm Zone is intended to allow for extended heatsinks and other thermal solutions while not prohibiting cabling of HSIO. Adherence to the 12mm zone is strongly recommended. While deviations are allowed, HPM designers should limit component selections which exceed the restriction to reduce interference with system design elements which will expect to inhabit this space.

- The 11.3mm Zone is intended to avoid interference with PCIe CEM cards directly above the HPM and its peripherals. Adherence to the 11.3mm Zone is required.

- The 6mm Zone is the most restrictive and is intended to prevent interference with mechanical elements in support of the fixed riser locations and retention holes. Adherence to the 6mm Zone is required. Note: The M-DNO workgroup is considering reducing the size or height restriction of this zone in the V1.0 release.in order to ease board placements.

Zone height restrictions apply specifically to soldered circuit board components, mated connector heights or other mated assemblies of soldered components. This does NOT apply to heatsinks of any kind, shrouds or other mechanical parts that are added to the board at a later integration stage.

DIMM connectors and other connectors placed by this specification are exempt from these restrictions (e.g. vertical PICPWR plugs).

This specification does not specify a specific Keep Out Zone for cable enablement.

Figure 30: Type 2 and 3 Primary Side Component Height Restriction Zones

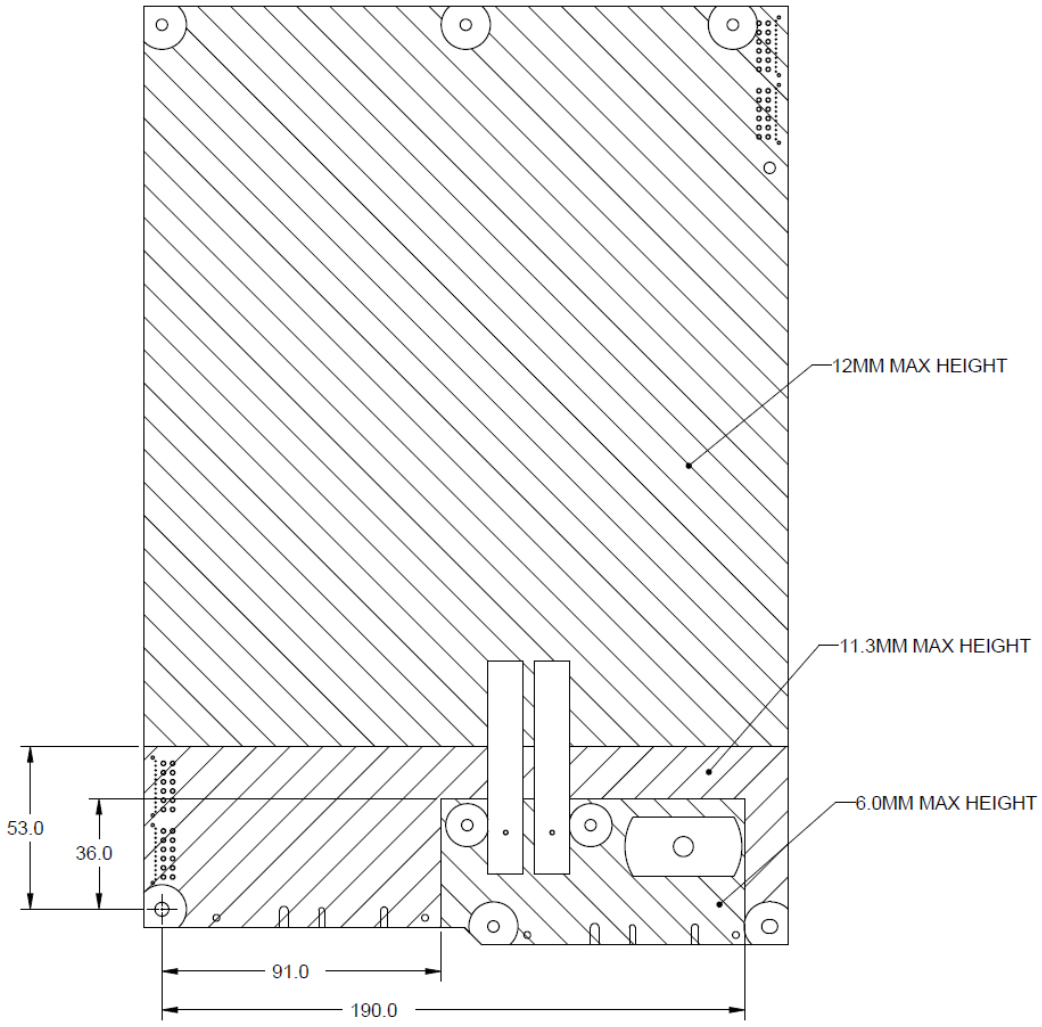
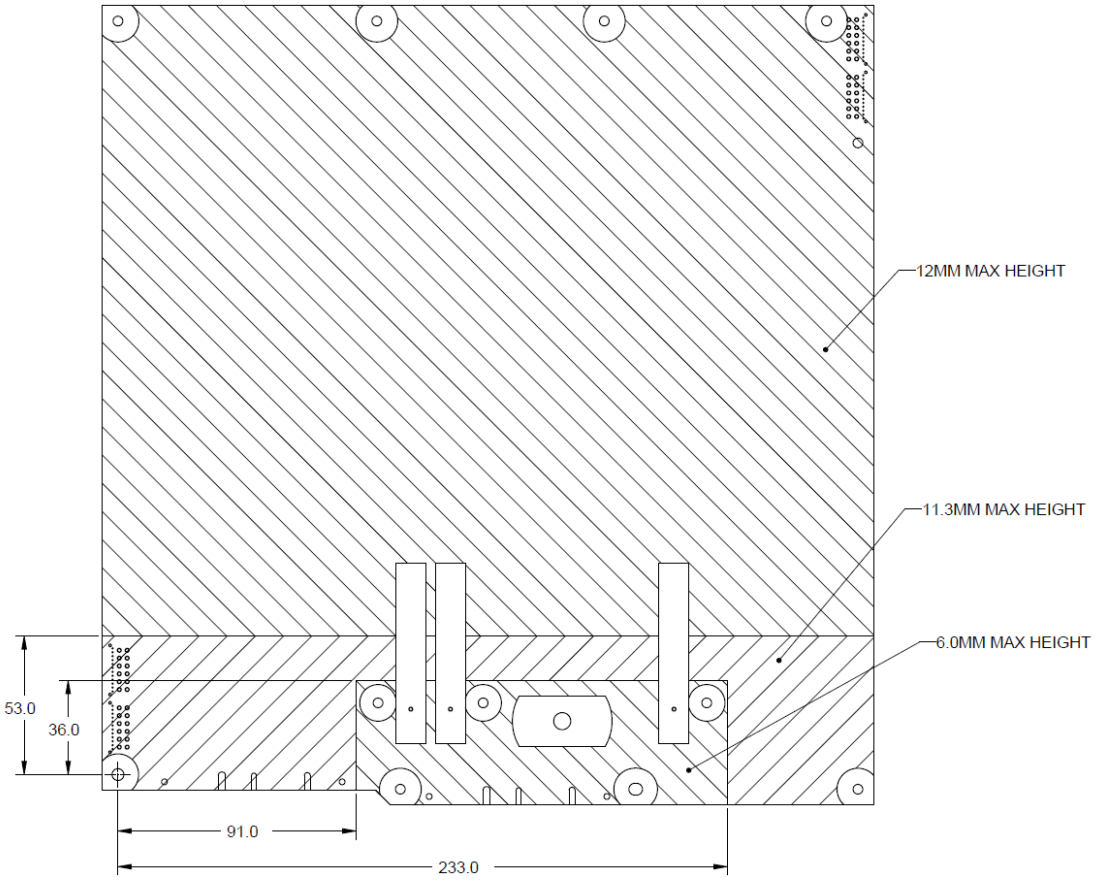


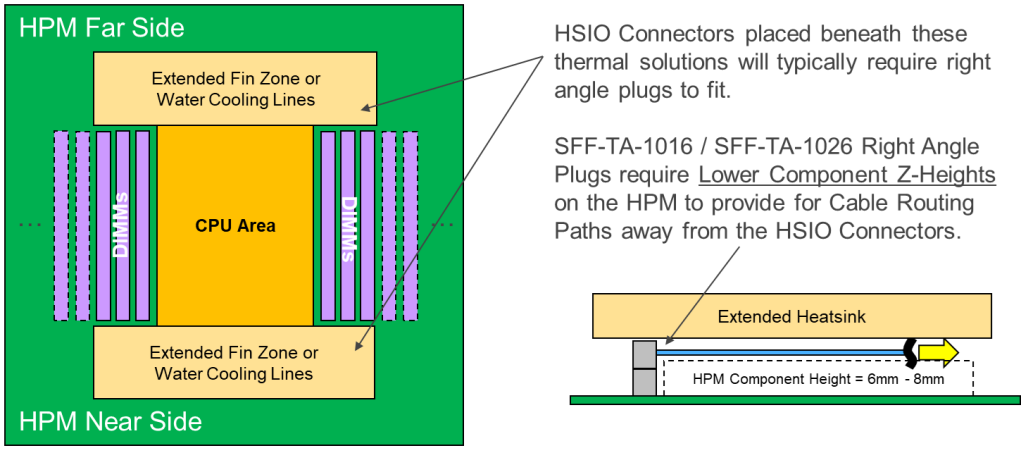
Figure 31: Type 4 Primary Side Component Height Restriction Zones



720

Implementors Note:

HPM designers must take care with component placements relative to cabled HSIO Connectors. Placements should allow for cable routing strategies beneath the defined maximum component heights. Failure to do so will limit potential system intercepts for the HPM.



10.13. Platform Custom Zone (Type 4 Only)

The Platform Custom Zone is defined as the Near Edge between the Far side of the OCP NIC R3 and the board edge. This area is intentionally undefined, so that System Designers may provide their desired features for the target platform.

Only Type 4 M-DNO HPMs feature a Platform Custom Zone.

The specification will define some options that are considered common use cases, to promote greater compatibility between future HPMs. This detail will be added in the V1.0 release and is intended to include using the Platform Custom Zone for:

- Adding a second OCP NIC R3 Slot
- Direct Dock E1.S

11. Power

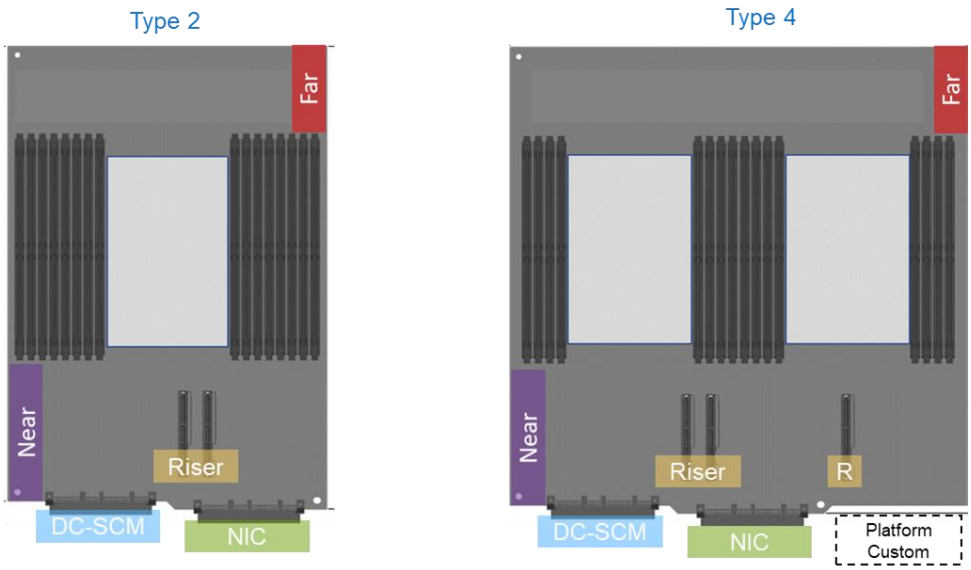
M-DNO compliant HPMs are assumed to Ingress / Egress 12V DC. While alternate voltages are under consideration for future versions (e.g. 48V DC implementations), this version assumes the burden for alternate power sources is placed on the system power delivery infrastructure (PDB, bus bar, etc.). For information on Power Management (including Power Gating and use of sideband signals) refer to the M-PIC specification.

11.1. HPM Power Zones

To enable a variety of system power configurations (See **Section 15**) there are two defined bi-directional power zones for each HPM type referred to as the “Near” and “Far” Ingress / Egress zones as shown in **Figure 32**. These zones are intentionally placed in opposing corners of the HPM to maximize flexibility of system orientation.

Additional power zones include power egress to DC-SCM, OCP NIC and each fixed board to board Riser location.

Figure 32: M-DNO Power Zone Overview (Type 2 and 4 Depicted)



11.1.1. Near and Far Bi-Directional (Ingress / Egress) Power Zones

Ingress / Egress Cabled Power Connector

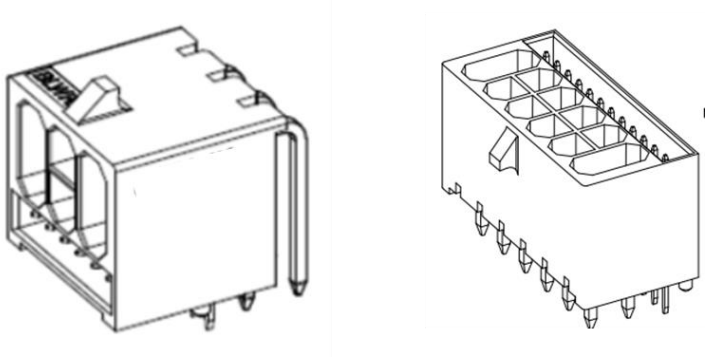
- **Power Connector Type**: 2x6+12SB and/or 2x3+6SB PICPWR .
  Refer to M-PIC Specification for additional details.
- **Connector Power Rating**: 864W (2x6) / 486W (2x3)
- **Typical usage**: Power ingress to HPM and / or egress to peripheral subsystems

It is assumed that most systems will provide power to M-DNO based HPMs via a cabled solution from a Power Distribution Board (PDB).

To maximize reuse of power delivery across all M-DNO HPMs, the required connectors for all Ingress / Egress power is the 2x6+12SB or 2x3+6SB PICPWR. An example of the 2x3+6 and 2x6+12SB is depicted in **Figure 33**.

Refer to the M-PIC specification for more information on PICPWR compliant connectors.

Figure 33: Example 2x3 + 6SB (Right Angle) and 2x6 + 12SB PICPWR Connector (Vertical)



Far Power Zone - Required

The Far Power Zone is **required** such that any system capable of providing power to the Far Zone of the HPM can provide ingress power to all M-DNO designs. While it is required for the HPM to implement this zone, the connector(s) may be depopulated.

Two connector locations are defined for each board type in the Far Power Zone. Refer to **Section 11.1.6** for specific locations per board Type.

One of the two defined locations is required and shall implement a 2x6+12SB PICPWR connector.

The second location is optional and may implement either a 2x6+12SB or 2x3+6SB PICPWR connector if implemented.

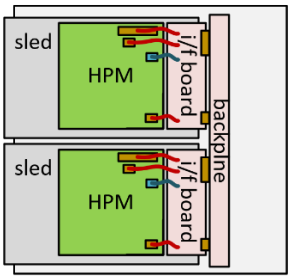
HPM designers electing to implement only a single connector may choose between either of the two specified locations.

The far power zone connectors should be capable of meeting the full HPM power budget when used for ingress.

Implementors Note:

HPMs which implement the cabled PICPWR connectors may still be used in multi-node systems via an interposer or interface board to enable blind mate into system backplane / infrastructure. Refer to **Section 14** for an example of such a system.

Figure 34: M-DNO HPM with multi-node interface board



Near Power Zone - Recommended

Due to the expected density of HPM designs in this area of the board, the Near Power Zone **may** be implemented at the discretion of the HPM designer. If Near zone power connectors are implemented, the connector(s) may be depopulated.

To increase the likelihood that this zone can be implemented, connectors may be placed anywhere within the designated zone area rather than having a fixed location. Refer to **Section 11.1.6** for this zone outline.

Within the defined zone any combination of 2x3+6SB and 2x6+12SB PICPWR connectors are allowed.

To maximize system use cases, it is recommended that HPM designers provide as much Ingress / Egress capability as feasible given HPM layout constraints. At a minimum, a single 2x3+6 (for egress to a peripheral subsystem) is recommended.

Implementors Note:

If providing Ingress power via the Near Power Zone is desired, it is recommended that the connector configuration matches the connector configuration of the Far Power zone in order to maximize flexibility for Power Ingress / Egress.

11.1.2. Fixed I/O Riser Location Power

- **Power Connector Type**: Integrated within Amphenol G03V213X2HR Recommended Refer to M-PIC Specification for additional details.
- **Connector Power Rating**: >180W
- **Minimum Power Delivered to Connector by HPM**: 87W
  Typical usage: Power egress for 1 (required) or more (optional) 75W PCIe CEM Devices per Riser

For each **implemented** fixed riser location (up to three):

- HPMs shall deliver a minimum of 87W of power to the riser connector (See **Table 5** for calculation of 87W effective total power required per slot). This requirement is defined to guarantee each riser location can support a minimum of one 75W PCIe CEM card and reduce power cabling requirements in dense systems.

- HPMs may deliver additional power to the riser connector to enable additional cards at each riser location.

- Additional supplemental I/O power (e.g. auxillary power for a GPU) is not defined and is assumed to be provided directly by system infrastructure (e.g. cable from PDB).

- I/O Risers must comply with M-PIC PICPWR sideband signaling requirements.

Table 5. Minimum HPM Power Provided to Fixed Riser Locations

Power Rail	**75 W Slot**[1]
+3.3Vaux	Generated on PCIe riser. Derived from +12V
+3.3V (V_{cc3_3})	Generated on PCIe riser. Derived from +12V
+12V Voltage Current	 12V nominal 7.25A total: 5.5 A (CEM 5.0) + 1.0A (VR conversion to V_{cc3_3}) + 0.35A (VR conversion to +3.3Vaux) + 0.40A (misc.)

11.1.3. DC-SCM 2.0

- **Power Connector Type**: See OCP DC-SCM 2.0 specification (Refer to **Section 6**)
- **Connector Power Rating**: 50W
- **Typical usage**: Power egress for DC-SCM 2.0

11.1.4. OCP NIC 3.0

- **Power Connector Type**: See OCP NIC 3.0 spec (Refer to **Section 6**)
- **Connector Power Rating**: 80W
- **Typical usage**: Power egress for OCP NIC 3.0

11.1.5. Platform Custom Zone (Type 4 Only)

Power to the Platform Custom Zone is not defined as it is considered implementation specific.

11.1.6. Ingress / Egress Power Connector Locations

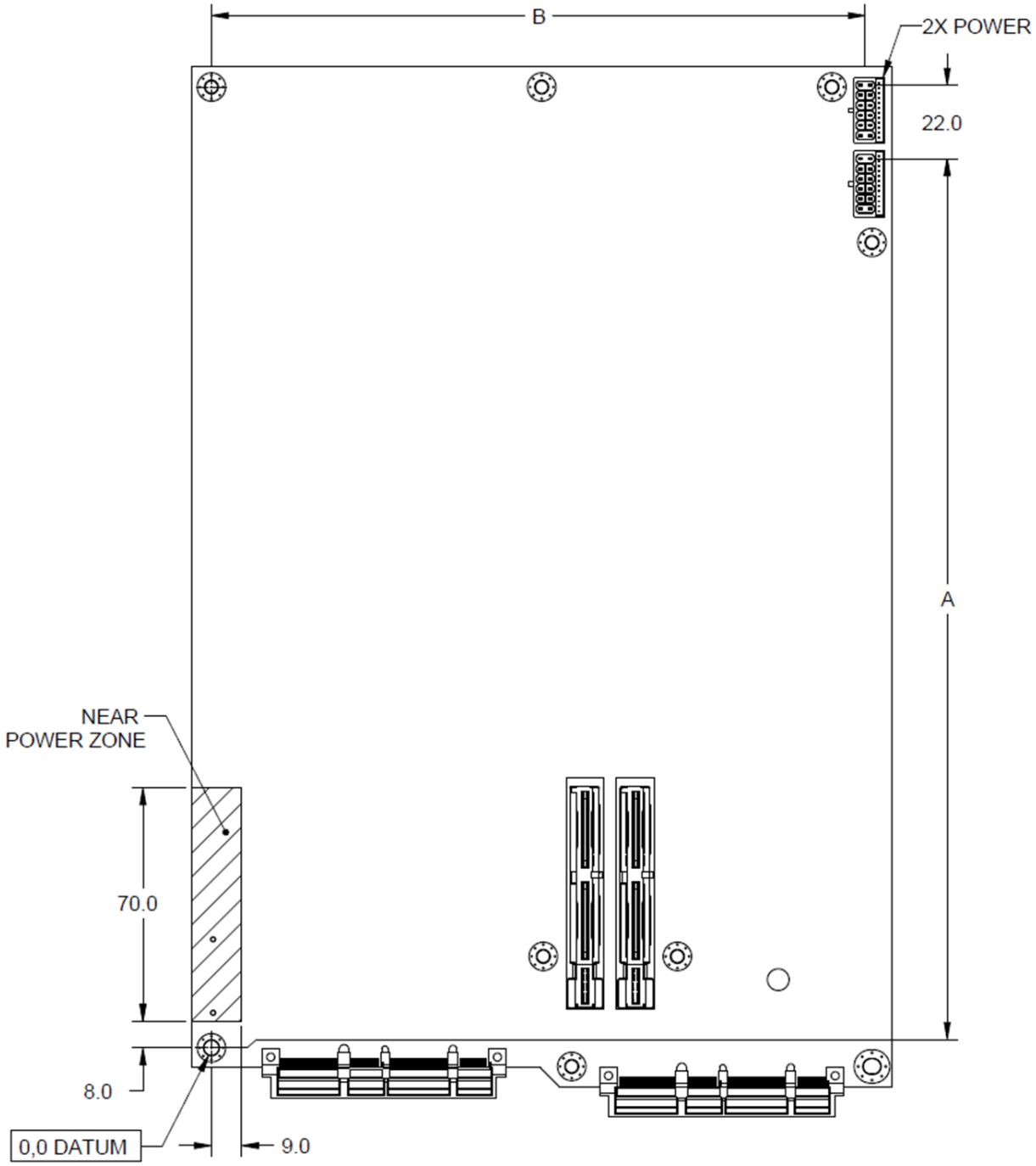
Figure 35 denotes the locations of the bidirectional Near and Far power ingress / egress connectors.

As described in **Section 11.1** the two Far power connector locations are fixed for each board type with common spacing between the two locations across all board types. Dimensioning is to Power Pin1 and is intended to be consistent for 2x6+12SB or 2x3+6SB selections.

Refer to the drawing and table within **Figure 35** for the fixed location for each board type. Note that while for simplicity only a Type 2 board is depicted the dimensions listed are valid for other board types.

If implemented, Near connectors may be placed anywhere within the depicted zone which is common across all board types.

Figure 35: Near and Far Power Zone Connector Locations



POWER CONNECTORS		
	DIMENSION	
TYPE	A	B
2	266.5	197.5
3	TBD	197.5
4	266.5	282.5

DIMENSIONED TO CIRCUIT1

855

11.2. HPM Power Planes

The HPM power planes have the following features

- At maximum load, the HPM power shapes have a maximum of 30°C T-rise and do not exceed 100°C absolute.
- At maximum load, the maximum HPM voltage drop (IR loss) between primary power ingress connectors and associated loads or egress connectors is less than or equal to 1%.
- It is not expected that all loads/connectors on the HPM will be operating at maximum power concurrently. However, it is recommended that minimally, the power distribution be designed to allow any single load/connector to operate at max power rating.

12. I/O System (Electrical Interfaces)

The HPM shall be required to implement electrical interfaces that must be in compliance with the DC-MHS family of specifications. Refer to **Section 6** for additional details.

This section provides additional guidance for specific connectors on M-DNO HPMs.

12.1. High Speed IO (HSIO) Connectors

HSIO connector selections are strongly suggested, but not required for compliance. Use of the suggested HSIO connectors will ensure broader compatibility with chassis, riser, and cable interfaces in the future.

Requirement: Connector Choices must be compliant with M-XIO specification.

Table 6: M-DNO Connector Recommendations

	Recommended Connector	Note
Fixed Riser	SFF-TA-1033	Compatible with 1016 cabled solutions
Near HSIO	SFF-TA-1016	Common interconnect for cabled connections and Riser solutions
Far HSIO	SFF-TA-1016 or SFF-TA-1026	Appropriate due to low profile and ability to fit under thermal solutions with appropriate plug selection

The Near HSIO location and flexibility is further described in **Section 10.9**.

12.2. Internal USB

- **M-PIC Section Reference:** “Internal USB3 Connector”
- **Connector Requirement:** Required (may be de-populated)
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to the DC-MHS M-PIC Specification

Electrical implementation for an internal USB3 connector follows the M-PIC specification. It is strongly recommended that HPMs implement a Type A connector. For M-DNO HPMs the connector shall be placed as defined in **Section 10.7**.

12.3. Intrusion Switch

- **M-PIC Section Reference:** “Intrusion Switch”
- **Connector Requirement:** Required (may be de-populated)
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to the DC-MHS M-PIC Specification

Electrical implementation for the intrusion switch follows the M-PIC specification. For M-DNO HPMs the connector shall be placed at the location defined in **Section 10.7**.

12.4. Boot Storage

- **M-PIC Section Reference:** “Boot Storage”
- **Connector Requirement:** Recommended
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to the DC-MHS M-PIC Specification

Electrical implementation for boot storage follows the M-PIC specification. Due to HPM layout density it is expected that the Cable Optimized connector will be more prevalent in M-DNO designs. Type 4 M-DNO HPMs may choose to utilize the platform custom zone to enable the Direct Attach Boot Storage option. The location for Boot Storage is defined in **Section 10.7**.

12.5. Control Panel

- **M-PIC Section Reference:** “Control Panel Interfacing”
- **Connector Requirement:** Primary Required(may be de-populated), Secondary Optional
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed
- **Connector:** Refer to the DC-MHS M-PIC Specification

Electrical implementation for the Control Panel(s) follows the M-PIC specification. For M-DNO HPMs the Primary Control Panel is required while the Secondary Control Panel is optional, the location of both control panel connectors is defined in **Section 10.7**.

12.6. PDB Management Connector

- **M-PIC Section Reference:** “PDB Management Connector”
- **Connector Requirement:** Required (may be de-populated)
- **Connector Placement:** Recommended fixed location provided, expanded zone allowed.
- **Connector:** Refer to the DC-MHS M-PIC Specification

Electrical implementation for the PDB Management Connector follows the M-PIC specification. For M-DNO HPMs implementation of this connector is required and the location is defined in **Section 10.7**.

13. Adapted M-DNO HPMs

This section shall define open and standardized adaptations of the M-DNO HPM specification.

1. Any changes to the form factor, which do not impact the specification compliance table (**Section 4)**, are still considered a base M-DNO compliant HPM.

2. If an HPM does not meet all the items in the specification compliance table (**Section 4)**, this results in an Adapted HPM which may not fit existing system infrastructure built for compliant boards.

Future Adapted HPMs will be documented in this section if productized and accepted in future M-DNO revisions.

13.1. Adapted Far Side Power Zone for Board to Board Interface

While it is expected that many systems will implement the required connector and provide power via the defined PICPWR cabled connectors, another M-DNO use case involves blind mating HPM “sleds” into multi-node chassis infrastructure. HPMs intended exclusively for these use cases may prefer to deviate from the compliance requirements and choose to adapt a blind mate / board to board style connector along the far edge of the board.

No specific connector or location is defined for these applications at the time of this specification release. The DC-MHS workgroup is considering additional guidance for board to board interfacing in a future release.

14. Supplemental Material: M-DNO Conceptual Implementation Examples

The M-DNO specification has multiple form factor types to address various product types and sizes. In this section some of the possible configurations and usages for the different Types will be shown.

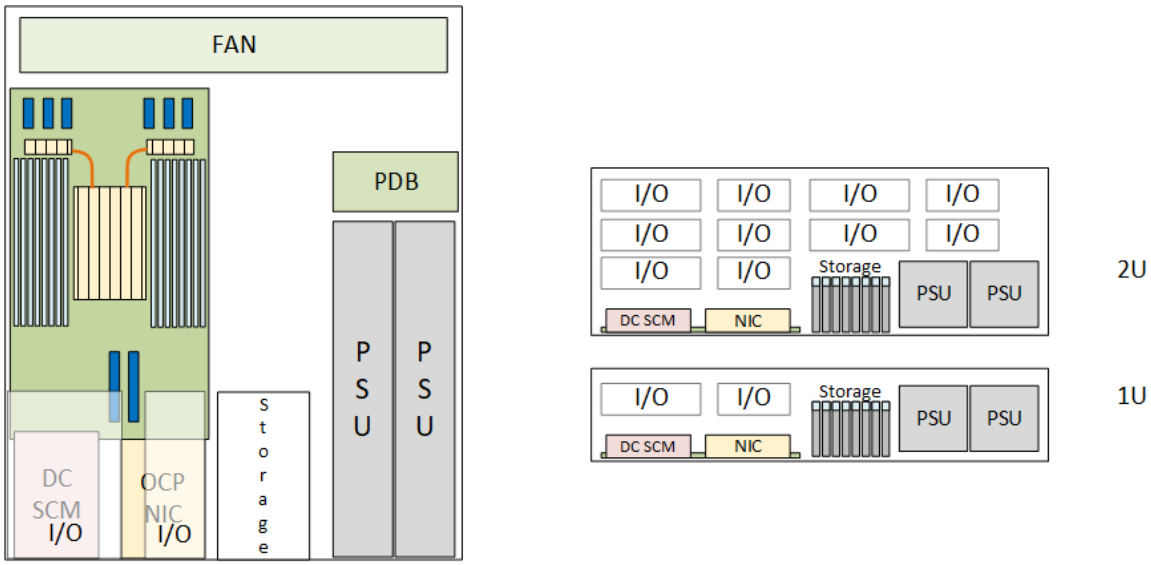
Note: Image representation of elements may not be to scale, and is subject to change

It is understood that the configurations shown represents a small sample of what could be possible. This section also conveys the reasoning behind the different sizes of HPM associated with the three types.

Type 2

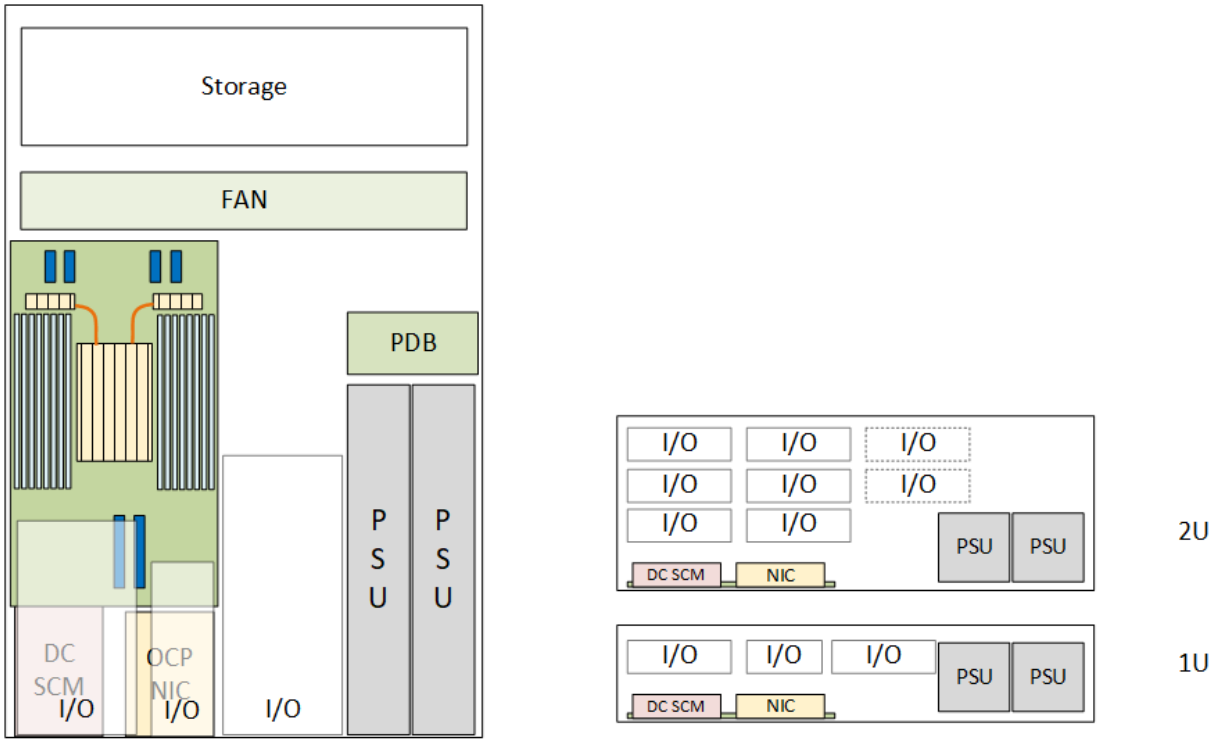
The Type 2 HPM was optimized to provide an ideal solution for Dense (1/2 Width) 1 Socket designs. Type 2 is intended to support PCIe direct attach risers and EVAC thermal solutions as well as larger CPU sockets.

Type 2 Configuration Example – 1 Node Edge



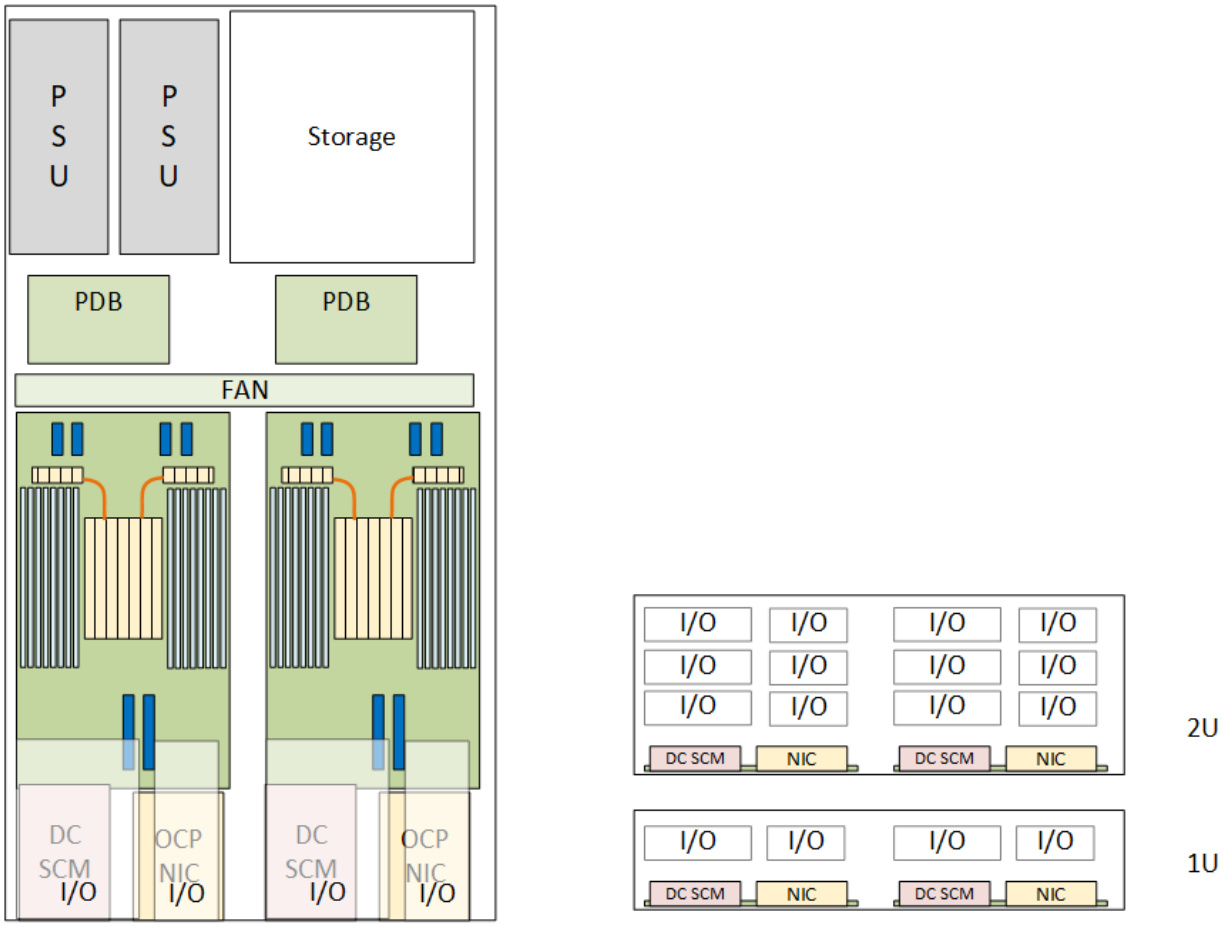
The Type 2 HPM would also be applicable for traditional enterprise server applications in or 1U or 2U heights. The variability of capabilities for I/O and Storage would be plentiful and facilitated by different riser, cable, and mid-plane configurations.

Type 2 Configuration Example – Enterprise Server



The Type 2 HPM would also be suitable for 2 Node products.

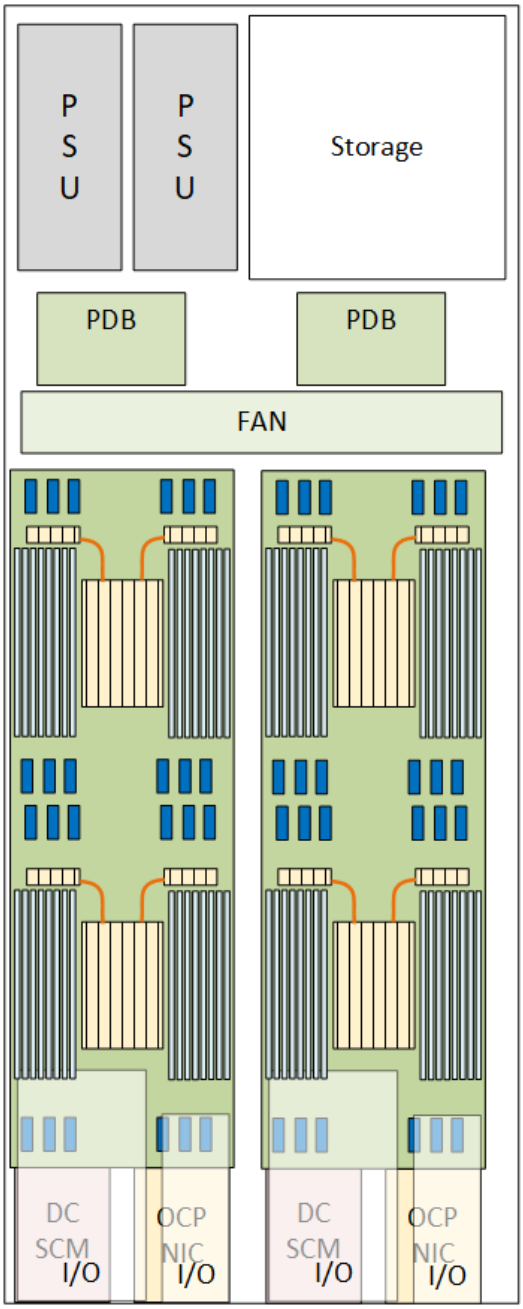
Type 2 Configuration Example – 2 Node

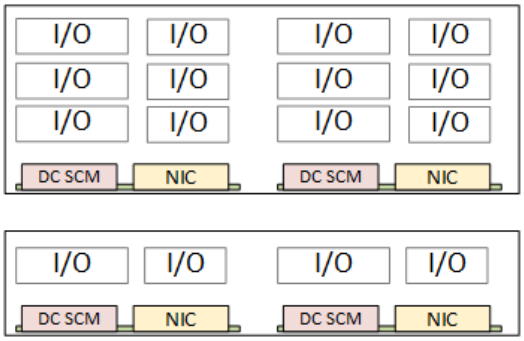


Type 3

The Type 3 HPM grows in depth to allow 2 socket “shadow core” designs, specifically to support 2 Nodes across a chassis. In this configuration the ability to utilize the full PCIe resources is de-prioritized. The ability to support EVAC thermal solutions would be applicable.

Type 3 Configuration Example – 4 Node

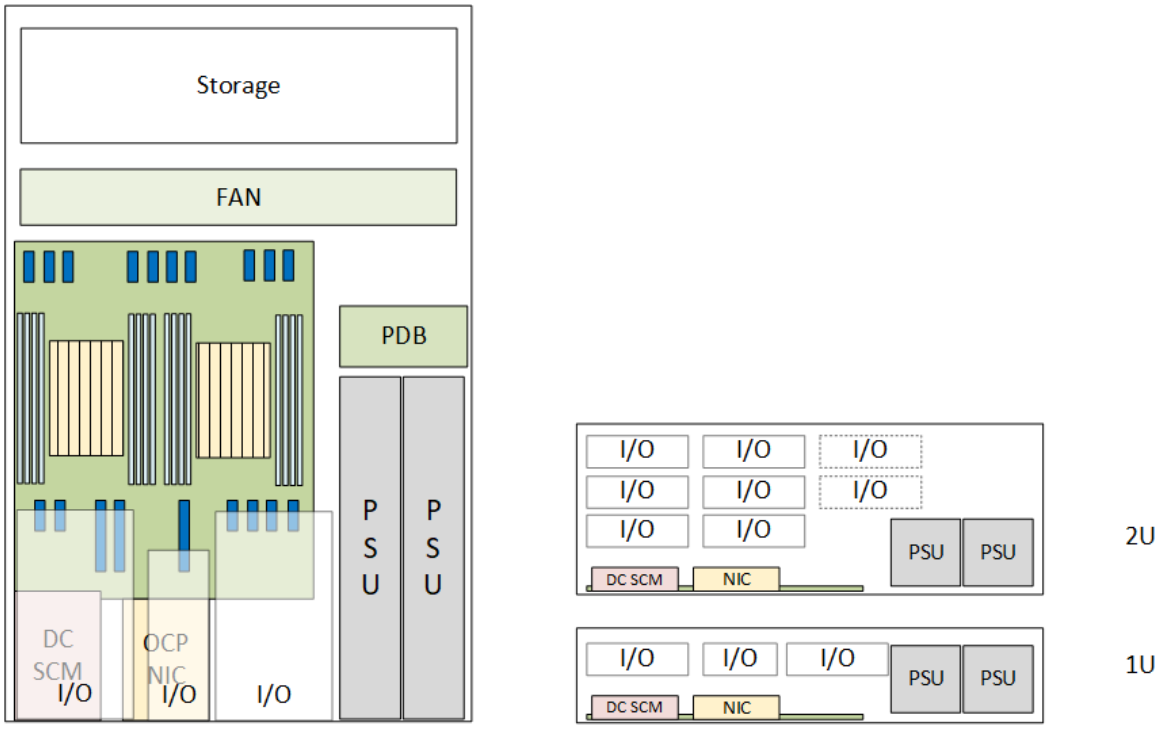




Type 4

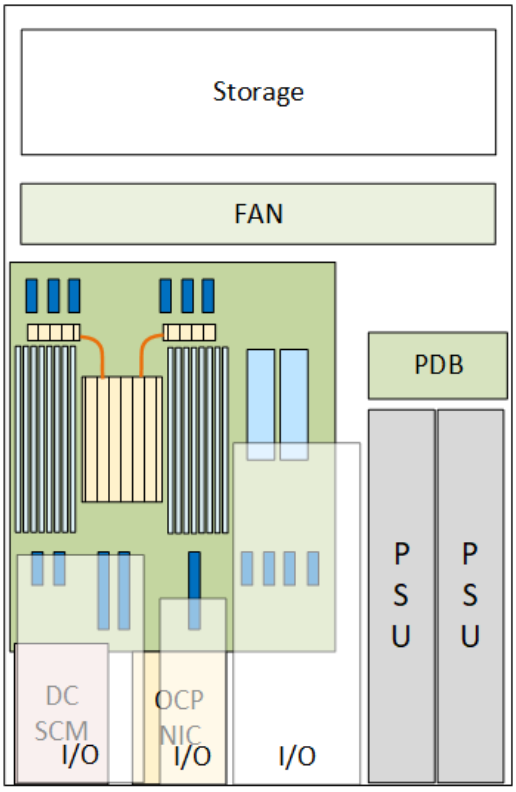
The Type 4 HPM is the only Type to grow in width. The primary driver for the Type 4 form factor is ability to support a dual socket “spread core” 2 Node product with adjacent PSUs in a 19” (or larger) rack. To achieve this 2 socket design a concession is made on memory socket support so that only one DIMM per channel is expected on a 8 channel per socket architecture. The other features intended to be supported on a Type 4 HPM would be full PCIe lane count, and EVAC thermal solutions.

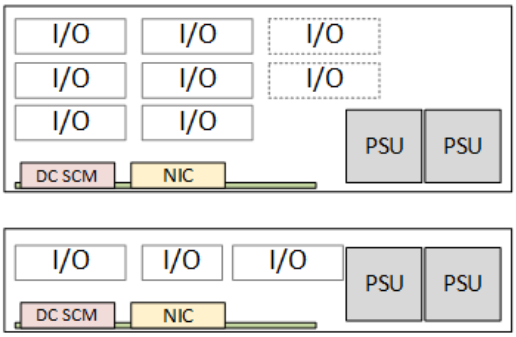
Type 4 Configuration Example – 2 Socket Spread Core



Another possible Type 4 HPM would be a 8 memory channel CPU with 2 DIMMS per channel
995 as in Type 2, but with more on board peripherals than the other ½ width Types.

Type 4 Configuration Example – Expanded Features 1 Node





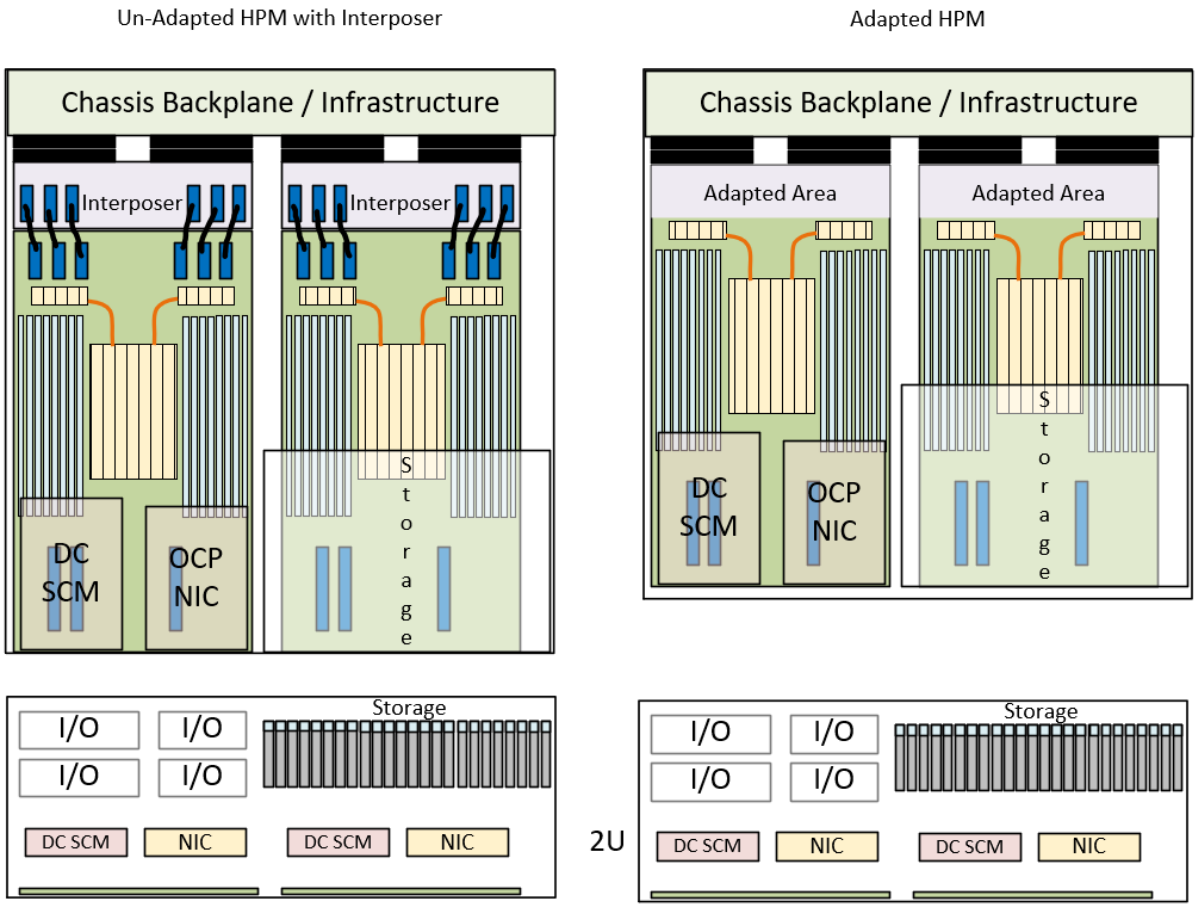
Multi-Node Specific

Multi-Node Adaptation

As described in the Power Zone **Section 11.1,** multi-node HPMs may choose to adapt the HPM to add board to board connectors on the Far board edge intended to directly mate into chassis power infrastructure (mid-plane, PDB, bus bar etc.).

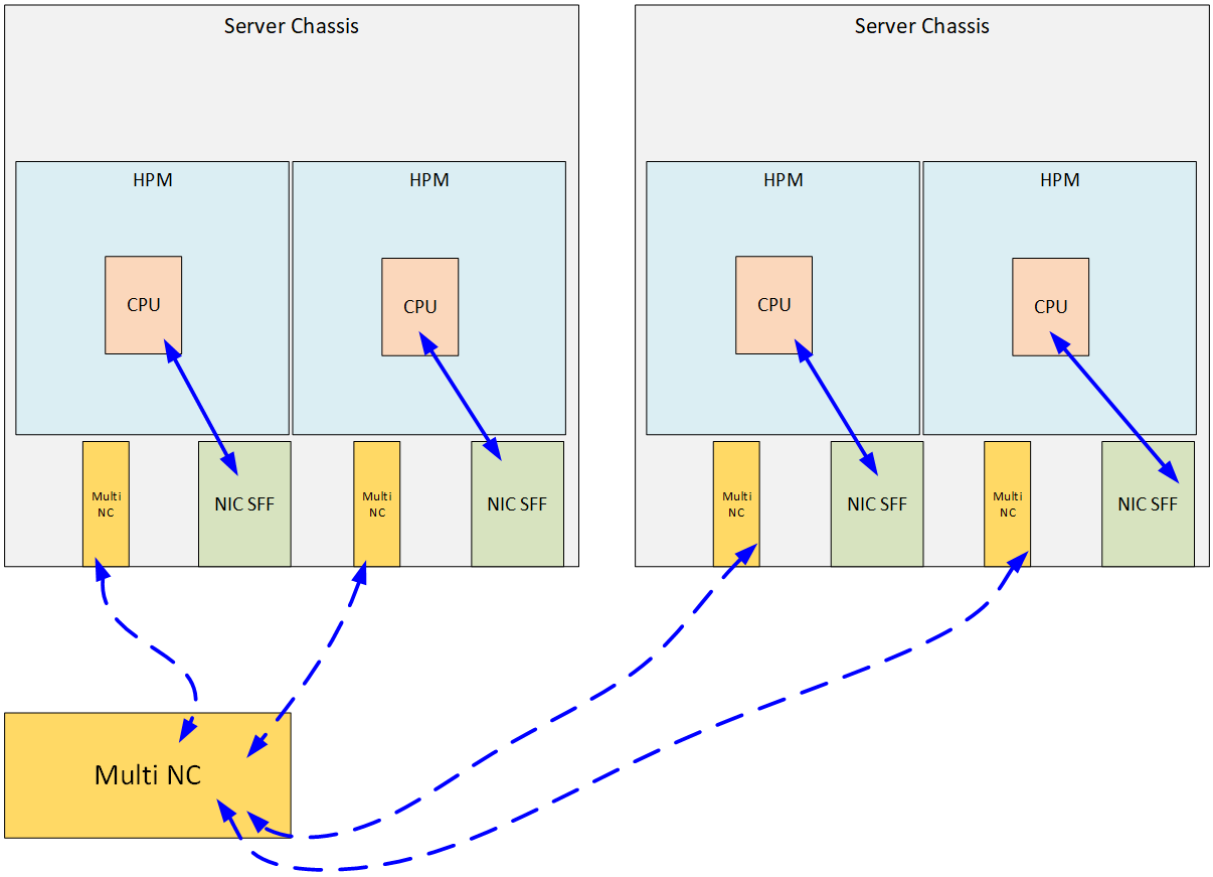
Un-adapted HPMs can also be leveraged with this type of chassis infrastructure by leveraging an interposer board between the HPM and the chassis infrastructure.

The example below depicts using an un-adapted HPM on the left and an adapted HPM on the right in a similar system. For this example, shown is a Type 2 node opting to "float" the DC-SCM and NIC cards as opposed to placing them Co-Planar. Additionally, a 21" chassis is depicted.



Multi-Node Management

How to deploy a multi-node management infrastructure using base specification complaint HPMs is outside of the scope of this specification. However, various common methodologies were evaluated to ensure that M-DNO compliant HPMs could be leveraged into these infrastructures. As an example, a small low-cost local node controller could be connected to the DC-SCM 4C+ connector and then connected to a chassis manager or multi-node controller.



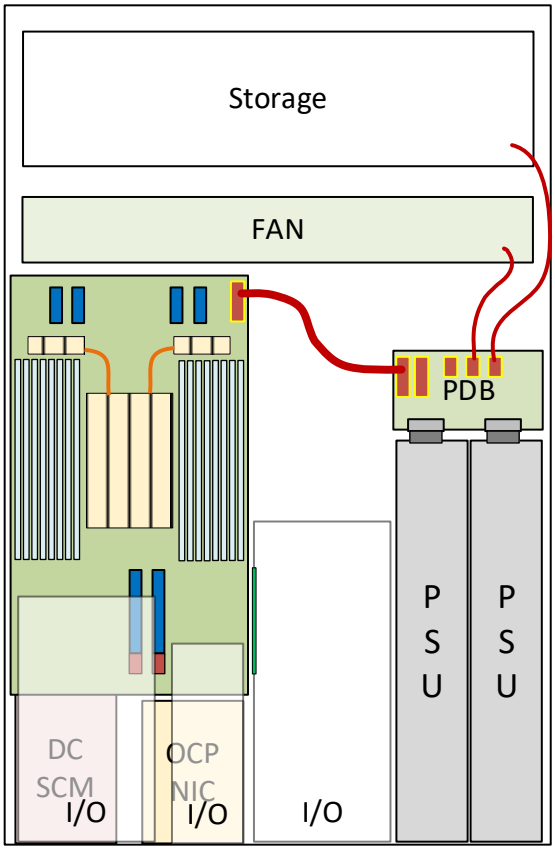
15. Supplemental Material: M-DNO Power Zone Usage Examples

The M-DNO specification provides some flexibility to HPM implementors and system designers when it comes to Power Zone Usage. In this section, demonstration of some expected configurations leveraging these various options are conveyed. For simplicity's sake, the different power flows are demonstrated using the same HPM board Type (Type 2), however the power zone use case flexibility is common across all board types.

The first example listed below shows a simple monolithic (one HPM) system where PSUs feed power to the system PDB, the HPM power zones are utilized in the minimum required model:

- Far Side Ingress: Power from PDB to HPM
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: None
- Supplemental Power to I/O: None

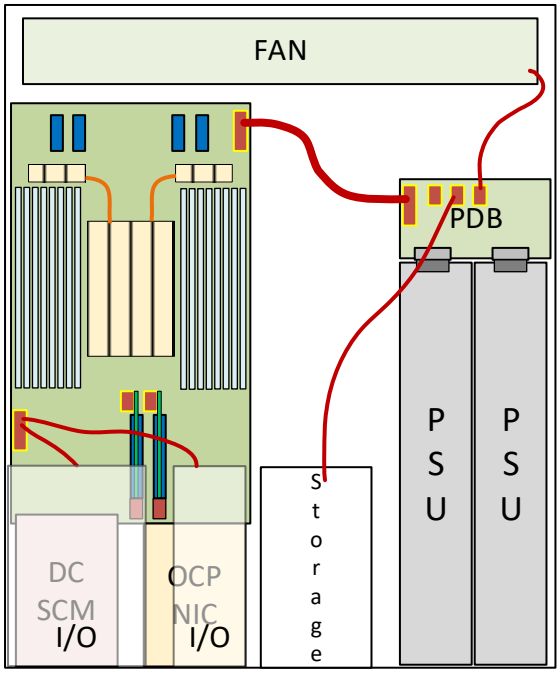
Example 1: Monolithic Basic One Zone Ingress



In the second example below, a monolithic (one HPM) system where PSUs feed power to the system PDB is shown. However, in this example, the optional Near Side power zone is leveraged:

- Far Side Ingress: Power from PDB to HPM
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: Supplemental power cable to CEM card aux (Note that the PICPWR definition requires a control “puck” to power gate these cables)
- Supplemental Power to I/O: From Near Zone (These cables could also be sourced from the PDB directly and would not require a “puck” as control logic could be based on the PDB.)
- Note that because the HPM depicted supports both power Ingress / Egress zones the same HPM could be used in systems which leverage the far side for ingress power

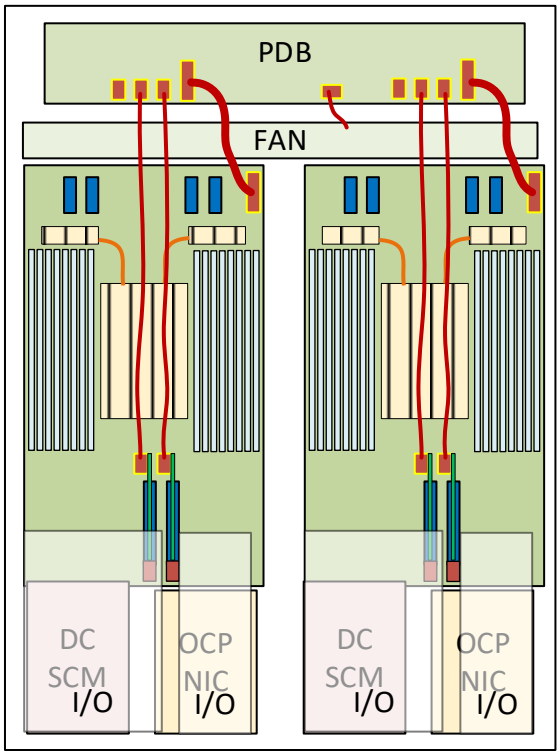
Example 2: Monolithic Leveraging Both Zones



The third example below illustrates a multi-node (>1 HPM) system with a Far Side PDB that could be supplied via PSUs, system level bus bars, or even rack level power distribution.

- Far Side Ingress: Power from PDB to HPM (while these connections are depicted with cables the HPM could also be adapted to support a board-to-board connector to chassis power infrastructure like a PDB as noted in **Section 11.1**)
- Far Side Egress: None
- Near Side Ingress: None
- Near Side Egress: None
- Supplemental Power to I/O: From the PDB directly (do not require a “puck” as control logic could be based on the PDB)

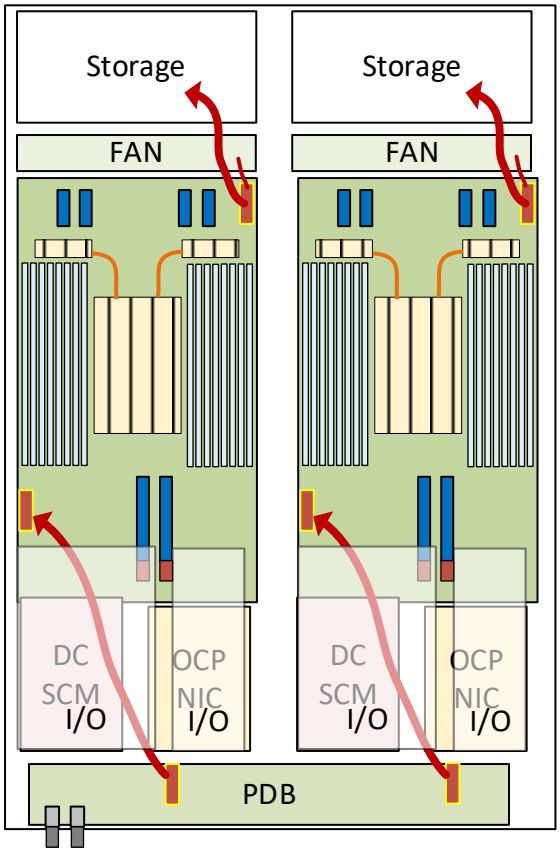
Example 3: Multi-node with Far Side PDB



The fourth example below demonstrates a multi-node (>1 HPM) system with a Near Side PDB that could be supplied via PSUs, system level bus bars or even rack level power distribution.

- Far Side Ingress: None
- Far Side Egress: Used to power Storage peripheral subsystem,
- Near Side Ingress: Power from PDB to HPM (cabled)
- Near Side Egress: None
- Supplemental Power to I/O: None
- Note that because the HPM depicted supports both power Ingress / Egress zones the same HPM could be used in systems which use to leverage the far side for ingress power

Example 4 : Multi-node with Near Side PDB



16. Appendix A - Checklist for IC approval of this specification (to be completed by contributor(s) of this Spec)

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document.

This will be filled out at V1.0

17. Appendix B-__ <supplier name> - OCP Supplier Information and Hardware Product Recognition Checklist

This is a Base Specification and no specific designs can be derived from this specification. Future Design Specifications will be established based on DC-MHS Rev 1.0 specifications, and supplier information and HW checklist will be applicable and filled by future contributors