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Compute Project

QCT F06S/ F06T 19" 2U 4Node/2Node System "Carmel"

Revision 0.1

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Revision History:

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1 INTRODUCTION

Both F06S and F06T (family code name Carmel) are 2RU height systems with OCP compliant 2P server board for standard 19" EIA rack. F06S is a 2U4N System with four hot-pluggable motherboard Sleds while F06T is a 2U2N System with two hot-pluggable motherboard Sleds. This specification is to define the interfaces, connection topology of various buses and control signals between different modules in the system. It includes the pin definition and basic electrical parameters.

1.1 F06S 2U4N System

F06S 2U4N System is a 2RU 4-Node (2U4N) system for standard 19" EIA rack which comprises of four F06S Sleds, two power suppler units, four dual-rotor system fans, and twenty-four front loading SFF HDD/SSD trays. F06S 2U4N System consists of four high performance 2P servers featuring Intel Grantley platform. Each F06S Sled contains an OCP compliant 2P server board (Facebook Server Intel motherboard v3.1, <http://www.opencompute.org/wiki/Motherboard/SpecsAndDesigns>), OCP mezzanine v1 card, Interposer board and Riser board. It connects with SFP+ connectors of OCP mezzanine v1 card or RJ45 connector of Intel I210 LOM. The BMC (Baseboard Management Controller) is used to manage the sled itself which supports both in-band management and out-of-band management through the sideband control of Ethernet LAN.

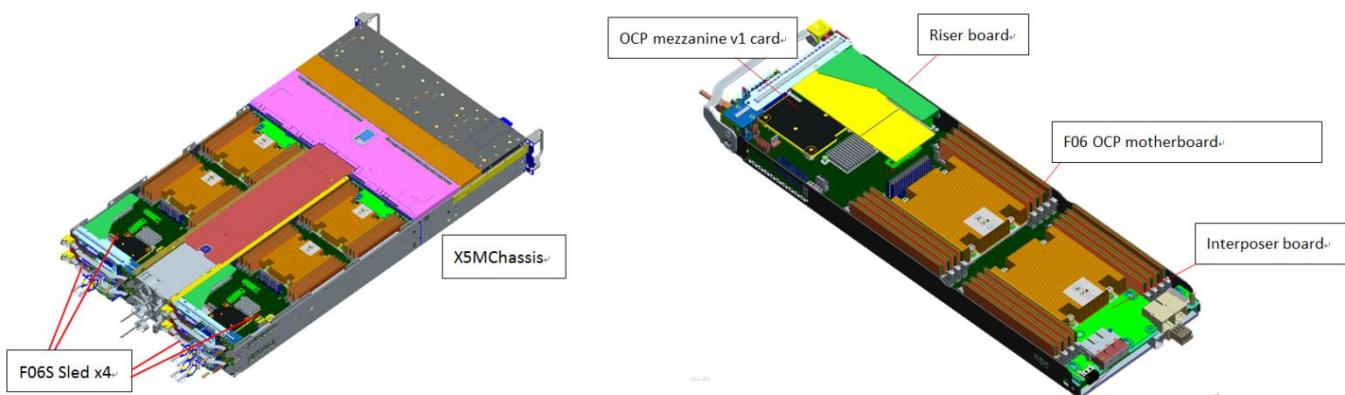


Figure 1-1 F06S 2U4N System Overview

1.2 F06T 2U2N System

F06T 2U2N System is a 2RU 2-Node (2U2N) system for standard 19" EIA rack which comprises of two F06T sleds, two power supply units, four system fans and twenty-four front loading SFF HDD/SSD trays. F06T 2U2N System consists of two high performance 2P servers featuring Intel Grantley platform. Each F06T Sled contains an OCP compliant 2P server board (Facebook Server Intel motherboard v3.1,

<http://www.opencompute.org/wiki/Motherboard/SpecsAndDesigns>), and it connects with SFP+ connectors of OCP mezzanine v1 card or RJ45 connector of Intel I210 LOM. The BMC (Baseboard Management Controller) is used to manage the sled itself which supports both in-band management and out-of-band management through the sideband control of Ethernet LAN.

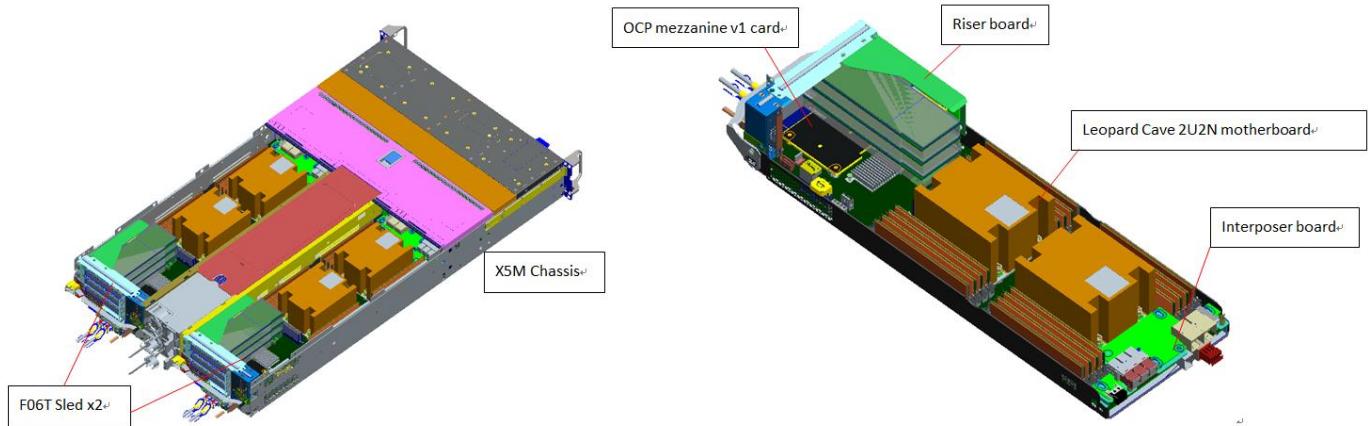


Figure 1-2 F06T 2U2N System Overview

1.3 F06 OCP motherboard

F06 OCP motherboard is the one used in F06S / F06T Sleds and it is fully compatible with OCP 2P server board (Facebook Server Intel motherboard v3.1) powered by Intel E5-2600 v3 / v4 CPU architecture.

The Facebook Server Intel motherboard's form factor is 6.5 x 20 inches.



Figure 1-3: Facebook Server Intel motherboard Placement

(quoted from Facebook Server Intel Next Generation Xeon motherboard v3.1,

<http://www.opencompute.org/wiki/Motherboard/SpecsAndDesigns>)

The figure below illustrates the functional block diagram of Facebook Server Intel motherboard

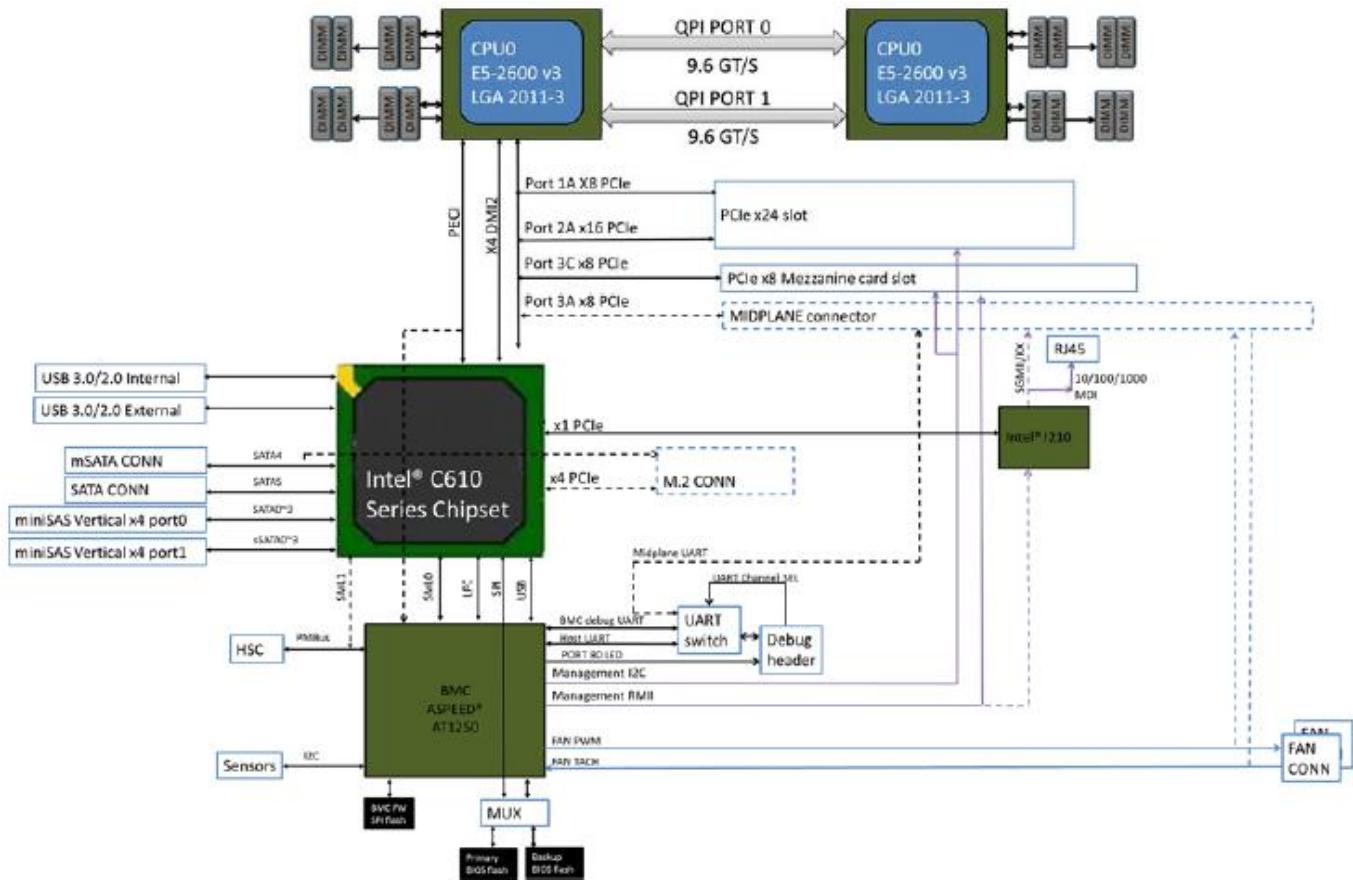


Figure 1-4 Facebook Server Intel motherboard functional Block Diagram
 (quoted from Facebook Server Intel Next Generation Xeon motherboard v3.1,
<http://www.opencompute.org/wiki/Motherboard/SpecsAndDesigns>)

The major differences between F06 OCP motherboard and Facebook Server Intel motherboard is as table 1-1 shown.

	F06 OCP motherboard for F06S 2U4N	F06 OCP motherboard for F06T 2U2N	Facebook Server Intel motherboard
Mini-SAS connectors (J9/J11)	Stuff	Stuff	Empty
AirMax 3x8 connector (J39)	Stuff	Stuff	Empty
Guide Pin (JP17)	Stuff	Stuff	Empty
Power connector (J38)	Stuff	Stuff	Empty , Wiring a Power cable
mSATA connector (J7)	Empty	Empty	Stuff
M.2 connector (J8)	Stuff	Stuff	Empty
Fan connectors(J35,J36)	Empty	Empty	Stuff

Table 1-1 BOM Difference between F06 OCP motherboard and Facebook Server Intel motherboard

2 PRODUCT ARCHITECTURE OVERVIEW

2.1 F06S 2U4N System Product Features

2.1.1 Product Features

F06S 2U4N System's ingredients and features are shown as follows.

Item	Features
Form Factor	2U Chassis 31.1"x17.48"x3.44"(789.94 x 444 x 87.5mm) [LxW xH]
Baseboard size / Quantity	20" x 6.5" (508 x 165mm), 12 layer, 2.16mm / up to 4 pcs per system
CPU (per node)	(2) Intel® Xeon® processor E5-2600 V3 and V4 family (up to 135W)
Max Processor Wattage	135W, VRD 12.5
QPI Speed	9.6 GT/s, 8.0GT/s, 6.4GT/s
Chipset	Intel® C610 series
Memory (per node)	(16) RDIMM slots Up to 256GB (16GB x16) for DDR4 RDIMM
PCIe Expansion Slot (per node)	(1) PCIe x16 Gen3 riser slot for Full-height, Half-length card per node (1) PCIe x8 Gen3 OCP mezzanine v1 card slot
Rear IO (per node)	(1) USB 3.0 port (1) GbE or 10G BASE-T RJ45 port
Front IO (per node)	(1) Power Button (1) USB 2.0 port
Network (per node)	Intel I210 Single GbE (1 MACs and 1 PHY Integrated) (Optional) Intel x520 10G / Mellanox CX4-Lx 25G mezzanine card (Optional) QCT 82599ES 10G/ QCT CX3pro 10G mezzanine card
Storage (per node)	(6) 2.5" SATA hot-plug drives (1) M.2 (support 2242 and 2260)
USB (per node)	(1) USB3.0 port on Rear panel (1) USB2.0 port on Front panel (Optional)
Series Port (per node)	(1) Serial port on debug card (Optional)
FAN	2U 4 dual-rotor FAN connectors on FAN board
ACPI	ACPI compliance, S0, S5 support. (* S1 and S3 are not supported.)
TPM (per node)	(1) TPM header, support TPM 1.2

Power-Supply	(2) 1600W high efficiency PSU, 220VAC 50/60Hz
Chassis	2U chassis in 19" EIA rack

Table 2-1 F06S 2U4N System Feature List

2.1.2 System Block Diagram

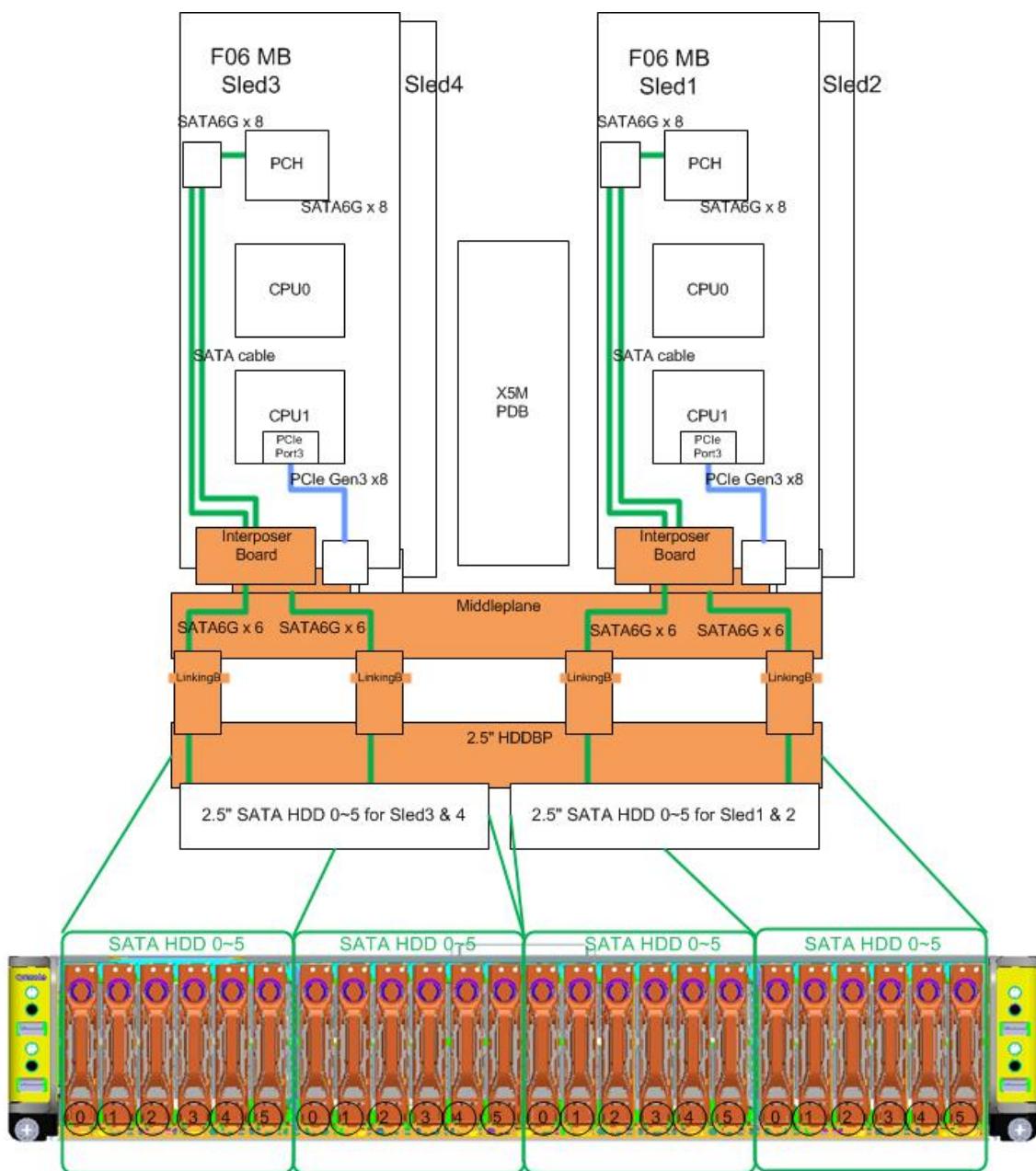


Figure 2-1 F06S 2U4N System Block diagram

2.2 F06T 2U2N System Product Features

2.2.1 Product Features

F06T 2U2N System's ingredients and features are shown as follows.

Board Name	F06T 2U2N System
Form Factor	2U Chassis (Carmel Chassis) 31.1"x17.48"x3.44"(789.94 x 444 x 87.5mm) [LxW xH]
Baseboard size / Quantity	20" x 6.5" (508 x 165mm), 12 layer, 2.16mm / 2 pcs per system
CPU (per node)	(2) Intel® Xeon® processor E5-2600 V3 and V4 family (up to 135W)
Max Processor Wattage	135W, VRD 12.5
QPI Speed	9.6 GT/s, 8.0GT/s, 6.4GT/s
Chipset	Intel® C610 series
Memory (per node)	(16) DDR4 RDIMM slots Up to 256GB (16GB x16) of memory for RDIMM
PCIe Expansion Slot (per node)	(3) PCIe x16 Gen3 riser slot for Full-height, Half-length card (1) PCIe x8 Gen3 OCP mezzanine v1 card slot
Rear IO (per node)	(1) USB 3.0 port (1) GbE or 10G BASE-T RJ45 port
Front IO (per node)	(1) Power Button (1) USB 2.0 port
Network (per node)	I210 Single GbE (1 MACs and 1 PHY Integrated) (Optional) Intel x520 10G / Mellanox CX4-Lx 25G mezzanine card (Optional) QCT 82599ES 10G / QCT CX3pro 10G mezzanine card
Storage (per node)	(12) 2.5" SATA hot-plug drives (2U Chassis) (1) M.2 (support 2242 and 2260)
USB (per node)	(1) USB3.0 port on Rear (1) USB2.0 port on Front panel (Optional)
Series Port (per node)	(1) Serial port on debug bard (Optional)
Fan	2U 4 dual-rotor fan connectors on FAN board
ACPI	ACPI compliance, S0, S5 support. (* S1 and S3 are note supported.)
TPM (per node)	(1) TPM header, support TPM specification 1.2
Power-Supply	(2) 1600W high efficiency PSU, 220VAC 50/60Hz
Chassis	2U chassis in 19" EIA rack

Table 2-2 F06T 2U2N System Feature List

2.2.2 System Block Diagram

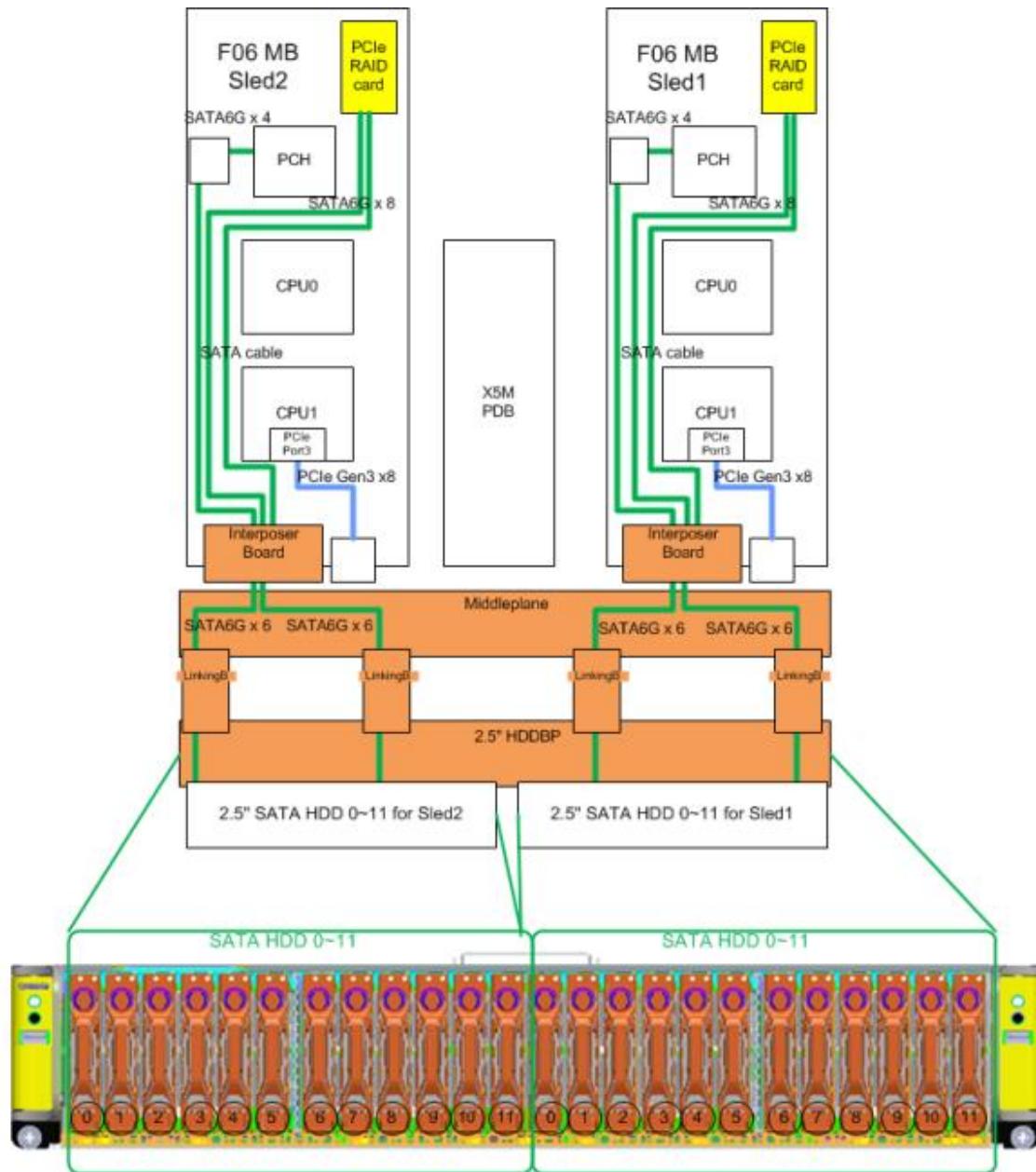


Figure 2-2 F06T 2U2N System Block diagram

2.3 Related Board Placement

2.3.1 Motherboard Placement

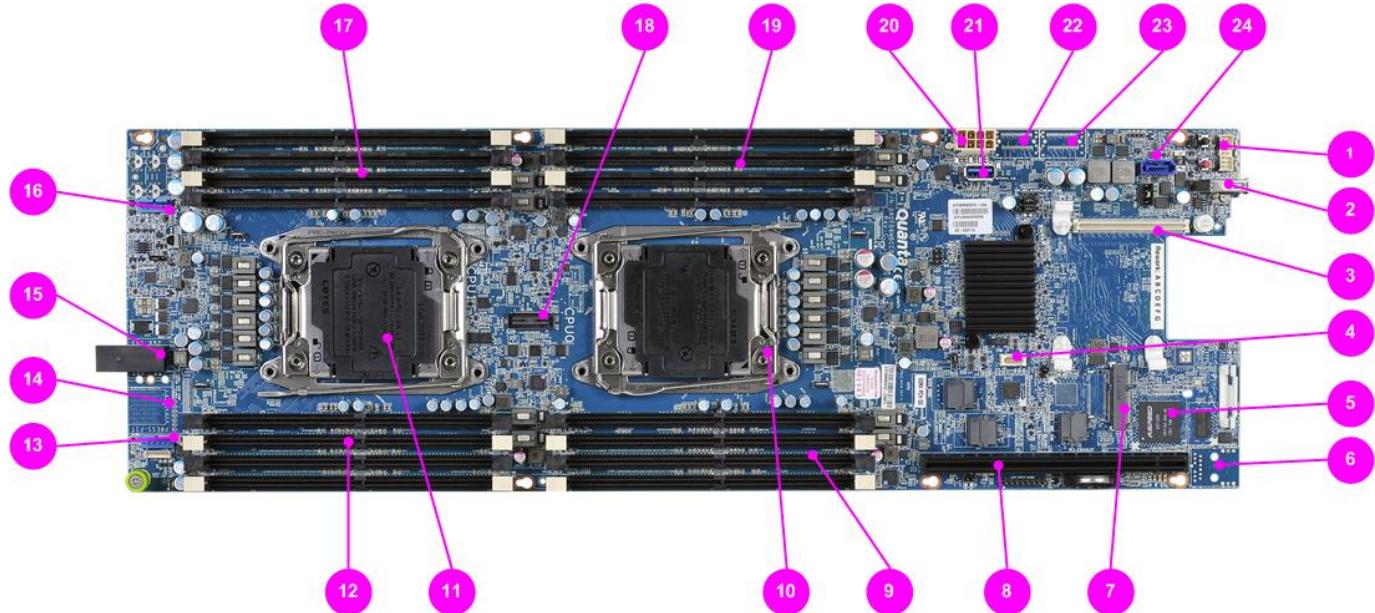


Figure 2-3 F06 OCP motherboard key part placement.

Item	Ref Designator / Silkscreen @PCB	Description
1	J1 / null	Debug port
2	U4 / USB	USB 3.0 connector
3	J6 / MEZZ CONN	OCP Mezzanine v1 connector
4	J12 / TPM	TPM connector
5	U12 / null	AST1250
6	J3 / ETH0	RJ45 for LOM
7	J7 / MSATA CONN	mSATA connector
8	J4B1 / PCI-EX24SLOT	PCIe x24 connector
9	J21,J22,J23,J24 / A7,A6,A5,A4	DIMM slot for CPU0
10	U48 / CPU0	CPU0
11	U64 / CPU1	CPU1
12	J30,J31,J32,J33 / B3,B2,B1,B0	DIMM slot for CPU1
13	J36 / Fan SYS1	FAN connector
14	J39 / B2B CONN	AirMax 3x8 connector
15	J38 / PWR CONN	AirMax Power connector
16	J36 / Fan SYS0	FAN connector
17	J26,J27,J28,J29 / B4,B5,B6,B7	DIMM slot for CPU1
18	J25 / CPU XDP	XDP connector
19	J17,J18,J19,J20 / A0,A1,A2,A3	DIMM slot for CPU0
21	JP9 / HDD_PWR	SATA HDD PWR connector

22	J11 / MINISAS2	Mini-SAS connector
23	J9 / MINISAS1	Mini-SAS connector
24	J5 / SATA	SATA connector

Table 2-2 F06 OCP motherboard key part location list

2.3.2 Interposer Board Placement

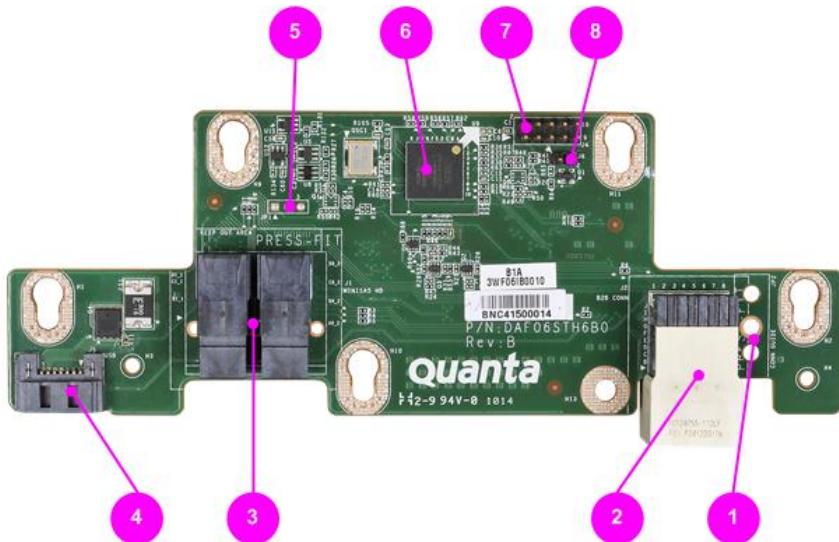


Figure 2-4 Interposer board key part placement

Item	Ref Designator / Silkscreen @PCB	Description
1	JP2 / CONN GUIDE	Guide pin for Middle-plane
2	J2 / B2B CONN	B2B connector for Middle-plane
3	J1 / MINISAS HD	Mini-SAS HD connector for motherboard
4	J5 / USB	USB connector for motherboard
5	JP1 / null	Debug I2C header for AST1250 of motherboard
6	U9 / null	CPLD
7	J4 / null	CPLD programming header
8	J6 / null	CPLD reset header

Table 2-3 Interposer board key part location list

2.4 Related Board Dimension

2.4.1 Sled Dimension

F06S Sled related dimension is 537.86mm (L, 21.17 ") x 173.75mm (W, 6.84") x 40.5mm (H, 1.59").

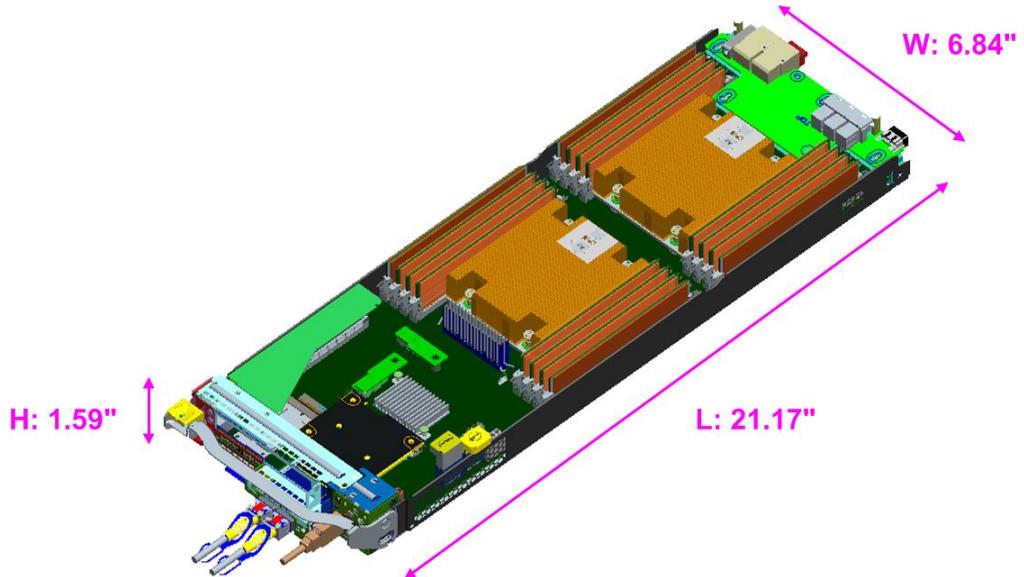


Figure 2-5 F06S Sled dimension

F06T Sled related dimension is 537.86mm (L, 21.17 ") x 173.75mm (W, 6.84") x 81.5mm (H, 3.2").

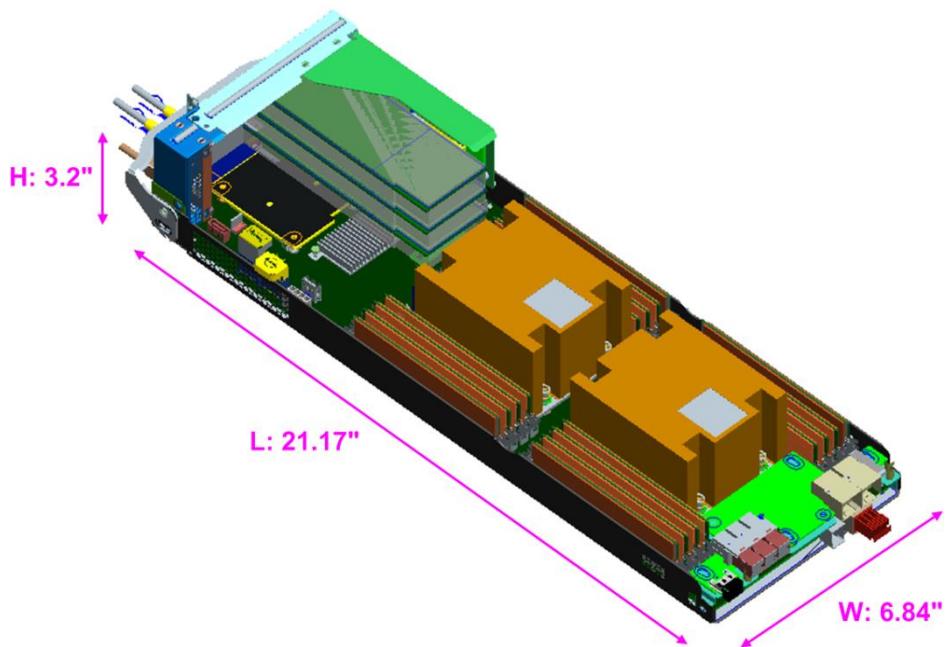


Figure 2-6 F06T Sled dimension

2.4.2 Motherboard Dimension

The Motherboard related dimension is 508mm (L, 20") x 165mm (W, 6.5").

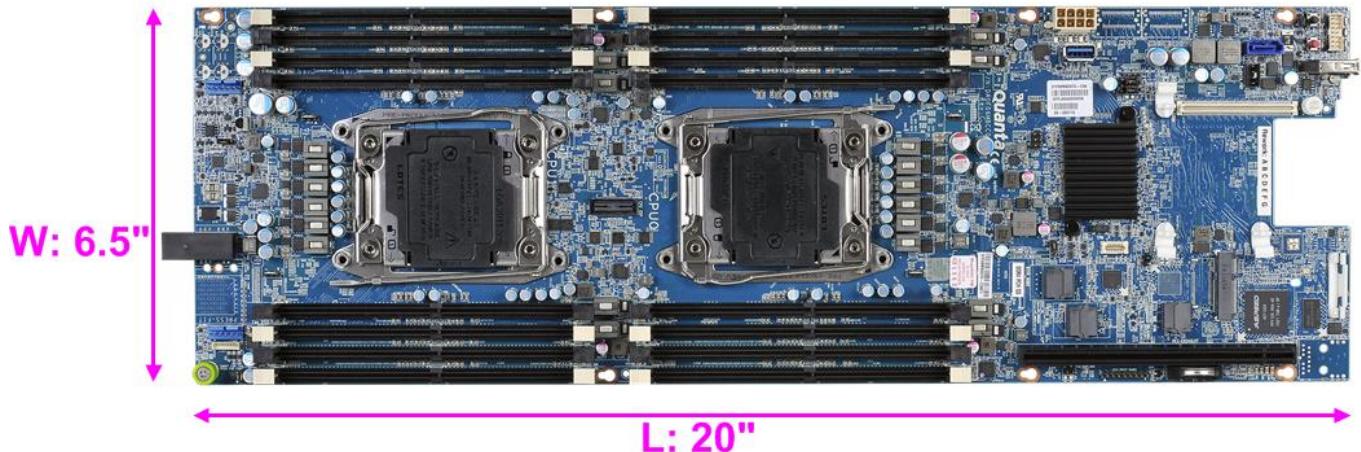


Figure 2-7 F06 OCP motherboard dimension

2.4.3 Interposer Board Dimension

The Interposer board related dimension is 162mm (L, 6.38") x 60mm (W, 2.37")



Figure 2-8 Interposer board dimension

3 PRODUCT FEATURES

3.1 Processor

The processor of Grantley platform is Xeon E5-2600 v3 and v4 (socket LGA2011 R3), the processor has internal voltage regulator (IVR). The key features are as shown below:

- Up to 18 cores (E5-2600 v3), 22 cores (E5-2600 v4)
- Up to 145W TDP
- Up to 10 x 4 PCIe Gen3
- Support 4 channels DDR4 RDIMM/LRDIMM (total 16 DIMMs)
- Single Processor mode is supported.

3.2 Memory

F06 OCP motherboard supports total 16 DDR4 DIMMs. Following is memory support tables for E5-2600 v3 and v4 processors.

E5-2600 v3	2 SPC	
	1 DPC	2 DPC
	1.2V	1.2V
RDIMM SR/DR	2133 MT/s	1866 MT/s
LRDIMM QR	2133 MT/s	2133 MT/s
LRDIMM(3DS)	2133 MT/s	2133 MT/s

E5-2600 v4	2 SPC	
	1 DPC	2 DPC
	1.2V	1.2V
RDIMM SR/DR	2400 MT/s	2133 MT/s
LRDIMM QR	2400 MT/s	2400 MT/s
LRDIMM(3DS)	2400 MT/s	2400 MT/s

3.2.1 DIMM Nomenclature

DIMMs are organized into physical slots on DDR4 memory channels that belong to processor sockets. The memory channels from Socket 0 (CPU-0) are identified as Channel A0~A7. The memory channels from Socket 1 (CPU-1) are identified as Channel B0~B7.

The DIMM identifiers printed on the motherboard provide information about the channel, and therefore the processor, to which they belong. For example, DIMM_A0 is the first slot on Channel A of processor 0. DIMM_B0 is the first DIMM socket on Channel B of processor 1.

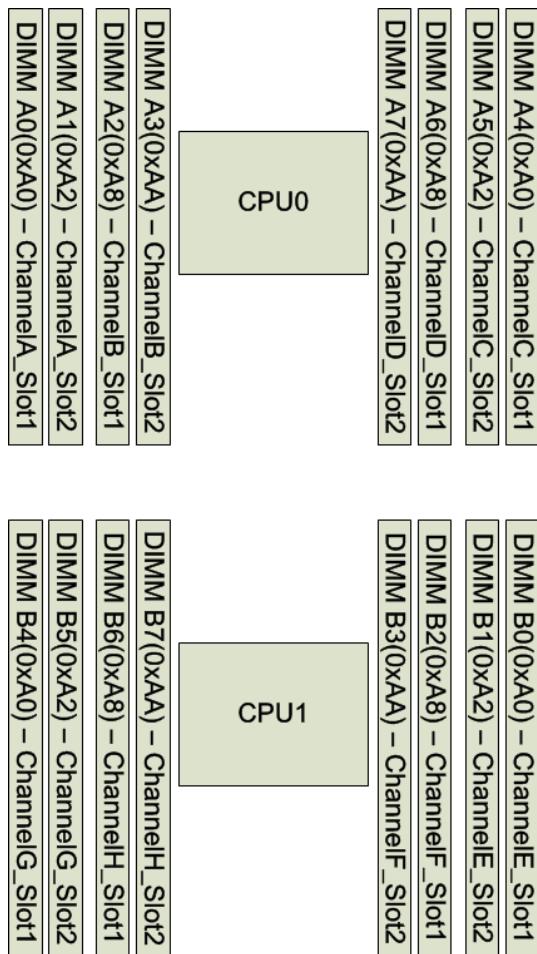


Figure 3-1 F06 2U4N motherboard DIMM nomenclature

3.3 PCH

The PCH of Grantley platform is C610. The key features are as shown below:

- Integrated system clocks w/ support for ext. clock buffers
- 10 SATA ports capable of 6Gb/s
- Up to 6 ports of USB3; 8 ports of USB2
- Up to 8 x1 PCIe Gen2

3.4 BMC

The Board Management Controller of F06 OCP motherboard is adopting ASPEED AST1250 that is a highly integrated single-chip solution, integrating several devices typically found on servers.

3.5 Clocks

The Grantley platform has three different clock architectures, external clock architecture (exCLK), integrated system clock (isCLK) architecture and hybrid architecture. The C610 (PCH) is capable of providing both exCLK and isCLK. F06 OCP motherboard uses isCLK mode. The external clock generator will not be necessary.

3.6 SATA

The C610 (PCH) supports total 10 SATA-III 6Gbs ports. The PCH contains three SATA controller modes, while IDE, ACHI and RAID mode.

The project supports 10 SATAIII ports, while one SATA port connects to 7-pin connector, eight SATA ports connect to two internal mini-SAS connectors for system HDD Back-Plane connection and one SATA port transfer to mSATA connection.

3.6.1 SATA PORT CONNECTIVITY

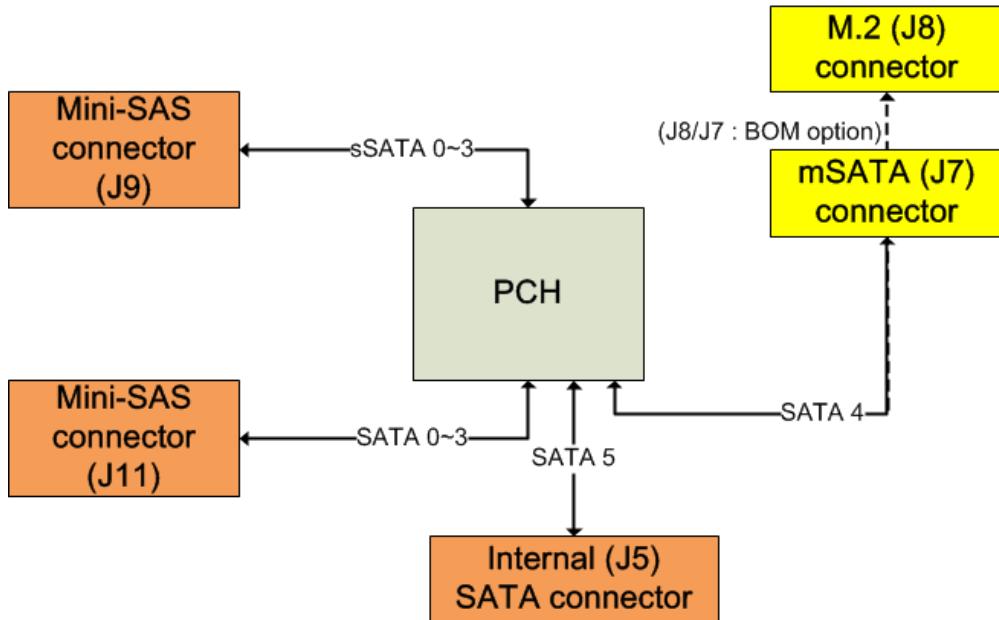


Figure 3-2 F06 OCP motherboard SATA connectivity

3.7 USB

The C610 (PCH) supports total 14 USB ports, 6 USB 2.0 ports and 8 USB 3.0 ports. The USB port distribution is as follows:

- ASPEED BMC AST1250 occupies 2 USB 2.0 ports (one 1.1 and one 2.0-this one is reserved for AST2400, AST1250 won't use USB2.0 channel)
- one Rear USB3.0 port is necessary for this project
- one Front-panel USB2.0 port is optional for 2U chassis

The USB ports on the products are not required to be powered from STBY.

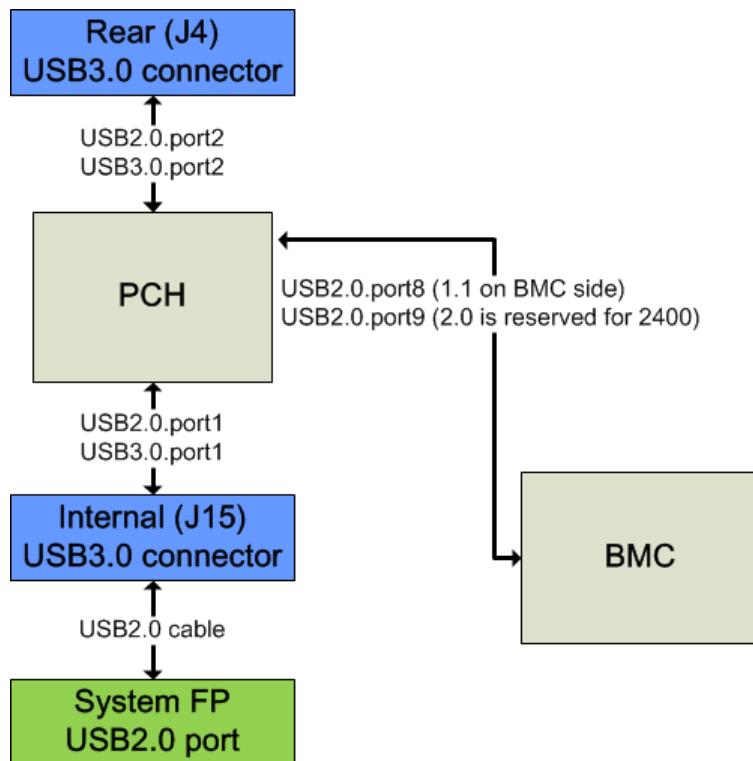


Figure 3-3 F06 OCP motherboard USB connectivity

3.8 PCIe BUS

PCI Express* Gen1, Gen2 and Gen 3 are dual-simplex point-to point serial differential low-voltage interconnects. The signaling bit rate is 2.5 Gbit/s one direction per lane for Gen1 (8b/10b encoding), 5.0 Gb/s one direction per lane for Gen2 (8b/10b encoding) and 8.0 Gb/s one direction per lane for Gen3 (128b/130b encoding). Each port consists of a transmitter and receiver pair. A link between the ports of two devices is a collection of lanes (x1, x2, x4, x8, x16).

3.8.1 PCIe PORT CONNECTIVITY

The following diagram lists the usage of the Intel Xeon E5 v3 and C610 (PCH) PCIe bus segments in F06 2U4N project.

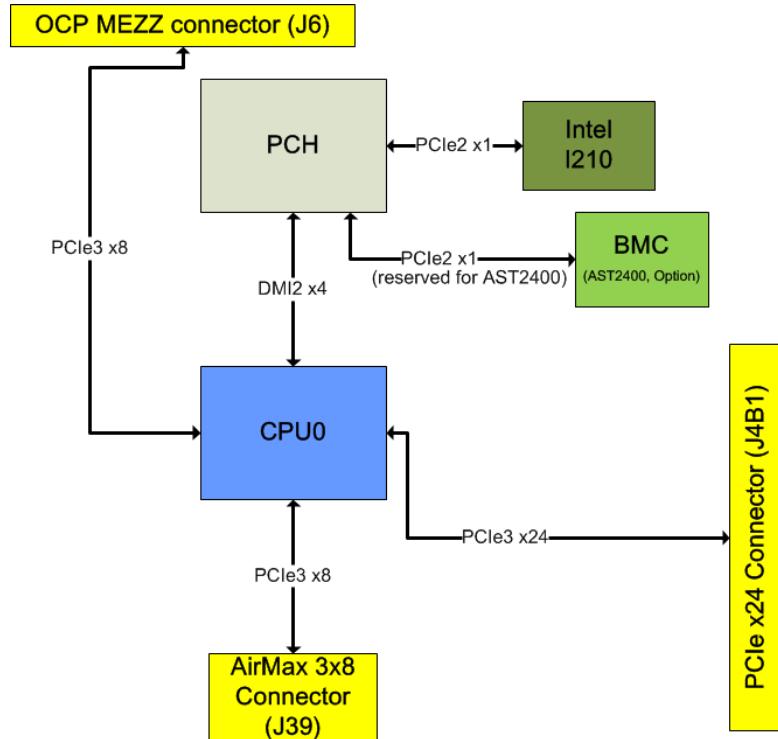


Figure 3-4 F06 OCP motherboard PCIe connectivity

3.9 PCIe Interface

There are two types of Riser boards and Mezzanine board for the system. The follow table lists the details.

Description		
F06S 2U4N System (per node)	PCIe x24 Riser (1U)	(1) PCIe Gen3 x16 Add-on Card support
	OCP Mezzanine	(1) PCIe Gen3 x8 Mezzanine v1 connector (NCSI interface support)
F06T 2U2N System (per node)	PCIe x24 Riser (2U)	(3) PCIe Gen3 x8 Add-on Card support
	OCP Mezzanine	(1) PCIe Gen3 x8 Mezzanine v1 connector (NCSI interface support)

Table 3-1 Riser and Mezzanine list

3.9.1 PCIe Connector PIN Definition

3.9.1.1 PClex24 Riser Slot PIN Definition

Pin	Side B Golden Finger	Side A Golden Finger	Pin
#	Name	Name	#
1	+12v	PRSNT#1	1
2	+12v	+12v	2
3	+12v	+12v	3
4	GND	GND	4
5	SMCLK	REFCLK3+	5
6	SMDAT	REFCLK3-	6
7	GND	GND	7
8	+3.3v	LAN_SMB_DAT	8
9	LAN_SMB_CLK	+3.3v	9
10	3.3Vaux	+3.3v	10
11	WAKE#	PERST#	11

Mechanical Key

12	LAN_SMB_ALERT_N	GND	12
13	GND	REFCLK1+	13
14	PETp(0)	REFCLK1-	14
15	PETn(0)	GND	15
16	GND	PERp(0)	16
17	PRSNT#2-1	PERn(0)	17
18	GND	GND	18
19	PETp(1)	RSVD	19
20	PETn(1)	GND	20
21	GND	PERp(1)	21
22	GND	PERn(1)	22
23	PETp(2)	GND	23
24	PETn(2)	GND	24
25	GND	PERp(2)	25
26	GND	PERn(2)	26
27	PETp(3)	GND	27
28	PETn(3)	GND	28
29	GND	PERp(3)	29

F06S/F06T 2U System Contribution

30	RSVD	PERn(3)	30
31	PRSNT#2-2	GND	31
32	GND	REFCLK2+	32
33	PETp(4)	REFCLK2-	33
34	PETn(4)	GND	34
35	GND	PERp(4)	35
36	GND	PERn(4)	36
37	PETp(5)	GND	37
38	PETn(5)	GND	38
39	GND	PERp(5)	39
40	GND	PERn(5)	40
41	PETp(6)	GND	41
42	PETn(6)	GND	42
43	GND	PERp(6)	43
44	GND	PERn(6)	44
45	PETp(7)	GND	45
46	PETn(7)	GND	46
47	GND	PERp(7)	47
48	PRSNT#2-3	PERn(7)	48
49	GND	GND	49
50	PETp(8)	SLT_CFG0	50
51	PETn(8)	GND	51
52	GND	PERp(8)	52
53	GND	PERn(8)	53
54	PETp(9)	GND	54
55	PETn(9)	GND	55
56	GND	PERp(9)	56
57	GND	PERn(9)	57
58	PETp(10)	GND	58
59	PETn(10)	GND	59
60	GND	PERp(10)	60
61	GND	PERn(10)	61
62	PETp(11)	GND	62
63	PETn(11)	GND	63
64	GND	PERp(11)	64
65	GND	PERn(11)	65

F06S/F06T 2U System Contribution

66	PETp(12)	GND	66
67	PETn(12)	GND	67
68	GND	PERp(12)	68
69	GND	PERn(12)	69
70	PETp(13)	GND	70
71	PETn(13)	GND	71
72	GND	PERp(13)	72
73	GND	PERn(13)	73
74	PETp(14)	GND	74
75	PETn(14)	GND	75
76	GND	PERp(14)	76
77	GND	PERn(14)	77
78	PETp(15)	GND	78
79	PETn(15)	GND	79
80	GND	PERp(15)	80
81	PRSNT#2-4	PERn(15)	81
82	GND	GND	82
83	PETp(16)	SLT_CFG1	83
84	PETn(16)	GND	84
85	GND	PERp(16)	85
86	GND	PERn(16)	86
87	PETp(17)	GND	87
88	PETn(17)	GND	88
89	GND	PERp(17)	89
90	GND	PERn(17)	90
91	PETp(18)	GND	91
92	PETn(18)	GND	92
93	GND	PERp(18)	93
94	GND	PERn(18)	94
95	PETp(19)	GND	95
96	PETn(19)	GND	96
97	GND	PERp(19)	97
98	GND	PERn(19)	98
99	PETp(20)	GND	99
100	PETn(20)	GND	100
101	GND	PERp(20)	101

102	GND	PERn(20)	102
103	PETp(21)	GND	103
104	PETn(21)	GND	104
105	GND	PERp(21)	105
106	GND	PERn(21)	106
107	PETp(22)	GND	107
108	PETn(22)	GND	108
109	GND	PERp(22)	109
110	GND	PERn(22)	110
111	PETp(23)	GND	111
112	PETn(23)	GND	112
113	GND	PERp(23)	113
114	PRSNT#2-5	PERn(23)	114
115	PRSNT#2-6	GND	115

Table 3-2 PIN definition of PCIe x24 Riser slot

3.9.1.2 OCP Mezzanine v1 Connector PIN Definition

Pin	Pin description	Pin	Pin description
#	Name	#	Name
61	P12V_PSU	1	MEZZ_PRSNT_N
62	P12V_PSU	2	P5V_AUX
63	P12V_PSU	3	P5V_AUX
64	GND	4	P5V_AUX
65	GND	5	GND
66	P3V3_AUX	6	GND
67	GND	7	P3V3_AUX
68	GND	8	GND
69	P3V3	9	GND
70	P3V3	10	P3V3
71	P3V3	11	P3V3
72	P3V3	12	P3V3
73	GND	13	P3V3
74	PCIE0_SMB_ALERT_N Z	14	RMII_MEZZ_NIC_CRS

75	SMB_MEZZ_NIC1_CLK	15	CLK_50M_LAN_RMII
76	SMB_MEZZ_NIC1_DAT	16	RMII_IBMC_NIC_TX_EN_S
77	MEZZ_WAKE_N	17	RST_PERST0_N
78	RMII_IBMC_NIC_RX_ER_S	18	SMB_MEZZ_NIC2_CLK
79	GND	19	SMB_MEZZ_NIC2_DAT
80	RMII_IBMC_NIC_TXD0_S	20	GND
81	RMII_IBMC_NIC_TXD1_S	21	GND
82	GND	22	RMII_MEZZ_NIC_RXD0
83	GND	23	RMII_MEZZ_NIC_RXD1
84	CLK_100M_PE3_DP	24	GND
85	CLK_100M_PE3_DN	25	GND
86	GND	26	CLK_100M_10G_MEZZA_DP
87	GND	27	CLK_100M_10G_MEZZA_DN
88	P3E_CPU0_PCIE3_TX_C_DP8	28	GND
89	P3E_CPU0_PCIE3_TX_C_DN8	29	GND
90	GND	30	P3E_CPU0_PCIE3_RX_DP8
91	GND	31	P3E_CPU0_PCIE3_RX_DN8
92	P3E_CPU0_PCIE3_TX_C_DP9	32	GND
93	P3E_CPU0_PCIE3_TX_C_DN9	33	GND
94	GND	34	P3E_CPU0_PCIE3_RX_DP9
95	GND	35	P3E_CPU0_PCIE3_RX_DN9
96	P3E_CPU0_PCIE3_TX_C_DP10	36	GND
97	P3E_CPU0_PCIE3_TX_C_DN10	37	GND
98	GND	38	P3E_CPU0_PCIE3_RX_DP10
99	GND	39	P3E_CPU0_PCIE3_RX_DN10
100	P3E_CPU0_PCIE3_TX_C_DP11	40	GND
101	P3E_CPU0_PCIE3_TX_C_DN11	41	GND
102	GND	42	P3E_CPU0_PCIE3_RX_DP11
103	GND	43	P3E_CPU0_PCIE3_RX_DN11
104	P3E_CPU0_PCIE3_TX_C_DP12	44	GND
105	P3E_CPU0_PCIE3_TX_C_DN12	45	GND
106	GND	46	P3E_CPU0_PCIE3_RX_DP12

107	GND	47	P3E_CPU0_PCIE3_RX_DN12
108	P3E_CPU0_PCIE3_TX_C_DP13	48	GND
109	P3E_CPU0_PCIE3_TX_C_DN13	49	GND
110	GND	50	P3E_CPU0_PCIE3_RX_DP13
111	GND	51	P3E_CPU0_PCIE3_RX_DN13
112	P3E_CPU0_PCIE3_TX_C_DP14	52	GND
113	P3E_CPU0_PCIE3_TX_C_DN14	53	GND
114	GND	54	P3E_CPU0_PCIE3_RX_DP14
115	GND	55	P3E_CPU0_PCIE3_RX_DN14
116	P3E_CPU0_PCIE3_TX_C_DP15	56	GND
117	P3E_CPU0_PCIE3_TX_C_DN15	57	GND
118	GND	58	P3E_CPU0_PCIE3_RX_DP15
119	GND	59	P3E_CPU0_PCIE3_RX_DN15
120	MEZZA_PRSNT_N	60	GND

Table 3-3 PIN definition of OCP Mezzanine connector

3.10 LAN on Motherboard (LOM)

F06 OCP motherboard's networking is powered by the Intel I210 Single 10/100/1000 integrated MAC and PHY controller. Intel I210 requires a PCIe x1 Gen2 upstream interface. Intel I210 also requires the use of the C610 (PCH) SMBus interface during Sleep states S5 as well as for ME Firmware. Intel I210 will be on standby power so that Wake on LAN and manageability functions can be supported. Intel I210 will be used in conjunction with the BMC for out of band Management traffic. The BMC will communicate with Intel I210 over a NC-SI interface (RMII physical). Intel I210 will be on standby power so that the BMC can send management traffic over the NC-SI interface to the network during sleep states S5.

3.11 Share-NIC (BMC management port)

BMC of motherboard is able to support Share-NIC for either direction up to 1Mb/s when using SMBus and 100 Mb/s for the NCSI (Network Controller Sideband Interface) interface, which enables the connection of a Baseboard Management Controller (BMC) to a set of Network Interface Controller (NICs) in server computer systems for the purpose of enabling out-of-band remote manageability.

When working over PCIe bus, the bandwidth is limited by the PCIe bandwidth and the I210 processing capabilities.

3.12 LPC BUS

The PCH implements an LPC interface as described in the Low Pin Count Interface Specification, Revision 1.1. The PCH LPC bus is used to connect to the BMC and to an optional TPM device.

3.13 TPM

The PCH supports TPM specification 1.2 level2 revisions 103. The F06 OCP motherboard provides an interface (connector J12), so you can plug TPM module into this interface for security request.

3.14 Serial port

A debug card defined in “Facebook Server Intel motherboard V3.1” specification is installed to motherboard through a debug header(J1) and it provides one UART serial port, two 7-segment LED displays, one reset button, and one UART channel selection button. UART interface provides a host console redirection and BMC debug console. UART channel selection button sends negative pulse to motherboard to select and rotate UART console in a loop of (host console->BMC debug console-> host console...so on). Default console channel is on host.

3.15 Fans

F06 OCP motherboard supports 2 fans. But system is adopting Fan Board to support 4 dual-rotor fans. The fan control and fan speed monitor are from BMC chip. BMC will have Fan Tachometer and PWM function. Note that all fans will operate at the same speed.

3.16 Jumper Definition

Below table is Jumper definition of F06 OCP motherboard.

JUMPER	LOCATION	DEFAULT SETTING.	FUNCTION
ME debug header	JP3	Pin1 Pin3	Pin1: Smb_Host_3V3sb_Clk Pin3: Smb_Host_3V3sb_Dat
ME FIRMWARE UPDATE	JP4	1-2	1-2 : HOLD (DEFAULT) 2-3 : ME IN FORCE UPDATE MODE
RECOVER BIOS JUMPER	JP5	1-2	1-2 : HOLD (DEFAULT) 2-3 : RECOVER BIOS
SMB_SML0 debug header	JP7	Pin1 Pin3	Pin1: Smb_Sml0_3V3sb_Clk Pin3: Smb_Sml0_3V3sb_Dat
Debug port Voltage selection	JP1	1-2	1-2 : P5V (DEFAULT) 2-3 : P5V_AUX
CLR RTC_RST	JP10	1-2	1-2 : HOLD (DEFAULT) 2-3 : CLR RTC_RST
VR Debug header	PJP1	Pin1 Pin2	Pin1: SMB_3V3SB_VR12_CLK Pin2: SMB_3V3SB_VR12_DAT

BMC Disable/Enable	J10	1-2	Open: HOLD (DEFAULT) 1-2: Disable BMC
CPLD update header	JP8	Pin1~8	CPLD JTAG update header
HSC OCP header	JP15	2-3	1-2: 33A / 420W 2-3: 46A / 587W (Default)
MB Mate header	J34	Close	Close: For F06 MB Open: For F06C MB

Table 3-4 BIOS/BMC Jumpers Setting

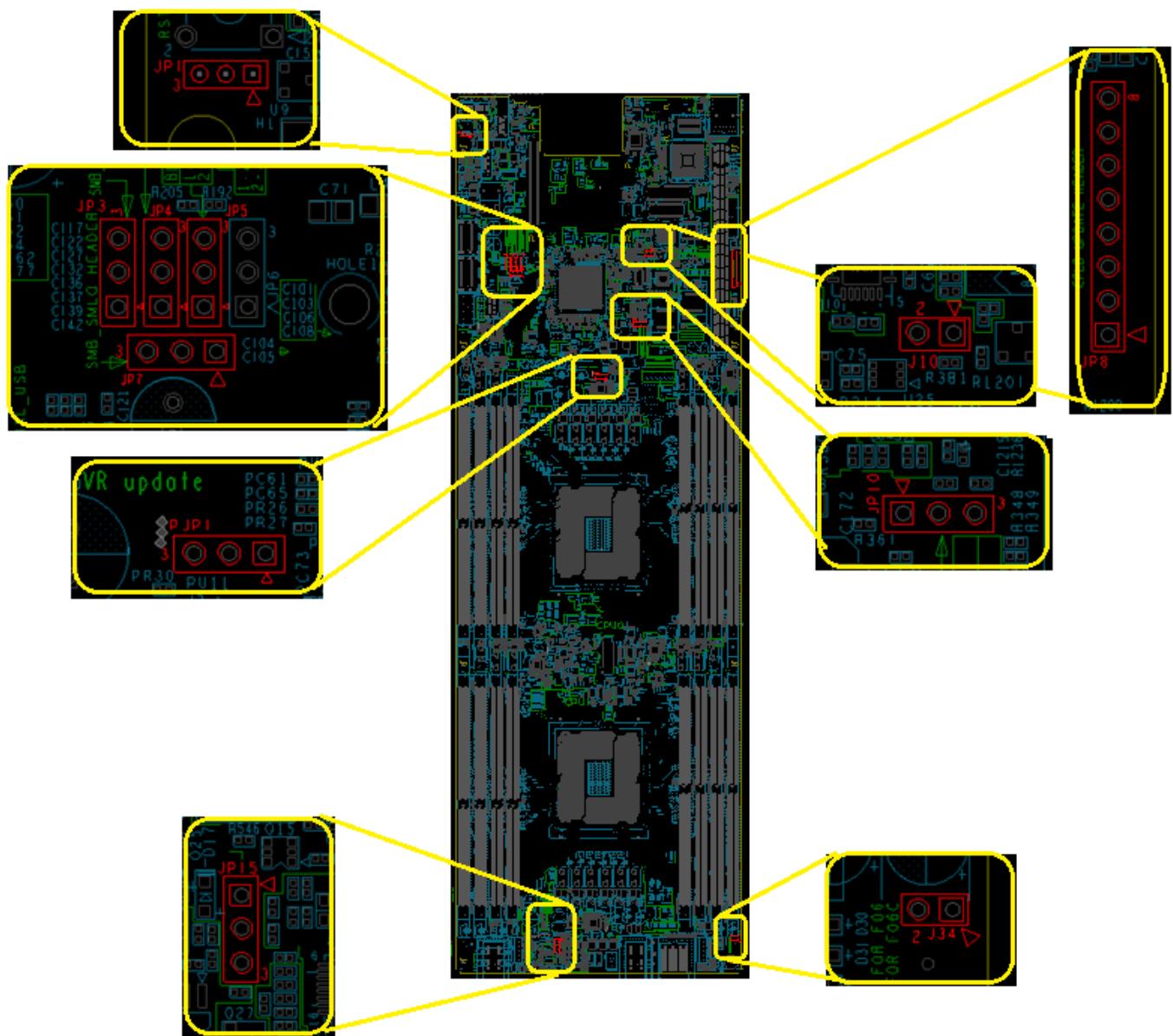


Figure 3-5 Jumper Location

3.17 Debug header Information

3.17.1 XDP Support

Standard XDP header mounted on F06 OCP motherboard for Intel Xeon E5 v3 processors (XDP) will be depopulated after production.

3.17.2 SMB Debug Header (JP7)

SMB Debug Header is a SMB debug header which is connected to PCH's HOST channel and BMC SMB channel 4.

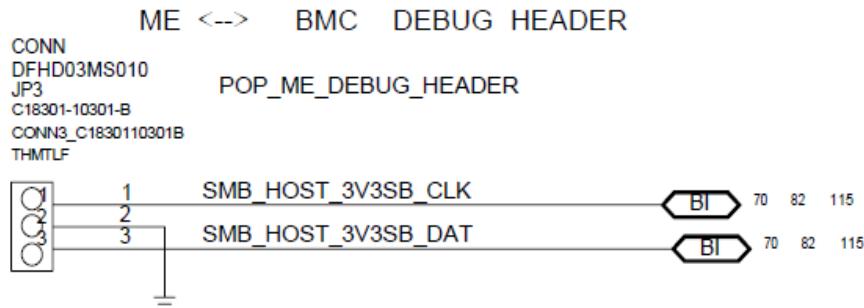


Figure 3-6 F06 OCP motherboard SMB debug Header

3.17.3 BMC Debug Header (J1 and J10)

F06 OCP motherboard provides an interface to monitor BMC and host console by debug board, you need to plug debug board into J1 of motherboard, then press channel SW button to select BMC or Host.

You can disable BMC from J10 for specific usage.

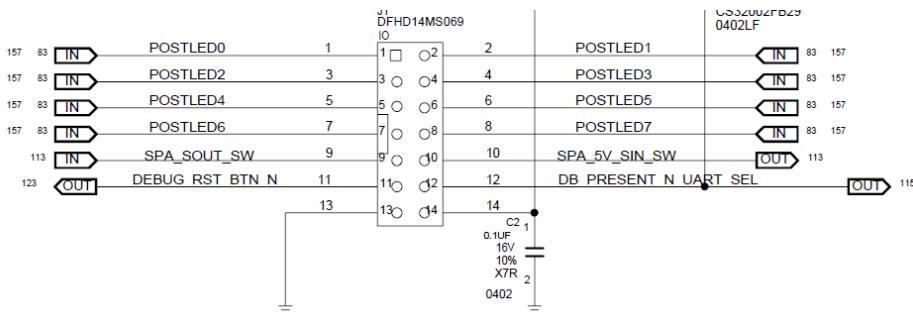


Figure 3-7 F06 OCP motherboard BMC debug header

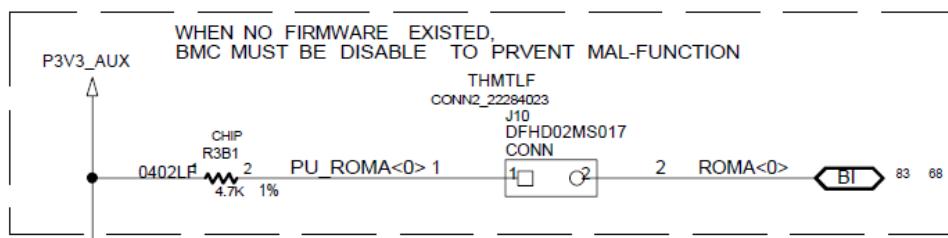


Figure 3-8 F06 OCP motherboard BMC Disable header

3.18 Product Sensors

Sensor	Description
TMP75 (U65,Q25)	Inlet temperature sensor under F06S / F06T System
TMP75 (U1,Q2)	Outlet temperature sensor under F06S / F06T System
AST1250 (BMC)	Monitor CPU / System voltage and temperature

Table 3-5 F06S OCP motherboard sensor list

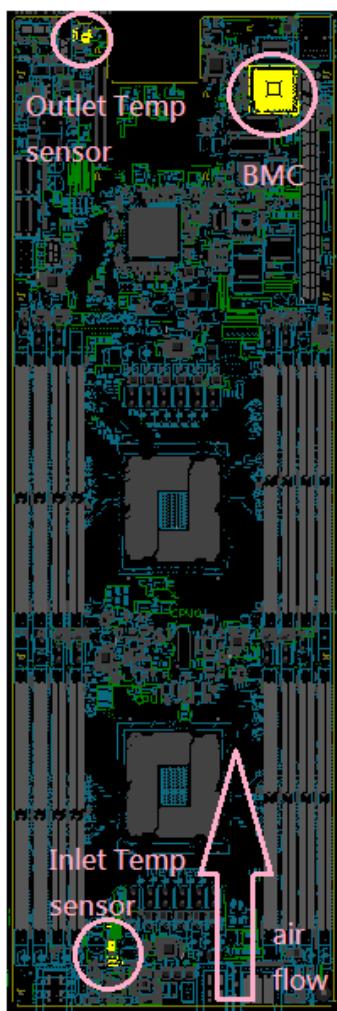


Figure 3-9 Sensors location (air flow direction)

3.19 SMBus

The products must comply with the Intel Xeon E5 v3 platform SMBus architecture. This is a requirement in order to minimize BIOS / Firmware code development efforts and improve product board stability and debugging.

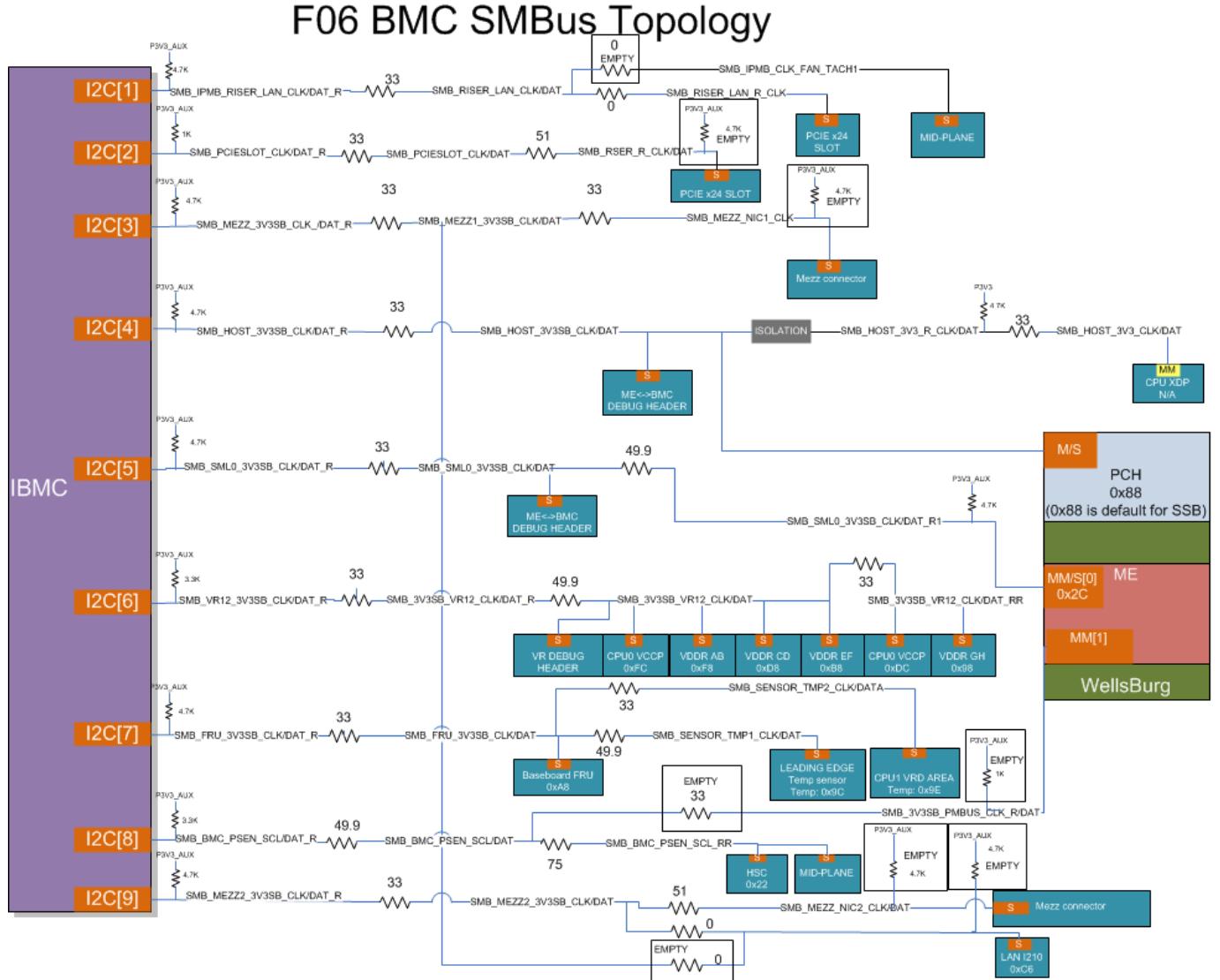


Figure 3-10 F06 OCP motherboard BMC SMBus Block Diagram

3.20 Power Consumption

These are max values (where available) for board VR design purposes and system. TDP power estimate for the main components are provided in below table.

F06S 2U/4N	Qty	Key component TDP	Power efficiency	Utilization	Watts(W)
BASEBOARD	4	350	90	90	1400.00
2.5" HDD	24	8.6	90	80	183.47
FAN	4	57.6	90	80	204.80
Addon card	4	25	80	50	62.50
System total power (Max)				100%	1850.77

Table 3-6 F06S 2U4N System power consumption

F06T	Qty	Key component TDP	Power efficiency	Utilization	Watts(W)
BASEBOARD	2	380	90	90	760.00
2.5" HDD	24	8.6	90	80	183.47
FAN	4	57.6	90	80	204.80
Addon card	6	25	80	50	93.75
System total power (Max)				100%	1242.02

Table 3-7 F06T 2U2N System power consumption

3.20.1 Power Supply PINOUT

F06 motherboard Power Connector (J38)			
Name	PIN		Name
P12V_MB	A1	B1	P12V_MB
P12V_MB	A2	B2	P12V_MB
P12V_MB	A3	B3	P12V_MB
GND	D1	C1	GND
GND	D2	C2	GND
GND	D3	C3	GND

Table 3-8 PIN definition of Power connector (J38)

3.21 LED Definition

3.21.1 HDD Active LED

Location D3



LED Status	LED COLOR	Description	Silk Screen Label
Off	N/A	No access	HDD
Blink	Green	Hard drive activity. This LED shall illuminate when there is activity on the motherboards SATA hard drive interfaces, or on-board mSATA and NGFF connector interface.	

3.21.2 Power+ID LED

Location D2

LED Status	LED COLOR	Description	Silk Screen Label
Off	N/A	No access	PWR
ON	Blue	Power LED. This LED shall have the same functionality of a traditional PC power LED. It shall only illuminate if the motherboard is in the power on state.	

3.21.3 Beep LED

Location D1

Silkscreen: BEEP

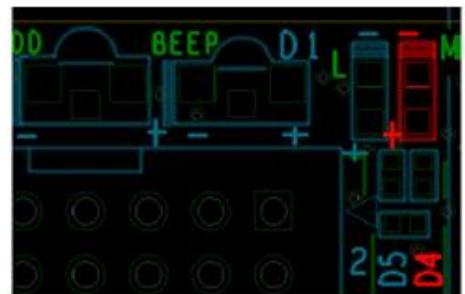
This LED replaces the functionality of the PC speaker. The motherboard shall cause the LED to light to illuminate for the same duration and sequence as the PC speaker would normally beep. The LED allows easier diagnosis in a noisy data center environment.

Error Description				LED Patterns			
PEI memory error	On (2s)	Off (0.25s)	On (2s)	Off (0.25s)	On (2s)	Off (3s)	...(repeat)
PEI DXE not found	On (2s)	Off (0.25s)	On (2s)	Off (0.25s)	On (0.25s)	Off (3s)	...(repeat)
DXE No Console	On (0.25s)	Off (0.25s)	On (0.25s)	Off (0.25s)	On (2s)	Off (3s)	...(repeat)
DXE flash update fail	On (2s)	Off (0.25s)	On (0.25s)	Off (0.25s)	On (0.25s)	Off (3s)	...(repeat)
DXE PCI requirement not met	On (0.25s)	Off (0.25s)	On (0.25s)	Off (0.25s)	On (0.25s)	Off (3s)	...(repeat)

3.21.4 Debug Port Switch and LED

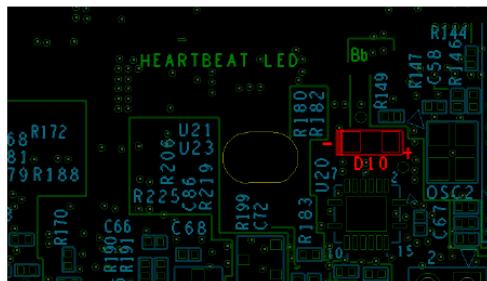
UART Debug port switch selection mode.

MSB UARTSW_MSB_N	YELLOW D4	LSB UARTSW_LSB_N	GREEN D5	DEBUG HEADER
0		0		HOST UART (DEFAULT) (LOCAL)
0		1		BMC DEBUG UART
1		0		MIDPLANE UART



3.21.5 BMC Heart beat LED

Location D10



4 PRODUCT SYSTEM REQUIREMENTS

F06S is at 2U height with 4x hot-plug Sleds and F06T is with 2x hot-plug Sleds. The Chassis will be enabled to complement the board offering and accommodate the marketing requirements of sled with 4 F06S sleds, peripheral boards, HDDs, FANs & PSUs.



Figure 4-1 Chassis Outline Dimension

4.1 F06S 2U4N System View

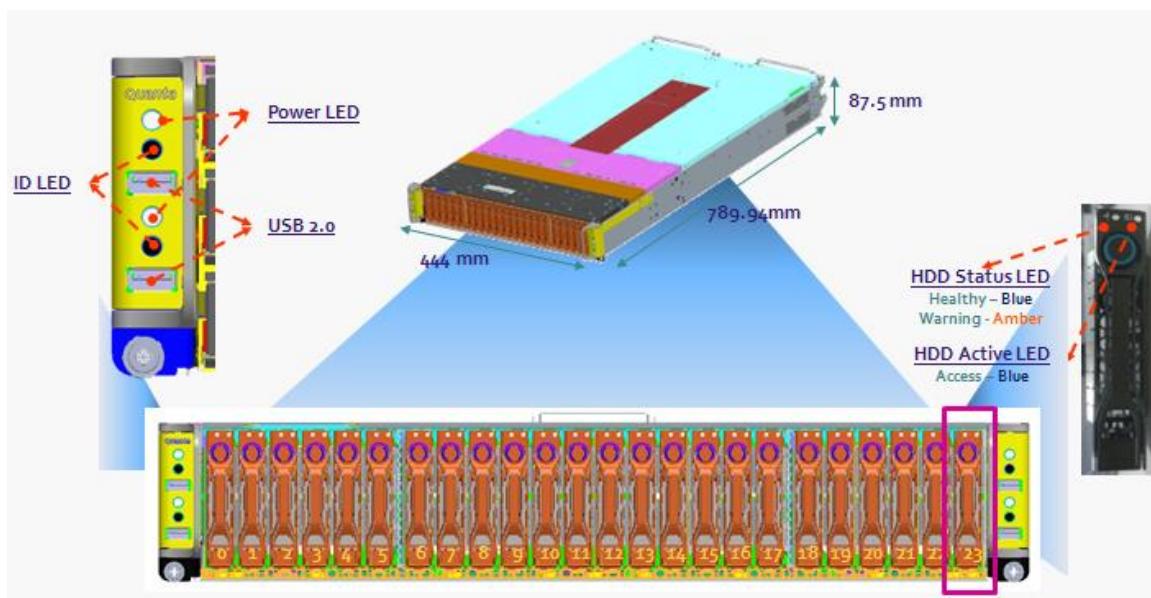


Figure 4-2 F06S 2U4N system Front View

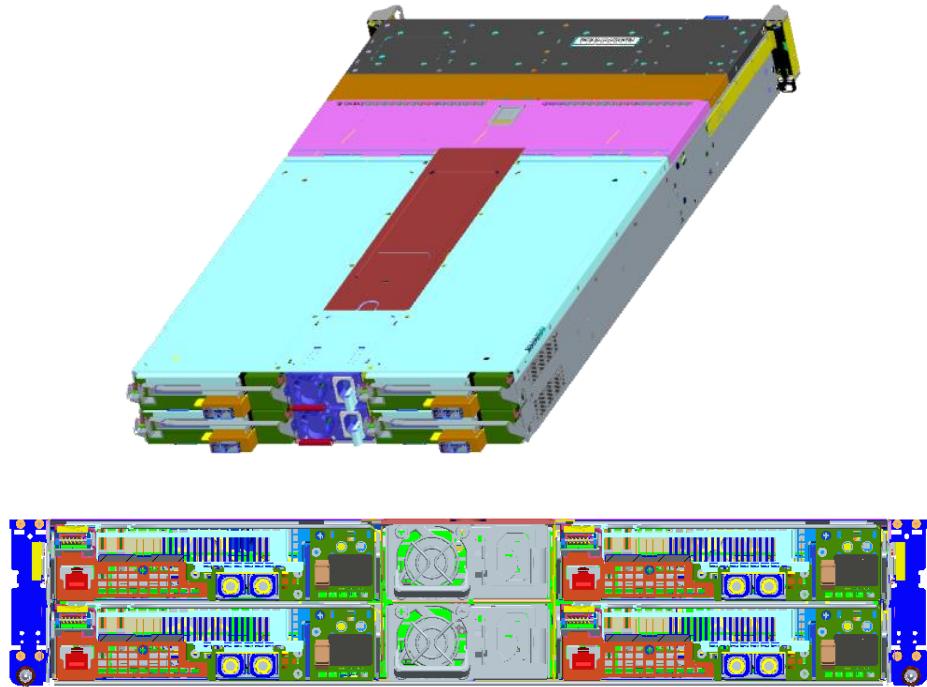


Figure 4-3 F06S 2U4N system Rear View

4.2 F06T 2U2N System View

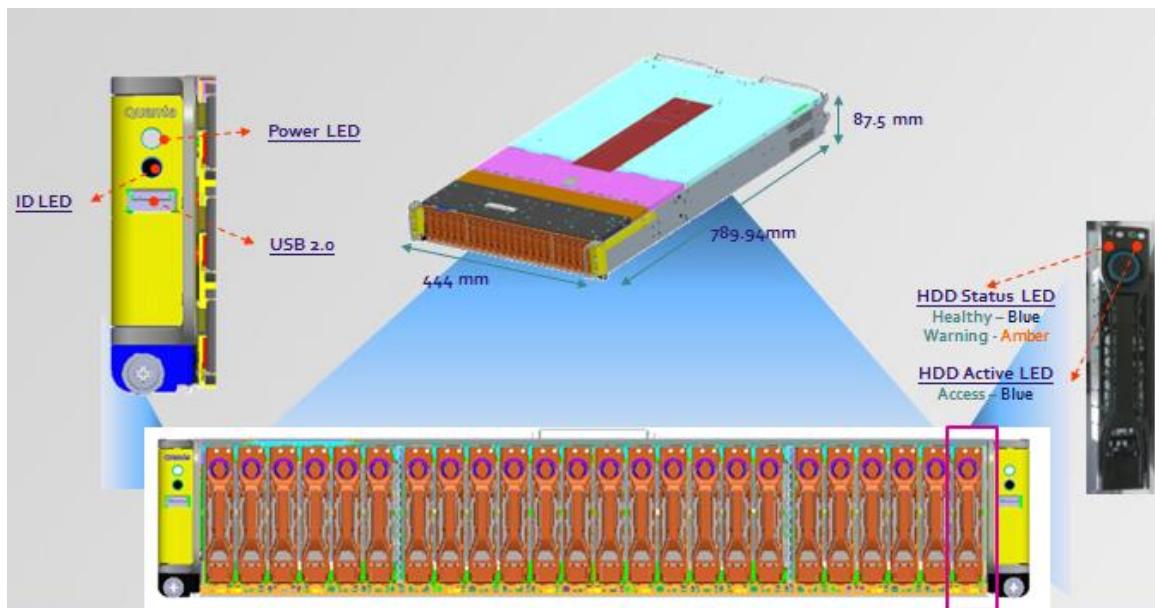


Figure 4-4 F06T 2U2N System Front View

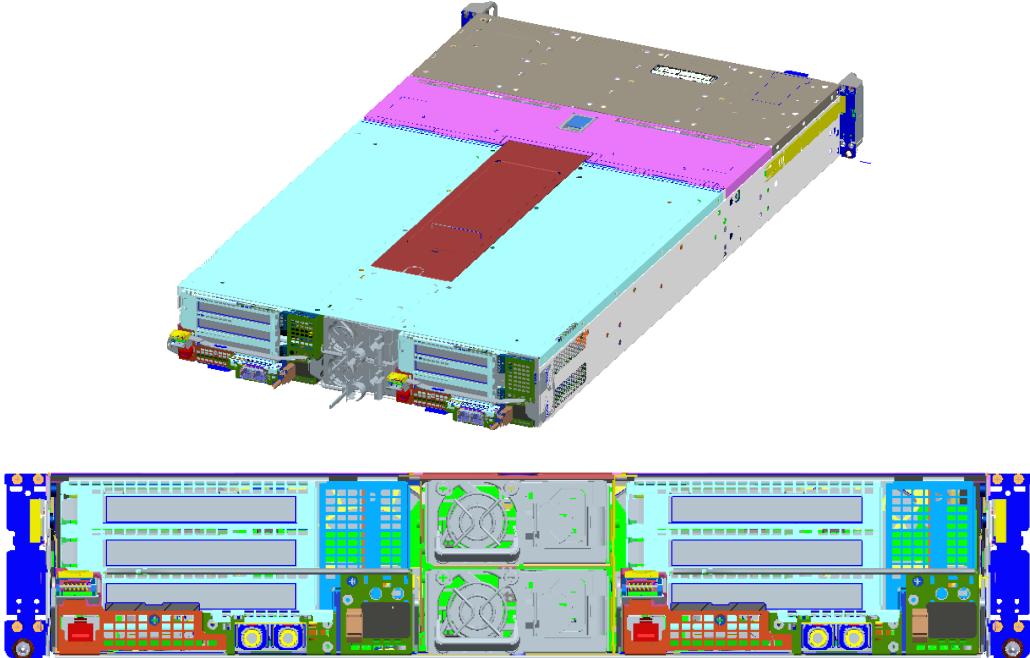


Figure 4-5 F06T 2U2N System Rear View

4.3 System BIOS and BMC Firmware

The system BIOS and BMC FW are third party proprietary and will come with binary format along with F06S / F06T system. System BMC firmware is optional to use open BMC from Facebook or AMI based code upon the feedback from OCP community.

4.4 Environmental Requirements

The system meets the following environmental requirements:

- Ambient operating temperature range: 0C to + 35C
- Operating and Storage relative humidity: 10% to 85% (non-condensing)
- Storage temperature range: - 40C to + 65C
- Transportation temperature range: - 40C to + 70C (short-term storage)
- Operating altitude with no de-ratings: 3200m (about 10656ft)

4.5 Power Supply Unit

The Chassis supports PSU type as below:

- Two 1600W high efficiency PSUs ,220V AC 50/60Hz

Number	Color	Display Status	Description
1	Green	On	Normal operation
	Amber	On	Fault and Stop DC output
	Green	Alternate blinking	Fault and keep DC output

Table 4-1 LED behavior of PSU

4.6 Fan

Four dual-rotor & Hot swap 80mmx 56mm variable-speed Fans to meet the requirement of air-flow 125cfm for F06S system configurations. Fan signals are made available via a consolidated header on Fan board and The Fan control and Fan speed monitor are by chassis management controller: H8 on PDB.

4.7 Front Panel LED Function and Behavior

Table below for the Buttons/LEDs definition in the front side of the chassis

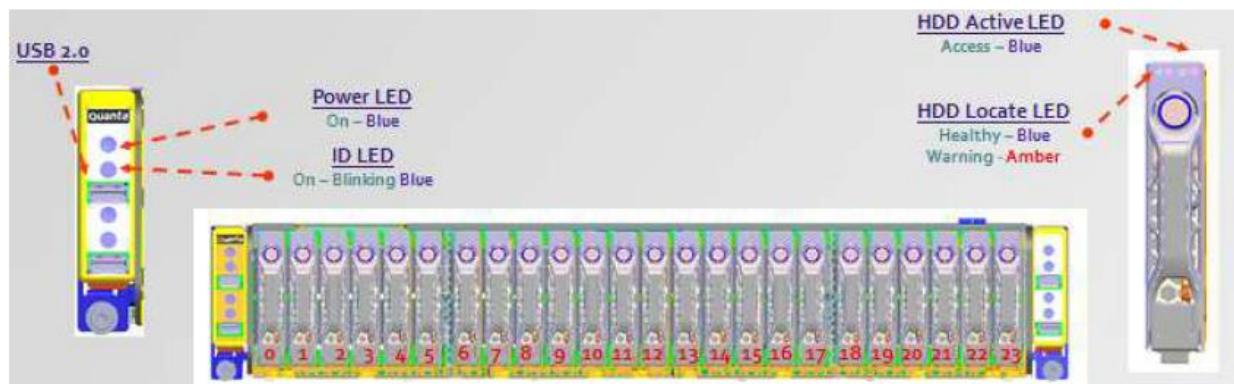


Figure 4-6 Front side LED

Chassis: X5M	Color	Display Status	Description
Front Panel Power Button LED	Blue	ON	DC On
	OFF		DC Off
	Amber	Blinking	DC Off and fault
	Blue	Amber	Alternate blinking
Front Panel ID Button LED	Blue	Blinking	Selected mode
	OFF		Normal mode
	ON		Identify module by BMC Web UI
Sled ID LED (Rear)	Blue	Blinking	Identify module by ID button / BMC WebUI
	Off		Normal mode
	ON		Identify module by BMC Web UI
HDD LED (MG9094 behavior)	Locate	Blue	ON
	Amber	ON	Warning
	Active	Blue	ON
		OFF	HDD not accessing

Table 4-2 Front side LED definition

4.8 Regulatory Compliance Specifications

Planned safety and Electromagnetic Compatibility (EMC) certification are listed below but may be changed upon the feedback from OCP community.

USA	UL 60950-1, 2nd Edition CSA C22.2 No. 60950-1-07, 2nd Edition
CB Scheme	CB Certificate and Report to IEC 60950-1:2005, Second Edition and/or EN 60950-1: 2006
Taiwan	BSMI CNS14336(94)

Table 4-3 Safety Certification List

USA	FCC Part 15 subpart B, Class A
Europe	EMC Directive, 2004/108/EC EN55022:2007 Class A Limit, Radiated & Conducted Emissions EN61000-3-2:2006, EN 61000-3-3:2005 EN55024:2003, Immunity Standard for Information Technology Equipment
Japan	VCCI V-3 2009.04 Class A ITE
Korea	KN22 Class A, KN24
Taiwan	BSMI CNS 13438 Class A

Table 4-4 EMC Certification List