MiTAC Capri 2S Server

Rev 0.1

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Revision History

Date	Name	Description
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1. Scope & Overview

Scope:

This document defines the technical specifications for the MiTAC E8020 used in Open Compute Project Capri 2S Server.

Overview:

MiTAC E8020 2S Server (Capri) is a highly optimized OCP system. This product follows the same form factor as Facebook Tioga Pass product and based on AMD EPYC™ 7002 Serial (Rome) product family CPU architecture and 7003 (Milan) CPU. It supports up to 8 DIMMs.

MiTAC E8020 2S Server (Capri) has two models for customers to choose depending on the drive type, **Advanced sku** has 6 SATA SSD (in the front) with 6 NVMe SSD (internal); while **Ultra sku** supports 10 NVMe SSD (4 in front and 6 internal).

2. Rack Compatibility

MiTAC E8020 2S Server (Capri) system is designed to work with Open Rack V2 (Orv2) structure.

3. Physical Specifications

3.1 Block Diagram

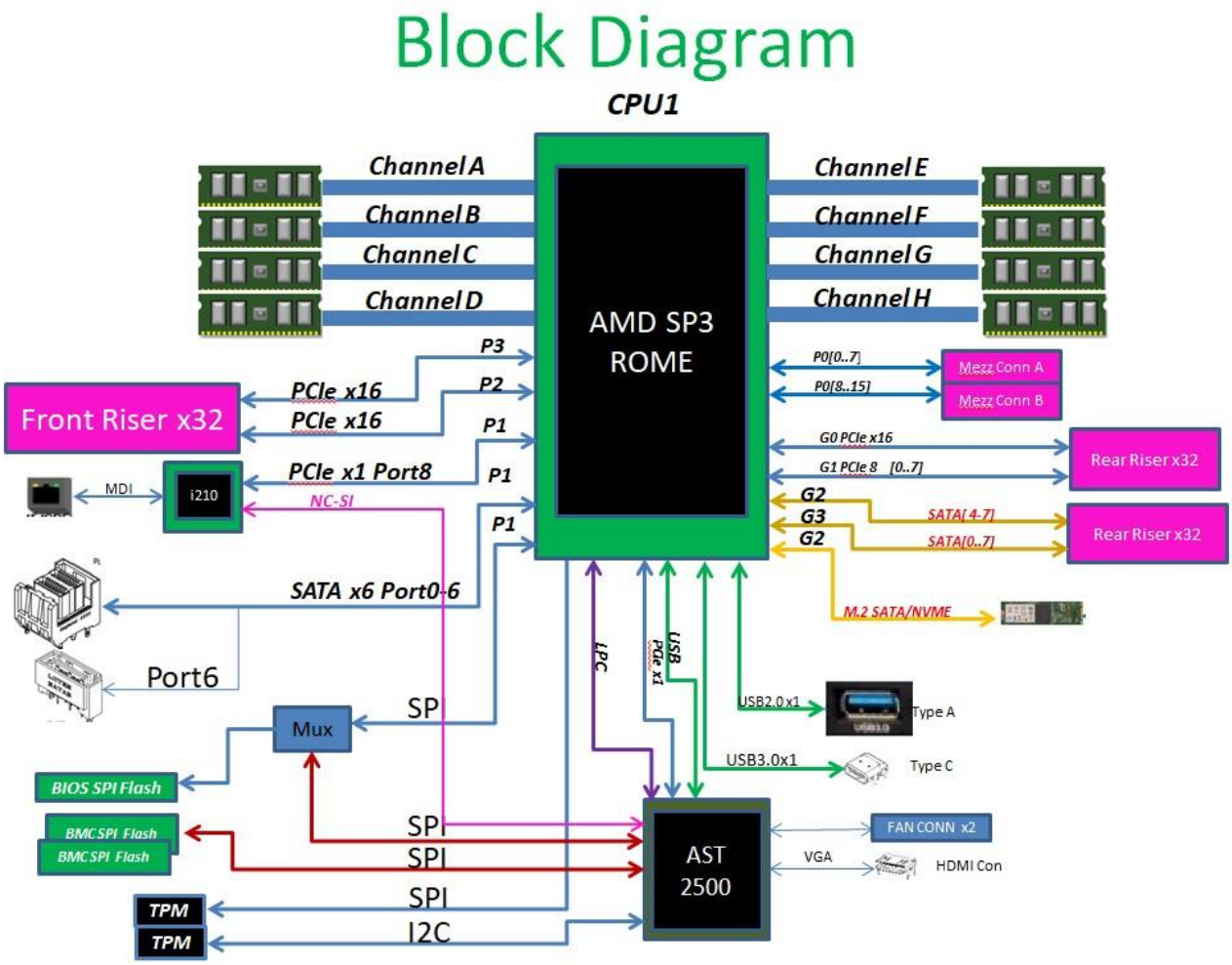


Figure 1 MiTAC E8020 2S Server (Capri) Block Diagram

3.2 Placement and Form Factor

MiTAC E8020 2S Server (Capri) dimension is 28.46” x 6.87” x 3.5” (723 x 174.5 x 89mm); this is compatible with Cubby (2OU 3NODES) chassis. For easy understanding, MiTAC E8020 2S Server (Capri) is having the same form factor as Facebook Tioga Pass. The sled applied on both Tioga Pass and Capri are the same, only the motherboard on it are different.

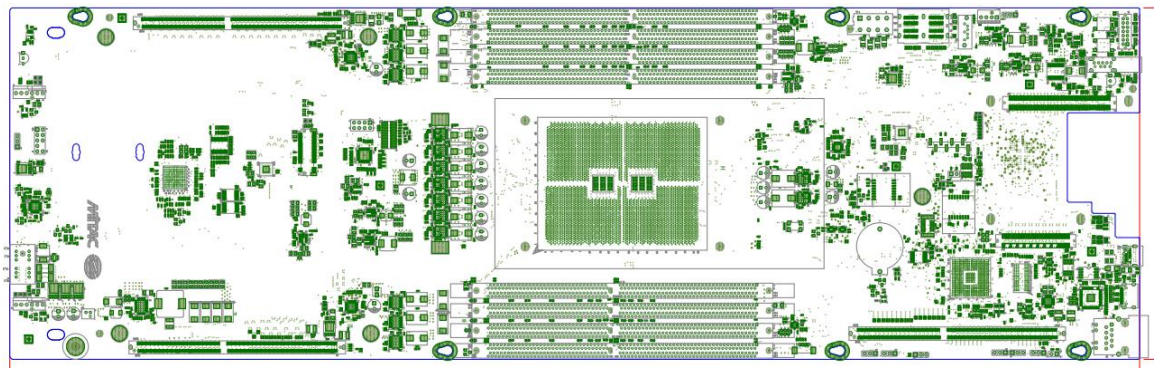
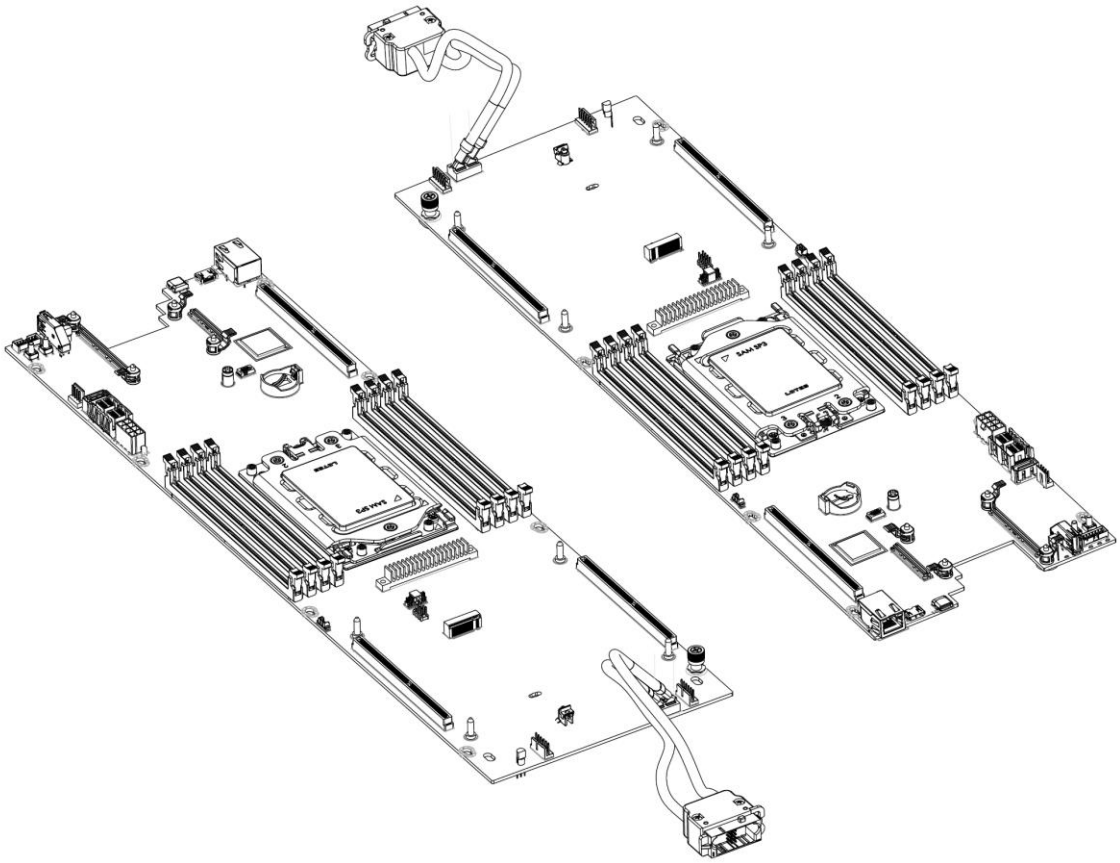


Figure 2 MiTAC E8020 2S Server (Capri) placement



3.3 CPU and Memory

As mentioned in Scope and Overview (Page 10), MiTAC E8020 2S Server (Capri) has two different sku and below is the table for CPU and Memory support.

	Advanced	**Ultra**
Processor	● AMD EPYC™ 7002, Rome (TDP: 225W) ● AMD EPYC™ 7003, Milan CPU will be supported in Q1 2021 (est. TDP: 225W)	
Memory	Up to 1024GB RDIMM/LRDIMM (Gen 4); 8 DIMM slots/ 8 channels (1DPC)	

3.4 PCB Stack-Up

MiTAC E8020 2S Server (Capri) has mainboard (same on Adv/Ultra), riser board (same on Adv/Ultra), and 2.5” drive backplane board (only applied on Ultra sku). Below is the stack-up info. for reference.

請框選▮或填數值	PCB層數：☐2L、☐4L、☐6L、☐8L、☐10L、☐12L、▮其他 __14__ L			板厚：	Single End Signal	Single End Signal	Differential Pair Signal	Differential Pair Signal	Differential Pair Signal
板名(MiTAC Project Name)：Capri				PCB板：	DDR4(1DPC)	DDR4(1DPC) dimm to dimm	HSD breakout	HSD breakout for back drill (BGA背鑽) via pad to via pad=20mil, **back drill clearance=28mil** via drill to trace=8mil, **Via pad to**	DDR4_DQS
PCB 板廠：ACCL									
PCB 材質 [板材 / Nominal Tg (℃) (DSC) / Minimum Td (℃) (TGA)(min)]： EM-526(RTF) / Tg230(TMA					Outer：50 Ω ± 10 %	Outer：50 Ω ± 10 %	Outer：線寬 / 線距 保持 3.9 / 3.9 m	Outer：線寬 / 線距 保持 3.7 / 3.6 mil 防	Outer：75 Ω ± 10 %
(板材MiTAC指定,Tg/Td板廠填寫) Ex: IT-180I / Tg175 / Td350 MiTAC 禁用材料 EMC台光(EM-320) &					Inner：40 Ω ± 10 %	Inner：50 Ω ± 10 %	Inner：線寬 / 線距 保持 3.9 / 3.9 m	Inner：線寬 / 線距 保持 3.7 / 3.6 mil 防	Inner：75 Ω ± 10 %
Layer Number	Layer Type Signal or plane	Layer Name	Layer Material Prepreg (RC%) / Core Copper 0.5, 1, 2oz (STD, RTF, RTF or...)	Thickness (unit: mil)	設計佈線(依調Layout 線寬) MiTAC Spec Width /	設計佈線(依調Layout 線寬) PCB	設計佈線(依調Layout 線寬) MiTAC	設計佈線(依調Layout 線寬) PCB	設計佈線(依調Layout 線寬 / 線距) MiTAC Spec Width /	設計佈線(依調Layout 線寬 / 線距) PCB vendor fine	設計佈線(依調Layout 線寬 / 線距) MiTAC Spec Width /	設計佈線(依調Layout 線寬 / 線距) PCB vendor
			Solder mask	0.7								
L1	Signal	Top	0.5 oz + plating (STD)	1.6	3.9 / 52.77	4.3 / 50.59	3.9 / 52.77	4.3 / 50.59	3.9 / 3.9 / 85.91	3.9 / 3.9 / 85.91	3.7 / 3.6 / 85.86	3.7 / 3.6 / 85.86	5.9 / 5 / 75.90	5.9 / 5 / 75.90
		Prepreg	1080(65%)	2.66										
L2	Plane	Gnd1	1 oz (RTF)	1.2	Gnd1	Gnd1	Gnd1	Gnd1	Gnd1	Gnd1	Gnd1	Gnd1	Gnd1	Gnd1
	H=3mil	Core	0.003"(1086*1)	3										
L3	Signal	In1	1 oz (RTF)	1.2	5.5 / 40.95	5.5 / 40.95	3.9 / 48.32	3.7 / 49.45	3.9 / 3.9 / 81.83	3.9 / 3.9 / 81.83	3.7 / 3.6 / 82.01	3.7 / 3.6 / 82.01	5.3 / 5 / 75.19	5.3 / 5 / 75.19
	>2.5~3H	Prepreg	2116HR(57%)+3313HR(59%)	8.36										
L4	Plane	Gnd2	1 oz (RTF)	1.2	Gnd2	Gnd2	Gnd2	Gnd2	Gnd2	Gnd2	Gnd2	Gnd2	Gnd2	Gnd2
	H=3mil	Core	0.003"(1086*1)	3										
L5	Signal	In2	1 oz (RTF)	1.2	5.5 / 40.95	5.5 / 40.95	3.9 / 48.32	3.7 / 49.45	3.9 / 3.9 / 81.83	3.9 / 3.9 / 81.83	3.7 / 3.6 / 82.01	3.7 / 3.6 / 82.01	5.3 / 5 / 75.19	5.3 / 5 / 75.19
	>2.5~3H	Prepreg	2116HR(57%)+3313HR(59%)	8.36										
L6	Plane	Gnd3	1 oz (RTF)	1.2	Gnd3	Gnd3	Gnd3	Gnd3	Gnd3	Gnd3	Gnd3	Gnd3	Gnd3	Gnd3
	4mil core	Core	0.004"(3313*1)1/2	4										
L7	Plane	Vcc1	2 oz (RTF)	2.4	Vcc1	Vcc1	Vcc1	Vcc1	Vcc1	Vcc1	Vcc1	Vcc1	Vcc1	Vcc1
	厚度 6mil 以上	Prepreg	1080HR(69%)*2	5.54										
L8	Plane	Vcc2	2 oz (RTF)	2.4	Vcc2	Vcc2	Vcc2	Vcc2	Vcc2	Vcc2	Vcc2	Vcc2	Vcc2	Vcc2
	4mil core	Core	0.004"(3313*1)1/2	4										
L9	Plane	Gnd4	1 oz (RTF)	1.2	Gnd4	Gnd4	Gnd4	Gnd4	Gnd4	Gnd4	Gnd4	Gnd4	Gnd4	Gnd4
	>2.5~3H	Prepreg	2116HR(57%)+3313HR(59%)	8.36										
L10	Signal	In3	1 oz (RTF)	1.2	5.5 / 40.95	5.5 / 40.95	3.9 / 48.32	3.7 / 49.45	3.9 / 3.9 / 81.83	3.9 / 3.9 / 81.83	3.7 / 3.6 / 82.01	3.7 / 3.6 / 82.01	5.3 / 5 / 75.19	5.3 / 5 / 75.19
	H=3mil	Core	0.003"(1086*1)	3										
L11	Plane	Gnd5	1 oz (RTF)	1.2	Gnd5	Gnd5	Gnd5	Gnd5	Gnd5	Gnd5	Gnd5	Gnd5	Gnd5	Gnd5
	>2.5~3H	Prepreg	2116HR(57%)+3313HR(59%)	8.36										
L12	Signal	In4	1 oz (RTF)	1.2	5.5 / 40.95	5.5 / 40.95	3.9 / 48.32	3.7 / 49.45	3.9 / 3.9 / 81.83	3.9 / 3.9 / 81.83	3.7 / 3.6 / 82.01	3.7 / 3.6 / 82.01	5.3 / 5 / 75.19	5.3 / 5 / 75.19
	H=3mil	Core	0.003"(1086*1)	3										
L13	Plane	Gnd6	1 oz (RTF)	1.2	Gnd6	Gnd6	Gnd6	Gnd6	Gnd6	Gnd6	Gnd6	Gnd6	Gnd6	Gnd6
		Prepreg	1080(65%)	2.66										
L14	Signal	Bottom	0.5 oz + plating (STD)	1.6	3.9 / 52.77	4.3 / 50.59	3.9 / 52.77	4.3 / 50.59	3.9 / 3.9 / 85.91	3.9 / 3.9 / 85.91	3.7 / 3.6 / 85.86	3.7 / 3.6 / 85.86	5.9 / 5 / 75.90	5.9 / 5 / 75.90
			Solder mask	0.7										
			board thickness (Unit: mil)	85.7										
			board thickness (Unit: mm)	2.17678	_SET2DIL or Delta-L_									

Figure 3 MiTAC E8020 2S Server (Capri) 14-layer PCB Stack-Up

PCB material: NPG-170D

MiTAC Proposed							Vendor data						
Layer	Type	thickness (mils)	Copper Weight (oz)		Dk	Df	Layer	Type	thickness (mils)	Structure	RC%	Dk	Df
	SM							SM	0.7			4.2	0.0156
L1	TOP						L1	TOP	1.6				
PP							PP	1080	2.92		64%	3.29	0.0055
L2	PWR/GND						L2	GND	1.2				
Core							Core	0.004"1/1	4		45.50%	3.68	0.0055
L3	Signal						L3	Signal	1.2				
PP							PP	1080H4*4x28mil 0/0	42.36			3.82	0.0055
L4	Signal						L4	Signal	1.2				
Core							Core	0.004"1/1	4		45.50%	3.68	0.0055
L5	PWR/GND						L5	GND	1.2				
PP							PP	1080	2.92		64%	3.29	0.0055
L6	BOT						L6	BOT	1.6				
	SM							SM	0.7			4.2	0.0156
	Total	61.80 mils						Total	62	mils			
		1.57 mm							1.57	mm			

Single-Ended								Differential				Differential (For High Speed Differential Pair Breakout)				Differential				Differential			
MiTAC Proposed		vendor Calculated		MiTAC Proposed		vendor Calculated		MiTAC Proposed		vendor Calculated		MiTAC Proposed		vendor Calculated		MiTAC Proposed		vendor Calculated		MiTAC Proposed		vendor Calculated	
Target Zo (Ω)	Width (mil)	Width (mil)	Referenced layers	Target Zo (Ω)	Width (mil)	Width (mil)	Referenced layers	Target Zo (Ω)	Width / Space (mil)	Width / Space (mil)	Referenced layers	Target Zo (Ω)	Width / Space (mil)	Width / Space (mil)	Referenced layers	Target Zo (Ω)	Width / Space (mil)	Width / Space (mil)	Referenced layers	Target Zo (Ω)	Width / Space (mil)	Width / Space (mil)	Referenced layers
49.12	4	5	L2	39.93	6.5	7.5	L2	84.63	6/6	5.5/6.5	L2	82.75	3.9/4.1	5/4.5	L2	94.47	4/8	4.5/7.5	L2	99.8	4/12	4.4/11.6	L2
49.48	5.5	5.5	L2/L5	40.89	6.5	8.5	L2/L5	84.66	6/6	5.7/6.3	L2/L5	83.4	3.9/4.1	5/4.5	L2/L5	95.94	4/8	4.5/7.5	L2/L5	100.84	4/12	4.6/11.4	L2/L5
49.48	5.5	5.5	L2/L5	40.89	6.5	8.5	L2/L5	84.66	6/6	5.7/6.3	L2/L5	83.4	3.9/4.1	5/4.5	L2/L5	95.94	4/8	4.5/7.5	L2/L5	100.84	4/12	4.6/11.4	L2/L5
49.12	4	5	L5	39.93	6.5	7.5	L5	84.63	6/6	5.5/6.5	L5	82.75	3.9/4.1	5/4.5	L5	94.47	4/8	4.5/7.5	L5	99.8	4/12	4.4/11.6	L5

Notes:

1. Board thickness tolerance should be (+8/-5) mils
2. Starting Copper weight on outer layers is 0.5oz; 1.5oz is approx weight after plating.

Figure 4 MiTAC E8020 2S Server (Capri) Riser Board Stack-Up

Material		MiTAC Proposal		Vendor proposal								50 ohm Single-Ended				85 ohm Differential				100 ohm Differential			
IT170GBA1(RTF)												MiTAC Design		Simulated		MiTAC Design		Simulated		MiTAC Design		Simulated	
No. of Layer	Type	Cu weight	THK (mil)	Structure	THK (mil)	RC%	Dk(1G)	Dk(3G)	Df (1G)	Df (3G)	Ref layers	Target Zo (Ω)	LW (mil)	Target Zo (Ω)	LW (mil)	Target Zo (Ω)	LW/LS (mil)	Target Zo (Ω)	LW/LS (mil)	Target Zo (Ω)	LW/LS (mil)	Target Zo (Ω)	LW/LS (mil)
	SM		0.5		0.5																		
L1	TOP	0.5+Plating	1.9		2.1						L2	50±10%	4.3	50.06	4.625	85±10%	5/7	84.92	5.25/6.75	100±10%	3.7/8.3	99.54	3.875/8.125
PP			2.7	1080*1	2.7875	65%	3.68	no data	0.0082	no data													
L2	GND	1	1.2		1.25																		
Core			4	2116X1	4.2		3.97	no data	0.0076	no data													
L3	Signal	1	1.2		1.25						L2/L4	50±10%	3.5	50.46	3.75	85±10%	4.5/8	84.5	5/7.5	100±10%	3.5/12	100.05	3.75/11.75
PP			4	2116*1	4.2125	57%	3.84	no data	0.0079	no data													
L4	GND	1	1.2		1.25																		
Core			4	2116X1	4.2		3.97	no data	0.0076	no data													
L5	Signal	1	1.2		1.25						L4/L6	50±10%	3.5	50.46	3.75	85±10%	4.5/8	84.5	5/7.5	100±10%	3.5/12	100.05	3.75/11.75
pp			4	2116*1	4.2125	57%	3.84	no data	0.0079	no data													
L5	PWR/GND	1	1.2		1.25																		
Core			8	7628X1	8		4.11	no data	0.0074	no data													
L7	PWR/GND	1	1.2		1.25																		
pp			4	2116*1	4.2125	57%	3.84	no data	0.0079	no data													
L8	Signal	1	1.2		1.25						L7/L9	50±10%	3.5	50.46	3.75	85±10%	4.5/8	84.5	5/7.5	100±10%	3.5/12	100.05	3.75/11.75
Core			4	2116X1	4.2		3.97	no data	0.0076	no data													
L9	GND	1	1.2		1.25																		
pp			4	2116*1	4.2125	57%	3.84	no data	0.0079	no data													
L10	Signal	1	1.2		1.25						L9/L11	50±10%	3.5	50.46	3.75	85±10%	4.5/8	84.5	5/7.5	100±10%	3.5/12	100.05	3.75/11.75
Core			4	2116X1	4.2		3.97	no data	0.0076	no data													
L11	PWR/GND	1	1.2		1.25																		
PP			2.7	1080*1	2.7875	65%	3.68	no data	0.0082	no data													
L12	BOT	0.5+Plating	1.9		2.1						L11	50±10%	4.3	50.06	4.625	85±10%	5/7	84.92	5.25/6.75	100±10%	3.7/8.3	99.54	3.875/8.125
	SM		0.5		0.5																		
	1.6mm+/-10%	Total	62.2	Total	63.925	mil																	
			1.57988316		1.623695																		
					W/O SM																		

Figure 5 MiTAC E8020 2S Server (Capri) 2.5” drive backplane board

3.5 Figures & Illustrations

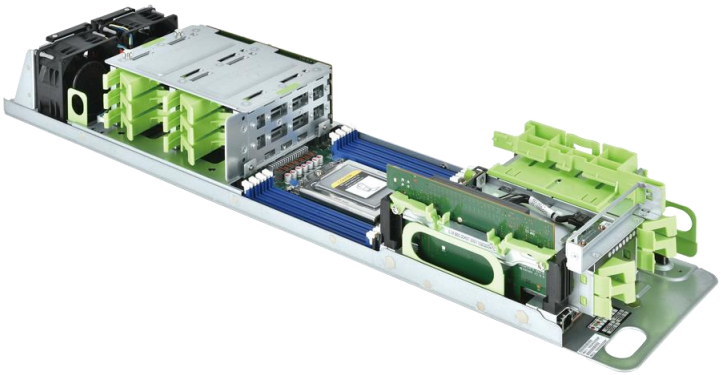


Figure 6 MiTAC E8020 2S Server (Capri)

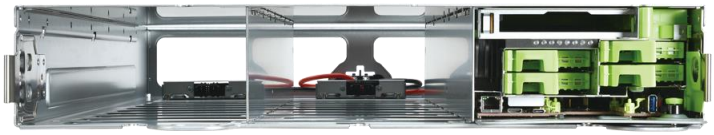


Figure 7 MiTAC E8020 2S Server (Capri) in Cubby

4. BIOS

4.1 BIOS Chip

MiTAC E8020 2S Server (Capri) follows OCP (Open Computing Project) v4_0v16 specification to design the board and it adopts AMD ROME processor. The ROM size of Capri BIOS is 32MB.

4.2 BIOS Source Code

The BIOS source code is from AMI.

4.3 BIOS Feature Requirements

4.3.1 Boot Logo

While BIOS booting, if there is a graphic display supported in the system, user can see the defined logo screen when enabling boot logo present feature. BIOS shall provide a selection option in SETUP for user to choose boot logo presented or not at the boot time. If this feature is enabled, it could be scale to full screen with sufficient image resolution and keep a while of seconds on screen.

If user set boot logo presented option to be disabled, BIOS shall switch to IBV native defined mode on display. The message must include platform information which is defined in section “4.3.2 Information Displayed during POST Time” to let user can properly to know system summary information.

Need to take care of logo resolution when it’s in full screen scale. The MiTAC logo file and the minimum format requirement are defined as,

- BMP format
- 8bits color depths
- 800x600 pixels dimension

4.3.2 Information Displayed during POST Time

During BIOS POST, the text message will be showed on the host display or redirected to remote console connection for user to examine the summary information about the whole system without entering BIOS setup. The screen contents shall hold and keep around **1** second so as to view the information easily. The contents would cover below information,

- BIOS Version
- BIOS Build Date
- BMC Version
- IPMI IP Address
- Total Installed Memory Size

4.3.3 BIOS Hotkeys

Support to use specified single key or combination keys to enter BIOS Setup Menu, the default setting is <Del> or <F2> during boot time when prompt information is displayed on screen or remote console. The following instructional message would be displayed on the screen.

- Press <F11> to prompt boot popup menu.
- Press <F12> to PXE Boot.
- [1]Press <DEL> or <F2> to enter setup.

[1] Number Lock function shall set **Disabled** as default.

Furthermore, the prompt presented time on the screen would be a selection in BIOS setup menu. User can define a specified value with seconds scale to wait for input actions.

The default setup prompt timeout is **1** seconds.

4.3.4 Remote Combination Hotkeys

BIOS provides serial redirection feature in various remote management console. Here is the combination key supported list for different kind of terminal setting.

Key or Function	Sequence
Right	<ESC> [, C
Left	<ESC> [, D
Up	<ESC> [, A
Down	<ESC> [, B
Home	<ESC> [, H
End	<ESC> [, K
F1	<ESC> O , P
F2	<ESC> O , Q
F3	<ESC> O , R
F4	<ESC> O , S
System Reset	<ESC>R<ESC>r<ESC>R

Figure 8 Standard ANSI Sequences

Key or Function	Sequence
F1	<ESC> O , P
F2	<ESC> O , Q
F3	<ESC> O , R
F4	<ESC> O , S
F5	<ESC> O , T
F6	<ESC> O , U
F7	<ESC> O , V
F8	<ESC> O , W
F9	<ESC> O , X
F10	<ESC> O , Y
F11	<ESC> O , Z
F12	<ESC> O , [
Home	<ESC> [, 1, ~
Ins	<ESC> [, 2, ~
Del	<ESC> [, 3, ~
End	<ESC> [, 4, ~
Page Up	<ESC> [, 5, ~
Page Dn	<ESC> [, 6, ~

Figure 9 Putty VT100 Keypad

4.3.5 BIOS POST Code

The POST codes are composed of two or four HEX codes according to Intel or AMD platform. During the period of POST time, BIOS shall output these HEX codes to specified interfaces or media to let user realize the system POST status. *E.g. BMC SoL.*

4.3.5.1 POST Code for OPROM Entry and Exit

It's a special pair of BIOS post codes to indicate the entry and exit of option ROM. Two consecutive bytes are assigned for the entry and exit to avoid the same sequence used on another BIOS POST code. The definition is,

- Use [AA][C0] to indicate entering Option ROM.
- Use [BB][C1] to indicate exiting Option ROM.

4.3.6 BMC FRB2 Watch Dog Timer

The default setting of watch dog function is DISABLED and only be enabled in MP stage. The default timeout setting is 15 minutes and then RESET the system when the timer expired. The watchdog timer is always disabled after POST.

4.3.7 Protected Processor Inventory Number

BIOS shall support PPIN and set default to **[Unlock and Enable]**. There are two ways for user to access PPIN,

- BIOS shall map PPIN of CPU to SMBIOS OEM Strings (Type 11) String 5 . User can view PPIN value from Linux's "dmidecode" command.
- BIOS shall implement Send_PPIN OEM Command to communicate to BMC, per BMC's request.

BIOS shall perform 2 actions to synchronize PPIN value to BMC,

- Serves SMI# signal from BMC and use Send_PPIN OEM command to communicate PPIN to BMC.
- Use Send_PPIN OEM command to communicate PPIN to BMC when BIOS POST COMPLETE.

4.3.8 Start of POST and End of POST Information

BIOS shall assert specified GPIO pin status to inform BMC about BIOS **start of POST** and **end of POST** events.

4.3.9 Manufacture Mode

BMC will provide an IPMI command to enter manufacture mode. It is a special BIOS mode designed to decrease the time which systems spend on the assembly line. This is done by skipping non-essential boot functions/tests and by prioritizing pre-defined boot devices ordering. These changes decrease the boot time significantly which allows more systems to complete the factory processes in less time.

BIOS shall replace AMI boot logo with a manufacture mode picture like below and set Quiet Mode to **disabled** to

show up on the screen during BIOS POST Time to indicate user that the system is booting on manufacture status.

4.3.9.1 Prerequisites

For example, BIOS could implement below listed items,

- Set “Onboard LAN” to be the first bootable device, if it presents.
- System console redirection would be always enabled.
- Do not launch onboard storage and add-on card, if it appears in system.
- Launch onboard storage and add-on card, if it doesn’t appear in system.

4.3.10 WHEA ID

Beginning with Windows Server 2008 and Windows Vista SP1, when a hardware error occurs, the operating system creates an error record that describes the error condition and sends an event tracing for Windows (ETW) event that contains the error record to user mode. The format of the error record is based on the Common Platform Error Record as described in Appendix N of version 2.2 of the Unified Extensible Firmware Interface (UEFI) Specification.

The following table describes each of the WHEA error-specific hardware error events that are defined for Windows Server 2008, Windows Vista SP1, and later versions of Windows.

Event	Event ID
WHEALOGR_DEFAULT_ERROR	1
WHEALOGR_DEFAULT_WARNING	2
WHEALOGR_DEFAULT_INFO	3
WHEALOGR_PCIE_ERROR	16
WHEALOGR_PCIE_WARNING	17
WHEALOGR_XPF_MCA_ERROR	18
WHEALOGR_XPF_MCA_WARNING	19
WHEALOGR_XPF_AMD64NB_MCA_ERROR	20
WHEALOGR_XPF_AMD64NB_MCA_WARNING	21
WHEALOGR_PLATFORM_MEMORY_ERROR	22
WHEALOGR_PLATFORM_MEMORY_WARNING	23
WHEALOGR_PCIXBUS_ERROR	24
WHEALOGR_PCIXBUS_WARNING	25
WHEALOGR_PCIXDEVICE_ERROR	26
WHEALOGR_PCIXDEVICE_WARNING	27
WHEALOGR_IPF_MCA_ERROR	38
WHEALOGR_IPF_MCA_WARNING	39
WHEALOGR_PCIE_NODEVICEID_ERROR	40
WHEALOGR_PCIE_NODEVICEID_WARNING	41
WHEALOGR_PCIXBUS_NODEVICEID_ERROR	42

WHEALOGR_PCIXBUS_NODEVICEID_WARNING	43
WHEALOGR_PCIXDEVICE_NODEVICEID_ERROR	44
WHEALOGR_PCIXDEVICE_NODEVICEID_WARNING	45
WHEALOGR_PLATFORM_MEMORY_NOTYPE_ERROR	46
WHEALOGR_PLATFORM_MEMORY_NOTYPE_WARNING	47

4.3.11 Endless Boot Support

If this feature was enabled, BIOS shall start to traverse all bootable devices constantly which are attached to the system. Particularly, it shall avoid entering in **EFI shell** or **BIOS SETUP** when BIOS tried to boot but failed for every device. However, during the period of endless loop, BIOS shall keep listening the hot key such as F2 or DEL to break the loop.

When this feature was disabled, it will show ***"Reboot and Select proper Boot device Or Insert Boot Media in selected Boot device and press a key"*** on the screen.

Be awarded that the LAN port which was dedicated to use by BMC was not included in Endless boot retry loop.

5. BMC

5.1 BMC overview in MiTAC E8020 2S Server (Capri)

The BMC firmware implements IPMI 2.0 based on AST2500 service processor. It performs all the BMC management tasks defined by IPMI 2.0 and, as a Service Processor, allows for remote monitoring using Serial Over LAN.

5.2 BMC Hardware Component in MiTAC E8020 2S Server (Capri)

Component	Size	Usage
Aspeed AST2500	NA	It's a vastly integrated SOC device playing as a service processor to support various functions required for highly manageable server platforms.
DDR4 SDRAM	512MB	BMC memory
SPI flash	32MB	BMC Flash part includes BMC FW, user configuration, SEL and SDR.
EPROM	8KB	FRU information
PHY NIC	10M/10M/1G	Dedicated for BMC

5.3 BMC Main Features

5.3.1 IPMI 2.0 Standard Features BMC Main Features

Feature	Description
System Interface support	• KCS • LAN(RMCP/RMCP+)
Text Console Redirection: SOL	• Support in IPMI stack for SOL to remotely access BIOS and text console before OS booting.
IPMI 2.0 based Management	• BMC stack with a full IPMI 2.0 implementation • Optional commands supported(refer to section 4.1.1) • OEM commands supported(refer to section 4.1.2 and section 5)
System Management	• System health monitoring. • System Power management • Fan speed monitor and control
Event Log and Alerting	• Read Log events • Sensor readings

	• SNMP traps
Remote Server Power Control	• Server's power status report • Support for remotely power-cycle, power-down, power-up, reset the server
Watchdog Timer Support	• Watchdog function that can generate interrupt or reset after zero count down
Sophisticated User Management	• IPMI based user management • Multiple user permission level • Extended security algorithms and cipher suites support

5.3.2 OEM features

Feature	Description
Management Network Interface	• BMC should have Shared-NIC uses RMII/NCSI interface for Out-of-Band access.
Port 80 POST	• BMC to support port 80 POST code display to drive 8 bit HEX GPIO and SOL • BMC should have access to POST code and record up to 256 POST codes.
FSC in BMC	• BMC should support FSC in both PID and step mode. BMC should support both In-Band and Out-of-Band FSC configuration update; updates should take effect immediately without reboot required. BMC should support FAN boost during fan failure. • Default fan PWM setting is 60% when power on by HW.
BIOS recovery	
UART port switch control	
Remote change BIOS boot mode/boot order	
Board ID	
FAB Revision ID	
Control Power and System Identification LED	
Auto BIOS Recovery	
Manual BIOS Copy	
Manual remote update BIOS	
Enable/Disable Auto BIOS recovery	
Get Dual BIOS feature status	
Get BIOS Version	
YAFU BMC/BIOS/CPLD remote update	
BMC web GUI	

5.4 Messaging interfaces

The BMC messaging interfaces comply with the IPMI 2.0 specification. The following interfaces are supported.

- Keyboard Controller Style (KCS) Host Interface – Chapter 9 of the IPMI 2.0 specification.
- LAN Interface – Chapter 13 of the IPMI 2.0 specification.
- IPMI Serial/Modem Interface – Chapter 14 of the IPMI 2.0 specification.

Channel	Interface
0h	IPMB
1h	RMII Sideband NIC
3h	KCS
Fh	Host/SMS

5.4.1. KCS Interface

Capri BMC provides one KCS interface for communication with host. The programmed address for KCS interface, data port is at CA2h and status port is at CA3h.

5.4.2. LAN Interface

Capri BMC uses the NCSI side-band network interface to provide support for IPMI messaging over LAN.

5.4.3. FRU ID Number

FRU Name	ID Number	I2C Bus	Slave Address	Support Command
Main Board FRU	0	7	A0h	1. Read/Write FRU Data 2. Master Write-Read

5.4.4. Ciphers and Keys Security implementation

All ciphers are supported by IPMI V.2.0 and disabled by default. There are only 2 ciphers (Cipher ID# 3, 8) at enabled status and all other ciphers will be at disable status by default. The detail ciphers table are listed below.

Cipher ID	Authentication Algorithm	Integrity Algorithm	Confidentiality Algorithm	Default Status
0	RAKP-none	None	None	Disable
1	RAKP-HMAC-SHA1	None	None	Disable
2	RAKP-HMAC-SHA1	HMAC-SHA1-96	None	Disable
3	RAKP-HMAC-SHA1	HMAC-SHA1-96	AES-CBC-128	Enable
6	RAKP-HMAC-MD5	None	None	Disable
7	RAKP-HMAC-MD5	HMAC-MD5-128	None	Disable
8	RAKP-HMAC-MD5	HMAC-MD5-128	AES-CBC-128	Enable

11	RAKP-HMAC-MD5	MD5-128	None	Disable
12	RAKP-HMAC-MD5	MD5-128	AES-CBC-128	Disable

5.5 BMC user account

Default user account as below table:

User ID	User Name	Password	Status	Default Privilege
1	[NULL]	[NULL]	Disable	Administrator
2	admin	admin	Enable	Administrator
3~10	Undefined	Undefined	Disable	Undefined

NOTE: Users need to modify the user password at first log-in.

5.6 Text console redirection – SOL (Serial over LAN)

Capri BMC FW provides the support for text console redirection (SOL) to remotely access BIOS setup or text consoles that are available on the serial console of host system.

The firmware includes support for IPMI based SOL where the standard IPMI client like IPMITOOL can be used to establish a SOL session with the service processor.

The SOL default baud rate is setup by BMC flash part as 57600. BMC and uEFI will synch at the system booting POST stage.

5.7 Commands Support

Capri BMC FW provides a fully-compliant IPMI 2.0 based management of the service processor.

All the mandatory requirements and commands in IPMI 2.0 are supported.

5.7.1. IPMI Global Commands

In addition to the mandatory criteria in IPMI 2.0 specification, Capri BMC FW also supports many optional commands.

The following is a list of commands that currently support to the Capri BMC firmware.

5.7.1.1. IPMI Global Commands

IPM Global Commands
Get Device ID
Cold Reset
Warm Reset
Get Self Test Results
Set ACPI Power State
Get ACPI Power State
Get Device GUID
Get NetFn Support
Get Command Support
Get Command Sub-function Support
Get Configurable
Get Configurable Command Sub-functions

5.7.1.2. BMC Watchdog Timer Commands

BMC Watchdog Timer Commands
Reset Watchdog Timer
Set Watchdog Timer
Get Watchdog Timer

5.7.1.3. IPMI Messaging Support Commands

IPMI Messaging Support Commands
Set BMC Global Enables
Get BMC Global Enables
Clear Message Flags
Get Message Flags
Enable Message Channel Receive
Get Message
Send Message
Read Event Message Buffer
Get System GUID
Get Channel Authentication Capabilities
Get Session Challenge
Activate Session
Set Session Privilege Level
Close Session
Get Session Info

Get AuthCode
Set Channel Access
Get Channel Access
Get Channel Info
Set Channel Security Keys
Set User Access
Get User Access
Set User Name
Get User Name
Set User Password
Master Write-Read
Get Channel Cipher Suites
Get System Interface Capabilities
Set System Info Parameters
Get System Info Parameters

5.7.1.4. RMCP+ Support and Payload Commands

RMCP+ Support and Payload Commands
Activate Payload
Deactivate Payload
Get Payload Activation Status
Get Payload Instance Info
Set User Payload Access
Get User Payload Access
Get Channel Payload Support
Get Channel Payload Version
Get Channel OEM Payload Info
Suspend/Resume Payload Encryption

5.7.1.5. Chassis Device Commands

Chassis Device Commands
Get Chassis Capabilities
Get Chassis Status
Chassis Control
Chassis Identify
Set Chassis Capabilities
Set Power Restore Policy – disable by default
Get System Restart Cause

Set System Boot Options
Get System Boot Options
Get POH Counter

5.7.1.6. Event Commands

Event Commands
Set Event Receiver
Get Event Receiver
Platform Event

5.7.1.7. PEF and Alerting Commands

PEF and Alerting Commands
Get PEF Capabilities
Arm PEF Postpone Timer
Set PEF Configuration Parameters
Get PEF Configuration Parameters
Set Last Processed Event ID
Get Last Processed Event ID
Alert Immediate
PET Acknowledge

5.7.1.8. Sensor Device Commands

Sensor Device Commands
Get Device SDR Info
Get Sensor Reading Factors
Set Sensor Hysteresis
Get Sensor Hysteresis
Set Sensor Threshold
Get Sensor Threshold
Set Sensor Event Enable
Get Sensor Event Enable
Re-arm Sensor Events
Get Sensor Event Status
Get Sensor Reading
Set Sensor Reading And Event Status
Set Sensor Type

5.7.1.9. FRU Inventory Area Info

FRU Device Commands
Get FRU Inventory Area Info
Read FRU Data
Write FRU Data

5.7.1.10. SDR Repository Device Commands

SDR Repository Device Commands
Get SDR Repository Info
Get SDR Repository Allocation Info
Reserve SDR Repository
Get SDR
Add SDR
Partial Add SDR
Delete SDR
Clear SDR Repository
Get SDR Repository Time
Enter SDR Repository Update Mode
Exit SDR Repository Update Mode
Run Initialization Agent

5.7.1.11. SEL Device Commands

SEL Device Commands
Get SEL Info
Get SEL Allocation Info
Reserve SEL
Get SEL Entry
Add SEL Entry
Partial Add SEL Entry
Clear SEL
Get SEL Time
Set SEL Time
Get SEL Time UTC Offset
Set SEL Time UTC Offset

5.7.1.12. IPMI LAN Commands

IPMI LAN Commands
Set LAN Configuration Parameters
Get LAN Configuration Parameters
Suspend BMC ARPs

5.7.1.13. SOL Commands

SOL Commands
Set Serial/Modem Configuration
Get Serial/Modem Configuration
SOL Activating
Set SOL Configuration Parameters
Get SOL Configuration Parameters

5.7.2. OEM command support

Except the Standard and optional commands, provide the system specific OEM commands that dedicated for Capri system, below are all the OEM commands that available for Capri.

The following is a list of OEM commands that planning to support on the Capri BMC firmware.

Command Set	Sub command	NetFn	CMD Code
FSC Command Set	Enter FSC Update Mode Command	30h	61h
	Exit FSC Update Mode Command	30h	62h
	Read FSC Profile Header Command	30h	63h
	Write FSC Profile Header Command	30h	64h
	Read FSC Profile Command	30h	65h
	Write FSC Profile Command	30h	66h
	Read Zone Control Setting Command	30h	67h
	Write Zone Control Setting Command	30h	68h
	Get PWM value Command	30h	69h
	Set PWM value Command	30h	70h
	Get the total number of PWM IDs Command	30h	71h
	Restore FSC Command	30h	72h
Auto BIOS Recovering command Set	Set Dual BIOS Mux Command	30h	43h
	Set Dual BIOS Recovery Command	30h	44h
	Get Dual BIOS Status Command	30h	45h
	Set Dual BIOS Version Obtain Command	30h	54h
	Get Dual BIOS Version Command	30h	50h
	Perform BIOS Recovery Command	30h	41h
	Perform BIOS Backup Command	30h	42h
	Get BIOS Flash Info	30h	55h
	Get BIOS Version Command	30h	83h
	Disable ARB Timer Command	3Ch	30h
Other OEM Command Set	Restore Factory Default Command	32h	66h

	Get 80 Port Record Command	30h	49h
	Set DIMM Information Command	30h	1Ch
	Get DIMM Information Command	30h	1Dh
	Set VR Monitor Enable Command	30h	D2h
	Get VR Monitor Enable Command	30h	D4h
	Get CPLD Information Command	3Ch	88h
	Set Network Sequence Command	30h	B0h
	Get Network Sequence Command	30h	B1h
	Replay SOL Buffer Command	30h	48h
	Set PPIN Command	30h	77h
	Get PPIN Command	30h	78h
	Set Preserve Configuration Command	32h	83h
	Get Preserve Configuration Command	32h	84h
	Set First Time BIOS Boot Flag Command	30h	40h
	Set PHY Reset Status Command	30h	30h
	Get PHY Reset Status Command	30h	31h
	Set GPIO Command	30h	E0h
	Get GPIO Command	30h	E1h
	Getting Multiple IPv6 IP Addresses command	32h	99h
	Get PIN	30h	DFh
	Get Board ID Command	3Ch	89h
	Get FAB Revision Command	3Ch	8Ah

5.7.2.1. Auto BIOS Recovering command Set

5.7.2.1.1. Set Dual BIOS Mux Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/Response Data**	**Description**
43h	Set Dual BIOS Mux	**Request:** Byte 1 – 00h = Set SPI flash bus to Host CPU. 01h = Set SPI flash bus to BMC. Byte 2 – 01h = Select primary BIOS flash. 02h = Select backup BIOS flash. **Response:** Byte 1 – Completion code. 00h = Command Completed Normally. D5h = Command could not be executed, BIOS in post/setup mode. C0h = Node Busy. The previous operation	This command could not execution during BIOS post、BIOS setup menu and system reboot.

		not finished yet.	

5.7.2.1.2. Set Dual BIOS Recovery Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/Response Data**	**Description**
44h	Set Dual BIOS Recovery	**Request:** Byte 1 –Setting of Dual BIOS recovery 00h = Disable 01h = Enable. **Response:** Byte 1 – Completion code. 00h = Command Completed Normally.	Setting of enable/disable Auto BIOS Recovery after 1st time boot after a BIOS update

5.7.2.1.3. Get Dual BIOS Status Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/Response Data**	**Description**
45h	Get Dual BIOS Status	Request: N/A Response: Byte 1 – Completion code. Byte 2 – Setting of Dual BIOS recovery 00h = Disabled 01h = Enabled. Byte 3 – 00h = SPI flash bus has been selected to CPU Host. 01h = SPI flash bus has been selected to BMC. Byte 4 – 01h = The primary flash has been selected. 02h = The backup flash has been selected.	The default Byte 2 = 0. The default Byte 3 = 0. The default Byte 4 = 1.

		Byte 5 – Recover/Backup status 00h = Nothing to happen 01h = Performing BIOS Recovery 02h = Performing BIOS Backup	

5.7.2.1.4. Set Dual BIOS Version Obtain Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/Response Data**	**Description**
54h	Set Dual BIOS Version Obtain	**Request: N/A** **Response:** Byte 1 – Completion code. D5h = Command could not be executed, BIOS in post/setup mode. C0h = Node Busy. The previous operation not finished yet.	Request BMC to read BIOS version from physical primary and backup SPI flash device, and save in BMC DRAM. Get dual BIOS version reads the same variable in BMC DRAM. This command could not execution during BIOS post、BIOS setup menu and system reboot. If completion code is C0h, please wait for 15 seconds and try this command again.

5.7.2.1.5. Get Dual BIOS Version Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/Response Data**	**Description**
50h	Get Dual BIOS Version	**Request:** Byte 1– 01h = Get primary BIOS FW version. 02h = Get backup BIOS FW version. **Response:**	Read BIOS version of primary and backup image from BMC DRAM.

		Byte 1 – Completion code. 00h = Command Completed Normally. CBh = Requested Sensor, data, or record not present. CCh = Invalid data field in Request. 82h = Dual BIOS version not ready Byte 2:N – BIOS FW version(ASCII code) (LSB first)	

5.7.2.1.6. Perform BIOS Recovery Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/Response Data**	**Description**
41h	Perform BIOS Recovery	**Request:** Byte 1 – 72h ('r') Byte 2 – 65h ('e') Byte 3 – 63h ('c') Byte 4 – 6Fh ('o') Byte 5 – 76h ('v') Byte 6 – 65h ('e') Byte 7 – 72h ('r') **Response:** Byte 1 – Completion code. 00h = Command Completed Normally. C0h = Node Busy. The previous operation not finished yet. D5h = Command could not be executed, BIOS in post/setup mode.	Copy backup BIOS image to primary BIOS image. This command could not execution during BIOS post、BIOS setup menu and system reboot. Please send the below command to execute Global Reset after the recovery is done 'ipmitool power cycle'

5.7.2.1.7. Perform BIOS Backup Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/Response Data**	**Description**
42h	Perform BIOS Backup	**Request:** Byte 1 – 62h ('b') Byte 2 – 61h ('a') Byte 3 – 63h ('c') Byte 4 – 6Bh ('k') Byte 5 – 75h ('u') Byte 6 – 70h ('p') **Response:** Byte 1 – Completion code. 00h = Command Completed Normally. C0h = Node Busy. The previous operation not finished yet. D5h = Command could not be executed, BIOS in post/setup mode	Copy primary BIOS image to backup BIOS image. This command could not execution during BIOS post、BIOS setup menu and system reboot. Please send the below command to execute Global Reset after the backup is done 'ipmitool power cycle'

5.7.2.1.8. Get BIOS Flash Info

Net Function = 30h (OEM)			
Code	**Command**	**Request/Response Data**	**Description**
55h	Get BIOS Flash Info	**Request:** Byte 1 – 00h = Primary BIOS SPI flash 01h = Backup BIOS SPI flash **Response:** Byte 1 – Completion code. 00h = Command Completed Normally. C0h = Node Busy. The previous operation not	Read BIOS SPI Flash JEDEC ID and status register

		finished yet. 82h = BIOS SPI flash info not ready. D5h = Command could not be executed, BIOS in post/setup mode. The below data can be respond while the BIOS flash info is ready in the BMC DRAM, Byte 2 – Manufactory ID Byte 3 – Memory type Byte 4 – Memory density/capacity Byte 5 – Status register	

5.7.2.1.9. Get BIOS Version Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/Response Data**	**Description**
83h	Get BIOS Version	**Request: N/A** **Response:** Byte 1 – Completion code. 00h = Command Completed Normally. CBh = Requested Sensor, data, or record not present. Byte 2:N – BIOS FW version (ASCii code)	Read BIOS version from BMC DRAM that BIOS passed to BMC during BIOS POST.

5.7.2.1.10. Disable ARB Timer Command

Net Function = 0x3C			
Code	**Command**	**Request/Response Data**	**Description**
0x30	Disable ARB Timer	**Request: N/A** **Response:** Byte[1] : Completion	This command only for BIOS. This command let BIOS to notify BMC to disable ARB timer. The disable conditions are as below:

		code	BIOS runs normally and BIOS will send a "disable ARB timer" command to BMC before boot to OS

5.7.3. BIOS Boot option Command Set

5.7.3.1. Get BIOS Boot Option Status Command

Net Function = Net Function = 3Ch (OEM) 0x3C (OEM)			
Code	**Command**	**Request/Response Data**	**Description**
0x10	Get BIOS Boot Option Status.	**Request: N/A** **Response:** Byte 1 – Completion code. Byte 2 – Boot Option Changed Status. 00h = Boot sequence no change. 01h = Boot sequence has been changed.	This command only for BIOS.

5.7.3.2. Get BIOS Boot Option Counter Command

Net Function = Net Function = 3Ch (OEM) 0x3C (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
0x11	Get BIOS Boot Option Counter.	**Request: N/A** **Response:** Byte 1 – Completion code. Byte 2 – Counter Number.	Byte 2 – 0: BIOS Boot Option Data is empty in BMC. This OEM command only for software tool and BIOS.

5.7.3.3. Get BIOS Boot Order Command

Net Function = Net Function = 30h (OEM) 0x3C (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
0x53	Get BIOS Boot Order	**Request:** Byte 1 – Set reading status. 0: first data reading. 1: To be continued. **Response:** Byte 1 – Completion code. Byte 2 – Data readable status. 0: Last batch. 1: Remaining. Byte 3 – Index Number.	This OEM command only for software tool and BIOS.

Net Function = Net Function = 30h (OEM) 0x3C (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
		Byte 4: 5 – Option Number (LSB first). Byte 6: 9 – Attribute (LSB first). Byte 10 – Device Type. Byte 11:74 – Option Name String (64Byte).	

5.7.3.4. Set BIOS Boot Order Command

Net Function = Net Function = 30h (OEM) 0x3C (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
0x52	Set BIOS Boot Order	**Request:** Byte 1 – Set writing status. 0: first data writing. 1: To be continued. Byte 2 – Index Number. Byte 3: 4 – Option Number (LSB first). Byte 5: 8 – Attribute (LSB first). Byte 9 – Device Type. Byte 10:73 – Option Name String.(64Byte) **Response:** Byte 1 – Completion code.	This OEM command only for software tool and BIOS.

5.7.3.5. Set BIOS Boot Option Status Command

Net Function = Net Function = 3Ch (OEM) 0x3C (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
0x14	Set BIOS Boot Option Status.	**Request:** Byte 1 – Boot Option Changed Status. 00h = Boot sequence no change. 01h = Boot sequence has been changed. **Response:** Byte 1 – Completion code.	This command only for software tool.

5.7.3.6. Set BIOS Boot Mode Command

Net Function = Net Function = 3Ch (OEM) 0x3C (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
0x15	Set BIOS Boot Mode	**Request:** Byte 1 – 0x00 = UEFI mode. 0x01 = Legacy mode. Byte 2 – 0x00 = Setting by uEFI.	This OEM command only for software tool and BIOS.

Net Function = Net Function = 3Ch (OEM) 0x3C (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
		– 0x01 = Setting by tool. **Response:** Byte 1 – Completion code.	

5.7.3.7. Get BIOS Boot Mode Command

Net Function = Net Function = 3Ch (OEM) 0x3C (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
0x16	Get BIOS Boot Mode	**Request: N/A** **Response:** Byte 1 – Completion code. Byte 2 – 0x00 = UEFI mode. 0x01 = Legacy mode.	

5.7.3.8. Get BIOS Boot Mode Status Command

Net Function = Net Function = 3Ch (OEM) 0x3C (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
0x17	Get BIOS Boot Mode Status.	**Request: N/A** **Response:** Byte 1 – Completion code. Byte 2 – 0x00 = No change. 0x01 = The boot mode has been changed by software tool.	

5.7.3.9. Clean BIOS Boot Mode Status Command

Net Function = 0x3C (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
0x18	Clean BIOS Boot Mode Status.	**Request: N/A** **Response:** Byte 1 – Completion code.	This OEM command only for BIOS.

5.7.4. Other OEM Command Set

5.7.4.1. Restore Factory Default Command

Net Function = 32h (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
66h	Restore Factory Default	**Request:** NA	When send this command to BMC, the LAN Configuration Parameters will be changed current setting value to default value

Net Function = 32h (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
		Respones: Byte 1 – Completion code.	as following: IP Address Source = 0x00(DHCP) The Network sequence priority default is Mezzanine card for PVT/MP. The MEZZ protocol priority default is NCSI for PVT/MP. User IDs (User/Password/Privilege/Channels). Debug Console Serial Parameters. Product Information - Product ID. - Manufacturer ID Remove all the special settings such as different priority, but SEL will not remove. (Note: The BMC will reset itself after restore to default.)

5.7.4.1.1. Set Over Current Detect Command

Net Function = 3Ch (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
6Ah	Set Over Current Detect Command	**Request:** Byte 1 – 00h = Disable Over Current Detect. 01h = Enable Over Current Detect **Response:** Byte 1 – Completion code.	Change setting of current based FM_OC_DETECT_EN_N. This OEM command only for BIOS.

5.7.4.1.2. Get Over Current Detect Command

Net Function = 3Ch (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
6Bh	Get Over Current Detect Command	**Request: N/A** **Response:** Byte 1 – Completion code.	Read setting of current based FM_OC_DETECT_EN_N. The Over Current Detect default is disable (FM_OC_DETECT_EN_N = high).

Net Function = 3Ch (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
		Byte 2 – 00h = Disable Over Current Detect. 01h = Enable Over Current Detect.	

5.7.4.1.3. Get 80 Port Record Command

Net Function = 30h (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
49h	Get 80 Port Record	**Request: N/A** **Response:** Byte 1 – Completion code. Byte 2:N – POST code.	Replay the last port 80 POST codes (up to 256x POST records). N: maximum number = 256

5.7.4.1.4. Set DIMM Information Command

Net Function = 0x30 (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
0x1C	Set DIMM Information	**Request:** Byte 1:N – All DIMM information. **Response:** Byte 1 – Completion code.	Write DIMM type to BMC by BIOS. This OEM command only for BIOS.

5.7.4.1.5. Get DIMM Information Command

Net Function = 30h (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
1Dh	Get DIMM Information	**Request: N/A** **Response:** Byte 1 – Completion code. Byte 2:N – All DIMM information.	Read DIMM Type from BMC.

5.7.4.1.6. Get VR FW Version

Net Function = 30h (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
51h	Get VR FW Version	**Request:** Byte 1 – The VR controller desired 00: CPU0 VR 01: CPU1 VR 02: CPU0 DIMM0 VR 03: CPU0 DIMM1 VR 04: CPU1 DIMM0 VR 05: CPU1 DIMM1 VR **Response:** Byte 1 – Completion code. Byte 2:5 – VR checksum (LSB first)	BMC can provide the NVM Checksum stored in the BMC DRAM for the specific VR controller.

5.7.4.1.7. Store VR version To BMC

Net Function = 30h (OEM)			
Code	**Command**	**Request, Response Data**	**Description**
D3h	Store VR version To BMC	**Request: N/A** **Response:** Byte 1 – Completion code.	While the command is executed, BMC can send MFR_SERIAL (9EH) PMBUS command to obtain NVM checksums for all the VR controllers and store them into the BMC DRAM.

5.7.4.1.8. Set VR Monitor Enable Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
D2h	Set VR Monitor Enable	**Request:** Byte 1 – 00h = Disable BMC to get VRD related sensor information 01h = Enable BMC to get VRD related sensor information.(Default) **Response:**	Change setting of enable/disable CPU Vcore and memory VDDQ VR sensor polling. This OEM command only for update VRD tool

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
		Byte 1 – Completion code.	

5.7.4.1.9. Get VR Monitor Enable Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
D4h	Get VR Monitor Enable	**Request: N/A** **Response:** Byte 1 – Completion code. Byte 2 – 0 = Disable BMC to get VRD related sensor information 1 = Enable BMC to get VRD related sensor information.(Default)	Read setting of enable/disable CPU Vcore and memory VDDQ VR sensor polling. The VR monitor default setting is enabling.

5.7.4.1.10. Set First Time BIOS Boot Flag Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
40h	Set First Time BIOS Boot Flag	**Request:** Byte 1 – 01h = Set First Time BIOS Boot Flag **Response:** Byte 1 – Completion code.	For inband BIOS update utility to set flag for first time boot after an inband BIOS update action.

5.7.4.1.11. Set Preserve Configuration Command

Net Function = 32h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
83h	Set Preserve Configuration	**Request:** Byte 1 – Selector Byte 2 – 0 = Disable 1 = Enable **Response:** Byte 1 – Completion code.	Set BMC configuration to be preserved or not after BMC FW update. This command is for YAFU flash update tool.

5.7.4.1.12. Get Preserve Configuration Command

Net Function = 32h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
84h	Get Preserve Configuration	**Request:** Byte 1 – Selector **Response:** Byte 1 – Completion code. Byte 2 – 00h = Disable 01h = Enable	

5.7.4.1.13. Get CPLD Information Command

Net Function = 3Ch (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
88h	Get CPLD Information	**Request: N/A** **Response:** Byte 1 – Completion code. Byte 2 – CPLD version number. Byte 3:6 – Device ID(LSB first). Byte 7:10 – Checksum(LSB first).	Get CPLD version via CPLD SGPIO by BMC. Get CPLD Device ID via JTAG interface by BMC.

5.7.4.1.14. Set Network Sequence Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
B0h	Set Network Sequence	**Request:** Byte 1 – 00h = LOM (I210) is priority 1. Mezzanine card is priority 2. 01h = Mezzanine card is priority 1. LOM (I210) is priority 2. **Response:** Byte 1 – Completion code.	Change setting of OOB interface priority between LOM and Mezzanine card. BMC will apply the new priority at next AC reset or cold reset The default setting as following: LOM (I210) is priority 1 Mezzanine card is priority 2.

5.7.4.1.15. Get Network Sequence Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
B1h	Get Network Sequence	**Request: N/A** **Response:** Byte 1 – Completion code. Byte 2 – 00h = LOM (I210) is priority 1. Mezzanine card is priority 2. 01h = Mezzanine card is priority 1. LOM (I210) is priority 2.	Read setting of OOB interface priority. The Network sequence priority default is LOM (I210) (Byte 2 = 0).

5.7.4.1.16. Replay SOL Buffer Command

Net Function = 30h			
Code	**Command**	**Request/ Response Data**	**Description**
48h	Replay SOL Buffer	**Request: N/A** **Response:** Byte 1 – Completion code.	Replay last 16KB of SOL screen in SOL console. Use this command can display 5x last frames buffer when SOL session is connecting.

5.7.4.1.17. Set PPIN Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
77h	Set PPIN	**Request:** Byte 1 – CPU number (CPU#0: 00h, CPU#1: 01h) Byte 2-9 –VALUE-The 64 bit (bit 63:0) inventory number (MS-byte first). **Response:** Byte 1 – Completion code.	BMC would pull the SMI signal to low after BMC reset; BIOS shall serve the request by using This command to write PPIN of CPU0 and CPU1 to BMC. BIOS also Set_PPIN when BIOS POST COMPLETE. This OEM command only for BIOS.

5.7.4.1.18. Get PPIN Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
78h	Get PPIN	**Request:** Byte 1 – CPU number (CPU#0: 00h, CPU#1: 01h) **Response:** Byte 1 – Completion code. Byte 2:9 – VALUE-The 64 bit (bit 63:0) inventory number (MS-byte first).	Read PPIN from BMC. BMC default provides 0xFFFFFFFFFFFFFFFF for CPU 0/1.

5.7.4.1.19. Set PHY Reset Status Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
30h	Set PHY Reset Status	**Request:** Byte 1 – 00h = Disable PHY reset. 01h = Enable PHY reset. **Response:** Byte 1 – Completion code.	Change setting to enable/disable shared NIC PHY reset of all shared NICs during system warm reboot and DC cycle. This default setting is 0.

5.7.4.1.20. Get PHY Reset Status Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
31h	Get PHY Reset Status	**Request: N/A** **Response:** Byte 1 – Completion code. Byte 2 – 00h = Disable PHY reset. 01h = Enable PHY reset.	Read setting of keep NIC PHY link up feature of all shared NICs. This default setting is 0.

5.7.4.1.21. Set GPIO Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
E0h	Set GPIO	**Request:** Byte 1 – GPIO number(GPIOA0=0, GPIOA1=1, GPIOA2=2,…GPIOA7=7, GPIOB0=8……GPIOZ7=0xCF,GPIOAA0=0xD0..GPIOAB7=0xDF) Byte 2 – 00h = Config to GPO. 01h = Config to GPI. Byte 3 – output value for GPO **Response:** Byte 1 – Completion code	Set GPIO status

5.7.4.1.22. Get GPIO Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
E1h	Get GPIO	**Request:** Byte 1 – GPIO number(GPIOA0=0, GPIOA1=1, GPIOA2=2,…GPIOA7=7, GPIOB0=8……GPIOZ7=0xCF,GPIOAA0=0xD0..GPIOAB7=0xDF) **Response:** Byte 1 – Completion code. Byte 2 – 00h = Config to GPO. 01h = Config to GPI. Byte 3 – GPIO value.	Read GPIO status.

5.7.4.1.23. Get PIN Command

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
DFh	Get PIN	**Request:** Byte 1:2 –Duration time (LSB first), resolution of 0.1s. **Response:**	Read average PIN in any duration between 0.1 to 60 seconds

Net Function = 30h (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
		Byte 1 – Completion code. Byte 2:3 –Average power (LSB first), resolution of 0.1W.	

5.7.4.1.24. Get Board ID Command

Net Function = 3Ch (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
89h	Get Board ID	**Request:** N/A **Response:** Byte 1 – Completion code. Byte 2 – 09h = SKU1 0ah = SKU2 0bh = SKU3 0ch = SKU4	Read Board SKU ID pin status

5.7.4.1.25. Get FAB Revision ID Command

Net Function = 3Ch (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
8Ah	Get FAB Revision ID	**Request:** N/A **Response:** Byte 1 – Completion code. Byte 2 – 00h = R0A 01h = R0B 02h = R0C 04h = R0D 05h = R0E	Read Board REV ID pin status

Net Function = 3Ch (OEM)			
Code	**Command**	**Request/ Response Data**	**Description**
		06h = R0F 07h = R0G	

5.7.5. Standard IPMI Option Command Support

5.7.5.1.1. Chassis Identify command

This command causes the chassis to physically identify itself by a mechanism chosen by the system implementation. Unless the optional "Force Identify On" capability is supported and used, the *Chassis Identify* command automatically times out.

Request/ Response Data
Request: **Byte 1:** [7:0] - Identify Interval in seconds. 1-based. Timing accuracy = -0/+20%. This field is optional. If this byte is not provided the default timeout shall be 15 seconds -0/+20%. Note that this byte can be overridden by optional byte 2. 00h = Turn off Identify **Byte 2:** Force Identify On. This optional field enables software to command the Identify to be On indefinitely. The BMC implementation should return an error completion code if this byte is not supported. [7:1] - reserved [0] - 1b = Turn on Identify indefinitely. This overrides the values in byte 1. 0b = Identify state driven according to byte 1.
Response: Byte[1] : Completion code

5.8 Monitoring

5.8.1. Sensors

The Table below shows the IPMI sensors monitored on the Capri by the AST2500 BMC. Details of these sensor connections are described in the following sections. The following thresholds are defined by the IPMI2.0 specification

5.8.1.1. Sensor List

Sensor Name	Sensor Number [1]	Sensor Type [2]	Sensor Reading Type [3]	Sensor Record Type [3]	Sensor Owner ID	Entity ID	Entity / Instance	Assertion Event[6]
Threshold Sensors								
Outlet Temp	01H	01H	01H	01H	20H	07H	00H	UC
Inlet Temp	07H	01H	01H	01H	20H	07H	00H	UC
CPU Temp	05H	01H	01H	01H	20H	03H	00H	UC
CPU VR Temp	02H	01H	01H	01H	20H	14H	00H	UC
DIMM VR0 Temp	0BH	01H	01H	01H	20H	14H	02H	UC
DIMM VR1 Temp	0CH	01H	01H	01H	20H	14H	03H	UC
HSC Temp	0FH	01H	01H	01H	20H	07H	00H	UC
CPU VR PIN	11h	0BH	01H	01H	20H	03H	00H	UC
HSC Input Power	29H	0BH	01H	01H	20H	07H	00H	UC
HSC Output Curr	28H	03H	01H	01H	20H	07H	00H	UC
HSC Input Volt	2AH	02H	01H	01H	20H	07H	00H	LC,UC
CPU Pkg Power	2CH	0BH	01H	01H	20H	07H	00H	NA
CPU VR POUT	22H	0BH	01H	01H	20H	14H	00H	UC
CPU VR Curr	23H	03H	01H	01H	20H	14H	00H	UC
CPU VR Volt	24H	02H	01H	01H	20H	14H	00H	LC,UC
DIMM VR0 POUT	32H	0BH	01H	01H	20H	14H	02H	UC
DIMM VR0 Curr	33H	03H	01H	01H	20H	14H	02H	UC
DIMM VR0 Volt	34H	02H	01H	01H	20H	14H	02H	LC,UC
DIMM VR1 POUT	35H	0BH	01H	01H	20H	14H	03H	UC
DIMM VR1 Curr	36H	03H	01H	01H	20H	14H	03H	UC
DIMM VR1 Volt	37H	02H	01H	01H	20H	14H	03H	LC,UC
SYS FAN0	46H	04H	01H	01H	20H	1DH	00H	LC
SYS FAN1	47H	04H	01H	01H	20H	1DH	01H	LC
DIMM0 Temp	B4h	01H	01H	01H	20H	0AH	00H	UC
DIMM1 Temp	B5h	01H	01H	01H	20H	0AH	00H	UC
P3V3	D0H	02H	01H	01H	20H	07H	00H	LC,UC
P5V	D1H	02H	01H	01H	20H	07H	00H	LC,UC
P12V STBY	D2H	02H	01H	01H	20H	07H	00H	LC,UC
P3V3 AUX	D5H	02H	01H	01H	20H	07H	00H	LC,UC
P5V AUX	D6H	02H	01H	01H	20H	07H	00H	LC,UC
P3V BAT	D7H	02H	01H	01H	20H	07H	00H	LC,UC

Sensor Name	Sensor Number [1]	Sensor Type [2]	Sensor Reading Type [3]	Sensor Record Type [3]	Sensor Owner ID	Entity ID	Entity / Instance	Assertion Event[6]
Front U2SSD Temp	B9H	01H	01H	01H	20H	04H	00H	LC,UC
Rear U2SSD Temp	BAH	01H	01H	01H	20H	04H	00H	LC,UC
PCIe card Temp	64H	01H	01H	01H	20H	07H	00H	LC,UC
Discrete Sensors								
System Status	10H	0BH	6FH	02H	20H	07H	00H	[0]=1b, CPU0 socket occupied [2]=1b, CPU0 Thermal trip [7]=1b, System throttle
SEL Status	5FH	0BH	6FH	02H	20H	D0H	00H	02h, SEL Clear. 08h, SEL Rollover.
DCMI Watchdog	60H	23H	6FH	02H	20H	D0H	01H	[0]=1b, Timer expired [1]=1b, Hard Reset [2]=1b, Power Down [3]=1b, Power Cycle [8]=1b, Timer interrupt
Chassis Pwr Sts	70H	0BH	6FH	02H	20H	15H	00H	[0]=1b, Power Off/Power Down [1]=1b, Power Cycle [2]=1b, Power On [3]=1b, Soft-Shutdown [4]=1b, AC Lost [5]=1b, Hard Reset
Sys Booting Sts	7EH	0BH	6FH	02H	20H	07H	00H	~~[0]=1b, SLP S5~~ ~~[1]=1b, SLP S3~~ [3]=1b, SYS PWROK [4]=1b, Platform reset [5]=1b, BIOS post complete

Sensor Name	Sensor Number [1]	Sensor Type [2]	Sensor Reading Type [3]	Sensor Record Type [3]	Sensor Owner ID	Entity ID	Entity / Instance	Assertion Event[6]
VR HOT	B2H	0BH	6FH	02H	20H	14H	00H	[0]=1b, CPU0 core VR hot [2]=1b, CPU0 DIMM VR0 HOT [3]=1b, CPU0 DIMM VR1 HOT
HSC Sts Low	2EH	0BH	6FH	02H	20H	14H	00H	[0]=1b, NONEABOVE_STATUS [1]=1b, CML_FAULT [2]=1b, TEMP_FAULT [3]=1b, VIN UV FAULT [4]=1b, IOUT OC FAULT [5]=1b, VOUT OV FAULT [6]=1b, HOTSWAP_OFF [7]=1b, BUSY
HSC Sts High	2FH	0BH	6FH	02H	20H	14H	01H	[0]=1b, Unknown [1]=1b, Other [2]=1b, Fans [3]=1b, Power Good [4]=1b, MFR Specific [5]=1b, Input [6]=1b, Iout/Pout [7]=1b, Vout
CPU Error	91H	0BH	6FH	02H	20H	03H	00H	[3]=Thermal Trip

Sensor Name	Sensor Number [1]	Sensor Type [2]	Sensor Reading Type [3]	Sensor Record Type [3]	Sensor Owner ID	Entity ID	Entity / Instance	Assertion Event[6]
Front SSD Slot0	66H	0Dh	6FH	02H	20H	04H	01H	[0]=1b, Drive Presence [1]=1b, Drive Fault [2]=1b, Predictive Failure [3]=1b, Hot Spare [4]=1b, Parity Check In Progress [5]=1b, In Critical Array [6]=1b, In Failed Array [7]=1b, Rebuild In Progress
Front SSD Slot1	67H	0Dh	6FH	02H	20H	04H	02H	[0]=1b, Drive Presence [1]=1b, Drive Fault [2]=1b, Predictive Failure [3]=1b, Hot Spare [4]=1b, Parity Check In Progress [5]=1b, In Critical Array [6]=1b, In Failed Array [7]=1b, Rebuild In Progress
Front SSD Slot2	68H	0Dh	6FH	02H	20H	04H	03H	[0]=1b, Drive Presence [1]=1b, Drive Fault [2]=1b, Predictive Failure [3]=1b, Hot Spare [4]=1b, Parity Check In Progress [5]=1b, In Critical Array [6]=1b, In Failed Array [7]=1b, Rebuild In Progress

Sensor Name	Sensor Number [1]	Sensor Type [2]	Sensor Reading Type [3]	Sensor Record Type [3]	Sensor Owner ID	Entity ID	Entity / Instance	Assertion Event[6]
Front SSD Slot3	69H	0Dh	6FH	02H	20H	04H	04H	[0]=1b, Drive Presence [1]=1b, Drive Fault [2]=1b, Predictive Failure [3]=1b, Hot Spare [4]=1b, Parity Check In Progress [5]=1b, In Critical Array [6]=1b, In Failed Array [7]=1b, Rebuild In Progress
Rear SSD Slot0	6AH	0Dh	6FH	02H	20H	04H	05H	[0]=1b, Drive Presence [1]=1b, Drive Fault [2]=1b, Predictive Failure [3]=1b, Hot Spare [4]=1b, Parity Check In Progress [5]=1b, In Critical Array [6]=1b, In Failed Array [7]=1b, Rebuild In Progress
Rear SSD Slot1	6BH	0Dh	6FH	02H	20H	04H	06H	[0]=1b, Drive Presence [1]=1b, Drive Fault [2]=1b, Predictive Failure [3]=1b, Hot Spare [4]=1b, Parity Check In Progress [5]=1b, In Critical Array [6]=1b, In Failed Array [7]=1b, Rebuild In Progress

Sensor Name	Sensor Number [1]	Sensor Type [2]	Sensor Reading Type [3]	Sensor Record Type [3]	Sensor Owner ID	Entity ID	Entity / Instance	Assertion Event[6]
Rear SSD Slot2	6CH	0Dh	6FH	02H	20H	04H	07H	[0]=1b, Drive Presence [1]=1b, Drive Fault [2]=1b, Predictive Failure [3]=1b, Hot Spare [4]=1b, Parity Check In Progress [5]=1b, In Critical Array [6]=1b, In Failed Array [7]=1b, Rebuild In Progress
Rear SSD Slot3	6DH	0Dh	6FH	02H	20H	04H	08H	[0]=1b, Drive Presence [1]=1b, Drive Fault [2]=1b, Predictive Failure [3]=1b, Hot Spare [4]=1b, Parity Check In Progress [5]=1b, In Critical Array [6]=1b, In Failed Array [7]=1b, Rebuild In Progress
Rear SSD Slot4	6EH	0Dh	6FH	02H	20H	04H	09H	[0]=1b, Drive Presence [1]=1b, Drive Fault [2]=1b, Predictive Failure [3]=1b, Hot Spare [4]=1b, Parity Check In Progress [5]=1b, In Critical Array [6]=1b, In Failed Array [7]=1b, Rebuild In Progress

Sensor Name	Sensor Number [1]	Sensor Type [2]	Sensor Reading Type [3]	Sensor Record Type [3]	Sensor Owner ID	Entity ID	Entity / Instance	Assertion Event[6]
Rear SSD Slot5	6FH	0Dh	6FH	02H	20H	04H	0AH	[0]=1b, Drive Presence [1]=1b, Drive Fault [2]=1b, Predictive Failure [3]=1b, Hot Spare [4]=1b, Parity Check In Progress [5]=1b, In Critical Array [6]=1b, In Failed Array [7]=1b, Rebuild In Progress

Note:

Refer to IPMI 2.0 Table 43-1 byte 8

Refer to IPMI 2.0 Table 43-1 byte 13

Refer to IPMI 2.0 Table 43-1 byte 14

Refer to IPMI 2.0 Table 43-1 byte 9

Refer to IPMI 2.0 Table 43-1 byte 9

Refer to IPMI 2.0 Table 43-1 byte 15~20

Enabled condition: 0. Always Enable

1. Power on
2. BIOS sets SPD MUX to BMC
3. CPU is present
4. DIMM# is present

Capri sensor for Event-Only Sensors

Sensor Name	Sensor Number	Generator ID	Assertion Event

POST Error	0x2B	0x0001	**Event Data1:** [7:6] 10b or 11b [5:4] 10b [3:0] Offset 0x00 (System Firmware Error) **Event Data2:** ED1[7:6]= 10b, LSB of POST Error Code. ED1[7:6]= 11b, Per IPMI Spec. **Event Data3:** MSB of POST Error Code
Machine Chk Err	0x40	0x0001	**Event Data1:** [7:6]=10b [5:4]=10b [3:0]=0Bh, Uncorrectable Or 0Ch, Correctable **Event Data2:** Machine Check bank Number (Any one of 0 to 21) **Event Data3:** [7:5] CPU Number [4:0] Core Number

PCIe Error	0x41	0x0001	**Event Data1:** [7:6]=10b [5:4]=10b [3:0]= 04h = PCI PERR 05h = PCI SERR 07h, correctable 08h, uncorrectable 0Ah, Bus Fatal **Event Data2:** [7:3] Device Number [2:0] Func Number **Event Data3:** [7:0] Bus No
Other IIO Err	0x43	0x0001	**Event Data1:** [7:6] 10b [5:4] 10b [3:0] Offset 0x00 (Other IIO) **Event Data2:** [7:0] Error ID [Refer to Haswell EDS Vol1 Sec 11.1.7 IIO module error codes] **Event Data3:** [7:5] CPU Number [4:3] Reserved [2:0] Source 000b = IRP0 001b = IRP1 010b = IIO-Core 011b = VT-d 100b = Intel Quick data 101b = Misc Others = Reserved

Power Error	0x56	0x0020	**Event Data1:** [7:6]=00b [5:4]=00b [3:0]=Event offset: 01h, SYS_PWROK Failure **Event Data2:** FFh - Not Used **Event Data3:** FFh - Not Used
Memory Error	0x00	0x0021	Event Data1: [7:6] 10b – OEM Code in Byte2 [5:4] 10b – OEM Code in Byte3 [3:0] Sensor-Specific offset 00h – Correctable ECC 01h – Uncorrectable ECC 04h – Memory device disabled Event Data2: If ED1 = A0h or A1h ED2 [7:0] 00h: Memory type is ECC 10h: Memory type is parity 20h: Memory type is CRC If ED1= A4h ED2 [7:0] Reserved. Event Data3: [7:4] DIMM Channel (*1, see below) [3:0] Reserved.
Software NMI	0x90	0x0001	**Event Data1:** [7:6] 00b – Unspecified byte2 [5:4] 00b – Unspecified byte3 [3:0] 03h – Software NMI **Event Data2:** FFh - Not Used **Event Data3:** FFh - Not Used
Button	0xAA	0x0020	**Event Data1:** [7:4] 0h [3:0] 0h: Power button pressed 2h: Reset button pressed **Event Data2:** FFh - Not Used **Event Data3:** FFh - Not Used

Power State	0xAB	0x0020	**Event Data1:** [7:4] 0h [3:0] 0h: Transition to running 2h: Transition to power off **Event Data2:** FFh - Not Used **Event Data3:** FFh - Not Used
Power Policy	0xAC	0x0020	**Event Data1:** [7:6]=00b [5:4]=00b [3:0]=Event offset: 05h: Soft-power control failure **Event Data2:** FFh - Not Used **Event Data3:** FFh - Not Used
Network Status	0xB1	0x0020	**Event Data1:** [7:6]=00b [5:4]=00b [3:0]=Event offset: 00h, After BMC has IP assigned, and Both IPv4 and IPv6 network cannot ping gateway. BMC in disconnection state 01h, Either IPv4 or IPv6 can ping gateway after disconnection state **Event Data2:** FFh - Not Used **Event Data3:** FFh - Not Used

System Event	0xE9	0x0020	**Event Data1:**
			
			[7:0]=E5h, Timestamp Clock synch.
			
			[7:0]=C4h, PEF Action.
			Event Data2:
			
			if ED1 = E5h:
			
			0x00: event is first of pair
			
			0x80: event is second of pair
			
			if ED1 = C4h:
			
			0x1: PEF Action
			
			Event Data3:
			
			if ED1 = E5h:
			
			Cause of time changed:
			
			~~00h: NTP~~
			
			01h: Host RTC
			
			02h: Set SEL time command
			
			03h: Set SEL time UTC offset Command
			
			FFh: Unknown
			
			if ED1 = C4h:
			
			FFh

Critical IRQ	0xEA	0x0020	**Event Data1:** 00h, Front Panel NMI / Diagnostic Interrupt **Event Data2:** FFh - Not Used **Event Data3:** FFh - Not Used

Dual BIOS Up Sts	0xEF	0x0020	**Event Data1:** 01h: Auto Recovery 02h: Manual Recovery 03h: OOB Directly **Event Data2:** if ED1 = 01h 01h: ARB Timer timeout 02h: BIOS Good de-assert (GPIOAA5) if ED1 = 02h 03h: Recovery from Gold to primary 04h: Recovery from Primary to Gold if ED1 = 03h 05h: Primary directly 06h: Gold directly **Event Data3:** if ED2 = 01h or 02h 01h: Start the progress for recovery 02h: End the progress for recovery
ABR ERR	0x89	0x0020	**Event Data1:** 00h Primary flash booting fail.

*1: Instance to Mainboard DIMM channel Mapping

Instance ID	DIMM Channel / Event Data 3
00h (UMC0)	DIMM A / 00h
10h (UMC1)	DIMM B / 10h
20h (UMC2)	DIMM D / 30h
30h (UMC3)	DIMM C / 20h
40h (UMC4)	DIMM H / 70h
50h (UMC5)	DIMM G / 60h
60h (UMC6)	DIMM E / 40h
70h (UMC7)	DIMM F / 50h

OEM event log #1 definition for BIOS post code for ABR sensor (0x89) log when ABR ERR trigger

Byte	Field	Description
1 2	Record ID	ID used for SEL Record access.
3	Record Type	0xE0
4 5	Generator	0x20 0x00
6	Sensor Number	0x89
7	Latest BIOS Post code#1	xx
8	Latest BIOS Post code#2	xx
9	Latest BIOS Post code#3	xx
10	Latest BIOS Post code#4	xx
11	Latest BIOS Post code#5	xx
12	Latest BIOS Post code#6	xx
13	Latest BIOS Post code#7	xx
14	Latest BIOS Post code#8	xx
15	Latest BIOS Post code#9	xx
16	Latest BIOS Post code#10	Xx

Byte	Field	Description
1 2	Record ID	ID used for SEL Record access.
3	Record Type	0xE0
4 5	Generator	0x20 0x00
6	Sensor Number	0x89
7	Latest BIOS Post code#11	xx
8	Latest BIOS Post code#12	xx
9	Latest BIOS Post code#13	xx
10	Latest BIOS Post code#14	xx
11	Latest BIOS Post code#15	xx
12	Latest BIOS Post code#16	xx
13	Latest BIOS Post code#17	xx

14	Latest BIOS Post code#18	xx
15	Latest BIOS Post code#19	xx
16	Latest BIOS Post code#20	xx

The definition of Event Data 2/3 for Dual BIOS Up Sts (EFh) SEL

Event Data 2	Event Data 3
if ED1 = 01h 01h: FRB2 WDT timeout 02h: BIOS Good de-assert (GPION2) 07h: Watchdog not enable if ED1 = 02h 03h: Recovery from Gold to Primary 04h: Recovery from Primary to Gold if ED1 = 03h 05h: Primary directly 06h: Gold directly if ED1 = 04h 08h: BMC Self test failed 09h: Unexpected power off 0Ah: BMC ready pin deassert (GPIOQ4)	if ED2 = 01h or 02h 01h: Start the progress for recovery 02h: End the progress for recovery 03h: Checksum compare failed 04h: Primary BIOS is not present 05h: Gold BIOS is not present

If ED1 = 05h 03h: Recovery from Gold to Primary	

5.8.1.2. Threshold Table for analog Sensors (Raw Reading)

BMC has access to all analog sensors on Capri directly or through PCH Management Engine. All analog sensors need to be displayed in sensor data record (SDR) repository. Currently, some values are setup as the min/max values and will be provided later when it is available.

IPMI 2.0 Thresholds Specification

Term	Full Name	Description
LNR	Lower non-recoverable	Anything below causes power down
LC	Lower critical	Below this point , the shelf will take action
LNC	Lower non-critical	Above this point is the normal operating point
UNC	Upper non-critical	below this point is the normal operating point
UC	Upper critical	above this point the shelf will take action
UNR	Upper non-recoverable	anything above causes power down

Threshold Table for analog Sensors

Sensor Description	Sensor No.	LNR	LC (raw data)	LC (real value)	LNC	UNC	UC (raw data)	UC (real value)	UNR	Formula[1]
Outlet Temp	01H	—	0x5	5	10	70	0x4b	75	—	y=x
Inlet Temp	07H	—	0x5	5	10	40	0x2D	45	—	y=x
CPU Temp	05H	—	0x5	5	10	90	0x64	100	—	y=x
CPU VR Temp	02H	—	0x5	5	10	90	0x69	105	—	y=x
DIMM VR0 Temp	0BH	—	0x5	5	10	90	0x64	100	—	y=x
DIMM VR1 Temp	0CH	—	0x5	5	10	90	0x64	100	—	y=x
HSC Temp	0FH	—	0x5	5	10	90	0x64	100	—	y=x
CPU VR PIN	11h						0xB6	364		y=2x
HSC Input Power	29H	—	—	—	—	—	0xF9	647.4	—	y=2.6x
HSC Output Curr	28H	—	—	—	—	—	0xF0	48	—	y=0.2x
HSC Input Volt	2AH	—	0x71	11.3	—	—	0x84	13.2	—	y=0.1x
CPU Pkg Power	2CH	—	—	—	—	—	N/A	N/A	—	-
CPU VR POUT	22H	—	—	—	—	—	0x9B	310	—	y=2x
CPU VR Curr	23H	—	—	—	—	—	0xf0	264	—	y=1.1x
CPU VR Volt	24H	—	0x39	0.57	—	—	0x83	1.31	—	y=0.01x
DIMM VR0 POUT	32H	—	—	—	—	—	0xf0	129.6	—	y=0.54x
DIMM VR0 Curr	33H	—	—	—	—	—	0xe4	102.6	—	y=0.45x
DIMM VR0	34H	—	0x74	1.16	—	—	0x7e	1.26	—	y=0.01x

Sensor Description	Sensor No.	LNR	LC (raw data)	LC (real value)	LNC	UNC	UC (raw data)	UC (real value)	UNR	Formula[1]
Volt										
DIMM VR1 POUT	35H	—	—	—	—	—	0xf0	129.6	—	y=0.54x
DIMM VR1 Curr	36H	—	—	—	—	—	0xe4	102.6	—	y=0.45x
DIMM VR1 Volt	37H	—	0x74	1.16	—	—	0x7e	1.26	—	y=0.01x
SYS FAN0	46H		0x5	500						y=100x
SYS FAN1	47H		0x5	500						y=100x
DIMM0 Temp	B4h		0x5	5	10	80	0x55	85		y=x
DIMM1 Temp	B5h		0x5	5	10	80	0x55	85		y=x
P3V3	D0H	—	0xaf	2.993	—	—	0xd2	3.591	—	y=0.0171x
P5V	D1H	—	0xae	4.489	—	—	0xd5	5.495	—	y=0.0258x
P12V STBY	D2H	—	0x71	11.3	—	—	0x84	13.2	—	y=0.1x
P3V3 AUX	D5H	—	0xaf	2.993	—	—	0xd2	3.591	—	y=0.0171x
P5V AUX	D6H	—	0xae	4.489	—	—	0xd5	5.495	—	y=0.0258x
P3V BAT	D7H	—	0x80	2.701	—	—	0xab	3.608	—	y=0.0211x
Front U2SSD Temp	B9H		0x5	5.0	10	65	0x46	70		y=x
Rear U2SSD Temp	BAH		0x5	5.0	10	65	0x46	70		y=x
PCIe card Temp	64H	-	0x5	5	10	90	0x69	105	-	y=x

Note:

1. Refer to IPMI 2.0 Section 36.3, where: y: Converted reading x: Raw reading.

   Table 10 below provides the converted reading for maintenance.

2. 2's complement for negative value.

5.9 Event logging and Alerting

All of the system events are logged to an internal 64K bytes flash. However, Capri BMC does not support any alert mechanism based on manufacturer per-configured Alert Policy.

5.10 Chassis and Power Control

This section describes the chassis control mechanism of Capri platform. The related chassis commands are specified in IPMI v2.0 chapter 28.

5.10.1. Chassis Capabilities

Provides Monitoring Interrupt (NMI)

Chassis provides intrusion sensor

5.10.2. Chassis Control

The BMC must have ability to perform system power on/off and reset functions. These functions will be controlled externally through the IPMI chassis commands that described in the IPMIv2.0 specification. Including Get chassis capabilities, Get chassis status, and chassis control, these kind of commands are mandatory IPMI commands and must be implemented.

Power down

Power up

Power cycle

Hard Reset

5.10.3. Chassis Control

The BMC have ability to generate unique events in SEL for the below button response.

Host System State	Button Action
Powered on	Any button press Short press (<=5 sec)
Powered off	Long press (1min> time >5 sec) Button stuck (>1min)

5.11 LAN Configuration

For SNMP Traps related LAN configuration setting, please refer to IPMI v2.0 spec Chapter 23.2 Get LAN Configuration Parameters Command “Table 23-4 LAN Configuration Parameters”, because Capri BMC is following IPMI v2.0 spec definition to implement related function. Therefore Capri BMC can’t allow user to enter host name to set LAN configuration.

Parameter	#	Parameter Data (non-volatile unless otherwise noted)[1]
Destination Addresses	19	Sets/Gets the list of IP addresses that a LAN alert can be sent to. This parameter is not present if the Number of Destinations parameter is 0. data 1 - Set Selector = Destination Selector. [7:4] - reserved [3:0] - Destination selector. Destination 0 is always present as a volatile destination that is used with the *Alert Immediate* command. data 2 - Address Format [7:4] - Address Format. 0h = IPv4 IP Address followed by DIX Ethernet/802.3 MAC Address [3:0] - reserved For Address Format = 0h: data 3 - Gateway selector [7:1] - reserved [0] - 0b = use default gateway 1b = use backup gateway data 4:7 - Alerting IP Address (MS-byte first) data 8:13 - Alerting MAC Address (MS-byte first)
Following parameters are introduced with IPMI v2.0 / RMCP+ *VLAN configuration can be used with IPMI v1.5 and IPMI v2.0sessions. Parameters labeled "RMCP+" are specific to IPMI v2.0 implementations that implement IPMI v2.0 / RMCP+ sessions.*		
802.1q VLAN ID (12-bit)	20	data 1

5.11.1. Get / Set LAN Configuration Parameters

In order to reflect the capabilities provided by the BMC for some of the network settings, the values for some of the parameter data is defined as shown below.

5.11.1.1. DHCP

In addition to the usual methods of obtaining an IP address, the BMC provides a mode where it attempts to obtain an IP address from a DHCP server for a given period of time and if unsuccessful fails over to using a static IP address.

Parameter	#	Parameter Data
IP Address Source	4	data 1 [7:4] – reserved [3:0] – address source 0h = unspecified 1h = static address (manually configured) 2h = address obtained by BMC running DHCP 3h = address obtained by BIOS or system software 4h = address obtained by BMC running other address assignment protocol. The BMC will use the value 4h to indicate the address mode of DHCP with failover to static.

5.12 Port 80 POST

Capri BMC support port 80 POST code display to drive 8 bit HEX GPIO to debug header described. The BMC post function would ready before system BIOS starts to send 1st POST code to port 80.

BMC would access to POST code and record up to 256x POST codes. OOB raw command can be used to retrieve last 20x POST code from BMC.

5.13 LED Control by BMC

5.13.1. BMC Heartbeat LED

The BMC heartbeat LED will be blinking while BMC is alive, otherwise it must be deactivated while BMC's firmware is out of working.

5.13.2. UART Channel LED

BMC would control UART channel switch signal, and then this signal would direct to LED signal.

UART Channel LED

UART Channel	UART_LED1	UART_LED0
Host console	OFF	OFF
BMC debug console	OFF	ON
BMC UART2/IE UART	ON	OFF

5.13.3. Power and System Identification LED

The motherboard combines Power LED and System Identification LED to a single blue LED at front side.

Power LED on is defined by the readiness of major run time power rails (P12V, P5V, and P3V3) but NOT the readiness of all run time power rails; for example, CPU core power rail being ready is not required for Power LED on indication.

Power LED blinking is used as system identification. The on time is different during power on and power off.

There are 4 states of Power/system identification LED depending on system power state, and chassis identify status.

Power off, Chassis identify off: LED consistently off

Power off, Chassis identify on: LED on for 0.1sec, off for 0.9sec, and loop

Power on, Chassis identify off: LED consistently on

Power on, Chassis identify on: LED on for 0.9sec, off for 0.1sec, and loop

5.14 UART channel selection

When press UART switch, BMC shall be received the pulses, and control UART MUX to change Host UART console(Default)->BMC debug UART console->BMC UART2/IE UART console.

UART channel and connection

Channel	UART Connection
01	Host console
02	BMC debug console
03	BMC UART2/IE UART

5.15 BIOS Load default

Capri BMC is following IPMI standard *Boot Option Parameters* #5 data 2 bit 7 *to enable BIOS load default (set* CMOS clear) *for "Set System Boot Options Command"* in IPMI 2.0 spec *Table 28-14, Boot Option Parameters.*

5.16 BMC Firmware Update

Capri BMC supports in-band and out-of-band flashing of the BMC firmware via related tools.

5.16.1. BMC Firmware Update tools

User is able to update BMC by the following manners.

These utilities should be workable for FW update.

Yafuflash (4.15 or above) via local USB or remote host via network for below OS:

Linux (CentOS 6.8/7.3 64-bit).

Socflash: provide by Aspeed.

Linux (CentOS 6.8/7.3 64-bit)

DOS based

5.16.2. CPLD Code Update

Capri BMC can access motherboard CPLD through JTAG and perform CPLD code upload from remote control server to BMC, update code from BMC to CPLD through CPLD JTAG interface. All the steps above shall be done from an update utility that supports CentOS 6.4 64-bit with updated Kernel specified by customer. BMC support OEM command to read CPLD code device ID, and version number.

5.17 Software Scheme

Auto BIOS recovery from backup flash to primary flash:

When 1st boot up after BIOS FW update fails and BMC watch dog timer (WDT) times out, BMC

determine BIOS needs recovery, takes over control of flash access and duplicate backup flash

content to primary flash.

Manual BIOS recovery from backup flash to primary flash :

User to use IPMI OEM command to trigger BMC taking over control of flash access and duplicate

backup flash content to primary flash.

Manual BIOS save from primary flash to backup flash:

User to use IPMI OEM command to trigger BMC taking over control of flash access and duplicate

primary flash to backup flash.

Manual Mux control:

User to use IPMI OEM command to trigger BMC to change of the state of two multiplexers.

Manual BIOS recovery from network to flash

User to use IPMI OEM command to trigger a BIOS SPI flash binary to be transferred to BMC and

written to primary or secondary flash, depending on the state of multiplexer.

Enable/Disable Auto BIOS recovery

User to use IPMI OEM command to Enable and Disable feature of Auto BIOS recovery from backup flash to primary flash:

Get dual BIOS feature status:

User to use IPMI OEM command to get current state of two multiplexers, and Auto recovery

Enable/Disable status.

Get dual BIOS version:

User to use IPMI OEM command to access and return BIOS version of both primary and

secondary flash.

5.17.1. Auto Recovering BIOS

Capri is a dual bios system and BMC provides a BIOS auto recovering feature that it will automatically switch to the second bios if there is a crash/unexpected interruption occurred while updating bios. This chapter specifies what kinds of functions are required and explains how the auto recovering bios process performs.

5.18 Other Settings

5.18.1. I210 NCSI Setting

The “Keep_PHY_Link_Up_En” is enabled in current I210 image, so BMC will enable “Critical Session mode” by “Enable PHY Link Up” OEM command to force PHY link not reset by PCIe reset.

The *Keep_PHY_Link_Up* bit is set by the MC through the Management Control command (refer to Section 10.5.9.1.5 for SMBus command and Section 10.6.3.10 for NC-SI command) on the sideband interface. It is cleared by the external MC (again, through a command on the sideband interface) when the manageability session ends. Once the *Keep_PHY_Link_Up* bit is cleared, the PHY updates its Dx state and acts accordingly (negotiates its speed).

10.6.3.10 Set Intel Management Control Formats

10.6.3.10.1 Set Intel Management Control Command (Intel Command 0x20)

	Bits			
Bytes	31:24	23:16	15:08	07:00
00...15	NC-SI Header			
16...19	Manufacturer ID (Intel 0x157)			
20...22	0x20	0x00	Intel Management Control 1	

Where Intel Management Control 1 is as follows:

Bit #	Default value	Description
0	0b	Enable Critical Session Mode (Keep PHY Link Up and Veto Bit) 0b — Disabled 1b — Enabled When critical session mode is enabled, the following behaviors are disabled: • The PHY is not reset on PE_RST# and PCIe resets (in-band and link drop). Other reset events are not affected — Internal_Power_On_Reset, device disable, Force TCO, and PHY reset by software. • The PHY does not change its power state. As a result link speed does not change. • The device does not initiate configuration of the PHY to avoid losing link.
1...7	0x0	Reserved

Field	Bit(s)	Initial Value	Description
KEEP_PHY_LINK_UP	18	0b[1]	Block PHY reset and power state changes. When this bit is set, the PHY reset and power state changes do not effect the PHY, This bit can not be written to unless the *Keep_PHY_Link_Up_En* Flash bit is set.

5.19 MCA dump

Capri BMC would dump MCA from both CPUs through PECI. This is a debug feature to allow the user to get critical debug information from faulty SUT on a server rack, without removing the system from a failure status and risking the loss of critical debug information. BMC firmware would perform MCA dump automatically when the CATERR_N/MSMI_N be asserted. The BMC would store the MCA dump data x3 in BMC flash.

5.20 BMC Network Status

BMC add one sensor #0xB1 with ED1=00/01 for LAN detection, expected behavior of this feature as following:

After BMC FW get IP address from DHCP server, BMC FW ping default GW IP.

If ping keep failed over 10x10 seconds , there will be ED1=00h SEL assertion event.

(Note: If ping successfully within 100 seconds, should not generate SEL log.)

Until ping successfully, then BMC generate ED=01h SEL event for de-assertion.

5.21 BMC Time Sync

In the Capri platform, BIOS should send 'Set SEL Time' command to set the BMC time during POST.

5.22 Average Power Reporting

After BMC FW ready, BMC keeps sampling READ_EIN_EXT readings in one second interval until 60 readings in buffer.

Then go on sampling reading and over-write old data to keep 60 readings in buffer.

Run Get_PIN OEM command, BMC will output average value of 60 readings in buffer by ASCII format. (example:

"1234.5" W)

There is a limitation that before BMC got 60 readings for average, there will be error response for command execution.

So after AC on, user needs to wait BMC ready plus around 60 seconds for sampling then this OEM command could work normally.

5.23 BMC Secure boot

There are two BMC flashes for BMC secure boot mechanism:

1. Primary flash FW – contains secure FW and golden BMC image

2. Secondary flash FW – contains signature FW image used for booting.

BMC FW boots from 1st flash for verifying signature of 2nd flash image.

If 2nd flash FW image is verified passed with signature, then booting process switch back to 2nd flash and go on normal booting.

If 2nd flash FW image is verified failed with signature, then secure FW stop booting process and proceed to program golden image into 2nd flash and continue FW booting process by 2nd flash golden image.

Note:

1. There is extra time (around 30 seconds) for BMC FW booting due to secure verification; if secure FW verified 2nd flash image failed, the extra BMC booting time is around 210 seconds due to re-program 2nd flash image by golden image.

2. If remove 2nd flash from socket, BMC FW booting will be stuck on booting process.

6. Thermal Design Requirements

To meet thermal reliability requirements, the thermal and cooling solution should dissipate heat from the components when the system operating at its maximum thermal power. The thermal solution should be found by setting a high power target for initial design in order to avoid redesign of cooling solution; however, the final thermal solution of the system should be most optimized and energy efficient under data center environmental conditions with the lowest capital and operating costs. The thermal solution should not allow any overheating issues for any components in the system. CPU or memory should not throttle due to any thermal issue under the following environment:

- Inlet temperature lower than or equal to 35°C, and 0 inch H 2 O datacenter pressure with all FANs in each thermal zone running properly

6.1 Data Center Environmental Conditions

The thermal design for Capri needs to satisfy the data center operational conditions as described below.

6.1.1. Location of Data Center/Altitude

Data centers may be located 3050 meters above sea level or higher. Any variation of air properties or environmental difference due to the high altitude needs to be considered when creating the thermal design.

6.1.2. Cold-Aisle Temperature

Data centers will generally maintain cold aisle temperatures between 18°C and 30°C (65°F to 85°F). The mean temperature in the cold aisle is 24°C with 3°C standard deviation. The cold aisle temperature in a data center may fluctuate minutely depending to the outside air temperature of the data center. Every component in the system must be cooled and maintained below its maximum specified temperature in any cold aisle temperature in a data center.

6.1.3. Cold-Aisle Pressurization

Data centers will maintain the cold aisle pressure to be between 0” H 2 O and 0.005” H 2 O. The thermal solution of the system accommodates the worst-case operational pressurization in the data centers, which is 0" H2O with no fan failures.

6.1.4. R.H

Most data centers will maintain the relative humidity to be between 20% and 90%. The thermal solution must sustain uninterrupted operation of the system across the aforementioned RH range. Server operational condition

6.2 Server operational condition

6.2.1. System Loading

The power consumption of individual components on the system motherboard will vary by application or by motherboard SKU. The total system power consumption may vary with use or with the number of existence of PCIe cards on the system:

- System Loading: idle to 100%
- Number of PCIe full height or half height cards that can be installed: 0 to 2
- Number of PCIe Mezz cards that can be installed: 0 to 1
- Number of 2.5” HDD: 0 to 10

Plan of record worst case configuration for thermal and power delivery design is 1 x 225W TDP CPU with 8 x 128GB DDR4 DIMM, or 8x 64GB DDR4 DIMM.

A unified thermal solution that can cover 100% of system loading is preferred. However, an ODM can propose non-unified thermal solution if there is alternative way to provide cost benefits. At least the air-duct design should be unified for all SKU.

6.2.2. DDR DIMM DRAM Operation

Thermal design should meet DIMM maximum operating temperature as 85°C with single refresh rate. Thermal test should be done based on a DIMM module's AVL (Approved Vendor List). The vendor should implement BIOS and memory subsystem to have optimized refresh rate and utilize optional DIMM Auto-Self-Refresh (ASR) based on DIMM temperature. The implementation should follow updated DDR4 memory controller and DIMM vendor's specification.

6.2.3. Inlet Temperature

The inlet air temperature will vary. The cooling system should cover inlet temperatures at 20°C, 25°C, 30°C, and 35°C. Cooling above 30°C is beyond operating specification, but used during validation to demonstrate design margin. CPU throttling is not allowed to activate over the validation range 0°C – 35°C.

6.2.4. Pressurization

Except for the condition of a single rotor in a server fan failing, the thermal solution should not be found with considering extra airflow from a data center cooling system. If and only if one rotor in server fan fails, the negative or positive DC pressurization can be considered in the thermal solution in the hot aisle or in cold aisle respectively.

6.2.5. System Airflow or Volumetric Flow

The unit of airflow (or volumetric flow) used for this spec is CFM (cubic feet per minute). The maximum allowable airflow per watt in the system must be 0.107. The desired airflow per watt is 0.1 or lower in the system at the mean temperature (plus or minus standard deviation). See section 7.1.2 for the temperature definitions.

6.2.6. Delta T

The delta T is the air temperature difference across the system or the temperature difference between outlet air temperature of system and inlet air temperature of system. The desired rack-level delta T must be greater than 13.9°C (25°F). The desired server-level delta T is 17°C (31°F) when the inlet air temperature to the system is equal to or lower than 30°C.

6.2.7. Thermal Margin

The thermal margin is the difference between the maximum theoretical safe temperature and the actual temperature. The board design operates at an inlet temperature of 35°C (95°F) outside of the system with a minimum 2% thermal margin for every component in the system. Otherwise, the thermal margin for every component in the system is at least 7% for temperatures up to 30°C.

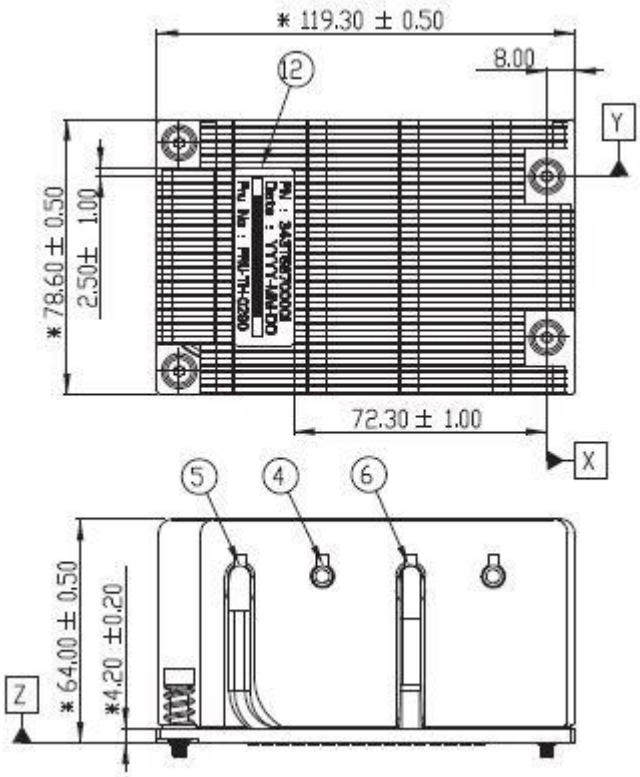
6.3 Thermal Kit Requirements

Thermal testing must be performed at up to 35°C (95°F) inlet temperature to guarantee high temperature reliability.

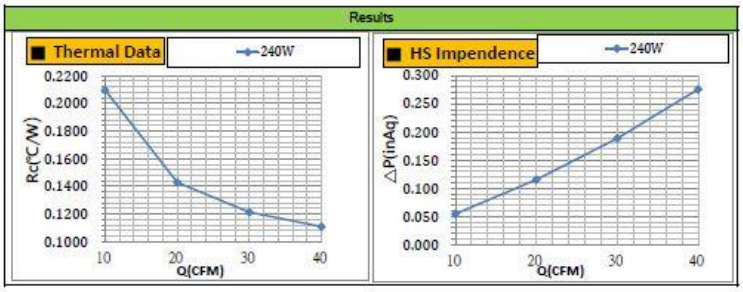
6.3.1. Heat Sink

The heat sink design should choose to be most optimized design with lowest cost. The heat sink design should be reliable and the most energy efficient design that satisfies all the conditions described above. The number of heat

pipes in the heat sink should not be more than three. The ODM can always propose for different heat sink type if there is alternative way to provide cost benefits. The heat sink should be without complex installation guidance, such as air-flow direction.



Thermal performace Test (Taisol)						
item	condition					
1. Test System	Wind Tunnel					
2. Grease	TC5026 t=0.15 mm					
3. Heat source	TTV					
4. Power	240 watt					
5. Air Flow	10 - 20 - 30 - 40 CFM					
Results						
240W						
CFM	Tc(℃)	Ta	ΔTca	W	Rca(℃/W)	△P(inAq)
10	72.70	22.4	50.3	240	0.2096	0.0546
20	56.50	22.2	34.3	240	0.1429	0.1154
30	51.40	22.3	29.1	240	0.1213	0.1886
40	48.60	22.0	26.6	240	0.1108	0.2758

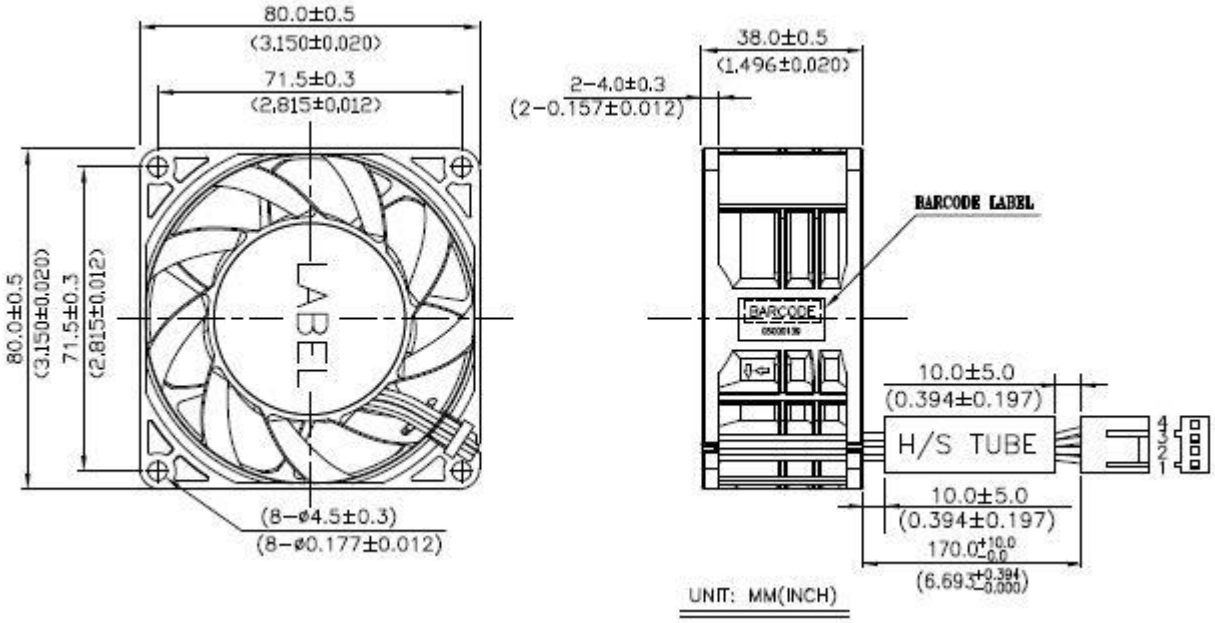


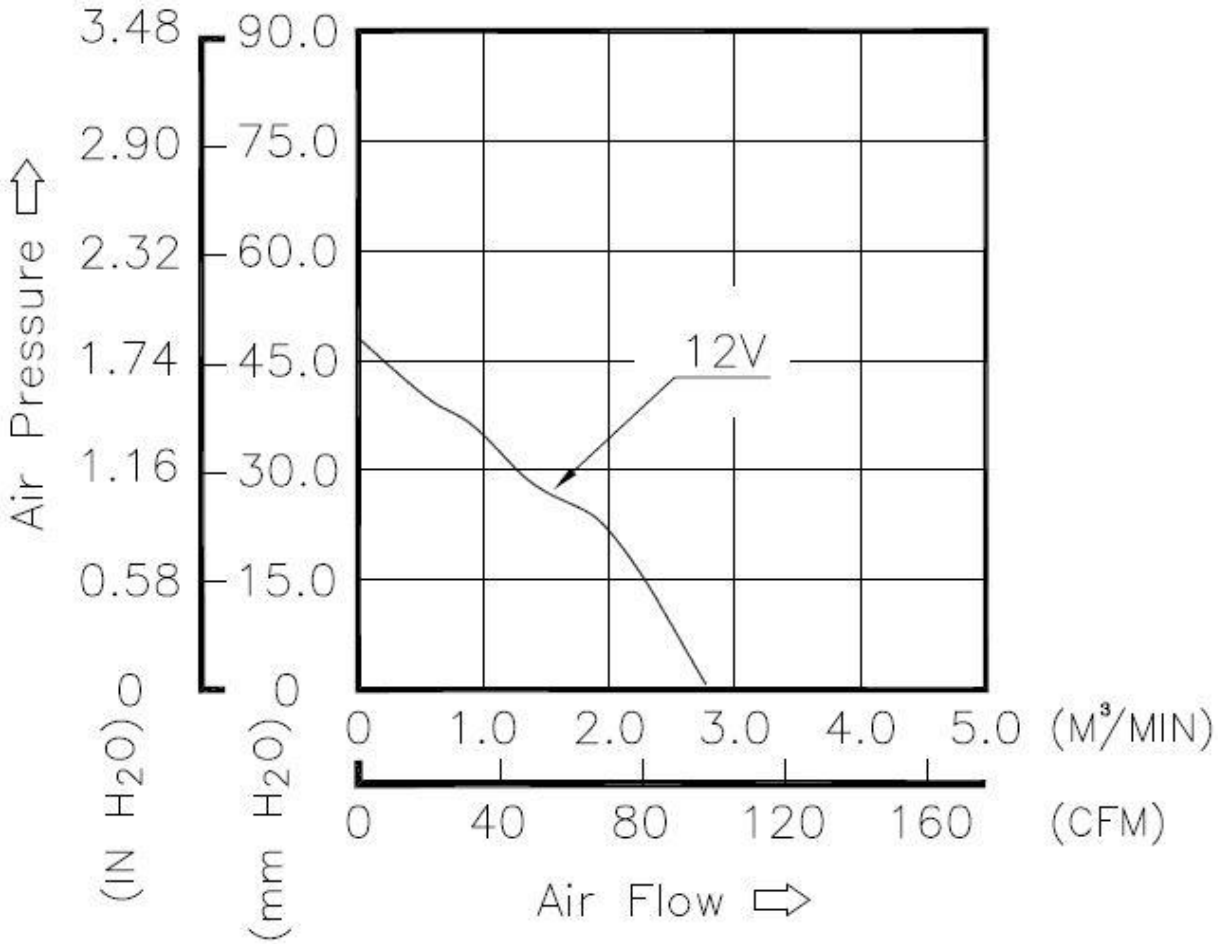
6.3.2. System Fan

The system fan must be highly power-efficient. The propagation of vibration cause by fan rotation should be minimized and limited. The minimum frame size of fan is 60x60mm and the maximum frame size is 80x80mm. ODM can propose larger frame size of fan than 80x80mm if and only if there is alternative way to provide cost benefits. The maximum thickness of fan should not be greater than 38mm. Each rotor in the fan should have a maximum of five wires. Except for the condition when one fan (or one rotor) fails, the fan power consumption in system should not be exceeding 5% of total system power excluding the fan power. System fan should not have back rush current in all condition. System fan should have an inrush current of less than 1A on 12V per fan. When there is a step change on fan PWM signal from low PWM to high PWM, there should be less than 10% of overshoot

or no overshoot for fan input current. System should stay within its power envelope (300W for Open Rack V1 configure) in all condition of fan operation.

ITEM	DESCRIPTION
RATED VOLTAGE	12 VDC
OPERATION VOLTAGE	11.25 - 13.75 VDC
INPUT CURRENT	1.60 (1.92 MAX.) A (SAFETY CURRENT 2.54A)
INPUT POWER	19.20 (23.04 MAX.) W
SPEED	10000±10% R.P.M.
MAX. AIR FLOW (AT ZERO STATIC PRESSURE)	2.76 (MIN. 2.48) M^3/MIN 97.780(MIN. 88.00) CFM
MAX.AIR PRESSURE (AT ZERO AIR FLOW)	47.72 (MIN. 38.65) mmH_2O 1.878 (MIN. 1.521) inH_2O
ACOUSTICAL NOISE (AVG.)	66.0 (MAX 70.0) dB-A
INSULATION TYPE	UL: CLASS A


80.0±0.5
(3.150±0.020)
71.5±0.3
(2.815±0.012)
LABEL
(8-ø4.5±0.3)
(8-ø0.177±0.012)
38.0±0.5
(1.496±0.020)
2-4.0±0.3
(2-0.157±0.012)
BARCODE LABEL
BARCODE
10.0±5.0
(0.394±0.197)
H/S TUBE
170.0
UNIT: MM(INCH)


Air Pressure
(IN H2O)
(mm H2O)
3.48
2.90
2.32
1.74
1.16
0.58
0
90.0
75.0
60.0
45.0
30.0
15.0
0
12V
0 1.0 2.0 3.0 4.0 5.0 (M3/MIN)
0 40 80 120 160 (CFM)
Air Flow

6.3.3. Air-Duct

The air duct needs to be part of the motherboard tray cover, and must be most energy efficient design. The air-duct design should be simple and easily serviceable. The air-duct design should be unified for all SKUs. Using highly green material or reusable material for the air duct is preferred.

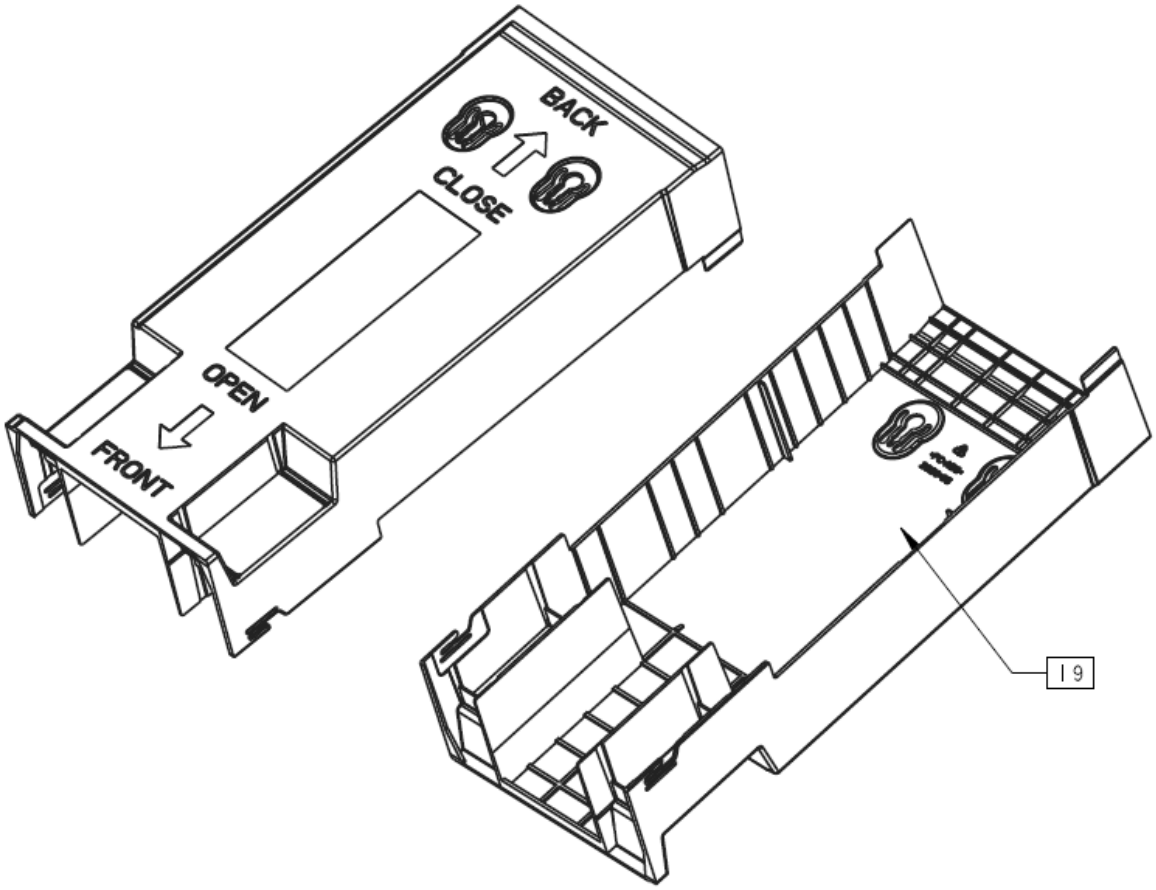


Figure 10 MiTAC E8020 Capri Air-Duct Figure

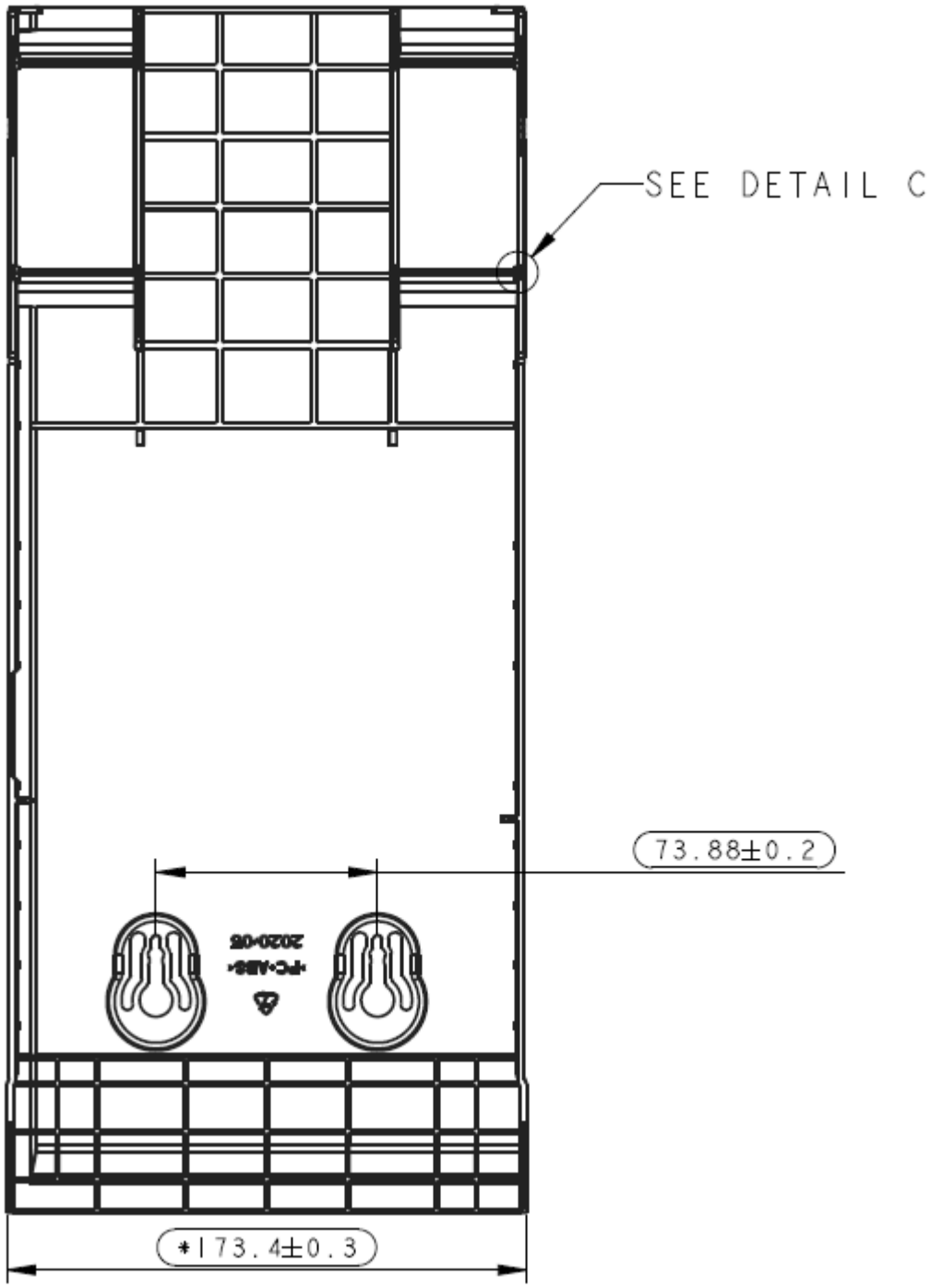


Figure 11 MiTAC E8020 Capri Top View

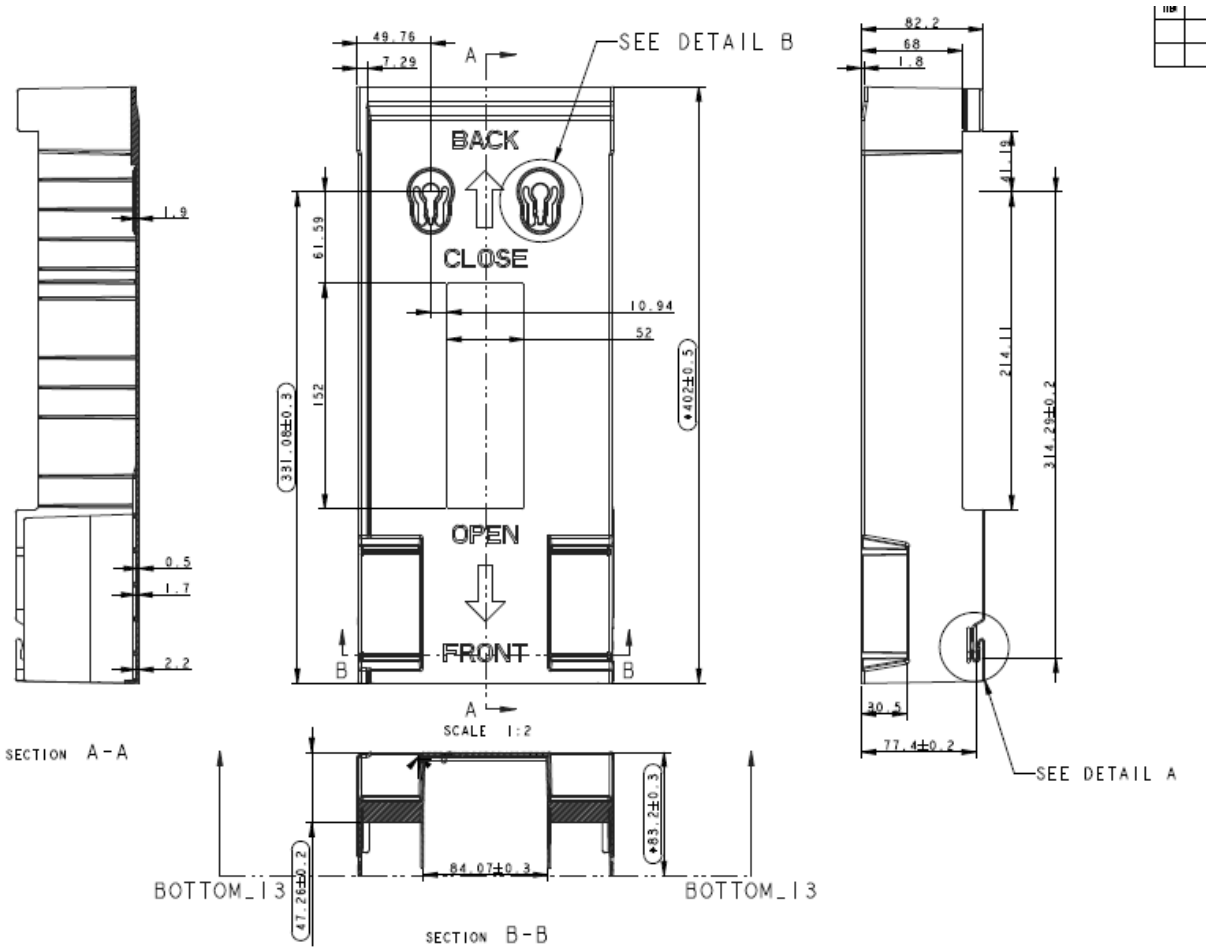


Figure 12 MiTAC E8020 Capri Dimension (B Detail)

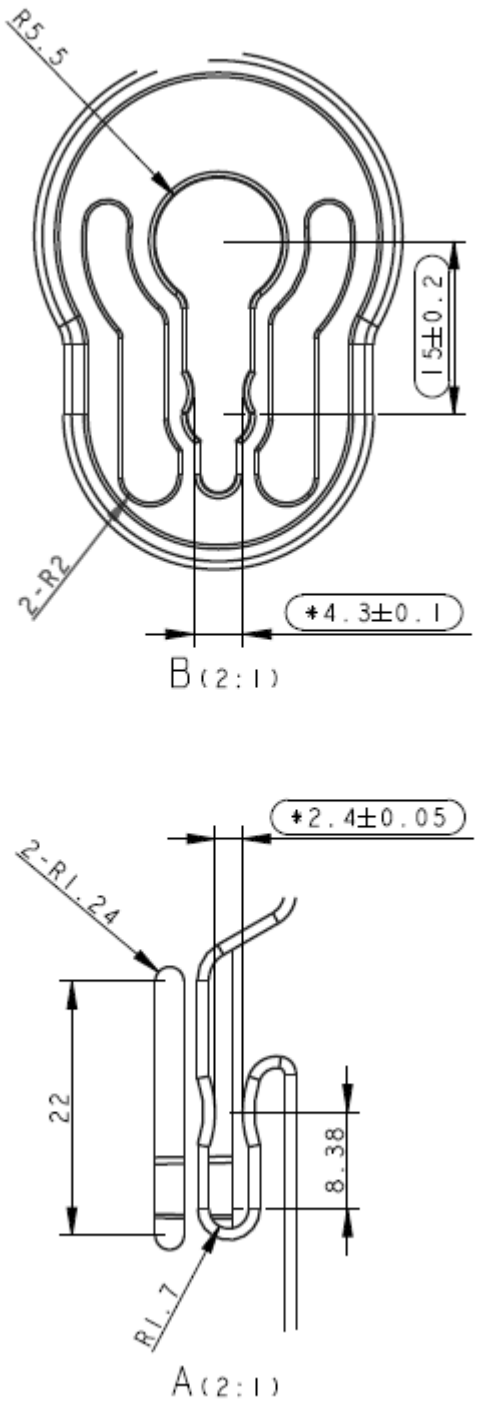


Figure 13 MiTAC E8020 Capri Dimension (A detail)

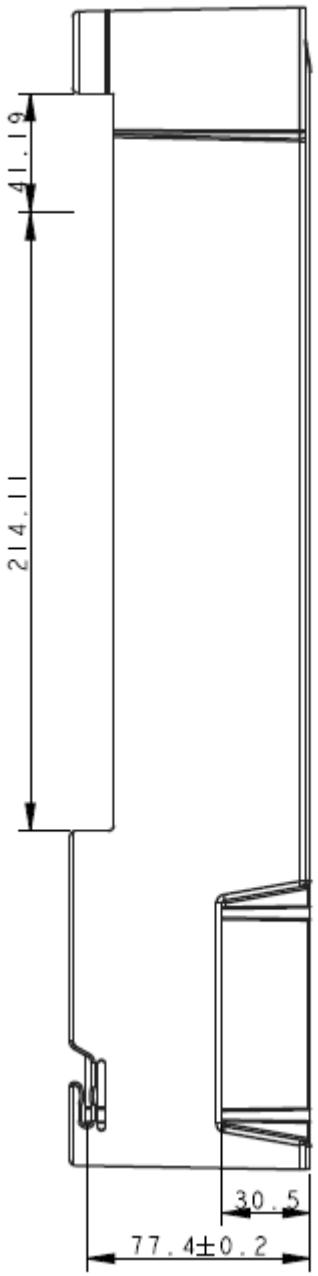


Figure 14 MiTAC E8020 Capri Dimension (Side View Detail 1)

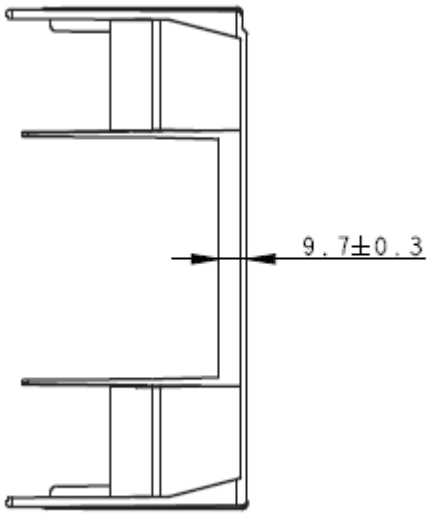


Figure 15 MiTAC E8020 Capri Dimension (Side View Detail 2)

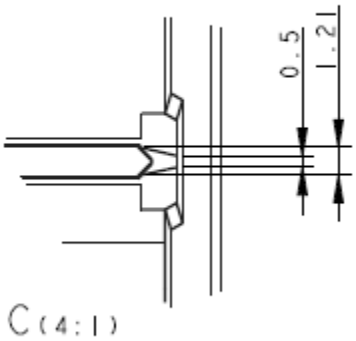


Figure 16 MiTAC E8020 Capri Dimension (C Detail)

6.3.4. Thermal sensor

The maximum allowable tolerance of thermal sensors in the motherboard is ±3°C.

7. I/O System

7.1 PCIe x32 Slot/Riser Card

7.1.1 Riser slot interface between riser card and motherboard

Two riser cards are used in this motherboard and two single, 2 X sockets are used by PCIE riser cards:

(1) A X 32 slot SAMTEC/ HSEC8-1100-01-L-DV-A-K (280pin) is used for X32 PCIE and power delivery

(2) A X 32 slot Samtec/SE102802611106X (280pin) is used for X24 PCIE and power delivery Slot location must follow mechanical requirement that will be delivered in DXF format.

All PCIE lanes to X32 PCIE is from CPU0. SUMBUS to PCIE host SUMBUS; SMB_CPU_HP_ALERT_N from CPU to PCIE SLOT SMB_CPU_HP_ALERT_N_R1&2&3 (PIN S27)

2U Riser Board x32 (J32) SAMTEC/ **HSEC8-1100-01-L-DV-A-K**			
2	P12V	1	P12V
4	P12V	3	P12V
6	P12V	5	P12V
8	P12V	7	P12V
10	P12V	9	P12V
12	P12V	11	P12V
14	GND	13	GND
16		15	SMB_FRONT_X32_SDA
18	FM_SLT_CFG1	17	SMB_FRONT_X32_CLK
20	FM_PWRBRK_SLOT_N	19	FM_SLT_CFG0
22	P3V3	21	P3V3
24	P3V3	23	P3V3
26	GND	25	P3V3_AUX
28	FM_PE_SLOTX24_WAKE_N	27	SMB_CPU_HP_ALERT_N
30	SMB_HOST_STBY_LVC3_SDA	29	RST_PCIE_FRONT_X32_N
32	SMB_HOST_STBY_LVC3_SCL	31	GND
34	GND	33	CLK_100M_PCIE_R1_DP
36	CLK_100M_PCIE_R2_DP	35	CLK_100M_PCIE_R1_DN
38	CLK_100M_PCIE_R2_DN	37	GND
40	GND	39	CLK_100M_PCIE_R3_DP
42	CLK_100M_PCIE_SSD_R4_DP	41	CLK_100M_PCIE_R3_DN
44	CLK_100M_PCIE_SSD_R4_DN	43	GND
46	GND	45	CLK_100M_PCIE_SSD_R5_DP
48	CLK_100M_PCIE_SSD_R6_DP	47	CLK_100M_PCIE_SSD_R5_DN
50	CLK_100M_PCIE_SSD_R6_DN	49	GND

52	GND	51	P3E_PCIE2_RISER_TX_DP<0>
54	P3E_CPU0_PE2_RX_DP<0>	53	P3E_PCIE2_RISER_TX_DN<0>
56	P3E_CPU0_PE2_RX_DN<0>	55	GND
58	GND	57	P3E_PCIE2_RISER_TX_DP<1>
60	P3E_CPU0_PE2_RX_DP<1>	59	P3E_PCIE2_RISER_TX_DN<1>
62	P3E_CPU0_PE2_RX_DN<1>	61	GND
64	GND	63	SMB_HP_LVC3_SCL
66	SMB_HP_LVC3_SDA	65	GND
68	GND	67	P3E_PCIE2_RISER_TX_DP<2>
70	P3E_CPU0_PE2_RX_DP<2>	69	P3E_PCIE2_RISER_TX_DN<2>
72	P3E_CPU0_PE2_RX_DN<2>	71	GND
74	GND	73	P3E_PCIE2_RISER_TX_DP<3>
76	P3E_CPU0_PE2_RX_DP<3>	75	P3E_PCIE2_RISER_TX_DN<3>
78	P3E_CPU0_PE2_RX_DN<3>	77	GND
80	GND	79	FM_FRONT_RISERX32_PRSNT_N
82	GND	81	GND
84	P3E_CPU0_PE2_RX_DP<4>	83	P3E_PCIE2_RISER_TX_DP<4>
86	P3E_CPU0_PE2_RX_DN<4>	85	P3E_PCIE2_RISER_TX_DN<4>
88	GND	87	GND
90	P3E_CPU0_PE2_RX_DP<5>	89	P3E_PCIE2_RISER_TX_DP<5>
92	P3E_CPU0_PE2_RX_DN<5>	91	P3E_PCIE2_RISER_TX_DN<5>
94	GND	93	GND
96	P3E_CPU0_PE2_RX_DP<6>	95	P3E_PCIE2_RISER_TX_DP<6>
98	P3E_CPU0_PE2_RX_DN<6>	97	P3E_PCIE2_RISER_TX_DN<6>
100	GND	99	GND
102	P3E_CPU0_PE2_RX_DP<7>	101	P3E_PCIE2_RISER_TX_DP<7>
104	P3E_CPU0_PE2_RX_DN<7>	103	P3E_PCIE2_RISER_TX_DN<7>
106	GND	105	GND
108	P3E_CPU0_PE2_RX_DP<8>	107	P3E_PCIE2_RISER_TX_DP<8>
110	P3E_CPU0_PE2_RX_DN<8>	109	P3E_PCIE2_RISER_TX_DN<8>
112	GND	111	GND
114	P3E_CPU0_PE2_RX_DP<9>	113	P3E_PCIE2_RISER_TX_DP<9>
116	P3E_CPU0_PE2_RX_DN<9>	115	P3E_PCIE2_RISER_TX_DN<9>
118	GND	117	GND
120	P3E_CPU0_PE2_RX_DP<10>	119	P3E_PCIE2_RISER_TX_DP<10>
122	P3E_CPU0_PE2_RX_DN<10>	121	P3E_PCIE2_RISER_TX_DN<10>
124	GND	123	GND
126	P3E_CPU0_PE2_RX_DP<11>	125	P3E_PCIE2_RISER_TX_DP<11>

128	P3E_CPU0_PE2_RX_DN<11>	127	P3E_PCIE2_RISER_TX_DN<11>
130	GND	129	GND
132	P3E_CPU0_PE2_RX_DP<12>	131	P3E_PCIE2_RISER_TX_DP<12>
134	P3E_CPU0_PE2_RX_DN<12>	133	P3E_PCIE2_RISER_TX_DN<12>
136	GND	135	GND
138	P3E_CPU0_PE2_RX_DP<13>	137	P3E_PCIE2_RISER_TX_DP<13>
140	P3E_CPU0_PE2_RX_DN<13>	139	P3E_PCIE2_RISER_TX_DN<13>
142	GND	141	GND
144	P3E_CPU0_PE2_RX_DP<14>	143	P3E_PCIE2_RISER_TX_DP<14>
146	P3E_CPU0_PE2_RX_DN<14>	145	P3E_PCIE2_RISER_TX_DN<14>
148	GND	147	GND
150	P3E_CPU0_PE2_RX_DP<15>	149	P3E_PCIE2_RISER_TX_DP<15>
152	P3E_CPU0_PE2_RX_DN<15>	151	P3E_PCIE2_RISER_TX_DN<15>
154	GND	153	GND
156	P3E_CPU0_PE3_RX_DN<0>	155	P3E_PCIE3_RISER_TX_DN<0>
158	P3E_CPU0_PE3_RX_DP<0>	157	P3E_PCIE3_RISER_TX_DP<0>
160	GND	159	GND
162	GND	161	P3E_PCIE3_RISER_TX_DN<1>
164	P3E_CPU0_PE3_RX_DN<1>	163	P3E_PCIE3_RISER_TX_DP<1>
166	P3E_CPU0_PE3_RX_DP<1>	165	GND
168	GND	167	P3E_PCIE3_RISER_TX_DN<2>
170	P3E_CPU0_PE3_RX_DN<2>	169	P3E_PCIE3_RISER_TX_DP<2>
172	P3E_CPU0_PE3_RX_DP<2>	171	GND
174	GND	173	P3E_PCIE3_RISER_TX_DN<3>
176	P3E_CPU0_PE3_RX_DN<3>	175	P3E_PCIE3_RISER_TX_DP<3>
178	P3E_CPU0_PE3_RX_DP<3>	177	GND
180	GND	179	P3E_PCIE3_RISER_TX_DN<4>
182	P3E_CPU0_PE3_RX_DN<4>	181	P3E_PCIE3_RISER_TX_DP<4>
184	P3E_CPU0_PE3_RX_DP<4>	183	GND
186	GND	185	P3E_PCIE3_RISER_TX_DN<5>
188	P3E_CPU0_PE3_RX_DN<5>	187	P3E_PCIE3_RISER_TX_DP<5>
190	P3E_CPU0_PE3_RX_DP<5>	189	GND
192	GND	191	P3E_PCIE3_RISER_TX_DN<6>
194	P3E_CPU0_PE3_RX_DN<6>	193	P3E_PCIE3_RISER_TX_DP<6>
196	P3E_CPU0_PE3_RX_DP<6>	195	GND
198	GND	197	PE_CLKREQ_N
200	NC	199	GND
202	GND	201	GND

204	P3E_CPU0_PE3_RX_DN<7>	203	P3E_PCIE3_RISER_TX_DN<7>
206	P3E_CPU0_PE3_RX_DP<7>	205	P3E_PCIE3_RISER_TX_DP<7>
208	GND	207	GND
210	P3E_CPU0_PE3_RX_DN<8>	209	P3E_PCIE3_RISER_TX_DN<8>
212	P3E_CPU0_PE3_RX_DP<8>	211	P3E_PCIE3_RISER_TX_DP<8>
214	GND	213	GND
216	P3E_CPU0_PE3_RX_DN<9>	215	P3E_PCIE3_RISER_TX_DN<9>
218	P3E_CPU0_PE3_RX_DP<9>	217	P3E_PCIE3_RISER_TX_DP<9>
220	GND	219	GND
222	P3E_CPU0_PE3_RX_DN<10>	221	P3E_PCIE3_RISER_TX_DN<10>
224	P3E_CPU0_PE3_RX_DP<10>	223	P3E_PCIE3_RISER_TX_DP<10>
226	GND	225	GND
228	P3E_CPU0_PE3_RX_DN<11>	227	P3E_PCIE3_RISER_TX_DN<11>
230	P3E_CPU0_PE3_RX_DP<11>	229	P3E_PCIE3_RISER_TX_DP<11>
232	GND	231	GND
234	P3E_CPU0_PE3_RX_DN<12>	233	P3E_PCIE3_RISER_TX_DN<12>
236	P3E_CPU0_PE3_RX_DP<12>	235	P3E_PCIE3_RISER_TX_DP<12>
238	GND	237	GND
240	P3E_CPU0_PE3_RX_DN<13>	239	P3E_PCIE3_RISER_TX_DN<13>
242	P3E_CPU0_PE3_RX_DP<13>	241	P3E_PCIE3_RISER_TX_DP<13>
244	GND	243	GND
246	P3E_CPU0_PE3_RX_DN<14>	245	P3E_PCIE3_RISER_TX_DN<14>
248	P3E_CPU0_PE3_RX_DP<14>	247	P3E_PCIE3_RISER_TX_DP<14>
250	GND	249	GND
252	P3E_CPU0_PE3_RX_DN<15>	251	P3E_PCIE3_RISER_TX_DN<15>
254	P3E_CPU0_PE3_RX_DP<15>	253	P3E_PCIE3_RISER_TX_DP<15>
256	GND	255	GND
258		257	JTAG_HOST_TDI
260		259	JTAG_HOST_TDO
262	GND	261	GND
264		263	USB2_RISER_HSD2_N
266	GND	265	USB2_RISER_HSD2_P
268	P12V	267	GND
270	P12V	269	P12V
272	GND	271	P12V
274	P12V	273	GND
276	P12V	275	P12V
278	GMD	277	P12V

280	P12V	279	GND
2U Riser Board x32 (J29) SAMTEC/ **HSEC8-1100-01-L-DV-A-K**			
2	P12V	1	P12V
4	P12V	3	P12V
6	P12V	5	P12V
8	P12V	7	P12V
10	P12V	9	P12V
12	P12V	11	P12V
14	P12V	13	P12V
16	P12V	15	P12V
18	P12V	17	GND
20	GND	19	SMB_REAR_X32_SDA
22	P3V3_AUX	21	SMB_REAR_X32_CLK
24	FM_REAR_PWRBRK_SLOTX32_N	23	HDD_LED
26	GND	25	P3V3_AUX
28	FM_PE_SLOTX32_WAKE_N	27	SMB_CPU_HP_ALERT_N
30	SMB_HOST_STBY_LVC3_SDA	29	RST_PCIE_REAR_X32_N
32	SMB_HOST_STBY_LVC3_SCL	31	GND
34	GND	33	CLK_100M_PCIEX32_BUFF2_DP<5>
36	CLK_100M_PCIEX32_BUFF2_DP<6>	35	CLK_100M_PCIEX32_BUFF2_DN<5>
38	CLK_100M_PCIEX32_BUFF2_DN<6>	37	GND
40	GND	39	CLK_100M_PCIEX32_BUFF2_DP<7>
42	CLK_100M_PCIEX32_BUFF2_DP<8>	41	CLK_100M_PCIEX32_BUFF2_DN<7>
44	CLK_100M_PCIEX32_BUFF2_DN<8>	43	GND
46	GND	45	CLK_100M_PCIEX32_BUFF2_DP<9>
48	CLK_100M_PCIEX32_BUFF2_DP<10>	47	CLK_100M_PCIEX32_BUFF2_DN<9>
50	CLK_100M_PCIEX32_BUFF2_DN<10>	49	GND
52	GND	51	P4E_CPU_G1_TX_C_DP<0>
54	P4E_CPU_G1_RX_DP<0>	53	P4E_CPU_G1_TX_C_DN<0>
56	P4E_CPU_G1_RX_DN<0>	55	GND
58	GND	57	P4E_CPU_G1_TX_C_DP<1>
60	P4E_CPU_G1_RX_DP<1>	59	P4E_CPU_G1_TX_C_DN<1>
62	P4E_CPU_G1_RX_DN<1>	61	GND
64	GND	63	SMB_HP_LVC3_SCL
66	SMB_HP_LVC3_SDA	65	GND
68	GND	67	P4E_CPU_G1_TX_C_DP<2>
70	P4E_CPU_G1_RX_DP<2>	69	P4E_CPU_G1_TX_C_DN<2>
72	P4E_CPU_G1_RX_DN<2>	71	GND

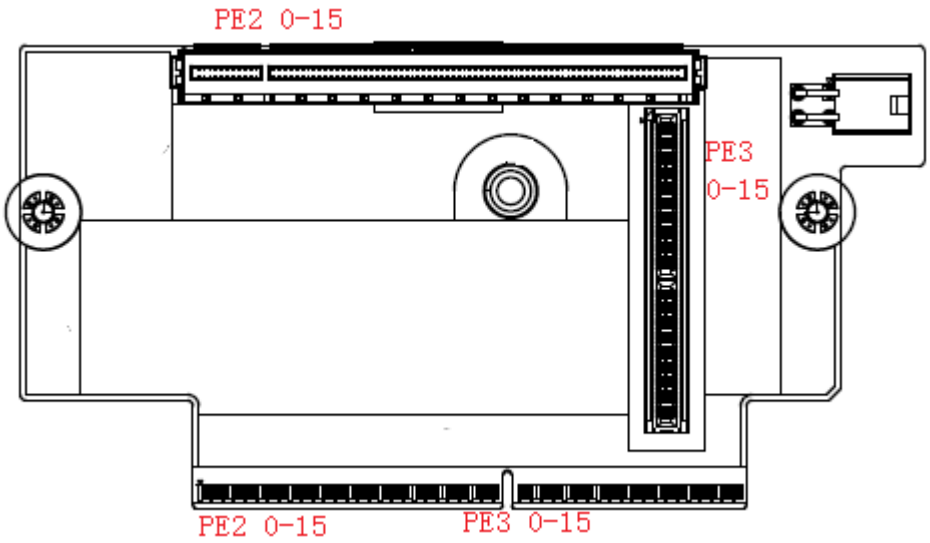
74	GND	73	P4E_CPU_G1_TX_C_DP<3>
76	P4E_CPU_G1_RX_DP<3>	75	P4E_CPU_G1_TX_C_DN<3>
78	P4E_CPU_G1_RX_DN<3>	77	GND
80	GND	79	FM_REAR_RISERX32_PRSNT_N
82	GND	81	GND
84	P4E_CPU_G1_RX_DP<4>	83	P4E_CPU_G1_TX_C_DP<4>
86	P4E_CPU_G1_RX_DN<4>	85	P4E_CPU_G1_TX_C_DN<4>
88	GND	87	GND
90	P4E_CPU_G1_RX_DP<5>	89	P4E_CPU_G1_TX_C_DP<5>
92	P4E_CPU_G1_RX_DN<5>	91	P4E_CPU_G1_TX_C_DN<5>
94	GND	93	GND
96	P4E_CPU_G1_RX_DP<6>	95	P4E_CPU_G1_TX_C_DP<6>
98	P4E_CPU_G1_RX_DN<6>	97	P4E_CPU_G1_TX_C_DN<6>
100	GND	99	GND
102	P4E_CPU_G1_RX_DP<7>	101	P4E_CPU_G1_TX_C_DP<7>
104	P4E_CPU_G1_RX_DN<7>	103	P4E_CPU_G1_TX_C_DN<7>
106	GND	105	GND
108	P4E_CPU_G1_RX_DP<8>	107	P4E_CPU_G1_TX_C_DP<8>
110	P4E_CPU_G1_RX_DN<8>	109	P4E_CPU_G1_TX_C_DN<8>
112	GND	111	GND
114	P4E_CPU_G1_RX_DP<9>	113	P4E_CPU_G1_TX_C_DP<9>
116	P4E_CPU_G1_RX_DN<9>	115	P4E_CPU_G1_TX_C_DN<9>
118	GND	117	GND
120	P4E_CPU_G1_RX_DP<10>	119	P4E_CPU_G1_TX_C_DP<10>
122	P4E_CPU_G1_RX_DN<10>	121	P4E_CPU_G1_TX_C_DN<10>
124	GND	123	GND
126	P4E_CPU_G1_RX_DP<11>	125	P4E_CPU_G1_TX_C_DP<11>
128	P4E_CPU_G1_RX_DN<11>	127	P4E_CPU_G1_TX_C_DN<11>
130	GND	129	GND
132	P4E_CPU_G1_RX_DP<12>	131	P4E_CPU_G1_TX_C_DP<12>
134	P4E_CPU_G1_RX_DN<12>	133	P4E_CPU_G1_TX_C_DN<12>
136	GND	135	GND
138	P4E_CPU_G1_RX_DP<13>	137	P4E_CPU_G1_TX_C_DP<13>
140	P4E_CPU_G1_RX_DN<13>	139	P4E_CPU_G1_TX_C_DN<13>
142	GND	141	GND
144	P4E_CPU_G1_RX_DP<14>	143	P4E_CPU_G1_TX_C_DP<14>
146	P4E_CPU_G1_RX_DN<14>	145	P4E_CPU_G1_TX_C_DN<14>
148	GND	147	GND

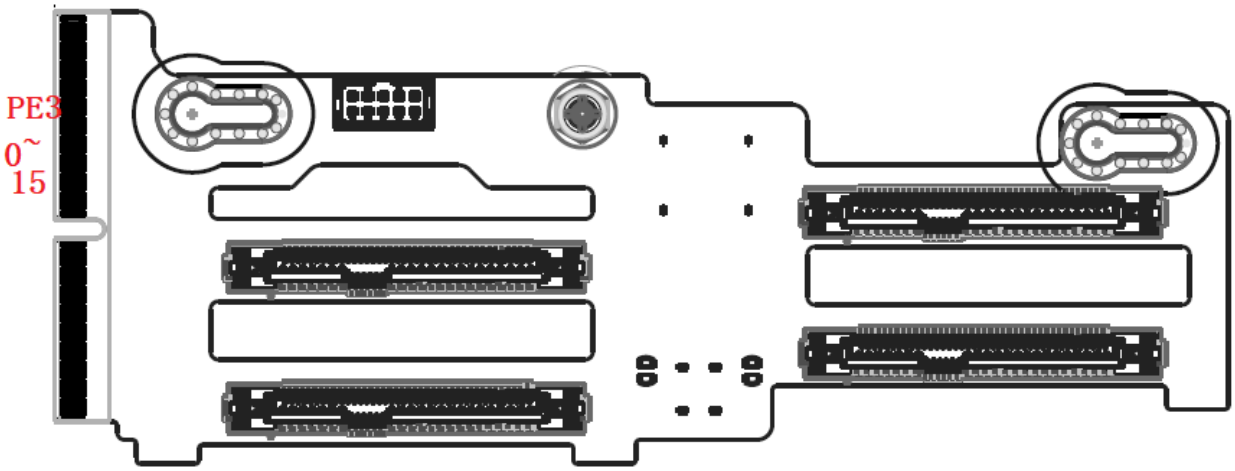
150	P4E_CPU_G1_RX_DP<15>	149	P4E_CPU_G1_TX_C_DP<15>
152	P4E_CPU_G1_RX_DN<15>	151	P4E_CPU_G1_TX_C_DN<15>
154	GND	153	GND
156	P4E_CPU_G0_RX_DP<15>	155	P4E_CPU_G0_TX_C_DN<15>
158	P4E_CPU_G0_RX_DN<15>	157	P4E_CPU_G0_TX_C_DP<15>
160	GND	159	GND
162	GND	161	GND
164	P4E_CPU_G0_RX_DP<14>	163	P4E_CPU_G0_TX_C_DN<14>
166	P4E_CPU_G0_RX_DN<14>	165	P4E_CPU_G0_TX_C_DP<14>
168	GND	167	GND
170	P4E_CPU_G0_RX_DP<13>	169	P4E_CPU_G0_TX_C_DN<13>
172	P4E_CPU_G0_RX_DN<13>	171	P4E_CPU_G0_TX_C_DP<13>
174	GND	173	GND
176	P4E_CPU_G0_RX_DP<12>	175	P4E_CPU_G0_TX_C_DN<12>
178	P4E_CPU_G0_RX_DN<12>	177	P4E_CPU_G0_TX_C_DP<12>
180	GND	179	GND
182	P4E_CPU_G0_RX_DP<11>	181	P4E_CPU_G0_TX_C_DN<11>
184	P4E_CPU_G0_RX_DN<11>	183	P4E_CPU_G0_TX_C_DP<11>
186	GND	185	GND
188	P4E_CPU_G0_RX_DP<10>	187	P4E_CPU_G0_TX_C_DN<10>
190	P4E_CPU_G0_RX_DN<10>	189	P4E_CPU_G0_TX_C_DP<10>
192	GND	191	GND
194	P4E_CPU_G0_RX_DP<9>	193	P4E_CPU_G0_TX_C_DN<9>
196	P4E_CPU_G0_RX_DN<9>	195	P4E_CPU_G0_TX_C_DP<9>
198	GND	197	GND
200	LEDPFAIL	199	LEDPACT
202	GND	201	GND
204	P4E_CPU_G0_RX_DP<8>	203	P4E_CPU_G0_TX_C_DN<8>
206	P4E_CPU_G0_RX_DN<8>	205	P4E_CPU_G0_TX_C_DP<8>
208	GND	207	GND
210	P4E_CPU_G0_RX_DP<7>	209	P4E_CPU_G0_TX_C_DN<7>
212	P4E_CPU_G0_RX_DN<7>	211	P4E_CPU_G0_TX_C_DP<7>
214	GND	213	GND
216	P4E_CPU_G0_RX_DP<6>	215	P4E_CPU_G0_TX_C_DN<6>
218	P4E_CPU_G0_RX_DN<6>	217	P4E_CPU_G0_TX_C_DP<6>
220	GND	219	GND
222	P4E_CPU_G0_RX_DP<5>	221	P4E_CPU_G0_TX_C_DN<5>
224	P4E_CPU_G0_RX_DN<5>	223	P4E_CPU_G0_TX_C_DP<5>

226	GND	225	GND
228	P4E_CPU_G0_RX_DP<4>	227	P4E_CPU_G0_TX_C_DN<4>
230	P4E_CPU_G0_RX_DN<4>	229	P4E_CPU_G0_TX_C_DP<4>
232	GND	231	GND
234	P4E_CPU_G0_RX_DP<3>	233	P4E_CPU_G0_TX_C_DN<3>
236	P4E_CPU_G0_RX_DN<3>	235	P4E_CPU_G0_TX_C_DP<3>
238	GND	237	GND
240	P4E_CPU_G0_RX_DP<2>	239	P4E_CPU_G0_TX_C_DN<2>
242	P4E_CPU_G0_RX_DN<2>	241	P4E_CPU_G0_TX_C_DP<2>
244	GND	243	GND
246	P4E_CPU_G0_RX_DP<1>	245	P4E_CPU_G0_TX_C_DN<1>
248	P4E_CPU_G0_RX_DN<1>	247	P4E_CPU_G0_TX_C_DP<1>
250	GND	249	GND
252	P4E_CPU_G0_RX_DP<0>	251	P4E_CPU_G0_TX_C_DN<0>
254	P4E_CPU_G0_RX_DN<0>	253	P4E_CPU_G0_TX_C_DP<0>
256	GND	255	GND
258	IFDET#_0	257	NVME_PRSNTN0
260	IFDET#_1	259	NVME_PRSNTN1
262	GND	261	GND
264	IFDET#_2	263	NVME_PRSNTN2
266	IFDET#_3	265	NVME_PRSNTN3
268	GND	267	GND
270	IFDET#_4	269	NVME_PRSNTN4
272	IFDET#_5	271	NVME_PRSNTN5
274		273	
276		275	
278		277	GND
280	GND	279	

7.1.2 Riser card types

Vender shall enable 2x riser card below for signal side


PE2 0-15
PE3
0-15
PE2 0-15
PE3 0-15


PE3
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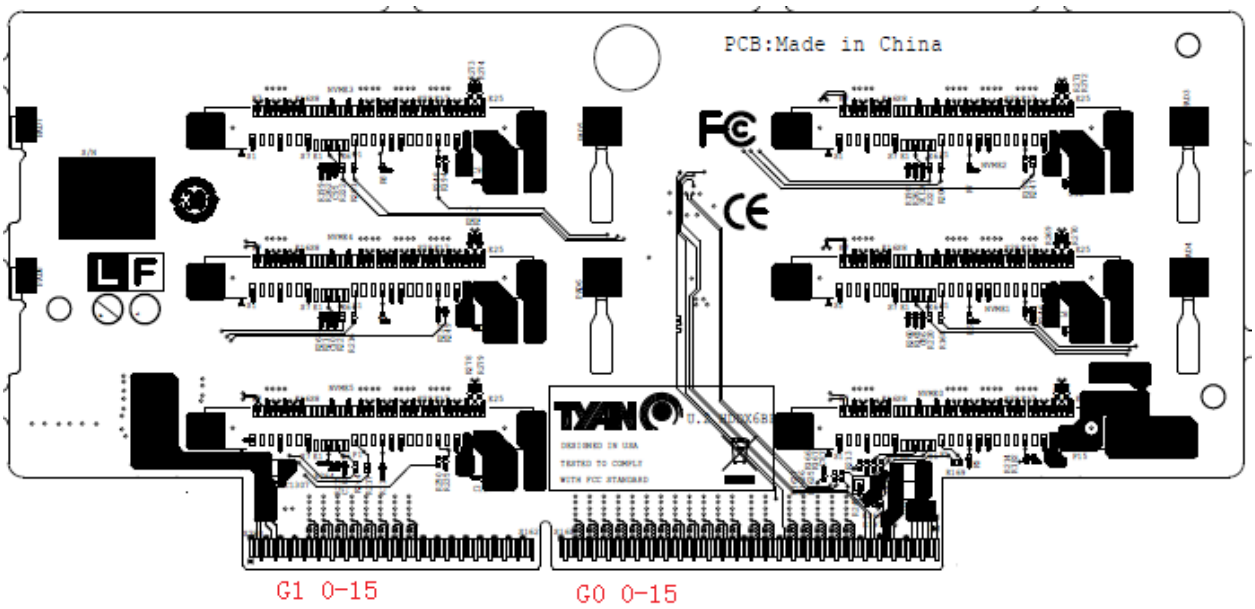
15



Please follow Table 8-1 to table 8-2 to use reserved pins on PCIE X16 slots, and follow 12-1 to set configuration pins on riser card, to indicate which riser on motherboard.

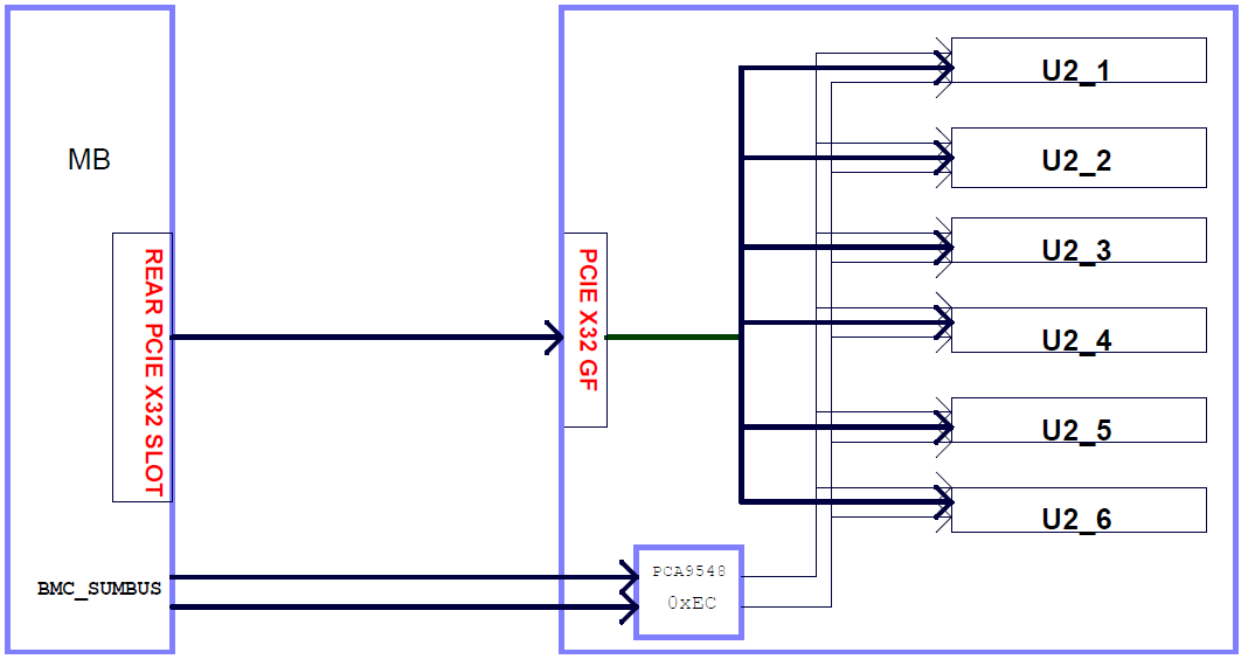
Table 8-1 2 slot PCIE X16 slot 1(high) pin usage on single side:

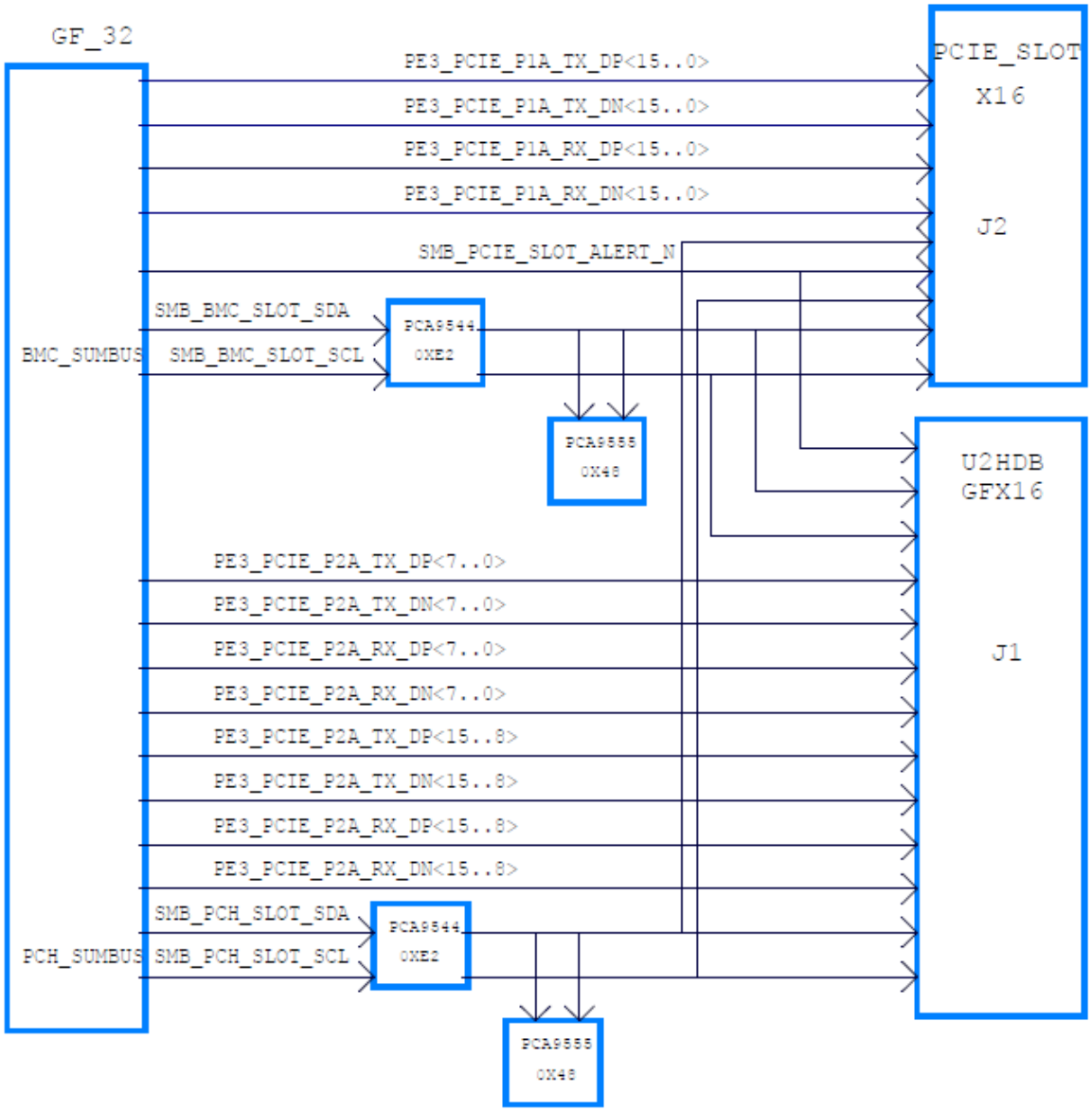
Pin	Pin Defined	Description
A7	SMB_PCH_SCL	PCH SMBUS Clock
A8	SMB_PCH_SDA	PCH SMBUS Data
A19	RSVD	Reserve
A32	USB2.0_P1	USB2.0 Port from Hub port 1
A33	USB2.0_N1	USB2.0 Port from Hub port 1
A50	SMB_ALERT_N	SMBUS Alert from PCIe card to system, OD, low active
B17	SLOT2_PRSNT-1	SLOT2 PRESENT1
B30	PWR_BRKN_N	Power Brake from system to PCIe card, OD, low active
B31	SLOT2_PRSNT-2	SLOT2 PRESENT2
B48	SLOT2_PRSNT-3	SLOT2 PRESENT3
B81	SLOT2_PRSNT-4	SLOT2 PRESENT4
B11	PCIE_SLOT_WAKE_N	PCIE device wake
B11	PE_CLKREQ_N	PCIE thermal alert

Table 8-2 2 slot PCIE X16 slot 2(right) pin usage on single side:

Pin	Pin Defined	Description
7	SMB_BMC_SLOT2_SCL	BMC SMBUS Clock
5	SMB_BMC_SLOT2_SDA	BMC SMBUS Data
9	PCIE_SLOT12_PERST_N	PCIE reset
2	SMB_HP_ALERT_N	HDD hotplug alert
6	SMB_SLOTX24_STBY_LVC3_SDA	PCH SMBUS Data
8	SMB_SLOTX24_STBY_LVC3_SCL	PCH SMBUS Clock

Riser card should implement SMBus Mux to avoid address confliction of PCIe cards.





Riser card should implement I2C to GPIO expander (PCA9555) to be accessed by both BIOS and BMC on motherboard, to tell what AICs are currently on each slot. BIOS shall follow below table 12-7 and table 12-8 to do PCIe bifurcation accordingly. Vendor should follow the SMBUS addresses defined in the diagram to avoid address conflict. The addresses are defined as 8-bit address.

Table 8-3 x16 PCIE card bios bifurcation table

I2C chip	PCA9555				PCA9555							
BMC GPIO port	GPIOY6_SCL2 & GPIOY7_SDA2											
Reg bit	IO_0_3	IO_0_2	IO_0_1	IO_0_0	IO_1_0							BIOS Bifurcation setting
NET name	FM_PCIE_2SLOT_1_PRSNT?_N				FM_PCIE_2SLOT_2_PRSNT_N							
PRSNT pin	4	3	2	1					SLT_CFG1	SLT_CFG0		
X16	0	X	X	X	X	X	X	X	0	0	X	1 X16
X8	1	0	X	X	X	X	X	X	0	0	X	1X8
X4	1	1	0	X	X	X	X	X	0	0	X	4X4
X1	1	1	1	0	X	X	X	X	0	0	X	1 X16
	1	1	1	1	X	X	X	X	0	0	X	1 X16
	X	X	X	X	0		X		0	0	X	4X4
	X	X	X	X	X		1		0	0	X	1X16

RISER	U2	2 SLOT
FM_PCIE_2SLOT_2_PRSNT_N	0	1
Slot Width 1(Port 1)	X16	X16
Slot Width 2(Port 2)	4x4	X16

7.1.3 Riser card Power outlet

Add 2x2 right angle power connector (Molex/46991-1004 or equivalent) for deliver power from riser to PCIe cards that need higher power than PCIe slot allows.

Table Riser power connector pin define:

Position	Type	Description
1,2	Ground	Ground return
3,4	P12V	P12V from riser to Add-on-Cards

7.2 DIMM Sockets

The motherboard requires 15u" gold contact for DDR4 SMT DIMM socket. Socket uses Blue housing and white/nature latch for far end DIMM in a DDR channel. Vendor shall announce if the color selection will increase the cost of the DIMM Socket.

7.3 Mezzanine Card

Tioga Pass is compatible with Mezzanine Card for OCP Mezzanine Card 2.0 design specifications.

The motherboard has Connector A and Connector B as OCP Mezz 2.0 specification to provide up to X 16 PCIE Gen3 connection to Mezzanine card.

The motherboard also has Connector C as OCP Mezz 2.0 Specification to provide up to x4 KR. Connector C can be used independently on Mezzanine card side.

The motherboard also has Connector C as OCP Mezz 2.0 specification to provide up to x4 KR. Connector C can be used independently on Mezzanine card side.

Motherboard mezzanine connector A is named as Slot1 in system.

7.3.1 Connector A

Below table shows connector A pin definition:

Table 1 Mezzanine Connector A pin Definition

Signal	Description	Pin	Pin	Signal	Description
P12V_AUX	Aux Power	61	1	MEZZ_PRSNT1_N	Present pin1, short to Pin120 on Mezz card
P12V_AUX	Aux Power	62	2	P5V_AUX	Aux Power
P12V_AUX	Aux Power	63	3	P5V_AUX	Aux Power
GND	Ground	64	4	P5V_AUX	Aux Power
GND	Ground	65	5	GND	Ground
P3V3_AUX	Aux Power	66	6	GND	Ground
GND	Ground	67	7	P3V3_AUX	Aux Power
GND	Ground	68	8	GND	Ground
P3V3	Power	69	9	GND	Ground
P3V3	Power	70	10	P3V3	Power
P3V3	Power	71	11	P3V3	Power
P3V3	Power	72	12	P3V3	Power
GND	Ground	73	13	P3V3	Power
LAN_3V3STB_ALERT_N	SMBus Alert for OOB	74	14	NCSI_RCSDV	BMC NCSI
SMB_LAN_3V3STB_CLK	SMBus Clock for OOB	75	15	NCSI_RCLK	BMC NCSI
SMB_LAN_3V3STB_DAT	SMBus Data for OOB	76	16	NCSI_TXEN	BMC NCSI
PCIE_WAKE_N	PCIE wake up	77	17	RST_PLT_MEZZ_N	PCIe reset signal
NCSI_RXER	BMC NCSI	78	18	RSVD (MEZZ_SMCLK)	Reserved(PCIe slot SMBus Clock)
GND	Ground	79	19	RSVD (MEZZ_SMDATA)	Reserved(PCIe slot SMBus Data)
NCSI_TXD0	BMC NCSI	80	20	GND	Ground
NCSI_TXD1	BMC NCSI	81	21	GND	Ground
GND	Ground	82	22	NCSI_RXD0	BMC NCSI
GND	Ground	83	23	NCSI_RXD1	BMC NCSI
CLK_100M_MEZZ1_DP	100MHz PCIe clock	84	24	GND	Ground
CLK_100M_MEZZ1_DN	100MHz PCIe clock	85	25	GND	Ground
GND	Ground	86	26	RSVD(CLK_100M_MEZZ2_DP)	Reserved(2nd set of 100MHz PCIe clock)
GND	Ground	87	27	RSVD(CLK_100M_MEZZ2_DN)	Reserved(2nd set of 100MHz PCIe clock)
MEZZ_TX_DP_C<0>	PCIE TX signal	88	28	GND	Ground
MEZZ_TX_DN_C<0>	PCIE TX signal	89	29	GND	Ground
GND	Ground	90	30	MEZZ_RX_DP<0>	PCIE RX signal
GND	Ground	91	31	MEZZ_RX_DN<0>	PCIE RX signal
MEZZ_TX_DP_C<1>	PCIE TX signal	92	32	GND	Ground

MEZZ_TX_DN_C<1>	PCIE TX signal	93	33	GND	Ground
GND	Ground	94	34	MEZZ_RX_DP<1>	PCIE RX signal
GND	Ground	95	35	MEZZ_RX_DN<1>	PCIE RX signal
MEZZ_TX_DP_C<2>	PCIE TX signal	96	36	GND	Ground
MEZZ_TX_DN_C<2>	PCIE TX signal	97	37	GND	Ground
GND	Ground	98	38	MEZZ_RX_DP<2>	PCIE RX signal
GND	Ground	99	39	MEZZ_RX_DN<2>	PCIE RX signal
MEZZ_TX_DP_C<3>	PCIE TX signal	100	40	GND	Ground
MEZZ_TX_DN_C<3>	PCIE TX signal	101	41	GND	Ground
GND	Ground	102	42	MEZZ_RX_DP<3>	PCIE RX signal
GND	Ground	103	43	MEZZ_RX_DN<3>	PCIE RX signal
MEZZ_TX_DP_C<4>	PCIE TX signal	104	44	GND	Ground
MEZZ_TX_DN_C<4>	PCIE TX signal	105	45	GND	Ground
GND	Ground	106	46	MEZZ_RX_DP<4>	PCIE RX signal
GND	Ground	107	47	MEZZ_RX_DN<4>	PCIE RX signal
MEZZ_TX_DP_C<5>	PCIE TX signal	108	48	GND	Ground
MEZZ_TX_DN_C<5>	PCIE TX signal	109	49	GND	Ground
GND	Ground	110	50	MEZZ_RX_DP<5>	PCIE RX signal
GND	Ground	111	51	MEZZ_RX_DN<5>	PCIE RX signal
MEZZ_TX_DP_C<6>	PCIE TX signal	112	52	GND	Ground
MEZZ_TX_DN_C<6>	PCIE TX signal	113	53	GND	Ground
GND	Ground	114	54	MEZZ_RX_DP<6>	PCIE RX signal
GND	Ground	115	55	MEZZ_RX_DN<6>	PCIE RX signal
MEZZ_TX_DP_C<7>	PCIE TX signal	116	56	GND	Ground
MEZZ_TX_DN_C<7>	PCIE TX signal	117	57	GND	Ground
GND	Ground	118	58	MEZZ_RX_DP<7>	PCIE RX signal
GND	Ground	119	59	MEZZ_RX_DN<7>	PCIE RX signal
MEZZ_PRSNT2_N	Present pin2, short to Pin1 on Mezz card	120	60	GND	Ground

Note: For x16 PCIe, lane 0~7 is mapped to connector A and lane 8~15 is mapped to connector B.

7.3.2 Connector B

Table 2 Mezzanine Connector B Pin Definition:

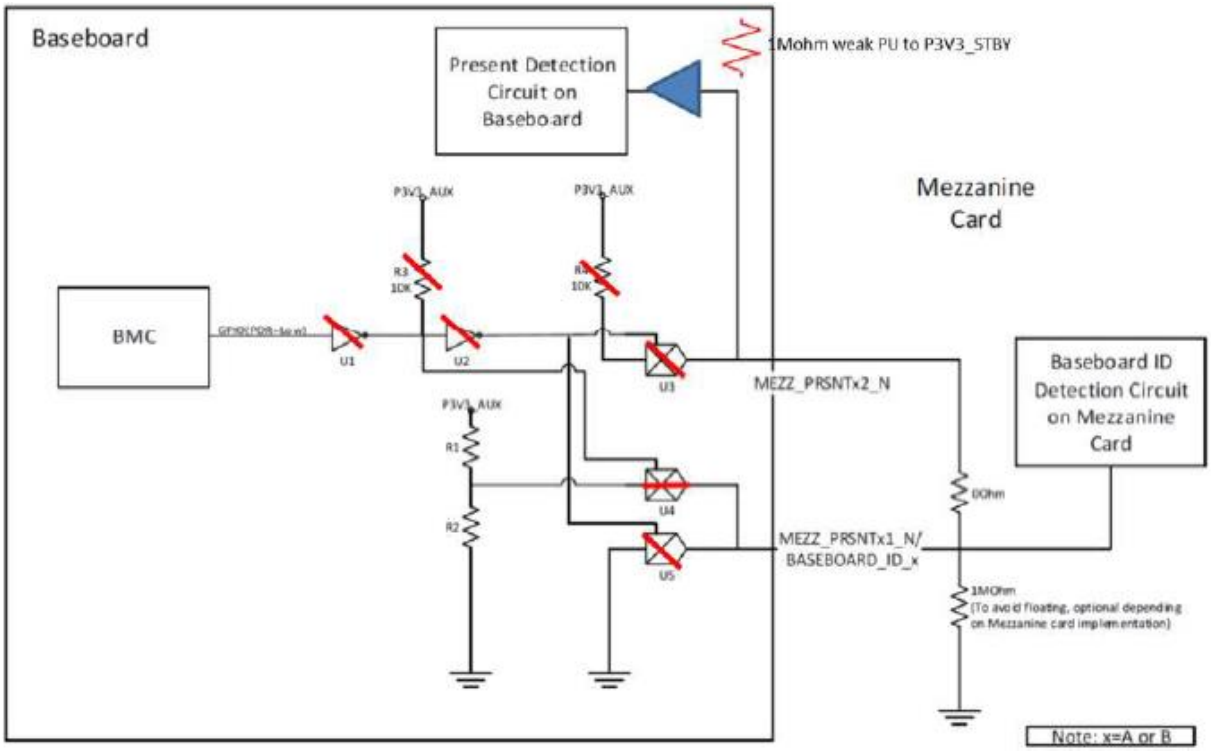
Signal	Description	Pin	Pin	Signal	Description
P12V_AUX/P12V	Aux Power	B41	B1	MEZZ_PRSNTB1_N /BASEBOARD_B_ID	Present pin1, short to Pin120 on Mezz card
P12V_AUX/P12V	Aux Power	B42	B2	GND	Ground
RSVD		B43	B3	MEZZ_RX_DP<8>	Aux Power
GND	Ground	B44	B4	MEZZ_RX_DN<8>	Aux Power
MEZZ_TX_DP<8>	Ground	B45	B5	GND	Ground
MEZZ_TX_DN<8>	Aux Power	B46	B6	GND	Ground
GND	Ground	B47	B7	MEZZ_RX_DP<9>	Aux Power
GND	Ground	B48	B8	MEZZ_RX_DN<9>	Ground
MEZZ_TX_DP<9>	Power	B49	B9	GND	Ground
MEZZ_TX_DN<9>	Power	B50	B10	GND	Power
GND	Power	B51	B11	MEZZ_RX_DP<10>	Power
GND	Power	B52	B12	MEZZ_RX_DN<10>	Power
MEZZ_TX_DP<10>	Ground	B53	B13	GND	Power
MEZZ_TX_DN<10>	SMBus Alert for OOB	B54	B14	GND	BMC NCSI
GND	SMBus Clock for OOB	B55	B15	MEZZ_RX_DP<11>	BMC NCSI
GND	SMBus Data for OOB	B56	B16	MEZZ_RX_DN<11>	BMC NCSI
MEZZ_TX_DP<11>	PCIE wake up	B57	B17	GND	PCIe reset signal
MEZZ_TX_DN<11>	BMC NCSI	B58	B18	GND	Reserved(PCIe slot SMBus Clock)
GND	Ground	B59	B19	MEZZ_RX_DP<12>	Reserved(PCIe slot SMBus Data)
GND	BMC NCSI	B60	B20	MEZZ_RX_DN<12>	Ground
MEZZ_TX_DP<12>	BMC NCSI	B61	B21	GND	Ground
MEZZ_TX_DN<12>	Ground	B62	B22	GND	BMC NCSI
GND	Ground	B63	B23	MEZZ_RX_DP<13>	BMC NCSI
GND	100MHz PCIe clock	B64	B24	MEZZ_RX_DN<13>	Ground
MEZZ_TX_DP<13>	100MHz PCIe clock	B65	B25	GND	Ground

MEZZ_TX_DN<13>	Ground	B66	B26	GND	Reserved(2nd set of 100MHz PCIe clock)
GND	Ground	B67	B27	MEZZ_RX_DP<14>	Reserved(2nd set of 100MHz PCIe clock)
GND	PCIE TX signal	B68	B28	MEZZ_RX_DN<14>	Ground
MEZZ_TX_DP<14>	PCIE TX signal	B69	B29	GND	Ground
MEZZ_TX_DN<14>	Ground	B70	B30	GND	PCIE RX signal
GND	Ground	B71	B31	MEZZ_RX_DP<15>	PCIE RX signal
GND	PCIE TX signal	B72	B32	MEZZ_RX_DN<15>	Ground
MEZZ_TX_DP<15>	PCIE TX signal	B73	B33	GND	Ground
MEZZ_TX_DN<15>	Ground	B74	B34	GND	PCIE RX signal
GND	Ground	B75	B35	CLK_100M_MEZZ2_DP	PCIE RX signal
GND	PCIE TX signal	B76	B36	CLK_100M_MEZZ2_DN	Ground
CLK_100M_MEZZ3_DP	PCIE TX signal	B77	B37	GND	Ground
CLK_100M_MEZZ3_DN	Ground	B78	B38	PERST_N1	PCIE RX signal
GND	Ground	B79	B39	PERST_N2	PCIE RX signal
MEZZ_PRSNTB2_N	PCIE TX signal	B80	B40	PERST_N3	Ground
P12V_AUX/P12V	PCIE TX signal	B41	B1	MEZZ_PRSNTB1_N /BASEBOARD_B_ID	Ground
P12V_AUX/P12V	Ground	B42	B2	GND	PCIE RX signal
RSVD	Ground	B43	B3	MEZZ_RX_DP<8>	PCIE RX signal
GND	PCIE TX signal	B44	B4	MEZZ_RX_DN<8>	Ground
MEZZ_TX_DP<8>	PCIE TX signal	B45	B5	GND	Ground
MEZZ_TX_DN<8>	Ground	B46	B6	GND	PCIE RX signal
GND	Ground	B47	B7	MEZZ_RX_DP<9>	PCIE RX signal
GND	PCIE TX signal	B48	B8	MEZZ_RX_DN<9>	Ground
MEZZ_TX_DP<9>	PCIE TX signal	B49	B9	GND	Ground
MEZZ_TX_DN<9>	Ground	B50	B10	GND	PCIE RX signal
GND	Ground	B51	B11	MEZZ_RX_DP<10>	PCIE RX signal
GND	PCIE TX signal	B52	B12	MEZZ_RX_DN<10>	Ground
MEZZ_TX_DP<10>	PCIE TX signal	B53	B13	GND	Ground
MEZZ_TX_DN<10>	Ground	B54	B14	GND	PCIE RX signal
GND	Ground	B55	B15	MEZZ_RX_DP<11>	PCIE RX signal
GND	PCIE TX signal	B56	B16	MEZZ_RX_DN<11>	Ground
MEZZ_TX_DP<11>	PCIE TX signal	B57	B17	GND	Ground
MEZZ_TX_DN<11>	Ground	B58	B18	GND	PCIE RX signal
GND	Ground	B59	B19	MEZZ_RX_DP<12>	PCIE RX signal
GND	Present pin2, short to Pin1 on Mezz card	B60	B20	MEZZ_RX_DN<12>	Ground
MEZZ_TX_DP<12>		B61	B21	GND	
MEZZ_TX_DN<12>		B62	B22	GND	
GND		B63	B23	MEZZ_RX_DP<13>	
GND		B64	B24	MEZZ_RX_DN<13>	
MEZZ_TX_DP<13>		B65	B25	GND	
MEZZ_TX_DN<13>		B66	B26	GND	
GND		B67	B27	MEZZ_RX_DP<14>	
GND		B68	B28	MEZZ_RX_DN<14>	
MEZZ_TX_DP<14>		B69	B29	GND	
MEZZ_TX_DN<14>		B70	B30	GND	
GND		B71	B31	MEZZ_RX_DP<15>	
GND		B72	B32	MEZZ_RX_DN<15>	
MEZZ_TX_DP<15>		B73	B33	GND	
MEZZ_TX_DN<15>		B74	B34	GND	
GND		B75	B35	CLK_100M_MEZZ2_DP	
GND		B76	B36	CLK_100M_MEZZ2_DN	
CLK_100M_MEZZ3_DP		B77	B37	GND	
CLK_100M_MEZZ3_DN		B78	B38	PERST_N1	
GND		B79	B39	PERST_N2	
MEZZ_PRSNTB2_N		B80	B40	PERST_N3	

7.3.3 Base board ID

Baseboard ID is to let Mezzanine card has awareness of different base board. Baseboard ID applies connector A and connector B.

The implementation of Baseboard ID circuit on Capri is shown below. R1 is 10K and R2 is 887 ohm on both connect A and connector B.



The Mezzanine card identifies different of Baseboard on the resistor pair R1/R2 shown in tables below:

Table: Connector A Baseboard Types

ConnA R1	Conn A R2	Baseboard type on Connector A
NC	0 Ω	One x8 PCIe Root Port on baseboard Connector A; No Connector B on Baseboard
10 KΩ	887 Ω	One x16 PCIe Root Ports on Baseboard Connector A and B
10 KΩ	2.10KΩ	One x8 PCIe Root Port on baseboard Connector A; Connector B presents on Baseboard
10 KΩ	3.83 KΩ	Two x4 PCIe Root Ports on baseboard Connector A
10 KΩ	6.49 KΩ	Four x2 PCIe Root Ports on baseboard Connector A
10 KΩ	11 KΩ	Eight x1 PCIe Root Ports on baseboard Connector A
10 KΩ	20.5 KΩ	RFU

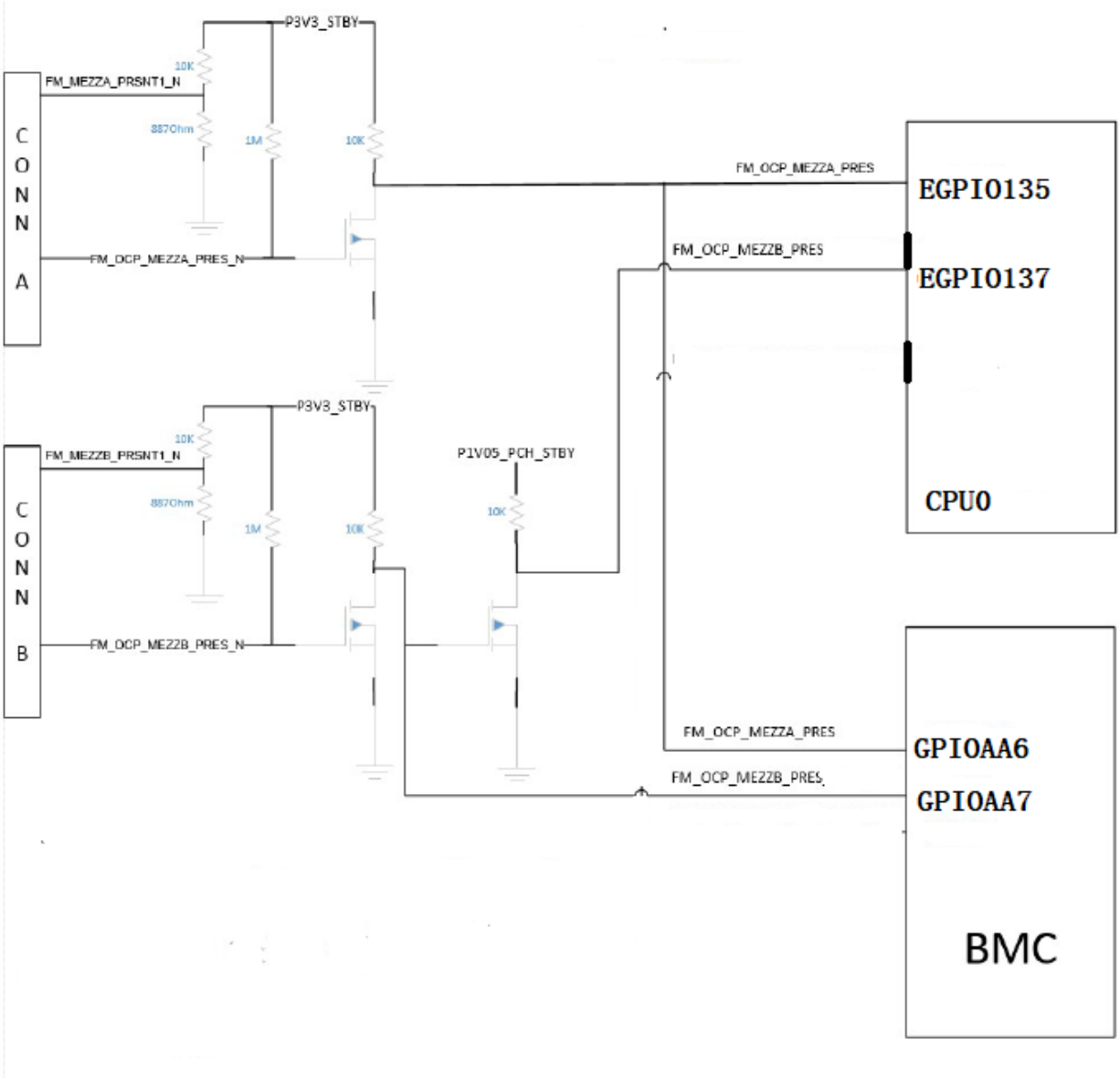
10 KΩ	48.7 KΩ	RFU
10 KΩ	NC	Up to 8x KR on baseboard Connector A

Table: Connector B baseboard Types

Conn B R1	Conn B R2	Baseboard type on Connector B
NC	NC	NO Connector B on baseboard; Mezzanine card samples Baseboard_ ID_B as 0 V with weak pull low on Mezzanine card side
10 kΩ	887 Ω	One x16 PCIe Root Ports on Baseboard Connector A and B
10 kΩ	2.10KΩ	One x8 PCIe Root Port on baseboard Connector B
10 kΩ	3.83 KΩ	Two x4 PCIe Root Ports on baseboard Connector B
10 kΩ	6.49 KΩ	Four x2 PCIe Root Ports on baseboard Connector B
10 kΩ	11 KΩ	Eight x1 PCIe Root Ports on baseboard Connector B
10 kΩ	KΩ	RFU
10 kΩ	48.7 KΩ	RFU
10 kΩ	NC	Up to 8x KR on baseboard Connector B

7.3.4 Mezzanine present pin

Capri Mezzanine present pins' connection to CPU and BMC as below:



7.4 Network

7.4.1 Data network

The motherboard uses OCP mezzanine 2.0 card as its primary data network interface at I/O side. There is option of single port and or dual ports.

One Intel I210 1G NIC is placed on board to provide optional 10/100/1000 data connection.

7.4.2 Management Network

The motherboard has 3X options of management network interface for BMC's connection. Management network shares data network's physical interface. Management connection should be independent from traffic, and OS/driver condition.

SFP+ shared-NIC from Mezzanine 10G NIC or PCIe NIC, driven by BMC through RMII/NC-SI or I2C.

7.4.3 IPv4/IPv6 support

The system needs to have the capacity to be deployed in both IPv4and IPv6 network environment. All data network and management network should have this capability. This includes, but not limited to: DHCP and static IP setting, PXE booting capability, NIC and BMC firmware support, OS driver, and utility in both IPv4 and IPv6.

7.5 USB

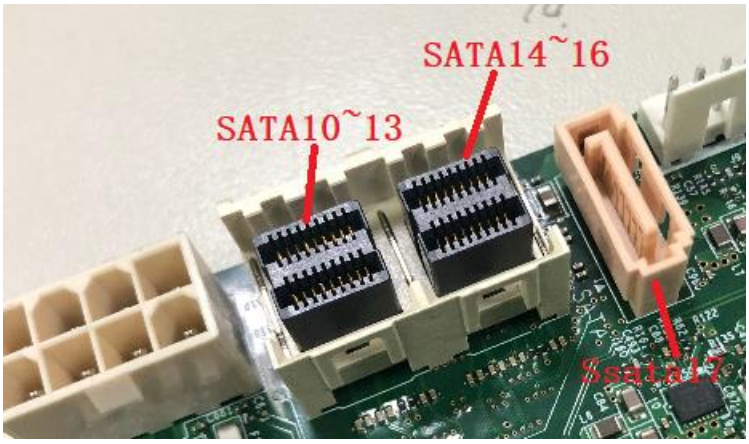
The motherboard has one external type A right angle USB 2.0/3.0 port and one USB 3.0 type C port located in front of the motherboard. BIOS should support following devices on motherboard:

- USB keyboard and mouse.
- USB flash drive (bootable)
- USB hard drive (bootable)
- USB optical drive (bootable)

7.6 SATA

The motherboard support AMD ROME CPU and CPU has SATA controller support 8x SATA3 ports.

SATA Port 10~16 can be connected to one vertical miniSAS HD 8 ports connector. sSATA Port 17 is connected to 1x vertical SATA connector on motherboard. This vertical SATA port is using a power-signal combined SATA connector with latch to allow 1-step and secured operation. Connector is Alltop/C18625-11331-L.



Both SATA connector and vertical SATA connector need to be placed near IO side of the motherboard for easy access. HDDs attached to all SATA connectors need to follow the requirement below:

When hard drive spins up after power on, it draws excessive current o both 12V and 5V. The peak current may reach 1.5A ~ 2A range in 12V.

7.7 M.2

The motherboard has 1x M.2 connector.M.2 connector has option connection of PCIEX4 or sSATA form CPU0.On board M.2 connector supports 2280, 22110 card form factor with both single side and double side.

Sideband signals such as WAKE# and SATA_ACTIVITY should be connected when it applies.

PERST# shall go active before the power on M.2 connector is removed per PCI CEM specification.

Vendor shall add SMBUS and Alert connection to BMC base on the latest M.2 spec.

7.8 Debug header

The motherboard has 2 debug headers to work with, 14 pin debug card and 3pin debug connector for bios.

7.8.1 14 pin debug card header

The 1st debug header is placed in front right of the motherboard. Debug card can be plugged into this header directly or through a cable. This debug header should support hot plug. Through this debug header, debug card should provide one UART serial port connector, two 7-segment LED displays, one reset button and one UART channel selection button. UART should provide console redirection function. Two 7-segment LED displays show BIOS POST code and DIMM error information. One reset button will trigger system reset when pressed. Debug card pin 14 power P5V_AUX on or off is controlled by CPLD. Default is enabled.

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The connector for the debug header is a 14 pin, shrouded, vertical, 2mm pitch connector. Figure 11-9 is an illustration of the headers. Debug card should have a key to match with the notch to avoid pin shift when plugging in.

Debug header pin definition:

1. LED_POSTCODE_0_R
2. LED_POSTCODE_1_R
3. LED_POSTCODE_2_R
4. LED_POSTCODE_3_R
5. LED_POSTCODE_4_R
6. LED_POSTCODE_5_R
7. LED_POSTCODE_6_R

8. LED_POSTCODE_7_R
9. SPA_MID_DBG1_TX
10. SP_BMC_UART5_RXD
11. FM_DEBUG_RST_BTN_N
12. FM_UART_SWITCH_N
13. GND
14. DEBUG_VCCIN

7.8.2 Debug Port power policy

User should be able to power on system by pressing power button on debug card with LCD. The USB port power should be standby power rail to support debug card MCU to function at S5 state. Vendor should implement debug card FW to control the 7 segment LED to be off when system is in S5 state.

7.9 LEDs

The table below indicates the color and function of each LED. The motherboard's silkscreen shall indicate the functionality of each of these LEDs.

■ **Power On LED**

Status	LED COLOR	Behavior	LED Location
System power on	ON	MB is in the power on status	U31
Chassis identify	Blinking	-LED on for 0.1sec, off for 0.9sec and loop when system power off. -LED on for 0.9sec, off for 0.1sec and loop when system power on.	U31

■ **HDD LED**

Status	LED COLOR	Behavior	LED Location
Hard drive activity	Blinking	Twinkling as M.2 （SATA Device）	U45

■ **CPLD HEARTBEAT LED**

Status	LED COLOR	Behavior	LED Location
CPLD ready	Blinking 1Hz	When CPLD FW initialize	LED4

■ **BMC HEARTBEAT LED**

status	LED COLOR	Behavior	LED Location
BMC ready	Blinking 1Hz	When BMC FW initialize	D18

■ **BMC FAIL LED**

status	LED COLOR	Behavior	LED Location
BMC error	ON	When BMC FW fail	U83

■ **CPLD Debug LED**

status	LED COLOR	Behavior	LED Location

HEX code for debug	ON	CPLD debug use	LED5-LED12

■ **UART SW LED**

status	LED COLOR	Behavior	LED Location
UART activity	Blinking	MSB	U119
UART activity	Blinking	LSB	U120

7.10 FAN connector

The motherboard has two system FAN connectors. FAN connector should follow "4-Wire Pulse Width Modulation (PWM) Controlled Fan Specification" Revision 1.3 September 2005 published by Intel Corporation. Basically the detail of the FAN connector is the same as MiTAC Tioga Pass one and below is the basic info. for reference.

FAN connector Pin Definition

6Pin x1 (J27/SYSFAN1)

Net Name	Pin #
GND	1
P12V_FAN	2
FAN_TACH0_CPU0_D1	3
FAN_PWM_OUT_SYS0_R	4
FAN_TACH1_CPU1_D1	5
TP_FAN_0	6

6Pin x1 (J26/SYSFAN2)

Net Name	Pin #
GND	1
P12V_FAN	2
FAN_TACH2_CPU1_D1	3
FAN_PWM_OUT_SYS1_R	4
FAN_TACH3_CPU1_D1	5
TP_FAN_1	6

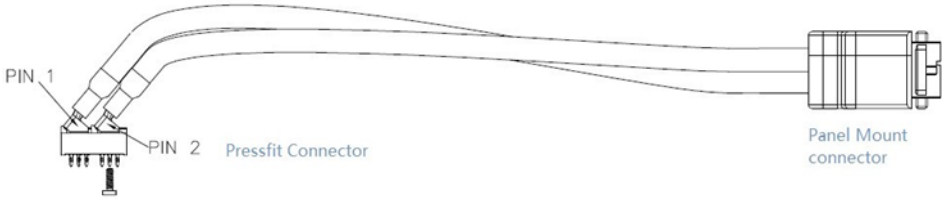
8. Rear Side Power, I/O and Midplane

8.1 Overview of Footprint and Population Options

There is 1x footprint at rear side of the motherboard to provide power to motherboard. The population of the footprints is flexible to fit the need of different use cases.

8.2 Midplane

A pressfit cable is enabled for the use case of ORv2 and Cubby chassis. A side view is shown below.



One side of the Pressfit cable is a pressfit power connector. The pressfit power connector is installed on motherboard with pressfit process, and secured by a screw for added strength. Pressfit power connector shares the same footprint and pin define as FCI/10124648-001LF.

The other side of the pressfit cable is a panel mount connector. It is installed on a sheet metal panel with tool-less install and remove.

9. ORv2 Implementation

MiTAC Capri is compatible and can be complied with Orv2. This is because the form factor of Capri follows Tioga Pass (2OU 3Nodes) therefore it is compatible with Open Rack v2.

10. Mechanical

10.1 Single Side Sled mechanical

Capri single sled mechanical design and tooling follows Tioga Pass in ORv2 sled. For the detail mechanical design, please refer to Tioga Pass document in OCP.

10.2 PCB Thickness

To ensure proper alignment of the motherboard and mid-plane interface within its mechanical enclosure, the motherboard should follow PCB stack up to have 85mil (2.16mm) PCB thickness. And thickness of mid-plane PCB should also be 61.8mil (1.57mm). Thickness of Mezzanine card and riser card PCB should also be 61.8mil (1.57mm).

10.3 Heat Sinks and ILM

The motherboard shall support heat sinks that are mounted according to the AMD thermal mechanical specification and design guide. The vendor shall comply with all keep out zones defined by AMD in the reference specification.

10.4 Silk Screen

The silk screen shall be white in color and include printings for the components listed below. Additional items required on the silk screen are listed in the section of Regulations.

- CPU1
- DIMM slot numbering.
- LEDs.
- Switches as PWR and RST.

10.5 PCB Color

Different PCB colors shall be used to help identify the motherboards revision. Table below indicates the PCB color to be used for each development revision.

Revision	PCB color
EVT	Red
DVT	Blue
PVT	Green
MP	Green

11. Motherboard Power System

11.1 Input Voltage

11.1.1 Input Voltage Level

The nominal input voltage delivered by the power supply is 12.5VDC nominal at light loading with a range of 11V to 13V. The motherboard shall accept and operate normally with input voltage tolerance range between 10.8V and 13.2V when all under voltage related throttling features are disable in 12.2.

Motherboard's under-voltage protection level should be less than 10.1V.

11.1.2 Capacitive Load

Previous server generations required a maximum capacitive load of 4000uF. This requirement does not apply to Capri design. The motherboard design requires greater than 10000uF capacitive loading on P12V_AUX for supplying surge current from CPU VR, and reduce the slew rate of P12V_AUX decaying for NVDIMM feature at surprising power fail. Hot Swap Controller design should limit the inrush current to node during soft-start to less or equal to 10A.

11.1.3 P12V as AUX rail

There is only one 12V rail delivered to the mother board as auxiliary power rail. Caution need to be taken to provide proper isolation to PCIe device, HDD, FAN, and all other devices in system, to meet voltage and timing requirement during running time and power on/off. The isolation circuit should have a soft start to avoid inrush current to P12V AUX rail, and prevent SOA damage of isolation MOSFET.

11.2 Hot-Swap Controller (HSC) Circuit

In order to have a better control of 12.5V DC power input to each motherboard, one HSC(ADI/ADM1278) is used on the mother board. HSC circuit provides the following functions:

- Inrush current control when motherboard is inserted and powered up.
- Current limiting protection for over current and short circuit. Over current trip point should be able to set to 68A and 41.4A with Iset jumper setting for single side motherboard; default is 68A.
- HSC UV protection shall be set to 9V~10.1V and OVP shall be set to 14.3V~15V.
- SOA protection during MOSFET turning on and off.
- HSC fault protection is set to latch off(default) with retry as stuff option.
- PMBUS interface to enable BMC following actions
  - Report server input power and log event if it triggers upper critical threshold.
  - Report input voltage(up to 1 decimal point) and log event if it triggers either lower or upper critical threshold.
  - Log status event based on hot swap controllers' status register.
- Use HSC or external circuit to provide fast(<20us) over current sense alert to trigger system throttling and CPU fast PROCHOT#; over current based fast PROCHOT# shall be controller by HSC Iset jumper. Fast PROCHOT# threshold shall be slightly lower than HSC DC OCP set point to be useful. Feature can be disabled by BMC GPIO directly. BIOS has a setting to control Enable/Disable/ [no change]. No change is the default. This means follow the BMC initial setting. BMC sets it to disable as the default. Before BMC is ready, the hardware POR state is enable.
- Use HSC or external circuit to provide fast(<20us) under-voltage alert to trigger system throttling and CPU fast PROCHOT#. This feature is enable by default with resistor option to disable. The threshold is set to 11.5V by default and with option to set it 11V. a jumper for UV_HIGH_SET is implemented together with BMC to control under voltage FPH trip point. When the jumper is at pin 1 and pin 2, trip point is 11.5V or follow BMC; when jumper is at pin 2 and 3, trip point is 11V.
- Use HSC or external circuit to provide fast(<20us) under-voltage alert to trigger system FAN throttling. This feature is disable by default with resistor option to enable.
- Use HSC or external circuit to provide HSC timer alert to trigger system throttling before HSC OCP happens.
- The voltage drop on HSC current sense resistor should be less or equal to 25mV at full loading. Hot swap controllers should have SMBUS address set to 0x44(7bit format) with 0.25m ohm Rsen on.

11.3 CPU VR

11.3.1 CPU maximum power

The motherboard shall be design to handle a processor with a maximum TDP of 225W. as a result the vendor shall optimize the CPU VR accordingly.

11.3.2 CPU VR Optimizations

CPU VR optimizations shall be implemented to remove cost and increase the efficiency of the power conversion system. Vendors shall only use the minimum number of total phases to support the maximum CPU power defined in 12.3.1. CPU VR should have auto phase dropping feature, and run at optimized phase count among 1, 2, 3, …,

and the maximum phase count. CPU VR should support all Power States to allow the VRM to operate at its peak efficiency at light loading.

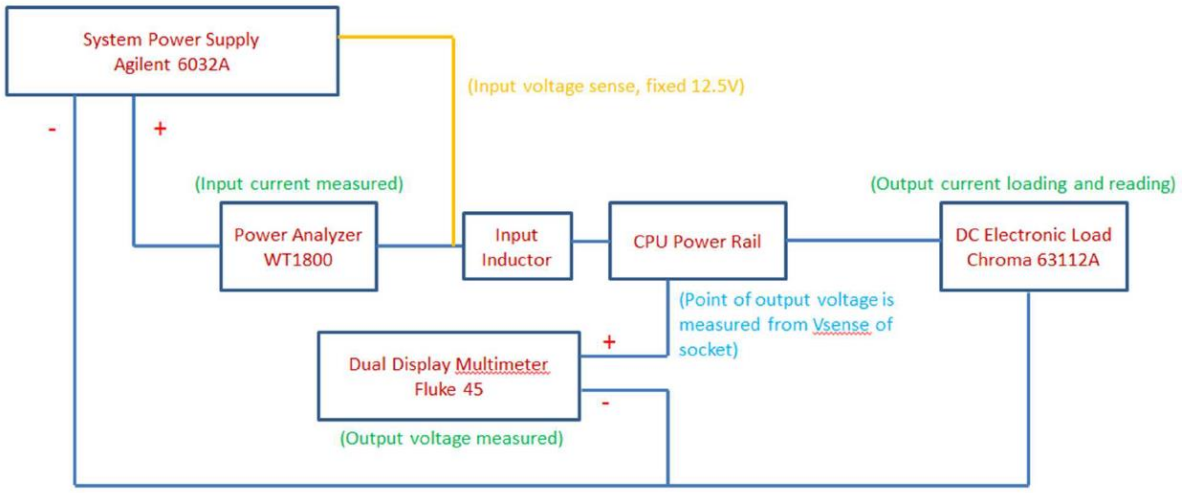
CPU VR should be compliant to latest AMD specification and validation method and pass test with margin.

11.3.3 CPU VRM Efficiency

For CPU efficiency measurement:

- VID is set to 0.9V
- Vin is set to 12V
- Efficiency is measured from input inductor to socket
- Driver and controller loss should be included
- Output voltage is gathered from Vsense of socket
- No additional air flow shall be supplied to the VR area other than the air flow caused by measure tool FAN.
- Test is done in room temperature(20C~25C)
- Voltage measurement shall be done by tool and method with 0.05% accuracy or better.
- Current measurement shall be done by tool and method with 0.05% accuracy or better.
- Efficiency should be over 91% at 20A~100A load.

Below is the efficiency test set up process for reference:



11.3.4 CPU VR configuration

Vendor should use CPU core VR solution with all configurations stored in NVRAM without any external resistor strapping. Vendor should provide utility under CentOS to perform VR configuration change. Configuration change should take effort without AC cycling node. The guaranteed rewrite count of NVRAM should be greater or equal to 15.

11.4 DIMM VR

11.4.1 DIMM maximum power

The motherboard has a DIMM configuration of CPU socket, 4 channels per socket and 2 slots per channel. Vendor should follow memory controller vendor's guideline to design and validate DIMM power rail to support maximum power needed for this configuration, and support 1.2V DDR4 DIMM

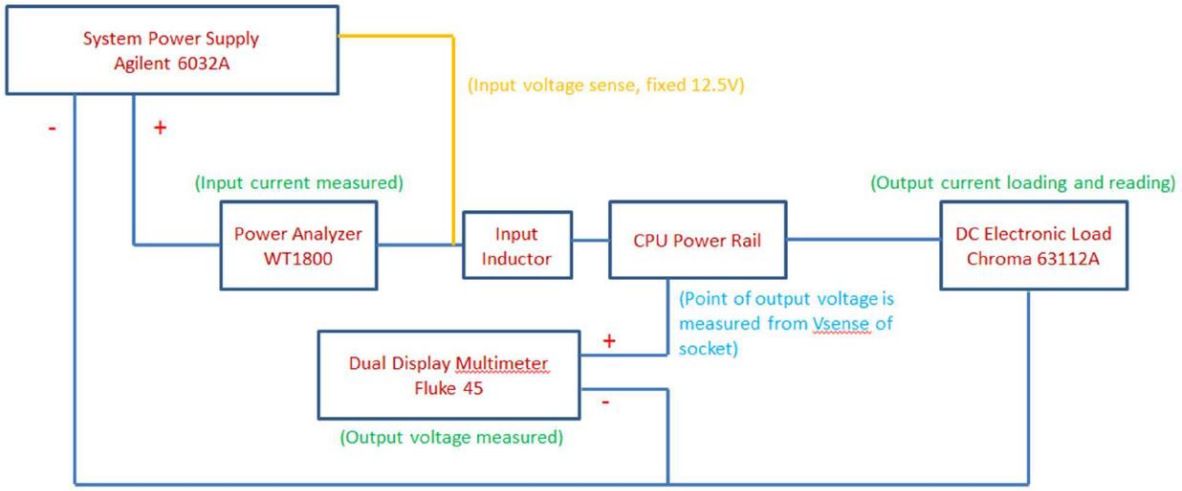
11.4.2 DIMM VR optimizations

DIMM VR should support auto phase dropping for high efficiency across loading. DIMM VR should be compliant to latest AMD specification and memory controller vendor's updated validation guideline, and pass test with margin.

11.4.3 DIMM VR efficiency

- VID is set to 1.2V
- Vin is set to 12V
- Efficiency is measured from input inductor to PCB near DIMM sockets.
- Driver and controller loss should be included
- Output voltage is gathered from PCB at middle of the 2nd and 3rd of 4x DIMM slots.
- No additional air flow shall be supplied to the VR area other than the air flow caused by measure tool FAN.
- Test is done in room temperature(20C~25C)
- Voltage measurement shall be done by tool and method with 0.05% accuracy or better.
- Current measurement shall be done by tool and method with 0.05% accuracy or better.
- Efficiency should be over 87% at 5A~40A load.

Below is the efficiency test set up process for reference:



11.4.4 DIMM VR configuration

DIMM VR has same configuration requirement as CPU VR, listed in 12.3.4.

11.5 MCP (Multi Core Package) VRM

There is 1x voltage regulator module for each CPU socket to supply the power rails needed for MCP Power.

For board that does not need MCP support, MCP VRM and the connector for MCP VRM is not installed. All system functions other than MCP shall still be supported.

11.6 VRM design guideline

For VRM, vendor should list current budget for each power rail based on worst case loading case in all possible operation conditions. General requirements for VR component selection and VR design should meet 120% of this budget, and OCP should set to 130%~200% of this budget. Vendors should do design check, inform purchasers about the actual OCP setting chosen for VRM and explain the reason if it cannot meet this general requirement above.

For VRM which requires firmware or power code or configuration file, vendors should maintain version control to track all the releases and changes between each version, and provide a method to retrieve version through application software during system run time. This software method should run under CentOS 7.x 64 bit with updated Kernel specified by customer.

- Different BOM options and VR firmware are allowed to accommodate AVL with exceptions. Vendor's manufacture process shall be able to handle different BOM, matching AVL of power stage.
- different BOM options do not apply to all other components
  - input/ouput inductor/capacitor shall not have BOM dependency to power stage AVL.
- If different VR firmware is required to support different power stages, VR firmware shall have unique ID in user specific area matching each power stage.

11.7 Hard Drive Power

The motherboard shall supply power to all possible hard drives connected. This means tu support 1A continuous per HDD on 12V power rail, and 0.75A continuous per HDD on 5V power rail. Inrush current required to spin up the drive must also be considered in power delivery design. Both 12V and 5V disk output power rails shall protect against shorts and overload conditions.

11.7.1 Spin-up delay

When hard drive spins up after power on, it draws excessive current on both 12V and 5V. the peak current may reach 1.5A ~ 2A range in 12V. system may have all hard drives installed, so there is need to spin up hard drive in sequence. BIOS should implement 5 seconds delay between each hard drive spinning up. In order to do this, SATA hard drive's power cable should have pin 11 as NC(No connection) to enable hard drive's spin-up delay function.

11.8 System VRM efficiency

Vendors shall supply high efficiency VRMS for all other voltage regulators over 20W not defined in this specification. All other voltage regulation modules shall be 80% efficiency over the 30% to 90% load range. Vendors are encouraged to deliver systems with higher efficiencies. If higher efficiencies are available at additional cost vendors shall present those options.

11.9 Power On

Motherboard should be set to restore last power state during AC on/off. This means that, when AC does on/off cycle, motherboard should power on automatically without requiring power button. Only when motherboard is powered off on purpose, then motherboard should be kept power off through AC on/off.

11.10 High power use case

High power use case means system power is between 480W (40A@12V) and 960W (80A@12V). This is not a typical use case, but need to have support to enable testing of such configuration. Typically it is caused by fully populating NVDIMM, high TDP CPU, and heavy load on PCIe slots, or a combination of the above.

Vendor shall perform simulation during design, and testing during validation for high power kit.

12. Environmental and Regulations

The motherboard shall meet the following environmental requirements:

- Ambient operating temperature range: +5C to +40C
- Operating and Storage relative humidity: 20% to 90%
- Storage temperature range: -40C to +70C
- Transportation temperature range: -40C to +70C

The full system shall meet the following environmental requirements:

- Ambient operating temperature range: +5C to +40C
- Operating and Storage relative humidity: 20% to 90%
- Storage temperature range: -40C to +70C
- Transportation temperature range: -40C to +70C

13. Environmental Requirements

13.1 Vibration & Shock

- OP Vibration: 0.3Grms, 5 to 500 Hz(5-20Hz; 6dB/Oct , 20-200Hz; 0.0003G^2/Hz , 200-500Hz; -6dB/Oct , 20 mins each of the three axes
- OP Shock: 5G, half-sine 11mS, 5 shocks per each of the 3 axes, Operational face (bottom) only
- Non-OP Vibration: 1G acceleration, sine wave, 5-500 Hz , 10 sweeps at 1 oct / min , per each of the 3 axes
- Non-OP Shock: 5G, half-sine 11mS, 10 shocks per each of the 3 axes, Operational face (bottom) only

13.2 Regulations

The components used on motherboard need to have rack level CE, and the sled should be compliant with RoHS and WEEE. The Capri mother board should have UL 94 V-0 certificate. The vendor should design an EMI panel kit and pass FCC Class A.

14. Prescribed Materials

14.1 Disallowed Components

The disallowed components in Capri follows the European Union's Restriction of Hazardous Substances Directive (RoHS).