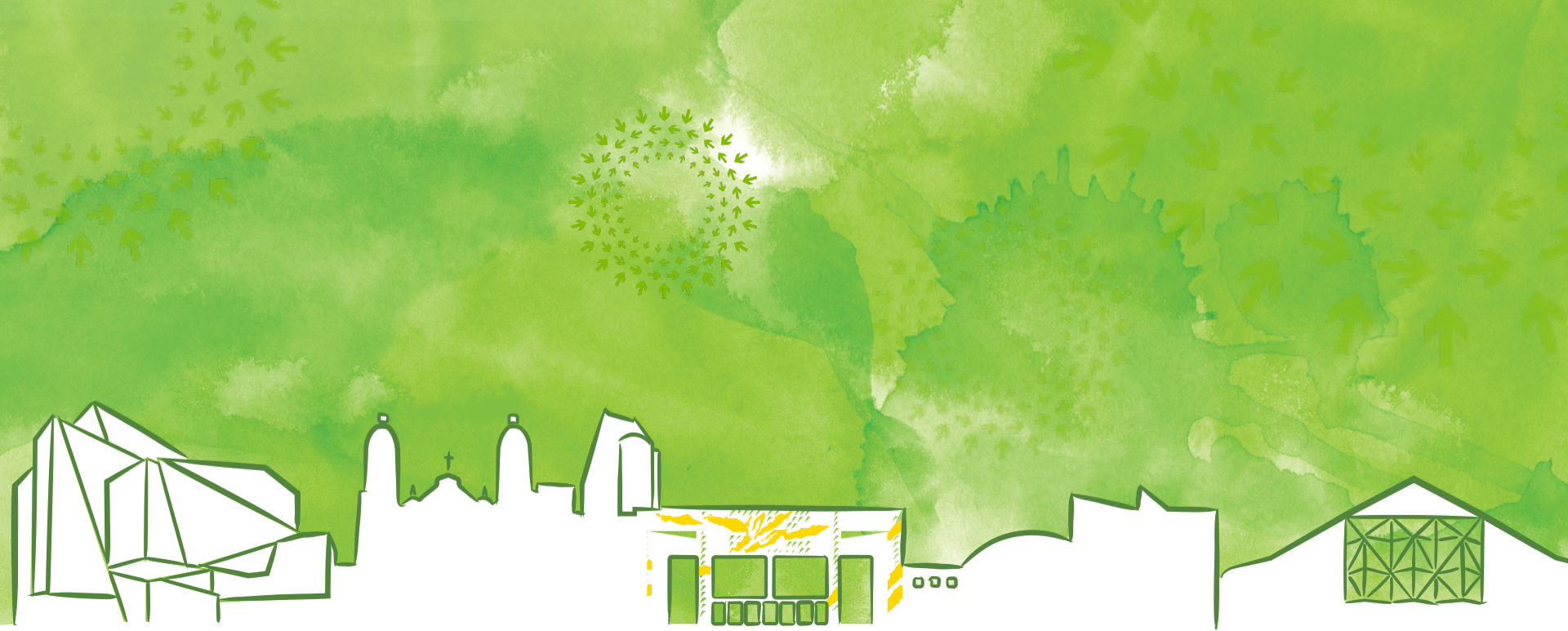

OCP Engineering Workshop 25 September 2017| Dallas, TX

OCP Engineering Workshop – 25 September 2017 – Dallas, TX

OCP NIC 3.0

Dell EMC Update

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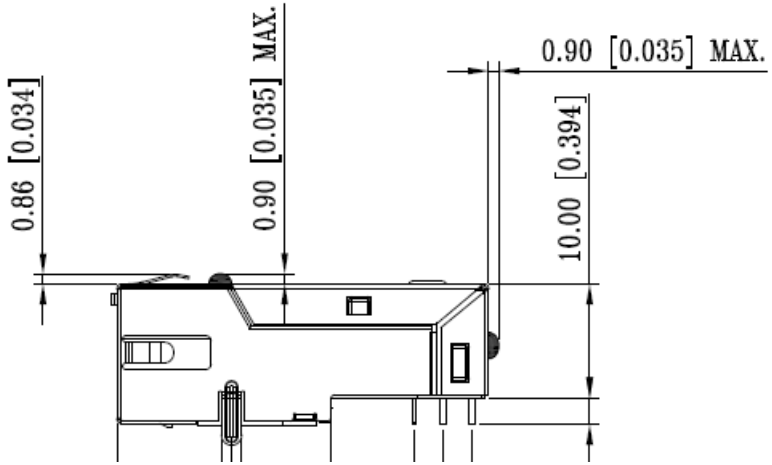
Distinguished Engineer

Agenda

- Form Factor Update
- Pinout:
  - Proposed changes to some pins/features
  - Pinout proposal for Connector A and B
- Closing thoughts

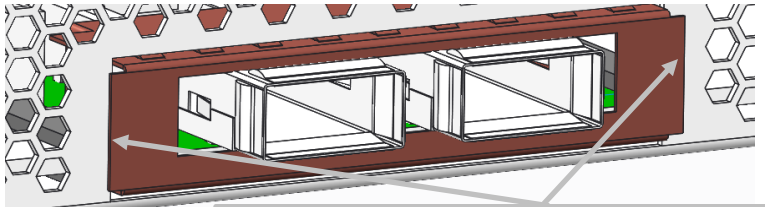
Form Factor

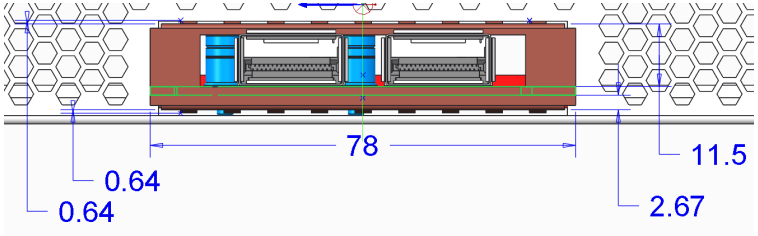


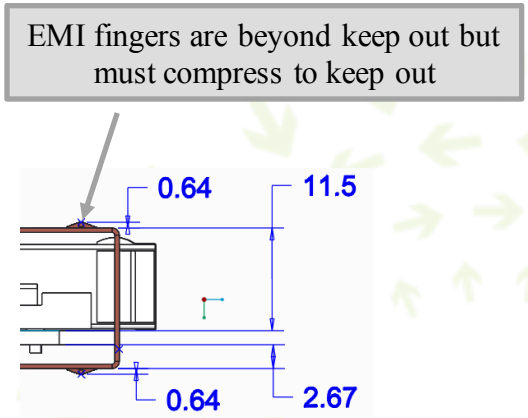
- Enumeration 14: 76 mm x 115 mm
- Top-side keepout: 11.0 mm
- Bottom-side keepout: 2.25 mm < x < 2.67 mm
  - Really need the NIC vendors to finalize this number.
- Motherboard Thickness: Agree with 0.062", 0.076" and 0.093" +/- 10% tolerances.
  - Allows a wide range of layer counts and materials to be supported.
- Connector A = SFF-TA-1002 style 168 pin straddle mount connector.
- Connector B → Proposing 140 pin to allow a full x16.
- RJ-45 connectors should be mid-plane mounted. (3D models available)
  - 1x1 max top side height is 8.8 mm
  - 1x4 max top side height is 10.0 mm

Faceplate Spec Definition

- Dell prefers design similar to the design shown:
  - Enables EMI solution on card.
  - Enables convenient space for latching.
  - Minimizes vertical stack.
- Design intent and spec details:
  - Top/Bottom fold over and are inserted into the chassis.
  - Left/Right side EMI seal flush against rear wall.
  - EMI fingers need to compress to be flush with top/bottom flanges.
  - Proposal gives flexibility for different connectors.
- Open Items, in order:
  - Do we need to protect the entire underside of card for installation?
  - Retention mechanism selection and definition (internal/external/both?)
    - Options for latching could include ¼ turn retention.
  - Should EMI fingers be on card or designed into chassis?
  - Do we need to specify LED locations, definitions, … ?

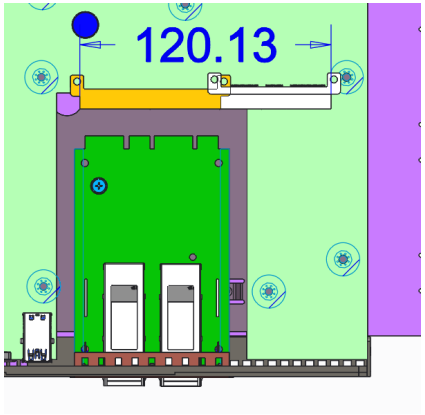


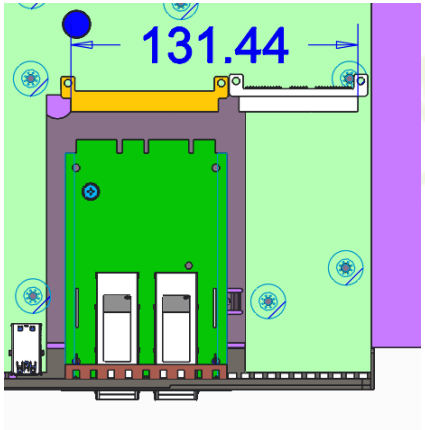




Wider Card Consideration

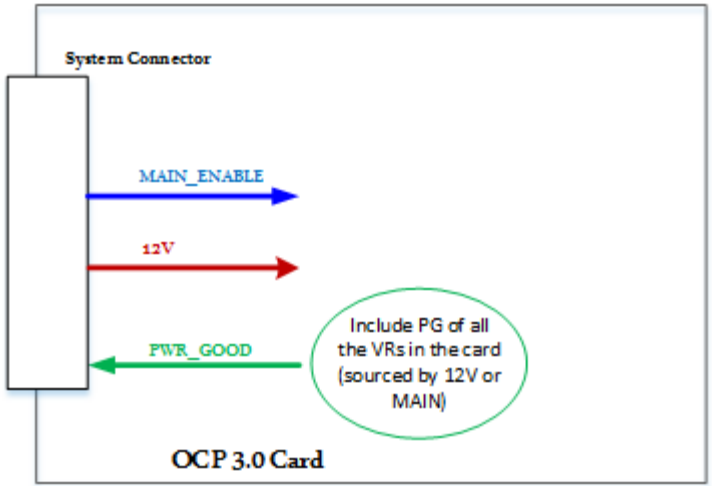
- For the wider board Dell EMC would like to see the board grow to the right instead of the left.
  - Prefer a x16 on the additional section
  - Grow width to support additional 140 pin
- Top picture: Single connector instead of 2 connectors. Not sure if this is possible but would represent the minimum width for a wider card = ~127mm.
- Bottom picture: Connector B = 140 pins from the current concept models for the connector suppliers. The would make the card ~138mm.

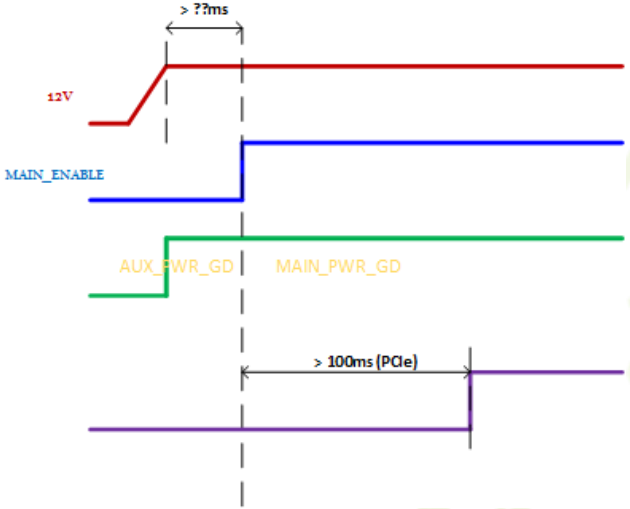




Proposed Pinout Description

- Power
  - Repurpose the 12VAUX pins
  - 6 – 12V pins ~= 79W which should be sufficient (assume 1.1A per pin)
  - MAIN_EN: Signal from System to NIC indicating main power available.
  - PWR_GOOD: Signal from NIC to System indicating VRs are operating nominally.
    - Includes all NIC rails.



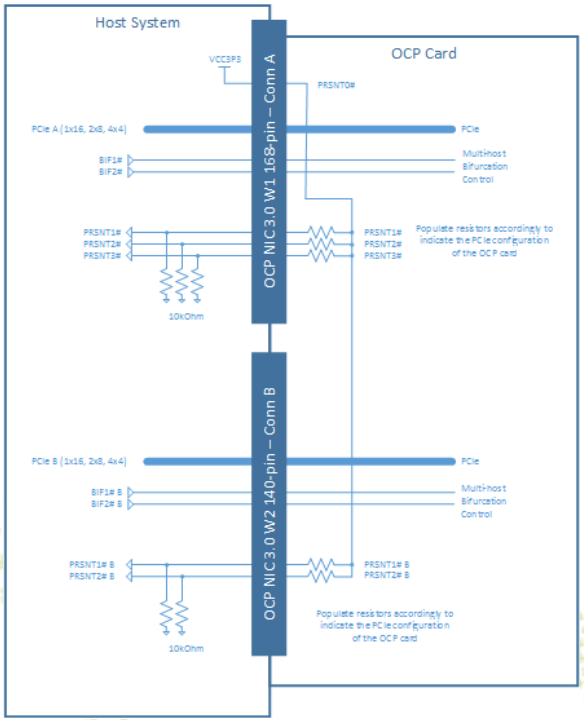


Pinout - continued

- Deprecate CLK_REQ
- Systems Management:
  - One SMBus
    - Includes FRU and temp sensor
  - One NC-SI RBT bus (including arbitration pins)
  - Add at least one “addressing” pin to enable dual OCP NIC 3.0 on the same management bus: SLOT_ID
    - I2C address changed
    - NC-SI package ID changed (This assumes that the maximum number of OCP NIC 3.0 cards on a bus is 2. Additional addressing pins would be necessary if that increased.)
- Multi-Host: For Gen4/5 PCIe x4 ports seem to be an optimal choice
  - 4 x {PERST#, WAKE#, REFCLK}
    - REFCLK likely still required prior to Gen 5 PCIe!
- Connector B: (140 pin to include x16)
  - 12V pins – 5 additional pins to increase power to ~145W (nominal assuming 1.1A per pin)
  - Multi-host support (4 sets of PERST#, WAKE#, REFCLK)

Pinout - continued

- Presence/Bifurcation
  - Dual-purpose the existing 3 presence pins and add 2 pins (BIFn#).
    - Allows for bidirectional bifurcation



Multi-host Bifurcation (from Host to OCP card)

W1 Conn A		W2 Conn B		Host Root Port Configuration	
BIF1#	BIF2#	BIF1# B	BIF2# B	Bus A	Bus B
0	0	0		x16	x16
1	0	0		2 x8	2 x8
0	1	0		4 x4	4 x4
1	1	0		x16	2 x8
0	0	1		x16	4 x4
1	0	1		2 x8	x16
0	1	1		2 x8	4 x4
1	1	1		4 x4	x16
				4 x4	2 x8

Root Port Bifurcation (from OCP card to Host)

W1 Conn A			W2 Conn B		Conn A End Device Config	Conn B End Device Config
PRSNT3#	PRSNT2#	PRSNT1#	PRSNT2# B	PRSNT1# B		
RFU	0	0	0	0	Not present	Not present
RFU	0	1	0	0	x16	Not present
RFU	1	0	0	0	2 x8	Not present
RFU	1	1	0	0	RFU	Not present
RFU	0	1	0	1	x16	x16
RFU	1	0	0	1	2 x8	x16
RFU	1	1	0	1	RFU	x16
RFU	0	1	1	0	x16	2 x8
RFU	1	0	1	0	2 x8	2 x8
RFU	1	1	1	0	RFU	2 x8
RFU	0	1	1	1	x16	RFU
RFU	1	0	1	1	2 x8	RFU
RFU	1	1	1	1	x32	

OCP x16 168 pin

Pin	Connector (lower row) Side B Signals	Connector (upper row) Side A Signals	Pin
1	Rsv	GND	1
2	Rsv	GND	2
3	Rsv	GND	3
4	PRSNT0#	MCSI_CLK	4
5	MCSI_CRSD	MCSI_TXEN	5
6	MCSI_RXD1	MCSI_TXD1	6
7	MCSI_RXD0	MCSI_TXD0	7
8	GND	GND	8
9	SLOTID	MCSI_ARB_IN	9
10	Rsv	MCSI_ARB_OUT	10
11	GND	GND	11
12	REFCLKn2	REFCLKn3	12
13	REFCLKp2	REFCLKp3	13
14	GND	GND	14
	Key	Key	
1	12V	GND	1
2	12V	GND	2
3	12V	GND	3
4	12V	GND	4
5	12V	GND	5
6	12V	GND	6
7	PWR_GOOD	SMCLK	7
8	PWR_BREAK	SMDAT	8
9	MAIN_EN	SMRST#/RFU	9
10	PERST0#	PERST1#	10
11	WAKE0#	WAKE1#	11
12	PWRDIS	PRSNT1#	12
13	GND	GND	13
14	REFCLKn0	REFCLKn1	14
15	REFCLKp0	REFCLKp1	15
16	GND	GND	16
17	PERn0	PETn0	17
18	PERp0	PETp0	18
19	GND	GND	19
20	PERn1	PETn1	20
21	PERp1	PETp1	21
22	GND	GND	22
23	PERn2	PETn2	23
24	PERp2	PETp2	24
25	GND	GND	25
26	PERn3	PETn3	26
27	PERp3	PETp3	27
28	GND	GND	28
	Key	Key	
29	GND	GND	29
30	PERn4	PETn4	30
31	PERp4	PETp4	31
32	GND	GND	32
33	PERn5	PETn5	33
34	PERp5	PETp5	34
35	GND	GND	35
36	PERn6	PETn6	36
37	PERp6	PETp6	37
38	GND	GND	38
39	PERn7	PETn7	39
40	PERp7	PETp7	40
41	GND	GND	41
42	PRSNT2#	BIF1#/RFU	42
	Key	Key	
43	GND	GND	43
44	PERn8	PETn8	44
45	PERp8	PETp8	45
46	GND	GND	46
47	PERn9	PETn9	47
48	PERp9	PETp9	48
49	GND	GND	49
50	PERn10	PETn10	50
51	PERp10	PETp10	51
52	GND	GND	52
53	PERn11	PETn11	53
54	PERp11	PETp11	54
55	GND	GND	55
56	PERn12	PETn12	56
57	PERp12	PETp12	57
58	GND	GND	58
59	PERn13	PETn13	59
60	PERp13	PETp13	60
61	GND	GND	61
62	PERn14	PETn14	62
63	PERp14	PETp14	63
64	GND	GND	64
65	PERn15	PETn15	65
66	PERp15	PETp15	66
67	GND	GND	67
68	PERST2#	PERST3#	68
69	WAKE2#	WAKE3#	69
70	PRSNT3#	BIF2#/RFU	70

Proposed pinout

Pin	Connector (lower row) Side B Signals	Connector (upper row) Side A Signals	Pin
1	12V	GND	1
2	12V	GND	2
3	12V	GND	3
4	12V	GND	4
5	12V	GND	5
6	Rsv	Rsv	6
7	PERST0#	PERST1#	7
8	WAKE0#	WAKE1#	8
9	Rsv	PRSNT0#	9
10	GND	GND	10
11	REFCLKn2	REFCLKn3	11
12	REFCLKp2	REFCLKp3	12
13	GND	GND	13
14	REFCLKn0	REFCLKn1	14
15	REFCLKp0	REFCLKp1	15
16	GND	GND	16
17	PERn0	PETn0	17
18	PERp0	PETp0	18
19	GND	GND	19
20	PERn1	PETn1	20
21	PERp1	PETp1	21
22	GND	GND	22
23	PERn2	PETn2	23
24	PERp2	PETp2	24
25	GND	GND	25
26	PERn3	PETn3	26
27	PERp3	PETp3	27
28	GND	GND	28
	Key	Key	
29	GND	GND	29
30	PERn4	PETn4	30
31	PERp4	PETp4	31
32	GND	GND	32
33	PERn5	PETn5	33
34	PERp5	PETp5	34
35	GND	GND	35
36	PERn6	PETn6	36
37	PERp6	PETp6	37
38	GND	GND	38
39	PERn7	PETn7	39
40	PERp7	PETp7	40
41	GND	GND	41
42	PRSNT1#	BIF1#/RFU	42
	Key	Key	
43	GND	GND	43
44	PERn8	PETn8	44
45	PERp8	PETp8	45
46	GND	GND	46
47	PERn9	PETn9	47
48	PERp9	PETp9	48
49	GND	GND	49
50	PERn10	PETn10	50
51	PERp10	PETp10	51
52	GND	GND	52
53	PERn11	PETn11	53
54	PERp11	PETp11	54
55	GND	GND	55
56	PERn12	PETn12	56
57	PERp12	PETp12	57
58	GND	GND	58
59	PERn13	PETn13	59
60	PERp13	PETp13	60
61	GND	GND	61
62	PERn14	PETn14	62
63	PERp14	PETp14	63
64	GND	GND	64
65	PERn15	PETn15	65
66	PERp15	PETp15	66
67	GND	GND	67
68	PERST2#	PERST3#	68
69	WAKE2#	WAKE3#	69
70	PRSNT2#	BIF2#/RFU	70

Closing Thoughts

- Given the current trajectory it would be nice to get together more frequently in targeted groups for discussions to close open items:
  - Mechanical: Faceplate, latching mechanism, ...
  - Pinout: definition of pins, new features, …

- Contact information:

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