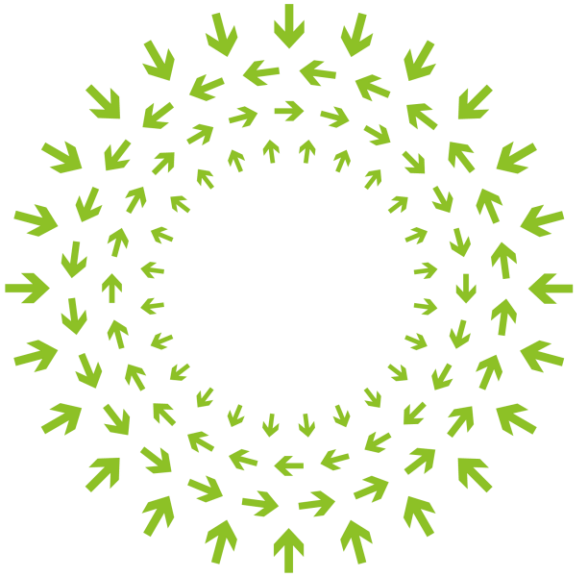

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Compute Project

<Decathlete v3 Specification>

<Revision 1.0>

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Table of Contents

2 Scope

This document defines the technical specifications for the Open Compute Project Decathlete v3

2.1 Overview

The Decathlete v3 will be IA-64 based dual-socket motherboard that supports the Purley – EP processors in combination with the Lewisburg PCH (PCH) to provide a balanced feature set between technology leadership and cost.

The intended audiences for this document are the Purley platform technical leads, software team, validation team, and board design engineers that need to utilize a comprehensive package. This document will provide the specific features that are required to be implemented on the boards. Product feature requirements and block diagrams will be provided.

Links to reference documents that dive into the implementation for the software stack, common-core solution, server management architecture, fan-speed control architecture, chassis, power budget, and thermal requirements are provided.

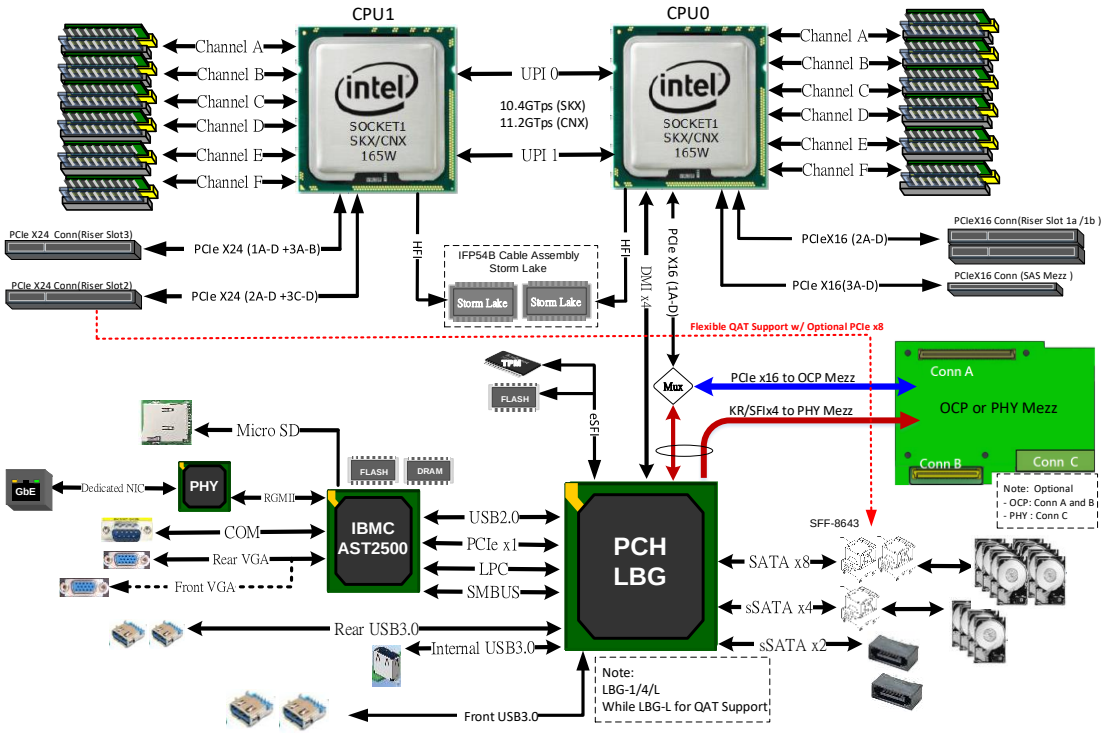
3 Feature Requirements

The Decathlete v3 24 DIMMs Server board will be Purley server product. The silicon ingredients and features are as follows list:

Table 1. Purley Decathlete v3 Feature List

Board Name	**Purley Server Baseboard**
Baseboard size	17.5” x 16.7”, 8 layer, 1.8mm, 24 DIMMs
CPU	Intel Skylake E5-2600V5, P0 Socket - Skylake Server Processor **without** Integrated Fabric (“SKL”) - Skylake Server Processor **with** Integrated Fabric (“SKL-F”)
Max Processor Wattage	205W, Optimized power delivery for 85W, VRD 13
UPI Speed	10.4 GT/s, 9.6GT/s
Chipset	Intel (R) C62x series chipset (Lewisburg) LBG-1 C621/LBG-4 C624and LBG-L C628
Memory	ECC RDIMM/ LRDIMM slots Up to 3TB (128Gx24) of memory for LRDIMM Up to 3TB (128Gx24) of memory for RDIMM Up to 7.5TB (128Gx12 AEP + 512G x12 RDIMM) of memory for AEP DIMM
Misc Features	(2) USB 3.0 ports (1) VGA port (BMC AST2500 SKU only) (1) RS232 serial port (1) ID LED (1) LAN (through OCP/PHY MEZZ)
Video	ASPEED AST2500 8MB DDR4 video memory
TPM	Yes (Option, SPI Mode)
System management	IPMI v2.0 Compliant, on board "KVM over IP" support

3.1 Architecture Block Diagram



3.2 BASEBOARD Dimensions

L 453mm (17.8”) X W 424.2mm (16.7 “)

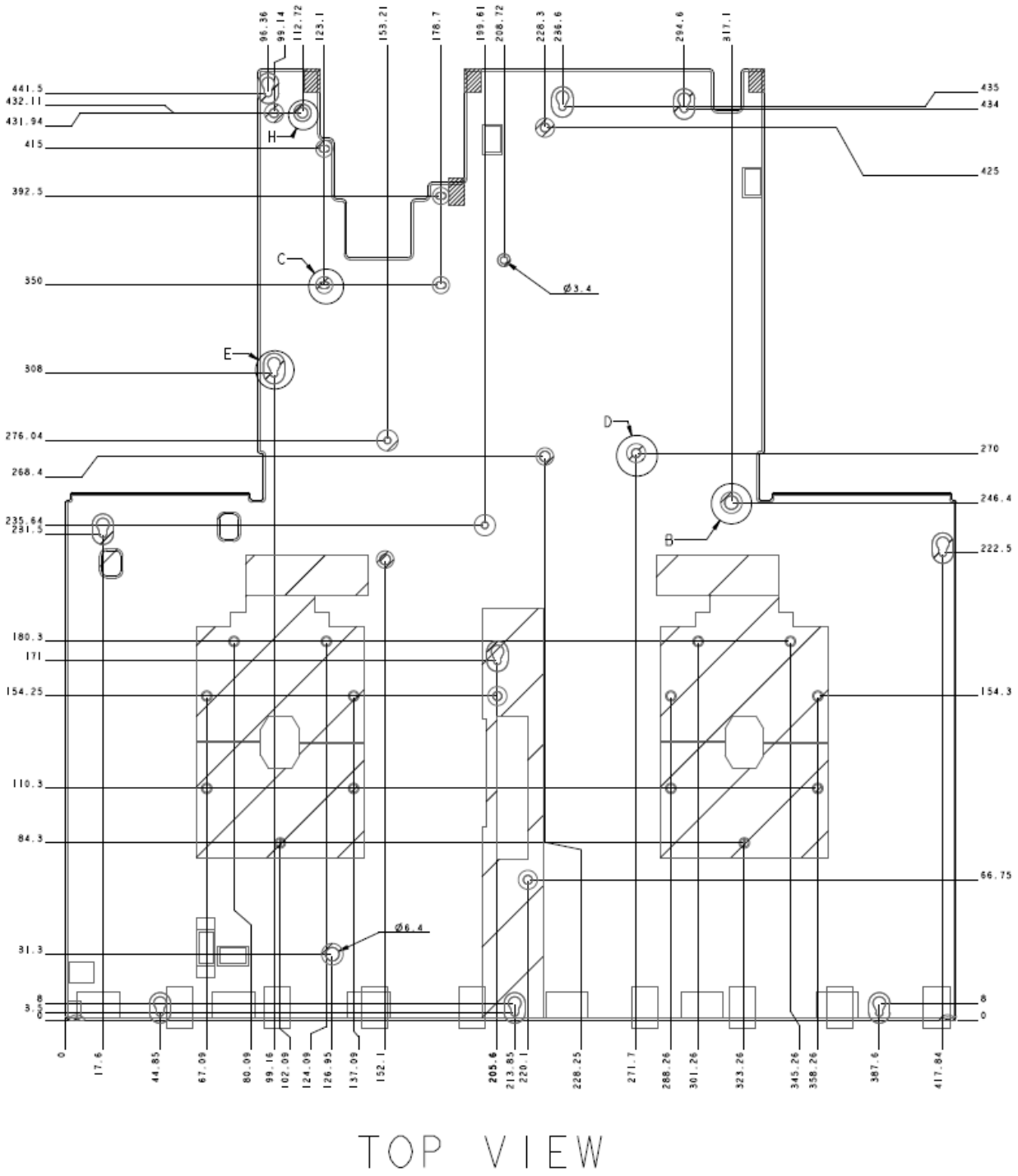


Figure 1 Purley 2S Decathlete v3 Baseboard Dimension

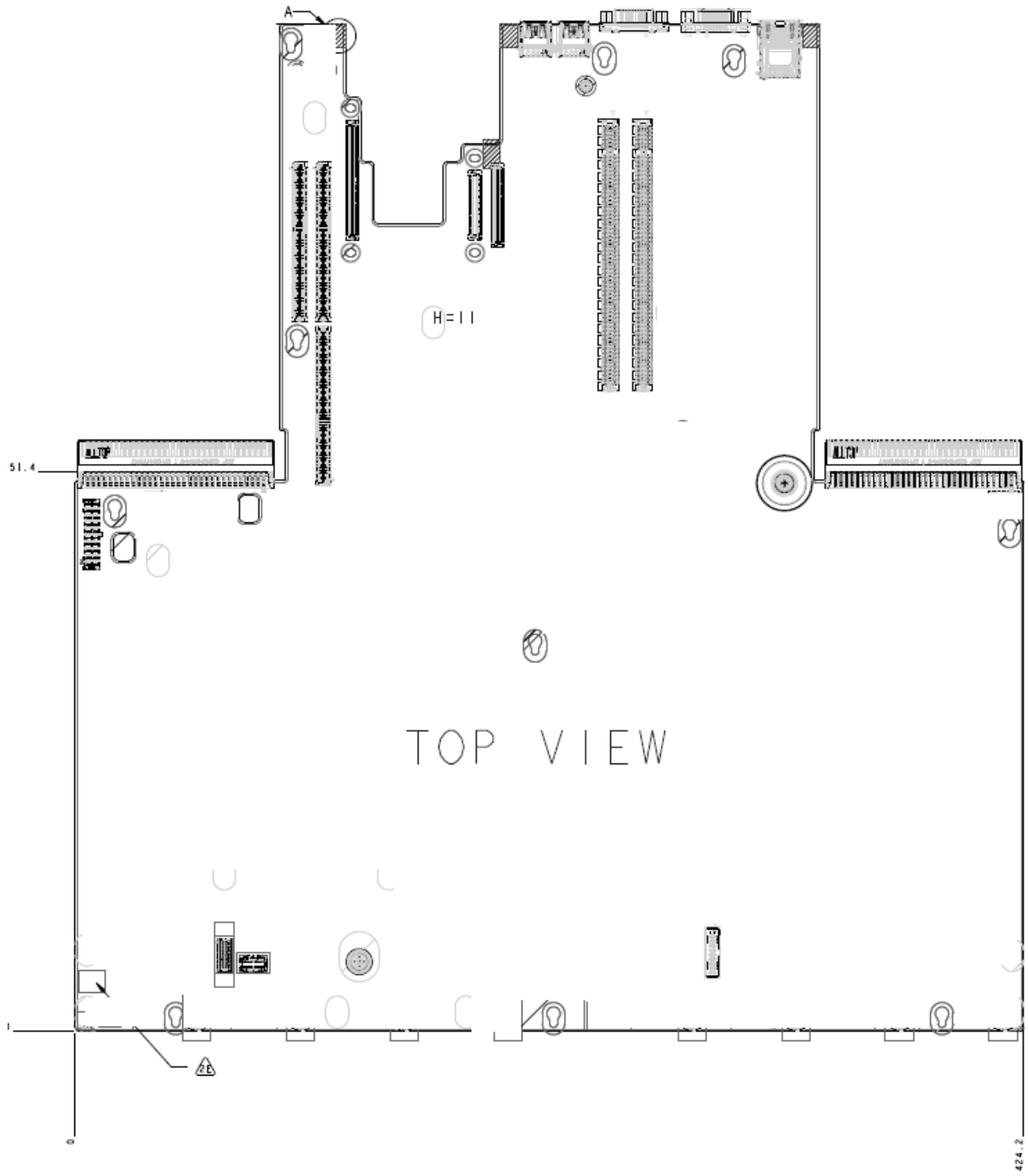


Figure 2 Purley 2S Decathlete v3 Baseboard Dimension

3.3 PCIe Riser

PCI Express* Gen1, Gen2 and Gen 3 are dual-simplex point-to point serial differential low-voltage interconnects. The signaling bit rate is 2.5 Gb/s one direction per lane for Gen1 (8b/10b encoding), 5.0 Gbit/s one direction per lane for Gen2 (8b/10b encoding) and 8.0 Gb/s one direction per lane for Gen3 (128b/130b encoding). Each port consists of a transmitter and receiver pair. A link between the ports of two devices is a collection of lanes (x1, x2, x4, x8, x16, etc.).

There are multi types of Riser boards, PHY, and Mezzanine boards for this project. Also we will have PCIe SSD Backplane connected to motherboard via Cable. The follow table lists of this project.

Table 2. Riser and Mezzanine list

Description		
	Riser 1A (PCIex16)	Support (1) PCIe Gen3 x16 Add-on Card
	Riser2 (PCIex24)	Support (1) PCIe Gen3 x16 and x8 Add-on Card
	Riser3 (PCIex24)	Support (1) PCIe Gen3 x16 and x8 Add-on Card
	Riser4 (PCIex16)	Support (1) SAS MEZZ PCIe Gen3 x16
	OCP Mezz	PCIe x16 OCP 2.0 connector NCSI interface support

3.3.1 Riser Slot PINOUT

3.3.1.1 Riser 1A PINOUT Definition

Table 3. PIN definition of PCIe Riser 1A

Riser 1A			
Name	PIN		Name
P12V	1	2	P12V
P12V	3	4	P12V
P12V	5	6	P12V
P12V	7	8	GND
FM_SYS_THROTTLE_PCIE_RISER3AB_N	9	10	P3V3
P3V3	11	12	P3V3
P3V3	13	14	P3V3
FM_RISER3B_SLOT_PRSNT_PE9_N	15	16	RST_PCIE_RISER3B_N
P3V3_AUX	17	18	SMB_RISER3B_3V3AUX_SCL
IRQ_LVC3_WAKE_N	19	20	SMB_RISER3B_3V3AUX_SDA
CPU0_RISER1AB_TYPE_ID0	21	22	GND
FM_RISER3B_SLOT_PRSNT_PE10_N	23	24	CLK_100M_PE_9_DP
GND	25	26	CLK_100M_PE_9_DN
P3E_CPU0_ PE1_3B _TX_C_DP0	27	28	GND
P3E_CPU0_ PE1_3B _TX_C_DN0	29	30	GND
GND	31	32	P3E_CPU0_PE1_3B_RX_C_DP0
GND	33	34	P3E_CPU0_PE1_3B_RX_C_DN0
P3E_CPU0_PE1_3B_TX_C_DP1	35	36	GND
P3E_CPU0_PE1_3B_TX_C_DN1	37	38	GND
GND	39	40	P3E_CPU0_PE1_3B_RX_C_DP1
GND	41	42	P3E_CPU0_PE1_3B_RX_C_DN1
P3E_CPU0_PE1_3B_TX_C_DP2	43	44	GND
P3E_CPU0_PE1_3B_TX_C_DN2	45	46	GND
GND	47	48	P3E_CPU0_PE1_3B_RX_C_DP2
GND	49	50	P3E_CPU0_PE1_3B_RX_C_DN2
P3E_CPU0_PE1_3B_TX_C_DP3	51	52	GND
P3E_CPU0_PE1_3B_TX_C_DN3	53	54	GND
GND	55	56	P3E_CPU0_PE1_3B_RX_C_DP3
GND	57	58	P3E_CPU0_PE1_3B_RX_C_DN3

P3E_CPU0_PE1_3B_TX_C_DP4	59	60	GND
P3E_CPU0_PE1_3B_TX_C_DN4	61	62	GND
GND	63	64	PCIE_RISER1AB_PRSNT_N
CPU0_RISER1AB_TYPE_ID1	65	66	GND
GND	67	68	P3E_CPU0_PE1_3B_RX_C_DP4
GND	69	70	P3E_CPU0_PE1_3B_RX_C_DN4
P3E_CPU0_PE1_3B_TX_C_DP5	71	72	GND
P3E_CPU0_PE1_3B_TX_C_DN5	73	74	GND
GND	75	76	P3E_CPU0_PE1_3B_RX_C_DP5
GND	77	78	P3E_CPU0_PE1_3B_RX_C_DN5
P3E_CPU0_PE1_3B_TX_C_DP6	79	80	GND
P3E_CPU0_PE1_3B_TX_C_DN6	81	82	GND
GND	83	84	P3E_CPU0_PE1_3B_RX_C_DP6
GND	85	86	P3E_CPU0_PE1_3B_RX_C_DN6
P3E_CPU0_PE1_3B_TX_C_DP7	87	88	GND
P3E_CPU0_PE1_3B_TX_C_DN7	89	90	GND
GND	91	92	P3E_CPU0_PE1_3B_RX_C_DP7
GND	93	94	P3E_CPU0_PE1_3B_RX_C_DN7
P3E_CPU0_PE1_3B_TX_C_DP8	95	96	GND
P3E_CPU0_PE1_3B_TX_C_DN8	97	98	GND
GND	99	100	P3E_CPU0_PE1_3B_RX_C_DP8
GND	101	102	P3E_CPU0_PE1_3B_RX_C_DN8
P3E_CPU0_PE1_3B_TX_C_DP9	103	104	GND
P3E_CPU0_PE1_3B_TX_C_DN9	105	106	GND
GND	107	108	P3E_CPU0_PE1_3B_RX_C_DP9
GND	109	110	P3E_CPU0_PE1_3B_RX_C_DN9
P3E_CPU0_PE1_3B_TX_C_DP10	111	112	GND
P3E_CPU0_PE1_3B_TX_C_DN10	113	114	GND
GND	115	116	P3E_CPU0_PE1_3B_RX_C_DP10
GND	117	118	P3E_CPU0_PE1_3B_RX_C_DN10
P3E_CPU0_PE1_3B_TX_C_DP11	119	120	GND
P3E_CPU0_PE1_3B_TX_C_DN11	121	122	GND
GND	123	124	P3E_CPU0_PE1_3B_RX_C_DP11
GND	125	126	P3E_CPU0_PE1_3B_RX_C_DN11
P3E_CPU0_PE1_3B_TX_C_DP12	127	128	GND
P3E_CPU0_PE1_3B_TX_C_DN12	129	130	GND
GND	131	132	P3E_CPU0_PE1_3B_RX_C_DP12

GND	133	134	P3E_CPU0_PE1_3B_RX_C_DN12
P3E_CPU0_PE1_3B_TX_C_DP13	135	136	GND
P3E_CPU0_PE1_3B_TX_C_DN13	137	138	GND
GND	139	140	P3E_CPU0_PE1_3B_RX_C_DP13
GND	141	142	P3E_CPU0_PE1_3B_RX_C_DN13
P3E_CPU0_PE1_3B_TX_C_DP14	143	144	GND
P3E_CPU0_PE1_3B_TX_C_DN14	145	146	GND
GND	147	148	P3E_CPU0_PE1_3B_RX_C_DP14
GND	149	150	P3E_CPU0_PE1_3B_RX_C_DN14
P3E_CPU0_PE1_3B_TX_C_DP15	151	152	GND
P3E_CPU0_PE1_3B_TX_C_DN15	153	154	GND
GND	155	156	P3E_CPU0_PE1_3B_RX_C_DP15
CLK_100M_PE_9_DP	157	158	P3E_CPU0_PE1_3B_RX_C_DN15
CLK_100M_PE_9_DN	159	160	GND

3.3.1.2 Riser 2 PINOUT Definition

Table 4. PIN definition of PCIe Riser 2

Riser 2			
Name	PIN		Name
P12V	B1	A1	GND
P12V	B2	A2	P12V
P12V	B3	A3	P12V
GND	B4	A4	P12V
P3V3	B5	A5	GND
P3V3	B6	A6	P3V3
P3V3	B7	A7	P3V3
P3V3	B8	A8	P3V3
GND	B9	A9	P3V3
P3V3_AUX	B10	A10	P3V3
IRQ_LVC3_WAKE_N	B11	A11	GND
TP_SLOT2_B12	B12	A12	RST_PERST1_N
SMB_PCI_3V3SB_CLK	B13	A13	SLOT2_PRESENT_N
SM B_PCI_3V3SB_DAT_SLOT2	B14	A14	FM_RISER2_CFG0
GND	B15	A15	FM_RISER2_CFG1
CLK_100M_PE4_DP	B16	A16	GND
CLK_100M_PE4_DN	B17	A17	CLK_100M_PE5_DP
GND	B18	A18	CLK_100M_PE5_DN
CLK_100M_PE6_DP	B19	A19	GND
CLK_100M_PE6_DN	B20	A20	P3E_CPU1_PCIE3_RX_DP8
GND	B21	A21	P3E_CPU1_PCIE3_RX_DN8
P3E_CPU1_PCIE3_TX_C_DP8	B22	A22	GND
P3E_CPU1_PCIE3_TX_C_DN8	B23	A23	GND
GND	B24	A24	P3E_CPU1_PCIE3_RX_DP9
GND	B25	A25	P3E_CPU1_PCIE3_RX_DN9
P3E_CPU1_PCIE3_TX_C_DP9	B26	A26	GND
P3E_CPU1_PCIE3_TX_C_DN9	B27	A27	GND
GND	B28	A28	P3E_CPU1_PCIE3_RX_DP10
GND	B29	A29	P3E_CPU1_PCIE3_RX_DN10
P3E_CPU1_PCIE3_TX_C_DP10	B30	A30	GND

P3E_CPU1_PCIE3_TX_C_DN10	B31	A31	GND
GND	B32	A32	P3E_CPU1_PCIE3_RX_DP11
GND	B33	A33	P3E_CPU1_PCIE3_RX_DN11
P3E_CPU1_PCIE3_TX_C_DP11	B34	A34	GND
P3E_CPU1_PCIE3_TX_C_DN11	B35	A35	GND
GND	B36	A36	P3E_CPU1_PCIE3_RX_DP12
GND	B37	A37	P3E_CPU1_PCIE3_RX_DN12
P3E_CPU1_PCIE3_TX_C_DP12	B38	A38	GND
P3E_CPU1_PCIE3_TX_C_DN12	B39	A39	GND
GND	B40	A40	P3E_CPU1_PCIE3_RX_DP13
GND	B41	A41	P3E_CPU1_PCIE3_RX_DN13
P3E_CPU1_PCIE3_TX_C_DP13	B42	A42	GND
P3E_CPU1_PCIE3_TX_C_DN13	B43	A43	GND
GND	B44	A44	P3E_CPU1_PCIE3_RX_DP14
GND	B45	A45	P3E_CPU1_PCIE3_RX_DN14
P3E_CPU1_PCIE3_TX_C_DP14	B46	A46	GND
P3E_CPU1_PCIE3_TX_C_DN14	B47	A47	GND
GND	B48	A48	P3E_CPU1_PCIE3_RX_DP15
GND	B49	A49	P3E_CPU1_PCIE3_RX_DN15
P3E_CPU1_PCIE3_TX_C_DP15	B50	A50	GND
P3E_CPU1_PCIE3_TX_C_DN15	B51	A51	GND
GND	B52	A52	P3E_CPU1_PCIE2_RX_DP0
GND	B53	A53	P3E_CPU1_PCIE2_RX_DN0
P3E_CPU0_PCIE2_TX_C_DP0	B54	A54	GND
P3E_CPU0_PCIE2_TX_C_DN0	B55	A55	GND
GND	B56	A56	P3E_CPU1_PCIE2_RX_DP1
GND	B57	A57	P3E_CPU1_PCIE2_RX_DN1
P3E_CPU0_PCIE2_TX_C_DP1	B58	A58	GND
P3E_CPU0_PCIE2_TX_C_DN1	B59	A59	GND
GND	B60	A60	P3E_CPU1_PCIE2_RX_DP2
GND	B61	A61	P3E_CPU1_PCIE2_RX_DN2
P3E_CPU0_PCIE2_TX_C_DP2	B62	A62	GND
P3E_CPU0_PCIE2_TX_C_DN2	B63	A63	GND
GND	B64	A64	P3E_CPU1_PCIE2_RX_DP3
GND	B65	A65	P3E_CPU1_PCIE2_RX_DN3
P3E_CPU0_PCIE2_TX_C_DP3	B66	A66	GND
P3E_CPU0_PCIE2_TX_C_DN3	B67	A67	GND

GND	B68	A68	P3E_CPU1_PCIE2_RX_DP4
GND	B69	A69	P3E_CPU1_PCIE2_RX_DN4
P3E_CPU0_PCIE2_TX_C_DP4	B70	A70	GND
P3E_CPU0_PCIE2_TX_C_DN4	B71	A71	GND
GND	B72	A72	P3E_CPU1_PCIE2_RX_DP5
GND	B73	A73	P3E_CPU1_PCIE2_RX_DN5
P3E_CPU0_PCIE2_TX_C_DP5	B74	A74	GND
P3E_CPU0_PCIE2_TX_C_DN5	B75	A75	GND
GND	B76	A76	P3E_CPU1_PCIE2_RX_DP6
GND	B77	A77	P3E_CPU1_PCIE2_RX_DN6
P3E_CPU0_PCIE2_TX_C_DP6	B78	A78	GND
P3E_CPU0_PCIE2_TX_C_DN6	B79	A79	GND
GND	B80	A80	P3E_CPU1_PCIE2_RX_DP7
GND	B81	A81	P3E_CPU1_PCIE2_RX_DN7
P3E_CPU0_PCIE2_TX_C_DP7	B82	A82	GND
P3E_CPU0_PCIE2_TX_C_DN7	B83	A83	GND
GND	B84	A84	P3E_CPU1_PCIE2_RX_DP8
GND	B85	A85	P3E_CPU1_PCIE2_RX_DN8
P3E_CPU0_PCIE2_TX_C_DP8	B86	A86	GND
P3E_CPU0_PCIE2_TX_C_DN8	B87	A87	GND
GND	B88	A88	P3E_CPU1_PCIE2_RX_DP9
GND	B89	A89	P3E_CPU1_PCIE2_RX_DN9
P3E_CPU0_PCIE2_TX_C_DP9	B90	A90	GND
P3E_CPU0_PCIE2_TX_C_DN9	B91	A91	GND
GND	B92	A92	P3E_CPU1_PCIE2_RX_DP10
GND	B93	A93	P3E_CPU1_PCIE2_RX_DN10
P3E_CPU0_PCIE2_TX_C_DP10	B94	A94	GND
P3E_CPU0_PCIE2_TX_C_DN10	B95	A95	GND
GND	B96	A96	P3E_CPU1_PCIE2_RX_DP11
GND	B97	A97	P3E_CPU1_PCIE2_RX_DN11
P3E_CPU0_PCIE2_TX_C_DP11	B98	A98	GND
P3E_CPU0_PCIE2_TX_C_DN11	B99	A99	GND
GND	B100	A100	P3E_CPU1_PCIE2_RX_DP12
GND	B101	A101	P3E_CPU1_PCIE2_RX_DN12
P3E_CPU0_PCIE2_TX_C_DP12	B102	A102	GND
P3E_CPU0_PCIE2_TX_C_DN12	B103	A103	GND
GND	B104	A104	P3E_CPU1_PCIE2_RX_DP13

GND	B105	A105	P3E_CPU1_PCIE2_RX_DN13
P3E_CPU0_PCIE2_TX_C_DP13	B106	A106	GND
P3E_CPU0_PCIE2_TX_C_DN13	B107	A107	GND
GND	B108	A108	P3E_CPU1_PCIE2_RX_DP14
GND	B109	A109	P3E_CPU1_PCIE2_RX_DN14
P3E_CPU0_PCIE2_TX_C_DP14	B110	A110	GND
P3E_CPU0_PCIE2_TX_C_DN14	B111	A111	GND
GND	B112	A112	P3E_CPU1_PCIE2_RX_DP15
GND	B113	A113	P3E_CPU1_PCIE2_RX_DN15
P3E_CPU0_PCIE2_TX_C_DP15	B114	A114	GND
P3E_CPU0_PCIE2_TX_C_DN15	B115	A115	GND

3.3.1.3 Riser 3 PINOUT Definition

Table 5. PIN definition of PCIe Riser 3

Riser 1			
Name	PIN		Name
P12V	B1	A1	GND
P12V	B2	A2	P12V
P12V	B3	A3	P12V
GND	B4	A4	P12V
P3V3	B5	A5	GND
P3V3	B6	A6	P3V3
P3V3	B7	A7	P3V3
P3V3	B8	A8	P3V3
GND	B9	A9	P3V3
P3V3_AUX	B10	A10	P3V3
IRQ_LVC3_WAKE_N	B11	A11	GND
P12V_STBY	B12	A12	RST_PERST0_N
SMB_PCI_3V3SB_CLK	B13	A13	SLOT1_PRESENT_N
SM B_PCI_3V3SB_DAT_SLOT1	B14	A14	FM_RISER1_CFG0
GND	B15	A15	FM_RISER1_CFG1
CLK_100M_PE1_DP	B16	A16	GND
CLK_100M_PE1_DN	B17	A17	CLK_100M_PE2_DP
GND	B18	A18	CLK_100M_PE2_DN
CLK_100M_PE3_DP	B19	A19	GND
CLK_100M_PE3_DN	B20	A20	P3E_CPU1_PCIE3_RX_DP7
GND	B21	A21	P3E_CPU1_PCIE3_RX_DN7
P3E_CPU1_PCIE3_TX_C_DP7	B22	A22	GND
P3E_CPU1_PCIE3_TX_C_DN7	B23	A23	GND
GND	B24	A24	P3E_CPU1_PCIE3_RX_DP6
GND	B25	A25	P3E_CPU1_PCIE3_RX_DN6
P3E_CPU1_PCIE3_TX_C_DP6	B26	A26	GND
P3E_CPU1_PCIE3_TX_C_DN6	B27	A27	GND
GND	B28	A28	P3E_CPU1_PCIE3_RX_DP5
GND	B29	A29	P3E_CPU1_PCIE3_RX_DN5
P3E_CPU1_PCIE3_TX_C_DP5	B30	A30	GND

P3E_CPU1_PCIE3_TX_C_DN5	B31	A31	GND
GND	B32	A32	P3E_CPU1_PCIE3_RX_DP4
GND	B33	A33	P3E_CPU1_PCIE3_RX_DN4
P3E_CPU1_PCIE3_TX_C_DP4	B34	A34	GND
P3E_CPU1_PCIE3_TX_C_DN4	B35	A35	GND
GND	B36	A36	P3E_CPU1_PCIE3_RX_DP3
GND	B37	A37	P3E_CPU1_PCIE3_RX_DN3
P3E_CPU1_PCIE3_TX_C_DP3	B38	A38	GND
P3E_CPU1_PCIE3_TX_C_DN6	B39	A39	GND
GND	B40	A40	P3E_CPU1_PCIE3_RX_DP2
GND	B41	A41	P3E_CPU1_PCIE3_RX_DN2
P3E_CPU1_PCIE3_TX_C_DP2	B42	A42	GND
P3E_CPU1_PCIE3_TX_C_DN2	B43	A43	GND
GND	B44	A44	P3E_CPU1_PCIE3_RX_DP1
GND	B45	A45	P3E_CPU1_PCIE3_RX_DN1
P3E_CPU1_PCIE3_TX_C_DP1	B46	A46	GND
P3E_CPU1_PCIE3_TX_C_DN1	B47	A47	GND
GND	B48	A48	P3E_CPU1_PCIE3_RX_DP0
GND	B49	A49	P3E_CPU1_PCIE3_RX_DN0
P3E_CPU1_PCIE3_TX_C_DP0	B50	A50	GND
P3E_CPU1_PCIE3_TX_C_DN0	B51	A51	GND
GND	B52	A52	P3E_CPU0_PCIE2_RX_DP15
GND	B53	A53	P3E_CPU0_PCIE2_RX_DN15
P3E_CPU0_PCIE2_TX_C_DP15	B54	A54	GND
P3E_CPU0_PCIE2_TX_C_DN15	B55	A55	GND
GND	B56	A56	P3E_CPU0_PCIE2_RX_DP14
GND	B57	A57	P3E_CPU0_PCIE2_RX_DN14
P3E_CPU0_PCIE2_TX_C_DP14	B58	A58	GND
P3E_CPU0_PCIE2_TX_C_DN14	B59	A59	GND
GND	B60	A60	P3E_CPU0_PCIE2_RX_DP13
GND	B61	A61	P3E_CPU0_PCIE2_RX_DN13
P3E_CPU0_PCIE2_TX_C_DP13	B62	A62	GND
P3E_CPU0_PCIE2_TX_C_DN13	B63	A63	GND
GND	B64	A64	P3E_CPU0_PCIE2_RX_DP12
GND	B65	A65	P3E_CPU0_PCIE2_RX_DN12
P3E_CPU0_PCIE2_TX_C_DP12	B66	A66	GND
P3E_CPU0_PCIE2_TX_C_DN12	B67	A67	GND

GND	B68	A68	P3E_CPU0_PCIE2_RX_DP11
GND	B69	A69	P3E_CPU0_PCIE2_RX_DN11
P3E_CPU0_PCIE2_TX_C_DP11	B70	A70	GND
P3E_CPU0_PCIE2_TX_C_DN11	B71	A71	GND
GND	B72	A72	P3E_CPU0_PCIE2_RX_DP10
GND	B73	A73	P3E_CPU0_PCIE2_RX_DN10
P3E_CPU0_PCIE2_TX_C_DP10	B74	A74	GND
P3E_CPU0_PCIE2_TX_C_DN10	B75	A75	GND
GND	B76	A76	P3E_CPU0_PCIE2_RX_DP9
GND	B77	A77	P3E_CPU0_PCIE2_RX_DN9
P3E_CPU0_PCIE2_TX_C_DP9	B78	A78	GND
P3E_CPU0_PCIE2_TX_C_DN9	B79	A79	GND
GND	B80	A80	P3E_CPU0_PCIE2_RX_DP8
GND	B81	A81	P3E_CPU0_PCIE2_RX_DN8
P3E_CPU0_PCIE2_TX_C_DP8	B82	A82	GND
P3E_CPU0_PCIE2_TX_C_DN8	B83	A83	GND
GND	B84	A84	P3E_CPU0_PCIE2_RX_DP7
GND	B85	A85	P3E_CPU0_PCIE2_RX_DN7
P3E_CPU0_PCIE2_TX_C_DP7	B86	A86	GND
P3E_CPU0_PCIE2_TX_C_DN7	B87	A87	GND
GND	B88	A88	P3E_CPU0_PCIE2_RX_DP6
GND	B89	A89	P3E_CPU0_PCIE2_RX_DN6
P3E_CPU0_PCIE2_TX_C_DP6	B90	A90	GND
P3E_CPU0_PCIE2_TX_C_DN6	B91	A91	GND
GND	B92	A92	P3E_CPU0_PCIE2_RX_DP5
GND	B93	A93	P3E_CPU0_PCIE2_RX_DN5
P3E_CPU0_PCIE2_TX_C_DP5	B94	A94	GND
P3E_CPU0_PCIE2_TX_C_DN5	B95	A95	GND
GND	B96	A96	P3E_CPU0_PCIE2_RX_DP4
GND	B97	A97	P3E_CPU0_PCIE2_RX_DN4
P3E_CPU0_PCIE2_TX_C_DP4	B98	A98	GND
P3E_CPU0_PCIE2_TX_C_DN4	B99	A99	GND
GND	B100	A100	P3E_CPU0_PCIE2_RX_DP3
GND	B101	A101	P3E_CPU0_PCIE2_RX_DN3
P3E_CPU0_PCIE2_TX_C_DP3	B102	A102	GND
P3E_CPU0_PCIE2_TX_C_DN3	B103	A103	GND
GND	B104	A104	P3E_CPU0_PCIE2_RX_DP2

GND	B105	A105	P3E_CPU0_PCIE2_RX_DN2
P3E_CPU0_PCIE2_TX_C_DP2	B106	A106	GND
P3E_CPU0_PCIE2_TX_C_DN2	B107	A107	GND
GND	B108	A108	P3E_CPU0_PCIE2_RX_DP1
GND	B109	A109	P3E_CPU0_PCIE2_RX_DN1
P3E_CPU0_PCIE2_TX_C_DP1	B110	A110	GND
P3E_CPU0_PCIE2_TX_C_DN1	B111	A111	GND
GND	B112	A112	P3E_CPU0_PCIE2_RX_DP0
GND	B113	A113	P3E_CPU0_PCIE2_RX_DN0
P3E_CPU0_PCIE2_TX_C_DP0	B114	A114	GND
P3E_CPU0_PCIE2_TX_C_DN0	B115	A115	GND

3.3.1.4 Riser 4 PINOUT Definition (Mezz Slot)

Table 6. PIN definition of PCIe Riser 4

Riser 4			
Name	PIN		Name
P12V	1	2	P12V
P12V	3	4	P12V
P12V	5	6	P12V
P12V	7	8	GND
GND	9	10	P3V3
P3V3	11	12	P3V3
P3V3	13	14	P3V3
OCP_SAS_MEZZ_SLOT1_PRSNT_R_N	15	16	RST_PCIE_CPU0_PERST_N
P3V3_AUX	17	18	SMB_SAS_MEZZ_3V3AUX_REP_SCL
IRQ_LVC3_WAKE_N	19	20	SMB_SAS_MEZZ_3V3AUX_REP_SDA
CPU0_SAS_MEZZ_TYPE_ID0	21	22	GND
OCP_SAS_MEZZ_SLOT2_PRSNT_R_N	23	24	CLK_100M_SAS_MEZZ_DP
GND	25	26	CLK_100M_ SAS_MEZZ_DN
P3E_CPU0_PE3_TX_C_DP15	27	28	GND
P3E_CPU0_PE3_TX_C_DN15	29	30	GND
GND	31	32	P3E_CPU0_PE3_RX_C_DP15
GND	33	34	P3E_CPU0_PE3_RX_C_DN15
P3E_CPU0_PE3_TX_C_DP14	35	36	GND
P3E_CPU0_PE3_TX_C_DN14	37	38	GND
GND	39	40	P3E_CPU0_PE3_RX_C_DP14
GND	41	42	P3E_CPU0_PE3_RX_C_DN14
P3E_CPU0_PE3_TX_C_DP13	43	44	GND
P3E_CPU0_PE3_TX_C_DN13	45	46	GND
GND	47	48	P3E_CPU0_PE3_RX_C_DP13
GND	49	50	P3E_CPU0_PE3_RX_C_DN13
P3E_CPU0_PE3_TX_C_DP12	51	52	GND
P3E_CPU0_PE3_TX_C_DN12	53	54	GND
GND	55	56	P3E_CPU0_PE3_RX_C_DP12
GND	57	58	P3E_CPU0_PE3_RX_C_DN12
P3E_CPU0_PE3_TX_C_DP11	59	60	GND

P3E_CPU0_PE3_TX_C_DN11	61	62	GND
GND	63	64	OCP_SAS_MEZZA_PRSNT_R_N
CPU0_SAS_MEZZ_TYPE_ID1	65	66	GND
GND	67	68	P3E_CPU0_PE3_RX_C_DP11
GND	69	70	P3E_CPU0_PE3_RX_C_DN11
P3E_CPU0_PE3_TX_C_DP10	71	72	GND
P3E_CPU0_PE3_TX_C_DN10	73	74	GND
GND	75	76	P3E_CPU0_PE3_RX_C_DP10
GND	77	78	P3E_CPU0_PE3_RX_C_DN10
P3E_CPU0_PE3_TX_C_DP9	79	80	GND
P3E_CPU0_PE3_TX_C_DN9	81	82	GND
GND	83	84	P3E_CPU0_PE3_RX_C_DP9
GND	85	86	P3E_CPU0_PE3_RX_C_DN9
P3E_CPU0_PE3_TX_C_DP8	87	88	GND
P3E_CPU0_PE3_TX_C_DN8	89	90	GND
GND	91	92	P3E_CPU0_PE3_RX_C_DP8
GND	93	94	P3E_CPU0_PE3_RX_C_DN8
P3E_CPU0_PE3_TX_C_DP7	95	96	GND
P3E_CPU0_PE3_TX_C_DN7	97	98	GND
GND	99	100	P3E_CPU0_PE3_RX_C_DP7
GND	101	102	P3E_CPU0_PE3_RX_C_DN7
P3E_CPU0_PE3_TX_C_DP6	103	104	GND
P3E_CPU0_PE3_TX_C_DN6	105	106	GND
GND	107	108	P3E_CPU0_PE3_RX_C_DP6
GND	109	110	P3E_CPU0_PE3_RX_C_DN6
P3E_CPU0_PE3_TX_C_DP5	111	112	GND
P3E_CPU0_PE3_TX_C_DN5	113	114	GND
GND	115	116	P3E_CPU0_PE3_RX_C_DP5
GND	117	118	P3E_CPU0_PE3_RX_C_DN5
P3E_CPU0_PE3_TX_C_DP4	119	120	GND
P3E_CPU0_PE3_TX_C_DN4	121	122	GND
GND	123	124	P3E_CPU0_PE3_RX_C_DP4
GND	125	126	P3E_CPU0_PE3_RX_C_DN4
P3E_CPU0_PE3_TX_C_DP3	127	128	GND
P3E_CPU0_PE3_TX_C_DN3	129	130	GND
GND	131	132	P3E_CPU0_PE3_RX_C_DP3
GND	133	134	P3E_CPU0_PE3_RX_C_DN3

P3E_CPU0_PE3_TX_C_DP2	135	136	GND
P3E_CPU0_PE3_TX_C_DN2	137	138	GND
GND	139	140	P3E_CPU0_PE3_RX_C_DP2
GND	141	142	P3E_CPU0_PE3_RX_C_DN2
P3E_CPU0_PE3_TX_C_DP1	143	144	GND
P3E_CPU0_PE3_TX_C_DN1	145	146	GND
GND	147	148	P3E_CPU0_PE3_RX_C_DP1
GND	149	150	P3E_CPU0_PE3_RX_C_DN1
P3E_CPU0_PE3_TX_C_DP0	151	152	GND
P3E_CPU0_PE3_TX_C_DN0	153	154	GND
GND	155	156	P3E_CPU0_PE3_RX_C_DP0
CLK_100M_SAS_MEZZ1_DP	157	158	P3E_CPU0_PE3_RX_C_DN0
CLK_100M_SAS_MEZZ1_DN	159	160	GND

3.3.1.5 OCP MEZZ PINOUT Definition

Table 7. PIN definition of PCIe OCP Mezz connector

OCP Mezz Conn A			
PIN	Name	PIN	Name
61	P12V	1	MEZZ_PRSNT1_N
62	P12V	2	P5V_AUX
63	P12V	3	P5V_AUX
64	GND	4	P5V_AUX
65	GND	5	GND
66	P3V3_AUX	6	GND
67	GND	7	P3V3_AUX
68	GND	8	GND
69	P3V3	9	GND
70	P3V3	10	P3V3
71	P3V3	11	P3V3
72	P3V3	12	P3V3
73	GND	13	P3V3
74	PU_SMB_LAN_ALERT_N_MEZZ	14	NCSI_OCP_RCSDV
75	SMB_PCI_3V3SB_CLK	15	NCSI_OCP_RCLK
76	SMB_PCI_3V3SB_DAT_MEZZ_R	16	NCSI_OCP_TXEN
77	IRQ_LVC3_WAKE_N	17	RST_PERST0_N
78	NCSI_OCP_RXER	18	TP_OCP_MEZZ_18
79	GND	19	TP_OCP_MEZZ_19
80	NCSI_OCP_TXD0	20	GND
81	NCSI_OCP_TXD1	21	GND
82	GND	22	NCSI_OCP_RXD0
83	GND	23	NCSI_OCP_RXD1
84	CLK_100M_OCP_MEZZA_DP	24	GND
85	CLK_100M_OCP_MEZZA_DN	25	GND
86	GND	26	CLK_100M_OCP_MEZZB_DP
87	GND	27	CLK_100M_OCP_MEZZB_DN
88	P3E_CPU0_PCIE3_TX_C_DP7	28	GND
89	P3E_CPU0_PCIE3_TX_C_DN7	29	GND
90	GND	30	P3E_CPU0_PCIE3_RX_DP7
91	GND	31	P3E_CPU0_PCIE3_RX_DN7

92	P3E_CPU0_PCIE3_TX_C_DP6	32	GND
93	P3E_CPU0_PCIE3_TX_C_DN6	33	GND
94	GND	34	P3E_CPU0_PCIE3_RX_DP6
95	GND	35	P3E_CPU0_PCIE3_RX_DN6
96	P3E_CPU0_PCIE3_TX_C_DP5	36	GND
97	P3E_CPU0_PCIE3_TX_C_DN5	37	GND
98	GND	38	P3E_CPU0_PCIE3_RX_DP5
99	GND	39	P3E_CPU0_PCIE3_RX_DN5
100	P3E_CPU0_PCIE3_TX_C_DP4	40	GND
101	P3E_CPU0_PCIE3_TX_C_DN4	41	GND
102	GND	42	P3E_CPU0_PCIE3_RX_DP4
103	GND	43	P3E_CPU0_PCIE3_RX_DN4
104	P3E_CPU0_PCIE3_TX_C_DP3	44	GND
105	P3E_CPU0_PCIE3_TX_C_DN3	45	GND
106	GND	46	P3E_CPU0_PCIE3_RX_DP3
107	GND	47	P3E_CPU0_PCIE3_RX_DN3
108	P3E_CPU0_PCIE3_TX_C_DP2	48	GND
109	P3E_CPU0_PCIE3_TX_C_DN2	49	GND
110	GND	50	P3E_CPU0_PCIE3_RX_DP2
111	GND	51	P3E_CPU0_PCIE3_RX_DN2
112	P3E_CPU0_PCIE3_TX_C_DP1	52	GND
113	P3E_CPU0_PCIE3_TX_C_DN1	53	GND
114	GND	54	P3E_CPU0_PCIE3_RX_DP1
115	GND	55	P3E_CPU0_PCIE3_RX_DN1
116	P3E_CPU0_PCIE3_TX_C_DP0	56	GND
117	P3E_CPU0_PCIE3_TX_C_DN0	57	GND
118	GND	58	P3E_CPU0_PCIE3_RX_DP0
119	GND	59	P3E_CPU0_PCIE3_RX_DN0
120	OCP_MEZZA_PRSNT_N	60	GND

OCP Mezz Conn B			
PIN	Name	PIN	Name
41	P12V_AUX	1	OCP_2_PRSNTB1_N
42	P12V_AUX	2	GND
43	RSVD	3	P3E_CPU0_PE2_NIC_RX_C_DN _DP8
44	GND	4	P3E_CPU0_PE2_NIC_RX_C_DP _DP8
45	P3E_CPU0_PE2_NIC_TX_C_DP _DP8	5	GND
46	P3E_CPU0_PE2_NIC_TX_C_DN _DP8	6	GND
47	GND	7	P3E_CPU0_PE2_NIC_RX_C_DN _DP9
48	GND	8	P3E_CPU0_PE2_NIC_RX_C_DP _DP9
49	P3E_CPU0_PE2_NIC_TX_C_DP _DP9	9	GND
50	P3E_CPU0_PE2_NIC_TX_C_DN _DP9	10	GND
51	GND	11	P3E_CPU0_PE2_NIC_RX_C_DN _DP10
52	GND	12	P3E_CPU0_PE2_NIC_RX_C_DP _DP10
53	P3E_CPU0_PE2_NIC_TX_C_DP _DP10	13	GND
54	P3E_CPU0_PE2_NIC_TX_C_DN _DP10	14	GND
55	GND	15	P3E_CPU0_PE2_NIC_RX_C_DN _DP11
56	GND	16	P3E_CPU0_PE2_NIC_RX_C_DP _DP11
57	P3E_CPU0_PE2_NIC_TX_C_DP _DP11	17	GND
58	P3E_CPU0_PE2_NIC_TX_C_DN_DP11	18	GND
59	GND	19	P3E_CPU0_PE2_NIC_RX_C_DN _DP12
60	GND	20	P3E_CPU0_PE2_NIC_RX_C_DP _DP12
61	P3E_CPU0_PE2_NIC_TX_C_DP _DP12	21	GND
62	P3E_CPU0_PE2_NIC_TX_C_DN _DP12	22	GND
63	GND	23	P3E_CPU0_PE2_NIC_RX_C_DN _DP13
64	GND	24	P3E_CPU0_PE2_NIC_RX_C_DP _DP13
65	P3E_CPU0_PE2_NIC_TX_C_DP _DP13	25	GND
66	P3E_CPU0_PE2_NIC_TX_C_DN_DP13	26	GND
67	GND	27	P3E_CPU0_PE2_NIC_RX_C_DN _DP14
68	GND	28	P3E_CPU0_PE2_NIC_RX_C_DP _DP14
69	P3E_CPU0_PE2_NIC_TX_C_DP _DP14	29	GND
70	P3E_CPU0_PE2_NIC_TX_C_DN_DP14	30	GND
71	GND	31	P3E_CPU0_PE2_NIC_RX_C_DN _DP15
72	GND	32	P3E_CPU0_PE2_NIC_RX_C_DP _DP15
73	P3E_CPU0_PE2_NIC_TX_C_DP _DP15	33	GND
74	P3E_CPU0_PE2_NIC_TX_C_DN _DP15	34	GND

75	GND	35	CLK_100M_DB1200_NIC_MEZZ_3_R_DP
76	GND	36	CLK_100M_DB1200_NIC_MEZZ_3_R_DN
77	CLK_100M_DB1200_NIC_MEZZ_4_R_DP	37	GND
78	CLK_100M_DB1200_NIC_MEZZ_4_R_DN	38	RST_OCP_2_DEVICE1_N
79	GND	39	RST_OCP_2_DEVICE2_N
80	OCP_NIC_MEZZB_PRSNT_R_N	40	RST_OCP_2_DEVICE3_N

OCP Mezz Conn C			
PIN	Name	PIN	Name
33	P12V_AUX	1	SMB_PHY_FRU_3V3AUX_SCL
34	P12V_AUX	2	SMB_PHY_FRU_3V3AUX_SDA
35	P12V_AUX	3	EXT_MDIO_I2C_SEL_R
36	RSVD	4	GND
37	FM_LVC3_GBE_SDP0_R	5	KR_PCH_P2_TX_DP
38	FM_LVC3_GBE_SDP1_R	6	KR_PCH_P2_TX_DN
39	GND	7	GND
40	KR_PCH_P0_TX_DP	8	LED_GBE_1_LINK_R
41	KR_PCH_P0_TX_DN	9	LED_GBE_1_ACT_R
42	GND	10	GND
43	LED_GBE_0_LINK_R	11	KR_PCH_P3_TX_DP
44	LED_GBE_0_ACT_R	12	KR_PCH_P3_TX_DN
45	GND	13	GND
46	KR_PCH_P1_TX_DP	14	LED_GBE_2_LINK_R
47	KR_PCH_P1_TX_DN	15	LED_GBE_2_ACT_R
48	GND	16	GND
49	KR_MDC_0	17	KR_PCH_P2_RX_DP
50	KR_MDIO_0	18	KR_PCH_P2_RX_DN
51	GND	19	GND
52	KR_PCH_P0_RX_DP	20	SMB_SFI_SCL_0
53	KR_PCH_P0_RX_DN	21	SMB_SFI_SDA_0
54	GND	22	GND
55	LED_GBE_3_LINK_R	23	KR_PCH_P3_RX_DP
56	LED_GBE_3_ACT_R	24	KR_PCH_P3_RX_DN
57	GND	25	GND
58	KR_PCH_P1_RX_DP	26	SMB_SFI_SCL_1
59	KR_PCH_P1_RX_DN	27	SMB_SFI_SDA_1
60	GND	28	GND
61	SMB_SFI_SCL_2	29	SMB_SFI_SCL_3
62	SMB_SFI_SDA_2	30	SMB_SFI_SDA_3
63	GND	31	FM_LVC3_GBE_SDP2_R
64	OCP_NIC_MEZZC_PRSNT_N	32	FM_LVC3_GBE_SDP3_R

3.4 Front control panel

The product has front control panel. Because of the limited space, only the following functions will be available.

Table 8. Pin Out of Front control panel connector

Front Panel Connector			
Signal Name	PIN		Signal Name
3VSB (Power LED Anode)	1	2	3VSB (Front Panel Power)
Key	3	4	5VSB (ID LEF Anode)
FP_PWR_LED_N	5	6	FP_ID_LED_N
3.3V (HDD Activity LED Anode)	7	8	LED_STATUS_GREEN_N
LED_HDD_ACTIVITY_N	9	10	LED_STATUS_AMBER_N
FP_PWR_BTN_N	11	12	LED_NIC1_ACT_N
GND (Power Button GND)	13	14	LED_NIC1_LINK_N
RST_BMC_RST_BTN_N	15	16	SMB_SDA
GND (Reset GND)	17	18	SMB_SCL
FP_ID_BTN	19	20	FM_INTRUDER_N
Pull-up (1-wire Temp Sensor)	21	22	LED_NIC2_ACT_N
FP_NMI_BTN_N	23	24	LED_NIC2_LINK_N

Table 9. LED behavior of 1U HDD system

Mark	Name	Color	Condition	Behavior	Voltage	Owner
	**Power LED**	**Blue**	**On**	**S0 System Power On**	**5VSB**	**BMC**
			OFF	**S5 System Power Off**		
	**ID LED**	**Blue**	**Blinking**	**Unit selected for Identification**	**5VSB**	**BMC**
			OFF	**No Identificaiton requested**		
	**Fault LED**	**Amber**	**Blinking**	**Critical Failure**	**5VSB**	**BMC**
				Non Critical Failure:		

			OFF	**SEL Cleared**		
				Last pending warning or Error has been deleted		

3.4.1 Rear Panel LED Function and Behavior

3.4.1.1 Rear ID LED Function and Behavior

Table 4-3 LED behavior of 1U HDD system

Name	Color	Condition	Behavior
ID LED	**Blue**	**Blinking**	**Unit selected for Identification**
		OFF	**No Identificaiton requested**

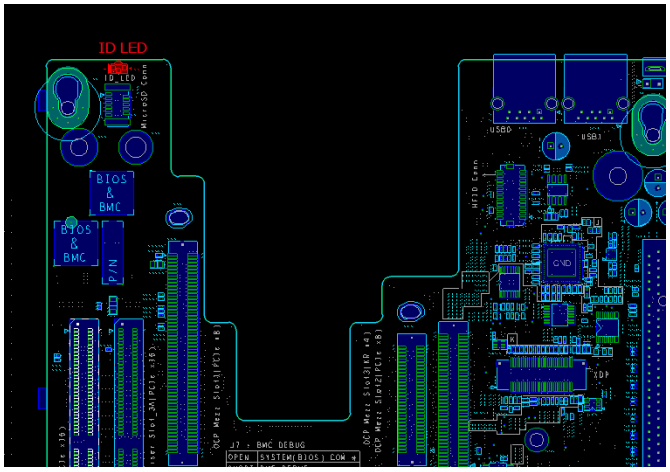


Figure 4-6 On board ID LED

3.4.1.2 Rear Delicade RJ45 MNG Function and Behavior

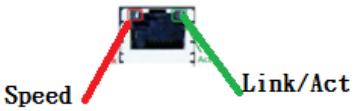
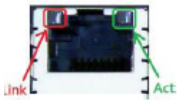


Table 4-6. MNG Delicate RJ45 LED



	Link (Left)	Activity(Right)
Unplug	Dark	Dark
1 G Link with Active	Amber	Green blinking
100M Link with Active	Green	Green blinking
10 M Link with Active	Dark	Green blinking

3.5 POWER SUPPLY

A couple of new power-supplies are being enabled by the power-supply team.

3.5.1 LED Behavior of POWER SUPPLY

Table 10 LED Behavior of PSU

LED TABLE	
Condition: Standby Mode / Single unit	
Status	**LED**
normal	**Green**
Fan lock (15 sec)	Amber

	LED Status
No AC input	OFF
Standby	Green; Blink at 0.5Hz
12V ON	Green; Solid
12V OC Fault	Amber; Solid
12V OV	Amber; Solid
12V UV	Amber; Solid
12Vstby OC	OFF
12Vstby OV	OFF
12Vstby UV > 9.5V	OFF
12Vstby UV < 9.5V	Unpredictable
OT WARN	Green; Solid
OT FAULT	Amber; Solid
FAN WARN	Green; Solid
FAN Failed	Amber; Solid
Cold Redundancy Standby	Green; Blink at 2Hz
Input UVW	Green; Solid
Input UVP	OFF
Input OVP	Amber; Solid

3.5.2 Power supply PINOUT

Table 12 PIN definition of Power Supply 0

Power Supply 0			
Name	PIN		Name
P12V	64	1	P12V
P12V	63	2	P12V
P12V	62	3	P12V
P12V	61	4	P12V
P12V	60	5	P12V
P12V	59	6	P12V
P12V	58	7	P12V
P12V	57	8	P12V
P12V	56	9	P12V
P12V	55	10	P12V
P12V	54	11	P12V
P12V	53	12	P12V
GND	52	13	GND
GND	51	14	GND
GND	50	15	GND
GND	49	16	GND
GND	48	17	GND
GND	47	18	GND
GND	46	19	GND
GND	45	20	GND
GND	44	21	GND
GND	43	22	GND
GND	42	23	GND
GND	41	24	GND
PSU_REMOTE_SENSE_P	40	25	TP_TACH
P12V_STBY	39	26	PSU_REMOTE_SENSE_N
PSU_A0	38	27	TP_VIN_GOOD
PWROK0	37	28	CSHARE
GND	36	29	FM_PS_EN_PSU_N
SMB_3V3SB_PMBUS_CLK	35	30	PS_KILL_0

PSU_PRESENT0_N	34	31	RESET_PS_0
SMB_3V3SB_PMBUS_DAT	33	32	IRQ_SML1_PMBUS_ALERT_N

Table 3-22. PIN definition of Power Supply 1

Power Supply 1			
Name	PIN		Name
P12V	64	1	P12V
P12V	63	2	P12V
P12V	62	3	P12V
P12V	61	4	P12V
P12V	60	5	P12V
P12V	59	6	P12V
P12V	58	7	P12V
P12V	57	8	P12V
P12V	56	9	P12V
P12V	55	10	P12V
P12V	54	11	P12V
P12V	53	12	P12V
GND	52	13	GND
GND	51	14	GND
GND	50	15	GND
GND	49	16	GND
GND	48	17	GND
GND	47	18	GND
GND	46	19	GND
GND	45	20	GND
GND	44	21	GND
GND	43	22	GND
GND	42	23	GND
GND	41	24	GND
PSU_REMOTE_SENSE_P	40	25	TP_TACH
P12V_STBY	39	26	PSU_REMOTE_SENSE_N
PSU_A1	38	27	TP_VIN_GOOD
PWROK1	37	28	CSHARE
GND	36	29	FM_PS_EN_PSU_N
SMB_3V3SB_PMBUS_CLK	35	30	PS_KILL_1

PSU_PRESENT1_N	34	31	RESET_PS_1
SMB_3V3SB_PMBUS_DAT	33	32	IRQ_SML1_PMBUS_ALERT_N

4 Environmental Requirements

This section provides regulatory and compliance information applicable to this system.

4.1 Product Regulatory Compliance Markings

This product is marked with the following Product Certification Markings

Regulatory Compliance	Region	Marking
cULus Listing Mark	USA / Canada	
CE Mark	Europe	
FCC Marking (Class A)	USA	This device complies with Part 15 of the FCC Rules. Operation of this device is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.
ICES	Canada	CAN ICES-3 (A)/NMB-3(A)
VCCI Marking (Class A)	Japan	この装置は、クラスA情報技術装置です。この装置を家庭環境で使用すると電波妨害を引き起こすことがあります。この場合には使用者が適切な対策を講ずるよう要求されることがあります。 VCCI-A
BSMI Certification Number & Class A Warning	Taiwan	 警告使用者： 此為甲類資訊技術設備，於居住環境使用中時，可能會造成射頻擾動，在此種情況下，使用者會被要求採取某些適當的對策。
EAC Marking	Russia	
Recycling Package Mark	Other than China	
MSIP	Korea	 A급 기기 (업무용 정보통신기기) 이 기기는 업무용으로 전자파적합등록을 한 기기이오니 판매자 또는 사용자는 이 점을 주의하시기 바라며, 만약 잘못판매 또는 구입하였을 때에는 가정용으로 교환하시기 바랍니다.
RCM	Australia	
CCC	China	 此为A级产品，在生活环境中，该产品可能会造成无线电干扰。 在这种情况下，可能需要用户对其干扰采取切实可行的措施。

4.2 Operating environment

- Operating temperature: 5°C to 40°C (41°F to 104°F)
- Non-operating temperature: -40°C to 70°C (-40°F to 158°F)
- Operating relative humidity: 20% to 85%RH
- Non-operating relative humidity: 10% to 95%RH