SIP Design Flow

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Consume. Collaborate. Contribute.

Chip Design Flow

DESIGN STEPS

1- Architecture, IP block selection, Package Selection, Technology Selection

2- Design Entry
- IO Planning
- RTL Design and Verification
- Schematic Capture
- Component Placement

3- Chip Layout / Routing / Package Layout

4- Verification
- Functional
- Electrical
- Thermal

5- Send to Manufacturing

MANUFACTURING STEPS

1- Chip Fab , Wafer Probe Test

2- Package Fabrication

3- Assembly

4- System Level Test

PCB Design Flow

DESIGN STEPS

1- Architecture, Component selection, Package Selection

2- Design Entry
IO Planning, Initial Placement
Schematic Capture
(HDL/Orcad/Altium/Pads/Allegro)
Placement Optimization

3- PCB Routing and Layout

4- Verification (skip for cheap board)
Functional
Electrical (PI/SI)
Thermal

5- Send to Manufacturing

MANUFACTURING STEPS

1- Substrate Fab , eTest

2- Tooling

3- Assembly

4- System Level Test

SIP Design Flow

DESIGN STEPS

1- Architecture, Component selection, Package Selection

2- Design Entry
- IO Planning, Initial Placement
- RTL Design and Verification
- Schematic Capture
- Placement Optimization

3- Package Routing and Layout (SiP, APD)

4- Verification
- Functional
- Electrical (PI/SI)
- Thermal

5- Send to Manufacturing

MANUFACTURING STEPS

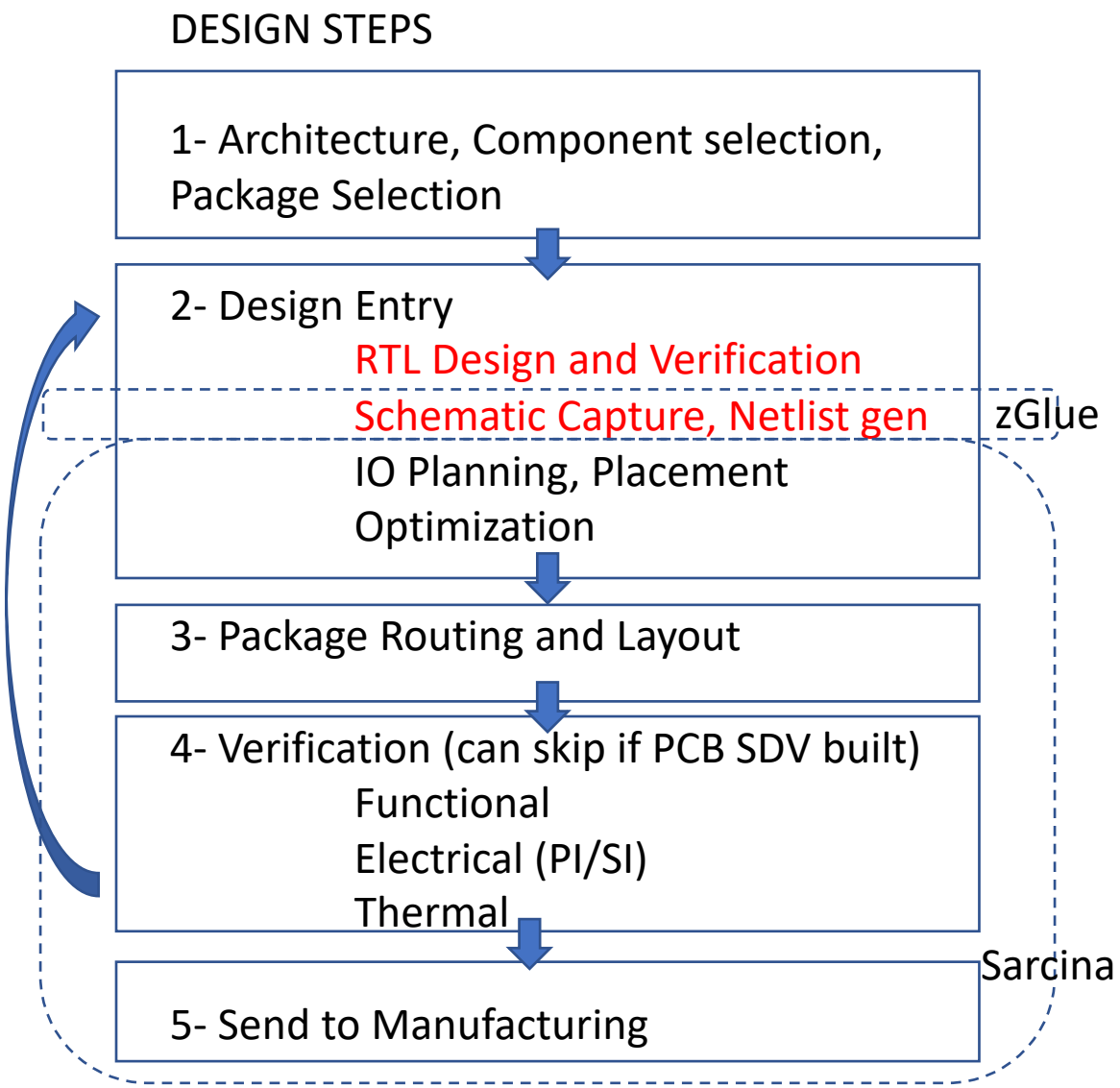
1- Substrate Fab , eTest

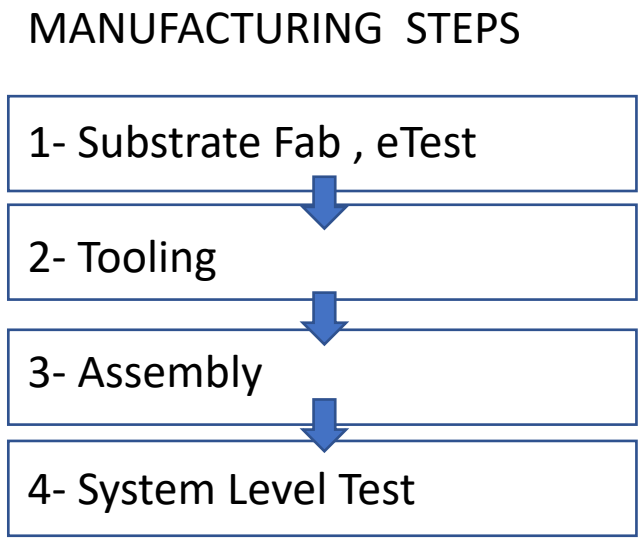
2- Tooling

3- Assembly

4- System Level Test

PoC Package Design Flow





PoC SW Dev Vechicle PCB Design Flow