OPEN

Compute Project



# AMD Open CS 1.0 Micro-Server Card Hardware v1.0

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# 1 Revision History

| Date | Revision | Description |
|---|---|---|
| April 2014 | 1.0 | Initial Release |

# 2 Scope

This document defines the technical specifications for the AMD Open CS 1.0 Micro-server Card that will be used in Open Compute Project servers.

**Note-1:** This document was based on the *Open Compute Project Micro-server Card Specification, v0.7*, and is subject to change

# 3 Contents

# 4 Overview

This document describes the " AMD Open CS 1.0 Micro-server Card," hereafter referred to as Open CS 1.0.

Open CS 1.0 is a common slot card that is optimized for cost and power, and designed to the *Open Compute Project Micro-server Card Specification, v0.7*. The card was designed to “Option 3” of the v0.7 specification. Please refer to the specification for further details. Schematics and layout files will be included in this contribution. BIOS files will not be included in the contribution.

## 4.1 License

## 4.2 CAD Models

CAD models as fully set forth in this specification will be made available on the OCP Server page at http://www.opencompute.org/wiki/Motherboard/SpecsAndDesigns.

# 5 Motherboard Features

The Open CS 1.0 design supports the following feature set. A general description of the Open CS 1.0 design is documented below.

| Component | Function |
|---|---|
| Processor | • One AMD SP1 package per board<br>• Support for AMD's "Seattle" processor<br>• Supports Infrastructure Group A and B: TDPs are TBD |
| Memory | • 2 ECC SO-DIMMs per channel (total of 4 ECC SO-DIMMs per card)<br>• Support up to 1866MHz for 1 DIMM and 1600MHz for 2 DIMMs per channel<br>• Supports DDR3L (1.35V)<br>• Targeted configuration is 64GB, 1.35V, ECC SO-DIMM DDR3, 1333 MHz |
| I/O | • SoC with integrated Southbridge functions<br>• SATA 3.0 ports<br>  ○ 1 iSSD<br>  ○ 1 mSATA connector<br>  ○ 6 SATA to card interface<br>• x8 PCI Express® Gen 3 to card interface |
| Video | No embedded support. |
| Networking | • Integrated dual port 10G-KR<br>• 1 10G-KR port to card interface |
| System Management | See Chapter 7 |
| Board Dimensions | 73.8mm x 210mm as per the *Open Compute Project, Micro-Server Card Hardware v0.7*. |
| Layer Count | 10 layers(see Chapter 5.1) |
| Power target per MB | See Chapter 10 |

## 5.1 PCB Stackup

| 1 | | SURFACE | AIR | |
|---|---|---|---|---|
| 2 | | DIELECTRIC | SOLDERMASK | 0.0127 |
| 3 | TOP | CONDUCTOR | 1/2OZ_COPPER+PLATE | 0.0457 |
| 4 | | DIELECTRIC | FR4_P_1080_2.7 | 0.06858 |
| 5 | L2_INNER | PLANE | 1OZ_COPPER | 0.03048 |
| 6 | | DIELECTRIC | FR4_C_10 | 0.0762 |
| 7 | L3_INNER | CONDUCTOR | 1/2OZ_COPPER | 0.01524 |
| 8 | | DIELECTRIC | FR4_P_10 | 0.381 |
| 9 | L4_INNER | CONDUCTOR | 1/2OZ_COPPER | 0.01524 |
| 10 | | DIELECTRIC | FR4_C_10 | 0.0762 |
| 11 | L5_INNER | PLANE | 1OZ_COPPER | 0.03048 |
| 12 | | DIELECTRIC | FR4_P_10 | 0.0762 |
| 13 | L6_INNER | PLANE | 1OZ_COPPER | 0.0305 |
| 14 | | DIELECTRIC | FR4_C_10 | 0.0762 |
| 15 | L7_INNER | CONDUCTOR | 1/2OZ_COPPER | 0.01524 |
| 16 | | DIELECTRIC | FR4_P_10 | 0.381 |
| 17 | L8_INNER | CONDUCTOR | 1/2OZ_COPPER | 0.0152 |
| 18 | | DIELECTRIC | FR4_C_10 | 0.0762 |
| 19 | L9_INNER | PLANE | 1OZ_COPPER | 0.03048 |
| 20 | | DIELECTRIC | FR4_P_1080_2.7 | 0.0686 |
| 21 | BOTTOM | CONDUCTOR | 1/2OZ_COPPER+PLATE | 0.0457 |
| 22 | | DIELECTRIC | SOLDERMASK | 0.0127 |
| 23 | | SURFACE | AIR | |

## 5.2 Block Diagram

Figure 1 illustrates the functional block diagram for Open CS 1.0.

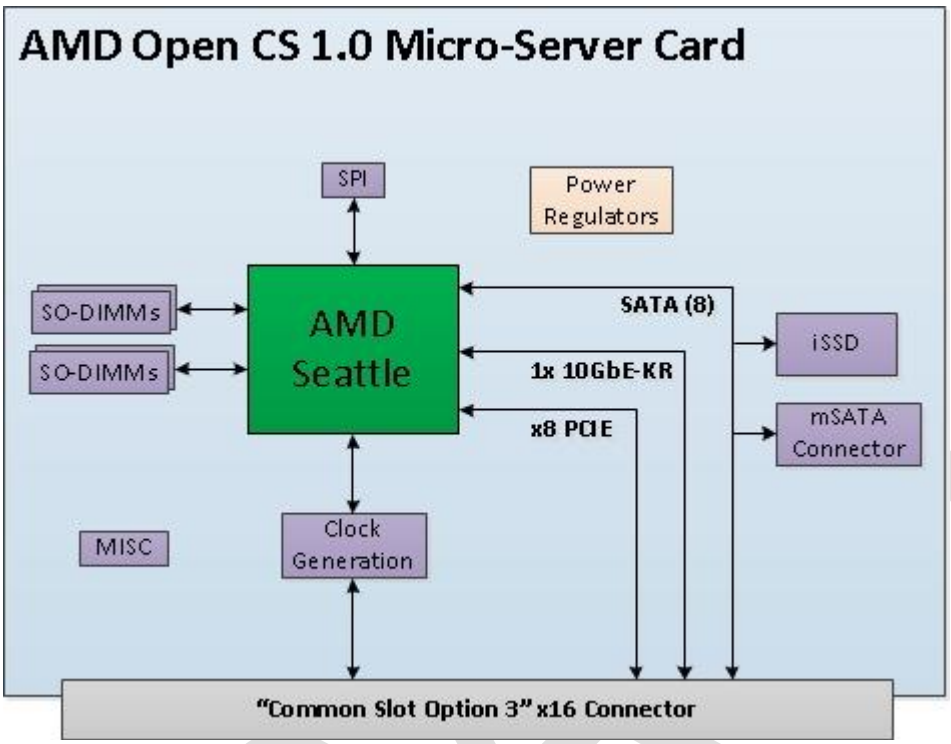


**Figure 1 Functional Block Diagram**

## 5.3 Placement and Form Factor

The Open CS 1.0 form factor is a 73.8 x 210 millimeter following the card mechanical outline info detailed in the *Open Compute Project, Micro-Server Card Hardware v0.7*. Figure 2 illustrates board placement. The placement shows the relative positions of key components, while exact dimension and position information will be determined in the future. Once released, the ODM should strictly follow the form factor, memory slot position, and mounting holes, while other components can be shifted based on preference as long as relative position is maintained.

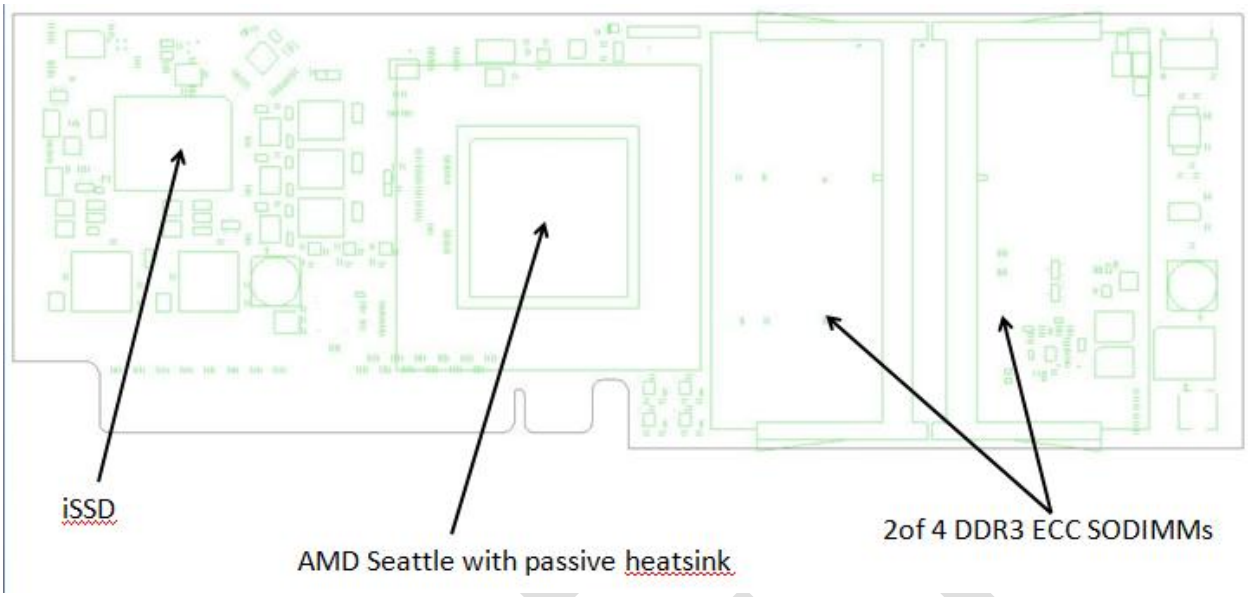


**Figure 2 AMD Motherboard Topside Component Placement**

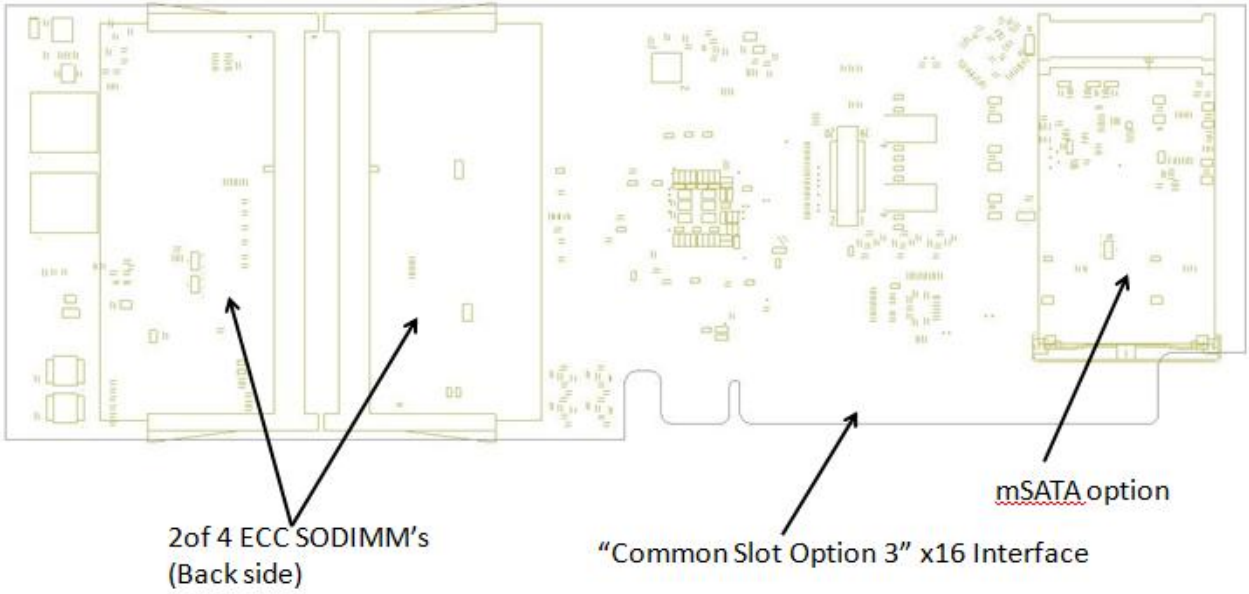


**Figure 3 AMD Motherboard Bottomside Component Placement**

## 5.4 CPU and Memory

Open CS 1.0 is designed to accommodate SP1 power bands TBD.

AMD's "Seattle" processor in the SP1 package has the following characteristic:

- 28 nm AMD Family 20h processor
- 8 or 4 ARM Cortex®-A57 cores
- Each individual core has its own TBD L1 data cache

- Dual-channel U/R-DDR3/ECC SO-DIMM memory

### 5.4.1 DDR3

It is a requirement to support 1.35V memory offerings. This still requires SPD detection by the system bios to detect the correct memory voltages; however hardware interfaces are simplified since only one voltage is supported.

Surface mount DIMM connectors are recommended for this design.

2 channels DDR3 registered memory interface on each SoC:

- 2 DDR3 slots per channel per processor (total of 4 DIMMs on the card)
- RDIMM (1.35V) and UDIMM (1.35V)
- SR, DR, and QR DIMMs
- DDR3 speeds up to 1866

## 5.5 PCIe Usage

Open CS 1.0 supports 8 lanes of PCI-Express Gen 3. All 8 lanes are routed to the card interface.

## 5.6 Integrated Peripheral Features

The AMD's "Seattle" processor supports the following integrated peripheral features:

- SATAIII ports
- SPI interface
- I2C interface (master and slave)
- Serial ports

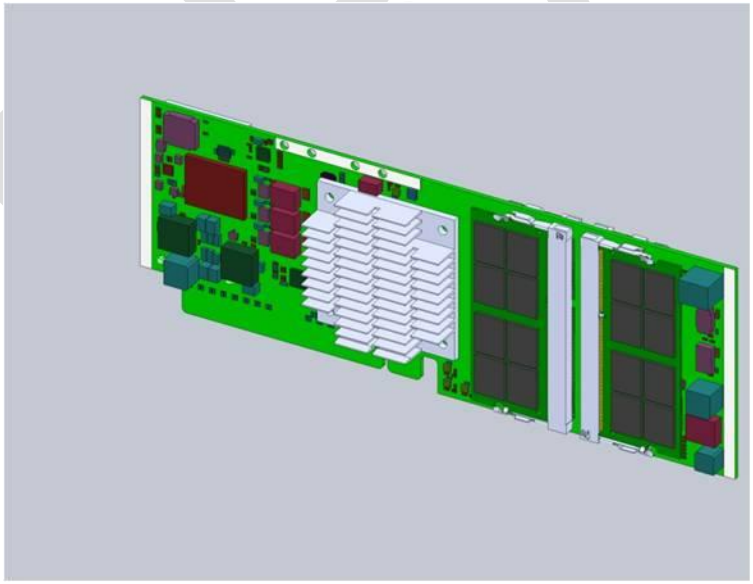

Figure 4 AMD Open CS 1.0 Micro-Server Card

The Open Platform board can fit into an Open Rack compliant chassis that will need to be developed. It can fit into future Open Compute1.0 chassis that have been designed with multiple holes punched into the base. However, it cannot fit into currently deployed Open Compute chassis because of incompatible hole patterns.

## 5.7 Heat Sink and Thermal Simulation

Open CS 1.0 supports a low profile, off the shelf heat sink from Aavid Thermalloy P/N 343627. The mounting device employs push pins to secure the heatsink to the card. The ODM must comply with all keep out zones defined by AMD.

### Thermal Simulation

Preliminary thermal simulations with a 35C ambient and 3m/s of flow should provide sufficient cooling for:

- Dual Row Implementation - a fully populated baseboard where rear row of cards are preheated and shadowed.
- Single Row Implementation - a half dense solution where only one row of cards are populated on the baseboard.

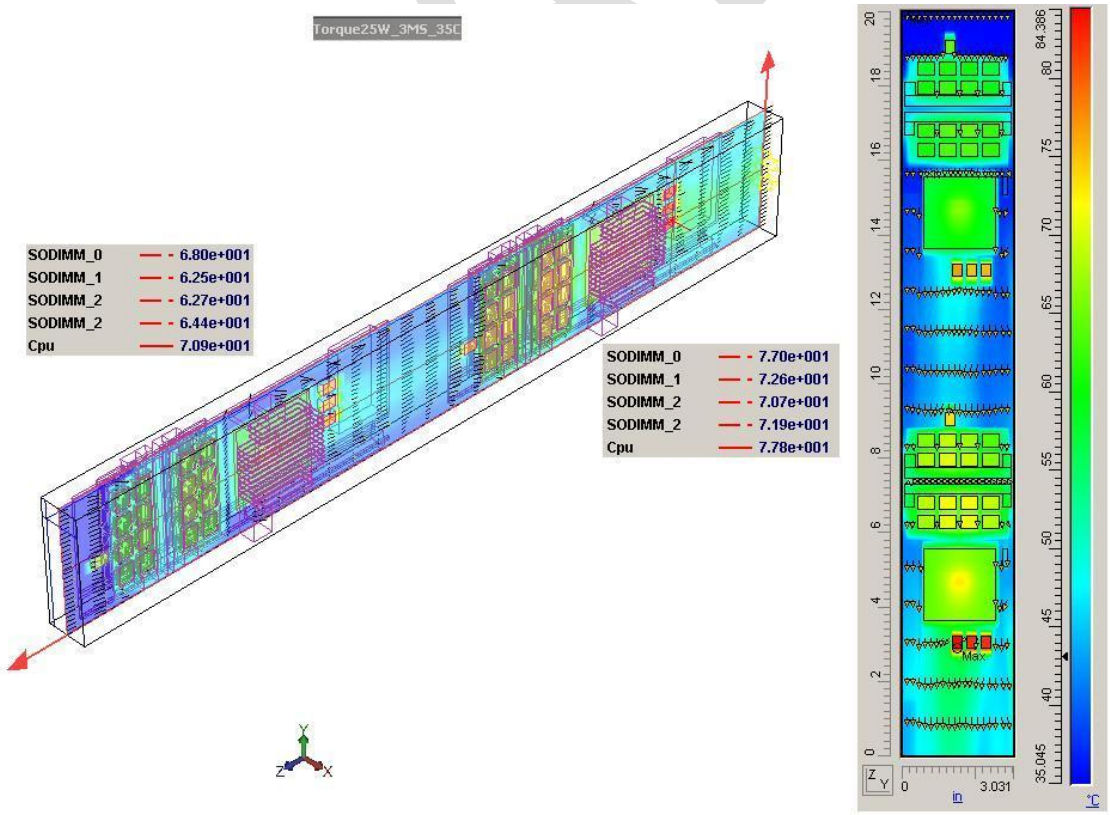


Figure 5 Dual Row Baseboard Thermal Simulation

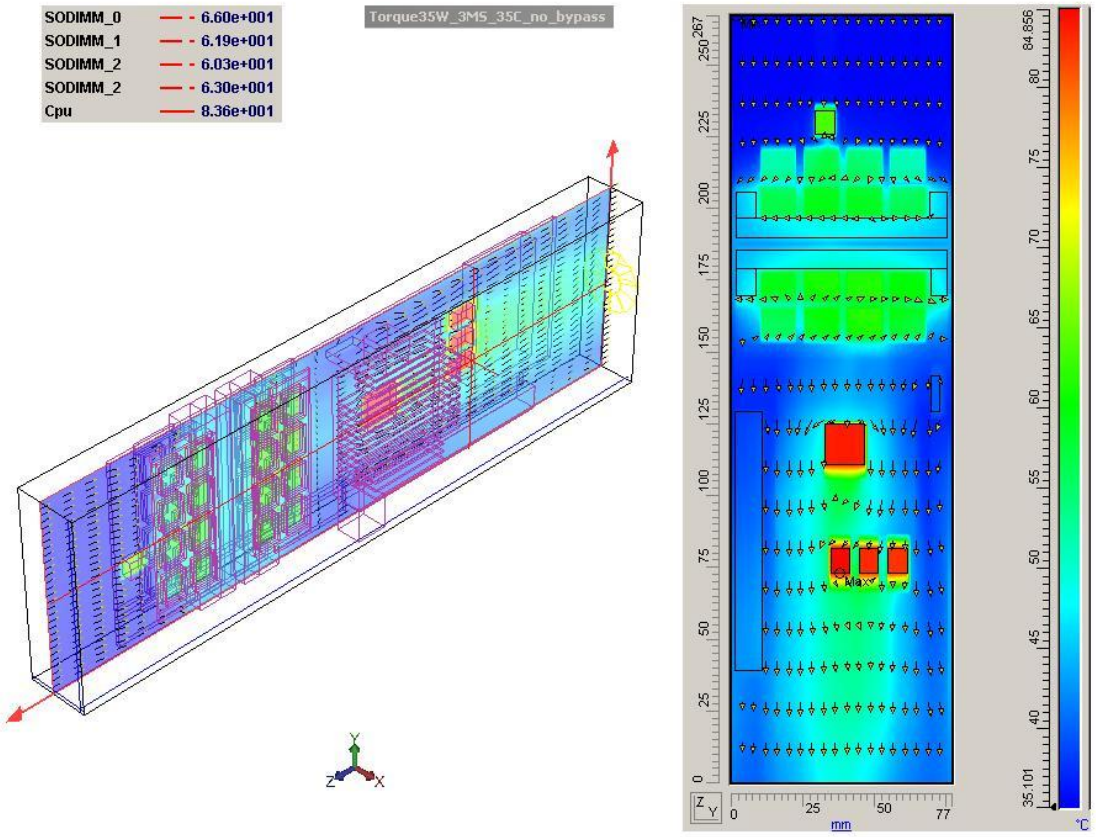


Figure 6 Single Row Baseboard Thermal Simulation

# 6 UEFI Firmware

The ODM is responsible for supplying the UEFI firmware for the card. The UEFI firmware is developed in collaboration with AMD's "Seattle" processor IBV support.

For more information, please contact AMD.

# 7 System Management

For more information, go to http://www.opencompute.org/assets/download/OpenComputeProjectOpenMachinesManagement.pdf.

## 7.1 Temperature Sensors

Per *Open Compute Project, Micro-Server Hardware v0.7*, the card should support these thermal sensors:

- One to monitor SOC temperature, retrieved through the SOC's temperature sensor interface
- SO-DIMM temperatures, retrieved from the on DIMM thermistor, if used

- Outlet temperature, retrieved through the thermistor, and located along the rear edge of the card

# 8 Power System

This chapter describes the power sub-system for the AMD Open CS 1.0 Micro-Server Card.

## 8.1 Power Budget for Open Platform Board Configurations

The Open CS 1.0 power budget fits within the allowed maximum of 60W for a x8 Card design per *Open Compute Project, Micro-Server Hardware v0.7.*

## 8.2 VRM Specifications

The SoC VRM solutions should be load line enabled and designed to fit the specified power loads only.

In addition, the voltage regulators with the following characteristics are recommended:

- Load line to minimize load step transient.
- Differential Sense for accurate voltage sensing.
- Support for high value, low ESR ceramic caps and low ripple noise.
- In general, the target for ripple from the regulator should be < 10% of the maximum allowable voltage range. This allows 90% for all other sources of noise.

### 8.2.1 Target Power Efficiencies

The following are the target power efficiencies for each given group:

- Core VR: > 91% when loaded between 30% and 90% of the full operating load
- DDR VR: > 91% when loaded between 30% and 90% of the full operating load

## 8.3 Power Sequencing

The Open CS 1.0 design should follow power sequencing requirements for the AMD Socket SP1. Specific sequencing requirements are outlined in available design guides.

## 8.4 Power Optimized Hardware Features

This section describes the high level power optimized hardware features needed for the AMD Open CS 1.0 Micro-Server Card.

### 8.4.1 Switching Regulators versus Linear Regulators

Because Open CS 1.0 is designed to maximize system power savings, careful consideration must be undertaken when designing power delivery to the various system components. There are cost and board space considerations to balance, but it is generally recommended that all voltage rails that consume more than 15W of power be implemented using more efficient switching solutions.

Specific space, cost, and efficiency tradeoffs should be carefully analyzed during the earliest stages of the design.

# 9 AMD Open CS 1.0 Micro-Server Card Interface

This section describes the Open CS 1.0 interface pinout.

## 9.1 PCI-Express Card Edge

The Open CS 1.0 design leverages a board edge connector as defined by the PCI Express Card Electromechanical Specification. Details of this edge connector are outlined in the *Open Compute Project, Micro-Server Hardware v0.7*.

## 9.2 Pin-out

Open CS 1.0 implements a x16 edge connector pinout. The lower x8 portion of the connector follows the Option 3 configuration detailed in the *Open Compute Project, Micro-Server Hardware v0.7.* The upper x8 portion of the connector implements the full x8 PCIE Express Gen 3 interface from AMD's "Seattle" processor. The x8 port can alternatively be configured as two x4 PCIE Express Gen 3 ports.

For more pinout details, please refer to the *Open Compute Project, Micro-Server Hardware v0.7* located at http://files.opencompute.org/oc/public.php?service=files&t=0ab1c41dd11111c4f3ceafc175883fcb.

The Open CS 1.0 pin-out is shown below.

| Pin Name | Side B | Side A | Pin Name |
|---|---|---|---|
| P12V | 1 | 1 | PRSNT# |
| P12V | 2 | 2 | P12V |
| P12V | 3 | 3 | P12V |
| GND | 4 | 4 | GND |
| I2C_SCL | 5 | 5 | SVR_ID0 |
| I2C_SDA | 6 | 6 | SVR_ID1 |
| GND | 7 | 7 | COM_TX |
| PWR_BTN# | 8 | 8 | COM_RX |
| PCIE1_REFCLK_P | 9 | 9 | SVR_ID2 |
| PCIE1_REFCLK_N | 10 | 10 | SVR_ID3 |
| SYS_RESET# | 11 | 11 | PCIE0_RESET# |
| I2C_ALERT# | 12 | 12 | GND |
| GND | 13 | 13 | PCIE0_REFCLK_P |
| GND | 14 | 14 | PCIE0_REFCLK_N |
| SATA5_TX_P | 15 | 15 | GND |
| SATA5_TX_N | 16 | 16 | GND |
| GND | 17 | 17 | SATA5_RX_P |
| GND | 18 | 18 | SATA5_RX_N |
| SATA4_TX_P | 19 | 19 | GND |
| SATA4_TX_N | 20 | 20 | GND |
| GND | 21 | 21 | SATA4_RX_P |

| Pin Name | Side B | Side A | Pin Name |
|---|---|---|---|
| GND | 22 | 22 | SATA4_RX_N |
| SATA3_TX_P | 23 | 23 | GND |
| SATA3_TX_N | 24 | 24 | GND |
| GND | 25 | 25 | SATA3_RX_P |
| GND | 26 | 26 | SATA3_RX_N |
| SATA2_TX_P | 27 | 27 | GND |
| SATA2_TX_N | 28 | 28 | GND |
| GND | 29 | 29 | SATA2_RX_P |
| GND | 30 | 30 | SATA2_RX_N |
| SATA1_TX_P | 31 | 31 | GND |
| SATA1_TX_N | 32 | 32 | GND |
| GND | 33 | 33 | SATA1_RX_P |
| GND | 34 | 34 | SATA1_RX_N |
| SATA0_TX_P | 35 | 35 | GND |
| SATA0_TX_N | 36 | 36 | GND |
| GND | 37 | 37 | SATA0_RX_P |
| GND | 38 | 38 | SATA0_RX_N |
| PCIE1_RESET# | 39 | 39 | GND |
| NC | 40 | 40 | GND |
| GND | 41 | 41 | NC |
| GND | 42 | 42 | NIC_SMBUS_ALERT# |
| NIC_SMBUS_SCL | 43 | 43 | GND |
| NIC_SMBUS_SDA | 44 | 44 | GND |
| GND | 45 | 45 | GE0_RX_P |
| GND | 46 | 46 | GE0_RX_N |
| GE0_TX_P | 47 | 47 | GND |
| GE0_TX_N | 48 | 48 | GND |
| GND | 49 | 49 | PCIE0_RX0_P |
| GND | 50 | 50 | PCIE0_RX0_N |
| PCIE0_TX0_P | 51 | 51 | GND |
| PCIE0_TX0_N | 52 | 52 | GND |
| GND | 53 | 53 | PCIE0_RX1_P |
| GND | 54 | 54 | PCIE0_RX1_N |
| PCIE0_TX1_P | 55 | 55 | GND |
| PCIE0_TX1_N | 56 | 56 | GND |
| GND | 57 | 57 | PCIE0_RX2_P |
| GND | 58 | 58 | PCIE0_RX2_N |
| PCIE0_TX2_P | 59 | 59 | GND |
| PCIE0_TX2_N | 60 | 60 | GND |

| Pin Name | Side B | Side A | Pin Name |
|---|---|---|---|
| GND | 61 | 61 | PCIE0_RX3_P |
| GND | 62 | 62 | PCIE0_RX3_N |
| PCIE0_TX3_P | 63 | 63 | GND |
| PCIE0_TX3_N | 64 | 64 | GND |
| GND | 65 | 65 | PCIE1_RX4_P |
| GND | 66 | 66 | PCIE1_RX4_N |
| PCIE1_TX4_P | 67 | 67 | GND |
| PCIE1_TX4_N | 68 | 68 | GND |
| GND | 69 | 69 | PCIE1_RX5_P |
| GND | 70 | 70 | PCIE1_RX5_N |
| PCIE1_TX5_P | 71 | 71 | GND |
| PCIE1_TX5_N | 72 | 72 | GND |
| GND | 73 | 73 | PCIE1_RX6_P |
| GND | 74 | 74 | PCIE1_RX6_N |
| PCIE1_TX6_P | 75 | 75 | GND |
| PCIE1_TX6_N | 76 | 76 | GND |
| GND | 77 | 77 | PCIE1_RX7_P |
| GND | 78 | 78 | PCIE1_RX7_N |
| PCIE1_TX7_P | 79 | 79 | GND |
| PCIE1_TX7_N | 80 | 80 | GND |
| GND | 81 | 81 | P12V |
| GND | 82 | 82 | P12V |

**Figure 7 AMD Open CS 1.0 Micro-Server Card Option 3 x16 Interface Pinout**

# 10 Environmental Requirements

The motherboard meets the following environmental requirements:

- Gaseous Contamination: Severity Level G1 per ANSI/ISA 71.04-1985
- Ambient operating temperature range: -5°C to +45°C.
- Operating and storage relative humidity: 10% to 90% (non-condensing)
- Storage temperature range: -40°C to +70°.
- Transportation temperature range: -55°C to +85°C (short-term storage).

The full OCP system also meets these requirements. In addition, the full system has an operating altitude with no de-ratings of 1000m (3300 feet).

## 10.1 Regulatory Compliance

The Open CS 1.0 card is designed to meet the below system targets in mind:

- FCC/CE Class "A" EMC
- UL Safety Enabled

## 10.2 Vibration and Shock

The Open CS 1.0 card is designed to meet the following shock and vibration requirements according to the following IEC specifications: IEC78-2-(*) and IEC721-3-(*) Standard & Levels. The testing requirements are listed below.

| | Operating | Non-Operating |
|---|---|---|
| **Vibration** | 0.5g acceleration, 1.5mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave/minute for each of the three axes (one sweep is 5 to 500 to 5 Hz) | 1g acceleration, 3mm amplitude, 5 to 500 Hz, 10 sweeps at 1 octave/minute for each of the three axes (one sweep is 5 to 500 to 5 Hz) |
| **Shock** | 6g, half-sine 11mS, 5 shocks for each of the three axes | 12g, half-sine 11mS, 10 shocks for each of the three axes |

**Figure 8 Vibration and Shock Requirements**

# 11 Prescribed Materials

## 11.1 Disallowed Components

The following components are not used in the design of the card:

- Components disallowed by the European Union's Restriction of Hazardous Substances Directive (RoHS 6)
- Trimmers and/or potentiometers
- Dip switches

## 11.2 Capacitors and Inductors

The following limitations apply to the use of capacitors:

- Only aluminum organic polymer capacitors made by high quality manufacturers are used; they must be rated 105°C.
- All capacitors have a predicted life of at least 50,000 hours at 45°C inlet air temperature, under worst conditions.
- Tantalum capacitors are forbidden.
- SMT ceramic capacitors with case size > 1206 are forbidden (size 1206 are still allowed when installed far from the PCB edge and with a correct orientation that minimizes risks of cracks).
- Ceramic material for SMT capacitors must be X7R or better material (COG or NP0 type should be used in critical portions of the motherboard).

Only SMT inductors may be used. The use of through hole inductors is disallowed.

## 11.3 SO-DIMM Connectors

The following SO-DIMM connectors are used in the design of the card:

- Foxconn AS0A626-H2S6-7H
- Foxconn AS0A626-H2R6-7H

# 12 Software Ecosystem

Most up to date information about OS and Tool support is listed below.

| Operating Systems | Status | Comments |
|---|---|---|
| Fedora for ARM64 | In process | Starts with the bootstrapping of Fedora 17<br>http://fedoraproject.org/wiki/Architectures/ARM/AArch64 |
| Ubuntu for ARM64 | Download Available | A bootable (raring) image available to download and run<br>http://lists.debian.org/debian-devel/2013/02/msg00413.html |
| Linux 3.7 | Available | Includes support for the ARM 64-bit architecture<br>http://kernelnewbies.org/Linux_3.7 |
| **Hypervisors** | **Status** | **Comments** |
| KVM | Ported to ARM64 | Implementation of KVM for arm64<br>http://marc.info/?l=kvm&m=136245528521204&w=2 |
| XEN | Ported to ARM64 | Has 32-bit and 64-bit ARM support available today<br>http://wiki.xenproject.org/wiki/Xen_ARM_with_Virtualization_Extensions |
| **Developer Tools** | **Status** | **Comments** |
| GCC 4.8 (compiler) | Available | Actively being used by Linaro community<br>http://gcc.gnu.org/gcc-4.8/changes.html |
| Glibc 2.17 (library) | Available | Includes ARM64 support contributed by Linaro<br>http://sourceware.org/ml/libc-announce/2012/msg00001.html |
| QEMU (emulator) | Available | FAST! processor emulator using a portable dynamic translator<br>https://launchpad.net/qemu-linaro/+milestone/2013.06 |

**Figure 9 Supported Operating Systems and Tools**

# 13 Adherence to AMD Motherboard Design;

The expectation is that close partnership between AMD and a selected ODM will occur. This will include joint review of specification, schematic, stack-up, layout, thermal, and chassis design.