

AT&T Open Programmable-PON OLT Specification

Revision 2.0

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# Acknowledgement

I would like to acknowledge the contribution and partnership of Xilinx, Feneck, CIG, ADLINK teams in development of this spec. Also to my colleagues at AT&T and at other Service Providers who provided invaluable insights into how the Open FPGA could be used. Lastly, the OCP, without whose support and existence this type of work would not be possible.

-Sumithra

# Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| Revision | Date | Author | Description |
| 1.0 | 09/22/17 | Sumithra Bhojan | Initial Draft |
| 2.0 | 10/24/18 | Sumithra Bhojan | Updated for 32 ports XGSPON, 25G PON support, 2 form factors |
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# Scope

This document defines the technical specifications for the AT&T Open Programmable-PON OLT submitted to the Open Compute Project.

# Overview

This document describes the technical specifications of the AT&T Open Programmable-PON OLT using FPGA. The system is a physical 1RU rack or half width 2RU Sled that is self‐ contained, and not part of a physical chassis system. However, like the GPON, XGSPON OLT system, this physical box is attached to a fabric (e.g. leaf and spine) that interconnects many to create large scale‐out virtual network elements[[1]](#footnote-1). The Open Programmable-PON OLT is a high-performance access design focused on NFV Infrastructure deployments which support 10Gbps/25Gbps PON access connectivity and provide up to 100Gbps uplinks to the ToR (Top of Rack) layer of the network. This design is intended to future proof the hardware design to include current XGSPON/NGPON2 and 25G PON readiness. One of the key benefit is that the FPGA’s can be dynamically configured to support higher speeds as subscriber’s transition to the next gen PON.

The OLT supports 32x SFP28 PON ports that each operate at 10G downstream (egress) and 10G upstream (ingress) and 8x 100G QSFP28 ports. For 25G PON, it would be a lower number of ports, with support for 8-16 PON ports at 25G downstream and 25G upstream. This will mature as 25G PON standards get finalized.

This Spec describes two variants of the OLT hardware design:

1. A 1RU design that supports standard 19” rack deployments.
2. A 2RU Half width sled design that supports CG19 Open rack deployments

The Open Programmable-PON OLT is a PHY‐Less design with the SFP28 connections directly attaching to the SERDES interfaces of the xPON FPGA for OLT. The Open Programmable-PON OLT supports traditional features found in Top of Rack switches such as:

* Redundant field replaceable power supply and fan units
* A variety of supported power supply voltages
* Support for “Front to Back” or “Back to Front” air flow direction

# Use case: Disaggregated Virtual OLT

For this use case, the device in this specification is part of disaggregated OLT that can be deployed in a central office or data centers as an edge cloud or an Edge POD. Figure 1 shows the disaggregation of a typical OLT and the mapping of its functions to NFV infrastructure, such as Aggregation Switch, Compute. Disaggregated virtual OLT can be part of a cloud infrastructure or a standalone POD that can scale dynamically. In this environment, the Open Programmable-PON OLT connects to an aggregation switch or leaf/spine devices that aggregate traffic and also provide transport for management and control.

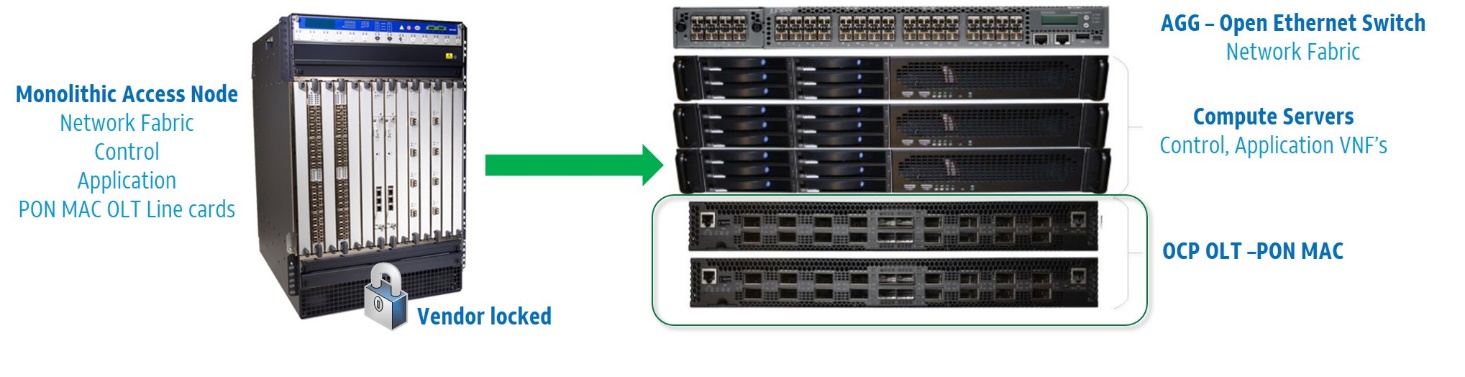


Figure – Disaggregated Virtual OLT

The low‐level management processes that might be typically performed by an embedded processor on a Programmable-PON 1RU OLT are performed outside the box, in a separate commodity server. This allows managing many OLT devices from a small number of commodity servers, and conserves compute and storage in the same way that performing aggregation in the ToR switch conserves aggregation typically performed on line cards to interface several 10/25G-PON PHY chips to a backplane or fabric.

This system is described as a disaggregated virtual OLT because the various software and hardware components that were once integrated into a single physical device have been separated and supported in a distributed way across NFV infrastructure. By doing this it becomes more likely to re‐use components among disparate networking functions and to independently scale resources and investments according the specific application of the technology.

# Use case: PON for xhaul

To support xHaul applications, the OLT need to provide: Low latency, capacity, and Synchronization.

Synchronization is accomplished using SyncE (Synchronous Ethernet) and IEEE 1588 timing paths.   
An optional Timing & Synchronization module can be added in this case.

To provide the latency and capacity needed for xHaul, the default DBA (Dynamic Bandwidth Allocation) is not sufficient. DBA in PON schedules the traffic in the Upstream, and is either Fixed or Reactive (by measuring the traffic upstream or requesting status from ONUs). Fix Bandwidth is Low Latency, but poor on capacity utilization and Reactive is good on capacity but poor on Latency.

Cooperative DBA is a method for the upper layer to “pro-actively” notify the DBA engine (scheduler), in advance of the actual traffic. This ensure both good latency and better capacity/utilization.

# Software Stack

The software used to support this system is shown in Figure 2. At the lowest level of the figure we find firmware and hardware drivers that are part of the software loaded and run on the FPGA chip. That software is loaded on the chip and then subsequently configured and managed through a matching low‐level API along with an OMCI stack which is run on a commodity/Open Compute server.

Open OLT should provide driver to interface with VOLTHA framework for management and control of the OLT. VOLTHA (Virtual OLT hardware Abstraction) is an open source project in Open Networking Foundation, that provides unified, vendor/technology agnostic management interface to the device. It hides PON level details such as T-CONT, GEM ports, OMCI etc. from the SDN controller and abstracts PON functions from the access device and makes it look like a switch that can be programmed by the northbound SDN controller.VOLTHA can be hosted on an external general purpose compute server or local to the Open OLT device.

*The licensing conditions of all required proprietary code and intellectual property MUST be clarified and publicly accessible and available for the OLT built with this specification.*

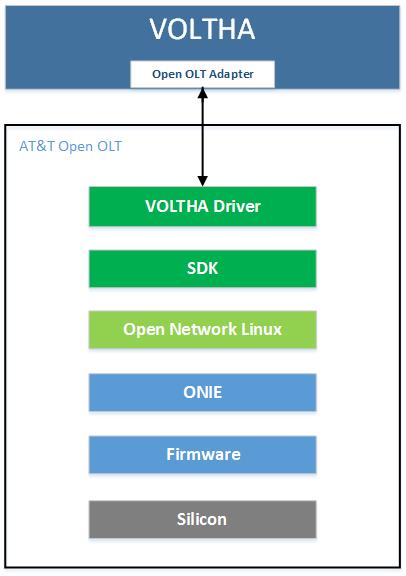


Figure 2 - Software stack for Open Programmable-PON OLT

# XGS-PON Network

A 10 Gigabit Services PON (XGS-PON) network supports symmetrical 10G/10G communications to enable a variety of applications. Some key features include:

* Data rates of : ~10Gbps (9953Mbps) DS/~10Gbps (9953Mbps) US
* At least 128 ONTs (downstream PON endpoints) per PON Link
* ToD synchronization
* ONT power saving operation
* Optional downstream AES encryption for each port
* IPv6
* Dual-stack IPv4 and IPv6
* Symmetric bandwidth allocation

Figure 3 shows a typical XGS-PON Network.

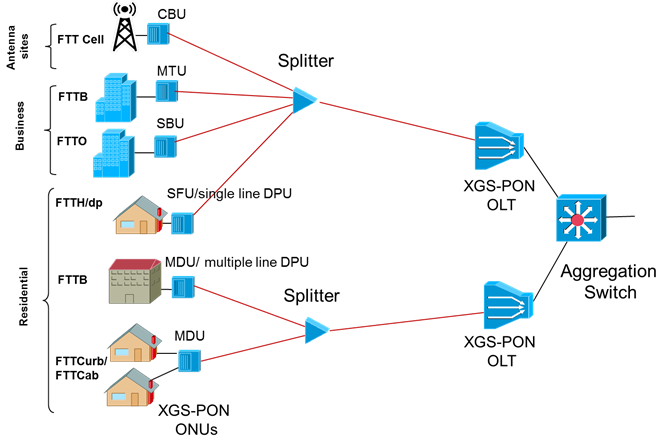


Figure 3 - XGS-PON Network

# Upgrade Path to 25GPON

The FPGA based module provides support for 25G PON. The FPGA Serdes needs to support 25G Burst Mode required for operation with future 25G PON Optics. 25G PON MAC will be larger from a FPGA resource perspective than 10G XGS-PON. The choice of FPGA size will determine how many 25G ports can be supported. A 10G PON optimized FPGA can support an approximate ratio of 2:1 (i.e. a 32 Port OLT for 10G or 16 ports for 25G). This specification does not preclude the use of larger FPGA to support more 25G Port as long as power budget is within the specified limits.

# FPGA PON BLOCK

Figure 4 shows the functional blocks of two 8-ports of XGSPON FPGA PON module. This module can then be used as a building block to develop various OLT hardware configuration for the different use cases for the service providers.

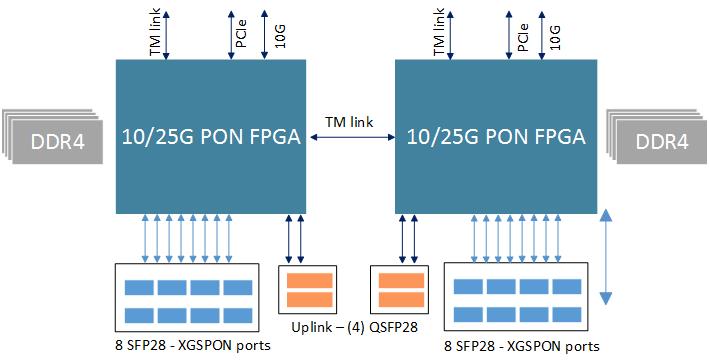


Figure 4 – FPGA PON Block diagram

The FPGA PON Module design is based on Xilinx Virtex model VU5P/7P. The Specification does not preclude other FPGA make/model that can meet this design requirements.

*The licensing conditions of all required proprietary code and intellectual property MUST be clarified and publicly accessible and available for the OLT built with this specification.*

Module consists of the following:

* Dual PON MAC FPGA
* 64 bit DDR4 memory for XGSPON reassembly (Capacity 32GB)
* 16 ports of XGSPON (10G) and future support of 25G PON using SFP28
* 4 QSFP28 uplinks; can be configured in different links/SERDES rate at 10G//25G
* Dual Interlaken or TM link (Optional) for aggregation between (2) 16 port modules
* Dual PCIe Gen4 and 25/10GE to CPU (Optional)

## PON MAC Feature:

* ITU-T G.9807 XGS-PON compliant
* Support up to 128 ONUs per PON port
* Support up to 1024 T-CONT/Alloc-ID per PON Port
* Support up to 1024 XGEM Ports per PON Port
* Total of 4096 XGEM-Port & Alloc-ID can be shared across a quad PON port
* External DDR4 Reassembly Memory
* Support both Status Reporting (SR) & Traffic Monitoring (TM ) DBA
* Support 20Km Reach (60 Km Logical)
* Downstream of 10 Gbps & Upstream of 10Gbps in XGS-PON

# System Design

The 8 port FPGA PON block can be used in different configuration to produce OLT system with 16, 24 and 32 ports of XGSPON to meet various use cases. This specification is targeted for the following design:

**32 port XGS PON OLT with no local aggregation** in the system. The disaggregated virtual OLT architecture uses an aggregation/leaf switch that OLT connects to and it’s efficient to perform aggregation in the centralized switch thus reducing power/cost.

There can be other designs (contribution driven) that can include local aggregation. The FPGA PON module will support that scenario as well.

Also there are two different hardware variants this specification will support:

1. A 1RU design that supports standard 19” rack deployments
2. A 2RU Half width sled design that supports CG19 Open rack deployments

Figure 5 shows the System block diagram, that uses two FPGA modules to provide (32) XGSPON ports and (8) 40G/100G uplink ports.

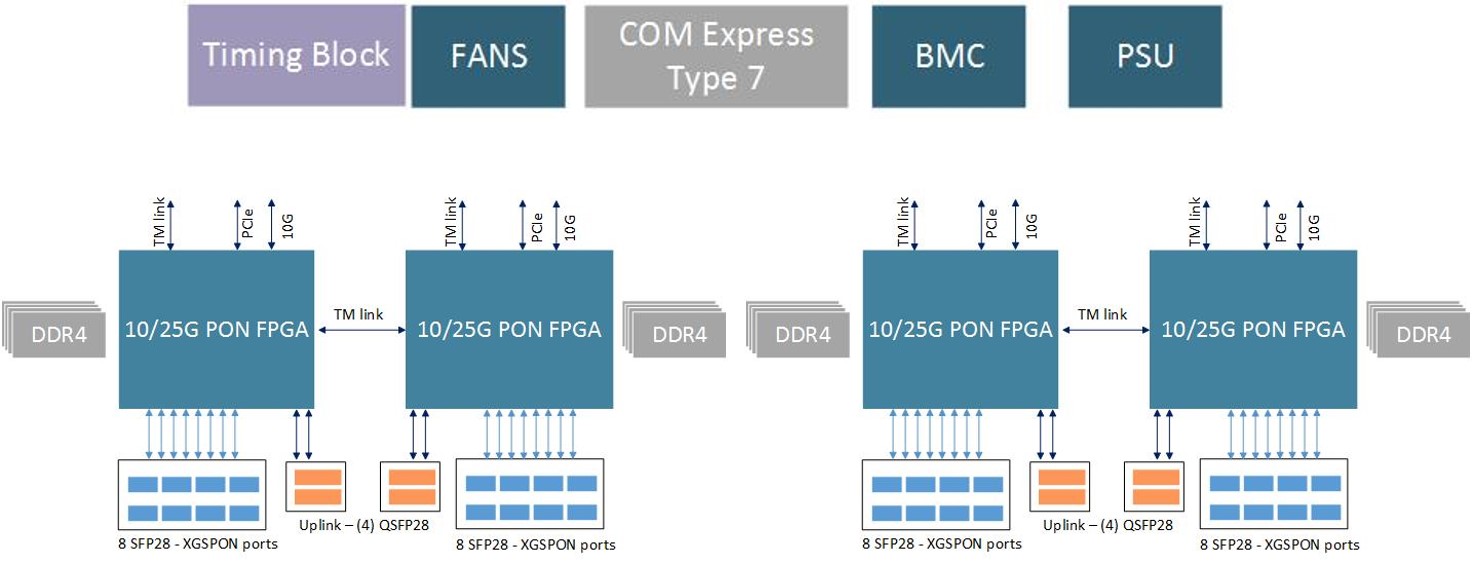


Figure 5 – System Level Block Diagram

## Host CPU (Optional)

The Host Module will use standard COM-Express type 7 form factor and interface. This supports choosing from a variety of different CPU options with different performance and price points including Intel Rangeley, D-1500, and ARM. COM-Express allows for different form factors in a compatible mounting strategy which this platform will support. A typical Host CPU for stand- alone OLT might include D-1500 2 to 4 Core with 16G RAM and 64G M.2 SSD.

## BMC

The BMC is associated with CPLD logic and allows for managing the Open XGS-PON 1RU vOLT. The BMC may be instantiated with a separate physical device, or a software component available with high reliability from the host module. When the BMC is provided on the host module, then the design must include a simplified, low-cost CPU 12 module to host the BMC software in those cases where a more functional CPU is not desired and the CPU module would normally be omitted from a build. The BMC must provide management for the following:

1) System, PON FPGA, and Host CPU module power management

2) Temperature monitoring

3) Voltage monitoring

4) Fan control

5) Reset control

6) Programming FPGA/CPLD/and other various flash/BIOS

7) Read the Rx loss and other signals from the SFP and QSFP ports

8) Host CPU Module boot up status

9) System Identifier, including ability to set user-defined identifier, as well as control of locator lamp.

10) Serial number / unique identifier

11) Board revision ID

12) I2C interfaces to Host CPU, USB, temperature sensors, and voltage controllers.

# Physical Overview

## Standard 19” 1RU unit

### Maximum Dimensions

|  |  |  |
| --- | --- | --- |
|  | Inches | Millimeters |
| Length - | 24 | 609.6 |
| Width – 19” rack | 17.5 with ears for 19” | 444.5 |
| Height – 1 RU | 1.75 | 44.45 |
| Note: Width does not include mounting ears – which must have holes or closed slots. Depth does not include PSU handles. | | |

4

5

## Front View

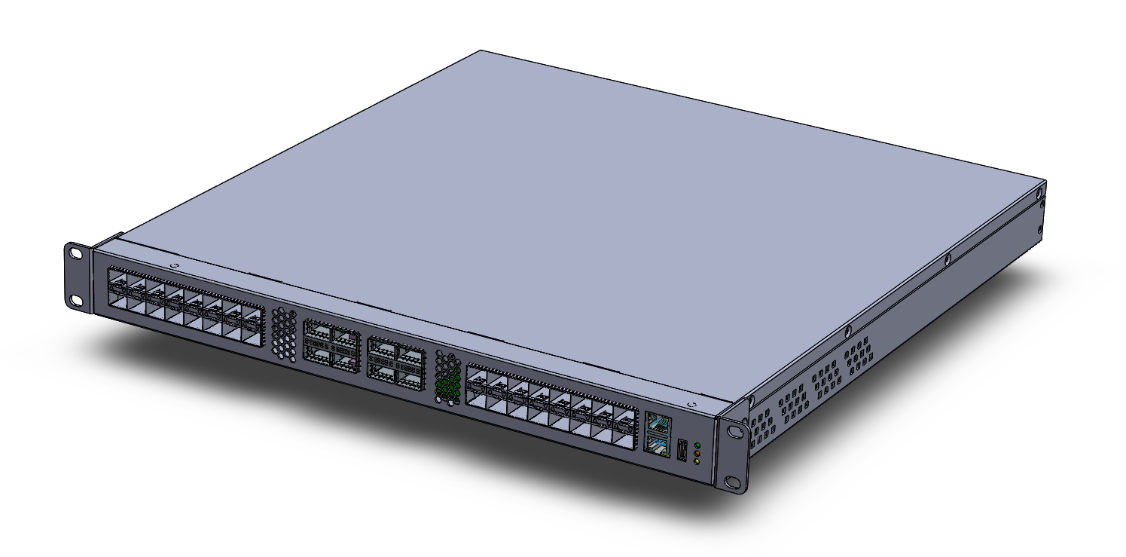
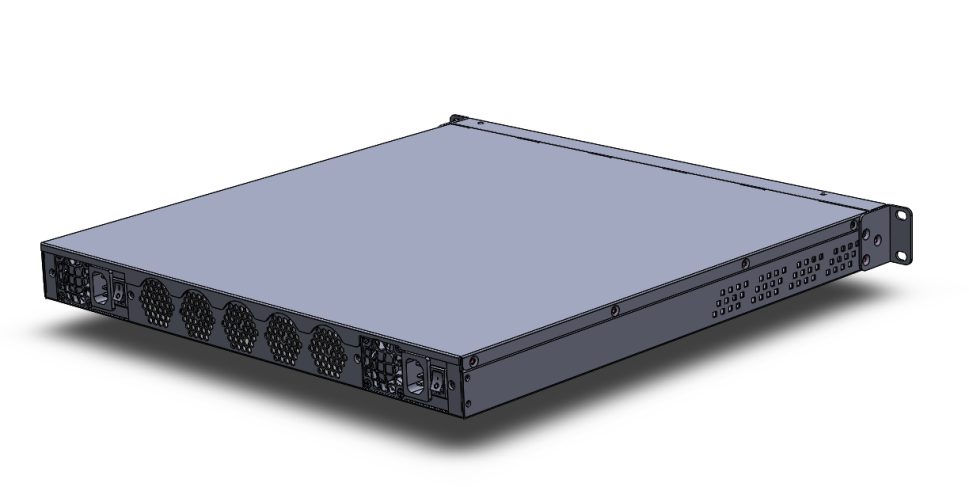


Figure 6 - Front Panel (Illustration only)

* PON Links: 32x SFP28 ports
* Uplink Ports: 8x QSFP28
* LEDs
  + SFP28 Module status
  + QSFP28 port status
  + System and PSU LED indicators
  + System Finder LED

## Rear View

* Five (4+1) redundant hot swappable fan modules (Including Color coding to indicate airflow direction)
* Two redundant hot swappable power supply modules
  + LED per power supply to indicate status
  + Color coding to indicate airflow direction



**Figure 7 – Rear view (Illustration only)**

2

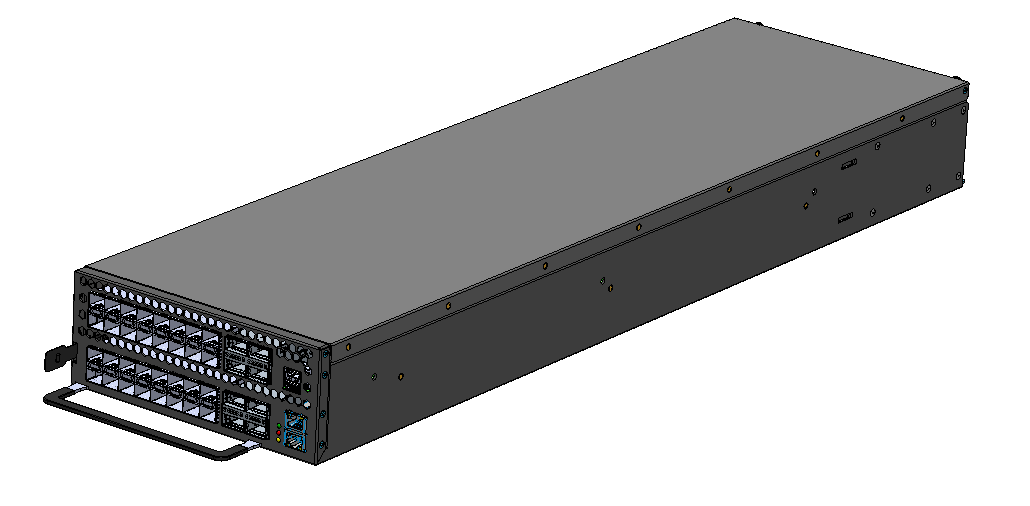
1

## CG-OpenRack-19 Half-Width OpenSled

### Maximum Dimensions

|  |  |  |
| --- | --- | --- |
|  | Inches | Millimeters |
| Length - | 30.7 | 780.00 |
| Width - | 8.4 | 215.00 |
| Height – 2 RU | 3.3 | 84.00 |

## Front View



**Figure 6 - Front Panel (Illustration only)**

* PON Links: 32x SFP28 ports
* Uplink Ports: 8x QSFP28
* LEDs
  + SFP28 Module status
  + QSFP28 port status
  + System and PSU LED indicators
  + System Finder LED

## Panel LED Definitions

|  |  |  |
| --- | --- | --- |
| LED Name | Description | State |
| PSU1 | Led to indicate status of Power Supply 1 | Green ‐ Normal  Amber ‐ Fault  Off – No Power |
| PSU2 | Led to indicate status of Power Supply 1 | Green ‐ Normal  Amber ‐ Fault  Off – No Power |
| Diag | LED to indicate system diagnostic test results | Green – Normal  Amber – Fault detected |
| FAN | LED to indicate the status of the system fans | Green – All fans operational  Amber – One or more fan fault |
| LOC | LED to indicate Location of switch in Data Center | Blue Flashing – Set by management to locate switch  Off – Function not active |
| SFP28 LEDS | LED built into  SFP28 cage to indicate port status | On Green/Flashing – Port up with active ONTs  Flashing indicates activity  On Amber – Port up with no active ONTs  Off – No Link/Port down |
| QSFP Break out LEDs | Each QSFP28 has four LEDs to indicate status of the individual 10-25G ports | On Green/Flashing – Individual 25G port has link at 25G. (yellow for 10G?)  Flashing indicates activity  Off – No Link |
| OOB LED | LED to indicate link status of 10/100/1000 management port | On Green/Flashing ‐ port has link  Off – No link |

## Field Replaceable Units

This section describes field replaceable modules used in the design. These include optical SFP28 and QSFP28 transceivers, fans and power supplies. All modules must be hot swappable without the use of tools.

### Power Supply Modules

The Open Programmable-PON OLT supports two hot swappable Power Supply Modules (PSMs) and needs only one to operate. Please use the below as a general guidelines for the PSUs selection:

* The PSM form factor should re-use an existing OCP form factor. (optional)
* The PSM must meet the power requirements of the design: e.g. 605W or more.
* The system must accept different PSM types (e.g. AC or DC) which have the same form factor.
* All PSMs must be available with F2B and B2F airflow.
* AC PSMs must support AC input between 100 & 240 VAC.
* AC PSMs must have a mechanism that prevents accidental dislodging of the cord.
* DC PSMs must support DC input between -57 & -40VDC.
* DC PSMs have additional physical connection requirements listed in AT&T TP 76450, section 2.4.



Figure 2 – Power Supply (Illustrative)

### Fan Modules

The Open Programmable-PON 1RU OLT supports multiple individual fan modules in an N+1 scheme where N modules are sufficient to cool the device. Fan modules may use different designs for number and size of fan, as long as the overall design cools appropriately with a failed device. In 1RU designs, a typical fan module might have two 40mmx40mmx54mm fans. An example of a suitable fan module is show from the front and back in Figure 3. There are two fan module types differentiated by airflow, Front-to-back and back-to-front (F2B and B2F).



Figure 3 – Fan (Illustrative B2F)

The design should re-use fan modules typically found in existing OCP specs.

## PCB Board Set

The Open Programmable-PON 1RU OLT is composed of several modules or PCBs. The design must have a separate board for the CPU to allow for different build options and for the CPU board to be omitted from a build completely.

The design may have additional modularity in PCB layout. For example, it’s acceptable to have a separate fan board module as a re-useable component across different system designs. Similarly so for other build options, like timing modules, and standard components like a BMC module.

Preferred designs for this spec. will re-use existing modules from other OCP Accepted designs.

# Software Support

The Open Programmable-PON OLT supports a base software package composed of the following components:

### BMC support

OpenBMC

### ONIE (Open Network Install Environment)

To allow installation and boot of ONL. ONIE version 2014.08 or greater will be supported

### Open Network Linux

See <http://opennetlinux.org/>for latest supported version

### Overall System Software

See http://opencord.org for information and documentation

See <https://github.com/opencord/cord> for software source

# General Specifications

## Power Consumption

The total estimated system power consumption of the AT&T 32 Port Open Programmable PON vOLT is ~544 Watts. A summary of power contributors is shown in Table 5.

All system components chosen for this build must be energy efficient to keep the energy consumption low.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Main Blocks | Qnt. | Typ. (W) | Max. (W) | Total Typ. (W) | Total Max. (W) |
| 16 port FPGA PON Module (PON MAC, DDR4) | 2 | 116 |  | 232 | <250 |
| QSFP28 Module | 8 | 4.95 | 5.0 | 39.6 | 40.0 |
| SFP28 Module | 32 |  | 3.8 | 121.6 | 121.6 |
| Timing (DPLL, clocks) | 1 | 3 | 3 | 3 | 3 |
| BMC | 1 | 3 | 3 | 3 | 3 |
| Fans | 5 | 18.0 | 24.0 | 90.0 | 120.0 |
|  |  |  |  |  |  |
| COME | 1 | 55 | 65 | 55 | 65 |
| Total estimated Power |  |  |  | 544.2 | 602.6 |

# Specification Requirements

AT&T has established specifications for servers and NFVI communications equipment that are intended to be used in Central Offices. These specs revisit classical NEBs requirements – particularly in the face of new resiliency and availability architectures. Servers and switches that are not a single point of failure for their services (e.g. follow a typical cloud resiliency model) follow ATT-TP-76207. Telco devices that do have or comprise single points of failure for their services including this specification follow ATT-TP-76208.

This specifications is subject to follow ATT-TP-76208 which is available at this URL: <https://ebiznet.sbc.com/sbcnebs/Documents/ATT-TP-76208_vOLT%20Equipment%20Standards.pdf>

These requirements are partially repeated here. Specifications that require testing must be confirmed by an accredited agency recognized by the National Cooperation for Laboratory Accreditation or ISO/IEC Guide 25 or ISO/IEC 17025. Note: These specifications are limitations placed on any design. The actual performance of Open XGSPON 1RU vOLT must meet or exceed these specifications.

## PowerConsumption

The total estimated system power consumption must be specified in watts. This is based upon worst case power assumptions for traffic, optics used, and environmental conditions. Typical power consumption should also be provided, as well as heat dissipation.

• ATIS TEER (ATIS-0600015.2009) should be measured and provided (Preferred)

• SPECpower\_ssj2008 can be substituted for ATIS TEER (Acceptable)

• US EPA Energy Star Certification is favored.

• Power terminations must be clearly labeled and fully protected with a non-metallic, non-flammable cover.

• ATT-TP-76208 lists additional power requirements for under and over voltage, grounding, and current characteristics.

## Environmental

• Light weight is favored

• 15 to 40°C operating range – de-rated 1°C for every 1000 ft (300 m) above 6000ft (1830m).

• Humidity 5% to 85% non-condensing (operational and storage)

• Vibration – IEC 68-2-36, IEC 68-2-6

• Shock – IEC 68-2-29 • Acoustic Noise Level – Under 78dB in 26 degree C

• Altitude: -200ft (-60 meters) to 6000ft (1830 meters).

## Safety

Fire Spread. Field conditions for telco deployment may require deployment in existing Carrier Communications Spaces that utilize Fire Code Exemptions and do not have automatic fire suppression. NFVI equipment, like the AT&T Open GPON OLT deployed in these locations must meet enhanced fire spread requirements:

Generally, the equipment must meet ATIS-0600319.2014 *Equipment Assemblies – Fire Propagation Risk Assessment Criteria* (see note below).

**Note:** Equipment may conform to this requirement by way of inherent design features that include all four items below:

1. Height of 2 RU or less
2. Horizontally mounted main printed circuit board
3. Metallic 5 sided enclosure with a metallic or non-metallic front cover or faceplate
4. Non-metallic materials shall comply with ATIS-0600307 4.1

For equipment that does not meet the fire spread requirements of ATIS-0600319.2014 by way of inherent design features noted above, the manufacturer must attest that the equipment has successfully passed the burn test as referenced in the ATIS document.

* UL/ Canada
* CB (Issued by TUV/RH)
* China CCC

## Electromagnetic Compatibility

* GR-1089-CORE
* FCC Title 47, Part 15, Subpart B Class A

## ROHS

Restriction of Hazardous Substances (6/6)

Compliance with Environmental procedure 020499-00 primarily focused on Restriction of Hazardous Substances (ROHS Directive 2002/95/EC) and Waste and Electrical and Electronic Equipment (WEEE Directive 2002/96/EC)

1. This type of system is described in ETSI NFV architecture, where it comprises the Infrastructure that supports Network Functions Virtualization – often called NFVI. Additionally, the open software beyond that described in this specification is collected and distributed by the Linux Foundation as part of the CORD project: http://opencord.org [↑](#footnote-ref-1)