Open Rack V3 Monitoring of Power and Battery Systems (PMC and PMI)

Rev: 0.65

10/13/2020

Authors:

License (OCP CLA Option)

Contributions to this Specification are made under the terms and conditions set forth in **Open Compute Project Contribution License Agreement ("OCP CLA")** ("Contribution License") by:

[Contributor Name(s) or Company name(s)]

You can review the signed copies of the applicable Contributor License(s) for this Specification on the OCP website at http://www.opencompute.org/products/specsanddesign

Usage of this Specification is governed by the terms and conditions set forth in [**select one: Open Web Foundation Final Specification Agreement ("OWFa 1.0"), Open Compute Project Hardware License – Permissive ("OCPHL Permissive"), Open Compute Project Hardware License – Copyleft ("OCPHL Reciprocal")**] **("Specification License").**

You can review the applicable Specification License(s) executed by the above referenced contributors to this Specification on the OCP website at http://www.opencompute.org/participate/legal-documents/

Note: The following clarifications, which distinguish technology licensed in the Contribution License and/or Specification License from those technologies merely referenced (but not licensed), were accepted by the Incubation Committee of the OCP:

[insert "None" or a description of the applicable clarifications].

NOTWITHSTANDING THE FOREGOING LICENSES, THIS SPECIFICATION IS PROVIDED BY OCP "AS IS" AND OCP EXPRESSLY DISCLAIMS ANY WARRANTIES (EXPRESS, IMPLIED, OR OTHERWISE), INCLUDING IMPLIED WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, FITNESS FOR A PARTICULAR PURPOSE, OR TITLE, RELATED TO THE SPECIFICATION. NOTICE IS HEREBY GIVEN, THAT OTHER RIGHTS NOT GRANTED AS SET FORTH ABOVE, INCLUDING WITHOUT LIMITATION, RIGHTS OF THIRD PARTIES WHO DID NOT EXECUTE THE ABOVE LICENSES, MAY BE IMPLICATED BY THE IMPLEMENTATION OF OR COMPLIANCE WITH THIS SPECIFICATION. OCP IS NOT RESPONSIBLE FOR IDENTIFYING RIGHTS FOR WHICH A LICENSE MAY BE REQUIRED IN ORDER TO IMPLEMENT THIS SPECIFICATION. THE ENTIRE RISK AS TO IMPLEMENTING OR OTHERWISE USING THE SPECIFICATION IS ASSUMED BY YOU. IN NO EVENT WILL OCP BE LIABLE TO YOU FOR ANY MONETARY DAMAGES WITH RESPECT TO ANY CLAIMS RELATED TO, OR ARISING OUT OF YOUR USE OF THIS SPECIFICATION, INCLUDING BUT NOT LIMITED TO ANY LIABILITY FOR LOST PROFITS OR ANY CONSEQUENTIAL, INCIDENTAL, INDIRECT, SPECIAL OR PUNITIVE DAMAGES OF ANY CHARACTER FROM ANY CAUSES OF ACTION OF ANY KIND WITH RESPECT TO THIS SPECIFICATION, WHETHER BASED ON BREACH OF CONTRACT, TORT (INCLUDING NEGLIGENCE), OR OTHERWISE, AND EVEN IF OCP HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

Table of Contents

Revision History

Date	Version	Change By	Comments
10/13/2020	0.65	hamidk@	Added comment on the edge connector and RJ45s to specify pull up/down.

1. Scope

This document defines the technical specifications for an Open Rack V3 Power Management Controller used in the Open Compute Project.

2. PMC Overview

Power Management Controller (PMC) is a management module that sits on a Open Rack V3 Power and Battery Shelves. On one end, in has communication with the PSU or BBUs for monitoring and control purposes – Downstream communication through sliver straddle connector. On the other end, the Upstream communication, interacts with centralized system through the use of RJ45 connectors.

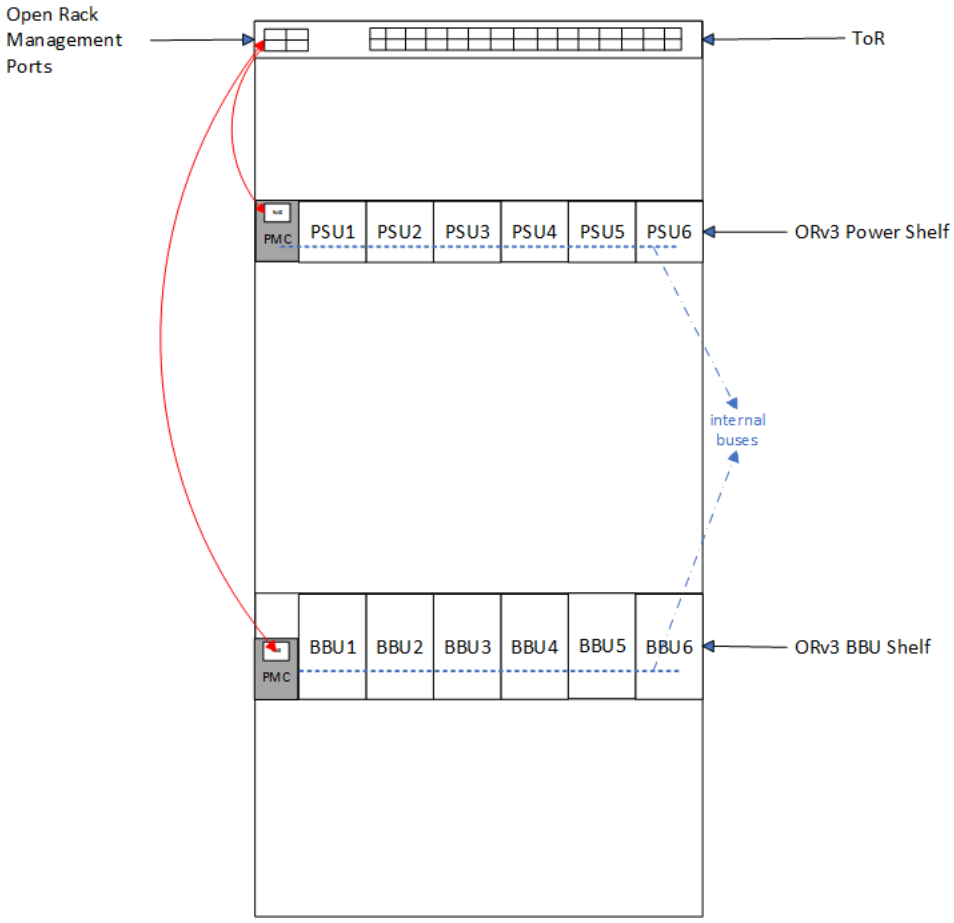


Figure 1: Overall block diagram of PMC

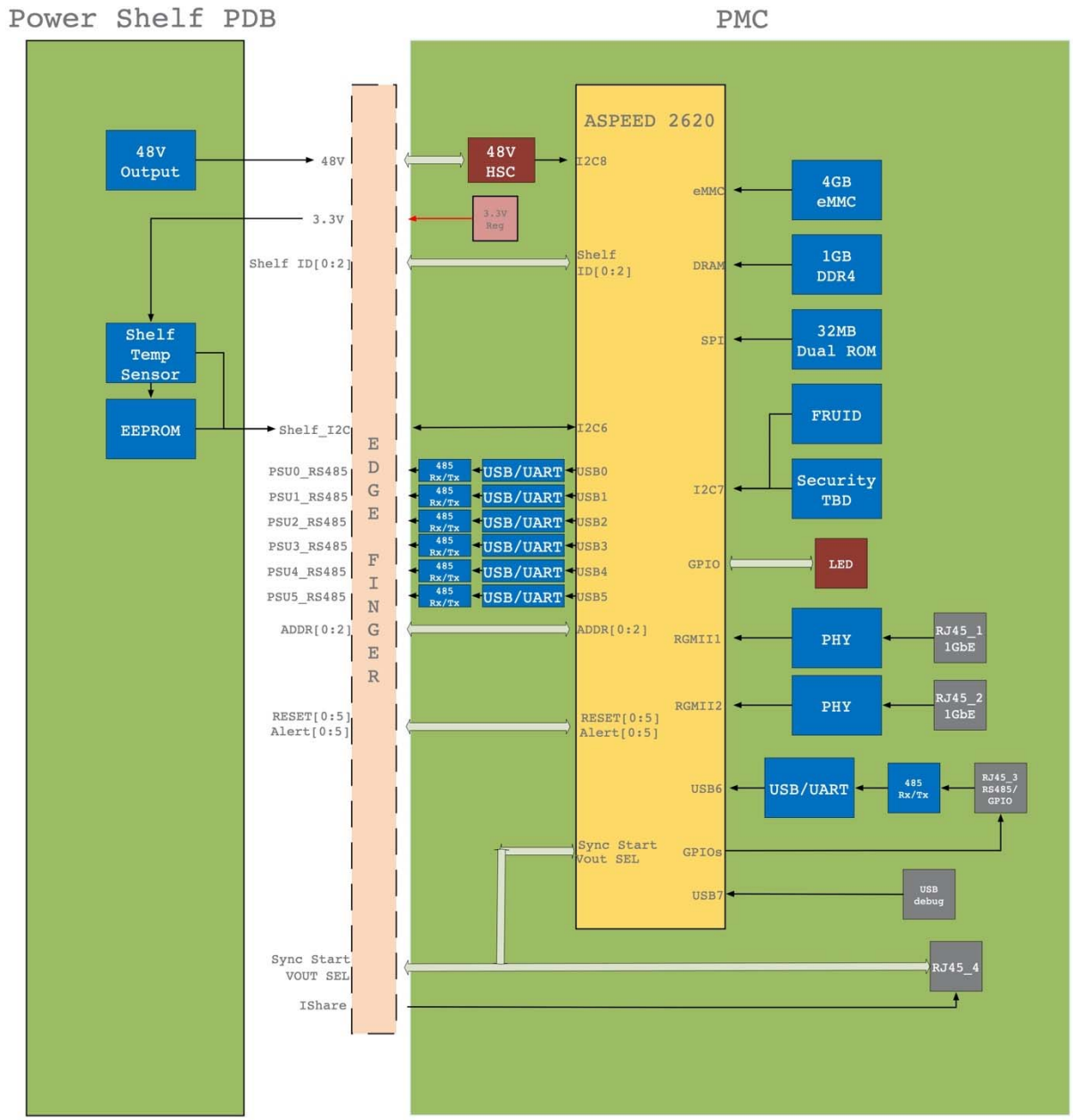


Figure 2 - Top Level Block Diagram of PMC

3. PMC Electrical

3.1 Microprocessor

The Power Management Controller shall incorporate the ASpeed ARM Cortex A7 processor AST2620. A list of key features is shown below. A functional block diagram of the processor is shown in Figure 3.

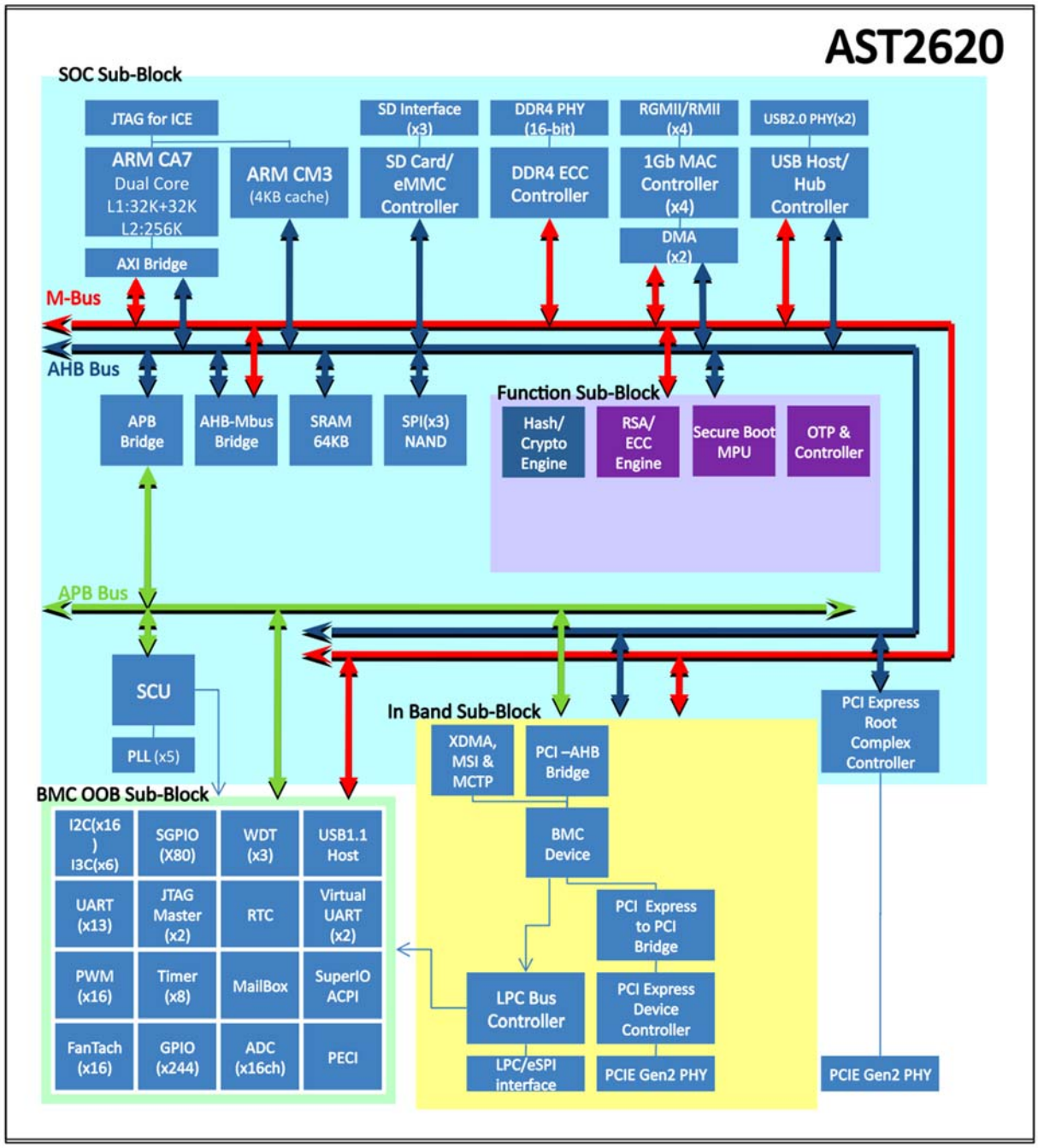


Figure 3 AST2600 Block Diagram

3.2 DDR4 Memory

The board shall support 1GB of DDR4 Memory.

3.3 2x NOR Flash

The Power Management Controller shall support 64MB of SPI NOR flash. TBD SPI clock

3.4 eMMC

The Power Management Controller shall support 4GB of eMMC.

Some use cases: storing SW images, Blackbox data, high-frequency data capture.

3.5 Clocks

TBD

3.6 Real Time Clock

TBD

3.7 FRU EEPROM

The PMC shall support a 32Kb FRUID EEPROM for storage of manufacturing data. The device shall be M24128-BWMN6TP or equivalent. Data in the EEPROM will be configured as an IPMI FRU device and fields are defined in the FRU ID Specification for the Rack Manager.

3.8 LEDs

The design shall contain the following bi-color LED to indicate functional status.

LED Name	REF Des	Color	Description
Power LED	TBD	Blue	Indicates Power Status of the PMC
Attention	TBD	Amber	Indicates that a fault has occurred

Table 1 - LED Assignments (bi-color)

The Power LED indicates that all of the power rails on the PMC are good. The LED shall be visible on the front bulkhead of the assembly.

The Attention LED indicates that a fault has been detected on the PMC. The LED shall be controlled by GPIO on the AST2600 and shall be visible on the front bulkhead of the assembly.

3.9 PSU/BBU Control

This section will define the interconnection signals between the Power Shelf back plane.

3.9.1 Reset

The PMC shall support a PSU_RESET_N output signal to each of up to 12 PSUs for allowing the PSUs to power up. The signals shall be available on the GPIOs of the processor. This signal is pulled low to ground through a low impendence resistor on the PMC (low = turn off PSU).

3.9.2 I2C/PMBUS

The PMC shall support and master a total of seven external I2C buses to communicate with the PSU's inside the chassis and the back plane. Each of six PSU I2C buses will be used to communicate up to max of two individual PSU's. One backplane management I2C with be used to identify backplane and PSUs.

3.9.3 RS485/MODBUS

The PMC shall support and master a total of seven external RS485 buses to communicate with the PSU's inside the chassis and the front panel.

3.9.4 Alert

The PMC shall support an active low PSU_ALERT_N signal from each of up to 12 PSUs. The signals shall be available on the GPIOs of the processor.

3.9.5 Ishare

The PMC shall support a passthrough analogue signal, PSU_ISHARE. This signal shall be a passthrough from the edge connector to the UART RJ-45 defined below.

3.9.6 Vout Select

The PMC shall support a PSU_VOUT_SEL signal to the collective PSU group for setting PSU Vout between 48 and 50V. This signal shall be available on a GPIO of the processor. This signal shall be asserted high for 50V and shall be pulled to ground for 48V. Time duration is adjustable.

3.9.7 Sync start

Pass through signal and capture.

3.9.8 3.3VDC Output

The PMC shall support a 3.3V power output from the edge connector to support the backplane FRU device. This output shall support 3.3V operation at up to 5mA.

3.9.9 Power Shelf Temp and FRU

The PMC would be connected to an I2C enabled Temperature sensor

3.10 48V input Power

PMC shall support 48V input power through the edge connector.

3.11 PS Kill

PS kill is a mate-first, break-last pin to initiate connection to the PSUs through the backplane to safely connect the PMC. It will be pulled low to the backplane. On the shelf side, short to the Ground.

3.12 PCB Revision

The power management controller shall support reading of a 3-bit PCB revision using GPIOs on the AST2600 processor. Revision shall be set using strapping resistors. The purpose of the ID bits is to communicate to firmware the identity of the Power Management Controller in the event that different PCB revisions will require different firmware features to be enabled or disabled. The ID should be incremented with each revision of the PCB.

ID	Description
000	EV
001	DV
010	PV
011	TBD
100	TBD
101	TBD
110	TBD
111	TBD

Table 2 - PCB Revision ID

3.13 Board Interface ID

The Power Management Controller shall support reading of a 3-bit interface ID

Shelf ID	Shelf type
000	1U power shelf
001	2U power shelf
010	Battery shelf
011	TBD
100	TBD
101	TBD
110	TBD
111	TBD

3.14 USB debug

TBD

4. PMC Connectors

4.1 4x RJ45 Connectors

The PMC shall contain four RJ45 connectors located on the bulkhead of the assembly. The pinouts of the four connectors are shown below. The RJ45 location shall be defined in the mechanical section 8.2.

Looking from the front, Top left RJ45 is #1, Top right is #2, bottom left is #3, bottom right is #4.

Table 3 : RJ45 #1 - Ethernet

Pin #	Signal	I/O	Description
1	TX_D1+	O	Transmit Data +
2	TX_D1-	O	Transmit Data -
3	RX_D2+	I	Receive Data +
4	BI_D3+	I/O	Bi-directional Data +
5	BI_D3-	I/O	Bi-directional Data -
6	RX_D2-	I	Receive Data -
7	BI_D4+	I/O	Bi-directional Data +
8	BI_D4-	I/O	Bi-directional Data -

Table 4 : RJ45 #2 – Ethernet

Pin #	Signal	I/O	Description
1	TX_D1+	O	Transmit Data +
2	TX_D1-	O	Transmit Data -
3	RX_D2+	I	Receive Data +
4	BI_D3+	I/O	Bi-directional Data +
5	BI_D3-	I/O	Bi-directional Data -
6	RX_D2-	I	Receive Data -
7	BI_D4+	I/O	Bi-directional Data +
8	BI_D4-	I/O	Bi-directional Data -

Table 5 : RJ45 #3, RS485

Pin	Wire color	I/O	Function	
1	White/Orange	I	GND	
2	Orange	O	PLS_F	Internal pull up 10k to 3.3V - Active Low.
3	White/Green	O	BKP_F	Internal pull up 10k to 3.3V - Active Low.
4	Blue	I/O	RS485A_F	
5	White/Blue	I/O	RS485B_F	
6	Green	I	RS485_Addr2_F	Internal pull up 10k to 3.3V
7	White/Brown	I	RS485_Addr1_F	Internal pull up 10k to 3.3V

8	Brown	I	RS485_Addr0_F	Internal pull up 10k to 3.3V

Table 6 : RJ45#4, Console/Debug

Pin	Wire color	I/O	Function	
1	White/Orange	A	ISHARE	Pass through signal.
2	Orange	I	GND	
3	White/Green	I/O	SYNC_START	
4	Blue	O	VOUT_SEL	Internal pull up 10k to 3.3V. Logic "Low"= Set Output 48V Logic "High"=Set Output 50V Default 50V for PSU. Default 48V for PSU.
5	White/Blue	I	GND	
6	Green	I		
7	White/Brown	I		
8	Brown	I		

4.2 Edge Connector

Pin #	Signal Name	I/O	Description	Comment
A1	ADDR_ID_0	I	Shelf ID	Internal pull up 10k to 3.3V. See shelf ID table for pin config on the shelf.
B1	ADDR_ID_1	I	Shelf ID	Internal pull up 10k to 3.3V. See shelf ID table for pin config on the shelf.
A2	ADDR_ID_2	I	Shelf ID	Internal pull up 10k to 3.3V. See shelf ID table for pin config on the shelf.
B2	GND	I	Ground	
A3	ALERT_0_N	I	PSU/BBU Alert	Internal pull up 10k to 3.3V - Active Low.
B3	ALERT_1_N	I	PSU/BBU Alert	Internal pull up 10k to 3.3V - Active Low.
A4	ALERT_2_N	I	PSU/BBU Alert	Internal pull up 10k to 3.3V - Active Low.
B4	ALERT_3_N	I	PSU/BBU Alert	Internal pull up 10k to 3.3V - Active Low.
A5	ALERT_4_N	I	PSU/BBU Alert	Internal pull up 10k to 3.3V - Active Low.
B5	ALERT_5_N	I	PSU/BBU Alert	Internal pull up 10k to 3.3V - Active Low.
A6	ALERT_6_N	I	PSU/BBU Alert	Internal pull up 10k to 3.3V - Active Low.
B6	ALERT_7_N	I	PSU/BBU Alert	Internal pull up 10k to 3.3V - Active Low.
A7	ALERT_8_N	I	PSU/BBU Alert	Internal pull up 10k to 3.3V - Active Low.
B7	ALERT_9_N	I	PSU/BBU Alert	Internal pull up 10k to 3.3V - Active Low.

A8	ALERT_10_N	I	PSU/BBU Alert	Internal pull up 10k to 3.3V - Active Low.
B8	ALERT_11_N	I	PSU/BBU Alert	Internal pull up 10k to 3.3V - Active Low.
A9	GND	I	Ground	
B9	RESET_0	O	PSU/BBU Reset	Internal pull down 10k resistor. Logic "low to High"= Reset the PSU/BBU.
A10	RESET_1	O	PSU/BBU Reset	Internal pull down 10k resistor. Logic "low to High"= Reset the PSU/BBU.
B10	RESET_2	O	PSU/BBU Reset	Internal pull down 10k resistor. Logic "low to High"= Reset the PSU/BBU.
A11	RESET_3	O	PSU/BBU Reset	Internal pull down 10k resistor. Logic "low to High"= Reset the PSU/BBU.
B11	RESET_4	O	PSU/BBU Reset	Internal pull down 10k resistor. Logic "low to High"= Reset the PSU/BBU.
A12	RESET_5	O	PSU/BBU Reset	Internal pull down 10k resistor. Logic "low to High"= Reset the PSU/BBU.
B12	RESET_6	O	PSU/BBU Reset	Internal pull down 10k resistor. Logic "low to High"= Reset the PSU/BBU.
A13	RESET_7	O	PSU/BBU Reset	Internal pull down 10k resistor. Logic "low to High"= Reset the PSU/BBU.
B13	RESET_8	O	PSU/BBU Reset	Internal pull down 10k resistor. Logic "low to High"= Reset the PSU/BBU.
A14	RESET_9	O	PSU/BBU Reset	Internal pull down 10k resistor. Logic "low to High"= Reset the PSU/BBU.
B14	RESET_10	O	PSU/BBU Reset	Internal pull down 10k resistor. Logic "low to High"= Reset the PSU/BBU.
A15	RESET_11	O	PSU/BBU Reset	Internal pull down 10k resistor. Logic "low to High"= Reset the PSU/BBU.
B15	GND	I	Ground	
A16	PLS	I	PSU/BBU Power Loss Siren	Internal pull up 10k to 3.3V - Active Low.
B16	BKP	I	PSU/BBU BKP (not used)	Internal pull up 10k to 3.3V - Active Low.
A17	RS485_Addr0	O	PSU/BBU MODBUS address	Internal pull up 10k to 3.3V
B17	RS485_Addr1	O	PSU/BBU MODBUS address	Internal pull up 10k to 3.3V
A18	RS485_Addr2	O	PSU/BBU MODBUS address	Internal pull up 10k to 3.3V
B18	RS485A_0	I/O	PSU/BBU MODBUS	
A19	RS485B_0	I/O	PSU/BBU MODBUS	
B19	RS485A_1	I/O	PSU/BBU MODBUS	
A20	RS485B_1	I/O	PSU/BBU MODBUS	
B20	RS485A_2	I/O	PSU/BBU MODBUS	
A21	RS485B_2	I/O	PSU/BBU MODBUS	
B21	RS485A_3	I/O	PSU/BBU MODBUS	
A22	RS485B_3	I/O	PSU/BBU MODBUS	
B22	RS485A_4	I/O	PSU/BBU MODBUS	
A23	RS485B_4	I/O	PSU/BBU MODBUS	
B23	RS485A_5	I/O	PSU/BBU MODBUS	
A24	RS485B_5	I/O	PSU/BBU MODBUS	

B24	I2C_SDA_shelf	I/O	I2C for Shelf Temp and FRU	Internal pull up 10k to 3.3V
A25	I2C_CLK_shelf	O	I2C for Shelf Temp and FRU	Internal pull up 10k to 3.3V
B25	GPIO0	I/O		
A26	GPIO1	I/O		
B26	GPIO2	I/O		
A27	GPIO3	I/O		
B27	GPIO4	I/O		
A28	GPIO5	I/O		
B28	GPIO6	I/O		
A29	GPIO7	I/O		
B29	GPIO8	I/O		
A30	GPIO9	I/O		
B30	GPIO10	I/O		
A31	GPIO11	I/O		
B31	GND	O	Ground	
A32	ISHARE	A	PSU/BBU Current Sharing	Pass through signal.
B32	SYNC_START	I/O	PSU/BBU Sync Start	
A33	VOUT_SEL	O	PSU/BBU Vout Select	Internal pull up 10k to 3.3V. Logic "Low"= Set Output 48V Logic "High"=Set Output 50V Default 50V for PSU. Default 48V for PSU.
B33	P3V3_shelf	O	3.3V for shelf I2C	
A34	GND	O	Ground	
B34	ADC0	A		
A35	ADC1	A		
B35	ADC2	A		
A36	ADC3	A		
B36	ADC4	A		
A37	ADC5	A		
B37	ADC6	A		
A38	ADC7	A		
B38	PMC_KILL	I	Power Kill, short pin	Internal pull up 10k to 3.3V Connected to GND on the shelf.
A39	RSVD	-	Reserved	
B39	RSVD	-	Reserved	
A40	P48V_RTN (GND)	I	Ground	
B40	P48V_RTN (GND)	I	Ground	
A41	NC (clearance)	-	No Connect	
B41	NC (clearance)	-	No Connect	
A42	P48V_IN	I	48V Power In	
B42	P48V_IN	I	48V Power In	

Yellow = No use-case currently, for future expansions.

5. PMC Downstream communication to PSU and BBU

This section contains PSU/BBU to Power Management Controller interface through I2C data and I2C clock signals on PMBus. The PMC shall be PMBus 2.0 compatible. The communication protocol, control, monitoring and reporting requirements of power supply and BBU operation are described in detail in the power supply specifications.

5.1 PSU Firmware Update

PMC Firmware shall support PSU firmware update. PMC firmware should also support SFTP so that client can upload the PSU firmware image and initiate the PSU firmware update. Please refer to “PSU Software Interface Specification” for details on specific command format and detailed flow for PSU firmware update.

Note:

Before starting the FW update process on the PSU's, PMC shall check for any faults in PSU using STATUS_WORD command and if any of phase in PSU has any fault, PMC should return FW_UPDATE_BLOCKED.

For FORCE_FW_UPDATE, PMC should not check for any fault and start FW update immediately.

6. PMC Upstream communication

6.1 RS-485: Modbus

The PMC utilizes the RS485 standard for communication between the power supplies residing in a 'Power Shel and a 'Rack Monitor'.

MODBUS is the serial communication protocol to be used with this standard.

All aspects of the MODBUS protocol are to follow the MODBUS Organization specifications and implementation guides, namely the reference documents below:

[1]: MODBUS Serial Line Protocol and Implementation Guide V1.02

[2]: MODBUS Protocol Specification (MODBUS APPLICATION PROTOCOL SPECIFICATIONV1.1b)

There will be exceptions granted if hardware does not allow for use of required transmission (MSB vs LSB). However, the transmission across products and vendors must remain as stated in this document

The protocol is a half-duplex Master/Slave. The Rack Monitor is always the master and has complete, unidirectional control over the slaves. Power supplies and other devices are considered slaves in this arrangement.

Unicast protocol mode is to be implemented. This means that the master always addresses one node only at a given time. Broadcast mode is not allowed in this communication scheme. There is only one master in the system. Slaves do not initiate communication to the master or other slaves.

6.1.1 Hardware Interface

Up to X racks can be connected to one Rack Monitor. In each rack, there can be at most X power shelves; each power shelf houses 6 power supplies. All slaves are to have their own unique address.

To accommodate for such addressing, without allowing broadcast mode, the following structure is to be used to give each power supply a unique address, for up to 18 power supplies.

6.1.2 Addressing

Slave addresses are reserved for 0x01 to 0xF7.

(Must add more details)

6.1.3 Message Frame

The message frame follows a standard MODBUS RTU frame format:

Start	**Address**	**Function**	**Data**	**CRC**	**End**
≥3.5 Bytes	1 Byte	1 Byte	0-32 Bytes	2 Bytes	≥3.5 Bytes

Parameter	Description
Bit Rate	19.2 kbps
Bits per Byte	1 Start Bit
	8 Data Bits (LSB sent first)
	1 Parity Bit (Even)
	1 Stop Bit
Address	Slave Address (xxx to xxx)
Function	Refer to Table 7
Data	Read request: 4 bytes
	Write request 1-32 bytes
	Read/Write request is determined by the number of Bytes received
CRC	Refer to reference 1, section 2.5.1.2
Start/End	At least 3.5 Bytes
Reply Timeout	1sec

6.1.4 MODBUS Functions

A subset of the standard MODBUS functions will be used. All functions that are not defined will return an exception code.

Read Holding register	R	Read register	0x03	Required
Read input register	R	Read register	0x04	Required
Write Single Register	W	Write register	0x06	Required but will fail on all read only registers
Write multiple register	W	Write multiple registers	0x10	Optional but will fail if not properly implemented
Read File Record	R	May be used by vendor for Firmware update, etc.	0x14	Optional but will fail if not properly implemented
Write File Record	W	May be used by vendor for Firmware update, etc.	0x15	Optional but will fail if not properly implemented
Bit masked Write register	W	Write only unmasked bits in a register	0x16	Optional but will fail if not properly implemented
R/W multiple	R/W	Read a register and write many registers at once	0x17	Optional but will fail if not properly implemented
Encapsulated Transport	NA	May be used by vendor for Firmware update, etc.	0x2B	Optional but will fail if not properly implemented
Vendor defined functions	N/A	May be used by vendor for Firmware update, etc.	0x41 to 0x48	Optional but will fail if not properly implemented

6.1.5 Two Wire MODBUS implementation

This serial communication is implemented on a two-wire interface in accordance with EIA/TIA-485. In this two-wire implementation only one Master-Slave (driver) pair can transmit.

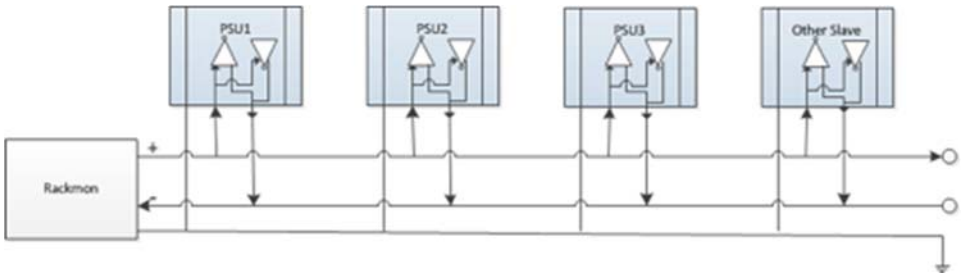
In addition to the two transmit wires. A reference ground will be available on pin 1.

Since this system is used locally within a rack, the wire length is under 2.5meters. The number of slaves will be limited to the number of power supplies used; 6 per rack. Also, considering the baud rate of the system, no termination is required at this time.

Note: Termination may be introduced if necessary at DVT, PVT

The unit load of each device will be ¼ units or less.

The Master and Slaves will utilize RJ45 connectors and twisted Cat-5 cable to accommodate for the two-wire system. Other extra pins on the cable and connector will be used for addressing purposes.



(Must add the rest later)

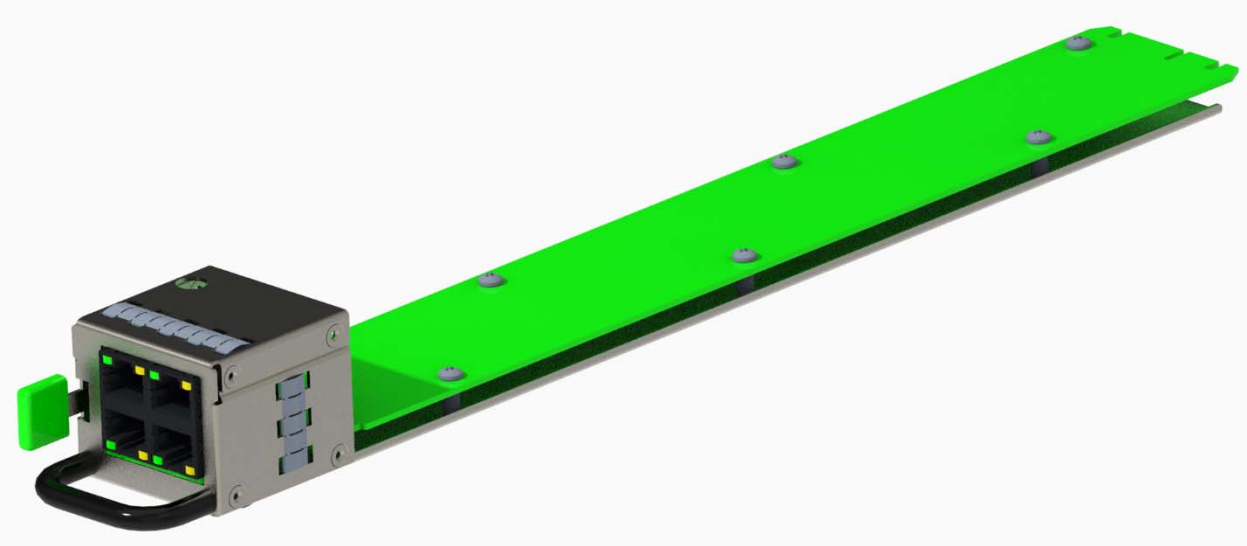
6.2 Ethernet: 1000 Base-T Ethernet

The PMC will have two 1GbE ports that will be used primarily for managing the power shelf and collect telemetry. From a firmware standpoint, we anticipate the ports to be symmetric. That is, the ports will provide the same APIs and services. Further, we anticipate that the PMC firmware stack will provide a RedFish compliant interface. The full specification of RedFish is here. We expect the pinout definition of both ports to be IEEE 802.3ab compliant as shown in the table below.

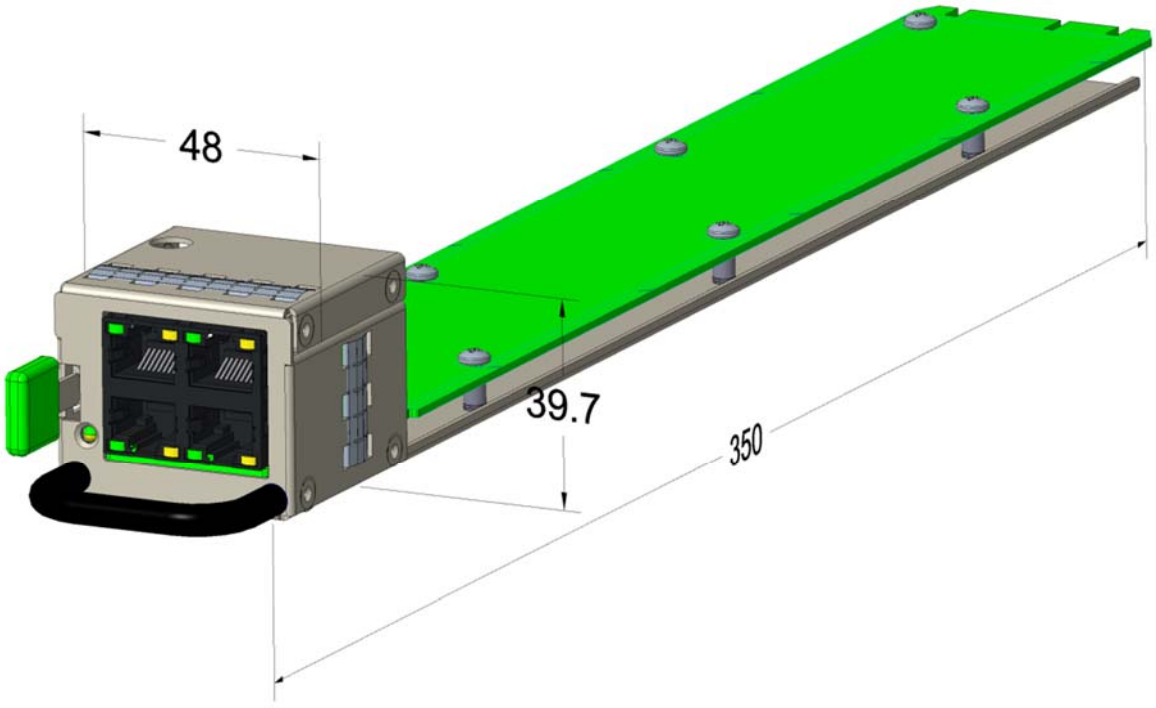
Pin	Name	Description

1	BI_DA+	Bi-directional pair A +
2	BI_DA-	Bi-directional pair A -
3	BI_DB+	Bi-directional pair B +
4	BI_DC+	Bi-directional pair C +
5	BI_DC-	Bi-directional pair C -
6	BI_DB-	Bi-directional pair B -
7	BI_DD+	Bi-directional pair D +
8	BI_DD-	Bi-directional pair D -

7. Mechanical



7.1 Major Dimensions

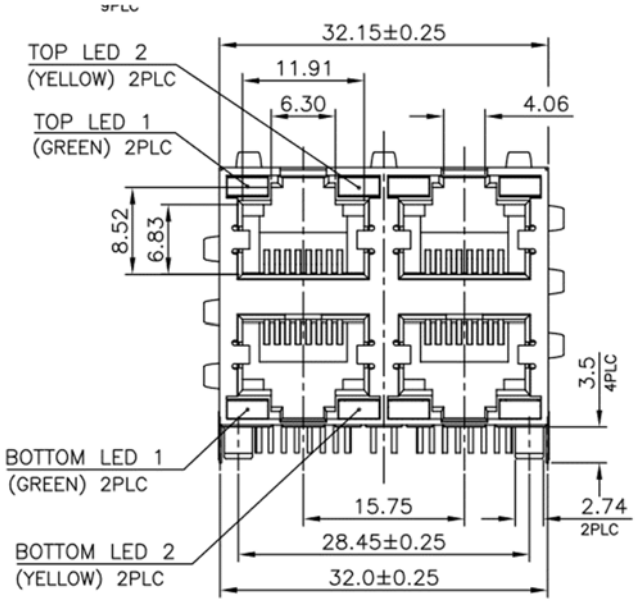


The PMC is 39.7mm tall, 48mm wide, and 350mm deep. Each of these has tolerances of ±1mm.

7.2 Connectors

7.2.1 RJ45 Connector

In the front of the PMC, there is a single 4xRJ45 connector. This is a modular jack connector in a 2x2 configuration of RJ45 with LED. The MPN shall be TE 2041376-2 or equivalent. Note that this connector comes with spring fingers. These must contact the chassis in order to provide good EMI sealing.

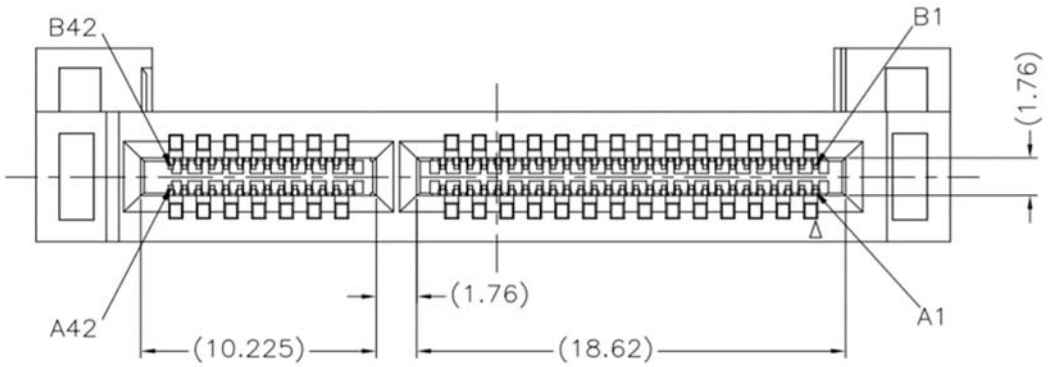


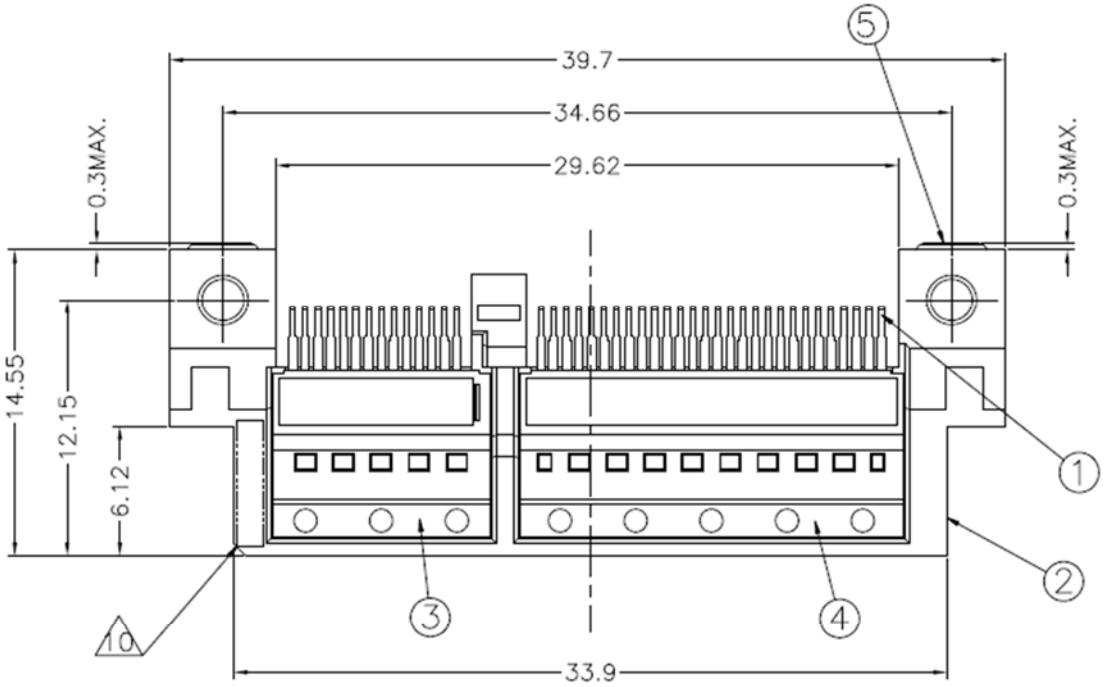
#1 #2

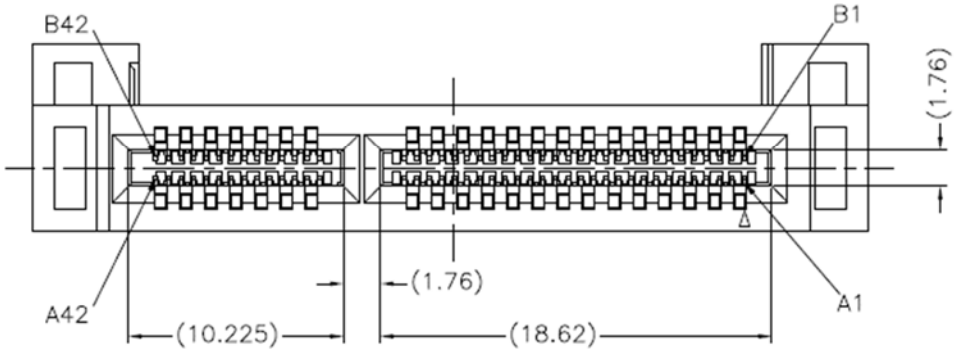
#3 #4

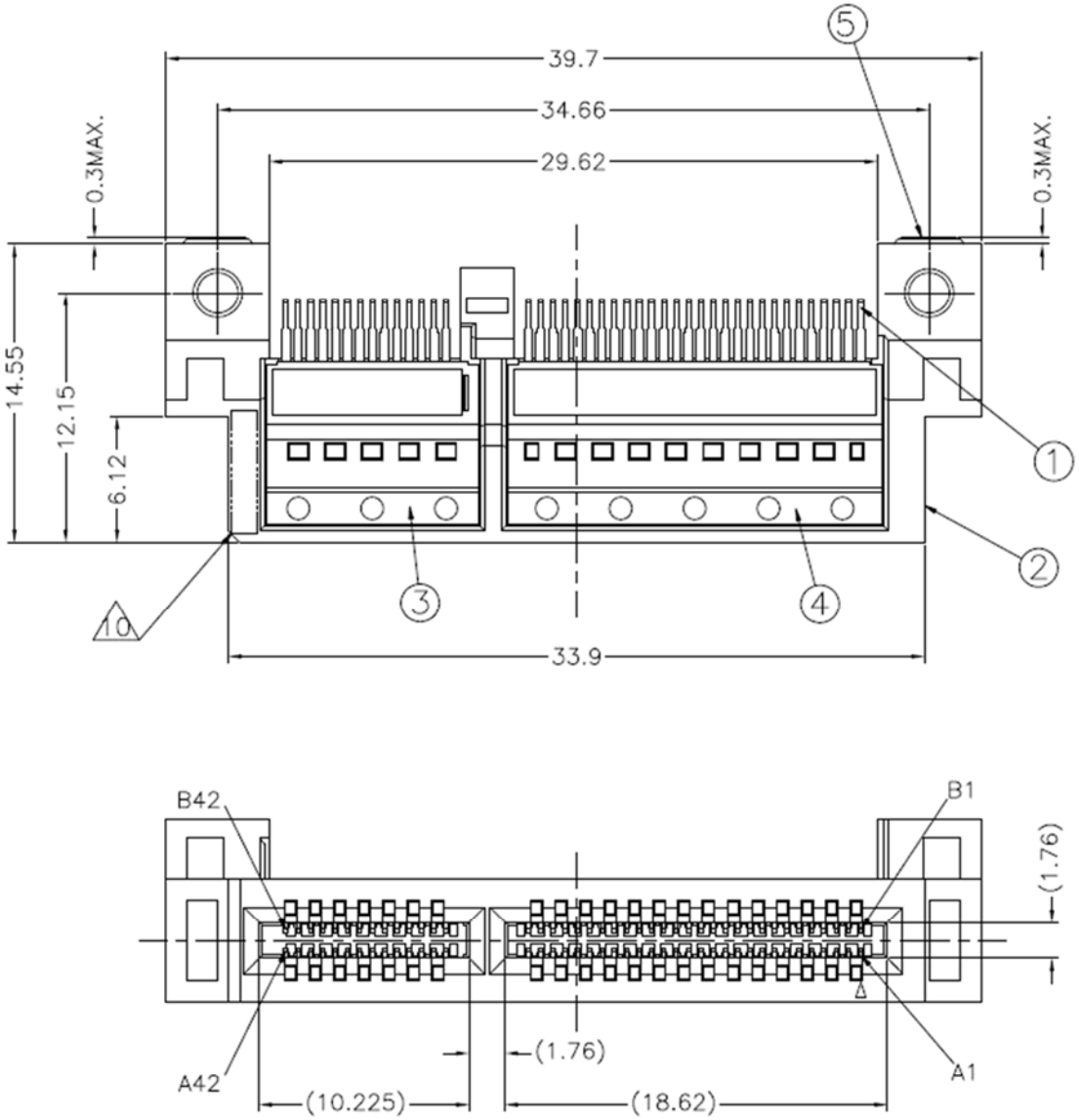
7.2.2 Blind Mate

The PCB (card edge) of the PMC module plugs into a 2C connector on the chassis side. For reference, this connector shall be a TE Sliver 2.0 Straddle Mount cable or PCB-mounted connector. This is TE 2340326-1 or equivalent, and can be customized for the particular power shelf. Please refer to the ORV3 Power Shelf specification for more details on this.


B42
B1
(1.76)
A42
(1.76)
A1
(10.225)
(18.62)


5
39.7
34.66
29.62
0.3MAX.
0.3MAX.
14.55
12.15
6.12
1
2
3
4
10
33.9


B42
B1
(1.76)
(1.76)
A42
A1
(10.225)
(18.62)



8. Serviceability

8.1 Required collateral

Shall include (at minimum) schematics, CAD, block diagrams, I2C diagram, Switch and jumper settings, service/repair/assembly/disassembly instructions (if applicable), LED definitions.

8.2 FRU information

FRU labels will include part number and serial number. FRU SEEPROM shall be per IPMI spec.

8.3 PCB information

PCBs shall have silkscreen markings for jumpers, LEDs, and FRUs.

8.4 LED Information

8.4.1 Power Status LED

One bi-color LED (blue and AMBER (602-610nm λD) LED shall be incorporated into the front face plate of equipment indicating the power-on, power-off & standby states as follows:

- Blue = power-on
- AMBER = Attention
- OFF = power-off

8.4.2 Management ethernet port LED

Two separate Blue LEDs shall be incorporated into the front face plate of equipment for each management Ethernet port to indicate activity and speed as follows:

1. ACTIVITY LED (left side of connector)
    - Solid blue = link established
    - Blinking blue = transmitting
2. SPEED LED (right side of connector)

Solid Blue = 1gbps

8.4.3 LED Visibility

All diagnostic LEDs shall be visible through the front panel

8.5 Port Symbols

The Management Ethernet connectors shall have the text “MGMT” printed on or the metal stamped “MGMT” near the dedicated network port and include appropriate pictogram, and Sideband RJ45 shall have the text “SB” printed on or the metal stamped “SB” near the dedicated network port and include appropriate pictogram.

8.6 Cold Aisle Repairs

PMC shall be serviced from the Cold Aisle

8.7 Programmable updates

Non-disruptive (no reboot required) update capability is required for all programmable devices. Utilities shall be provided by the Design Partner with the capability to up and down-rev each article of firmware in the equipment.

8.8 Additional Service Requirements

Additional Service requirements may be added based on Safety and Data Center requirements. Contact specification owner for latest requirements.

9. Thermal

9.1 Environmental (operational)

- Cold aisle (inlet) temperature: -5°C to 45°C
- Relative humidity: 10% to 90%, non-condensing
- Altitude: up to 3050m (10,000ft)
- Acoustic noise: If active cooling is required, target sound pressure should not exceed 85dBA when fan modules are running at full speed and operating within the defined environmental envelope.

9.2 Thermal requirements

- Operational
  - Thermal margin: Reserving adequate margins on components is critical. These margins should be defined with respect to de-rated values, as appropriate. Following are the requirements.
    - Component thermal margin of ≥7% or ≥5°C up to 30°C inlet/ambient and 3050m (10,000ft) above sea-level. Target whichever value is larger.
    - Component thermal margin of ≥4% or ≥3°C at greater than 30°C inlet/ambient and up to 3050m (10,000ft) above sea-level. Target whichever value is larger.
    - Margin to de-rated temperatures should account for associated differences in reading and measurement location. Impact to reliability should also be considered when determining required margin.
- Thermal kit
  - Sensor accuracy: For discrete and critical sensors (such as ambient temperature), an accuracy of ≤±2°C is required (≤±1°C is preferred). If a component does not have an integrated temperature sensor, and uses a proxy, need to target an accuracy ≤±5°C (≤±2°C is preferred). If this component is temperature sensitive, thermal margin requirements defined above should account for sensor inaccuracy.
  - System fan (if required): Should be sized to support operation across environmental and loading envelopes, with an adequate operating range (speed) to achieve requirements outlined in this document. The fan should also have adequate overhead to accommodate back-pressure resulting from shelf design, rack-level accessories and data center operation. In general, head room to overcome a back-pressure of ≥ 0.25 inches of water is highly recommended (placeholder value; to be verified and updated). This does not take in to account impedance created at the front of the shelf to entrain airflow in the PMC as needed. In addition, to ensure thermally-efficient operation, airflow greater than 5CFM should be avoided.
  - Surface temperature: To make the PMC safe for handling in-operation, accessible surfaces should not exceed a temperature of 70°C.

The PMC shall operate within a standard OCPv3 21” rack with 10degreesC - 35 degreesC ambient with no active cooling.

10. Compliance requirements

10.1 Safety Standards

Power/Battery Shelf Management Controller (PMC) shall be tested together in the OCP power shelf and shall comply with all safety requirements specified in OCP Open Rack V3 Power shelf and Battery shelf

Any component or signal that controls charging and discharging battery shall be evaluated under single fault condition per UL62368-1 Annex M

10.2 EMC Requirements

Power/Battery Shelf Management Controller (PMC) shall be tested together in the OCP power shelf and shall comply with all EMC requirements specified in OCP Open Rack V3 Power shelf document.

10.3 Environmental Compliance

Manufacturer of PMC shall provide full material disclosure, and technical documentations to demonstrate compliance to environmental compliance requirements such as ROHS, REACH, WEEE etc, depending on the end user's goals and business need.

10.4 Documentation

Power/Battery Shelf Management Controller (PMC) shall be covered under all documents specified in OCP Open Rack V3 Power shelf document.

11. Power Management Interface (PMI)

PMI is an extension module, which brings MODBUS of the PSU/BBUs directly out for upstream communication.

- Wiring from edge connector to RJ45 #3:

RJ45 #3		Edge connector
Pin	**Signal**	**Signal**
1	GND	GND
2	PLS_F	PLS
3	BKP_F	BKP
4	RS485A_F	RS485A_0 RS485A_1 RS485A_2 RS485A_3 RS485A_4 RS485A_5
5	RS485B_F	RS485B_0 RS485B_1 RS485B_2 RS485B_3 RS485B_4 RS485B_5
6	RS485_Addr2_F	RS485_Addr2
7	RS485_Addr1_F	RS485_Addr1
8	RS485_Addr0_F	RS485_Addr0

- Wiring from edge connector to RJ45 #4: ISHARE, SYNC_START, VOUT_SEL, and GND are connected directly.
- RJ45 #1 and RJ45 #2 connector pins get the same signals as RJ45 #3, with the exception of pin 6 of RJ45 #2, which should be grounded.