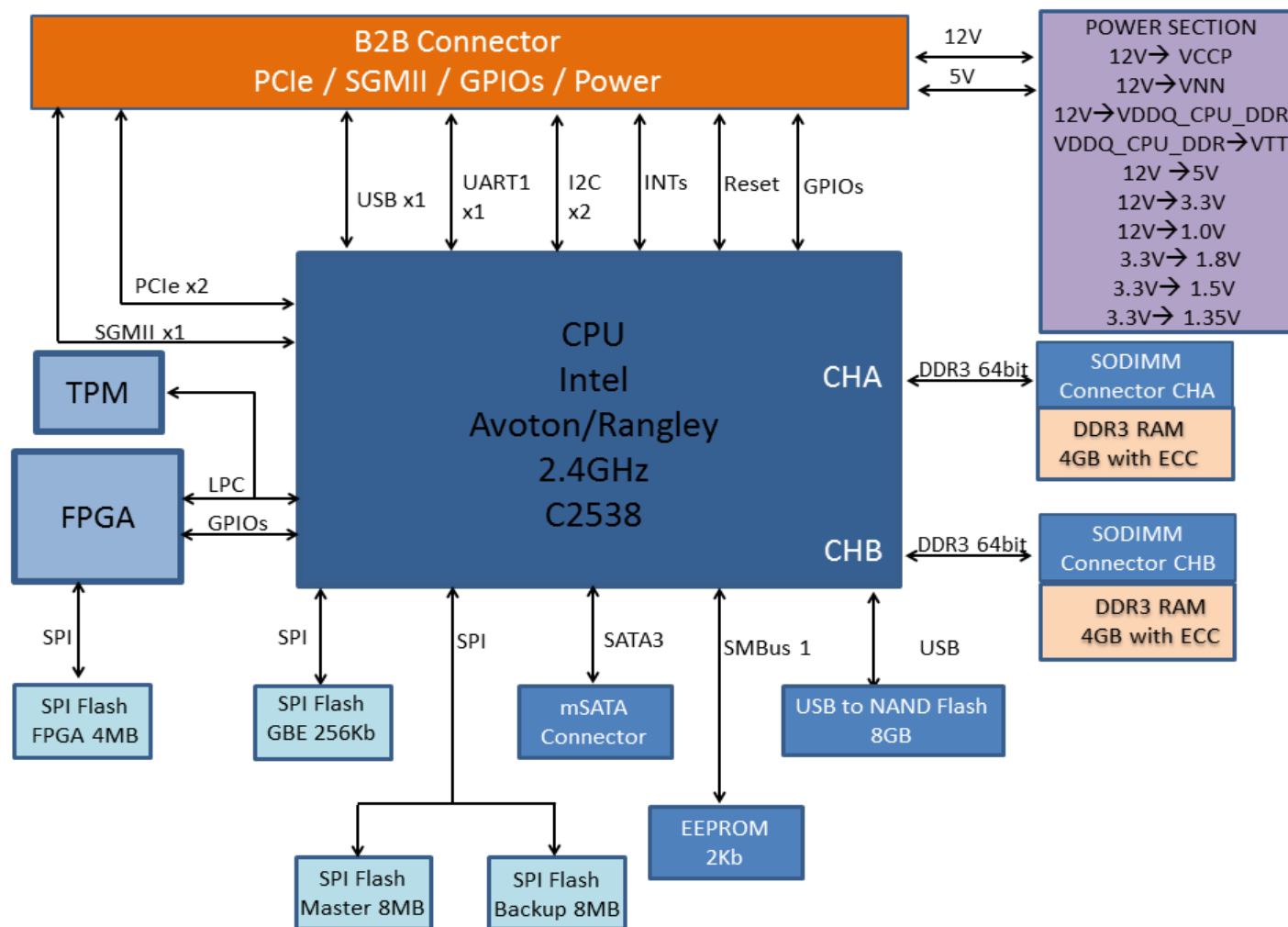


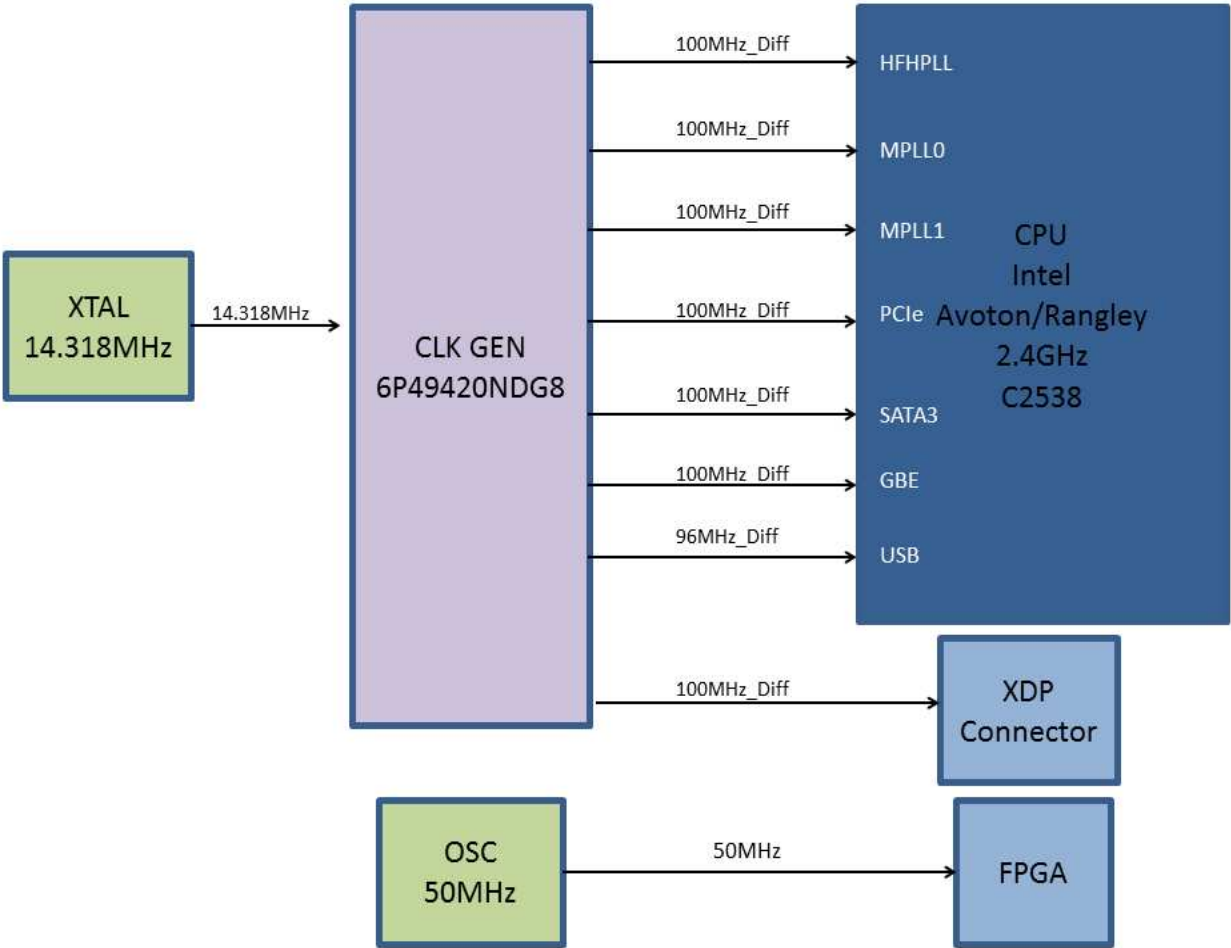
## Table of Contents

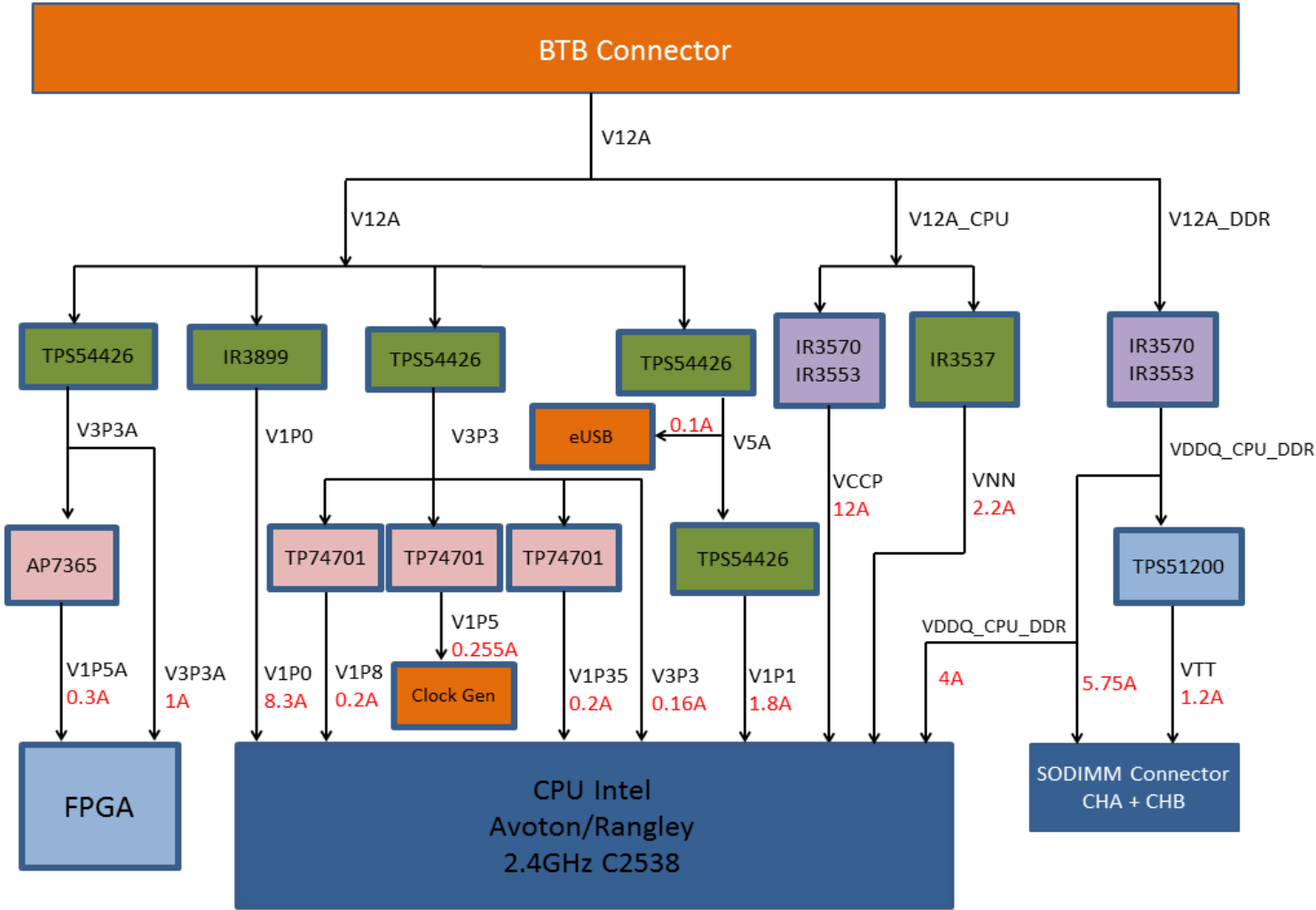
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3	Block Diagram	20	DDR3 SODIMM_CH1
4	Clock Tree	21	XDP_PORT80 Debug
5	Power Tree	22	SPI_SCREW_HS_RPCAP
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14	Rangeley SATA,USB,MISC	31	V5A_V3P3
15	Rangeley Power	32	LDO_V1P8_V1P5_V1P35_V1P5A
16	Rangeley Power	33	Debug LED
17	Rangeley Power_GND		

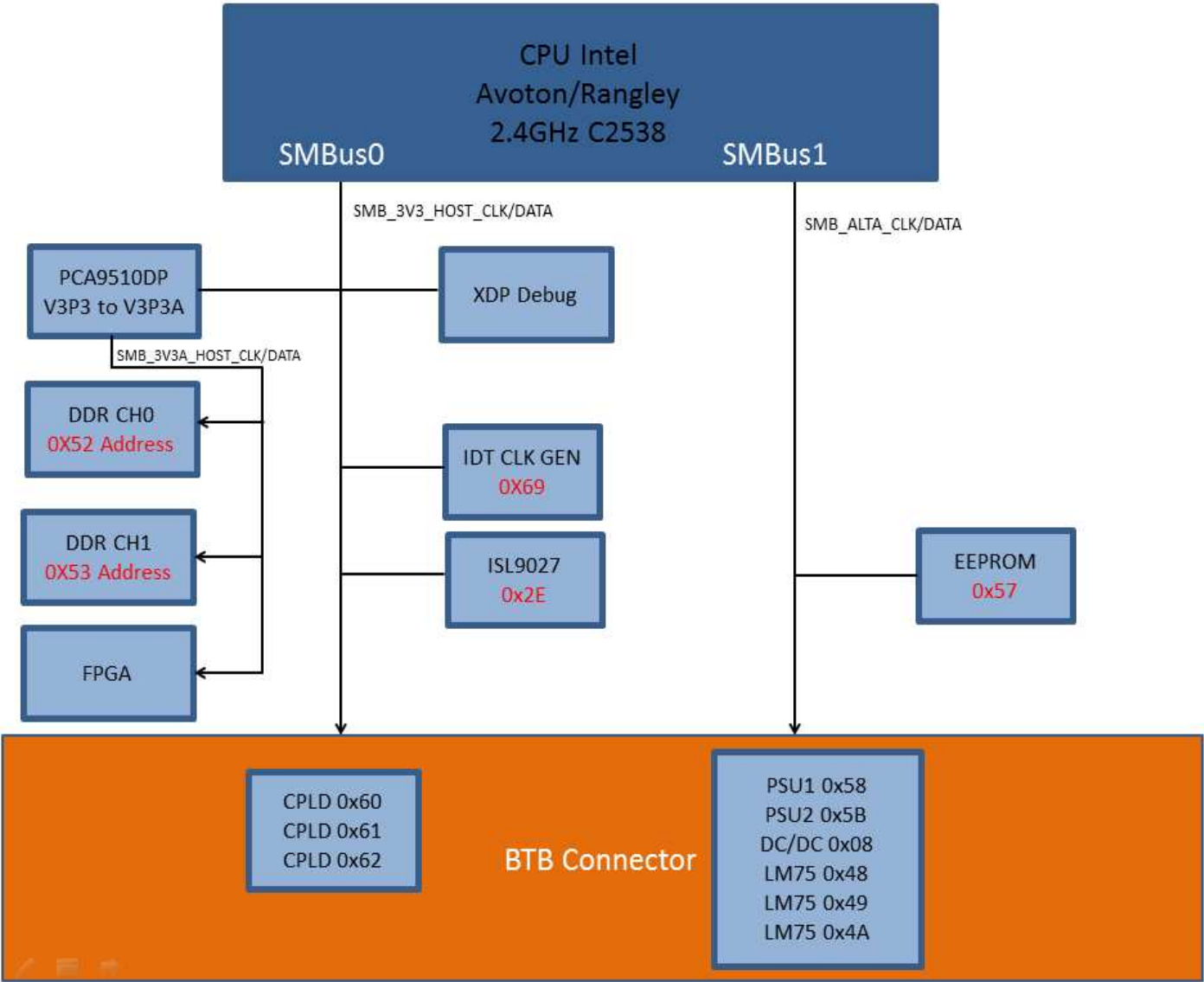
# History

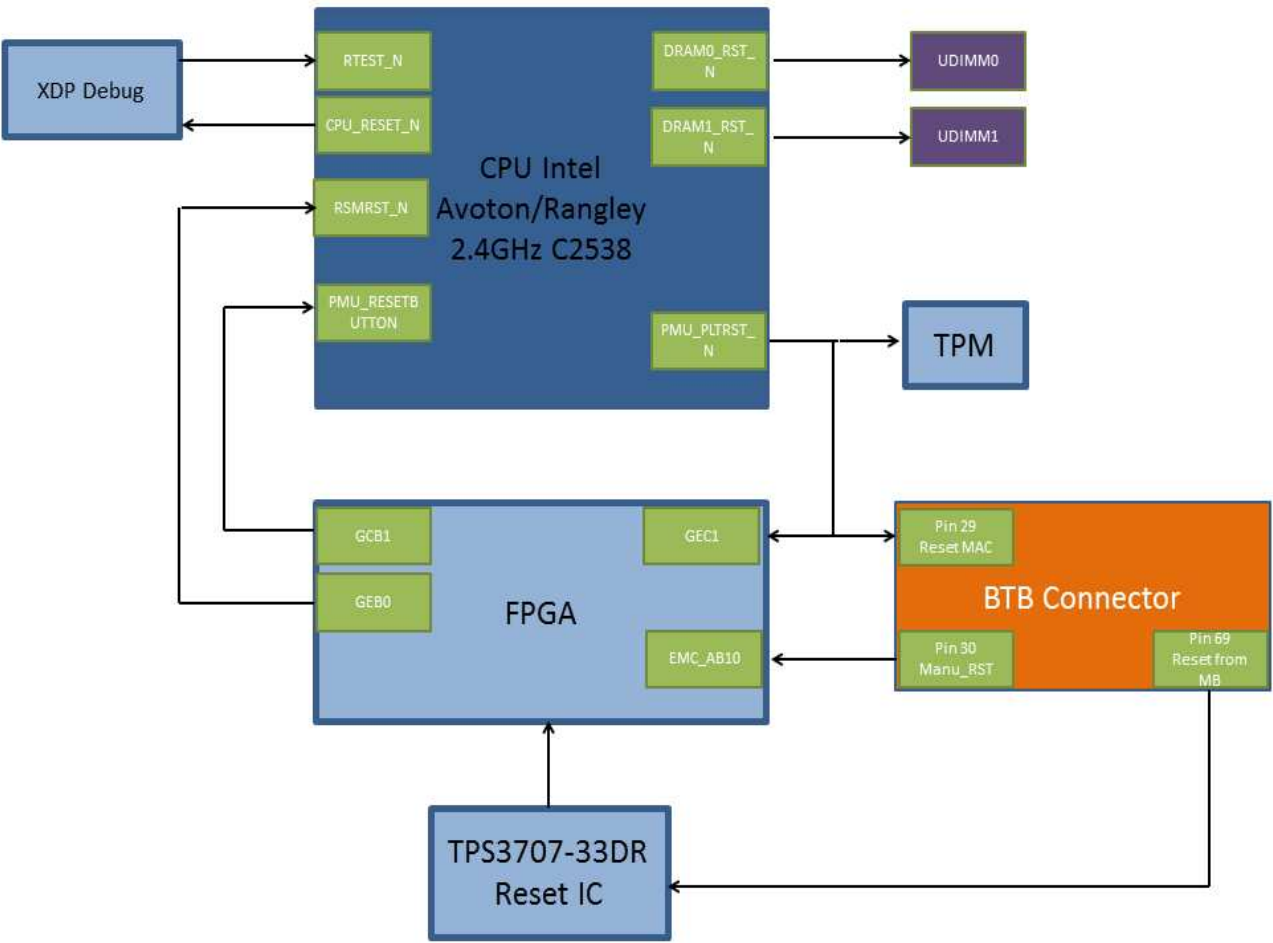
SCH Version	Date	Description
R0A	2014/03/05	Initial Version
R01	2014/06/30	Release to MP

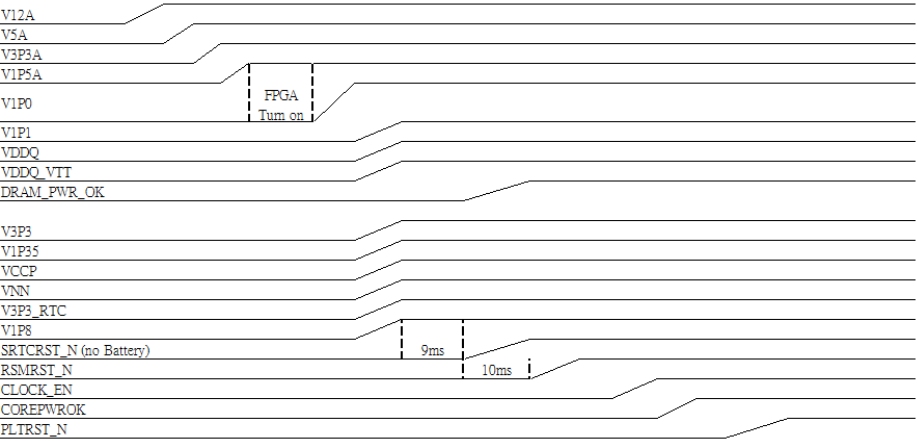








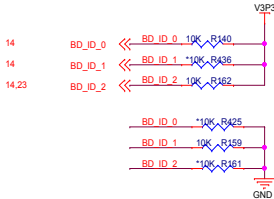






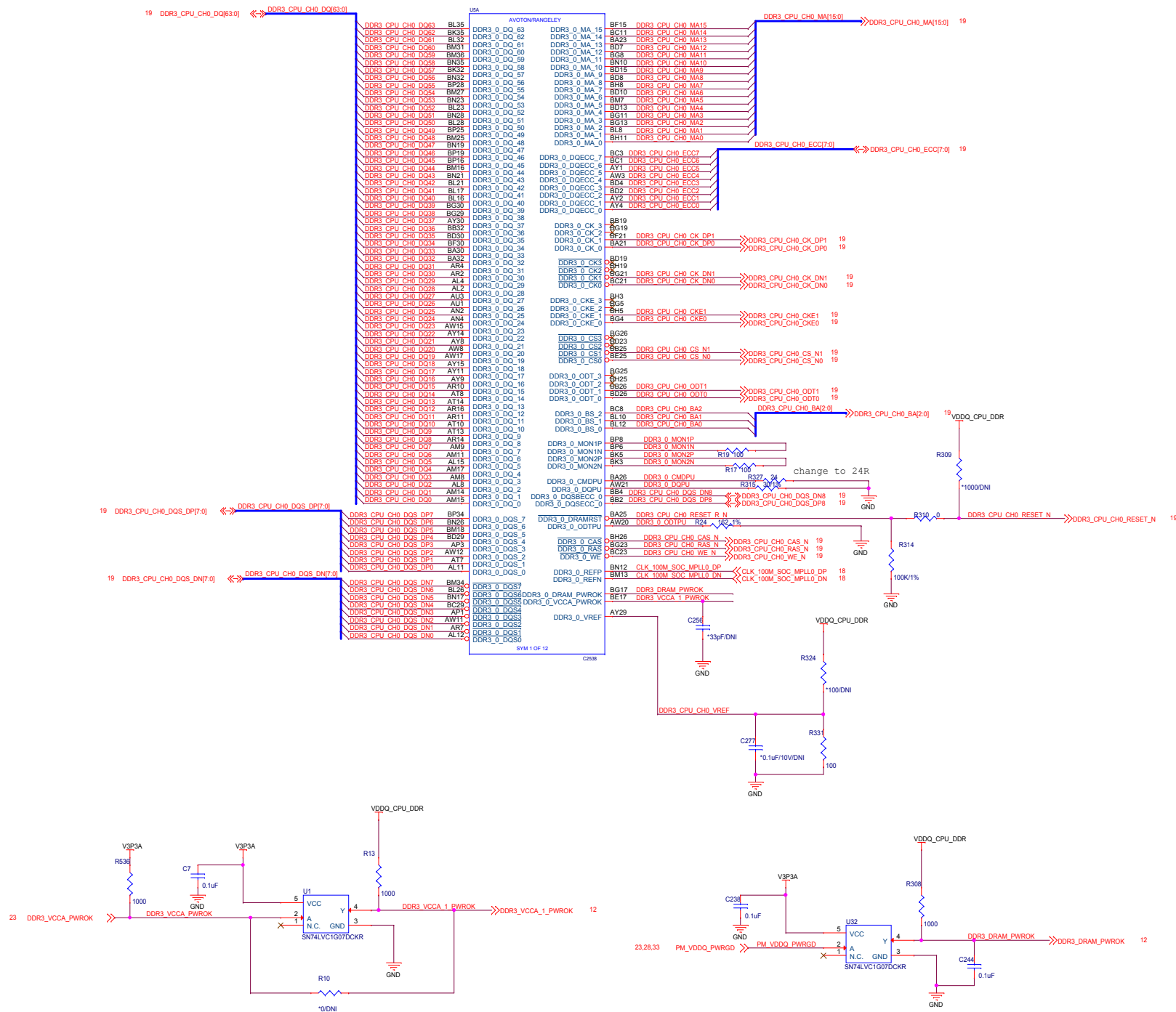
GPIOs	Pin#	Alternate Function	Rangeley Configuration
GPIO_0	AL56	NMI	Alternate Function
GPIO_1	AL63	ERROR2_B	Alternate Function
GPIO_2	AL62	ERROR1_B	Alternate Function
GPIO_3	AL65	ERROR0_B	Alternate Function
GPIO_4	AM52	IRERR_B	Alternate Function
GPIO_5	AL52	MCERR_B	Alternate Function
GPIO_6	AG50	UART1_RXD	Alternate Function
GPIO_7	AH50	UART1_TXD	Alternate Function
GPIO_8	AN62	SMB_CLK0	Alternate Function
GPIO_9	AP62	SMB_DATA0	Alternate Function
GPIO_10	AL58	SMB_ALRT_N0	Alternate Function
GPIO_11	AN63	SMB_DATA1	Goes to Mainboard
GPIO_12	AR63	SMB_CLK1	Goes to Mainboard
GPIO_13	AN65	SMB_DATA2	UART0_TXD
GPIO_14	AR65	SMB_CLK2	UART0_RXD
GPIO_15	AT63	SATA_GPO	BD_ID_0
GPIO_16	AL49	SATA_LEDN	N/A
GPIO_17	AH51	SATA3_GPO	BD_ID_1
GPIO_18	AH54	SATA3_LEDN	Alternate Function
GPIO_19	AH59	FLEX_CLK_SBD	Alternate Function
GPIO_20	AG56	FLEX_CLK_SE1	Alternate Function
GPIO_21	AG54	LPC_LAD0	Alternate Function
GPIO_22	AM53	LPC_LAD1	Alternate Function
GPIO_23	AL53	LPC_LAD2	Alternate Function
GPIO_24	AG59	LPC_LAD3	Alternate Function
GPIO_25	AH56	LPC_FRAMEB	Alternate Function
GPIO_26	AG51	LPC_CLKOUT0	Alternate Function
GPIO_27	AM49	LPC_CLKOUT1	Alternate Function
GPIO_28	AH48	LPC_CLKRUNB	Alternate Function
GPIO_29	AT50	ILB_SERIRQ	Alternate Function
GPIO_30	AM58	PMU_RESETBUTTON_B	Alternate Function

GPIOs	Pin#	Alternate Function	Rangeley Configuration
GPIO_SUS0	V66	N/A	ALTA_CPLD_TCK
GPIO_SUS1	W54	N/A	ALTA_CPLD_TDI
GPIO_SUS2	T53	N/A	BD_ID_2
GPIO_SUS3	Y63	CPU_RESET_B	Alternate Function
GPIO_SUS4	Y57	SUSPWRDNACK	N/A ; pull up
GPIO_SUS5	AD58	PMU_SUSCLK	N/A
GPIO_SUS6	AC52	PMU_SLP_DDRVTT_B	Goes to FPGA, Output
GPIO_SUS7	Y50	PMU_SLP_LAN_B	Goes to FPGA, Output
GPIO_SUS8	AD66	PMU_WAKE_B	Alternate Function
GPIO_SUS9	AC49	PMU_PWRBTN_B	Alternate Function
GPIO_SUS10	AB65	SUS_STAT_B	N/A, pull down
GPIO_SUS11	AD63	USB_OC0_B	Alternate Function
GPIO_SUS12	AC58	SPL_CS1_B	Alternate Function
GPIO_SUS13	W51	GBE_EE_DI	Alternate Function
GPIO_SUS14	W60	GBE_EE_DO	Alternate Function
GPIO_SUS15	T50	GBE_EE_SK	Alternate Function
GPIO_SUS16	R59	GBE_EE_CS	Alternate Function
GPIO_SUS17	T58	GBE_SDP0_0	CPLD_INT_L
GPIO_SUS18	T48	GBE_SDP0_1	CPLD2_INT_L
GPIO_SUS19	P46	GBE_LED0	N/A, pull down
GPIO_SUS20	W50	GBE_LED1	N/A, pull down
GPIO_SUS21	P48	GBE_LED2	N/A, pull down
GPIO_SUS22	R58	GBE_LED3	N/A, pull down
GPIO_SUS23	V63	GBE_WOL	N/A, pull down
GPIO_SUS24	W56	GBE_MDIO0_I2C_CLK	MDIO0_CLK
GPIO_SUS25	W59	GBE_MDIO0_I2C_DATA	MDIO0_DATA
GPIO_SUS26	Y54	GBE_MDIO1_I2C_CLK	ALTA_CPLD_TDO
GPIO_SUS27	Y53	GBE_MDIO1_I2C_DATA	ALTA_CPLD_TMS

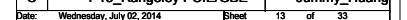


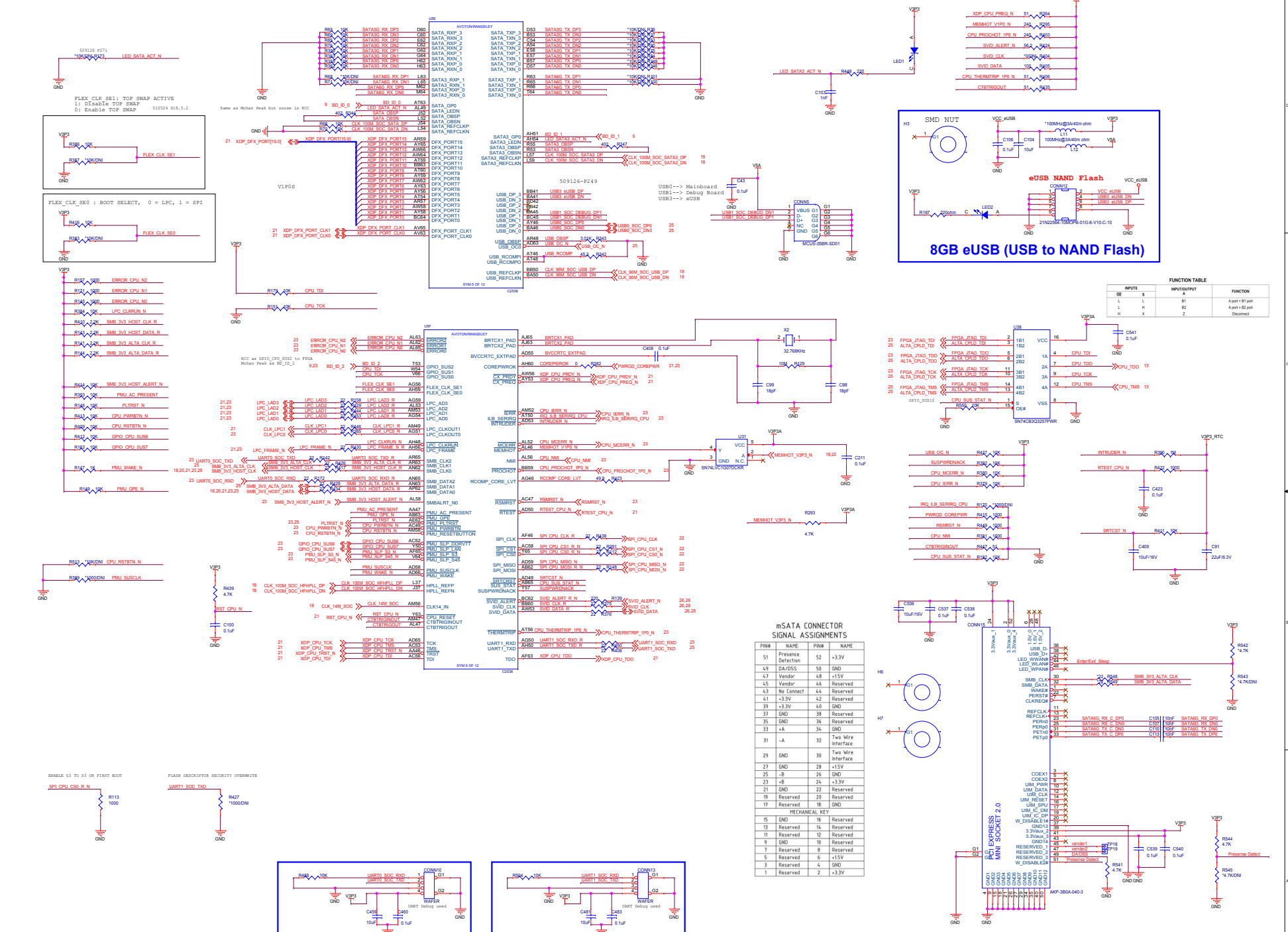
Board assignments			
BD_ID_2	BD_ID_1	BD_ID_0	Board Type
0	0	0	Lyon Peak SV
0	0	1	Lyon Peak BDV
0	1	0	Lyon Peak PPV
1	0	0	Mohon Peak
1	0	1	Intel Project 2
1	1	0	Tiger Cove

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FUNCTION TABLE		
DE	INPUT/OUTPUT	FUNCTION
B	B	A port = B1 port
L	L	A port = B1 port
R	R	A port = B1 port
H	H	A port = B1 port

mSATA CONNECTOR SIGNAL ASSIGNMENTS

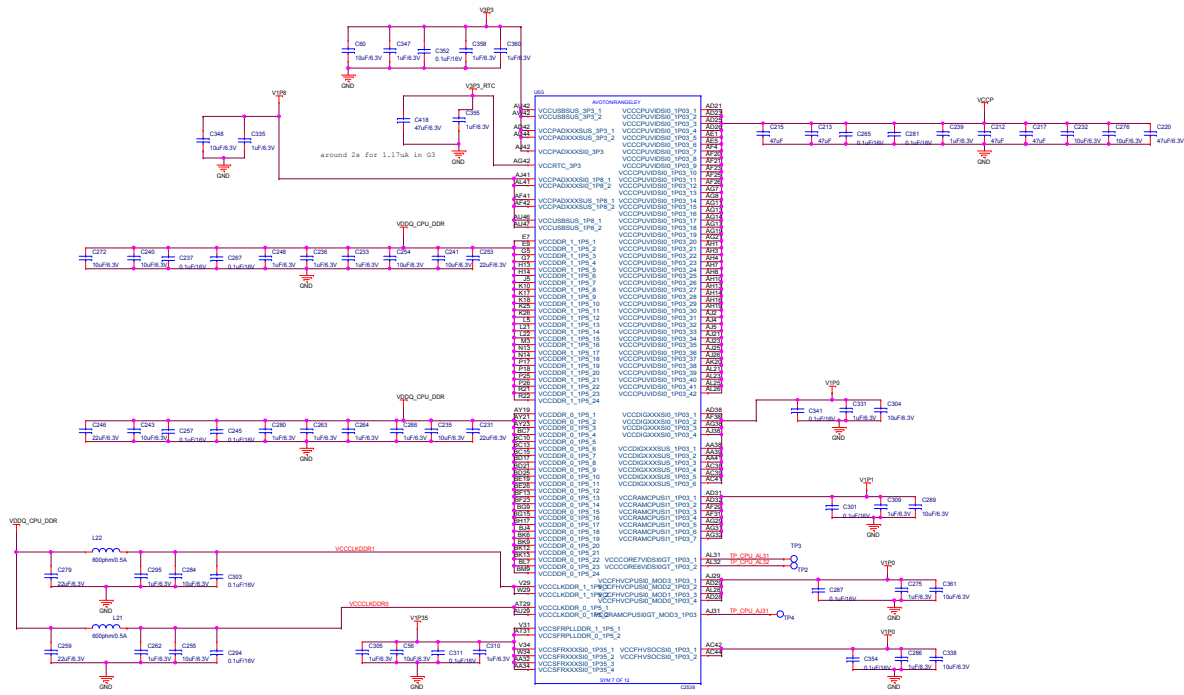
NAME	NAME	NAME
51 Presence Detection	52 +3.3V	
49 DA/DESS	48 +1.5V	
47 Vendor	46 Reserved	
45 Vendor	44 Reserved	
43 No Connect	42 Reserved	
41 +3.3V	40 Reserved	
39 +3.3V	38 Reserved	
37 GND	36 Reserved	
35 GND	34 GND	
33 +A	32 Two Wire Interface	
31 -A	30 Two Wire Interface	
29 GND	28 +1.5V	
27 GND	26 +3.3V	
25 +B	24 +3.3V	
23 +B	22 Reserved	
21 GND	20 Reserved	
19 Reserved	18 Reserved	
17 Reserved	16 Reserved	
15 GND	14 Reserved	
13 Reserved	12 Reserved	
11 Reserved	10 Reserved	
9 GND	8 Reserved	
7 Reserved	6 +1.5V	
5 Reserved	4 GND	
3 Reserved	2 +3.3V	
1 Reserved		

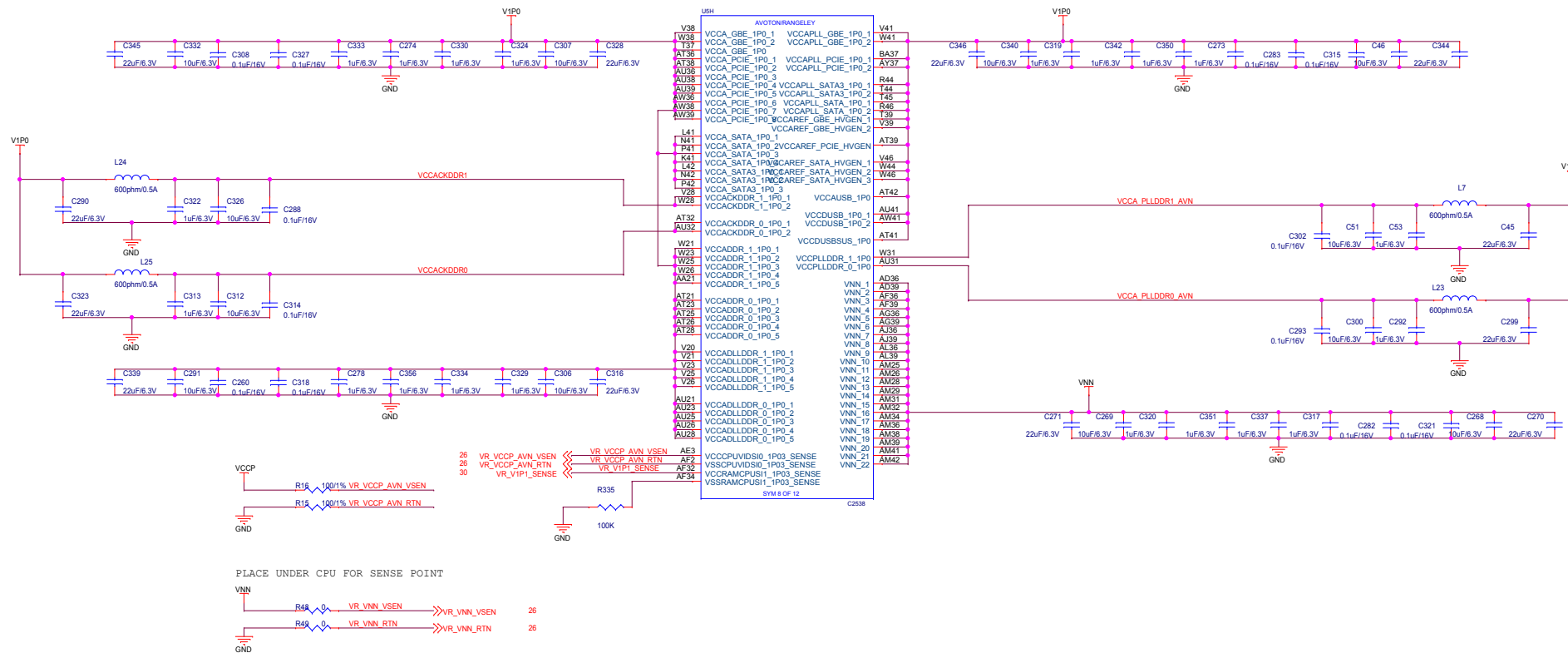
Reserve Console

Debug Console (CPU to Mainboard)

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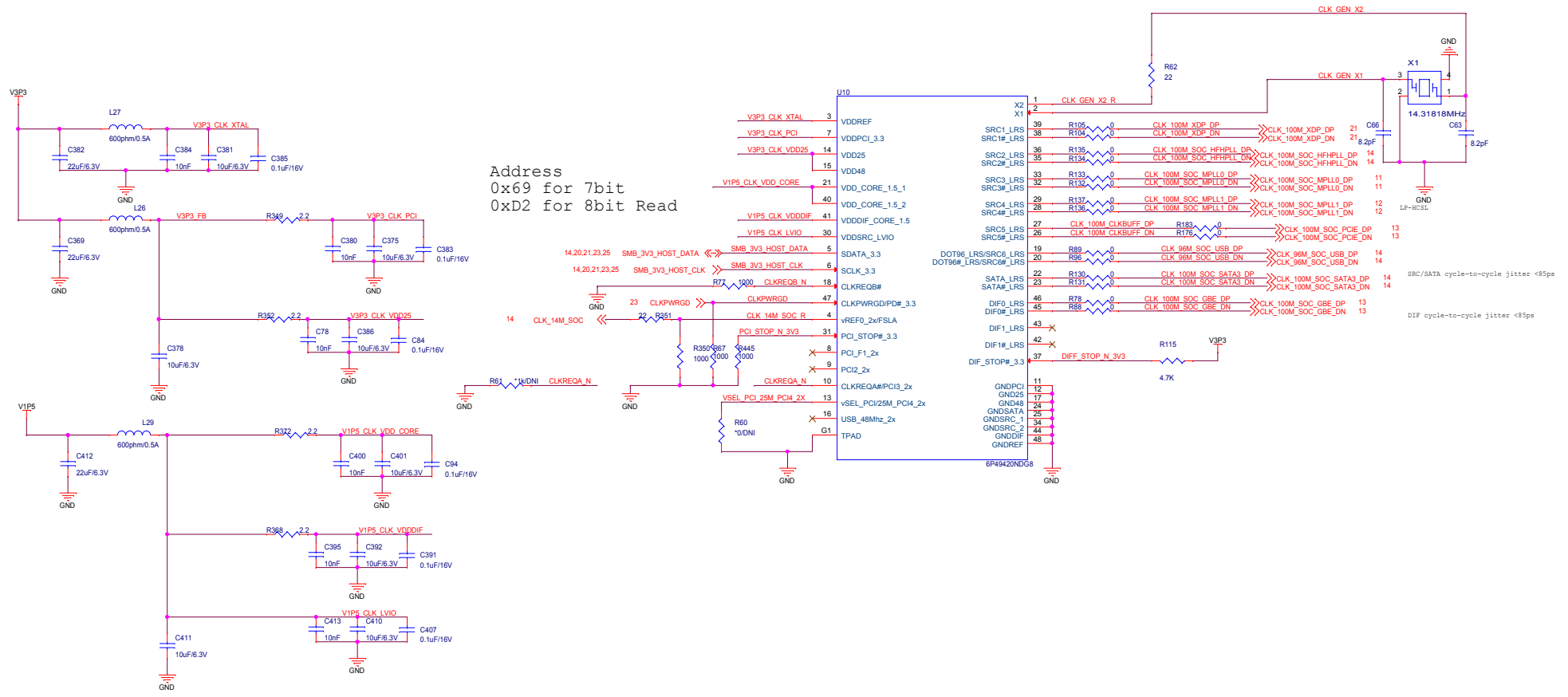
Model Name	ES0648T2-CPU-FLF-ZZ	Rev	R01
Pin Name	Custom P14_Rangeley SATA,USB,MS	Engineer	Kummy_Huang
Date	Wednesday, May 12, 2014	Page	14 of 31

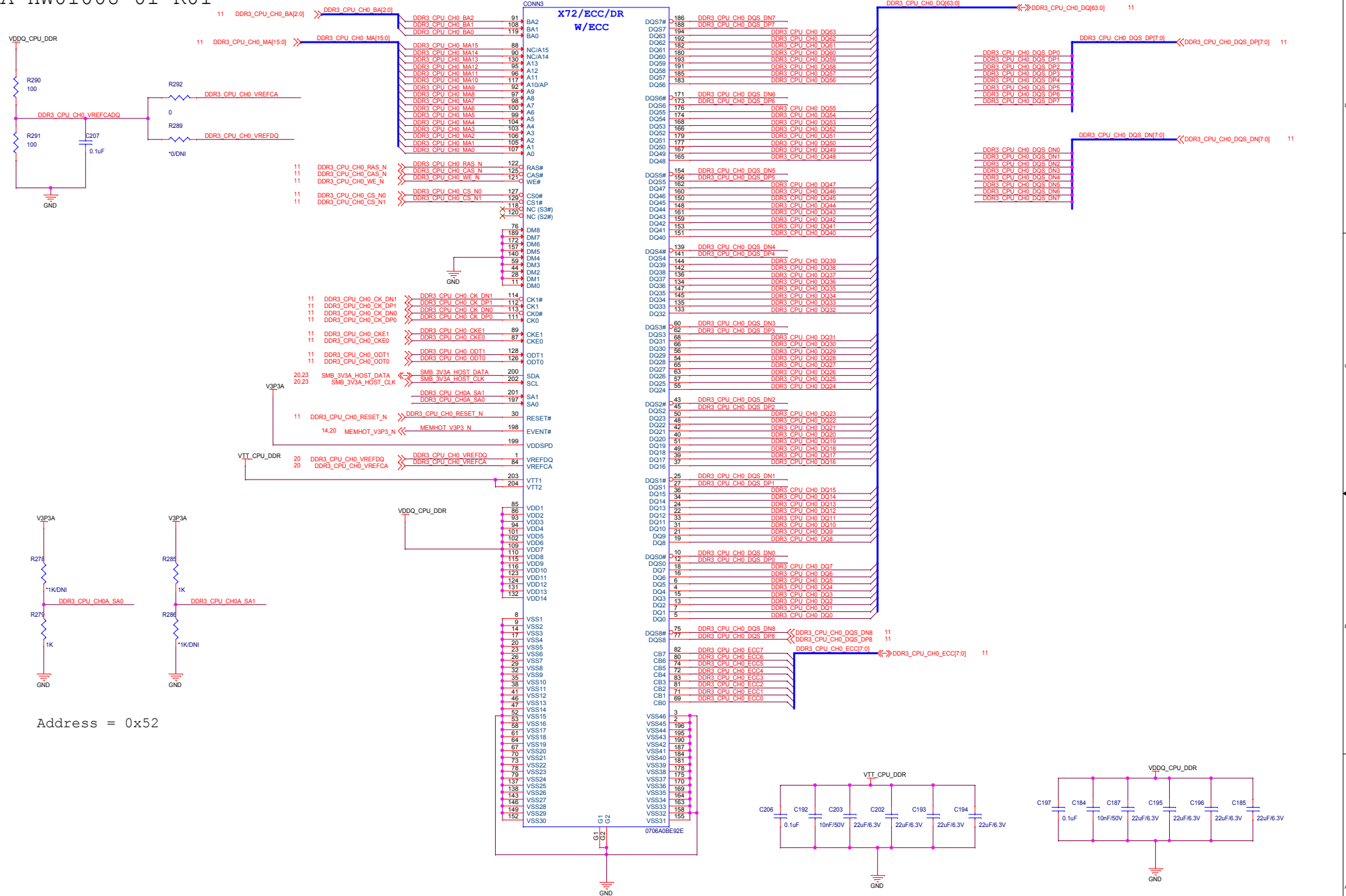






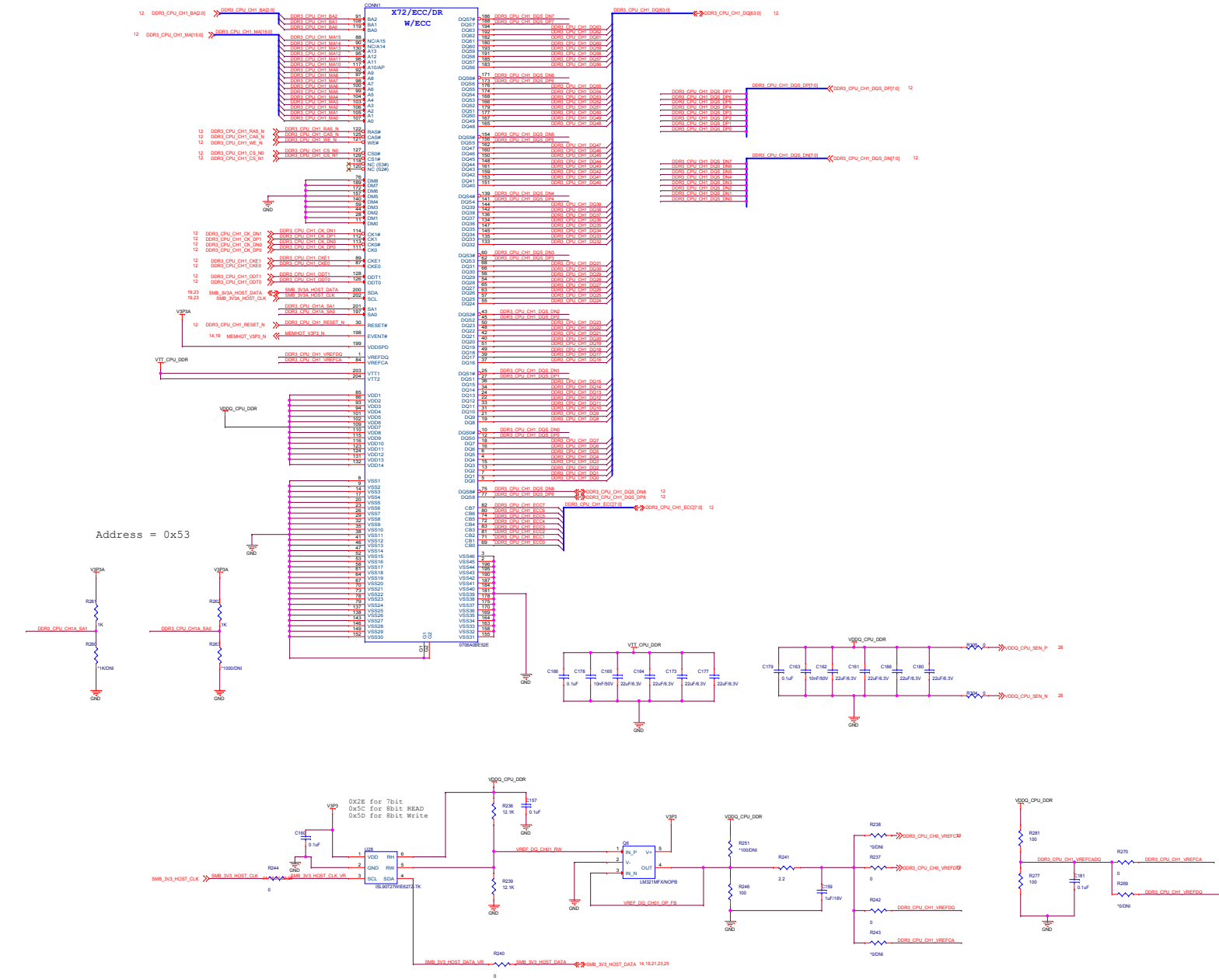


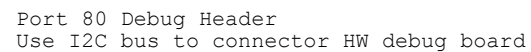
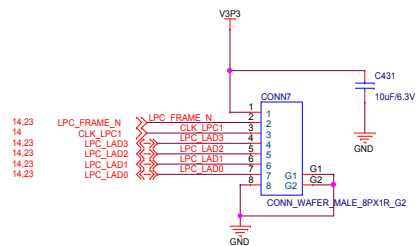
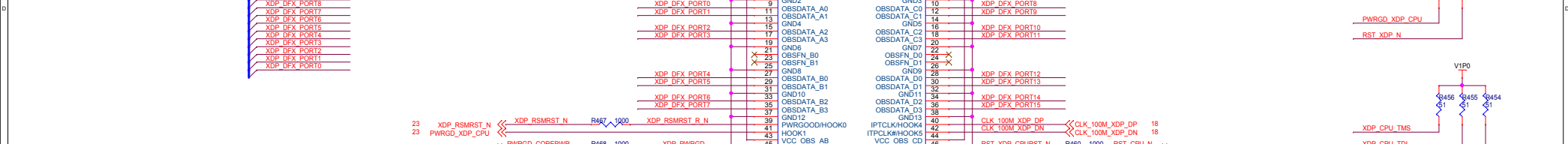


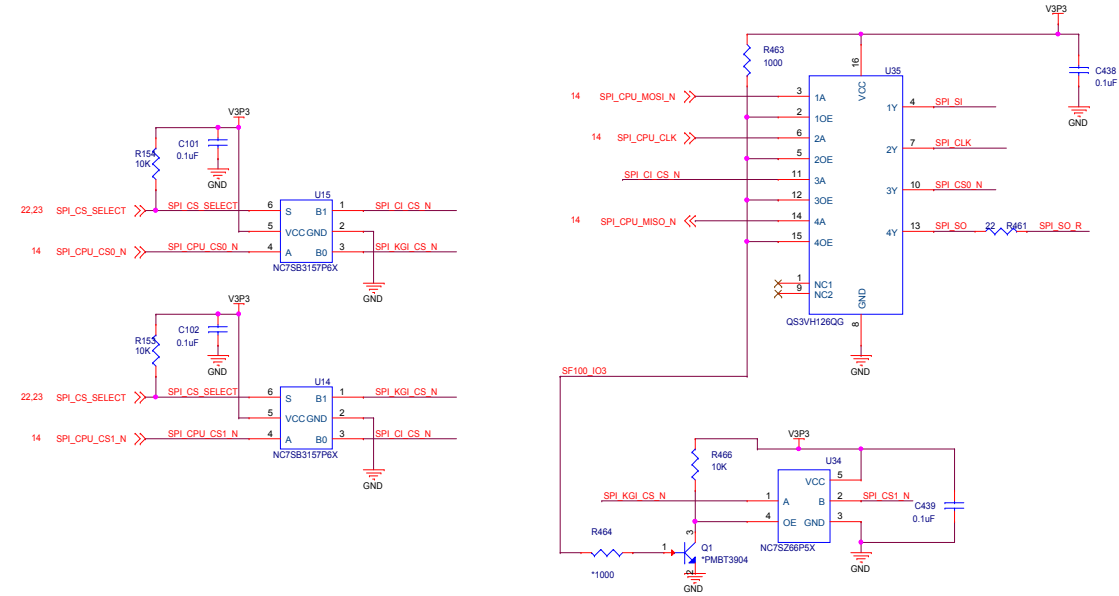
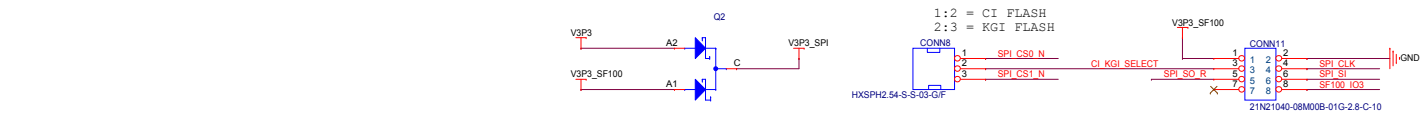
$$H=9.2\text{mm}$$


Address = 0x52

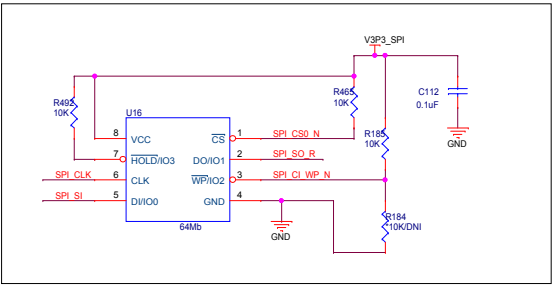
H = 5.2mm



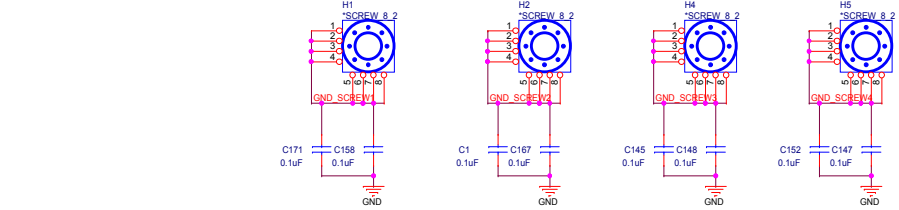
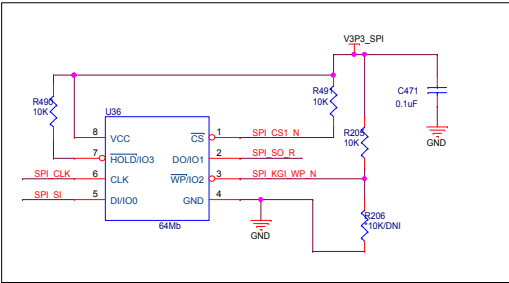




SPI CI Flash



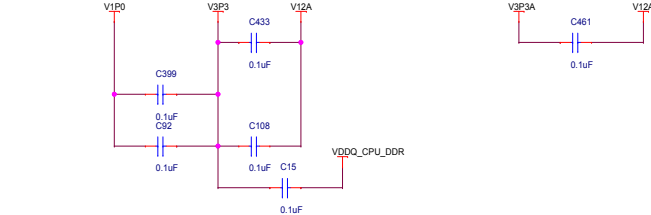
SPI KGI Flash

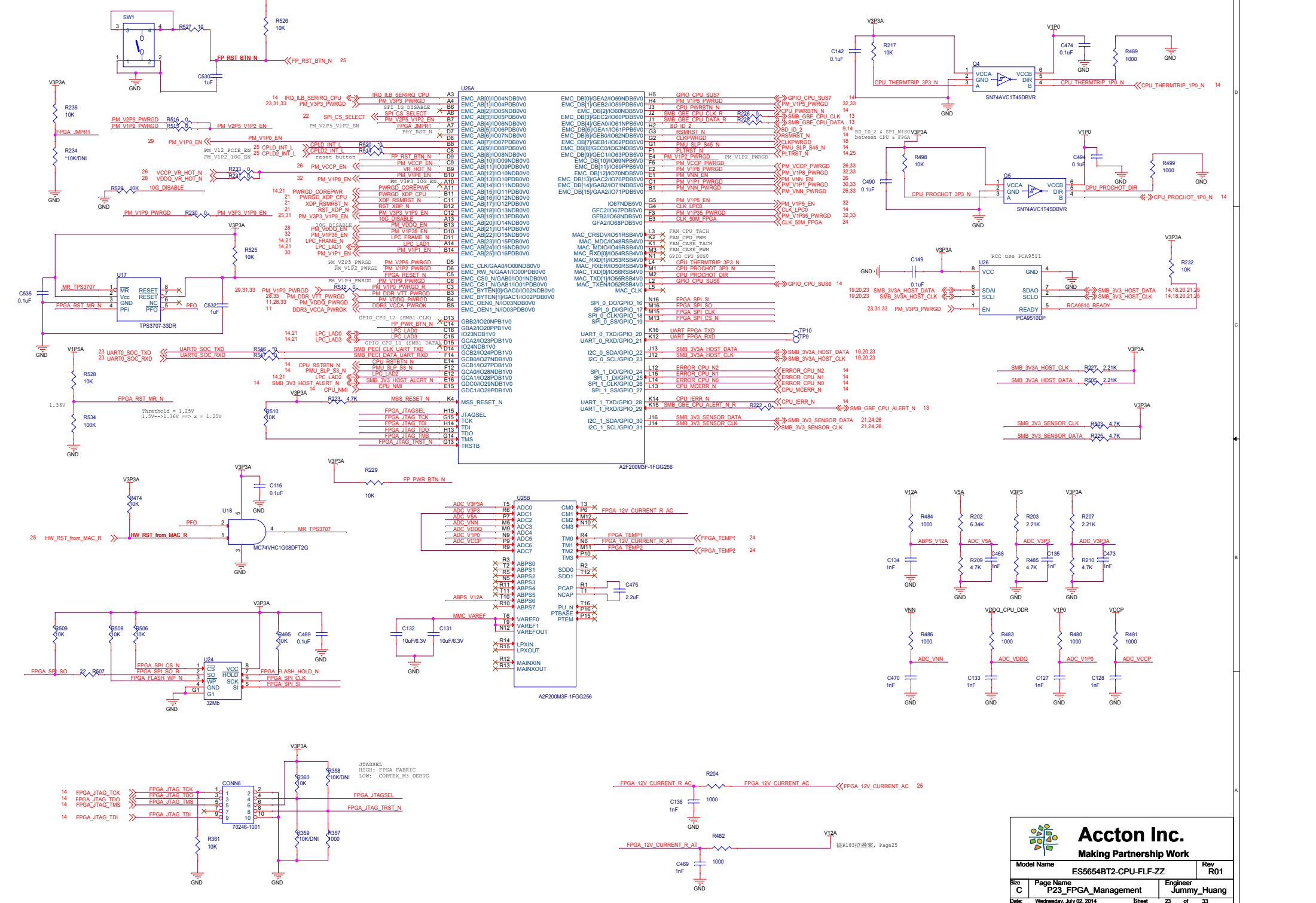


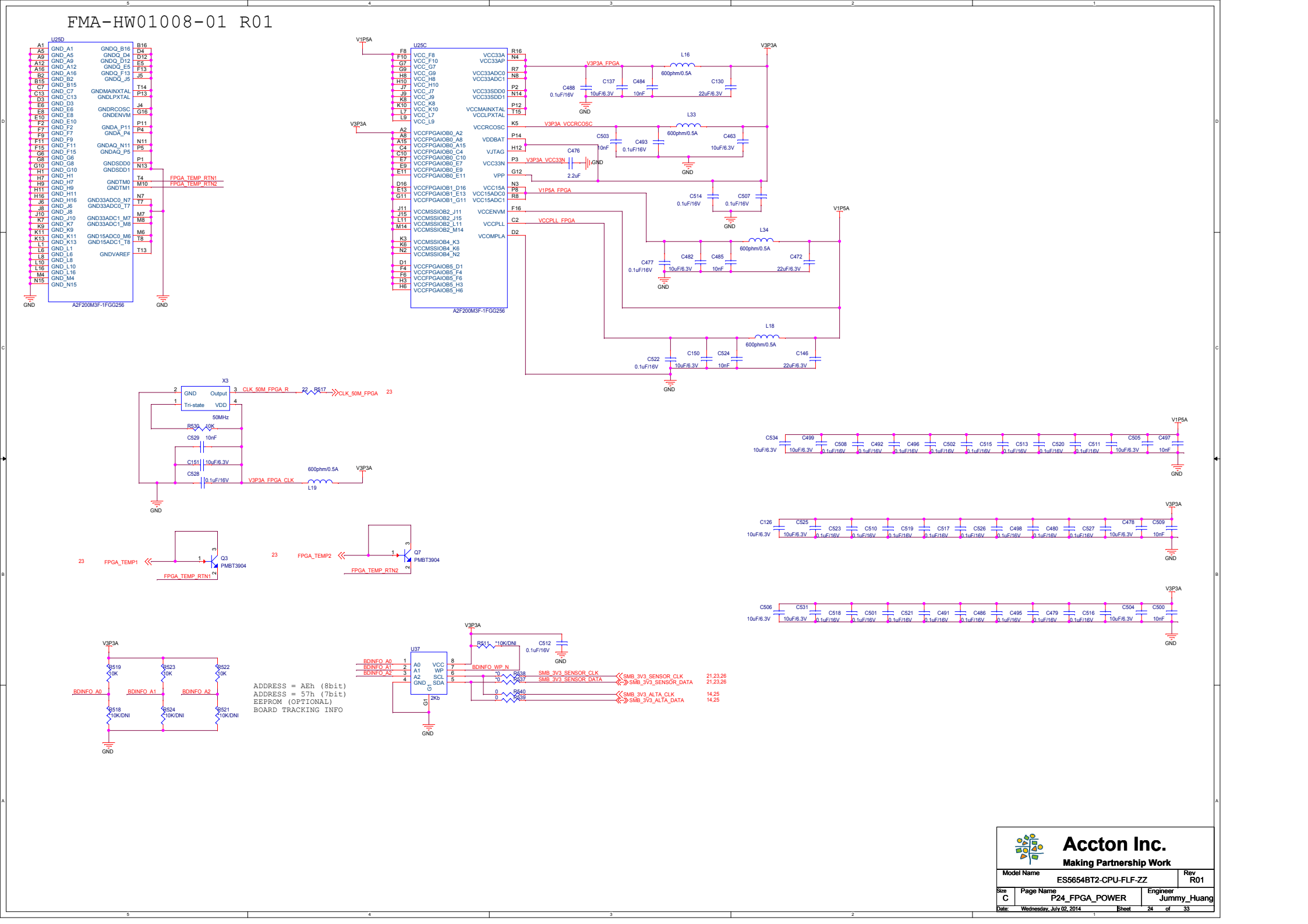
CPU Heatsink



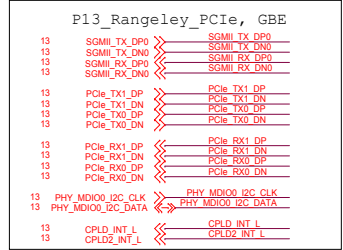
Change to 50mmx50mmx14mm



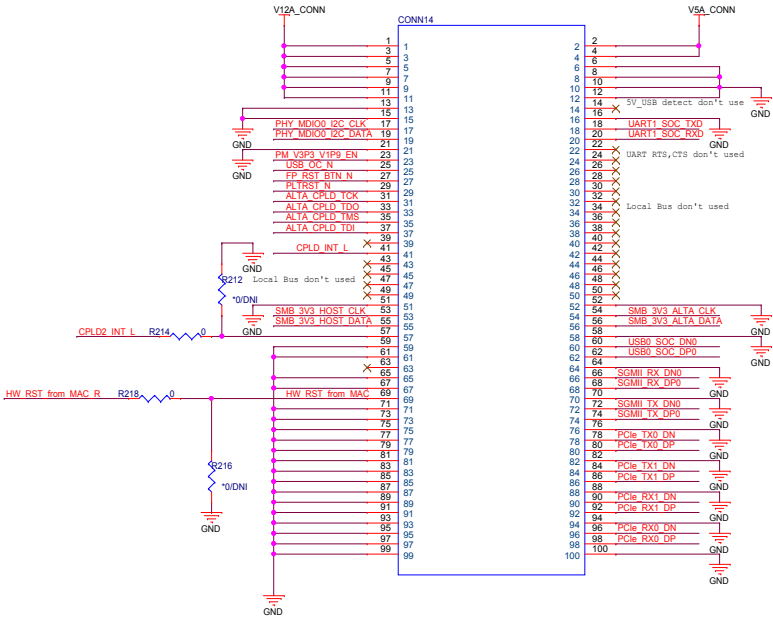
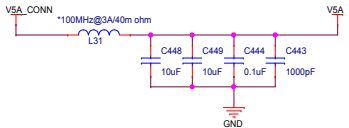
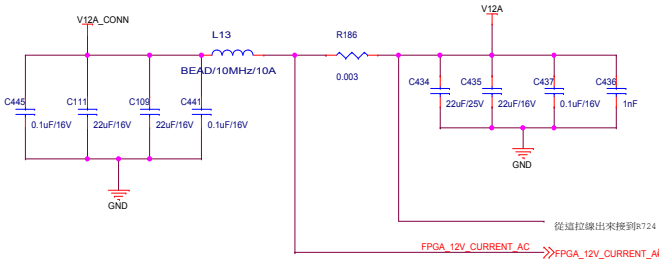
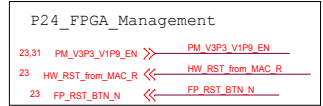
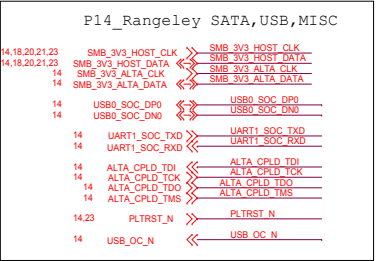


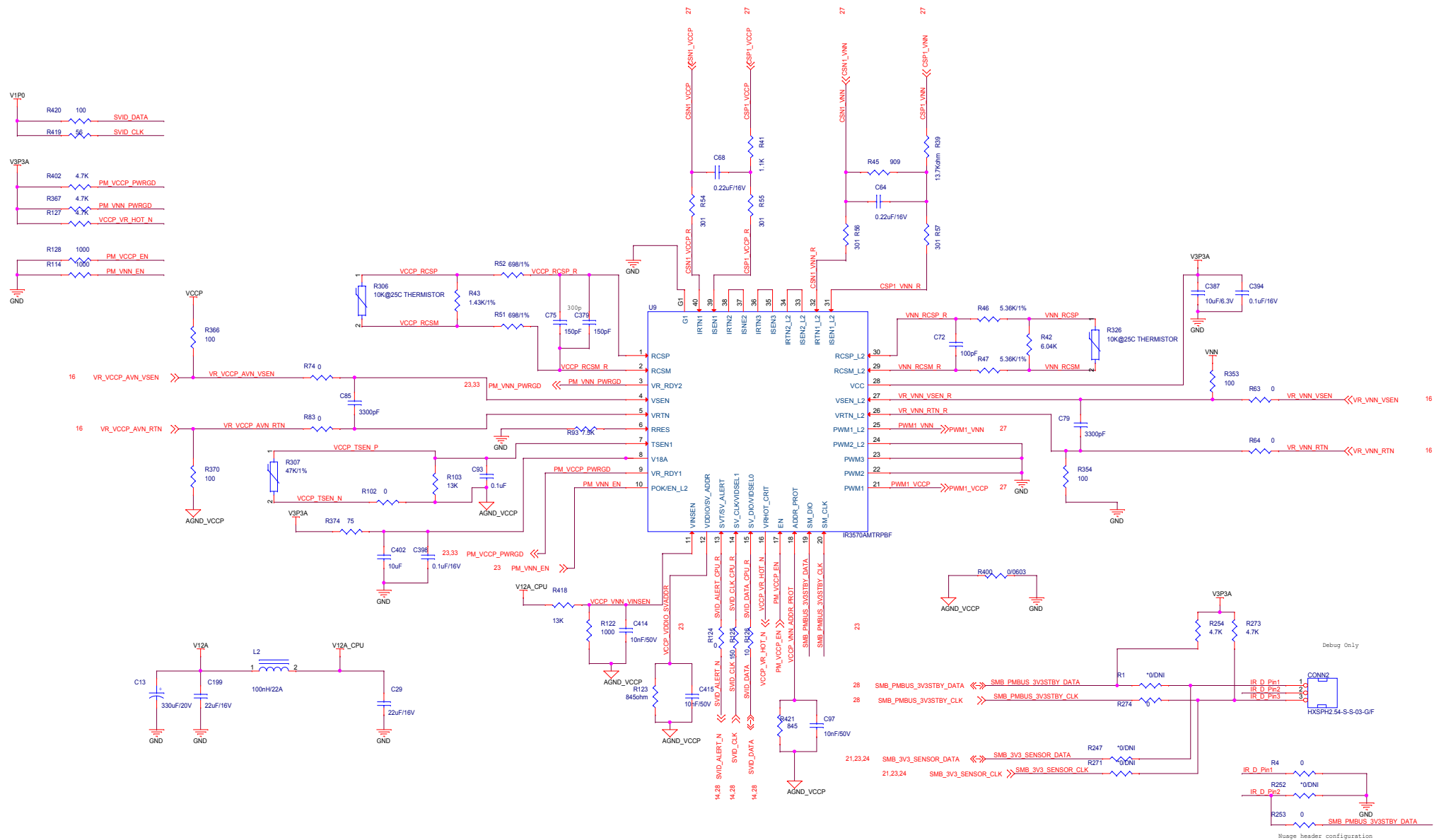


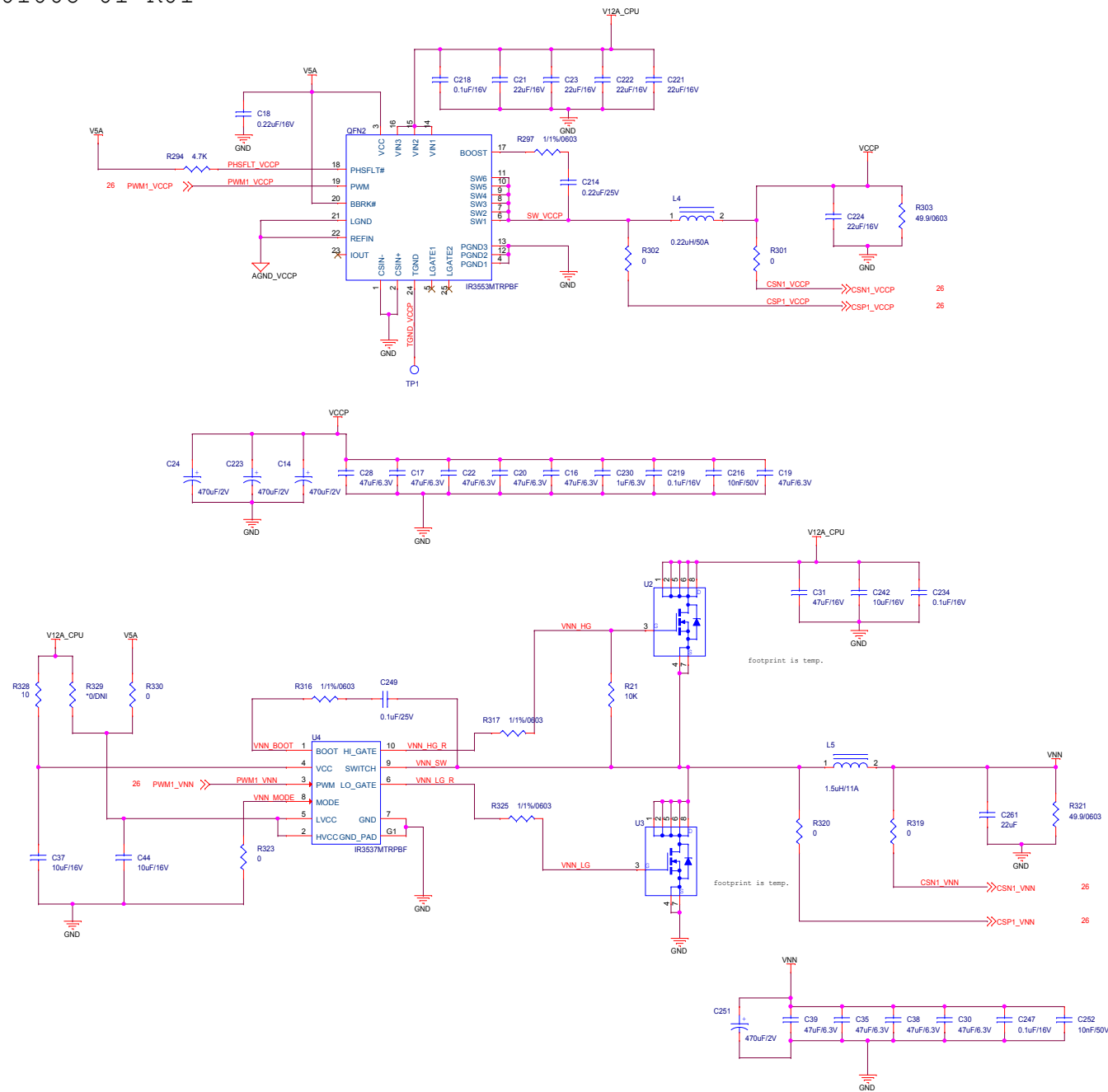




Resistor	96+0	96+8	48+6	32x40
R467	DI (Yes)	DNI (NO)	DNI (NO)	DNI (NO)
R495	DI (Yes)	DNI (NO)	DNI (NO)	DNI (NO)
R476	DNI (NO)	DI (Yes)	DI (Yes)	DI (Yes)
R477	DNI (NO)	DI (Yes)	DI (Yes)	DI (Yes)





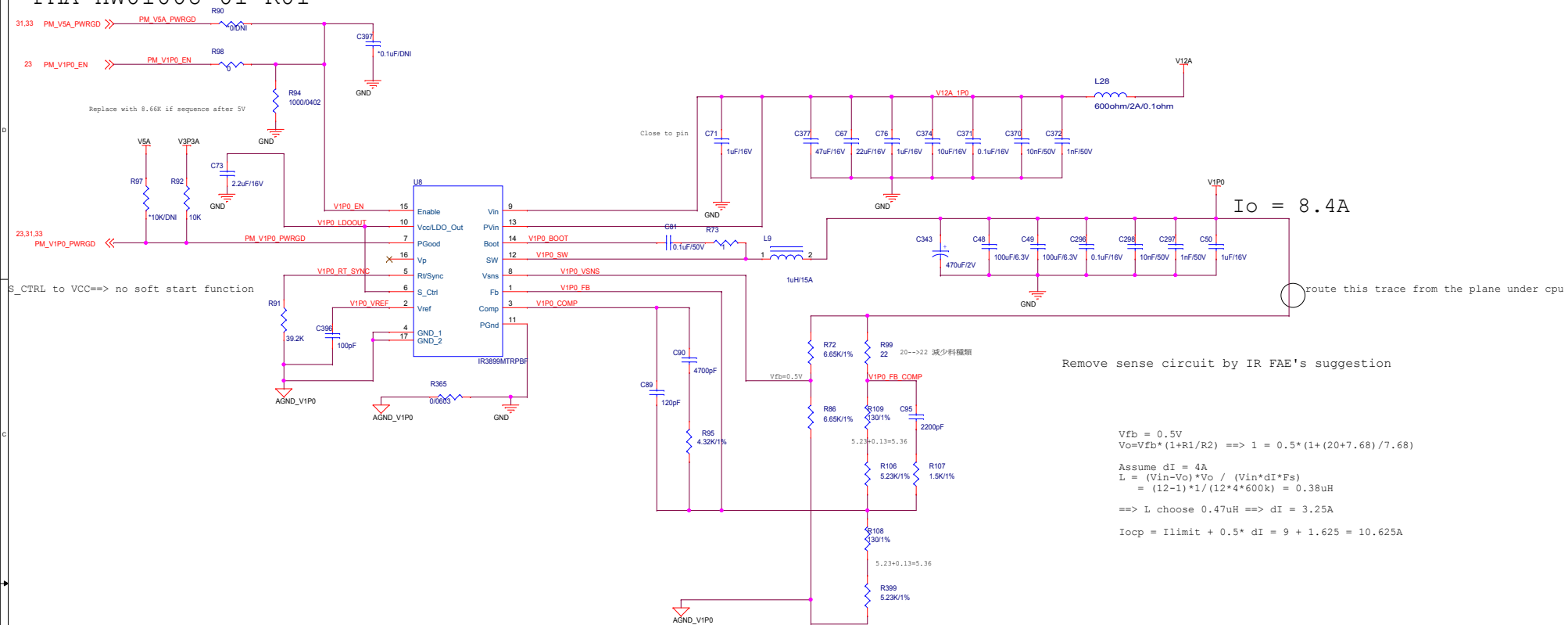


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Model Name		ES5654BT2-CPU-FLF-ZZ	Rev	R01
Size	Page Name	P27_VCCP_VNN_MOS	Engineer	Jummy_Huang
C				
Date		Wednesday, July 02, 2014	Sheet	27 of 33



FMA-HW01008-01 R01

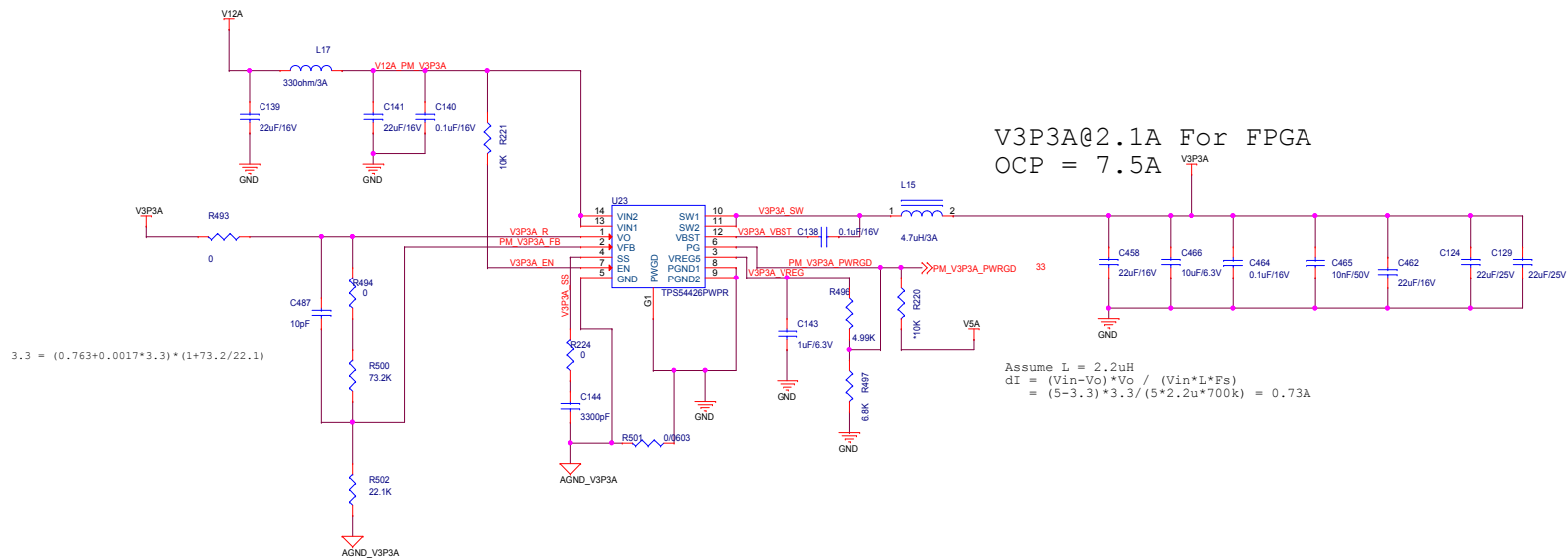
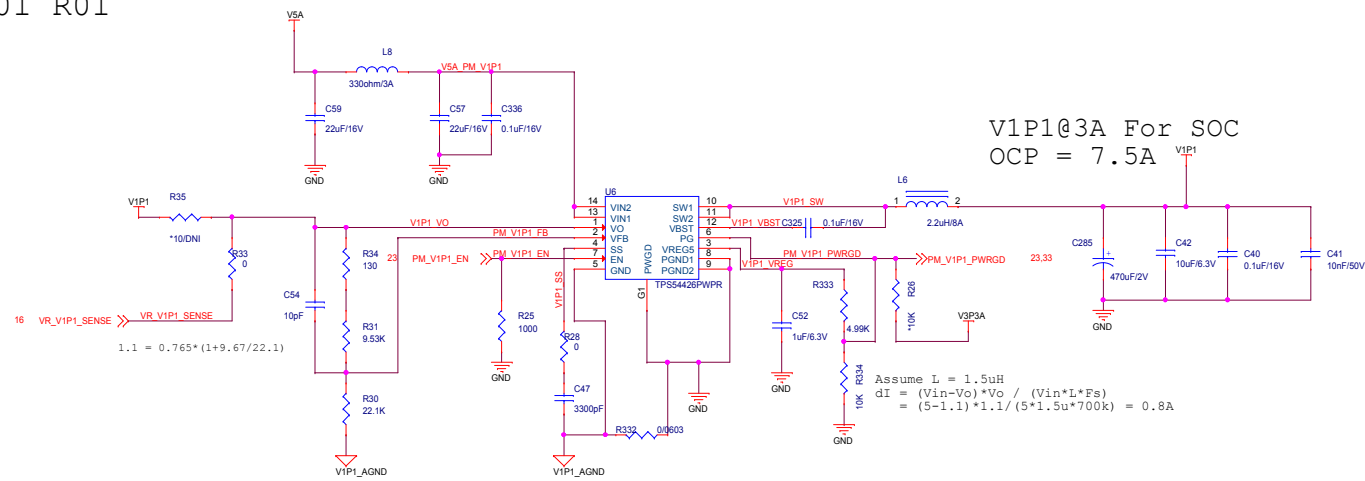


```
Vfb = 0.5V
Vo=Vfb*(1+R1/R2) ==> 1 = 0.5*(1+(20+7.68)/7.68)

Assume dI = 4A
L = (Vin-Vo)*Vo / (Vin*dI*Fs)
  = (12-1)*1/(12*4*600k) = 0.38uH

==> L choose 0.47uH ==> dI = 3.25A

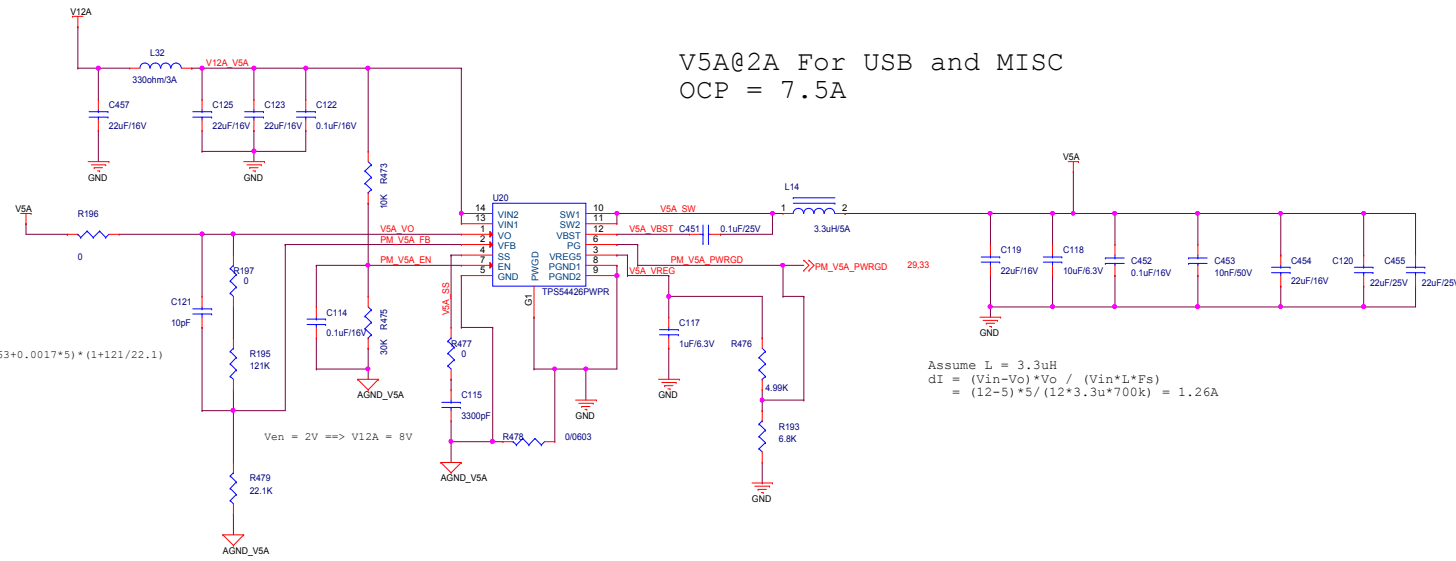
Iocp = Ilimit + 0.5* dI = 9 + 1.625 = 10.625A
```



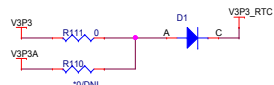
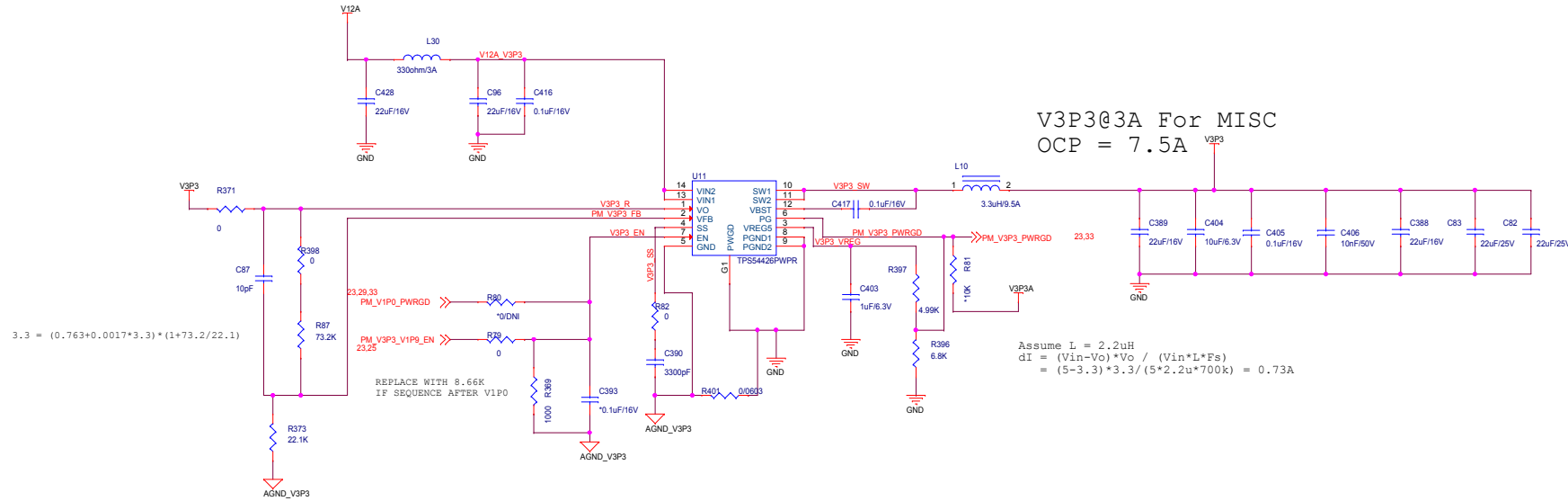
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Model Name		ES5654BT2-CPU-FLF-ZZ	Rev	R01
Size	Page Name	P30_V3P3A_V1P1	Engineer	Jummy_Huang
C				
Date: Wednesday, July 02, 2014		Sheet 30 of 33		

# V5A@2A For USB and MISC OCP = 7.5A

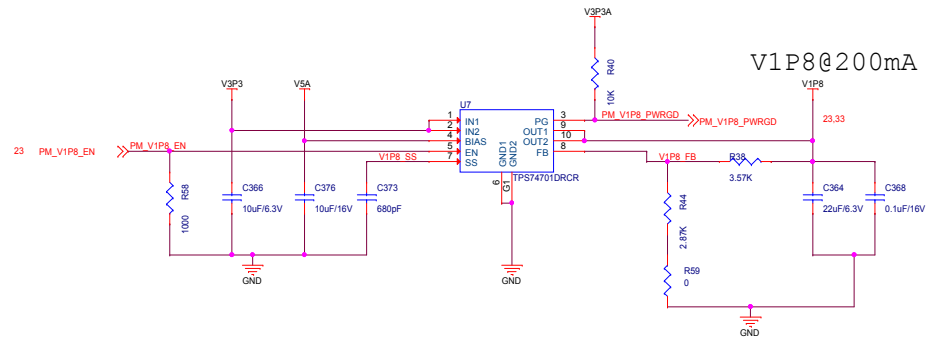


# V3P3@3A For MISC OCP = 7.5A

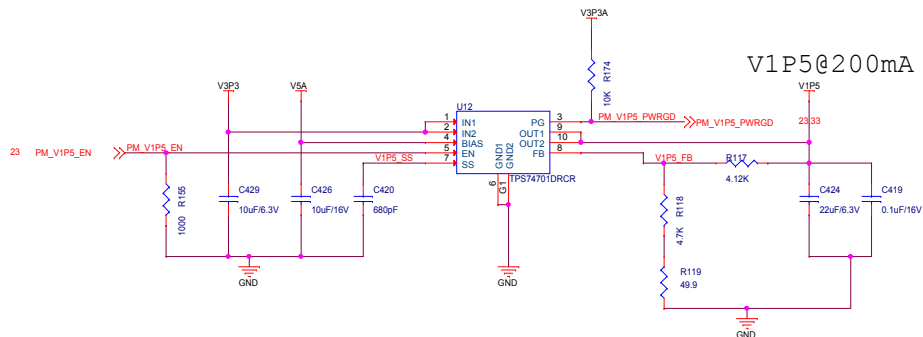


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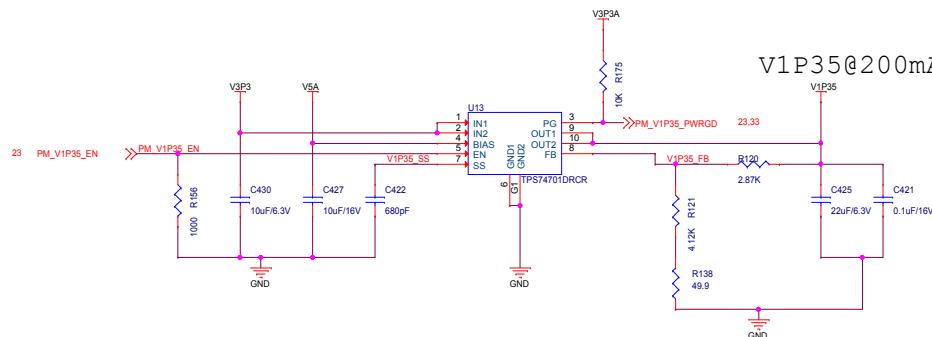
Model Name	ES654BT2-CPU-FLF-ZZ	Rev	R01
Page Name	P31_V5A_V3P3	Engineer	Jummy_Huang
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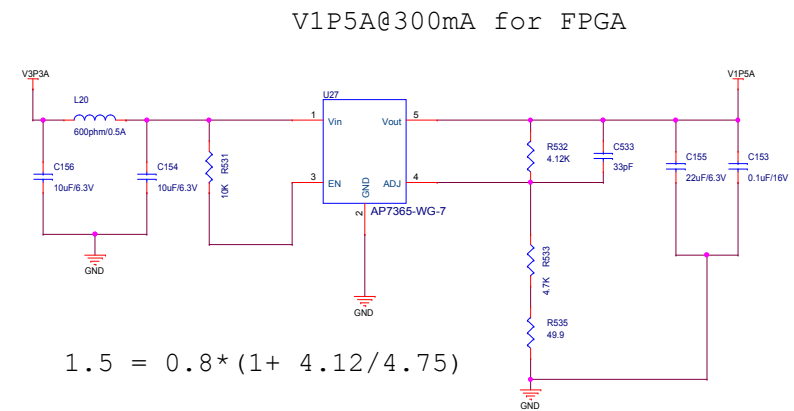
$$1.8 = 0.8 * (1 + 3.57/2.87)$$



$$1.5 = 0.8 * (1 + 4.12/4.75)$$



$$1.35 = 0.8 * (1 + 2.87/4.12)$$



$$1.5 = 0.8 * (1 + 4.12/4.75)$$



- Sequence
- 1. V5A / V3P3A
  - 2. V1P5A
  - 3. V1P0
  - 4. V1P1 / VDDQ/VTT...else power

