

REVISION HISTORY

Version	Date	Change Description

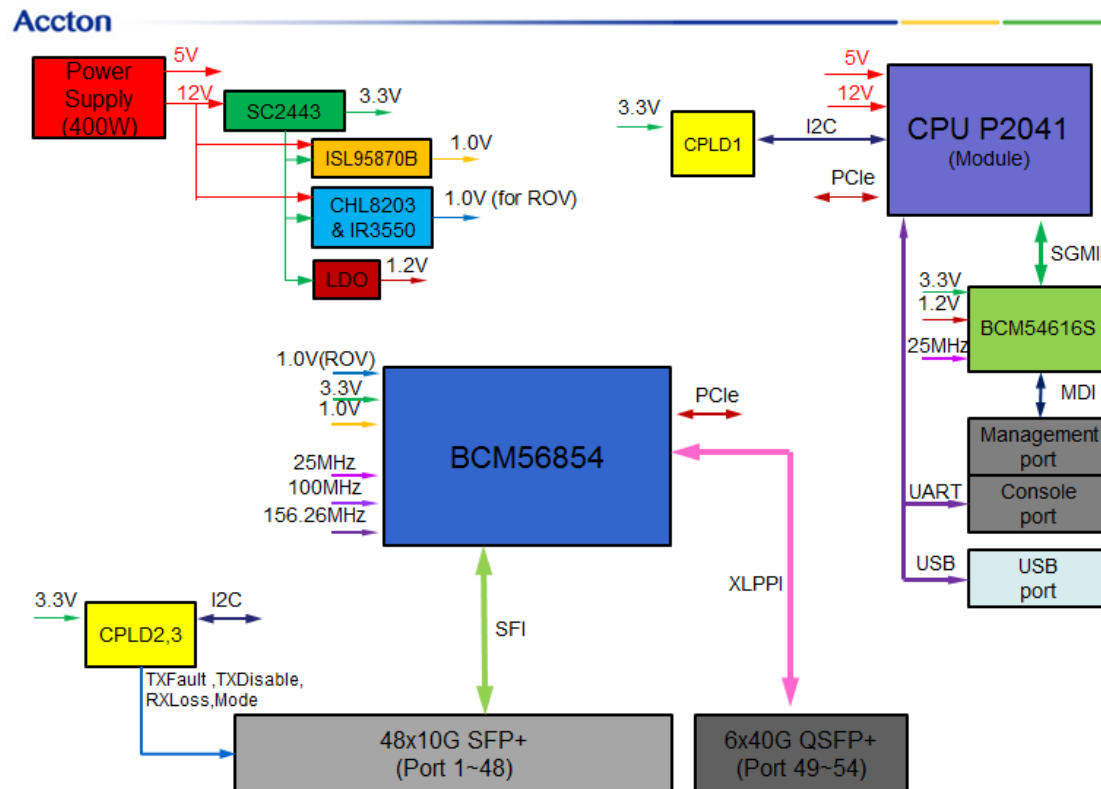
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## ES5654BT-FLF-ZZ



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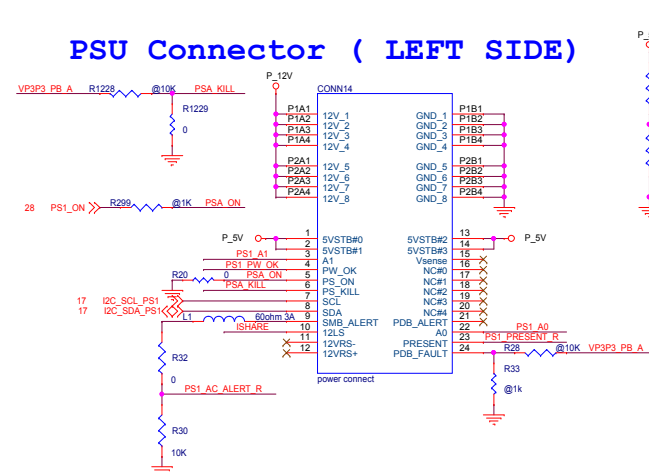


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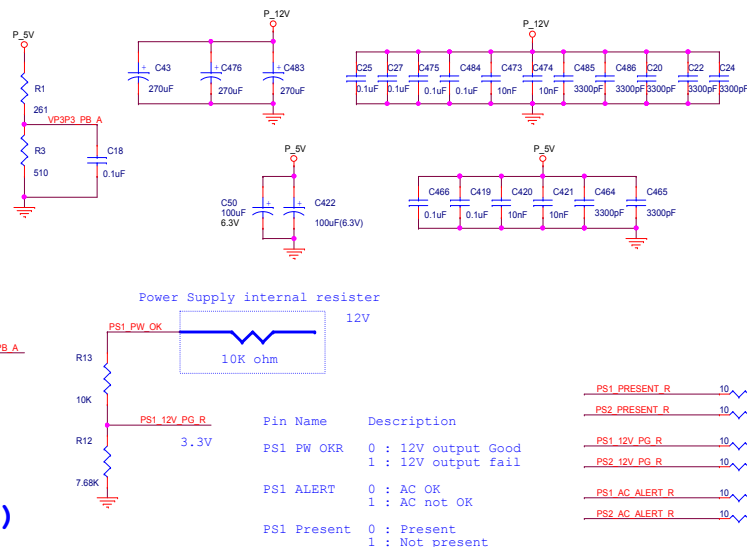
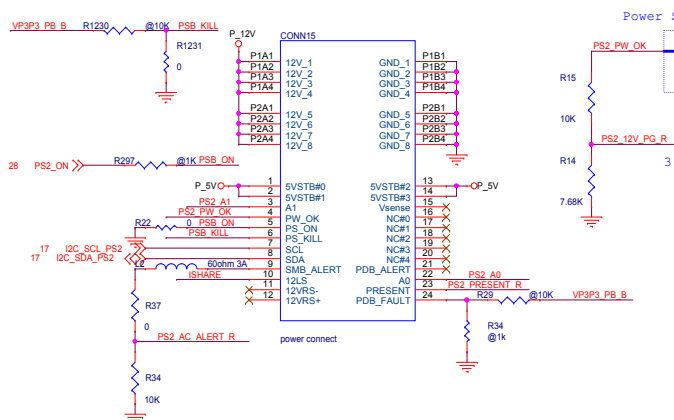
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## PSU Connector ( LEFT SIDE)



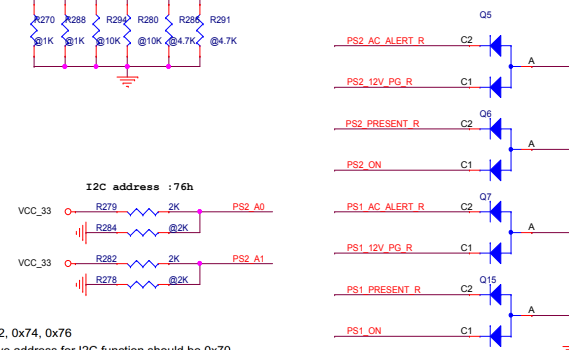
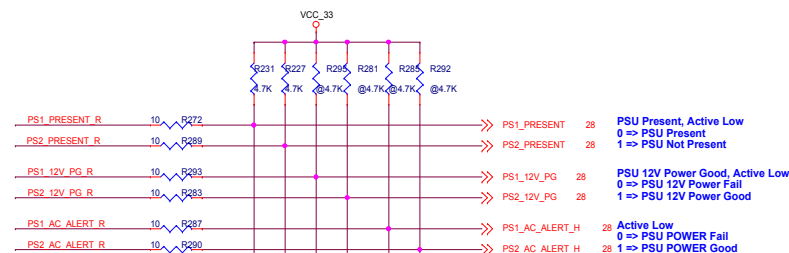
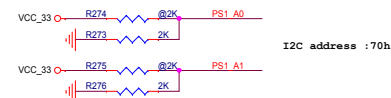
## PSU Connector ( RIGHT SIDE )



Slave address will be 0x70 (default), 0x72, 0x74, 0x76

For non-redundant power supply, the slave address for I2C function should be 0x70.

System addressing	0/0	0/1	1/0	1/1
Address1 (A1) /Address0 (A0)				
Power supply I2C slave address	70h	72h	74h	76h

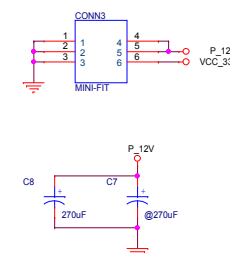
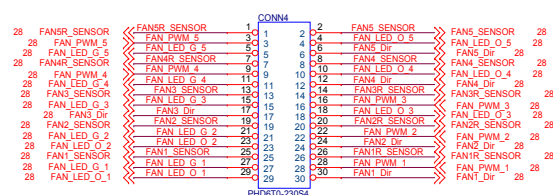
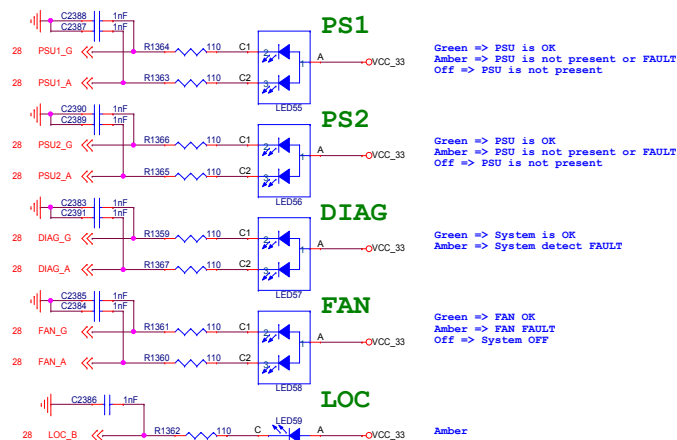


Slave address will be 0x70 (default), 0x72, 0x74, 0x76

For non-redundant power supply, the slave address for I2C function should be 0x70.

System addressing Address1 (A1) /Address0 (A0)	0/0	0/1	1/0	1/1
Power supply I2C slave address	70h	72h	74h	76h

## Fan-Board Connector



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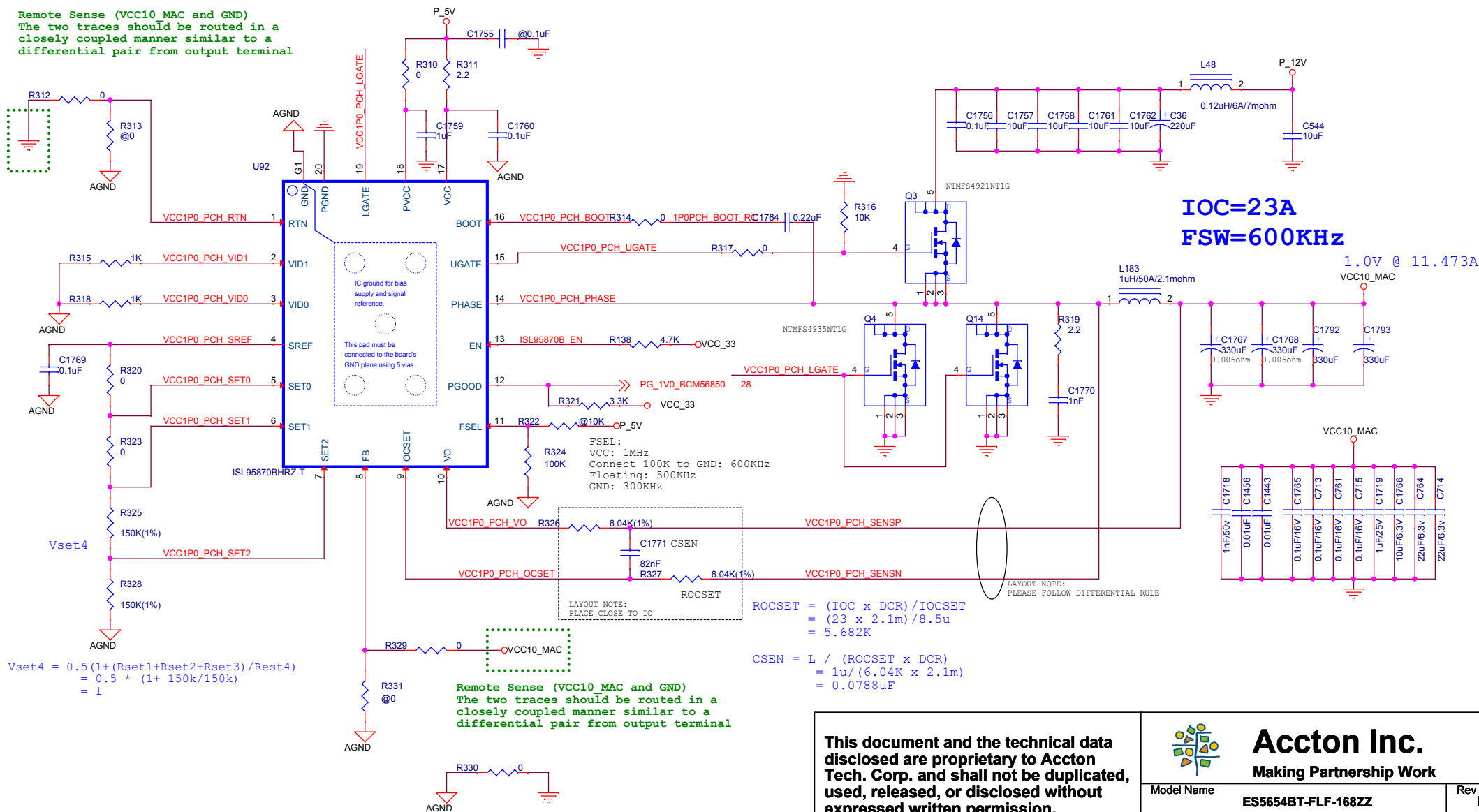
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Remote Sense (VCC10 MAC and GND)  
The two traces should be routed in a  
closely coupled manner similar to a  
differential pair from output terminal



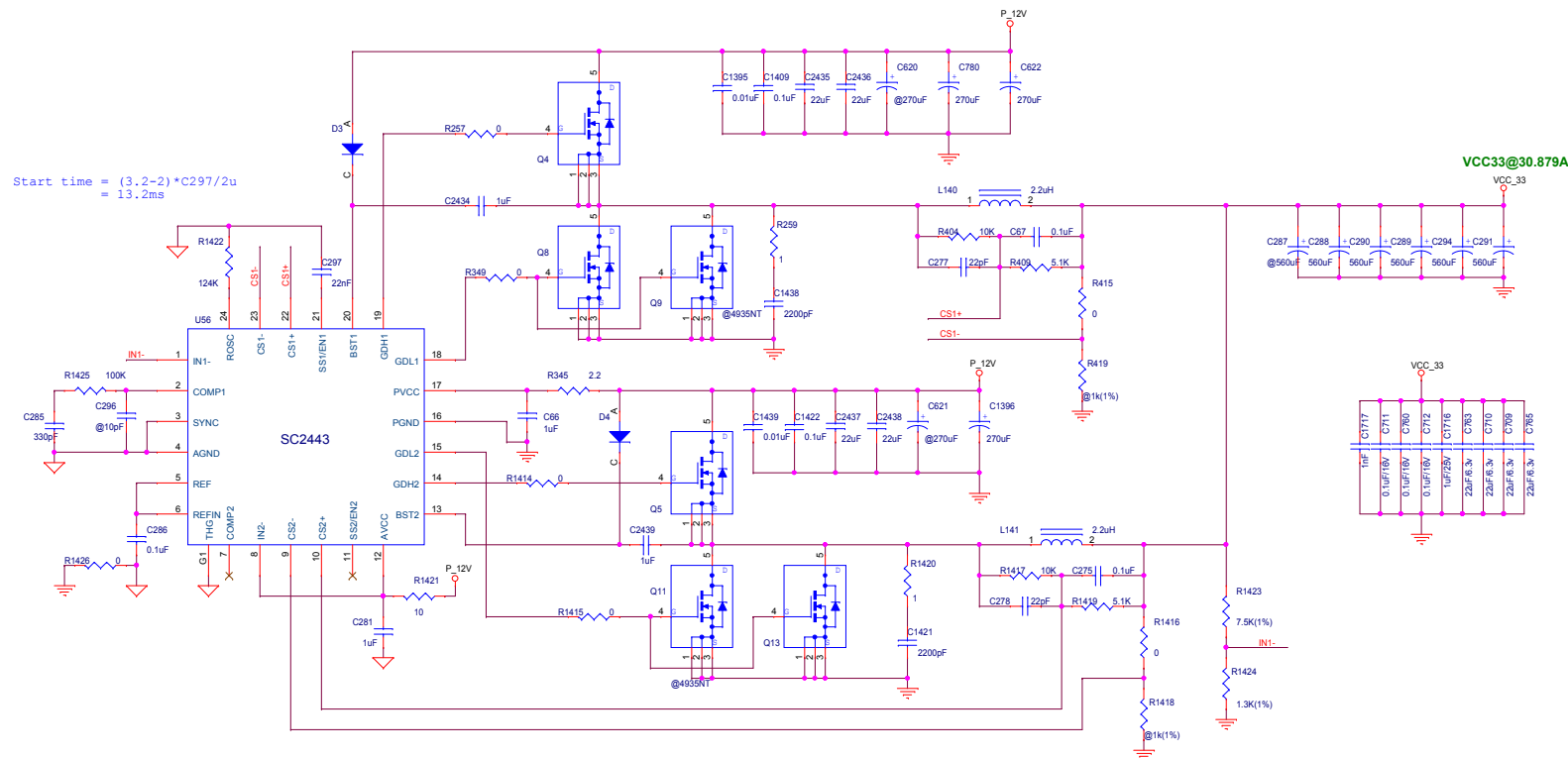
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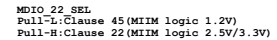
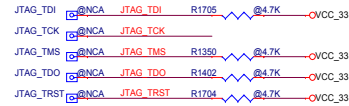
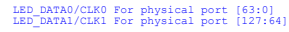


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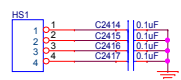
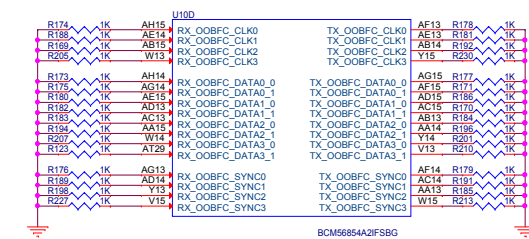
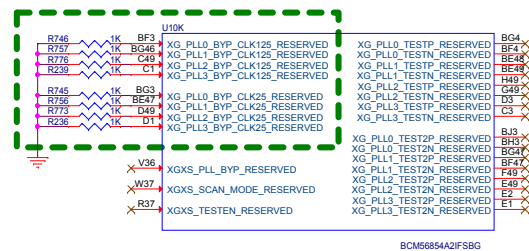
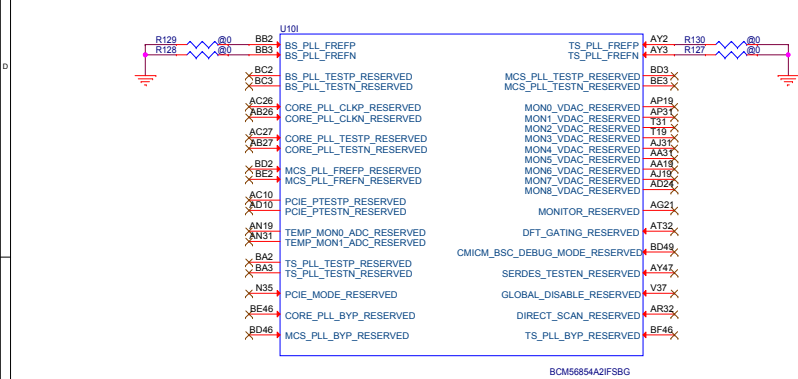
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```
EEPROM load enable
* 0: EEPROM load not enable
  1: EEPROM load enable
```

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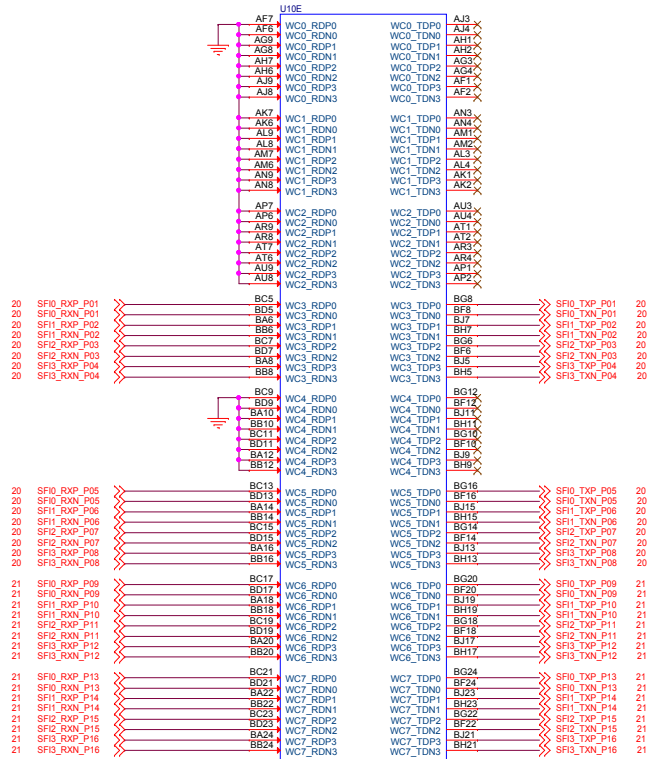
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Model Name		ES9654BT-FLF-168ZZ	Rev	R0B
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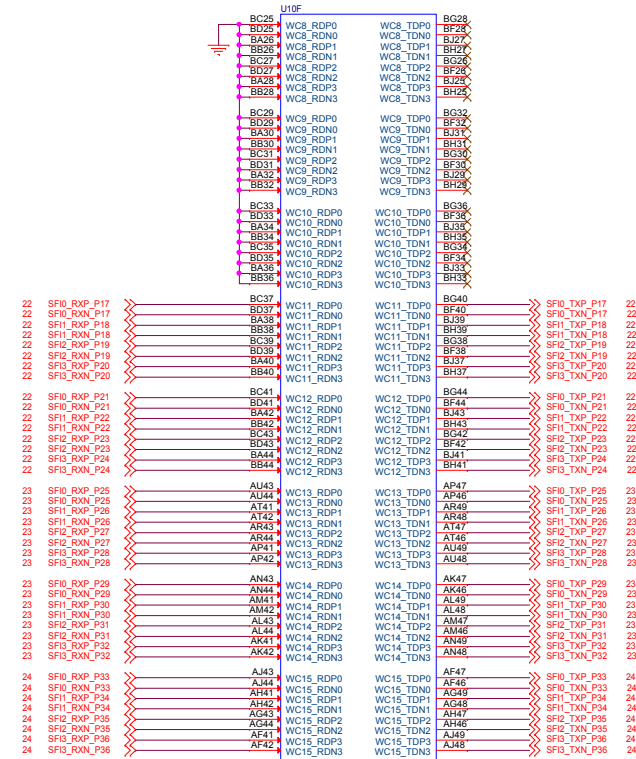
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		WC2	WC1	WC0	WC31	WC30	WC29	
SFP+ P01~04	WC3							WC28 No Use
No Use	WC4							WC27 QSFP+ 04
SFP+ P05~08	WC5	X-Quadrant 0			Y-Quadrant 1			WC26 QSFP+ 06
SFP+ P09~12	WC6							WC25 QSFP+ 03
SFP+ P13~16	WC7							WC24 QSFP+ 05
No Use	WC8							WC23 No Use
No Use	WC9							WC22 No Use
No Use	WC10	X-Quadrant 1			Y-Quadrant 0			WC21 No Use
SFP+ P17~20	WC11							WC20 QSFP+ 01
SFP+ P21~24	WC12							WC19 QSFP+ 02
		WC13	WC14	WC15	WC16	WC17	WC18	
		SFP+ P25~28	SFP+ P29~32	SFP+ P33~36	SFP+ P37~40	SFP+ P41~44	SFP+ P45~48	

## WC0~7



BCM5685A2IFSBG

## WC8~15



BCM5685A2IFSBG

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		No Use	No Use	No Use	No Use	No Use	No Use		
		WC2	WC1	WC0	WC31	WC30	WC29		
SFP+ P01~04	WC3							WC28	No Use
No Use	WC4							WC27	QSFP+ 04
SFP+ P05~08	WC5	X-Quadrant 0			Y-Quadrant 1			WC26	QSFP+ 06
SFP+ P09~12	WC6							WC25	QSFP+ 03
SFP+ P13~16	WC7							WC24	QSFP+ 05
No Use	WC8							WC23	No Use
No Use	WC9							WC22	No Use
No Use	WC10	X-Quadrant 1			Y-Quadrant 0			WC21	No Use
SFP+ P17~20	WC11							WC20	QSFP+ 01
SFP+ P21~24	WC12							WC19	QSFP+ 02
		WC13	WC14	WC15	WC16	WC17	WC18		
		SFP+ P25~28	SFP+ P29~32	SFP+ P33~36	SFP+ P37~40	SFP+ P41~44	SFP+ P45~48		

WC16~23



BCM56854A2IFS8G

WC24~31



BCM56854A2IFS8G

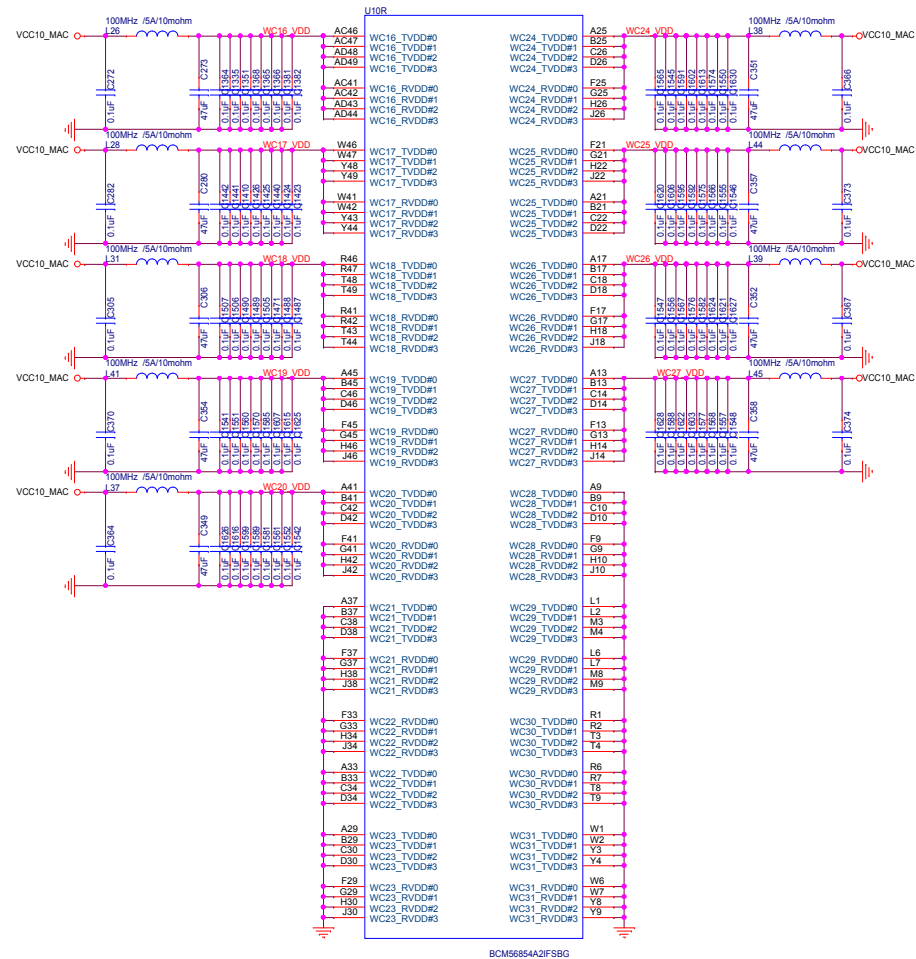
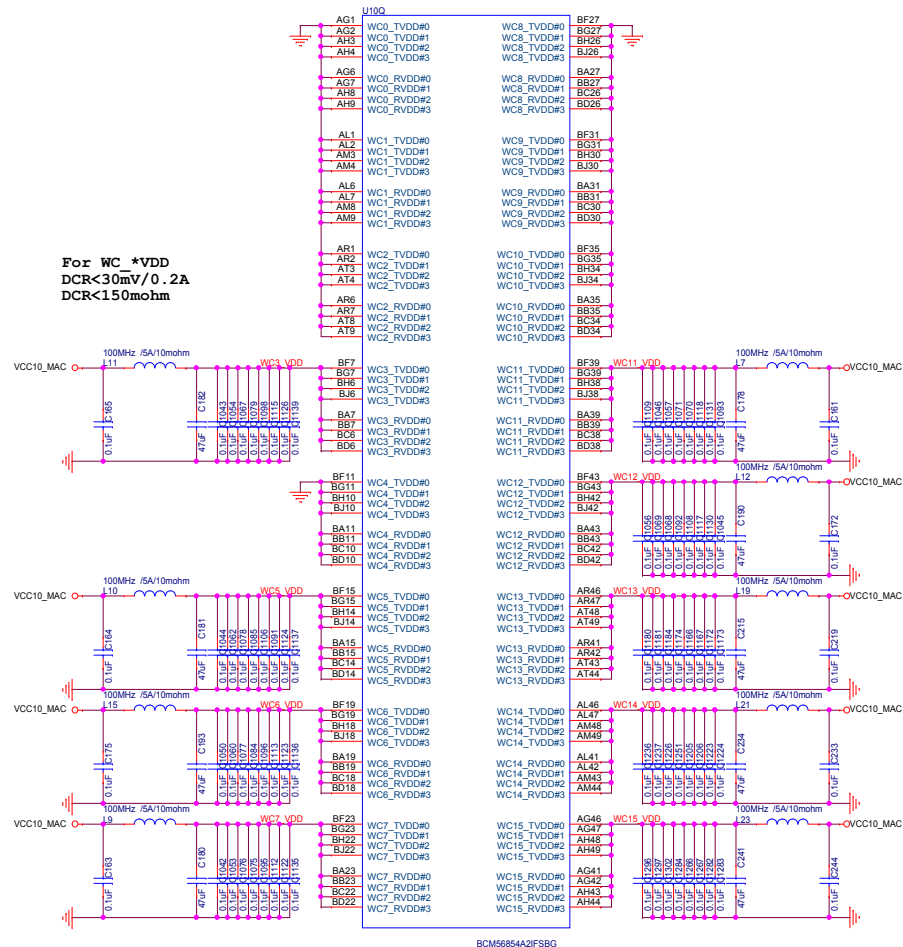
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For WC \*VDD  
DCR<30mV/0.2A  
DCR<150mhm



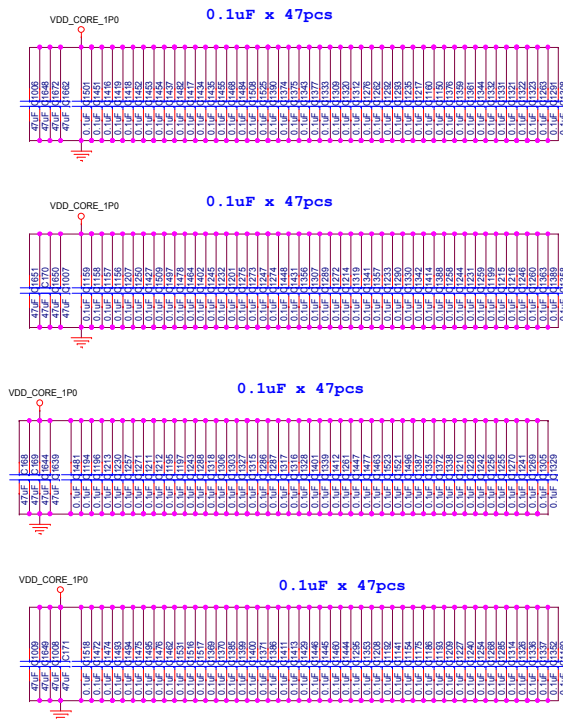
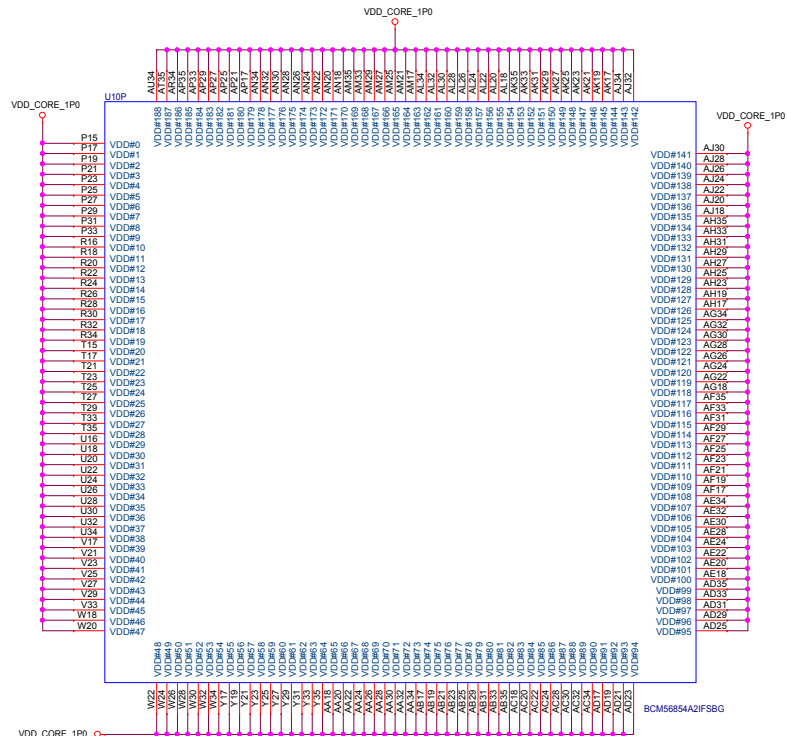
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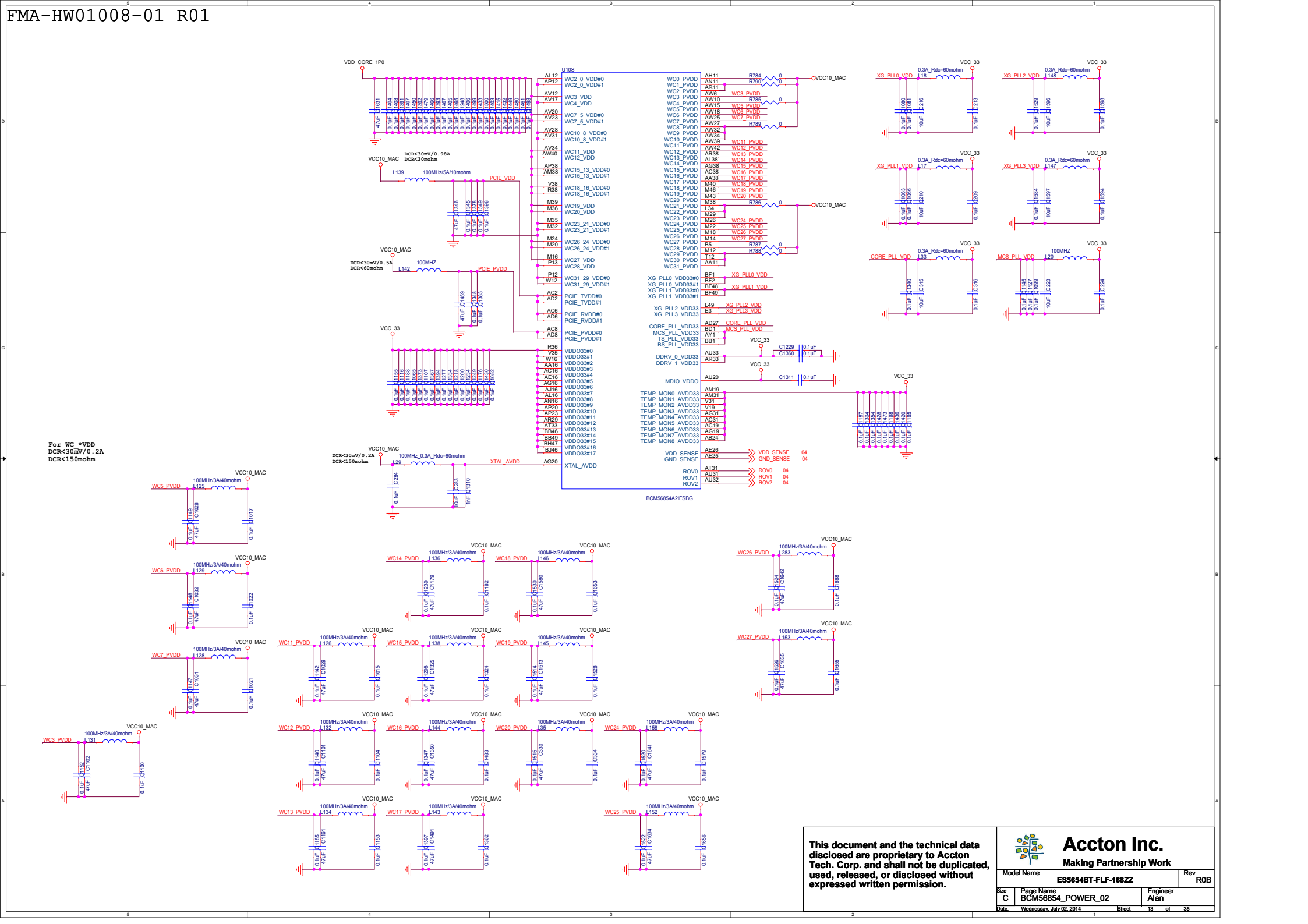


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**FMA-HW01008-01 R01**

VDD\_CORE\_IP0

VCC10\_MAC

VCC10\_MMC

VCC10\_MMC#1

VCC10\_MMC#2

VCC10\_MMC#3

VCC10\_MMC#4

VCC10\_MMC#5

VCC10\_MMC#6

VCC10\_MMC#7

VCC10\_MMC#8

VCC10\_MMC#9

VCC10\_MMC#10

VCC10\_MMC#11

VCC10\_MMC#12

VCC10\_MMC#13

VCC10\_MMC#14

VCC10\_MMC#15

VCC10\_MMC#16

VCC10\_MMC#17

VCC10\_MMC#18

VCC10\_MMC#19

VCC10\_MMC#20

VCC10\_MMC#21

VCC10\_MMC#22

VCC10\_MMC#23

VCC10\_MMC#24

VCC10\_MMC#25

VCC10\_MMC#26

VCC10\_MMC#27

VCC10\_MMC#28

VCC10\_MMC#29

VCC10\_MMC#30

VCC10\_MMC#31

VCC10\_MMC#32

VCC10\_MMC#33

VCC10\_MMC#34

VCC10\_MMC#35

VCC10\_MMC#36

VCC10\_MMC#37

VCC10\_MMC#38

VCC10\_MMC#39

VCC10\_MMC#40

VCC10\_MMC#41

VCC10\_MMC#42

VCC10\_MMC#43

VCC10\_MMC#44

VCC10\_MMC#45

VCC10\_MMC#46

VCC10\_MMC#47

VCC10\_MMC#48

VCC10\_MMC#49

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VCC10\_MMC#51

VCC10\_MMC#52

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VCC10\_MMC#57

VCC10\_MMC#58

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VCC10\_MMC#60

VCC10\_MMC#61

VCC10\_MMC#62

VCC10\_MMC#63

VCC10\_MMC#64

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VCC10\_MMC#91

VCC10\_MMC#92

VCC10\_MMC#93

VCC10\_MMC#94

VCC10\_MMC#95

VCC10\_MMC#96

VCC10\_MMC#97

VCC10\_MMC#98

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VCC10\_MMC#100

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VCC10\_MMC#103

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VCC10\_MMC#111

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VCC10\_MMC#113

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VCC10\_MMC#213

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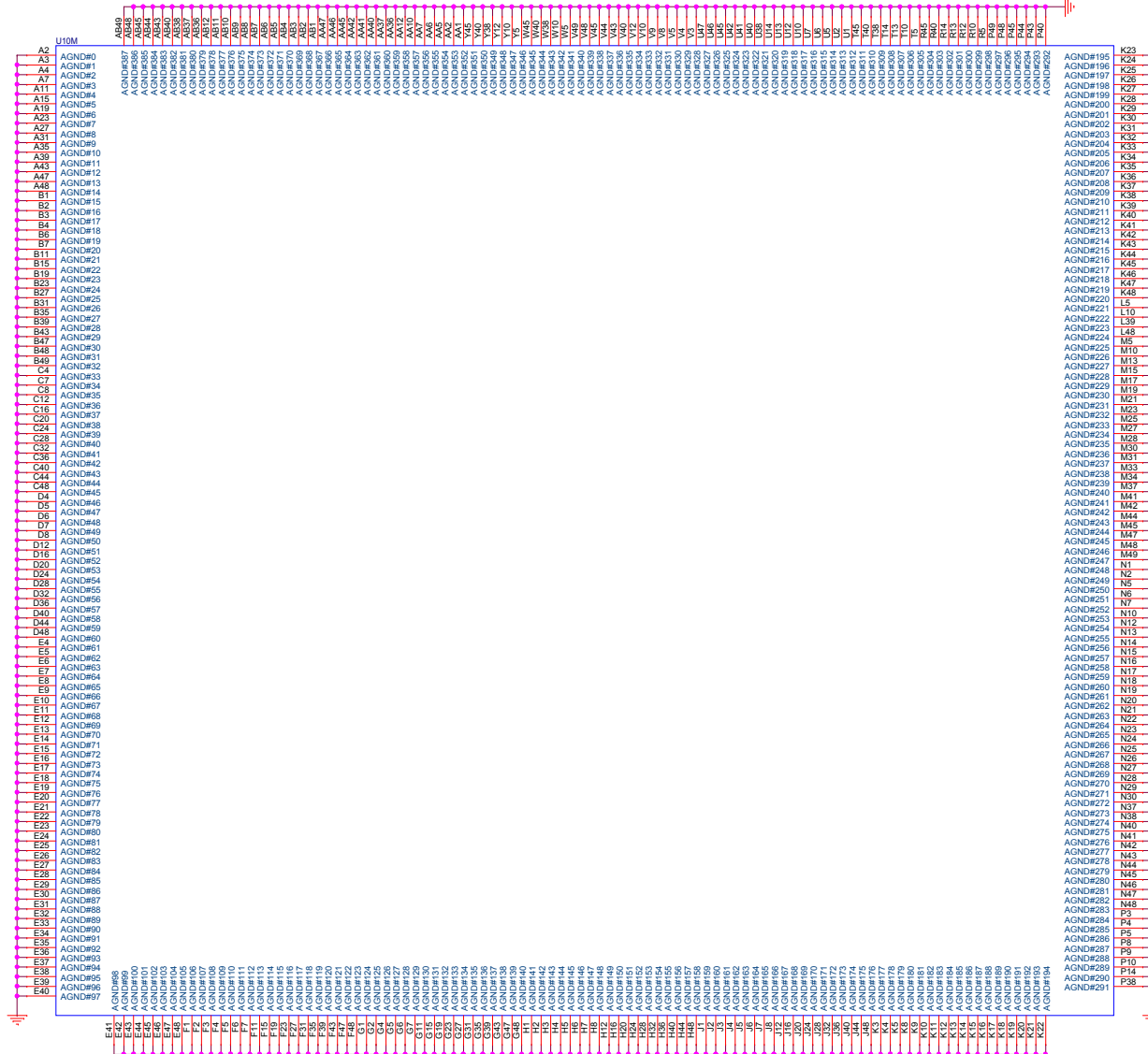
VCC10\_MMC#262

VCC10\_MMC#263

VCC10\_MMC#264

VCC10\_MMC#265

VCC



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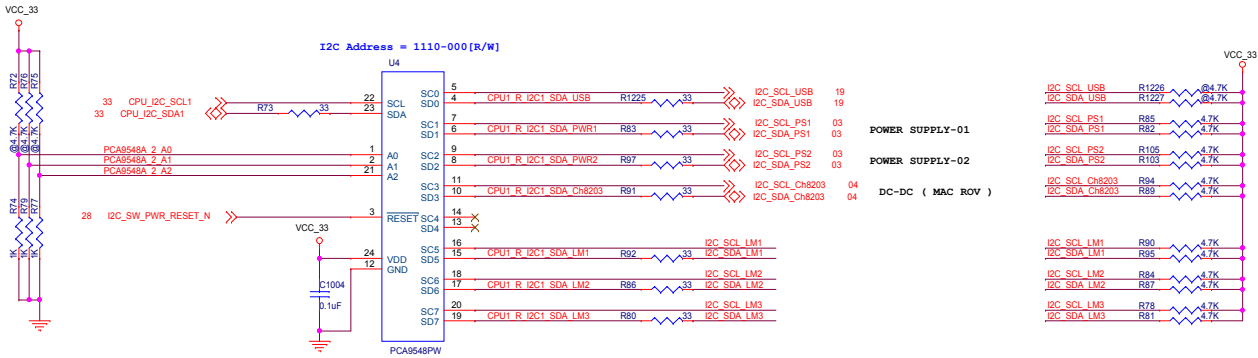
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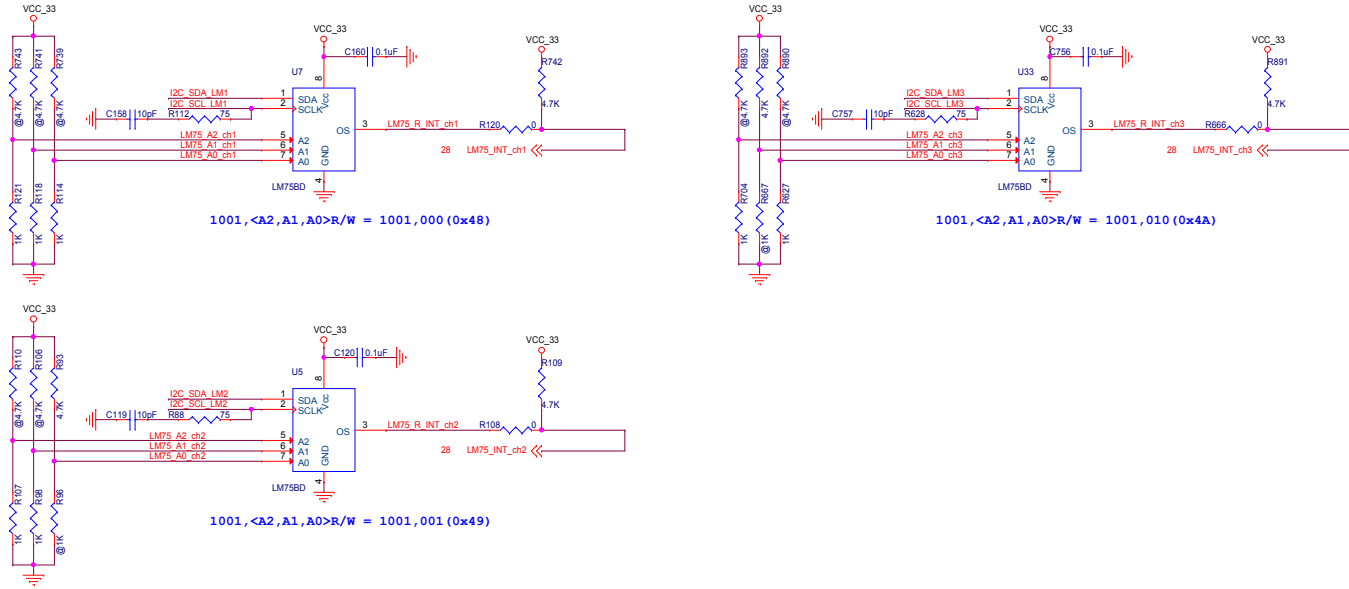








**THERMAL SENSOR**



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REFCLK\_SEL [1:0]  
 00 = Select differential clock input  
 01 = Select single-ended CMOS  
 \*10 = Select XTAL input  
 11 = Not allowed

INTERF\_SEL [1:0]  
 00 = RGMII-Copper (Copper mode)  
 01 = RGMII-Fiber (Fiber mode)  
 \*10 = SGMII-Copper (SGMII mode)  
 11 = SerDes-Copper (Media Converter mode)

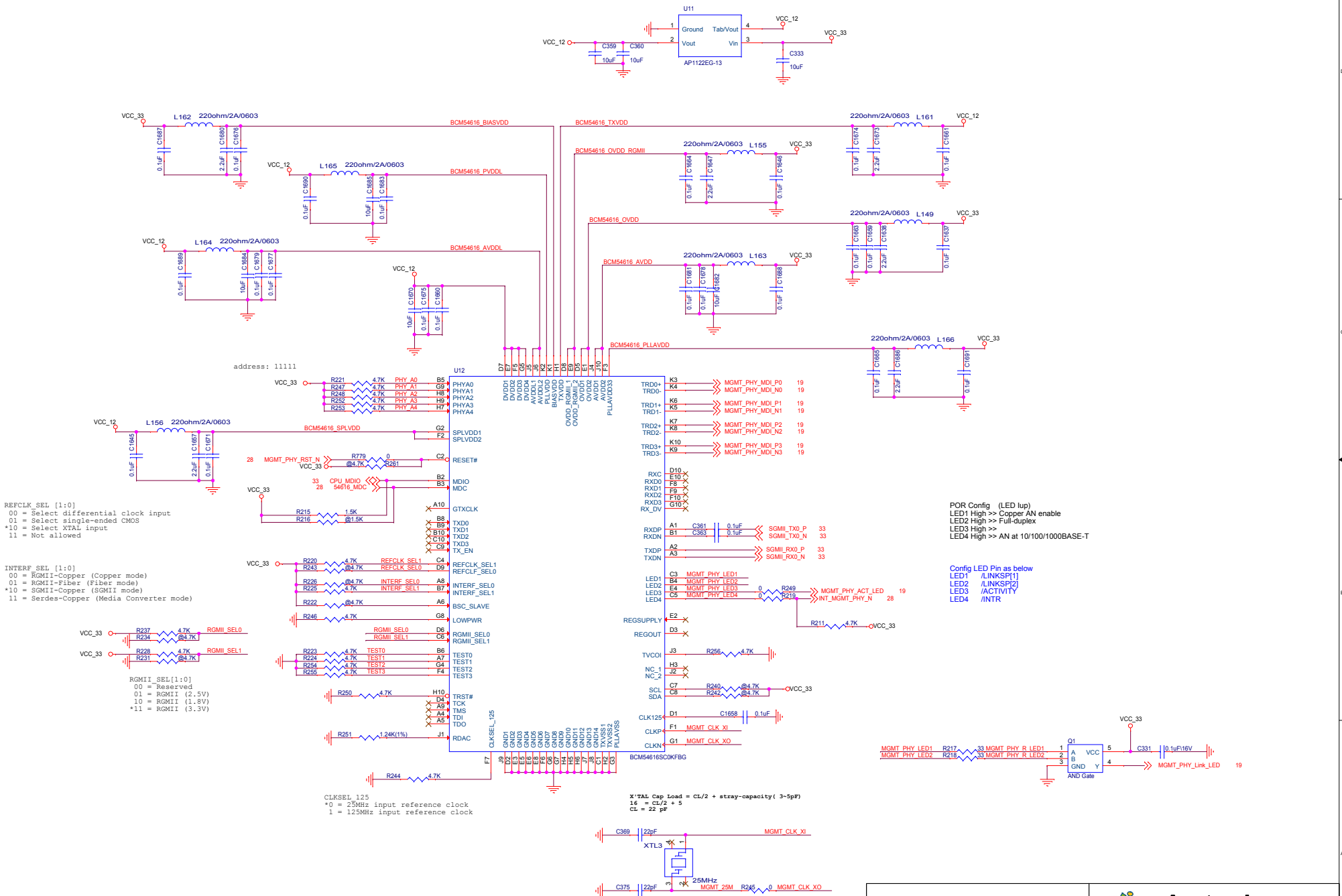
RGMII\_SEL [1:0]  
 00 = Reserved  
 01 = RGMII (2.5V)  
 10 = RGMII (1.8V)  
 \*11 = RGMII (3.3V)

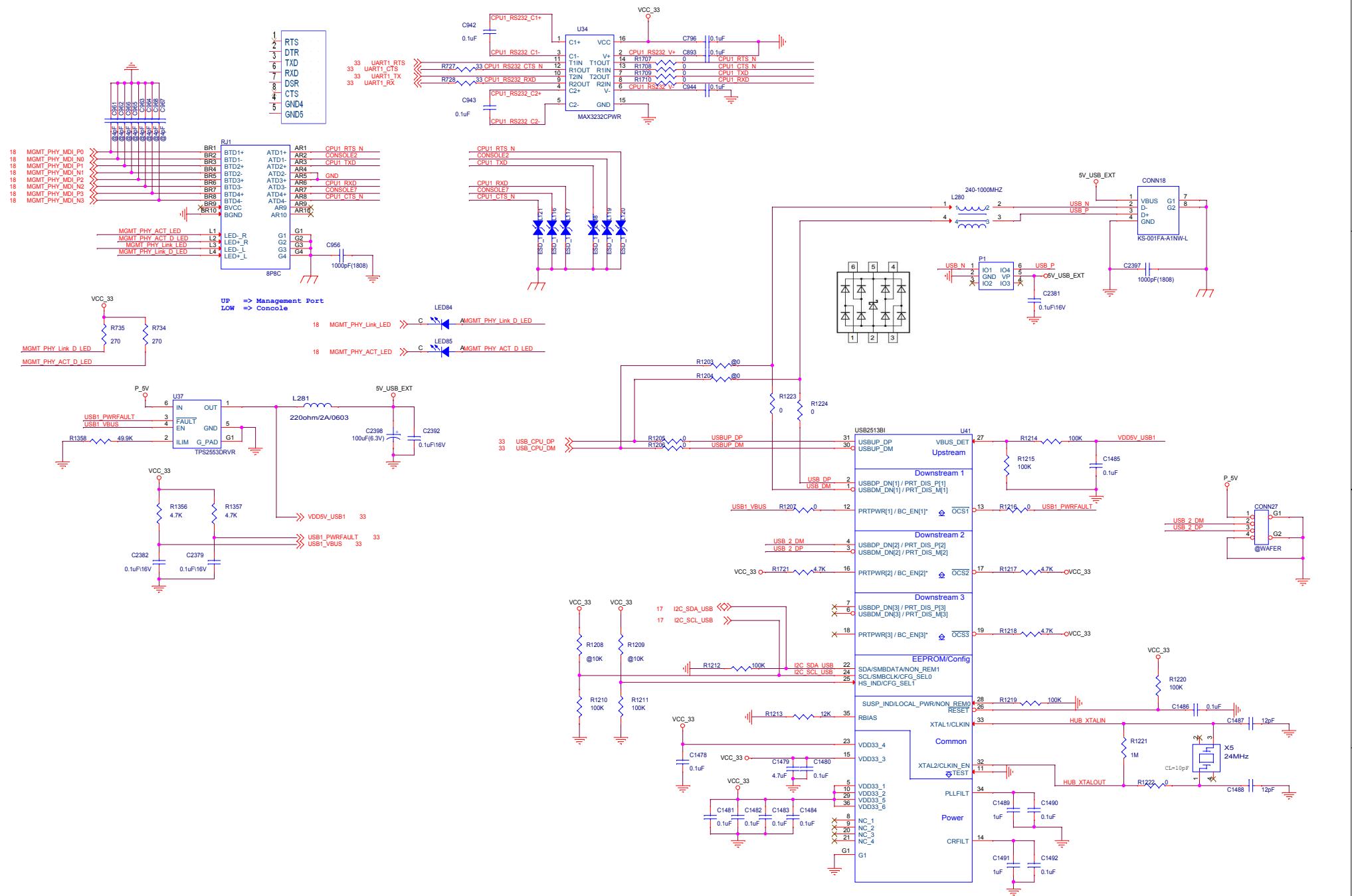
CLKSEL\_125  
 \*0 = 25MHz input reference clock  
 1 = 125MHz input reference clock

X'tal Cap Load =  $CL/2 + \text{stray-capacity}$  (3-5pF)  
 16 =  $CL/2 + 5$   
 CL = 22 pF

POR Config (LED up)  
 LED1 High >> Copper AN enable  
 LED2 High >> Full-duplex  
 LED3 High >>  
 LED4 High >> AN at 10/100/1000BASE-T

Config LED Pin as below  
 LED1 /LINKSP1  
 LED2 /LINKSP2  
 LED3 /ACTIVITY  
 LED4 /INTR



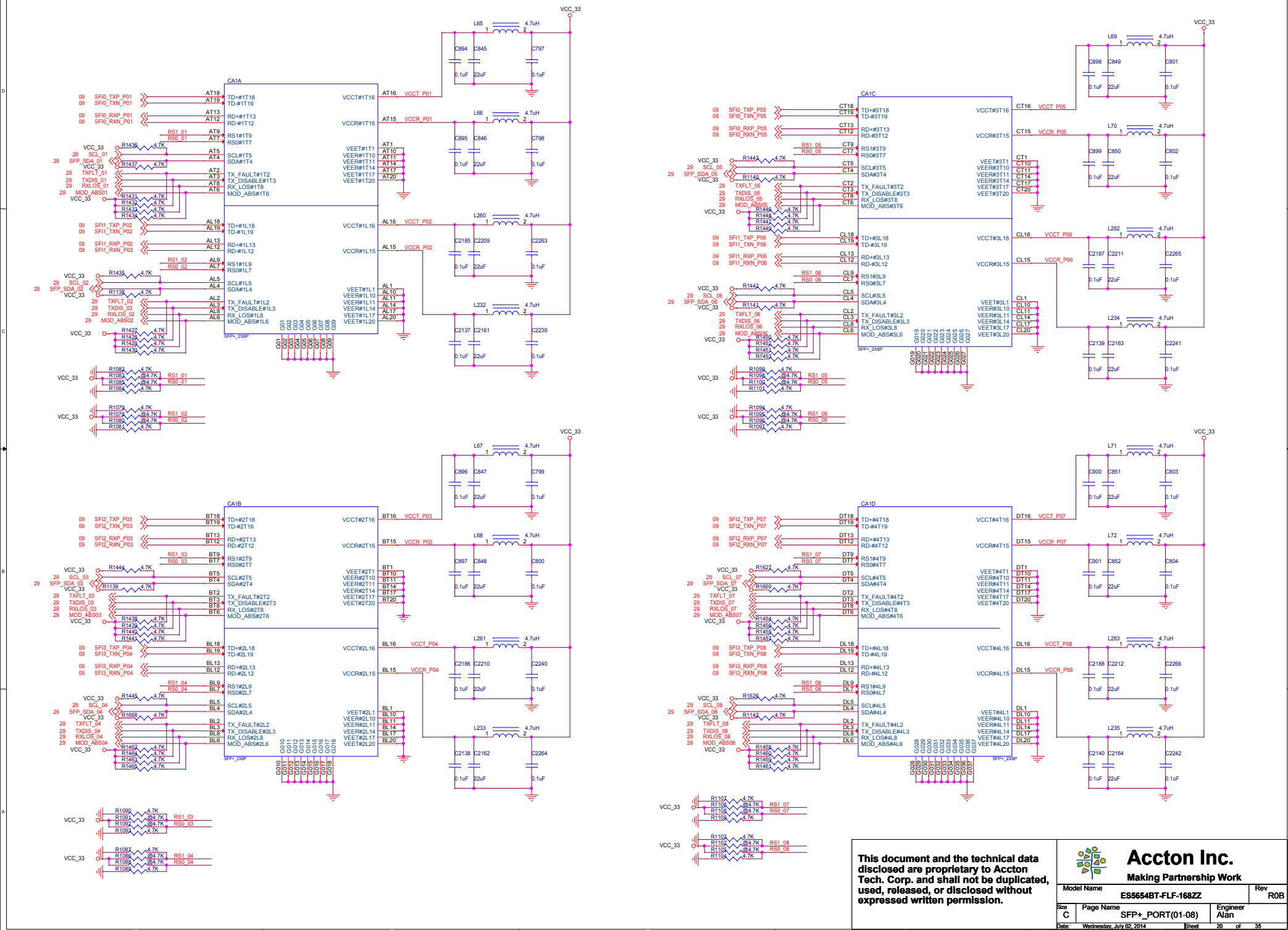



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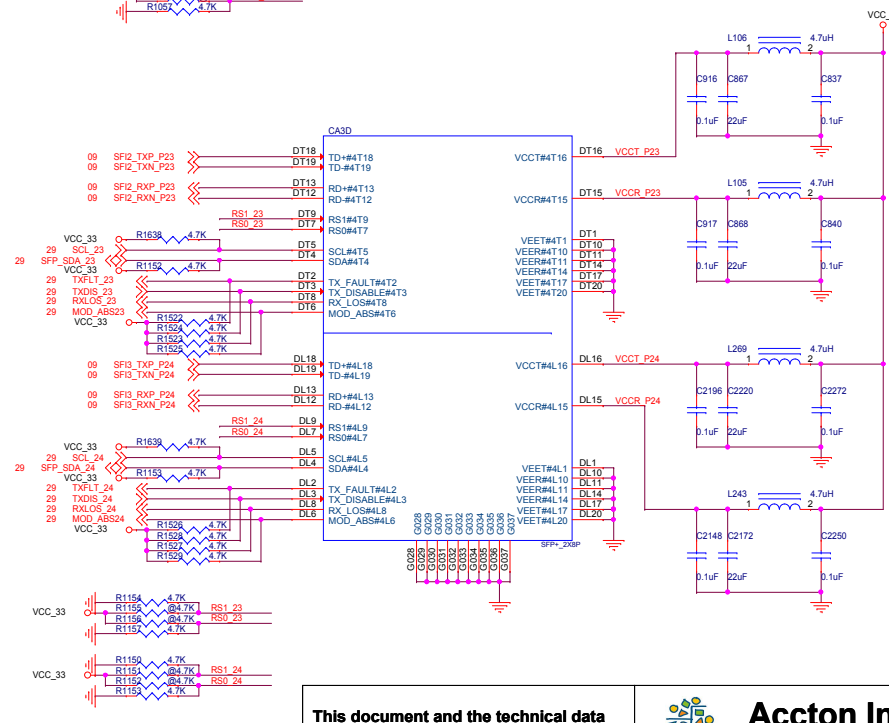
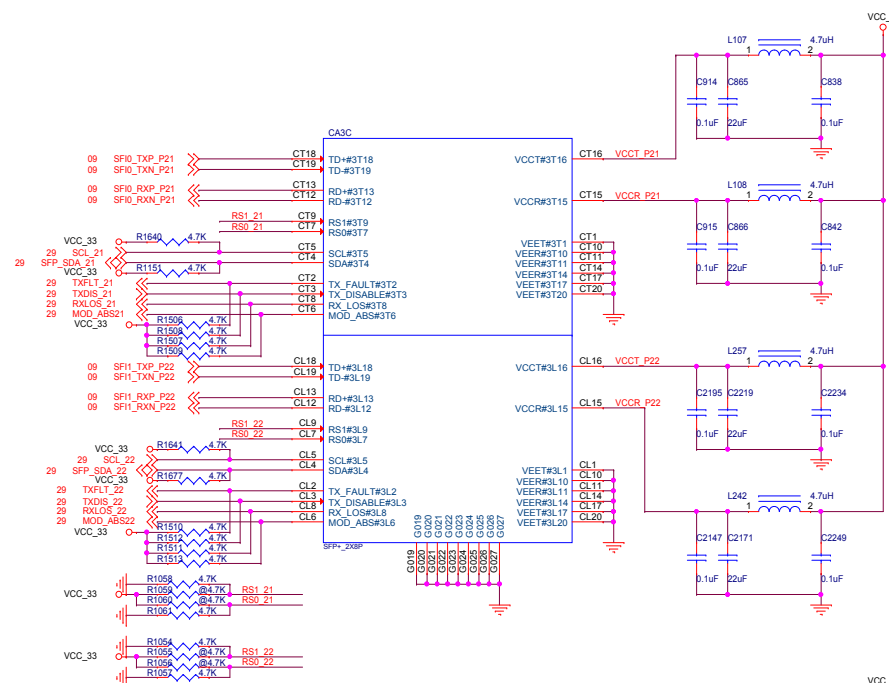
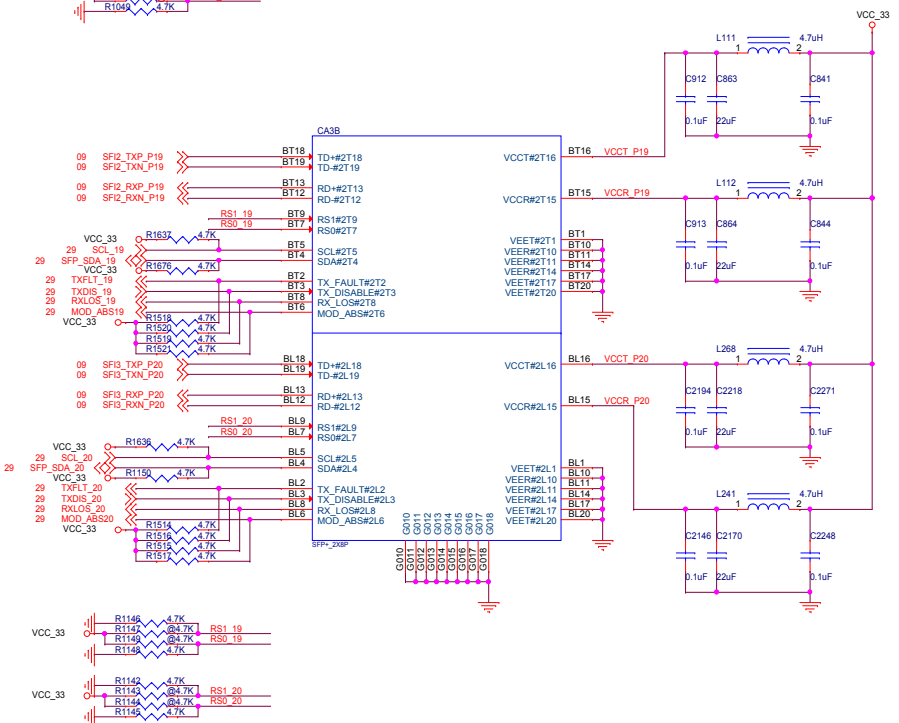
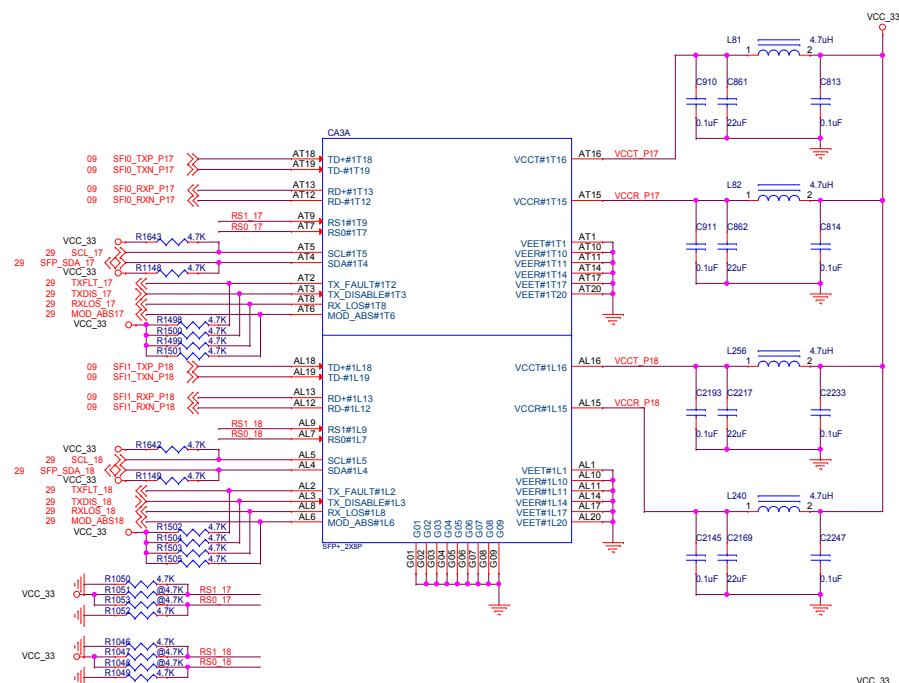


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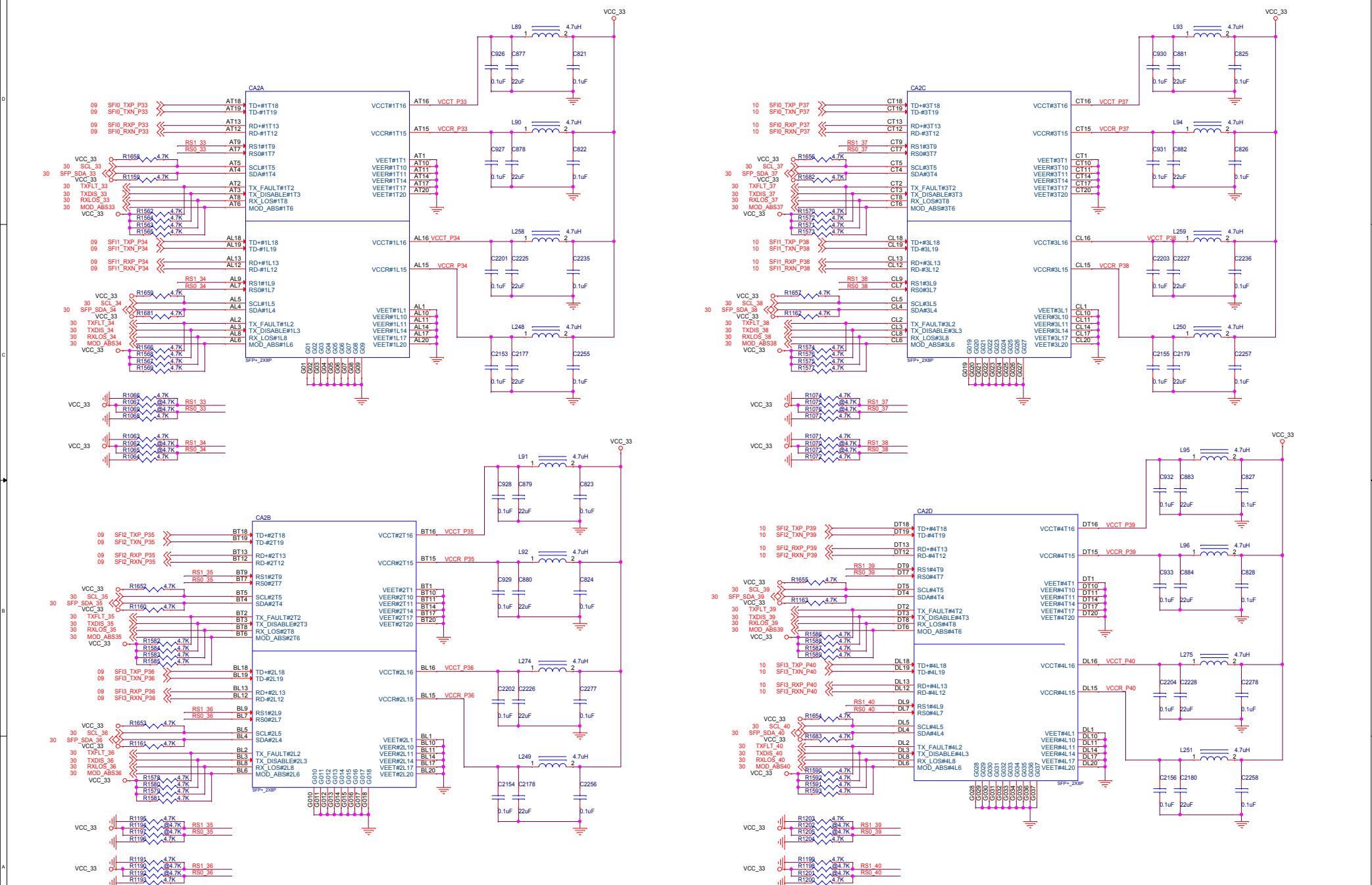


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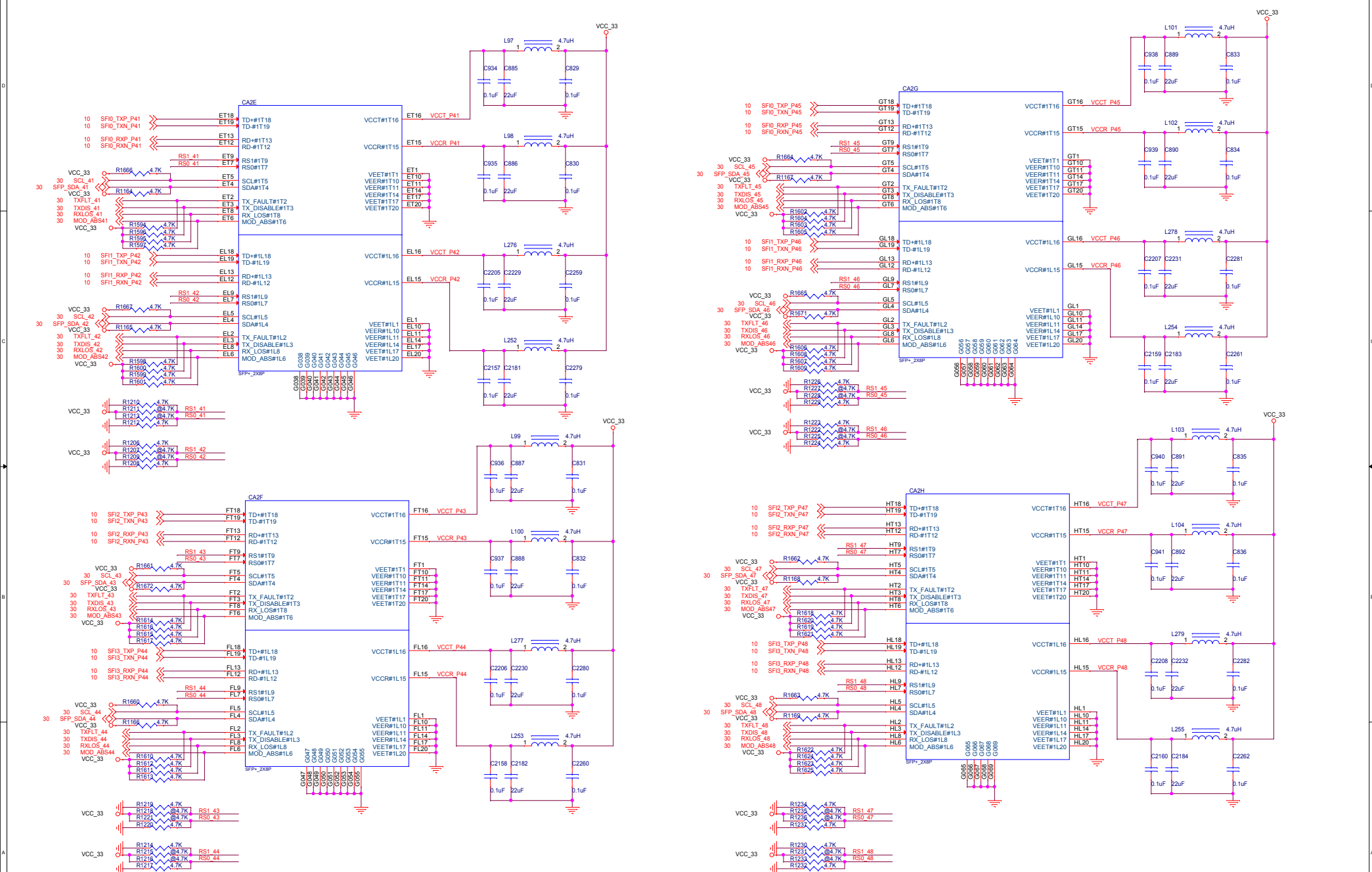
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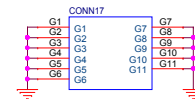
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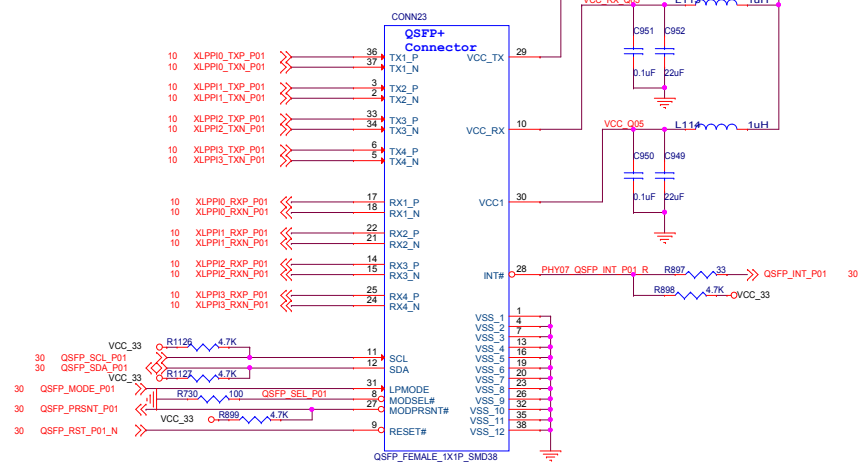
# Accton Inc.

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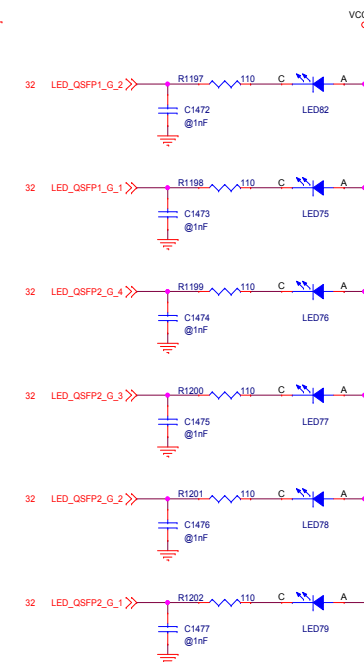
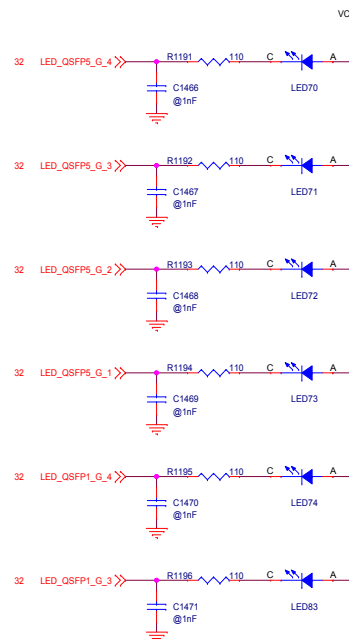
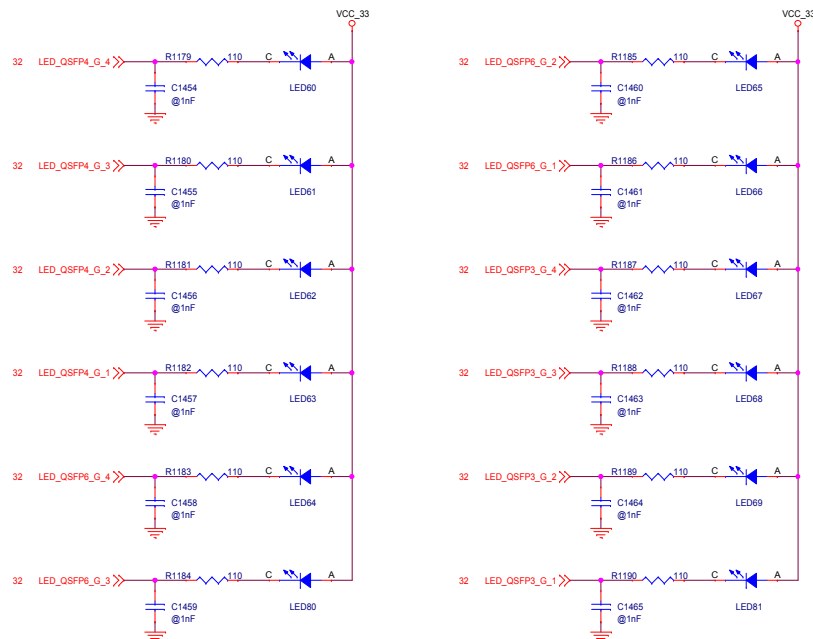
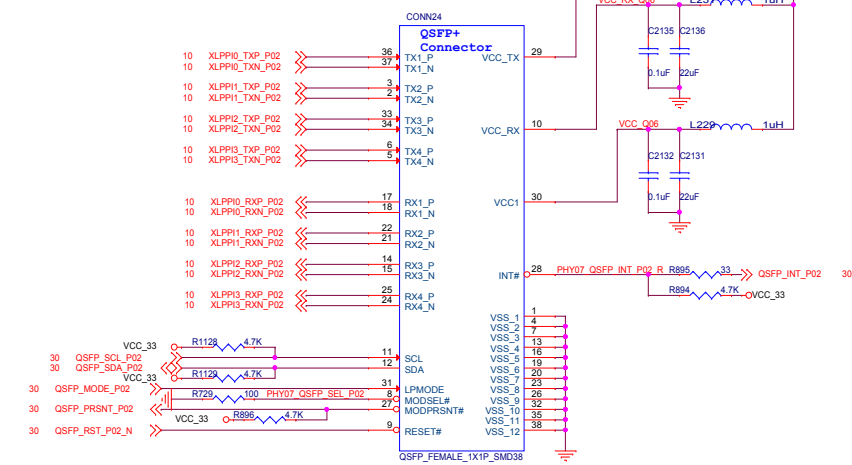
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## QSFP PORT01



## QSFP PORT02



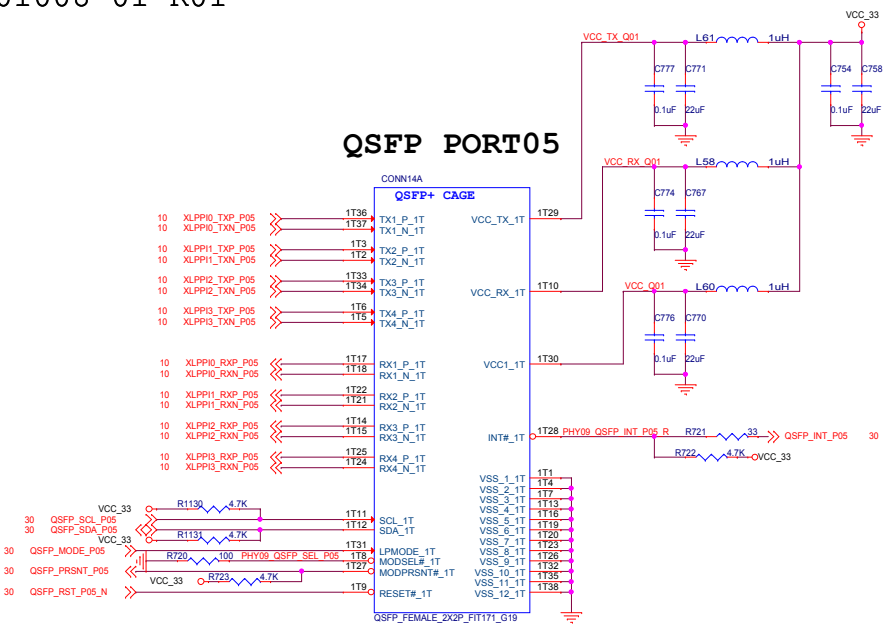
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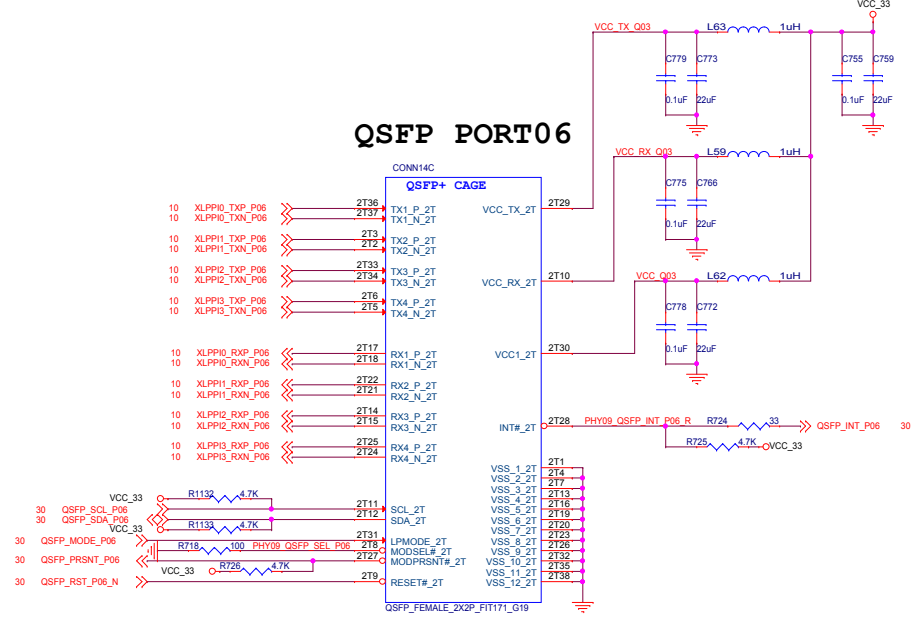
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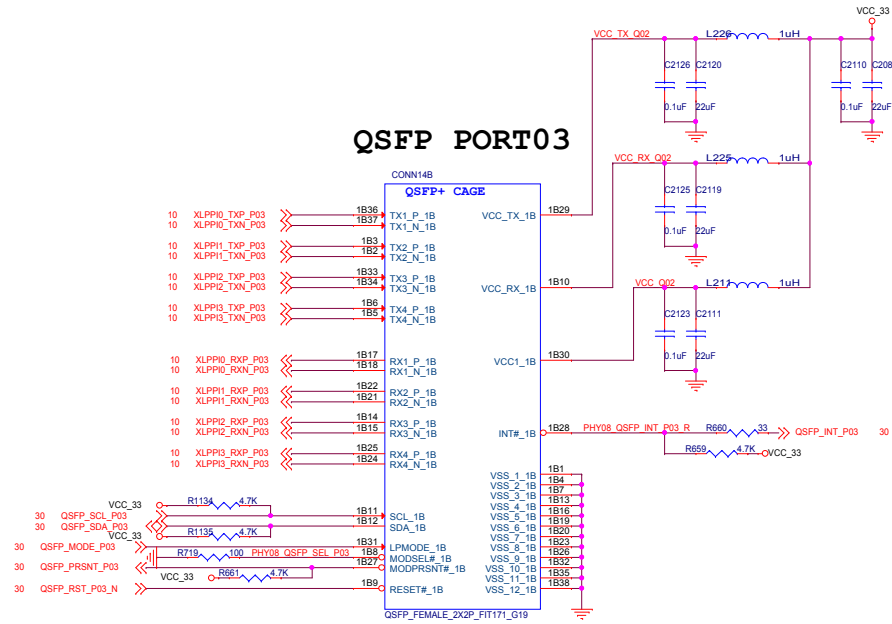
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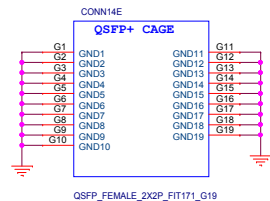
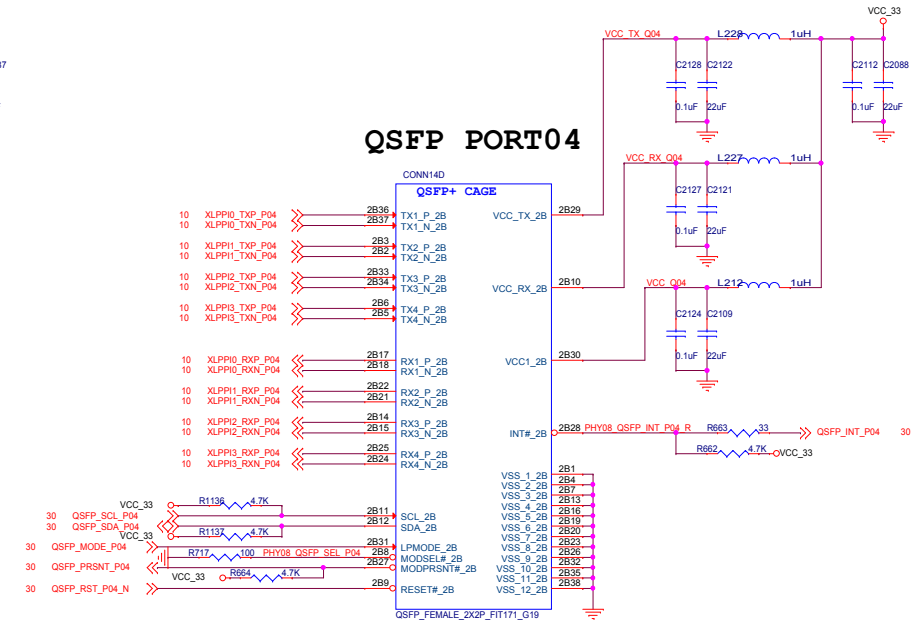
## QSFP PORT06



## QSFP PORT03



## QSFP PORT04




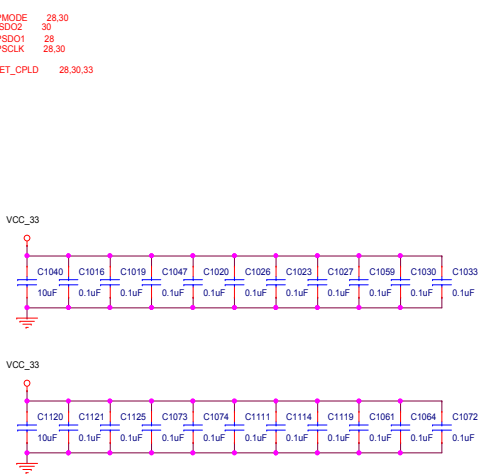
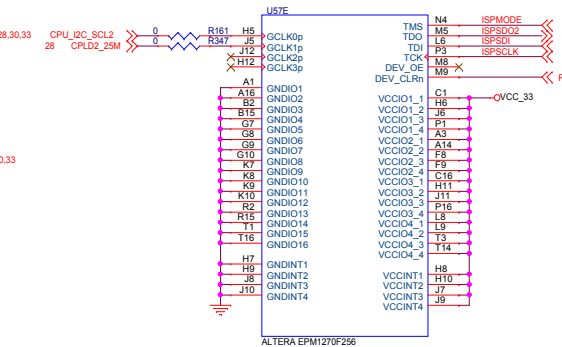
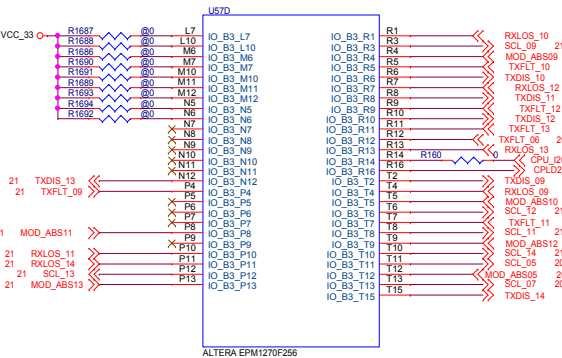
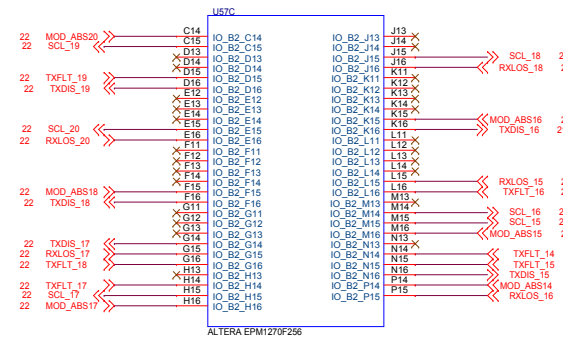
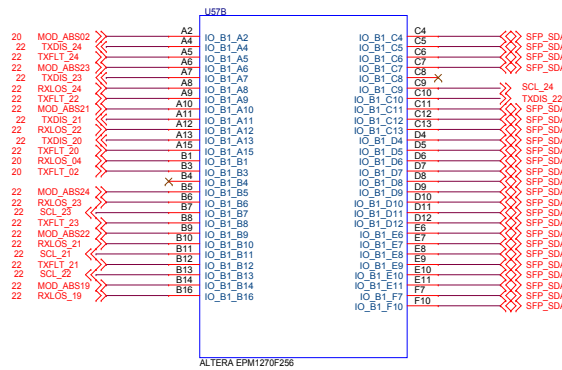
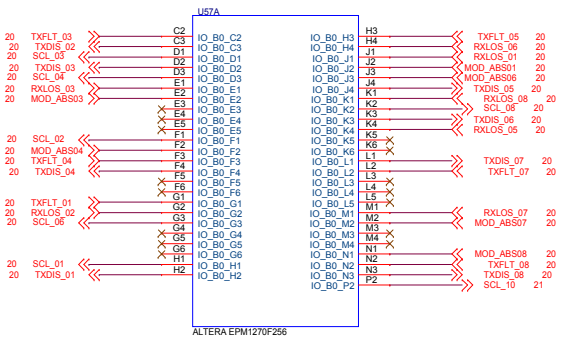
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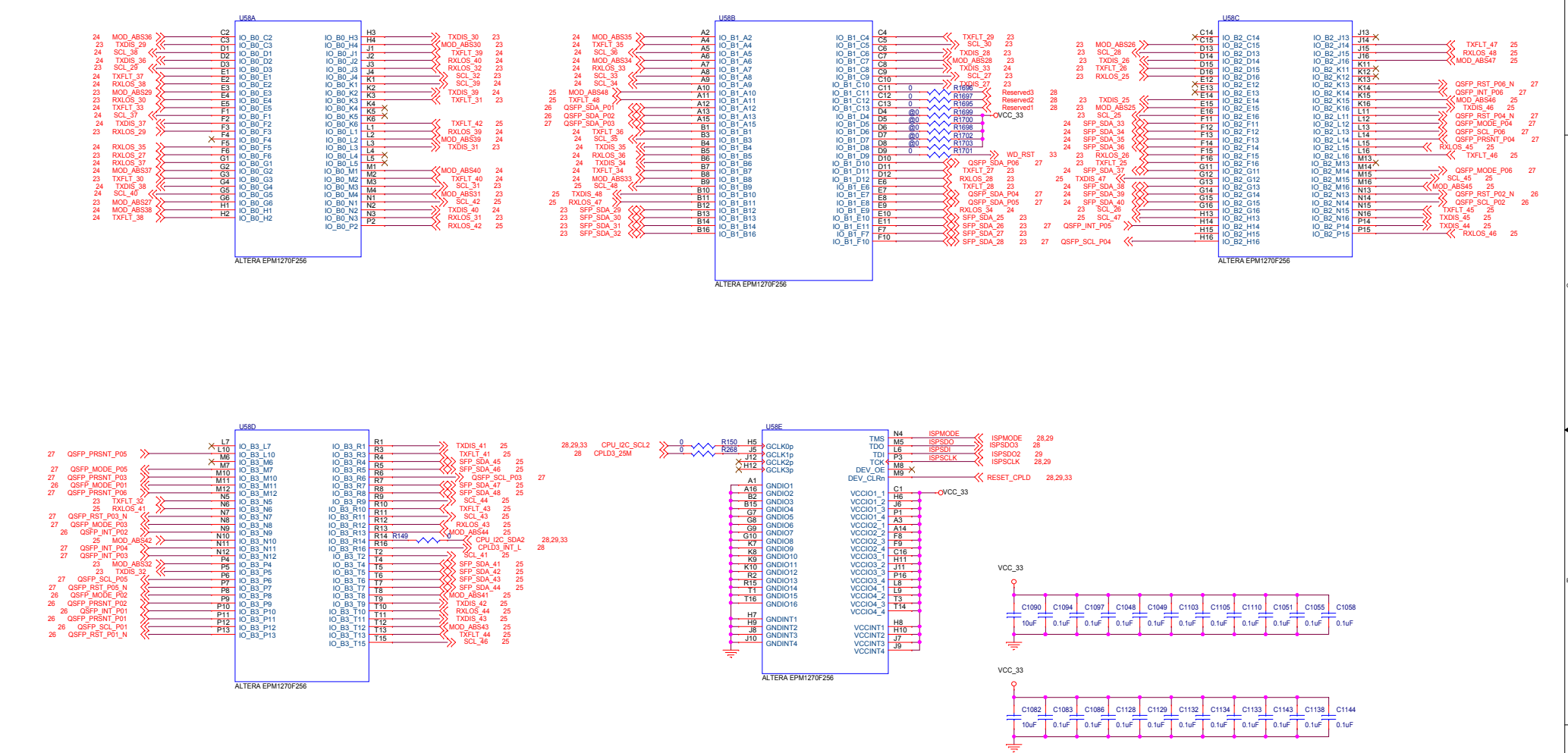


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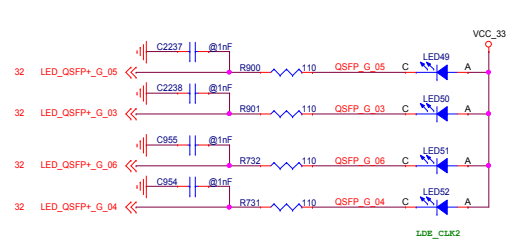
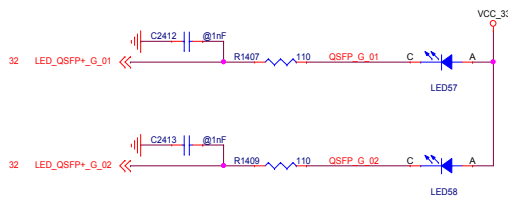
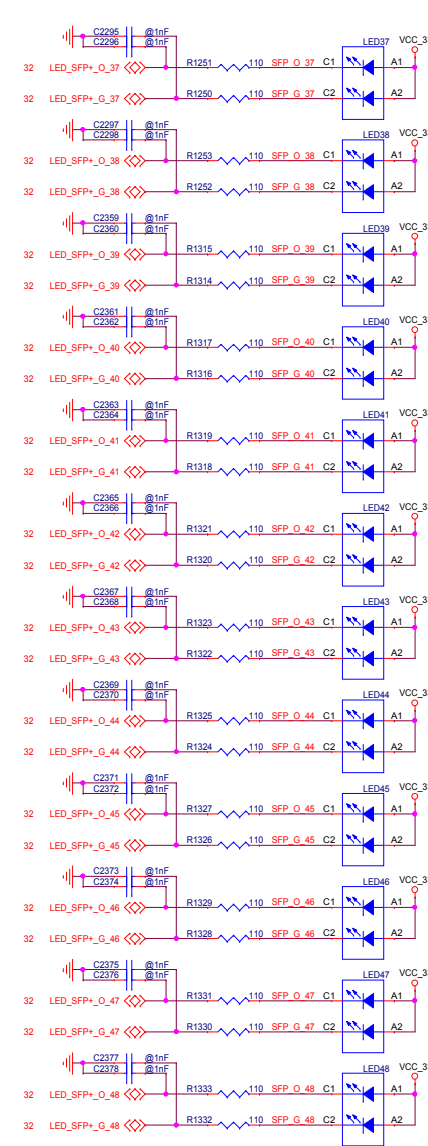
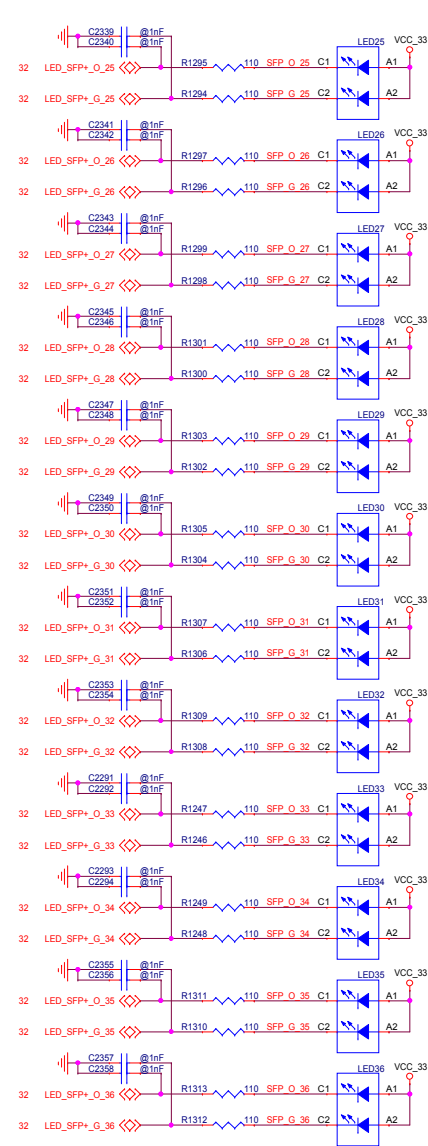
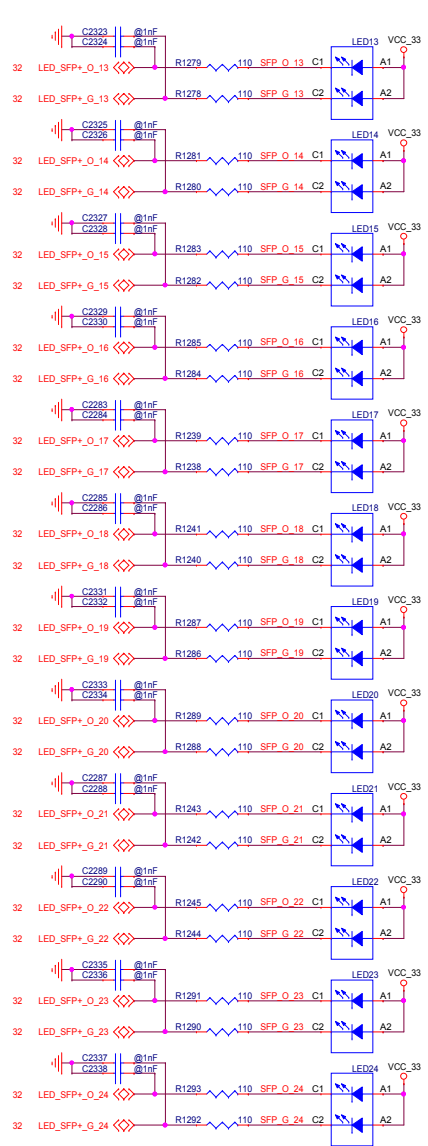
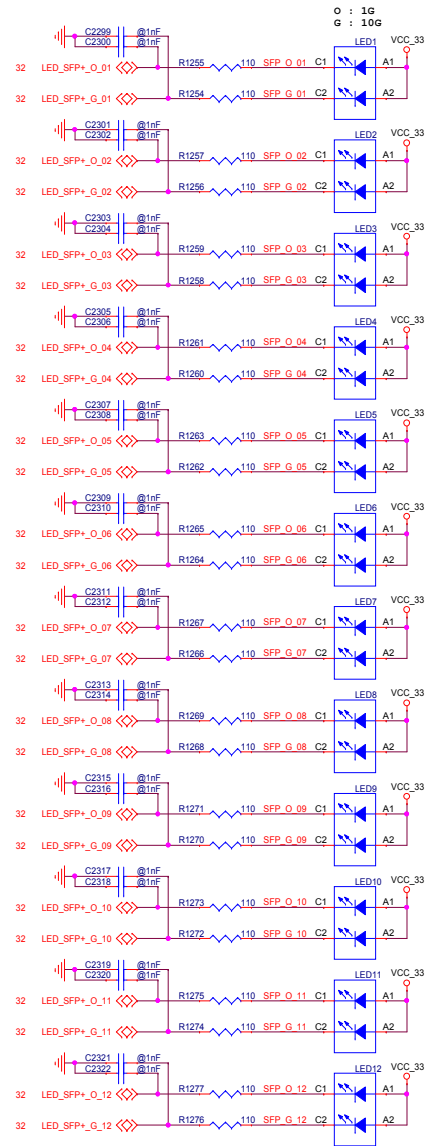


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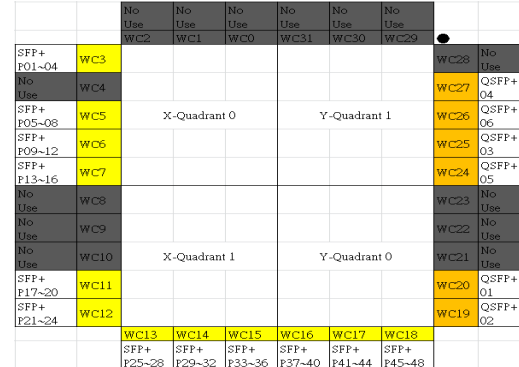
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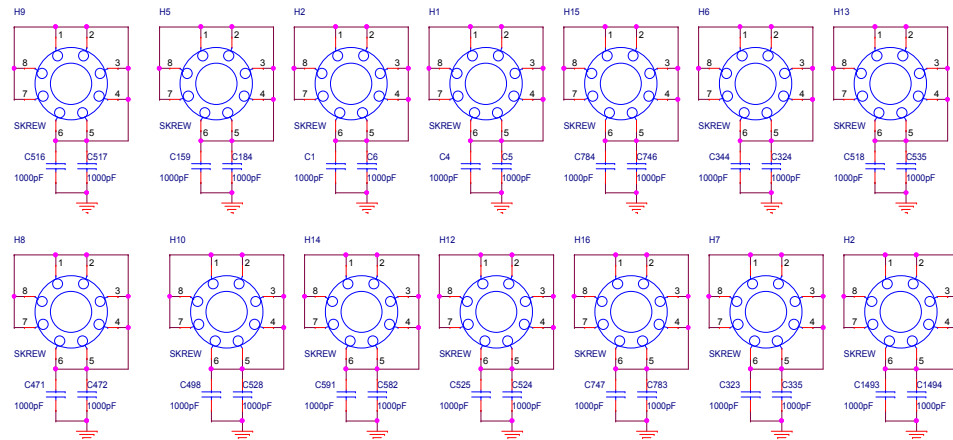
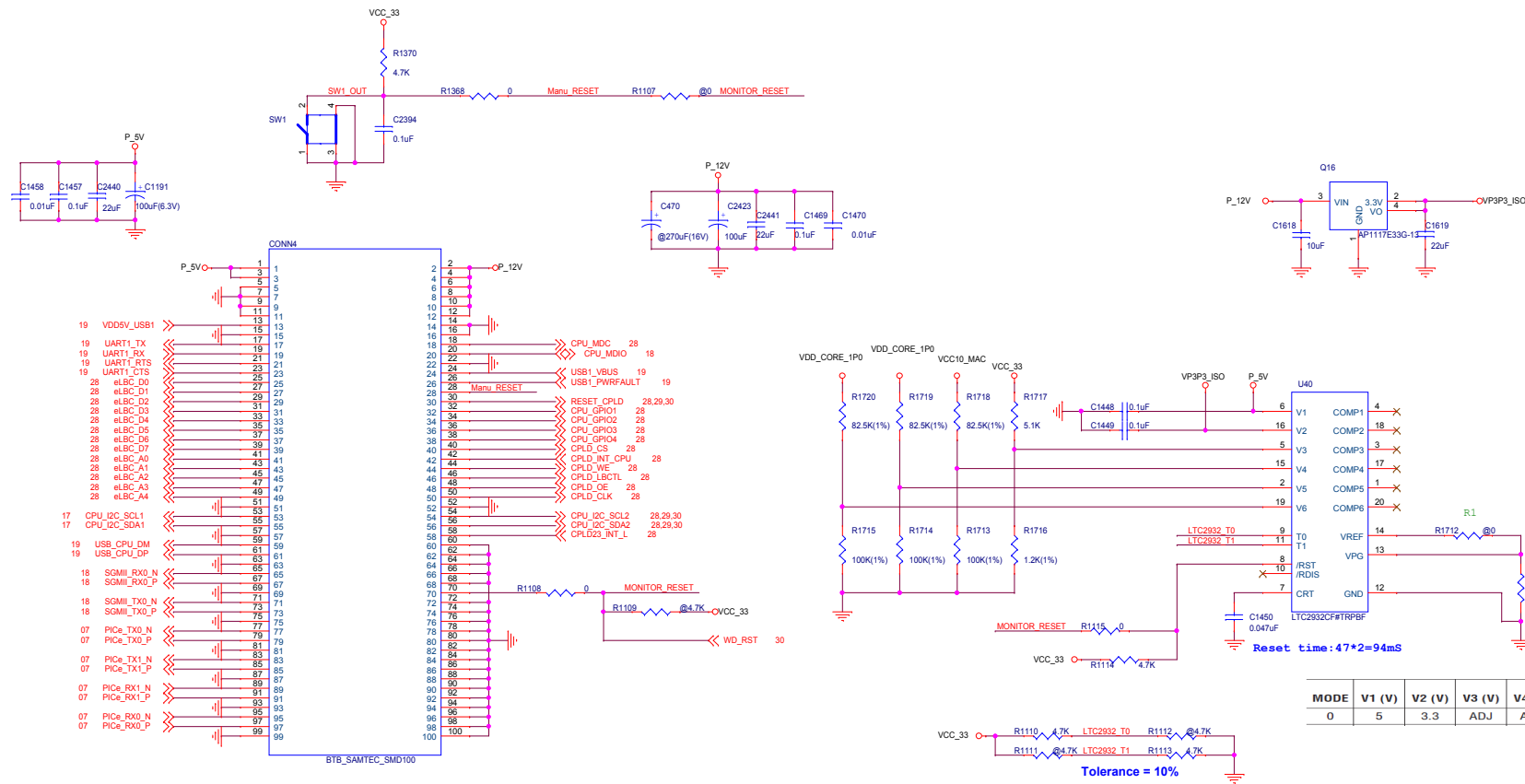
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