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History

SCH Version	Date	Description
P1A	2013/03/21	Initial Version

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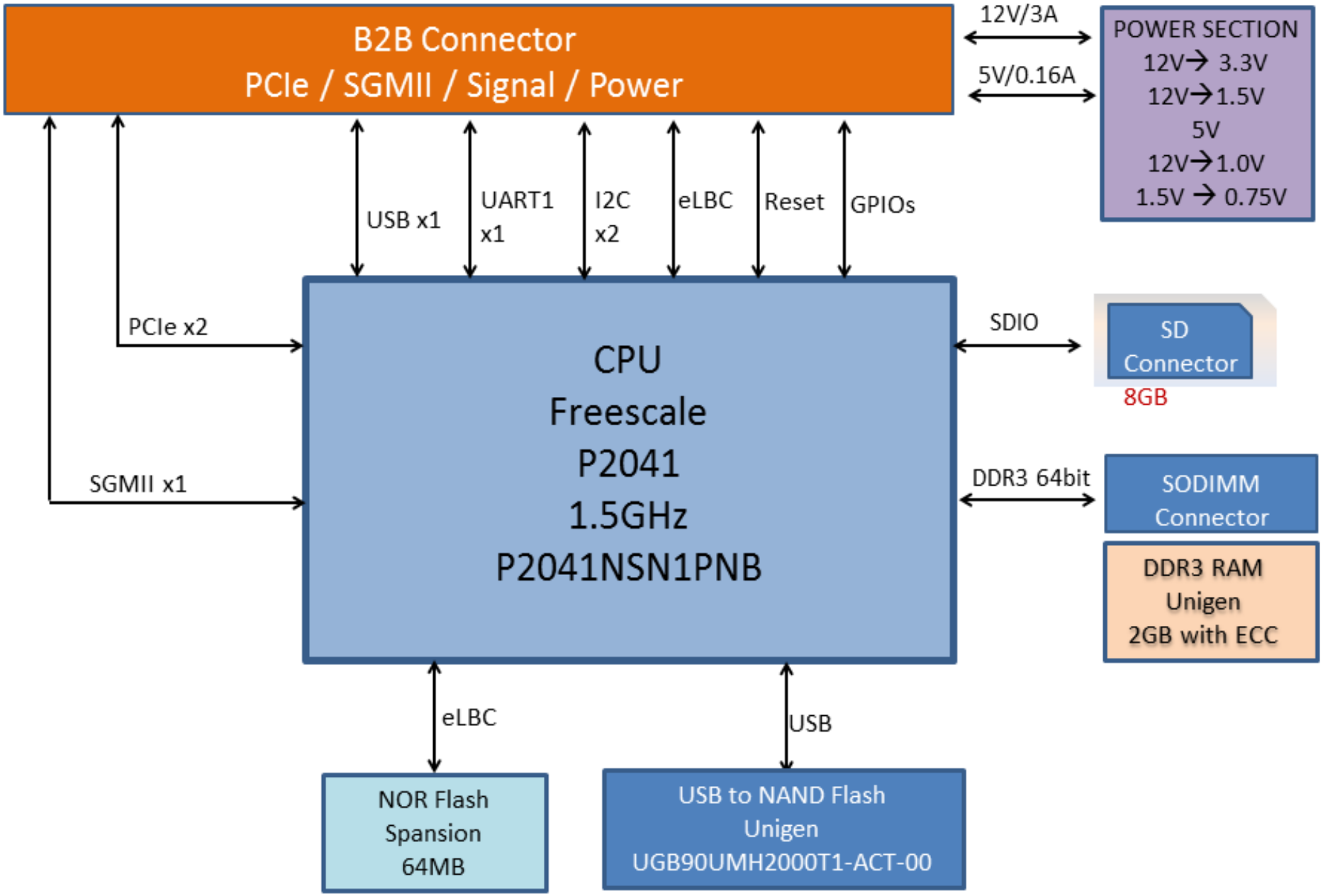

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Size: C	Page Name: Block Diagram	Engineer: Jummy Huang
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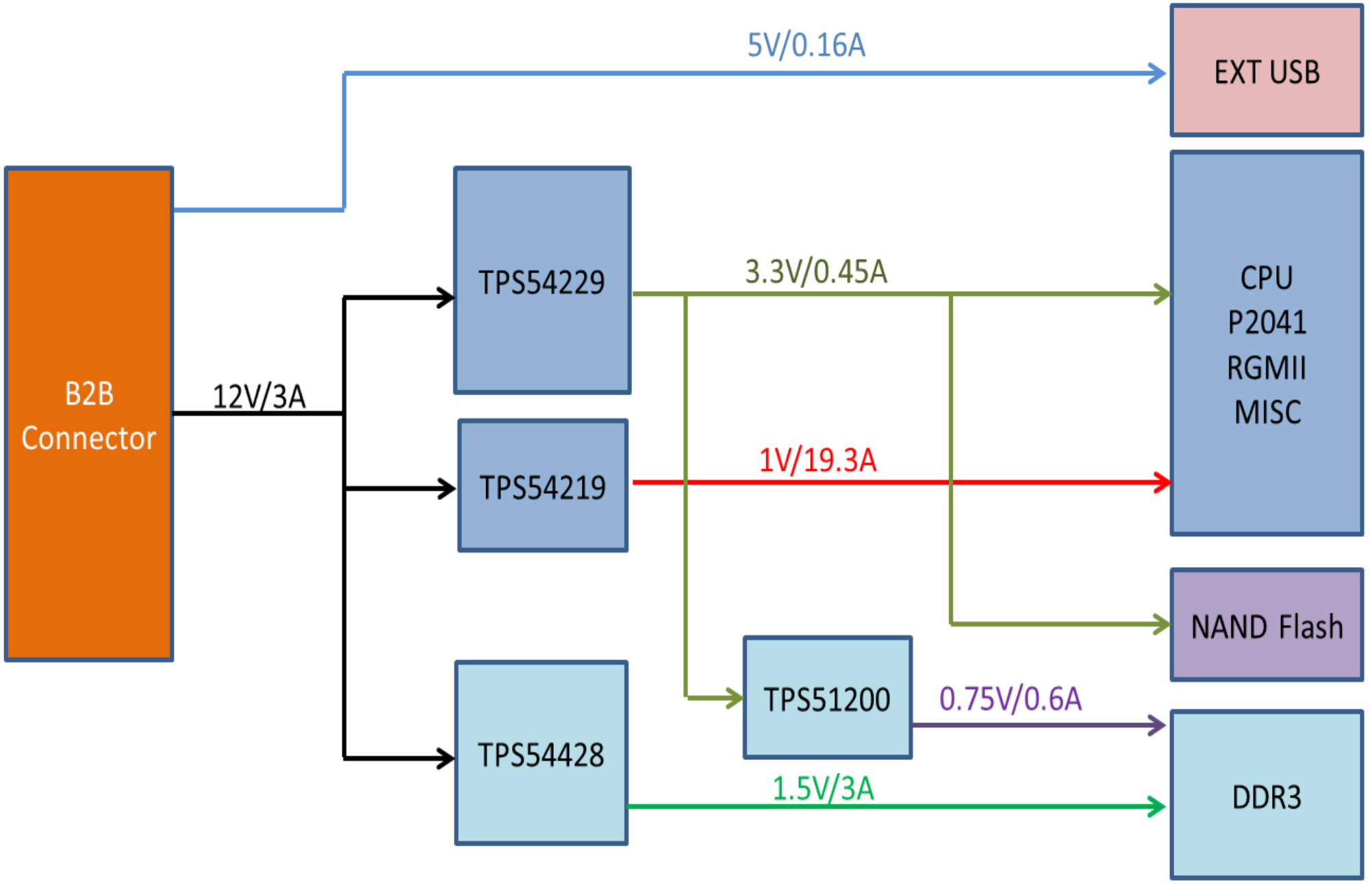

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Size	Page Name	Engineer
C	Power Tree	Jummy Huang

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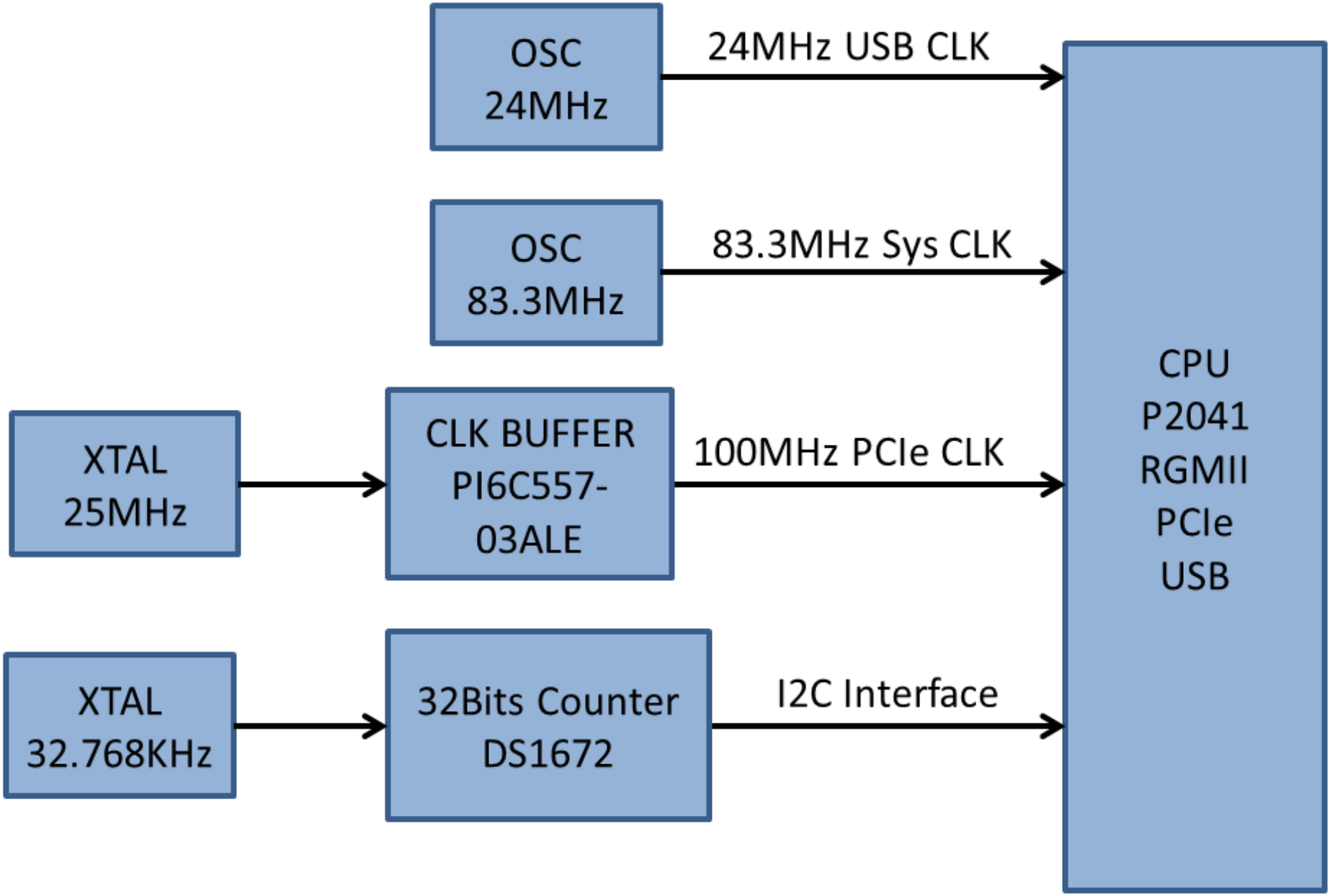

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Size	Page Name	Engineer
C	Clock Tree	Jummy Huang

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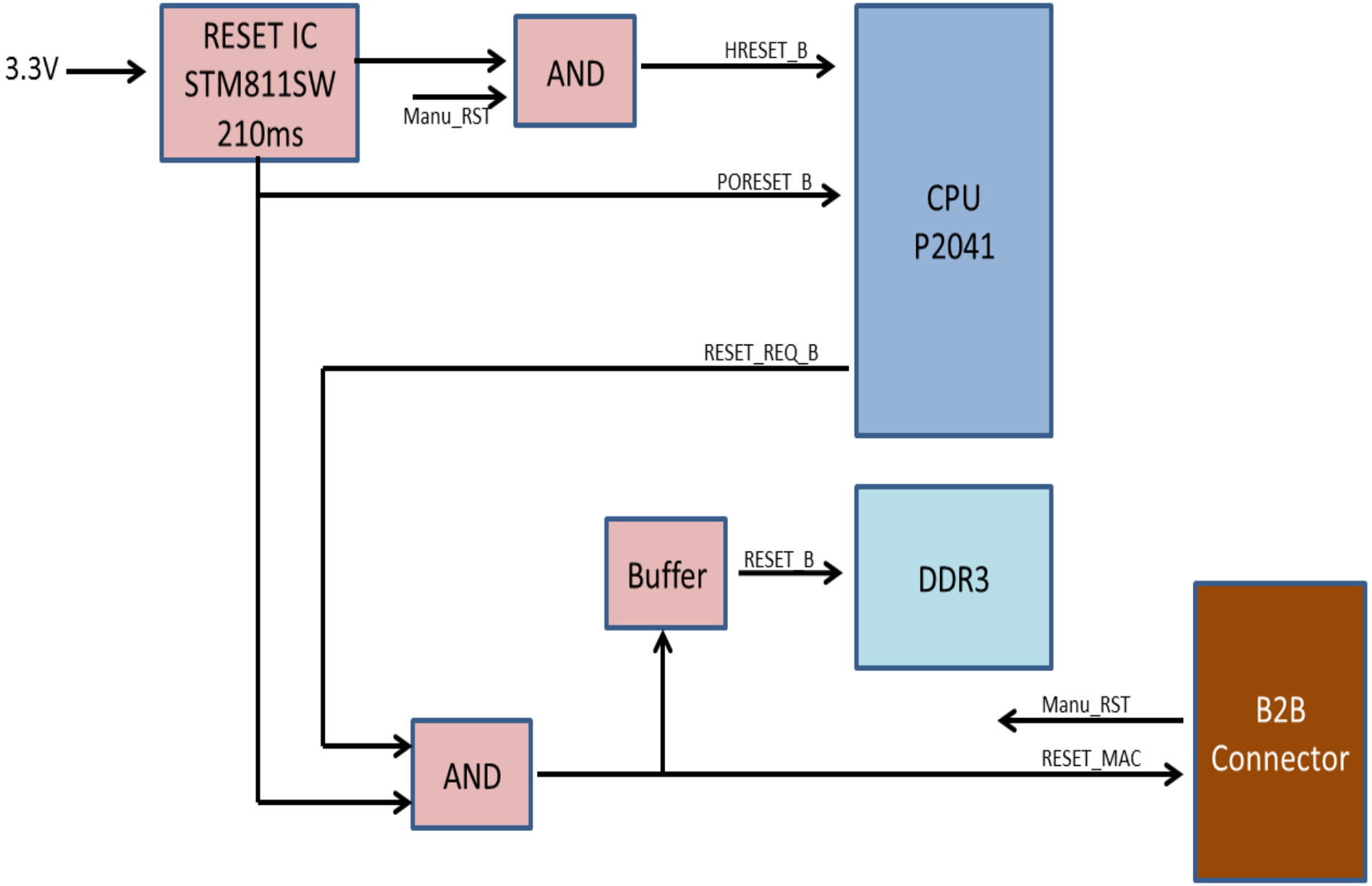

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Size	Page Name	Engineer
C	Reset Tree	Jummy Huang

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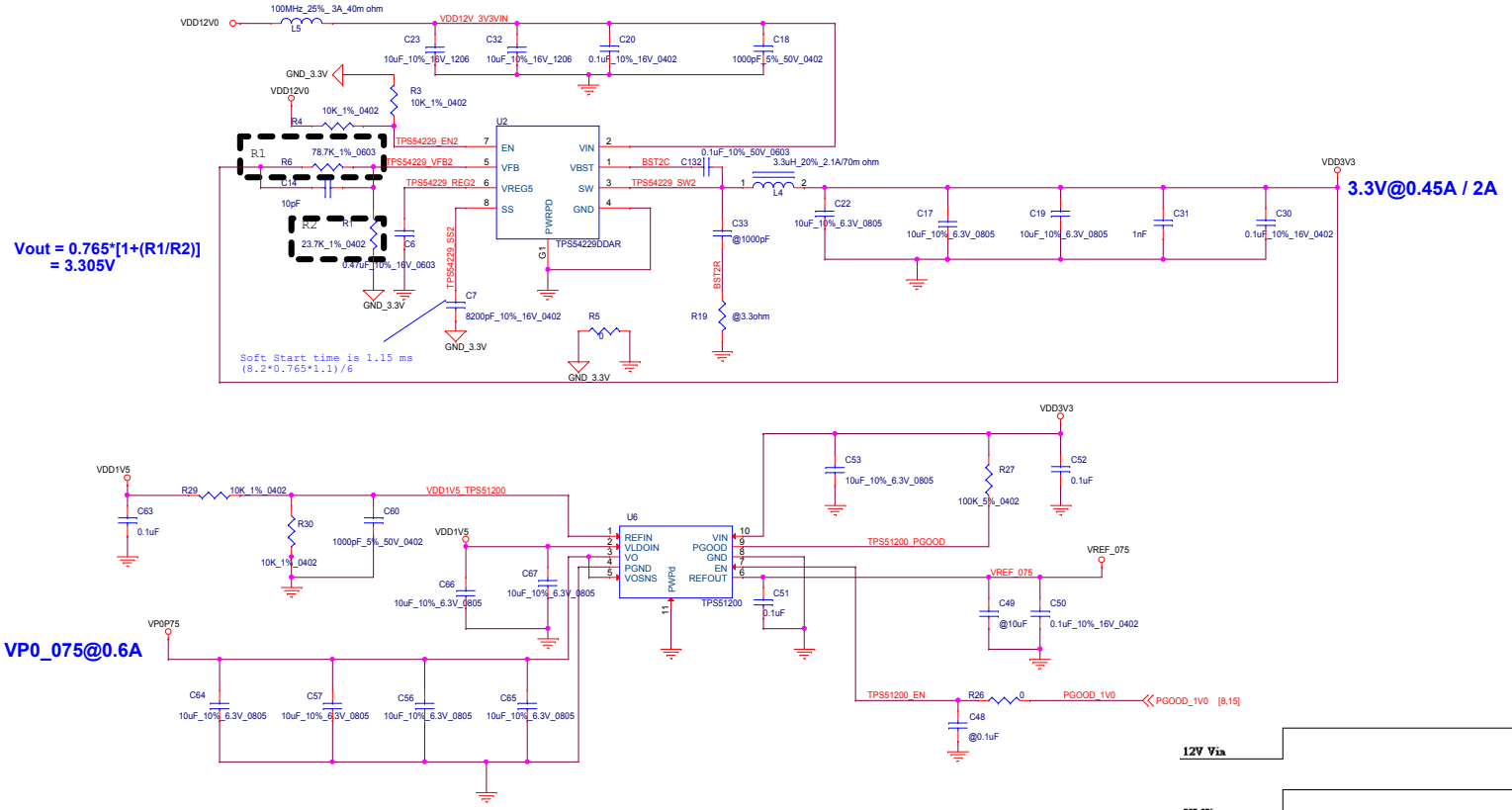
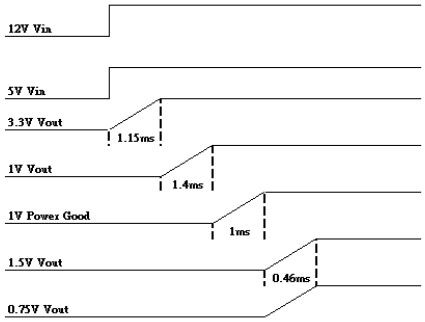
```
Power Up Sequency
1. Bring up OVDD,LVDD,BVDD,CVDD,and USB_VDD_3P3.        << 3.3V
2. Bring up VDD_CA_CB_PL, SVDD, AVDD, and USB_VDD_1P0.  << 1.0V
3. Bring up GVDD(DDR) and XVDD.                         << 1.5V
```





2.2 Power Up Sequencing

The device requires that its power rails be applied in a specific sequence in order to ensure proper device operation. These requirements are as follows for power up:

1. Bring up OV_{DD}, LV_{DD}, BV_{DD}, CV_{DD}, and USB_V_{DD}_3P3. Drive POV_{DD} = GND.
   - — $\overline{\text{PORESET}}$ input must be driven asserted and held during this step.
   - — IO_VSEL inputs must be driven during this step and held stable during normal operation.
   - — USB_V_{DD}_3P3 rise time (10% to 90%) has a minimum of 350 µs.
2. Bring up $V_{DD_CA_CB_PL}$, SV_{DD}, AV_{DD} (cores, platform, SerDes) and USB_V_{DD}_1P0. $V_{DD_CA_CB_PL}$ and USB_V_{DD}_1P0 must be ramped up simultaneously.
3. Bring up GV_{DD} (DDR) and XV_{DD}.
4. Negate $\overline{\text{PORESET}}$ input as long as the required assertion/hold time has been met per Table 16.

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Size	Page Name	Engineer
C	Power_3.3V & 0.75V	Jummy Huang

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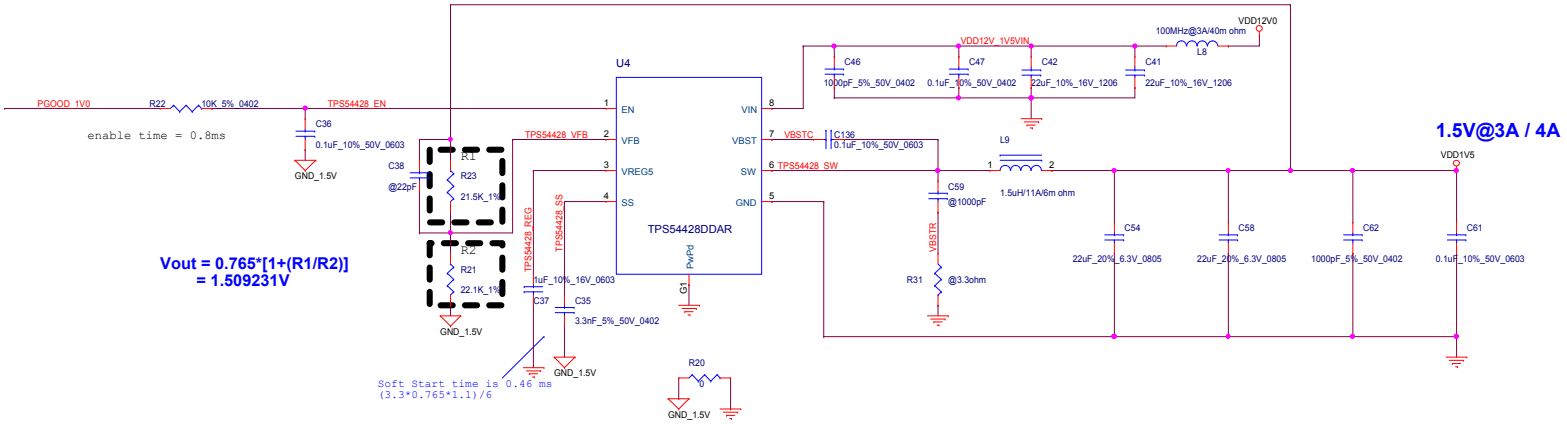

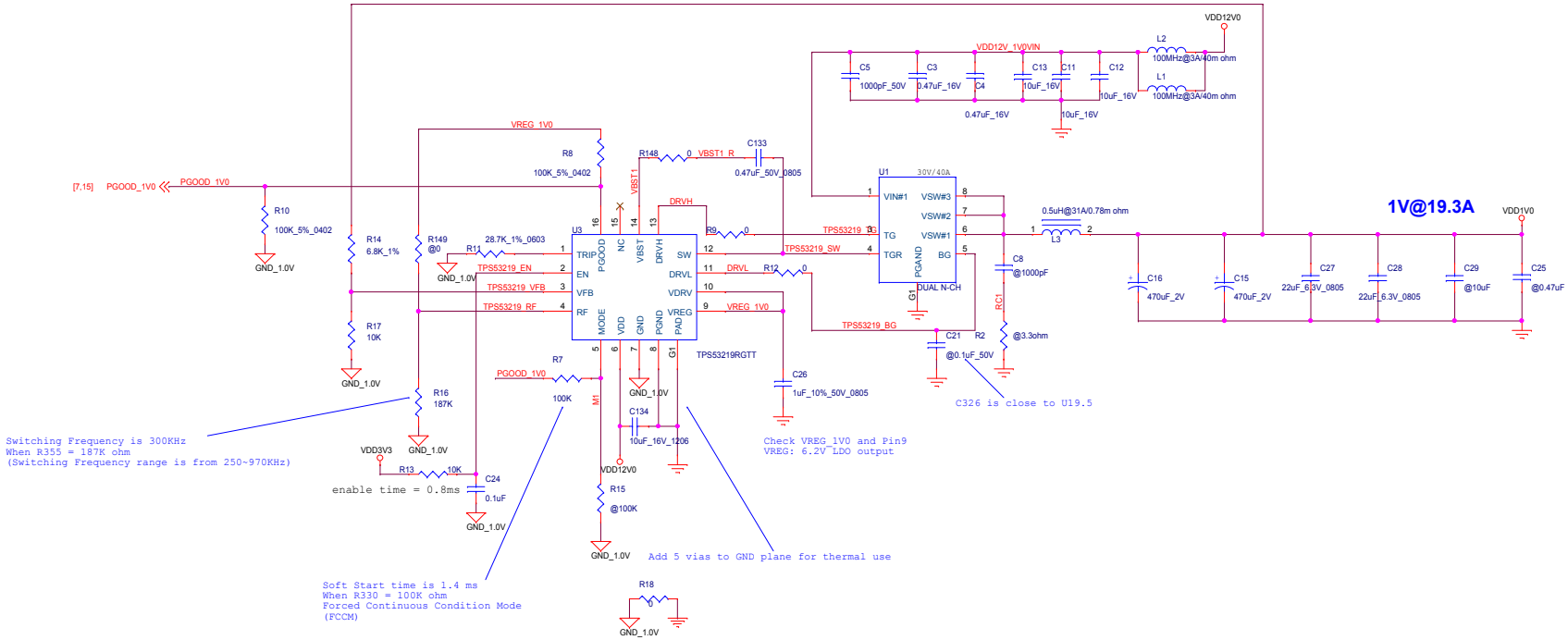

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Size	Page Name	Engineer
C	POWER 1V & 1.5	Jummy Huang

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LVDD : eTSEC1,2,3; Ethernet Management; 1588
0: 3.3V <<
1: 2.5V

BVDD[0:1] : Local Bus, GPIO[8:15]
00 : 3.3V
01 : 2.5V
10 : 1.8V
11 : 3.3V <<

CVDD[0:1] : USB, eSDHC, SPI
00 : 3.3V
01 : 2.5V
10 : 1.8V
11 : 3.3V <<

IO_VSEL[4:0] = 00000
==>BVDD:3.3V,CVDD:3.3V,LVDD:3.3V

Temp Sensor I2C1ADDRESS:
"0011000" = 18H

RTC I2C1ADDRESS:
"1101000" = 68H

JTAG

TCK pulled up by 5-10K
TMS pulled up by 5-10K
TDI pulled up by 5-10K
TRST# ANDed with PORESET#
COP pin 2 NC / short to GND
COP pin 5 (QREQ#) pulled up by 5-10K
COP pin 15 (CKSTP_OUT) pulled up by 5-10K
COP pin 6 connect to 3.3V by 10ohm for current limiting

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Size	Page Name	Engineer
C	CPU MISC	Jummy Huang

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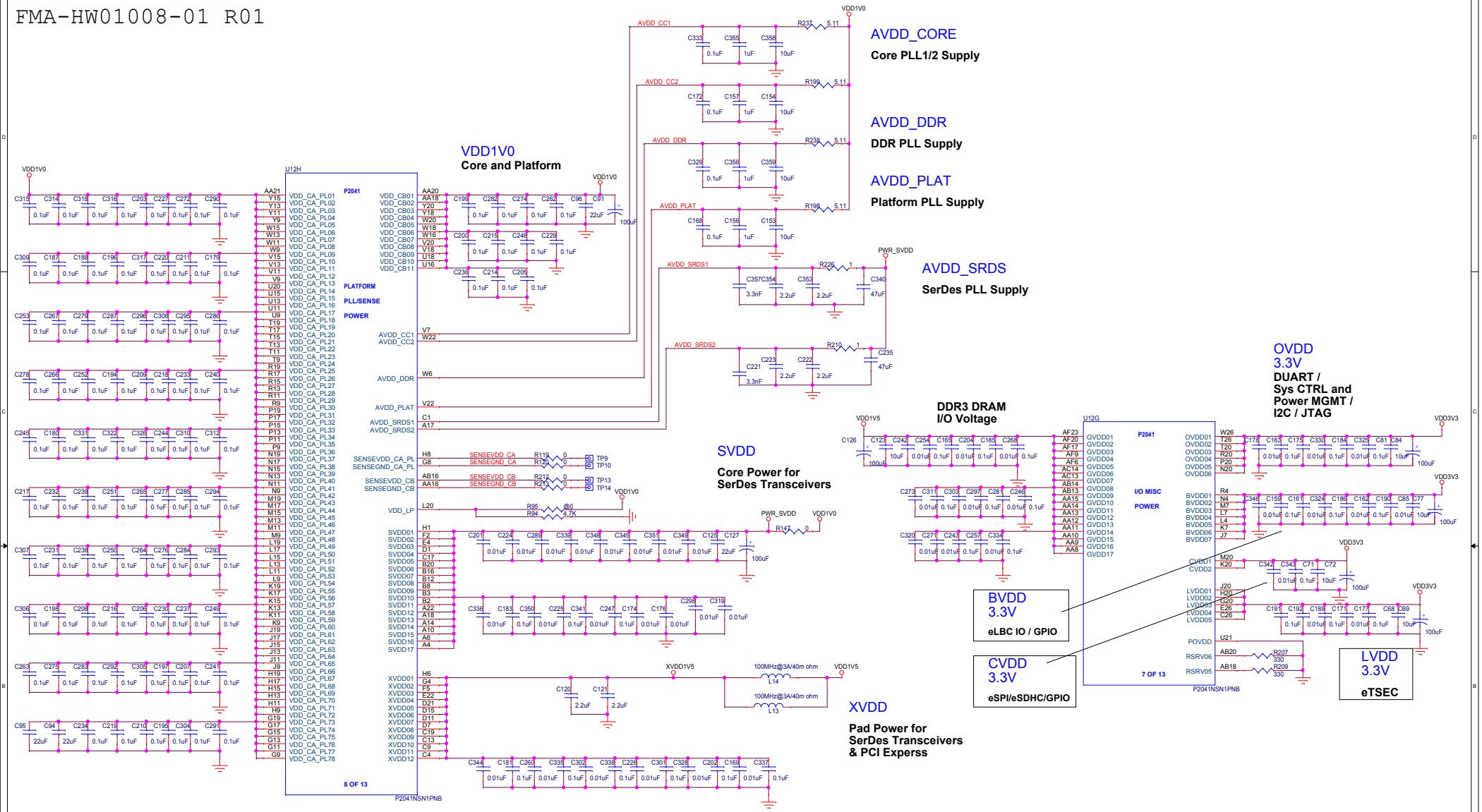

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Size	Page Name	Engineer
C	CPU Power	Jummy Huang

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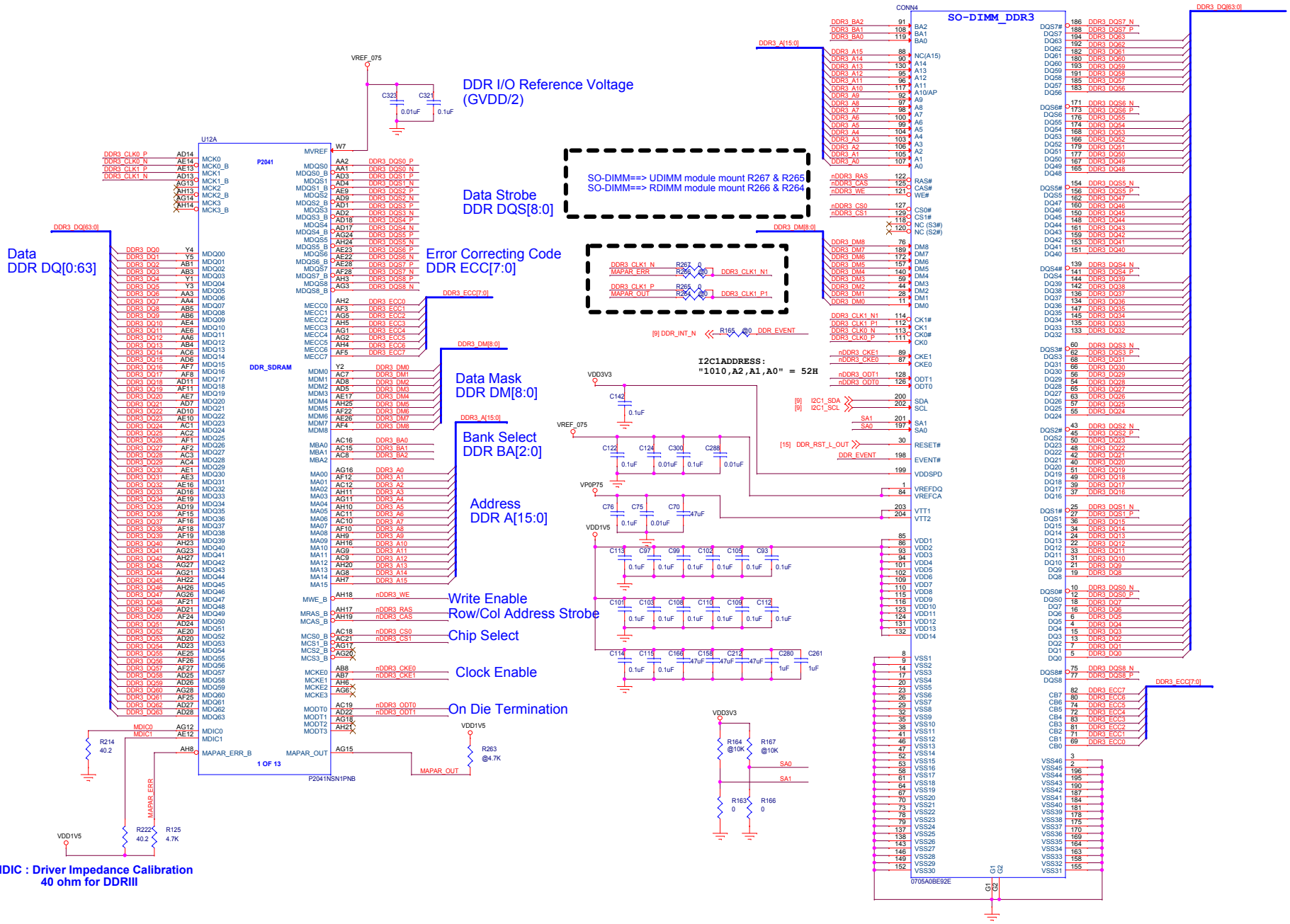

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Size	Page Name	Engineer
C	CPU MEMORY	Jummy Huang

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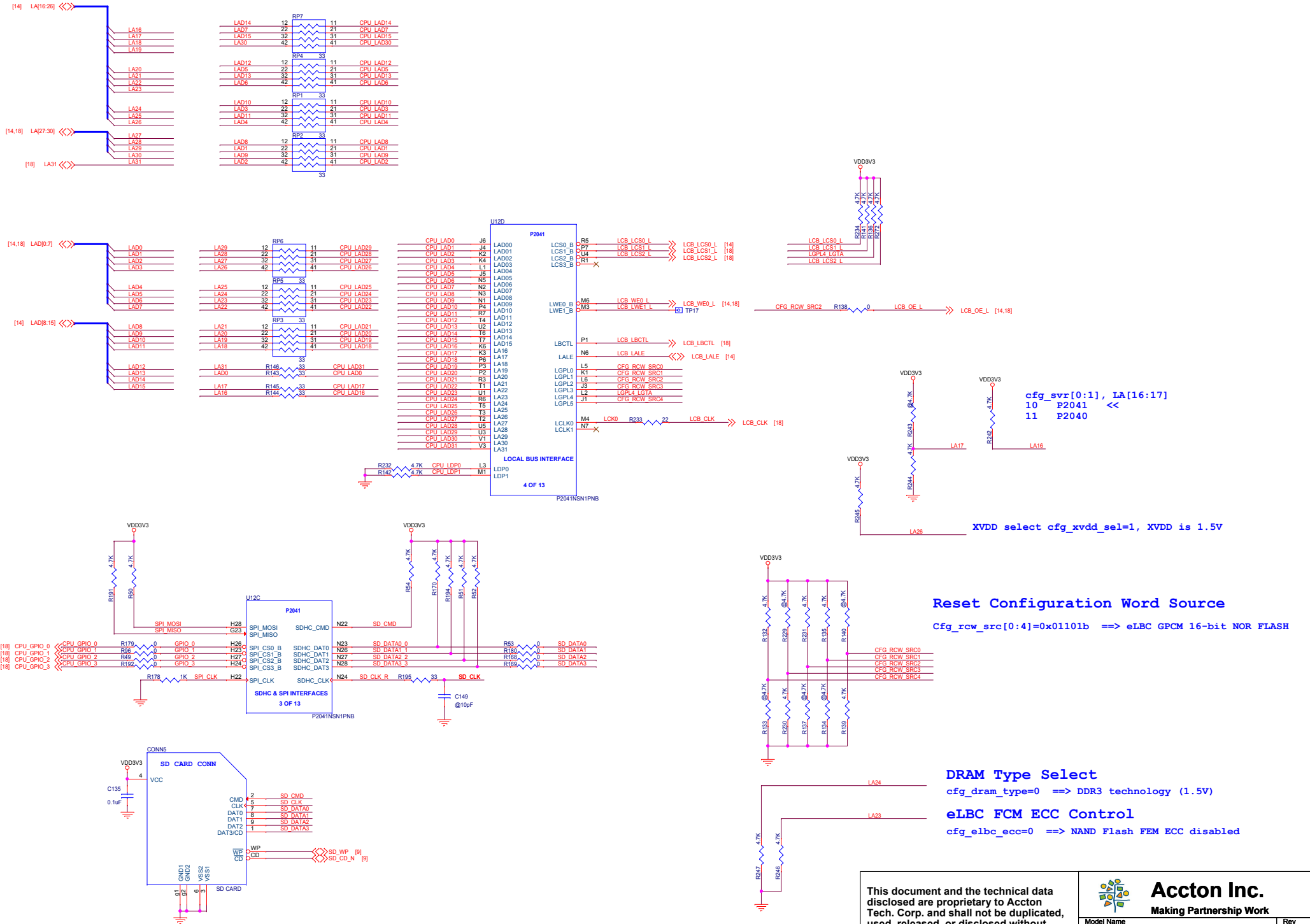

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Size	Page Name	Engineer
C	CPU LOCAL BUS	Jummy Huang

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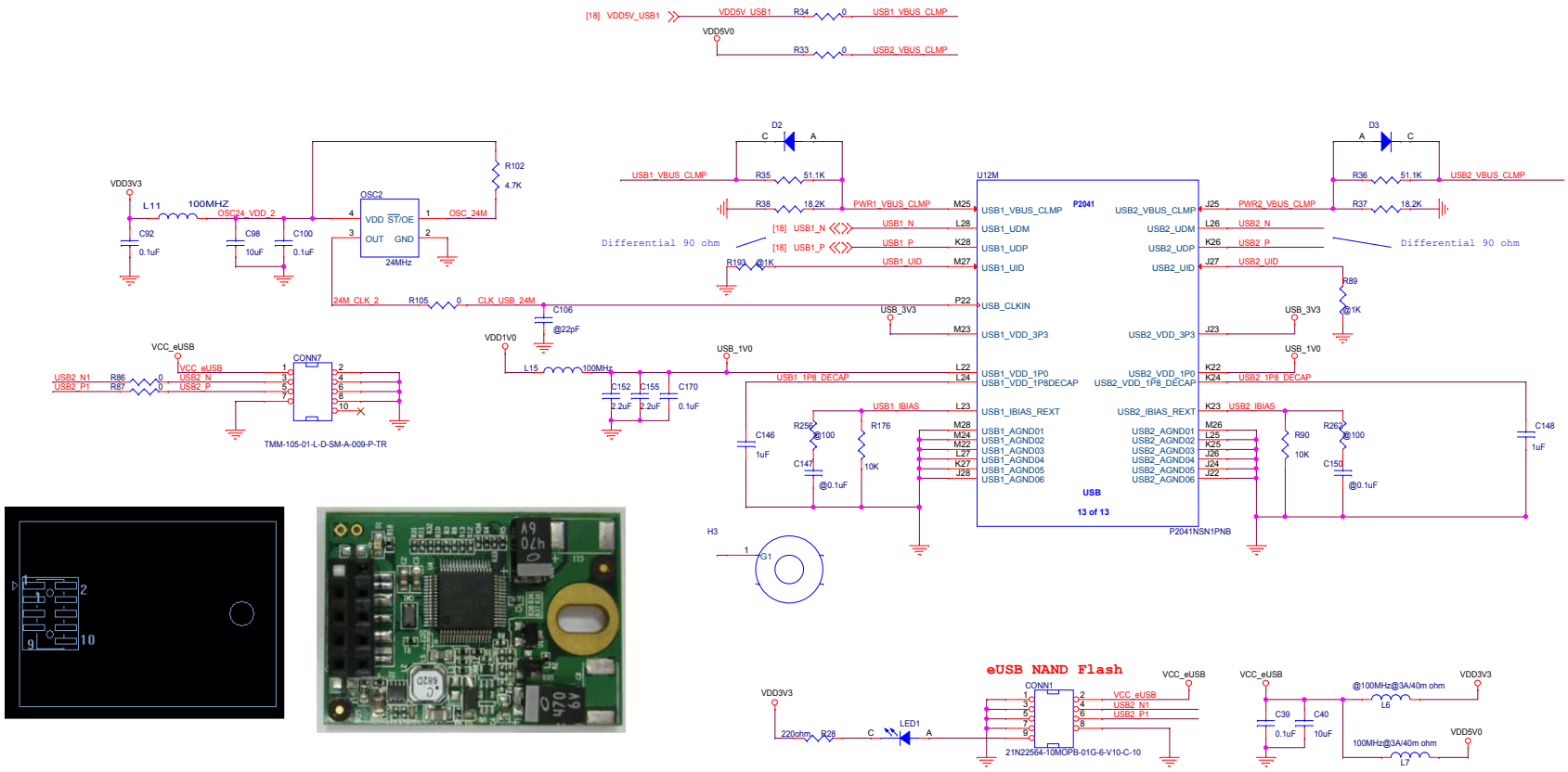

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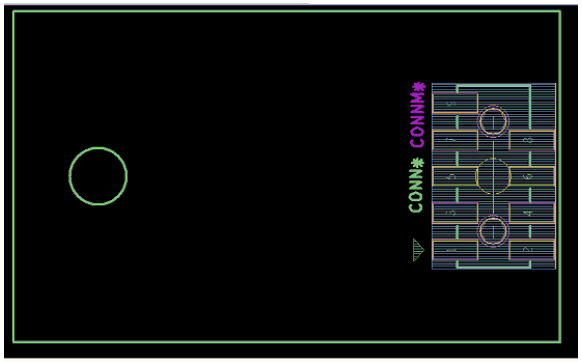

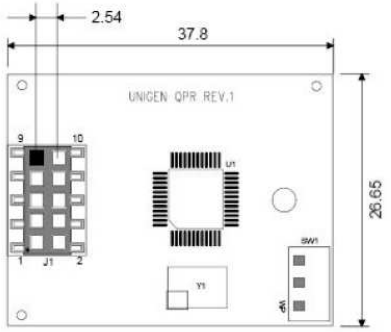

Horizontal Type Left side

Table 2-2: 10 pin USB Connector Pin Assignments and Description

Pin No.	Signal	Signal Types	Function
1	VCC	PWR	Input Power
3	D-	I/O	Differential Signal
5	D+	I/O	Differential Signal
7	VSS	GND	Ground
9			Key
2,4,6,8		NC	No Connect
10	LED	I/O	Activity

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C	CPU USB & NAND Flash	Jummy Huang

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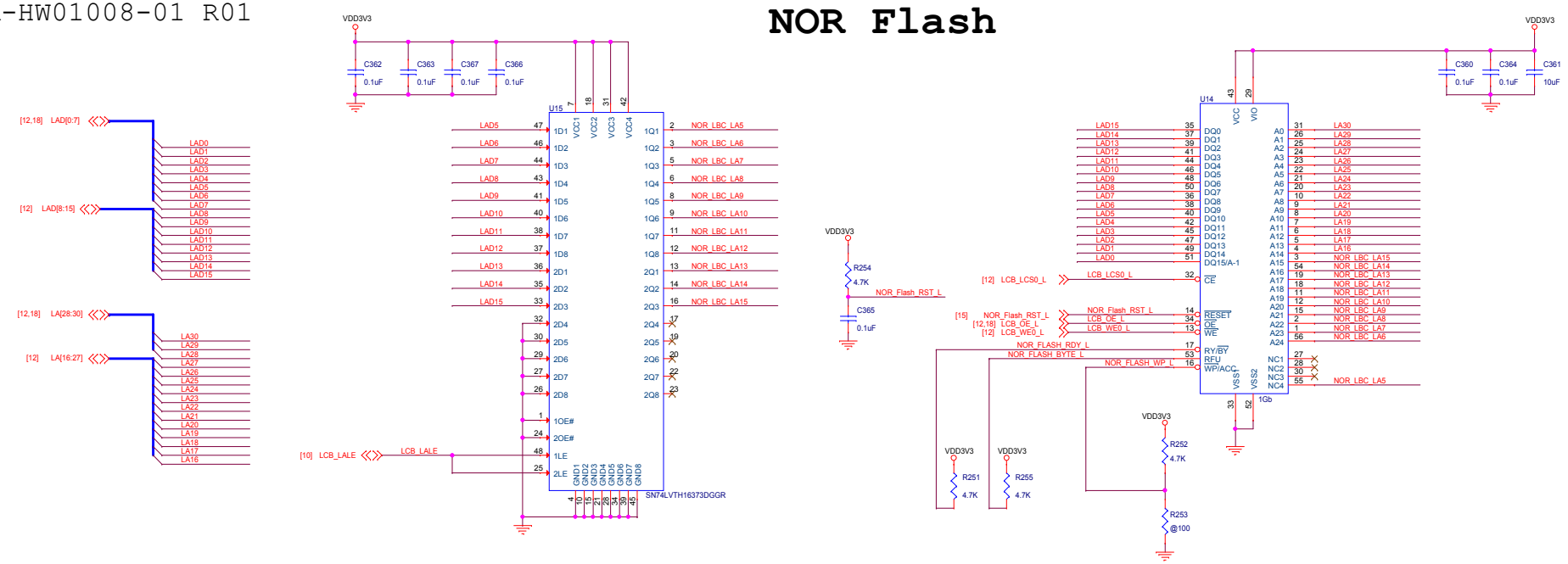
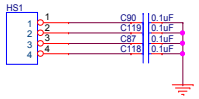
NOR Flash



Heak Hink for P2041 (U1)
50mm x 50mm x 14mm



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Size	Page Name	Engineer
C	NOR Flash	Jummy Huang

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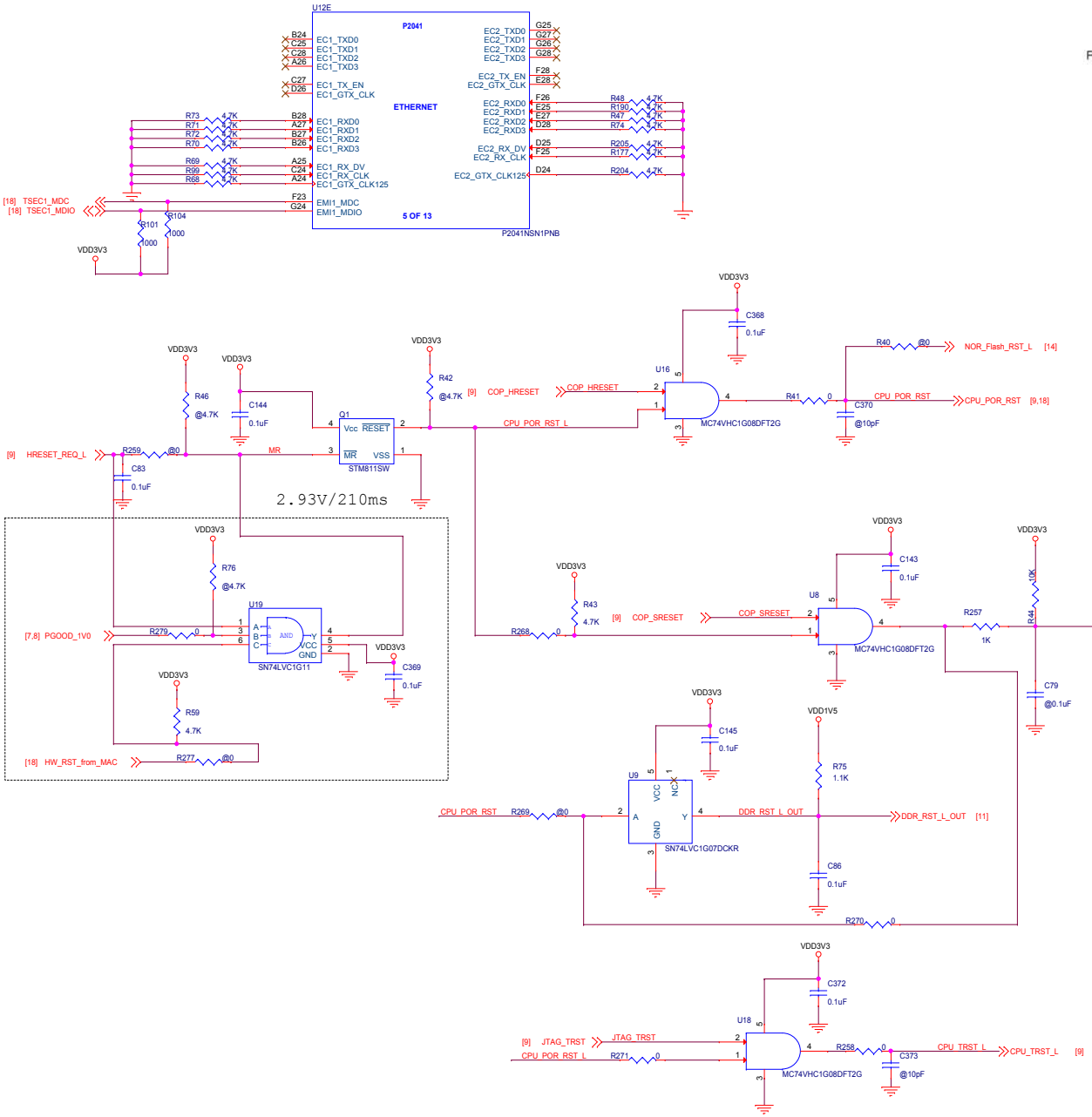

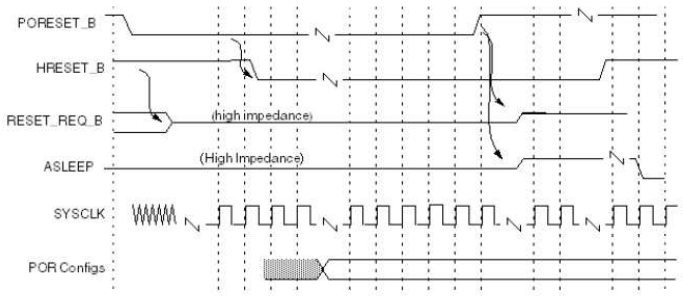

Figure 4-22. Power-On Reset Sequence

Table 16. RESET Initialization Timing Specifications

Parameter	Min	Max	Unit[1]	Note
Required assertion time of $\overline{\text{PORESET}}$	1	—	ms	3
Required input assertion time of $\overline{\text{HRESET}}$	32	—	SYSCLKs	1, 2
Input setup time for POR configs with respect to negation of $\overline{\text{PORESET}}$	4	—	SYSCLKs	1
Input hold time for all POR configs with respect to negation of $\overline{\text{PORESET}}$	2	—	SYSCLKs	1
Maximum valid-to-high impedance time for actively driven POR configs with respect to negation of $\overline{\text{PORESET}}$	—	5	SYSCLKs	1

Note:

1. SYSCLK is the primary clock input for the device.
2. The device asserts $\overline{\text{HRESET}}$ as an output when $\overline{\text{PORESET}}$ is asserted to initiate the power-on reset process. The device releases $\overline{\text{HRESET}}$ sometime after $\overline{\text{PORESET}}$ is negated. The exact sequencing of $\overline{\text{HRESET}}$ negation is documented in Section 4.4.1, "Power-On Reset Sequence," in the chip reference manual.
3. $\overline{\text{PORESET}}$ must be driven asserted before the core and platform power supplies are powered up. Refer to Section 2.2, "Power Up Sequencing."

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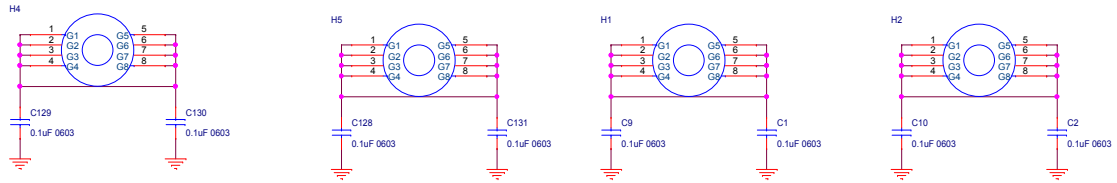

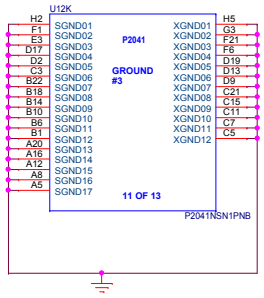

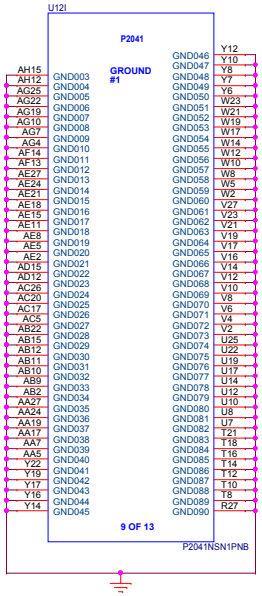

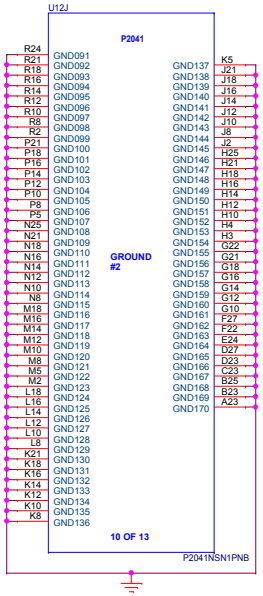

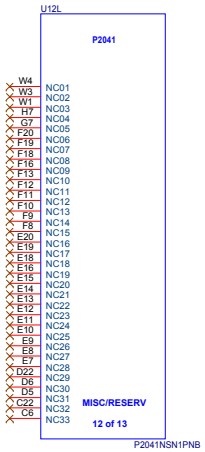

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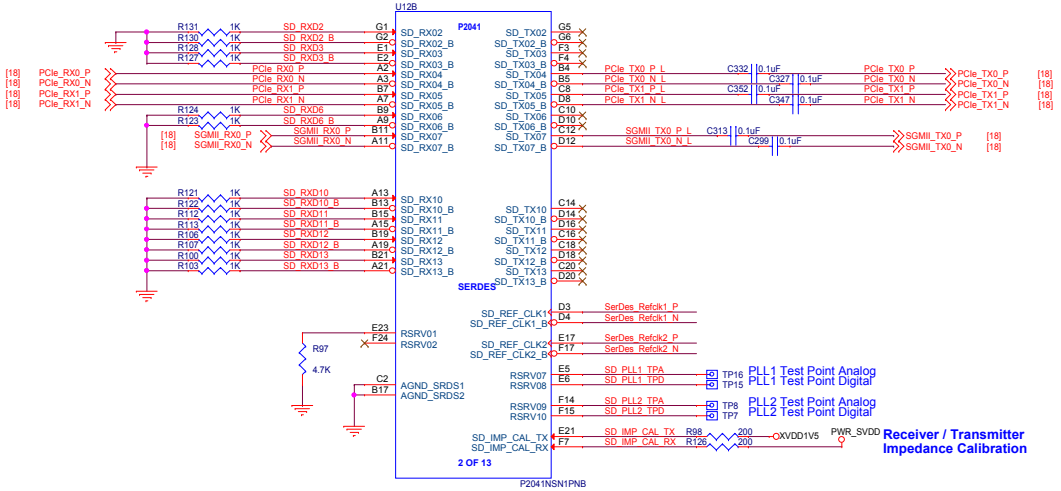
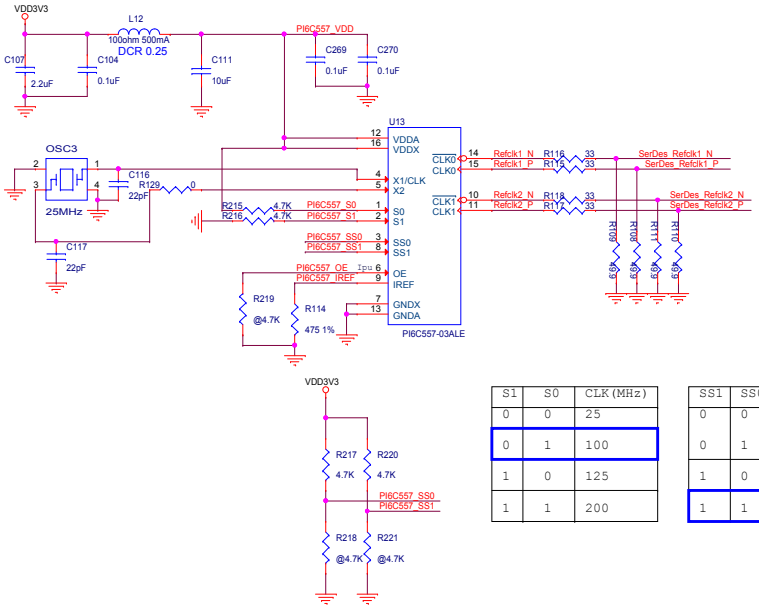
Table 4. P2040/P2041 SerDes lane multiplexing/configuration (continued)

SRDS_PRTCL	Bank 1						Bank 2			
	C	D	E	F	G	H	A	B	C	D
0x14	SGMII1 (1.25G)	SGMII2 (1.25G)	PCIe2 (5/2.5G)		sRIO1 (5/2.5G)		Debug (5/3.125/ 2.5G) [1]	SGMII5 (1.25G or 3.125G) [1]	SGMII3 1.25G or 3.125G) [1]	SGMII4 1.25G or 3.125G) [1]
0x15	SGMII1 (1.25G)	SGMII2 (1.25G)	PCIe2 (5/2.5G)	sRIO2 (5/2.5G)	sRIO1 (5/2.5G)				SATA1 (3/1.5G)	SATA2 (3/1.5G)
0x16	PCIe1 (5/2.5G)	PCIe3 (5/2.5G)	PCIe2 (5/2.5G)		SGMII3 (1.25G)	SGMII4 (1.25G)			SATA1 (3/1.5G)	SATA2 (3/1.5G)
0x17	**PCIe1 (5/2.5G)**	**PCIe3 (5/2.5G)**	**PCIe2 (5/2.5G)**		**SGMII3 (1.25G)**	**SGMII4 (1.25G)**	**XAUI 10GEC (P2041 only, P2040 does not support 10 GEC)**			
0x18	PCIe1 (5/2.5G)	PCIe3 (5/2.5G)	sRIO2 (5/2.5G)		SGMII3 (1.25G)	SGMII4 (1.25G)			SATA1 (3/1.5G)	SATA2 (3/1.5G)





S1	S0	CLK(MHz)
0	0	25
0	1	100
1	0	125
1	1	200

SS1	SS0	Spread
0	0	Center +/- 0.25
0	1	Down -0.5
1	0	Down -0.75
1	1	No Spread

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P09_CPU_MISC

[9] UART1_RXD — UART1_RXD
[9] UART1_TXD — UART1_TXD
[9] UART1_RTS — UART1_RTS
[9] UART1_CTS — UART1_CTS
[9] CPLD2_INT_L — CPLD2_INT_L
[9] CPLD_INT_L — CPLD_INT_L
[9] USB1_5V_EN — USB1_5V_EN
[9] USB1_PWRFAULT — USB1_PWRFAULT
[9] I2C2_SCL — I2C2_SCL
[9] I2C2_SDA — I2C2_SDA
[9] I2C4_SCL — I2C4_SCL
[9] I2C4_SDA — I2C4_SDA

P12_CPU_LOCAL_BUS

[12] CPU_GPIO_0 — CPU_GPIO_0
[12] CPU_GPIO_1 — CPU_GPIO_1
[12] CPU_GPIO_2 — CPU_GPIO_2
[12] CPU_GPIO_3 — CPU_GPIO_3
[12] LCB_CLK — LCB_CLK
[12] LCB_LBCTL — LCB_LBCTL
[12,14] LCB_WE0_L — LCB_WE0_L
[12] LCB_LCS1_L — LCB_LCS1_L
[12,14] LCB_OE_L — LCB_OE_L
[18] LCB_LCS2_L — LCB_LCS2_L

P13_CPU USB & NAND FLASH

[13] VDD5V_USB1 — VDD5V_USB1
[13] USB1_N — USB1_N
[13] USB1_P — USB1_P

P15_CPU Ethernet & Reset

[15] TSEC1_MDC — TSEC1_MDC
[15] TSEC1_MDIO — TSEC1_MDIO
[15] CPU_POR_RST — CPU_POR_RST
[9] Manu_RST — Manu_RST
[15] HW_RST_from_MAC — HW_RST_from_MAC

P17_CPU_PCIE

[17] PCIe_RX0_P — PCIe_RX0_P
[17] PCIe_RX0_N — PCIe_RX0_N
[17] PCIe_RX1_P — PCIe_RX1_P
[17] PCIe_RX1_N — PCIe_RX1_N
[17] PCIe_TX0_P — PCIe_TX0_P
[17] PCIe_TX0_N — PCIe_TX0_N
[17] PCIe_TX1_P — PCIe_TX1_P
[17] PCIe_TX1_N — PCIe_TX1_N

[18] SGMII_TX0_P — SGMII_TX0_P
[18] SGMII_TX0_N — SGMII_TX0_N

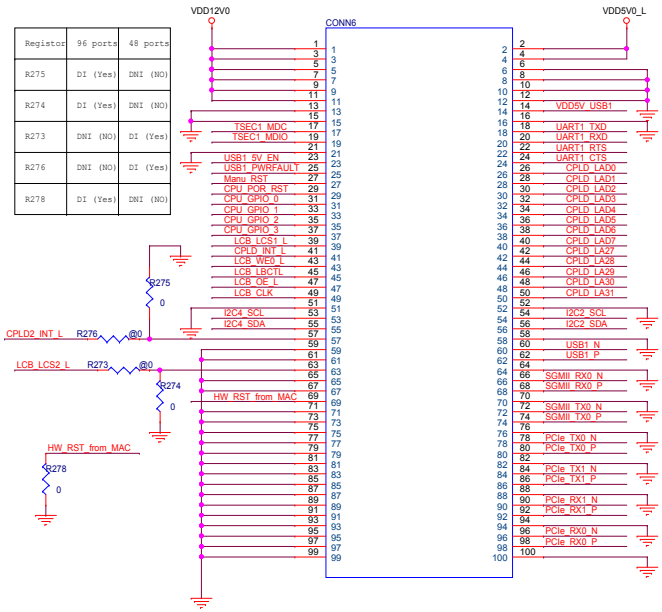
[15] SGMII_RX0_P — SGMII_RX0_P
[15] SGMII_RX0_N — SGMII_RX0_N

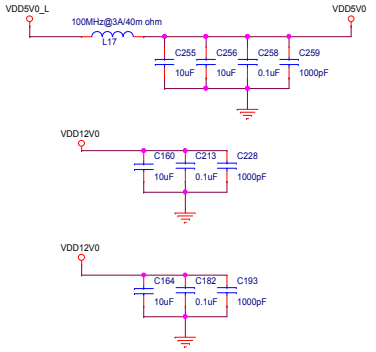
P12_CPU_LOCAL_BUS

[12] LAD[0:7]
LAD0 — R223 0 — CPLD_LAD0
LAD1 — R224 0 — CPLD_LAD1
LAD2 — R225 0 — CPLD_LAD2
LAD3 — R227 0 — CPLD_LAD3
LAD4 — R228 0 — CPLD_LAD4
LAD5 — R235 0 — CPLD_LAD5
LAD6 — R236 0 — CPLD_LAD6
LAD7 — R239 0 — CPLD_LAD7

[12] LA[27:30]
LA27 — R240 0 — CPLD_LA27
LA28 — R241 0 — CPLD_LA28
LA29 — R248 0 — CPLD_LA29
LA30 — R249 0 — CPLD_LA30
[12] LA31 — LA31 — R250 0 — CPLD_LA31

Register	96 ports	48 ports
R275	DI (Yes)	DNI (NO)
R274	DI (Yes)	DNI (NO)
R273	DNI (NO)	DI (Yes)
R276	DNI (NO)	DI (Yes)
R278	DI (Yes)	DNI (NO)





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Accton Inc.
Making Partnership Work

Model Name	Rev
ES56A4BT-FLF-ZZ/ES5696BT-FLF-AO	R02

Size	Page Name	Engineer
C	B2B CONNECTOR	Jummy Huang

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