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Compute Project

Wiwynn 19” 2U Server System “Carmel” (2U4N) v0.5

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1 Revision History

Date	Name	Description
16-Feb-01	Jackie Lee	Version 0.5

2 Scope

This specification of this project describes how to integrate an Open Compute Project motherboard "Open_Compute_Project_FB_Server_Intel_Motherboard_v3.1" spec into an EIA 19" 2U chassis with 4 or 2 server nodes. And all components, Server Sled, Drives, PSUs , Fans of this system are mechanically designed for ease-of-configure and ease-of-maintain.

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5 Overview

When the Open Compute Project proves its efficiency in the energy consumption, reliability and cost for data centers, its demand grows time to time. However, Open Compute Project defined Open Rack spec which is basically different than conventional rack. Open rack is 21" width and 1.8" (48mm) height of each Open Unit (OU) comparing with EIA-19" rack unit in a 1.75" (47.5mm) height. To accommodate OCP project means a new investment in a new segment for traditional data centers. This project communicates the agreed upon requirements and product specifications to utilize OCP certified mother board and new system design for an EIA 19" rack to adapt with existing rack investment of data centers.

Based on a component of "Open_Compute_Project_FB_Server_Intel_Motherboard_v3.1" ("the motherboard"), this project integrates 4 or 2 server nodes into a 2-RU chassis to act as a high-density computing system. Specification of the motherboard is available in http://www.opencompute.org/wiki/Server/SpecsAndDesigns

The components including Server Sleds, PSUs, Fans, and Drives are capable of front access or hot pluggable characteristics for easy system maintenance and management.

6 System Overview

The project is an EIA-19" 2U rack mount design, high-density server with built-in 4 server nodes in one chassis which is named 2U4N. The mother board is OCP certified so the project can benefit from OCP technologies and converge conventional rack architecture of data centers. Key features of the system are highlighted in Table 1.

Table 1. System Key Features

System Specification	**2U4N**
Chassis Dimension	2RU, 448mm (W) x 87.6mm (H) x 800mm (D)
Sled for Server Node	4 Nodes, Front serviceable
Fan	4 pcs Dual rotor 8056 fans, 3+1 redundant
PSU	2 pcs 1600W, 1+1 redundant, 86 mm x 196 mm (Platinum)
Server Node Specification	**2U4N**
CPU	Dual socket Intel Xeon E5-2600 v4
TDP	135W
DIMM	16 pcs DDR4 ECC RDIMM, 1600/1867/2133/2400 MT/s
NIC Mezz	10/25/40/50Gb Mezzanine card
Management LAN	. 1 pc Dedicated 1G BaseT, or Shared Mezz NIC; . IPMI v2.0/iKVM support, via AST2400
HDD/SSD support	. 1 pc M.2 SATA SSD . 1 pcs 2.5" (9.5 mm) HDD/SSD, Front serviceable
PCIe add-on card	1 pc PCIe 3.0 x16, FHHL
USB 3.0	1 pc External; 1 pc Internal port

Figure 1 and Figure 2 illustrate the system overview and front view.

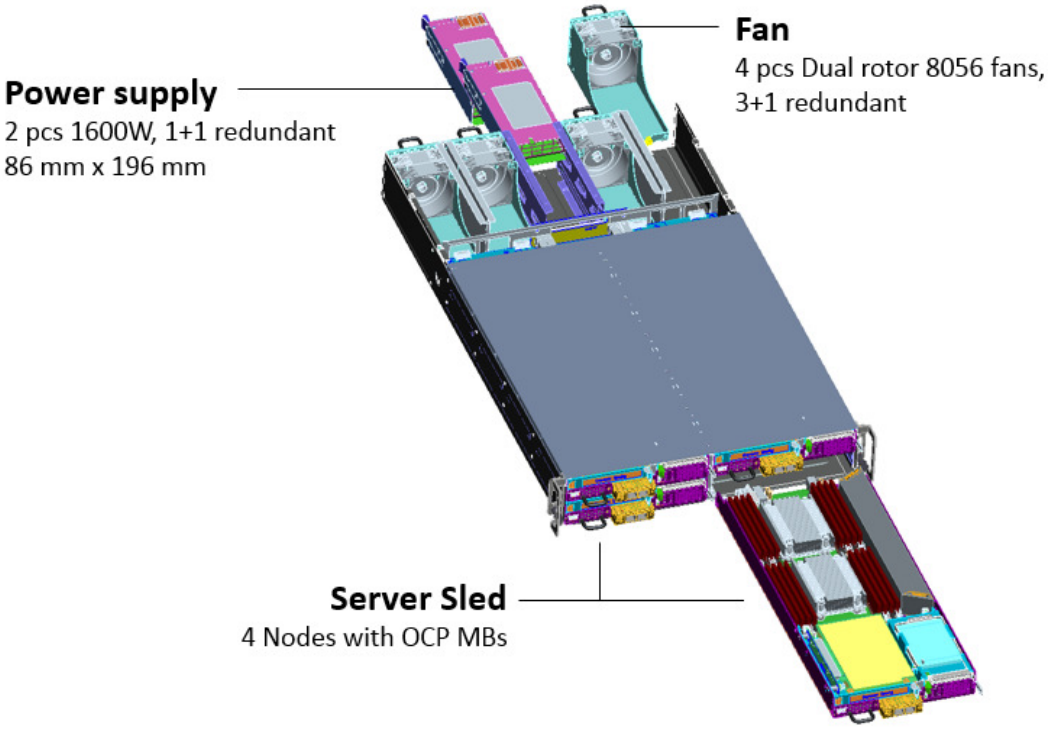


Figure 1 System Overview

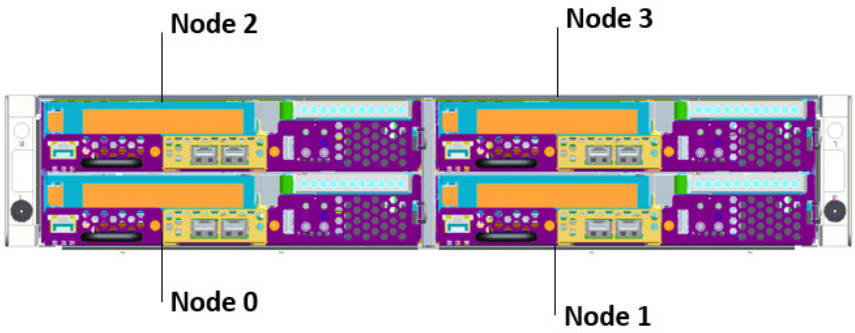


Figure 2 System Front View

The system rear view is shown in Figure 3.

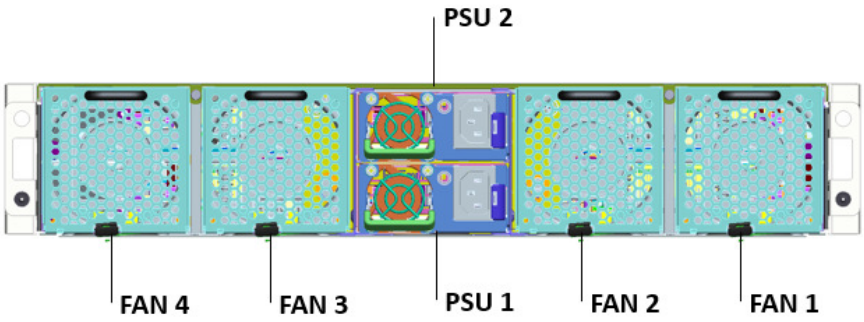


Figure 3 System Rear View

7 System Design Requirements

7.1 Motherboard

The system motherboard leverages "Open_Compute_Project_FB_Server_Intel_Motherboard_v3.1" spec and MB is fit into a server sled. 4 server sleds are combined into a 2U chassis of EIA 19" rack mount design. Following BOM stuff option change are populated or non-populated comparing with the OCP MB.

1. Stuff AST2400 instead of AST1250 and relative components to support BMC iKVM functions
2. Stuff M.2 SATA SSD module instead of mSATA SSD and relative components
3. Stuff AirMax VS® Power 2x2 FCI connector (P/N FCI/10124648-001LF) instead of pressfit cable (P/N TE/2159562-1) for mating Midplane (Power Backplane Board)
4. Stuff AirMax® Guide 7.2mm R/A (P/N FCI/10045588-101LF)
5. Stuff Intel i210 with relative components and RJ45 connector for gigabit LOM
6. Stuff MiniSAS connectors (can be optionally nonpopulated in 2U4N system)

7.2 PCIe Riser Card

PCIe riser card needs modifications to accommodate following requirements:

PCIe riser card of each server node in 2U4N system should be modified to support 1x PCIe full-height, half-length card in 1U height. The slot should use x16 PCIe connector with x16 PCIe signal.

7.3 Server Sled

Server sled contains MB, HDD(s), PCIe riser card(s), and motherboard tray as shown in Figure 5 and Figure 5. The sled is connected to and powered from the Midplane (also called power backplane board, detail is in section 7.5) and can be hot-swappable from the front cold aisle side of the system. The server sled of 2U4N is 1U height, 217mm wide and 520mm deep. An air baffle is designed in 2U4N Sled to

eliminate the air-bypass of each node to guide more airflow into CPU heatsinks. Up to 4x server sleds can be installed in the chassis.

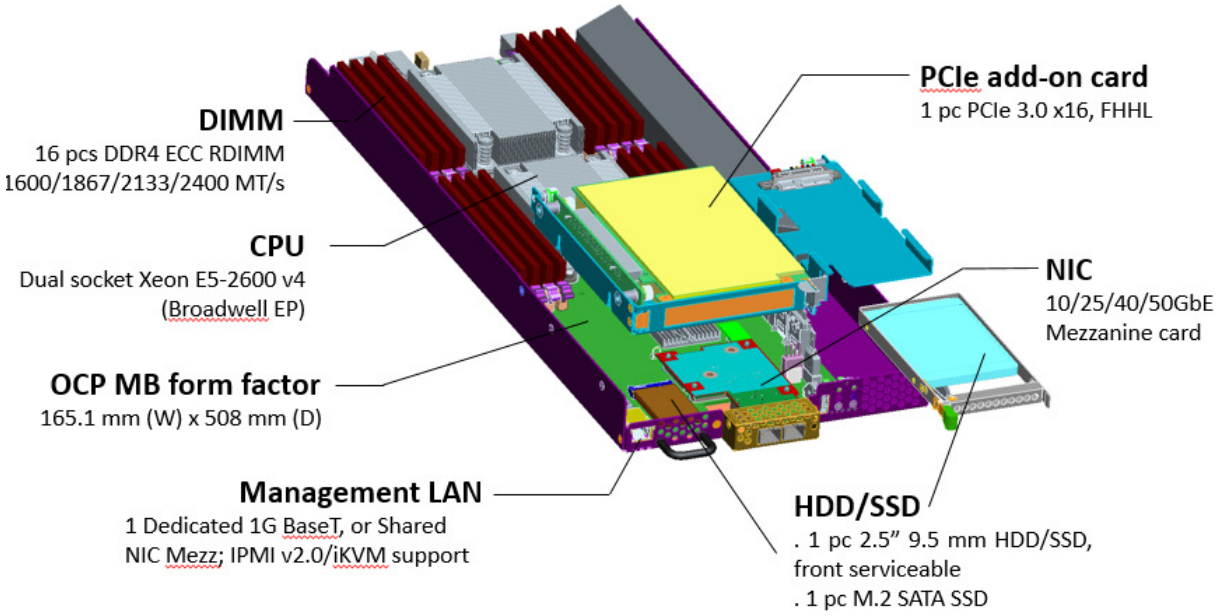


Figure 4 Server Sled

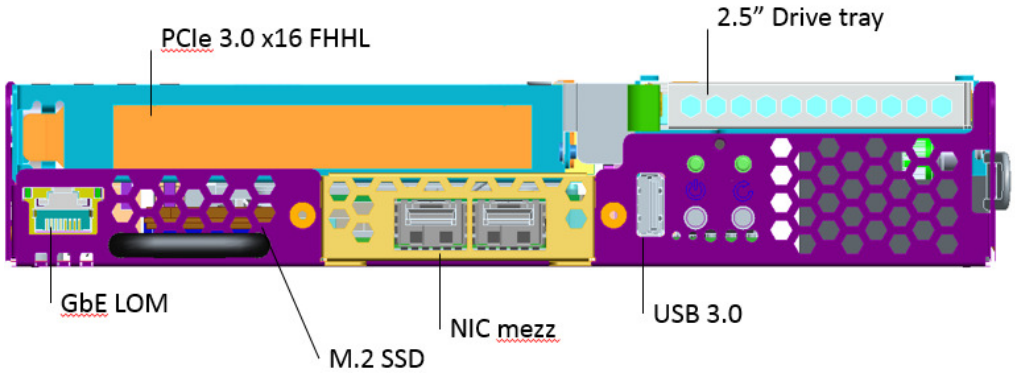


Figure 5 Server Sled Front View

7.4 HDD/SSD Support

The drives carrier of mechanical design in the system should support front service requirement.

Each server node holds 1x 2.5" 9.5mm height HDD/SSD as shown in Figure 6. The drive bracket is right beneath the PCIe add-on card. A power/SATA connector is fixed on it and connected to the 7-pin SATA port and power connector of the MB. The drive tray can be front access and pluggable for easy drive maintenance.

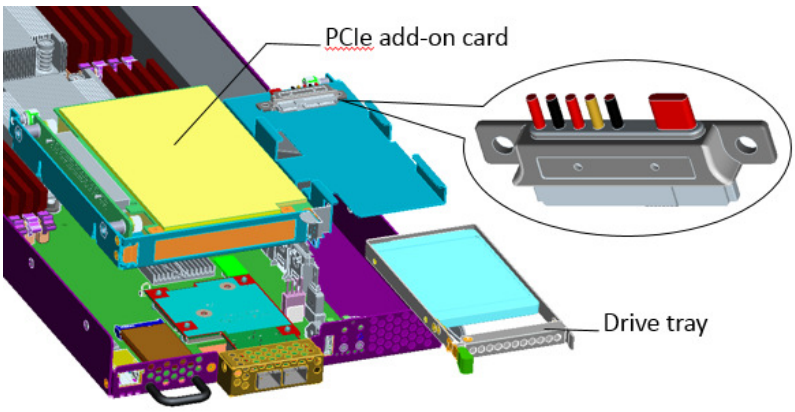
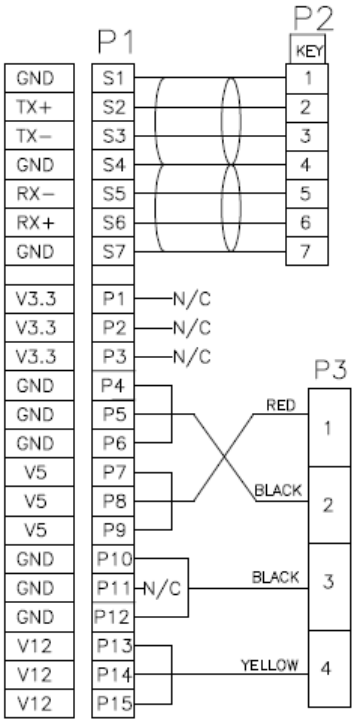


Figure 6 HDD support of 2U4N Sled

Pin definition of the power/SATA connector is shown below:



7.5 Midplane and Power Distribution Board

Midplane (Power Backplane Board, will call it PBB in the document) is a PCB (the size is 430mm x 55mm) which provides connections between sleds, FANs and vertical Power Distribution Board (PDB).

There are two PBBs for lower sleds and upper sleds respectively. PBBs are installed horizontally in the system. The fan speed and PSU signals are handled by the Altera FPGA (EP4CE6E22C8N) located on lower PBB.

Power Distribution Board (PDB, the size is 150mm x 80mm) is a vertical PCB that connects PSUs and PBBs. It provides the path for DC power to server sleds and the signal bridge between upper and lower PBBs. Two vertical type connectors (P/N FCI/10128101-102LF, CN4 is for upper PBB; CN6 is for lower PBB) are used on PDB which provide connection for PBB sideband signals. When installing the PBBs and PDB, the male connector (MIDCN2, AirMax 3x8 FCI/10124755-111LF) on PBBs mate with female connectors on PDB and route the upper sleds' fan control signals to the FPGA on lower PBB. The design concept is shown as Figure 7. Fan control by FPGA on lower PBB is detailed in Section 7.8

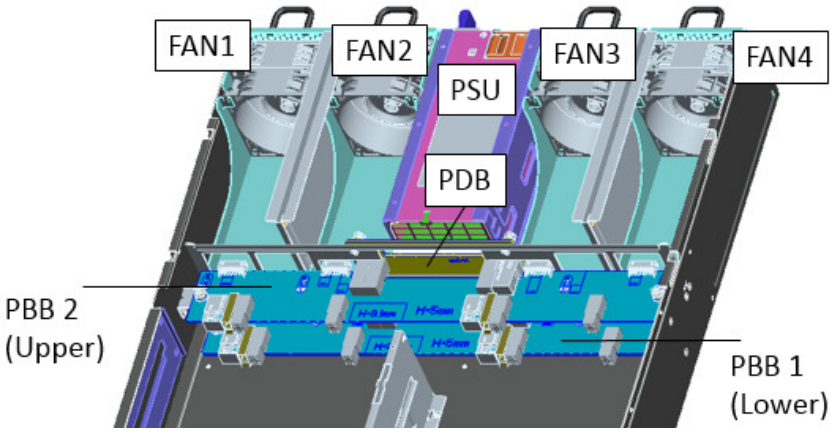


Figure 7 Midplane and Power Distribution Board

Board to Board connectors with associating name label of PDB and PBB are figured in Figure 8. Figure 8 also illustrates connector and names for PBB and mother board connections.

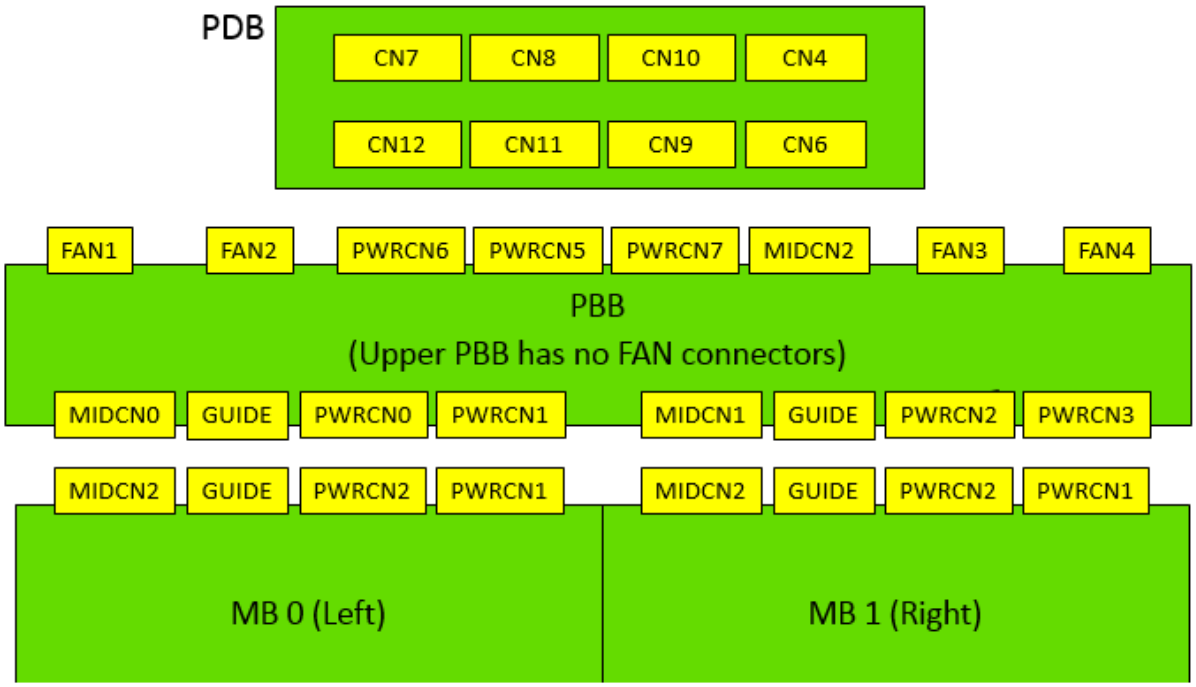


Figure 8 Board to Board Connections

The pin definition of signal connectors MIDCN2 on the upper PBB and upper connector CN4 on the PDB is listed in Table 2. Connectors and its Vendor P/N are shown in Figure 9.

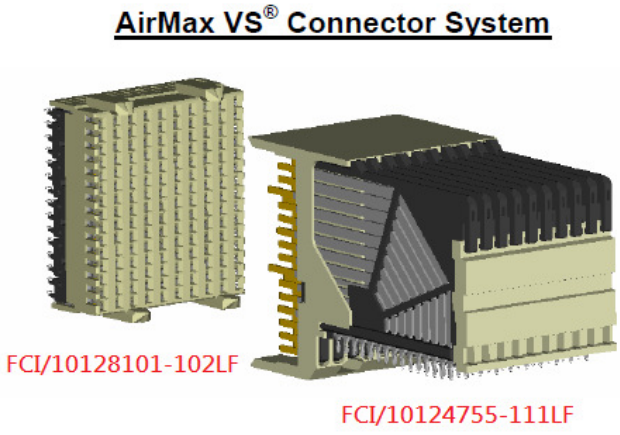


Figure 9 Signal Connectors of PBB, PDB

Table 2. Signal Connector Pin Definition of Upper PBB, PDB

MIDCN2 on the upper PBB FCI/10124755-111LF	
Pin	Net Name
A1	P12V_SB
A2	GND
A3	PSU1_PWROK
A4	PSU1_PSON#
A5	PSU1_ALERT#
A6	PSU0_ALERT#
A7	PSU_SDA
A8	P3V3_SB
B1	P12V_SB
B2	GND
B3	PSU0_PSON#
B4	PSU1_VIN_GOOD#
B5	PSU1_PRESENT#
B6	PSU1_PSKILL
B7	GND
B8	P3V3_SB
C1	P12V_SB
C2	GND
C3	PSU0_VIN_GOOD#
C4	PSU0_PRESENT#
C5	PSU0_PSKILL
C6	PSU0_PWROK
C7	PSU_SCL
C8	P3V3_SB
D1	P12V_SB
D2	MB3_PRESENT#
D3	MB2_PRESENT#
D4	PBB_TOP_PRESENT_N
D5	MB3_CPLD_PS_EN_N

CN4 on the PDB P/N FCI/10128101-102LF	
Pin	Net Name
A1	P12V_SB
A2	GND
A3	NC
A4	NC
A5	NC
A6	NC
A7	NC
A8	P3V3_SB
B1	P12V_SB
B2	GND
B3	NC
B4	NC
B5	NC
B6	NC
B7	GND
B8	P3V3_SB
C1	P12V_SB
C2	GND
C3	NC
C4	NC
C5	NC
C6	NC
C7	NC
C8	P3V3_SB
D1	P12V_SB
D2	MB3_PRESENT#
D3	MB2_PRESENT#
D4	PBB_TOP_PRESENT_N
D5	MB3_CPLD_PS_EN_N

D6	MB2_CPLD_PS_EN_N
D7	GND
D8	P3V3_SB
E1	P12V_SB
E2	MB3_MATED_IN#
E3	MB2_MATED_IN#
E4	MB2_FAN2A_TACH
E5	MB2_FAN2_TACH
E6	MB2_FAN1A_TACH
E7	MB2_FAN1_TACH
E8	GND
F1	P12V_SB
F2	GND
F3	MB3_FAN2A_TACH
F4	GND
F5	MB3_FAN1A_TACH
F6	GND
F7	MB3_FAN1_TACH
F8	NC
G1	P12V_SB
G2	GND
G3	NC
G4	MB3_FAN2_TACH
G5	GND
G6	MB2_FAN_PWM
G7	GND
G8	MB3_FAN_PWM
H1	P12V_SB
H2	P12V_SB
H3	GND
H4	NC
H5	GND

D6	MB2_CPLD_PS_EN_N
D7	GND
D8	P3V3_SB
E1	P12V_SB
E2	MB3_MATED_IN#
E3	MB2_MATED_IN#
E4	MB2_FAN2A_TACH
E5	MB2_FAN2_TACH
E6	MB2_FAN1A_TACH
E7	MB2_FAN1_TACH
E8	GND
F1	P12V_SB
F2	GND
F3	MB3_FAN2A_TACH
F4	GND
F5	MB3_FAN1A_TACH
F6	GND
F7	MB3_FAN1_TACH
F8	NC
G1	P12V_SB
G2	GND
G3	NC
G4	MB3_FAN2_TACH
G5	GND
G6	MB2_FAN_PWM
G7	GND
G8	MB3_FAN_PWM
H1	P12V_SB
H2	P12V_SB
H3	GND
H4	NC
H5	GND

H6	GND
H7	NC
H8	GND
I1	P12V_SB
I2	P12V_SB
I3	MB2_SMB_ALT_N
I4	MB2_SDATA_BUF
I5	MB2_SCLK_BUF
I6	MB3_SMB_ALT_N
I7	MB3_SDATA_BUF
I8	MB3_SCLK_BUF
J2	GND
J4	GND
J6	GND
J8	GND

H6	GND
H7	NC
H8	GND
I1	P12V_SB
I2	P12V_SB
I3	MB2_SMB_ALT_N
I4	MB2_SDATA_BUF
I5	MB2_SCLK_BUF
I6	MB3_SMB_ALT_N
I7	MB3_SDATA_BUF
I8	MB3_SCLK_BUF

The Pin definition of signal connectors MIDCN2 on the lower PBB and lower connector CN6 on PDB is listed as Table 3.

Table 3. Signal Connector Pin Definition of Lower PBB, PDB

MIDCN2 on the lower PBB FCI/10124755-111LF	
Pin	Net Name
A1	P12V_SB
A2	GND
A3	PSU1_PWROK
A4	PSU1_PSON#
A5	PSU1_ALERT#
A6	PSU0_ALERT#
A7	PSU_SDA
A8	P3V3_SB
B1	P12V_SB

CN6 on the PDB P/N FCI/10128101-102LF	
Pin	Net Name
A1	P12V_SB
A2	GND
A3	PSU1_PWROK
A4	PSU1_PSON#
A5	PSU1_ALERT#
A6	PSU0_ALERT#
A7	PSU_SDA
A8	P3V3_SB
B1	P12V_SB

B2	GND
B3	PSU0_PSON#
B4	PSU1_VIN_GOOD#
B5	PSU1_PRESENT#
B6	PSU1_PSKILL
B7	GND
B8	P3V3_SB
C1	P12V_SB
C2	GND
C3	PSU0_VIN_GOOD#
C4	PSU0_PRESENT#
C5	PSU0_PSKILL
C6	PSU0_PWROK
C7	PSU_SCL
C8	P3V3_SB
D1	P12V_SB
D2	MB3_PRESENT#
D3	MB2_PRESENT#
D4	PBB_TOP_PRESENT_N
D5	MB3_CPLD_PS_EN_N
D6	MB2_CPLD_PS_EN_N
D7	GND
D8	P3V3_SB
E1	P12V_SB
E2	MB3_MATED_IN#
E3	MB2_MATED_IN#
E4	MB2_FAN2A_TACH
E5	MB2_FAN2_TACH
E6	MB2_FAN1A_TACH
E7	MB2_FAN1_TACH
E8	GND
F1	P12V_SB

B2	GND
B3	PSU0_PSON#
B4	PSU1_VIN_GOOD#
B5	PSU1_PRESENT#
B6	PSU1_PSKILL
B7	GND
B8	P3V3_SB
C1	P12V_SB
C2	GND
C3	PSU0_VIN_GOOD#
C4	PSU0_PRESENT#
C5	PSU0_PSKILL
C6	PSU0_PWROK
C7	PSU_SCL
C8	P3V3_SB
D1	P12V_SB
D2	MB3_PRESENT#
D3	MB2_PRESENT#
D4	PBB_TOP_PRESENT_N
D5	MB3_CPLD_PS_EN_N
D6	MB2_CPLD_PS_EN_N
D7	GND
D8	P3V3_SB
E1	P12V_SB
E2	MB3_MATED_IN#
E3	MB2_MATED_IN#
E4	MB2_FAN2A_TACH
E5	MB2_FAN2_TACH
E6	MB2_FAN1A_TACH
E7	MB2_FAN1_TACH
E8	GND
F1	P12V_SB

F2	GND
F3	MB3_FAN2A_TACH
F4	GND
F5	MB3_FAN1A_TACH
F6	GND
F7	MB3_FAN1_TACH
F8	NC
G1	P12V_SB
G2	GND
G3	NC
G4	MB3_FAN2_TACH
G5	GND
G6	MB2_FAN_PWM
G7	GND
G8	MB3_FAN_PWM
H1	P12V_SB
H2	P12V_SB
H3	GND
H4	NC
H5	GND
H6	GND
H7	NC
H8	GND
I1	P12V_SB
I2	P12V_SB
I3	MB2_SMB_ALT_N
I4	MB2_SDATA_BUF
I5	MB2_SCLK_BUF
I6	MB3_SMB_ALT_N
I7	MB3_SDATA_BUF
I8	MB3_SCLK_BUF
J2	GND
J4	GND

F2	GND
F3	MB3_FAN2A_TACH
F4	GND
F5	MB3_FAN1A_TACH
F6	GND
F7	MB3_FAN1_TACH
F8	NC
G1	P12V_SB
G2	GND
G3	NC
G4	MB3_FAN2_TACH
G5	GND
G6	MB2_FAN_PWM
G7	GND
G8	MB3_FAN_PWM
H1	P12V_SB
H2	P12V_SB
H3	GND
H4	NC
H5	GND
H6	GND
H7	NC
H8	GND
I1	P12V_SB
I2	P12V_SB
I3	MB2_SMB_ALT_N
I4	MB2_SDATA_BUF
I5	MB2_SCLK_BUF
I6	MB3_SMB_ALT_N
I7	MB3_SDATA_BUF
I8	MB3_SCLK_BUF
J2	
J4	

J6	GND
J8	GND

J6	
J8	

7.5.1 DC Input Connection

DC power input connection on PDB is a vertical type connector (P/N FCI/10028916-5555P00LF) which can mate with the FCI/10124648-001LF on PBBs and provide power to sleds through PBBs.

There are four vertical-type power connectors (FCI/10028916-5555P00LF) installed on PDB (two for upper PBB and the other two for lower one) and each of the connector can deliver up to 20A of power, total 40A for one PBB. (There are two more connectors reserved for larger power demands). Each power connector mates with one FCI/10124648-001LF on the PBB. Power Connectors and vendor's P/N of PDB, PBB is shown in Figure 10.

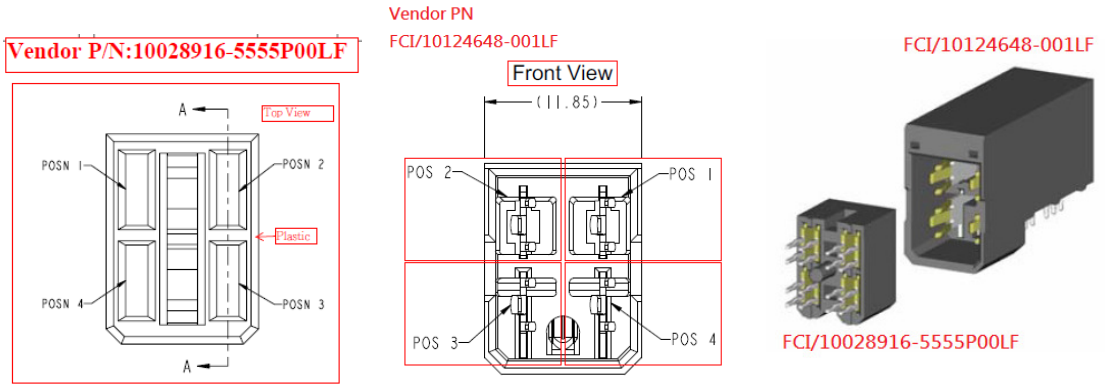


Figure 10 Power Connector of PDB, PBB

Pin definition of power connectors CN7~CN12 on PDB and PWRCN5~PWRCN7 on both upper and lower PBBs are as Table 4. Connector vendor's P/N is shown too.

Table 4. Power Connector Pin Definition of PBB, PDB

CN7~CN12 on the PDB FCI/10028916-5555P00LF	
POSN	Net Name
1	P12V

PWRCN5~PWRCN7 on the PBB FCI/10124648-001LF	
POSN	Net Name
1	P12V

2	P12V
3	GND
4	GND

2	P12V
3	GND
4	GND

On the other side of PDB, two 64-pin FCI/10046971-001LF connectors (CN1 & CN2) are used for two PSUs connection as Figure 11.

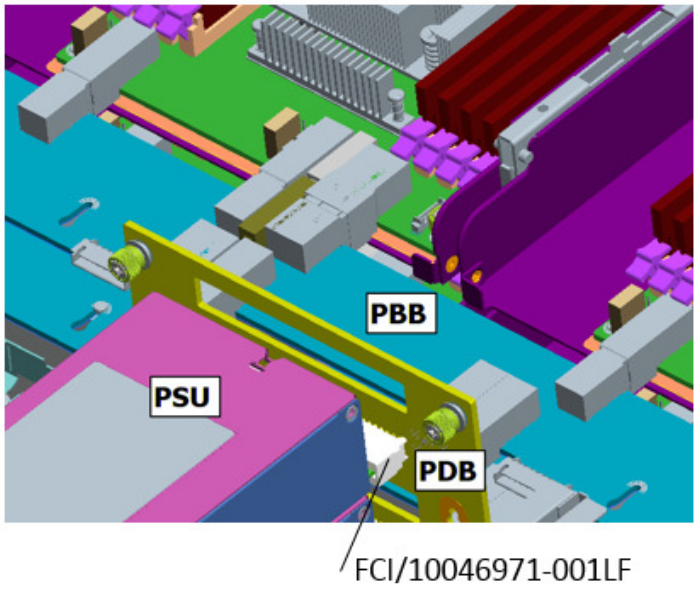


Figure 11 PSU connection with PDB

Pin definition and connector P/N of CN1 (upper) & CN2 (lower) on the PDB for PSU connectors are as Table 5.

Table 5. PSU Connectors of PDB

CN1 on PDB FCI/10046971-001LF	
Pin	Net Name
1	P12V
2	P12V
3	P12V
4	P12V
5	P12V

CN2 on PDB FCI/10046971-001LF	
Pin	Net Name
1	P12V
2	P12V
3	P12V
4	P12V
5	P12V

6	P12V
7	P12V
8	P12V
9	P12V
10	P12V
11	P12V
12	P12V
13	GND
14	GND
15	GND
16	GND
17	GND
18	GND
19	GND
20	GND
21	GND
22	GND
23	GND
24	GND
25	NC
26	PSU1_SENSE-
27	PSU1_VIN_GOOD#
28	PSU1_C_SHARE#
29	PSU1_PSON#
30	PSU1_PSKILL
31	NC
32	PSU1_ALERT#
33	PSU_SDA
34	PSU1_PRESENT#
35	PSU_SCL
36	GND
37	PSU1_PWROK

6	P12V
7	P12V
8	P12V
9	P12V
10	P12V
11	P12V
12	P12V
13	GND
14	GND
15	GND
16	GND
17	GND
18	GND
19	GND
20	GND
21	GND
22	GND
23	GND
24	GND
25	NC
26	PSU0_SENSE-
27	PSU0_VIN_GOOD#
28	PSU0_C_SHARE#
29	PSU0_PSON#
30	PSU0_PSKILL
31	NC
32	PSU0_ALERT#
33	PSU_SDA
34	PSU0_PRESENT#
35	PSU_SCL
36	GND
37	PSU0_PWROK

38	PSU1_ADD0
39	P12V_SB
40	PSU1_SENSE+
41	GND
42	GND
43	GND
44	GND
45	GND
46	GND
47	GND
48	GND
49	GND
50	GND
51	GND
52	GND
53	P12V
54	P12V
55	P12V
56	P12V
57	P12V
58	P12V
59	P12V
60	P12V
61	P12V
62	P12V
63	P12V
64	P12V

38	PSU0_ADD0
39	P12V_SB
40	PSU0_SENSE+
41	GND
42	GND
43	GND
44	GND
45	GND
46	GND
47	GND
48	GND
49	GND
50	GND
51	GND
52	GND
53	P12V
54	P12V
55	P12V
56	P12V
57	P12V
58	P12V
59	P12V
60	P12V
61	P12V
62	P12V
63	P12V
64	P12V

7.5.2 Motherboard Connectors

Each PBB (upper or lower) has following connectors to connect with mother boards.

1. Four FCI/10124620-5545P00LF female right-angle power connectors, which mates with mother board's FCI/10124648-001LF male right angle connector. Two (1

reserved) of the connectors are for Mother Board 0 (left) connection, and the other two for Mother Board 1 (right).

2. Two FCI/10124756-101LF connectors to mate with FCI/10124755-111LF on MBs (left and right) for the signal handling.
3. Two FCI/10045367-101LF connectors to mate AirMax guide FCI/10045588-101LF on MB. One is for Mother Board 0, and the other one for Mother Board 1.

Pin definition of power connectors PWRCN0~PWRCN3 on the PBB and PWRCN1~PWRCN2 on each MB are as Table 6. The connector and vendor's P/N are shown as Figure 12.

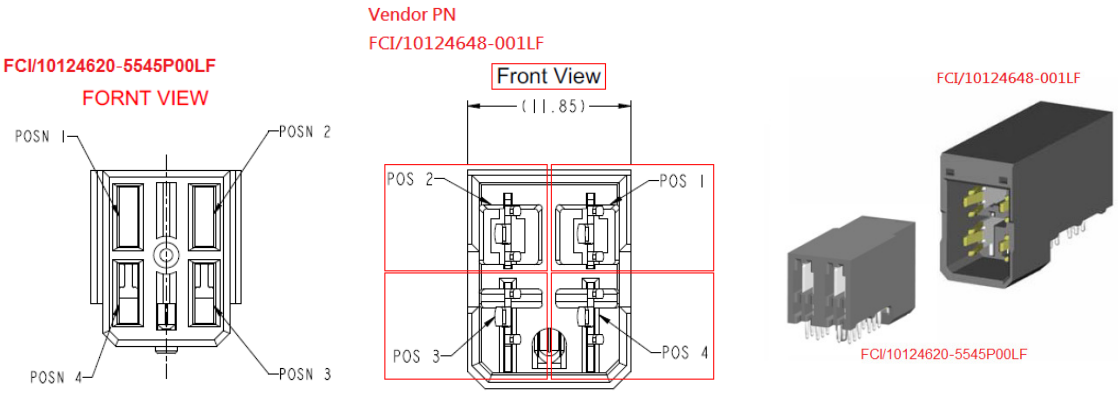


Figure 12 Power Connectors of PBB, MB

Table 6. Power Connector Pin Definition of PDB, MB

PWRCN0~PWRCN3 on the PBB FCI/10124620-5545P00LF	
POSN	Net Name
1	P12V
2	P12V
3	GND
4	GND

PWRCN1~PWRCN2 on the MB FCI/10124648-001LF	
POSN	Net Name
1	P12V
2	P12V
3	GND
4	GND

The Pin definition of signal connector MIDCN0, MIDCN1 on the PBB and MIDCN2 on the MB are as Table 7 and

Table 8. Connector and vendor's P/N is shown in Figure 13.

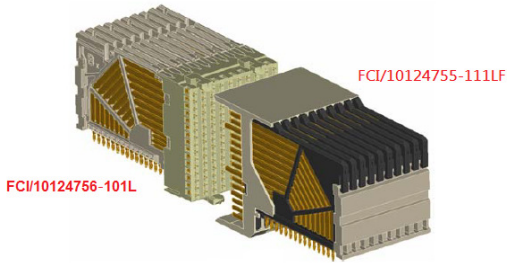


Figure 13 Signal Connectors of PBB, MB

Table 7. Signal Connector Pin Definition of PBB, MB (Left)

MIDCN0 on the PBB FCI/10124756-101LF	
Pin	Net Name
A1	NC
A2	GND
A3	NC
A4	MB0_FAN2A_TACH
A5	NC
A6	MB0_SMB_ALT_N
A7	NC
A8	GND
B1	NC
B2	NC
B3	NC
B4	MB0_FAN2_TACH
B5	NC
B6	MB0_SDATA
B7	NC
B8	NC
C1	GND
C2	NC

MIDCN2 on the MB FCI/10124755-111LF	
Pin	Net Name
A1	NC
A2	GND
A3	NC
A4	FAN1_TACH1A
A5	NC
A6	IRQ_MID_PMBUS_ALERT_N
A7	NC
A8	GND
B1	NC
B2	NC
B3	NC
B4	FAN1_TACH
B5	NC
B6	SMB_PMBUS_DATA
B7	NC
B8	NC
C1	GND
C2	NC

C3	GND
C4	MB0_FAN1A_TACH
C5	GND
C6	MB0_SCLK
C7	GND
C8	NC
D1	NC
D2	GND
D3	NC
D4	MB0_FAN1_TACH
D5	NC
D6	GND
D7	NC
D8	GND
E1	NC
E2	NC
E3	NC
E4	MB0_MATED_IN_N
E5	NC
E6	NC
E7	NC
E8	NC
F1	GND
F2	NC
F3	GND
F4	LP_MB0_FAN0_PWM
F5	MB0_SLOT_ID0
F6	NC
F7	GND
F8	NC
G1	NC
G2	GND

C3	GND
C4	FAN0_TACH0A
C5	GND
C6	SMB_PMBUS_CLK
C7	GND
C8	NC
D1	NC
D2	GND
D3	NC
D4	FAN0_TACH
D5	NC
D6	GND
D7	NC
D8	GND
E1	NC
E2	NC
E3	NC
E4	MATED_IN_N
E5	NC
E6	NC
E7	NC
E8	NC
F1	GND
F2	NC
F3	GND
F4	FAN0_PWM
F5	MB_SLOT_ID0
F6	NC
F7	GND
F8	NC
G1	NC
G2	GND

G3	NC
G4	MB_PRESENT1#
G5	MB0_SLOT_ID1
G6	GND
G7	NC
G8	GND
H1	NC
H2	NC
H3	NC
H4	NC
H5	MB0_SLOT_ID2
H6	NC
H7	NC
H8	NC
I1	GND
I2	NC
I3	MB0_ON_N
I4	NC
I5	NC
I6	NC
I7	GND
I8	NC
J2	GND
J4	GND
J6	GND
J8	GND

G3	NC
G4	GND
G5	MB_SLOT_ID1
G6	GND
G7	NC
G8	GND
H1	NC
H2	NC
H3	NC
H4	NC
H5	MB_SLOT_ID2
H6	NC
H7	NC
H8	NC
I1	GND
I2	NC
I3	MB_ON_N
I4	NC
I5	NC
I6	NC
I7	GND
I8	NC
J2	GND
J4	GND
J6	GND
J8	GND

Table 8. Signal Connector Pin Definition of PBB, MB (Right)

MIDCN1 on the PBB FCI/10124755-111LF	
Pin	Net Name
A1	NC

MIDCN2 on the MB FCI/10124755-111LF	
Pin	Net Name
A1	NC

A2	GND
A3	NC
A4	MB1_FAN2A_TACH
A5	NC
A6	MB1_SMB_ALT_N
A7	NC
A8	GND
B1	NC
B2	NC
B3	NC
B4	MB1_FAN2_TACH
B5	NC
B6	MB1_SDATA
B7	NC
B8	NC
C1	GND
C2	NC
C3	GND
C4	MB1_FAN1A_TACH
C5	GND
C6	MB1_SCLK
C7	GND
C8	NC
D1	NC
D2	GND
D3	NC
D4	MB1_FAN1_TACH
D5	NC
D6	GND
D7	NC
D8	GND
E1	NC

A2	GND
A3	NC
A4	FAN1_TACH1A
A5	NC
A6	IRQ_MID_PMBUS_ALERT_N
A7	NC
A8	GND
B1	NC
B2	NC
B3	NC
B4	FAN1_TACH
B5	NC
B6	SMB_PMBUS_DATA
B7	NC
B8	NC
C1	GND
C2	NC
C3	GND
C4	FAN0_TACH0A
C5	GND
C6	SMB_PMBUS_CLK
C7	GND
C8	NC
D1	NC
D2	GND
D3	NC
D4	FAN0_TACH
D5	NC
D6	GND
D7	NC
D8	GND
E1	NC

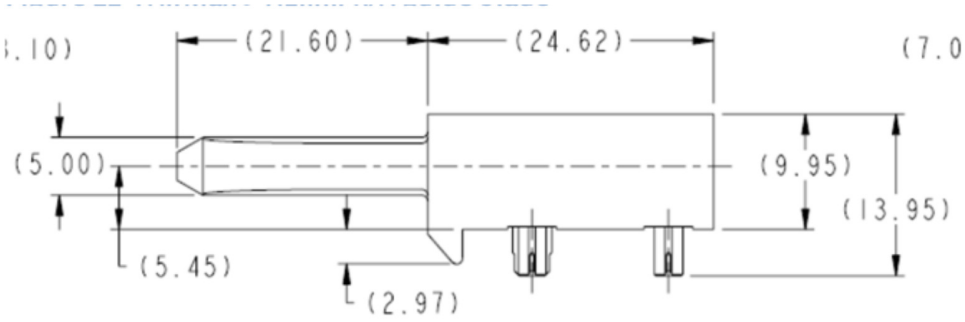
E2	NC
E3	NC
E4	MB1_MATED_IN_N
E5	NC
E6	NC
E7	NC
E8	NC
F1	GND
F2	NC
F3	GND
F4	LP_MB1_FAN0_PWM
F5	MB1_SLOT_ID0
F6	NC
F7	GND
F8	NC
G1	NC
G2	GND
G3	NC
G4	MB_PRESENT2#
G5	MB1_SLOT_ID1
G6	GND
G7	NC
G8	GND
H1	NC
H2	NC
H3	NC
H4	NC
H5	MB1_SLOT_ID2
H6	NC
H7	NC
H8	NC
I1	GND
I2	NC

E2	NC
E3	NC
E4	MATED_IN_N
E5	NC
E6	NC
E7	NC
E8	NC
F1	GND
F2	NC
F3	GND
F4	FAN0_PWM
F5	MB_SLOT_ID0
F6	NC
F7	GND
F8	NC
G1	NC
G2	GND
G3	NC
G4	GND
G5	MB_SLOT_ID1
G6	GND
G7	NC
G8	GND
H1	NC
H2	NC
H3	NC
H4	NC
H5	MB_SLOT_ID2
H6	NC
H7	NC
H8	NC
I1	GND
I2	NC

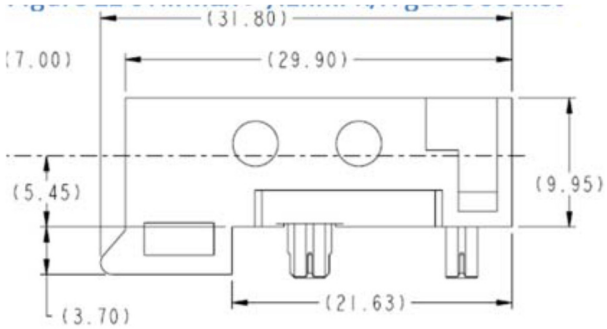
I3	MB1_ON_N
I4	NC
I5	NC
I6	NC
I7	GND
I8	NC
J2	GND
J4	GND
J6	GND
J8	GND

I3	MB_ON_N
I4	NC
I5	NC
I6	NC
I7	GND
I8	NC
J2	GND
J4	GND
J6	GND
J8	GND

A pair of AirMax 7.2mm R/A guide are used on the MB of server sled and PBB for blind mate. 1x AirMaxR 7.2mm R/A guide is used at sled side as below:



2x AirMaxR 7.2mm R/A guide socket are used in PBB as below for MB0, MB1:



7.5.3 Hot Swap Controller

Hot swap controller's implementation should follow the Motherboard Design Specification.

7.5.4 FAN connectors

The lower PBB has 4x 8-pin FAN connectors shown as Figure 8. The connector is JWT/A2501WR2-8P (Figure 14) and provides connection to the matting connector JWT/A2501H02-8P or similar of FAN module in the Fan tray. FAN connector signals should follow "4-Wire Pulse Width Modulation (PWM) Controlled Fans Specification" Revision 1.3 September 2005 published by Intel Corporation. The connectors can be used to support dual rotor FAN that shares PWM control signal but has separate TACH signals. The fan power/PWM/Tachometer should be connected at the lower PBB. Upper PBB has no FAN connector. The FAN power should not be turned off when any Node during S0.

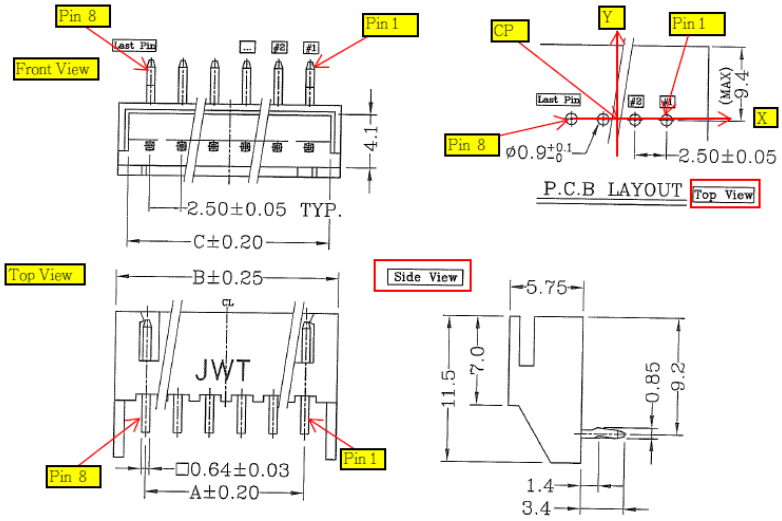


Figure 14 Fan Connector

Pin definition of Fan connectors (FAN1~FAN4) on the lower PBB are as Table 9.

Table 9. FAN Connector Pin Definition

FAN1~FAN4 on the lower PBB JWT/A2501WR2-8P	
Pin	Net Name
1	FAN_TACHx
2	FAN_PWMx

3	FAN_TACHxA
4	GND
5	GND
6	NC
7	+12V
8	+12V

7.6 Chassis

The chassis of 2U4N is a 19" 2U rack mountable design in dimension of 448 mm(W) x 87.6 mm(H) x 800 mm(D) as shown in Figure 15. The chassis can fit for 4 Server sleds, 2 PBBs, 1 PDB, 4 Fan Trays, 2 PSUs and other necessary mechanical designs for easy assemble, tool-less system maintenance as shown in Figure 16. The mechanical parts sustains the components and guide for the component installations.

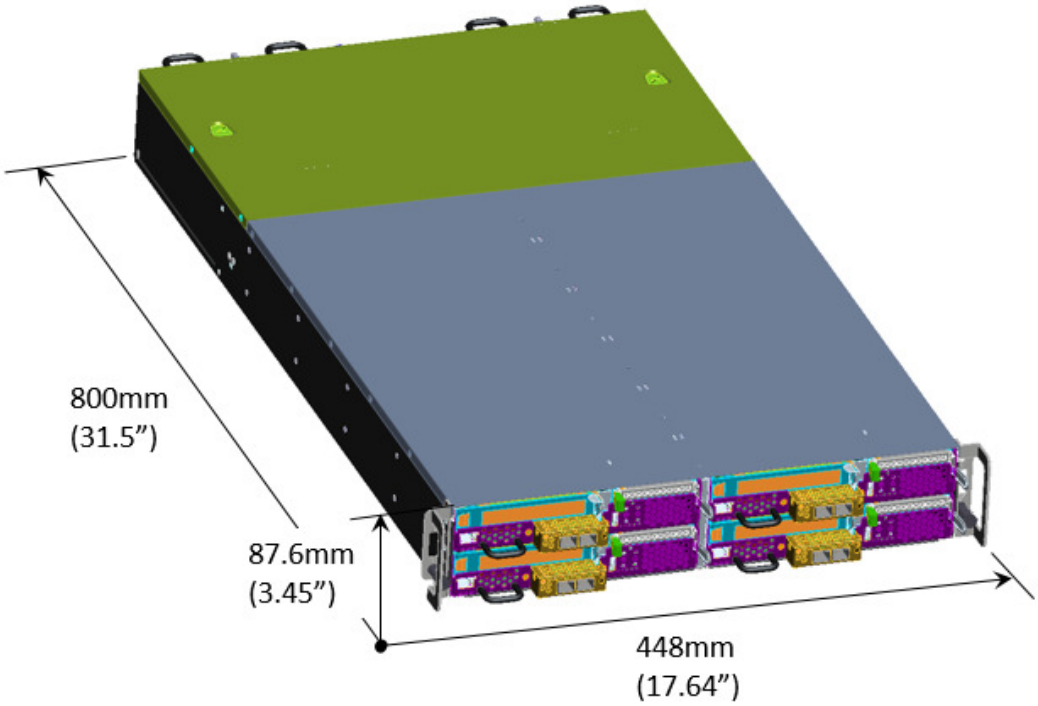


Figure 15 System Chassis

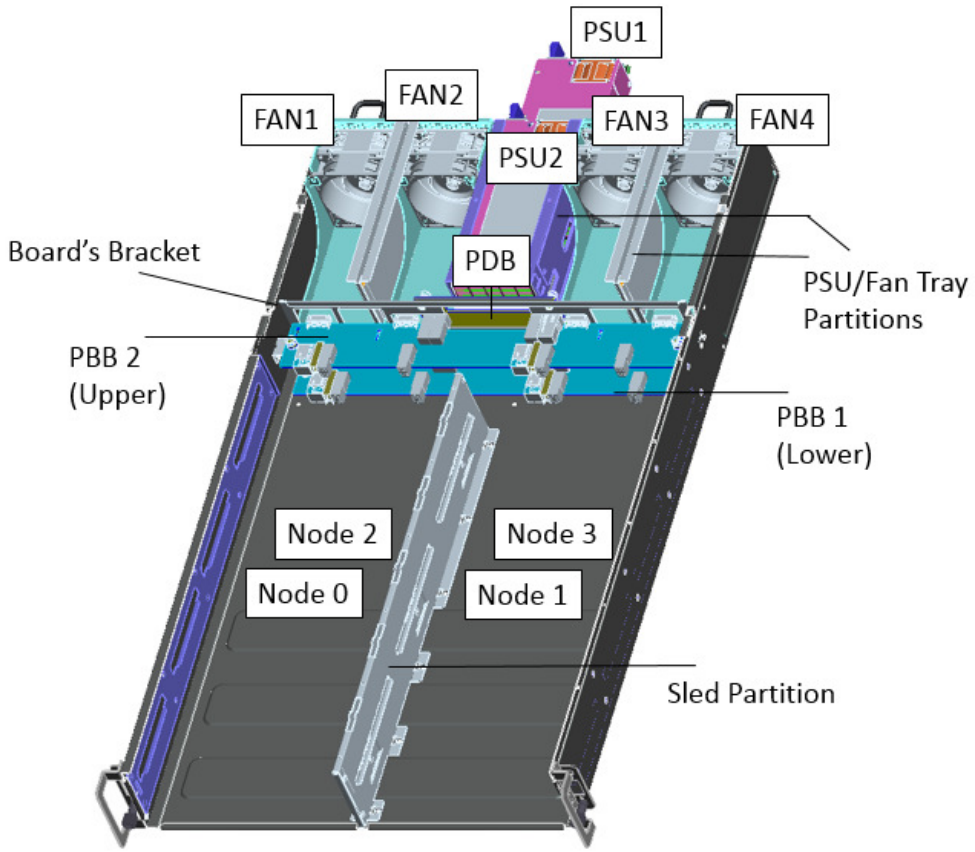


Figure 16 Components in Chassis

The system supports 2U slide rail from supplier King Slide. P/N of slide rail is A861-557.

7.7 Power Supply

2U4N system uses two 1U 1600W 1+1Redundant PSU from Chicony P/N R1K6A016L.

7.8 FAN

Fan should use four 80mm x 56mm dual rotor fans with 3+1 redundant support. Each fan is installed in a fan tray. Fan tray aligns the fan module's connector being connected to the fan connector on the lower PBB. The fan tray is hot pluggable for easy to maintain the fan module as shown in Figure 17.

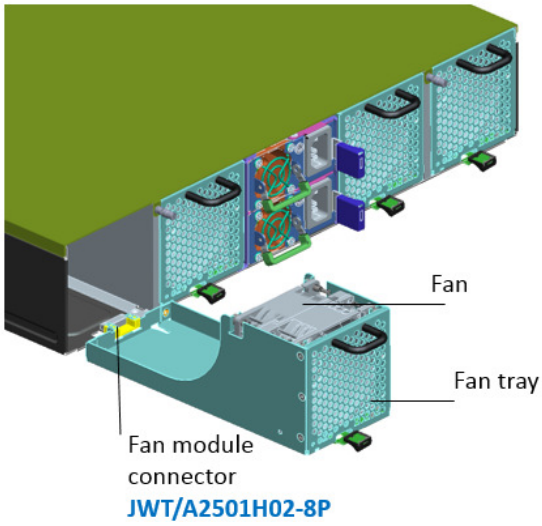


Figure 17 Fan Module Maintenance

7.8.1 CFM

The maximum CFM of 2U4N system is 230CFM with a CPU TDP of 135W when operating at maximum 35°C ambient temperature.

7.8.2 FAN Control

As described in Section 7.5, an Altera FPGA (EP4CE6E22C8N) on the lower PBB is used to control fan signals. Figure 18 and Table 10 illustrates the fan signal control mechanism. All fans are running at the same speed and managed by the maximum PWM of all server nodes.

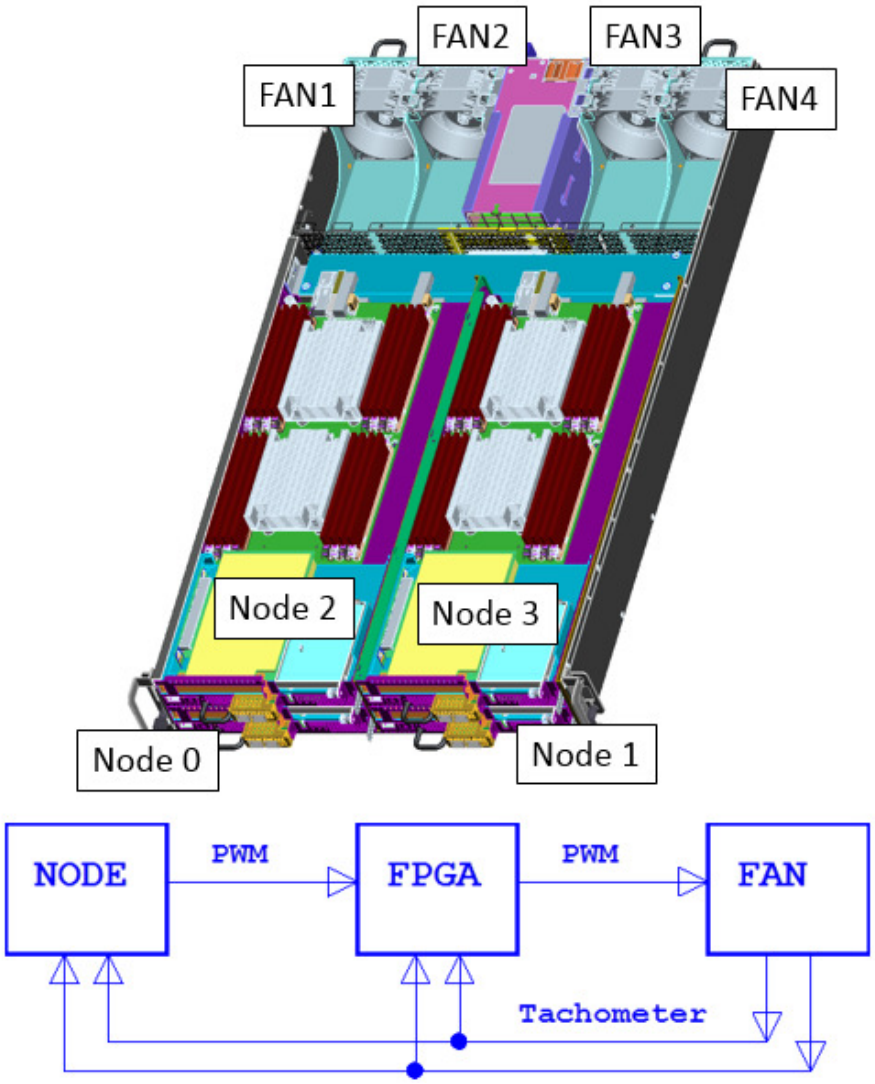


Figure 18 Fan Control Diagram

Table 10. FAN Tachometer Reading

	2U4N
Node Index	FAN Tachometer reading from
Node 0	FAN1/FAN1A/FAN2/FAN2A
Node 1	FAN3/FAN3A/FAN4/FAN4A
Node 2	FAN1/FAN1A/FAN2/FAN2A
Node 3	FAN3/FAN3A/FAN4/FAN4A

7.9 Environmental Requirement

The system needs to fulfill following Environmental requirement

1. Temperature and Humidity
    - Ambient operating temperature range: -5 to +35 degree C, 40 degree within 2 hrs.
    - Operating and Storage relative humidity: 10% to 90% (non-condensing)
    - Storage temperature range: -40 to +70 degree C
    - Transportation temperature range: MIL-STD-810G METHOD 503.5
    - Operating altitude with no de-ratings: 1000m (3300 feet)

2. Vibration & Shock

    The motherboard shall meet shock and vibration requirements according to the following IEC specifications: IEC68-2, 68-2-27 & IEC68-2-6 Standard & Levels. The motherboard shall exhibit fully compliance to the specification without any electrical discontinuities during the operating vibration and shock tests. No physical damage or limitation of functional capabilities (as defined in this specification) shall occur to the motherboard during the non-operational vibration and shock tests.

7.10 Regulations

The system needs to meet following regulations

- UL, CE, FCC, CB
- BSMI, VCCI, CCC (option)

The sled should be compliant with RoHS and WEEE.

7.11 Operating System Compatibility

The System needs to comply with following operating systems.

- RedHat® Enterprise Linux® 7.0
- CentOS 6.5 (64 bits)
- Windows® Server 2012 R2
- VMware ESXi 6.0