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Facebook/Microsoft
M.2 Carrier Card Design Specification

Version 0.3

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Contents

1 Overview

This specification provides the requirements for a PCIe Full Height Half Length (FHHL) form factor card, that supports up to four M.2 form factor solid-state drives (SSDs). The card shall support 110mm (Type 22110) or 80mm (Type 22080) dual sided M.2 modules.

2 Features

2.1 PCIe

The card shall interface to the motherboard through standard PCIe x16 edge card connector. The 16 lanes shall be bifurcated to 4x4 to accommodate the 4 M.2 modules. The card shall be designed to meet the electrical requirements of PCIe Gen3, but can electrically accommodate all generations of PCIe. The lane mapping between the edge connector and the M.2 modules is shown in Figure 1.

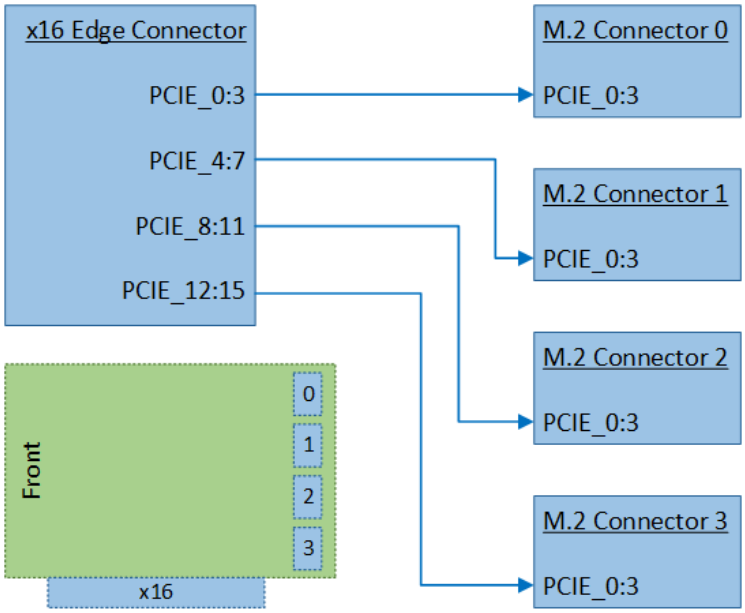


Figure 1. PCIe Lane Mapping

2.1.1 Bifurcation Settings

The card shall support 4x4 bifurcation of the x16 PCIe lanes. To support automated bifurcation detection, the bifurcation information is made available to the motherboard and BIOS using pullup and pulldown resistors on the unused present pin B31. This pin is pulled high on the card to indicate 4x4 bifurcation to the BIOS. Otherwise, bifurcation will need to be set manually in the BIOS. The pinout for the PCIe x16 connector is shown in Section 3.1.

2.2 Reset

The card shall support PERST# from the PCIe card edge connector. The signal shall be buffered and fanned out to the individual M.2 modules as shown in Figure 2**Error! Reference source not found.** The card also supports an option out of band (OOB) reset enabling reset of individual M.2 modules through an I2C IO expander.

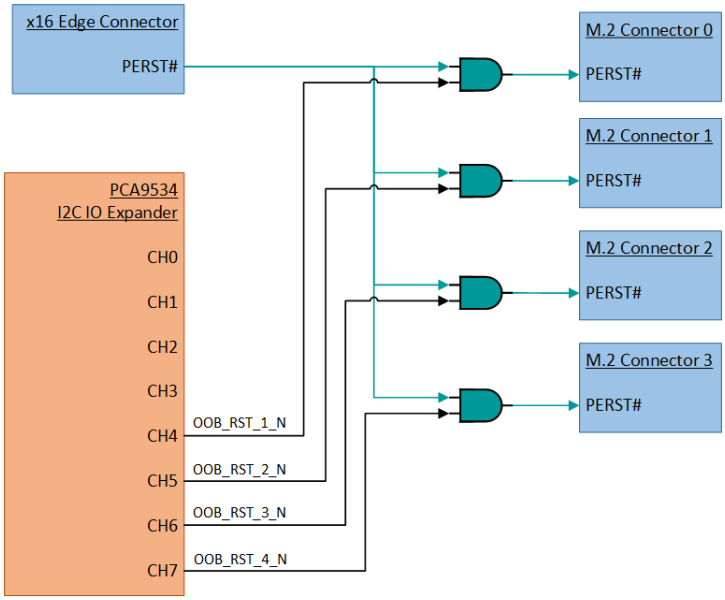


Figure 2. Reset Block Diagram

2.3 REFCLK

The card shall support a single PCIe reference clock (REFCLK) from the PCIe edge card connector. REFCLK shall be buffered and fanned out to the individual M.2 modules using an I2C-configurable clock buffer (9DB433AGLFT or equivalent) as shown in Figure 3.

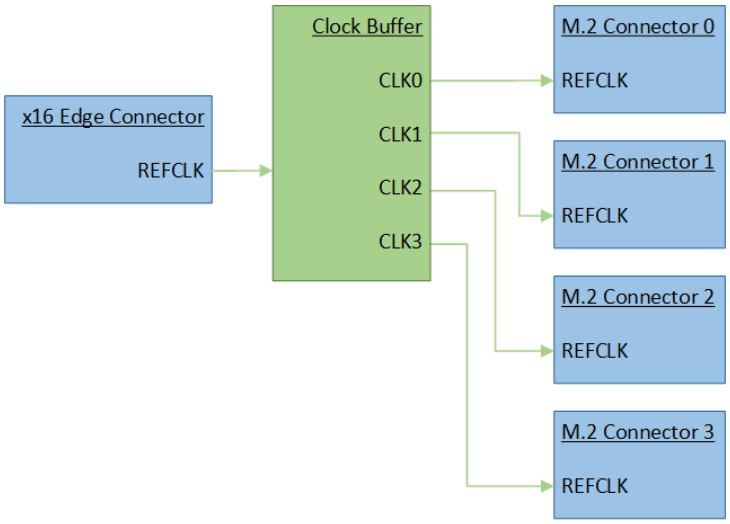


Figure 3. PCIe Clock Block Diagram

2.4 I2C

The card shall support I2C communication with the motherboard BMC through the PCIe card edge connector. The block diagram is shown in Figure 4.

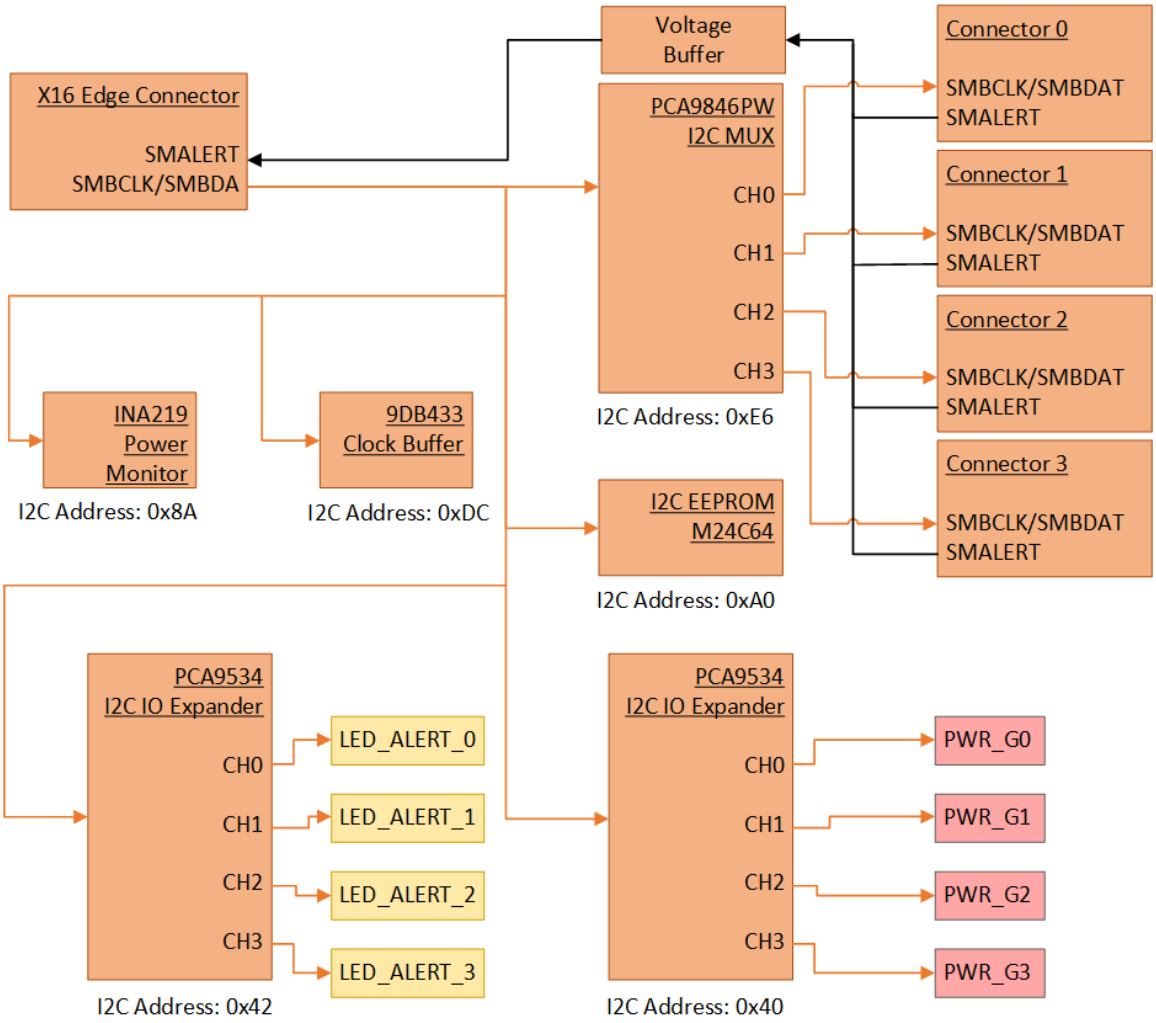


Figure 4. I2C Block Diagram

Pull-ups exist on the host side for SMBCLK, SMBDAT, and SMALERT; however, for the purposes of bring-up, de-populated pull-ups should be provisioned.

The card shall provide the SMBUS connection to the M.2 modules as outlined in the ECN to the PCIe M.2 Specification, titled “SMBus interface for SSD Socket 2 and Socket 3” (August 11, 2014). The M.2 modules shall be connected to the host through an I2C Mux. Note that the logic level required by the M.2 module is 1.8V. Therefore, it is required that the I2C Mux support voltage translation from 3.3V to 1.8V.

For the purposes of bringup, all I2C address lines should have options for both pull-ups and pull-downs.

2.5 EEPROM

The card shall support a 64Kb EEPROM (FRUID) for storage of manufacturing data. The EEPROM shall be available to the motherboard using the I2C bus.

2.6 LEDs

The card shall support LEDs for communicating state and failure information. Bicolor (red/blue) LEDs should be placed towards the front of the mechanical bracket and should be visible through the front bulkhead. The LED number should be clearly visible on the bracket, along with the silkscreen of its corresponding connector on the PCB. The LED to connector mapping is shown below for both orientations. Silkscreen should be placed on both top and bottom sides of the PCB to clearly indicate LED and connector positions. A block diagram of the LED circuitry is shown in Figure 5.

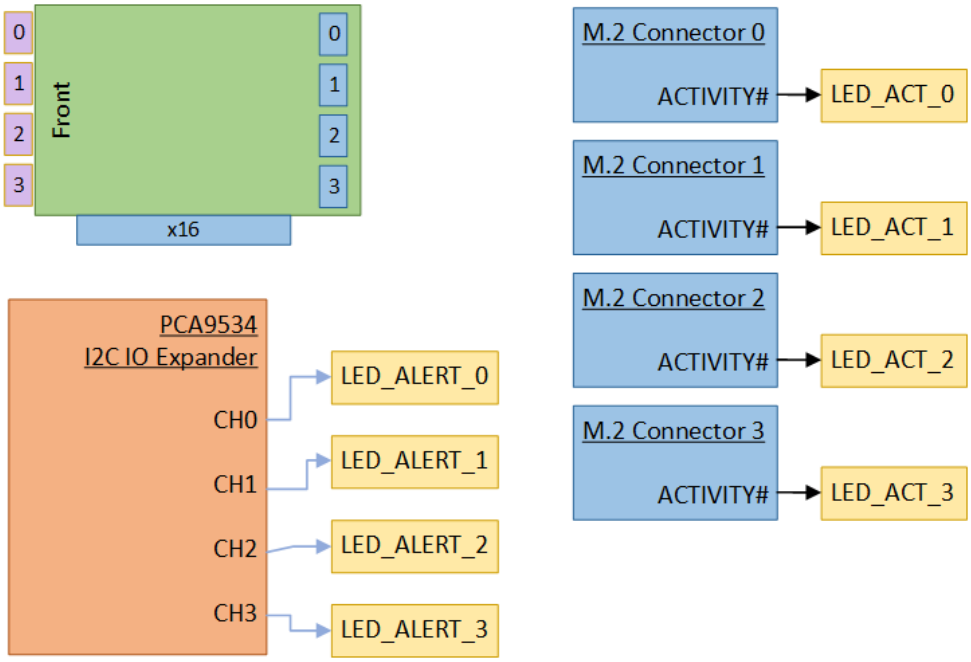


Figure 5. LED Block Diagram

The blue LEDs are to indicate M.2 activity, and should be driven by the LED signal (Pin 10) of the M.2 modules. The LED should be on when the SSD is installed and idle, and flashing when there is activity.

The red LEDs are to indicate module fault, and should be driven by the I2C-addressable GPIO expander.

2.7 Power

The card shall support 12V, 3.3V, and 3.3V Aux power through the PCIe edge connector. A block diagram of the power tree is shown in Figure 6.

12V shall be supplied to the card through a hot swap controller. This is required to limit the in-rush current and to isolate the rest of the system from any power fault on the card. Power to the M.2 modules shall be generated from a 3.3V switching converter that is supplied by the 12V output of the hot swap controller. The converter shall be scaled to support 8.5W per M.2 module up to 14.85W per M.2 module.

Optionally, the card shall support FETs to enable the system to control power to individual M.2 modules. This enables the system to clear errors by cycling power to specific modules. The card shall contain the necessary design components to bypass this feature if it is not required by the system.

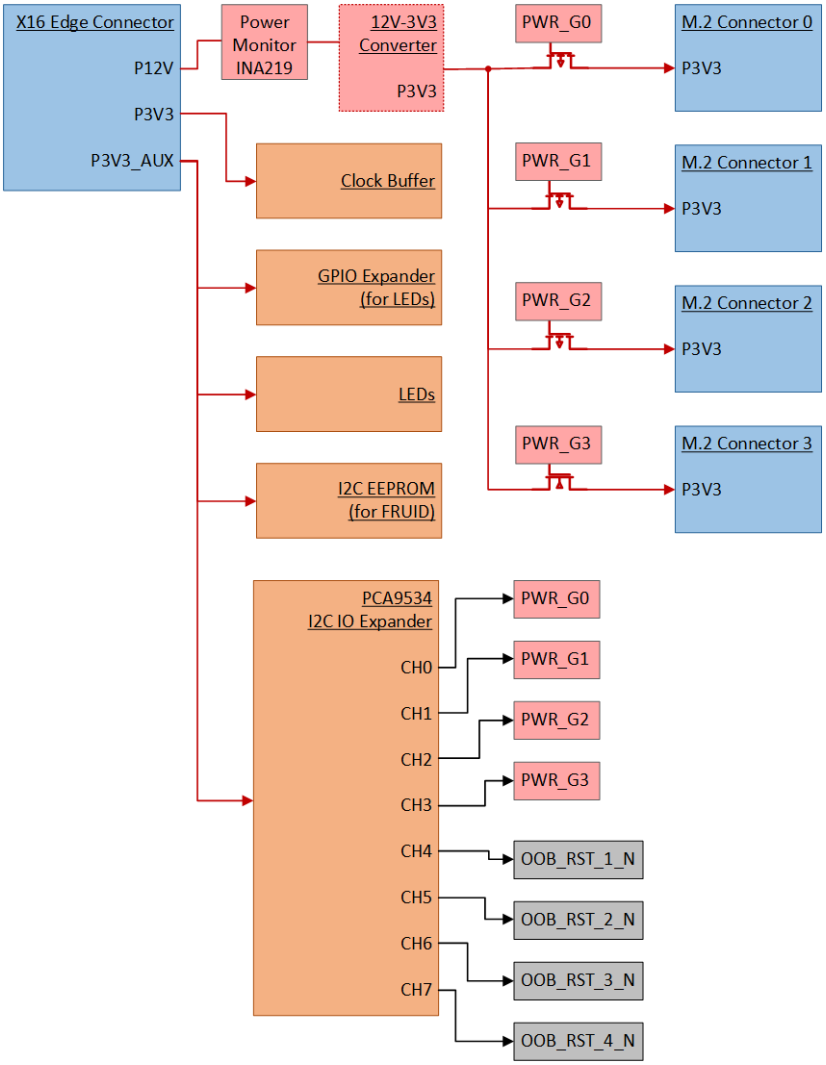


Figure 6. Power Bock Diagram

2.8 OOB Power and Reset

Timing for control of the 3.3V power enable and reset of the M.2 modules should adhere to the PCIe specification. Figure 7 shows the recommended timing.

- PERST_RISER_N - Active low signal coming from the motherboard (PERST#).
- OOB_RST_1_N is the active low signal coming from the I2C IO expander shown in Figure 2.
- PERST_M2_1_N is the PERST# input to the M.2 module.
- PWR_G1 is the FET control signal driven by the I2C IO expander shown in Figure 6
- P3V3_M2_1 is the 3.3V power output of the FET to the M.2 module

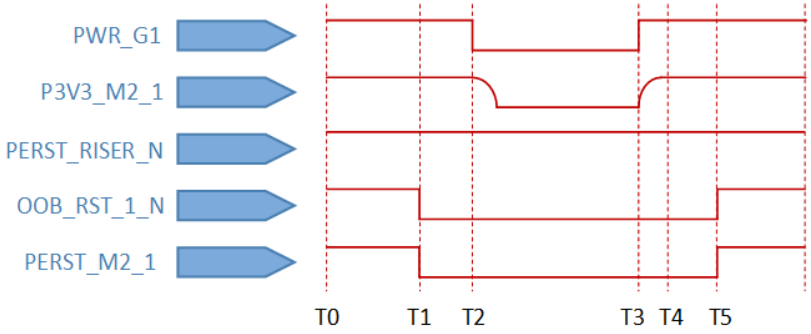


Figure 7. PCIe reset timing diagram for optional FET control

The timing sequence is as follows:

- T0-T1: Normal operation.
- T1: To initiate a reset, the GPIO OOB_RST_1_N is asserted.
- T1-T2: After sufficient timing as per the PCIe specification, PWR_G1 is de-asserted which causes P3V3_M2_1 to fall out of regulation.
- T3: After the module has been powered off for a sufficient amount of time, PWR_G1 is asserted.
- T4: P3V3_M2_1 is stable once again.
- T4-T5: After sufficient timing as per the PCIe specification, OOB_RST_1_N is released.

2.9 PCB Stackup

The stackup should use a sufficiently low-loss material, such that the PCIe signals can be driven at 8 GT/s without the need for redrivers. The carrier card plus the M.2s must meet the channel loss requirements as defined in the PCIe CEM specification.

The PCB should have an ENIG finish or equivalent to prevent oxidation.

2.9.1 6 Layer Stackup

Below is a suggested stackup, with EM888 provided as a reference.

			PCB Stack-up					
Layer	Material: EM-888					Copper Coverage (%)	Design Thickness	Stacking Thickness
			Glass Type	DK at 1 GHz	DK at 4 GHz			Unit : mil
	Solder mask		Green Liquid	3.75	3.75		0.60	0.60
TOP	SIG	Copper	1/2 oz+plating			50	2.00	2.00
		p.p	1086	3.46	3.41		3.90	3.54
L2	GND	Copper	1 oz			70	1.20	1.20
		core	3313	3.79	3.75		4.00	4.00
L3	SIG/PWR	Copper	1 oz			30	1.20	1.20
		p.p	2113x4	3.71	3.66		17.20	15.52
		core	1037x2	3.4	3.35		7.00	7.00
		p,p	2113x4	3.71	3.66		17.20	15.52
L4	SIG/PWR	Copper	1 oz			30	1.20	1.20
		core	3313	3.79	3.75		4.00	4.00
L5	GND	Copper	1 oz			70	1.20	1.20
		p.p	1086	3.46	3.41		3.90	3.54
BOT	SIG	Copper	1/2 oz+plating			50	1.80	2.00
	Solder mask		Green Liquid	3.75	3.75		0.60	0.60
			Total thickness:		1.6			63.1
			Specification		1.6			63.0
			Tolerance:	mm				±10 %

2.9.2 8 Layer Stackup

To enable routing of high speed traces, a higher layer count may be required. Below is a suggested stackup.

[To be determined]

2.10 BOM Options

The following table describes 2x BOM options, but additional combinations are possible:

#	Description	SKU 1	SKU 2	Notes
1	Use Hotswap Controller	Yes	No	For power monitoring
2	SMBUS lines connected to 3.3V instead of 1.8V	No	No	For future proofing
3	High power 12V-3.3V VR (18A @ 3.3V)	Yes	No	For future proofing
4	Low power VR (10.5A @ 3.3V)	No	Yes	
5	Bypass M.2 power-control FETs	No	No	
6	Populate attention LEDs	Yes	Yes	
7	Populate status LEDs	Yes	Yes	

3 Connectors

3.1 PCIe Connector

The blade shall support a standard PCIe x16 edge card connector. The pinout for supporting PCIe x16 described in Table 13. For further information, refer to the PCI Express® Card Electromechanical Specification. Note that pin B31 has been repurposed to support automated bifurcation. Additionally pin B12 has been repurposed to add a SMBus Alert signal.

The card shall also implement the hot-plug present detection scheme as defined in the PCIe CEM spec. Since this is a x16 card, pin B81 (PRSNT#2) should be connected to pin A1 (PRSNT#1).

Table 1. PCIe x16 Connector Pinout

Pin	Side B Connector		Side A Connector	
#	Name	Description	Name	Description
1	+12v	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12v	+12 volt power	+12v	+12 volt power
3	+12v	+12 volt power	+12v	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3v	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3v	+3.3 volt power
10	3.3Vaux	3.3v volt power	+3.3v	+3.3 volt power
11	WAKE#	Link Reactivation	PERST#	Fundamental reset
Mechanical Key				
12	SMBALERT#	SMBus Alert	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock
14	PETP(0)	Transmitter Lane 0,	REFCLK-	Differential pair
15	PETN(0)	Differential pair	GND	Ground
16	GND	Ground	PERP(0)	Receiver Lane 0,
17	PRSNT#2	Presence detect	PERN(0)	Differential pair
18	GND	Ground	GND	Ground
19	PETP(1)	Transmitter Lane	RSVD	Reserved

		1,		
20	PETN(1)	Differential pair	GND	Ground
21	GND	Ground	PERP(1)	Receiver Lane 1,
22	GND	Ground	PERN(1)	Differential pair
23	PETP(2)	Transmitter Lane 2,	GND	Ground
24	PETN(2)	Differential pair	GND	Ground
25	GND	Ground	PERP(2)	Receiver Lane 2,
26	GND	Ground	PERN(2)	Differential pair
27	PETP(3)	Transmitter Lane 3,	GND	Ground
28	PETN(3)	Differential pair	GND	Ground
29	GND	Ground	PERP(3)	Receiver Lane 3,
30	RSVD	Reserved	PERN(3)	Differential pair
31	BIFURx4	1 = PCIe x4 Bifurcation	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETP(4)	Transmitter Lane 4,	RSVD	Reserved
34	PETN(4)	Differential pair	GND	Ground
35	GND	Ground	PERP(4)	Receiver Lane 4,
36	GND	Ground	PERN(4)	Differential pair
37	PETP(5)	Transmitter Lane 5,	GND	Ground
38	PETN(5)	Differential pair	GND	Ground
39	GND	Ground	PERP(5)	Receiver Lane 5,
40	GND	Ground	PERN(5)	Differential pair
41	PETP(6)	Transmitter Lane 6,	GND	Ground
42	PETN(6)	Differential pair	GND	Ground
43	GND	Ground	PERP(6)	Receiver Lane 6,
44	GND	Ground	PERN(6)	Differential pair
45	PETP(7)	Transmitter Lane 7,	GND	Ground
46	PETN(7)	Differential pair	GND	Ground
47	GND	Ground	PERP(7)	Receiver Lane 7,
48	PRSNT#2	Hot plug detect	PERN(7)	Differential pair
49	GND	Ground	GND	Ground

50	PETP(8)	Transmitter Lane 8, Differential pair	RSVD	Reserved
51	PETN(8)		GND	Ground
52	GND	Ground	PERP(8)	Receiver Lane 8, Differential pair
53	GND	Ground	PERN(8)	
54	PETP(9)	Transmitter Lane 9, Differential pair	GND	Ground
55	PETN(9)		GND	Ground
56	GND	Ground	PERP(9)	Receiver Lane 9, Differential pair
57	GND	Ground	PERN(9)	
58	PETP(10)	Transmitter Lane 10, Differential pair	GND	Ground
59	PETN(10)		GND	Ground
60	GND	Ground	PERP(10)	Receiver Lane 10, Differential pair
61	GND	Ground	PERN(10)	
62	PETP(11)	Transmitter Lane 11, Differential pair	GND	Ground
63	PETN(11)		GND	Ground
64	GND	Ground	PERP(11)	Receiver Lane 11, Differential pair
65	GND	Ground	PERN(11)	
66	PETP(12)	Transmitter Lane 12, Differential pair	GND	Ground
67	PETN(12)		GND	Ground
68	GND	Ground	PERP(12)	Receiver Lane 12, Differential pair
69	GND	Ground	PERN(12)	
70	PETP(13)	Transmitter Lane 13, Differential pair	GND	Ground
71	PETN(13)		GND	Ground
72	GND	Ground	PERP(13)	Receiver Lane 13, Differential pair
73	GND	Ground	PERN(13)	
74	PETP(14)	Transmitter Lane 14, Differential pair	GND	Ground
75	PETN(14)		GND	Ground
76	GND	Ground	PERP(14)	Receiver Lane 14, Differential pair
77	GND	Ground	PERN(14)	
78	PETP(15)	Transmitter Lane 15, Differential pair	GND	Ground
79	PETN(15)		GND	Ground

80	GND	Ground	PERP(15)	Receiver Lane 15,
81	PRSNT#2	Hot plug present detect	PERN(15)	Differential pair
82	RSVD#2	Hot Plug Detect	GND	Ground

3.2 M.2 Connector

The pin-out shall follow the M.2 Socket 3, M-key pin-out defined in the M.2 specification. The pinout includes SMBus pin definitions contained in the ECN to the PCIe M.2 Specification, titled "SMBus interface for SSD Socket 2 and Socket 3" (August 11, 2014). This update assigns SMBus pins to pins 44, 42, and 40. The pinout is shown in Table 2.

Table 2. M.2 Connector Pinout

M.2 Module Standard Pinout					
Pin	**Signal**	**Description**	**Pin**	**Signal**	**Description**
74	3.3V	3.3V Power.	75	GND	Ground
72	3.3V	3.3V Power	73	GND	Ground
70	3.3V	3.3V Power	71	GND	Ground
68	SUSCLK(32KHz)	Reduce Power Clock	69	NC	Reserved
66	KEY	Module Key	67	GND	Ground
64	KEY	Module Key	65	KEY	Module Key
62	KEY	Module Key	63	KEY	Module Key
60	KEY	Module Key	61	KEY	Module Key
58	NC	Reserved	59	KEY	Module Key
56	NC	Reserved	57	GND	Ground
54	PEWAKE#	PCIe PME Wake (OD)	55	REFLKCP	PCIe Reference Clock
52	CLKREQ#	Reference Clock Request	53	REFLKCN	PCIe Reference Clock
50	PERST#	PCIe Reset	51	GND	Ground
48	NC	Reserved	49	PETP0	PCIe Transmit Lane 0
46	NC	Reserved	47	PETN0	PCIe Transmit Lane 0
44	SMBALERT#	SMBus Alert	45	GND	Ground
42	SMDATA	SMBus Data	43	PERP0	PCIe Receive Lane 0
40	SMCLK	SMBus Clock	41	PERN0	PCIe Receive Lane 0
38	DEVSLP	Device Sleep	39	GND	Ground
36	NC	Reserved	37	PETP1	PCIe Transmit Lane 1
34	NC	Reserved	35	PETN1	PCIe Transmit Lane 1
32	NC	Reserved	33	GND	Ground
30	NC	Reserved	31	PERP1	PCIe Receive Lane 1
28	NC	Reserved	29	PERN1	PCIe Receive Lane 1
26	NC	Reserved	27	GND	Ground
24	NC	Reserved	25	PETP2	PCIe Transmit Lane 2
22	NC	Reserved	23	PETN2	PCIe Transmit Lane 2

20	NC	Reserved	21	GND	Ground
18	3.3V	3.3V Power	19	PERP2	PCIe Receive Lane 2
16	3.3V	3.3V Power	17	PERN2	PCIe Receive Lane 2
14	3.3V	3.3V Power	15	GND	Ground
12	3.3V	3.3V Power	13	PETP3	PCIe Transmit Lane 3
10	DAS/DSS#	Drive Active Signal (OD)	11	PETN3	PCIe Transmit Lane 3
8	NC	Reserved	9	GND	Ground
6	NC	Reserved	7	PERP3	PCIe Receive Lane 3
4	3.3V	3.3V Power	5	PERN3	PCIe Receive Lane 3
2	3.3V	3.3V Power	3	GND	Ground
			1	GND	Ground

4 Component Placement and Labelling

The M.2 connectors shall be silkscreened in large font, on both top and bottom sides of the card.

No silkscreen shall be placed over high speed traces on the top or bottom layer.

5 FRUID Contents

The format of the contents of the FRUID EEPROM should follow the IPMI TBD spec. The contents of the FRUID are defined below in Table 3.

Offset	Name	Description

Table 3 FRUID Contents

6 Mechanical

6.1 Mechanical Drawing

The card shall meet the PCIe CEM Specification Rev 3.0 for a full height, half-length form factor PCIe card including top and bottom side component height and keepout requirements. M.2 modules shall be oriented to support a longitudinal airflow allowing air to traverse the length of the card before intersecting with the M.2 connectors. The mechanical drawing is shown in Figure 8**Error! Reference source not found.**.

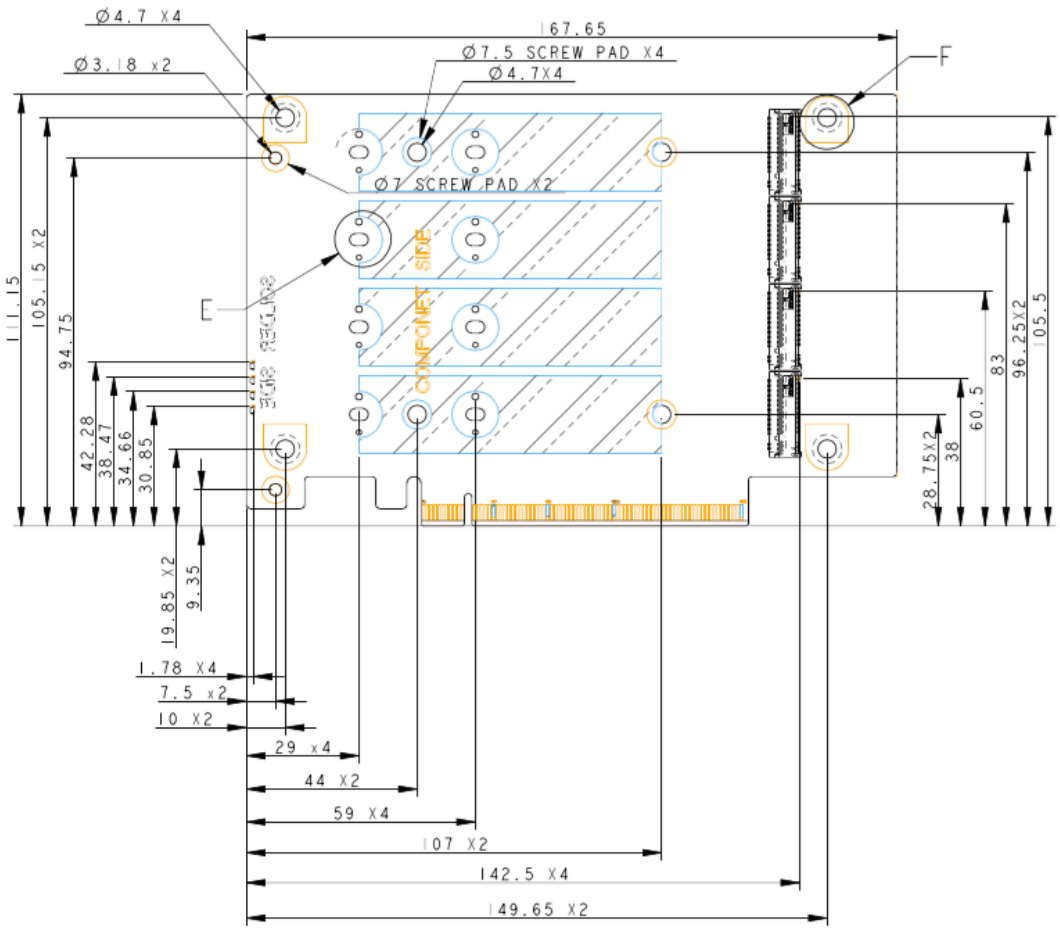


Figure 8. Mechanical Drawing

6.2 M.2 Support

6.2.1 M.2 module types

The card shall support type 2280 and 22110 M.2 modules. It must also support M.2's with a maximum of 1.5mm bottom-side height and a maximum top-side height of 3.1mm.

6.2.2 M.2 module retention

The card shall support The M.2 module retention is a single piece that presses into the board, and retains the modules with a plastic tab. An example is shown in Figure 9.

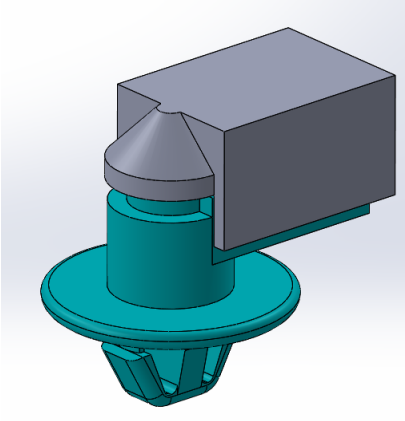


Figure 9. M.2 module retention

6.2.3 M.2 mounting hole

The M.2 retention clip requires a hole in the PCB with the dimensions as shown in Figure 10.

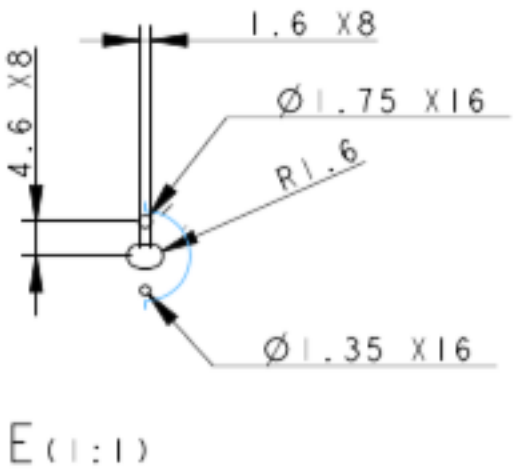
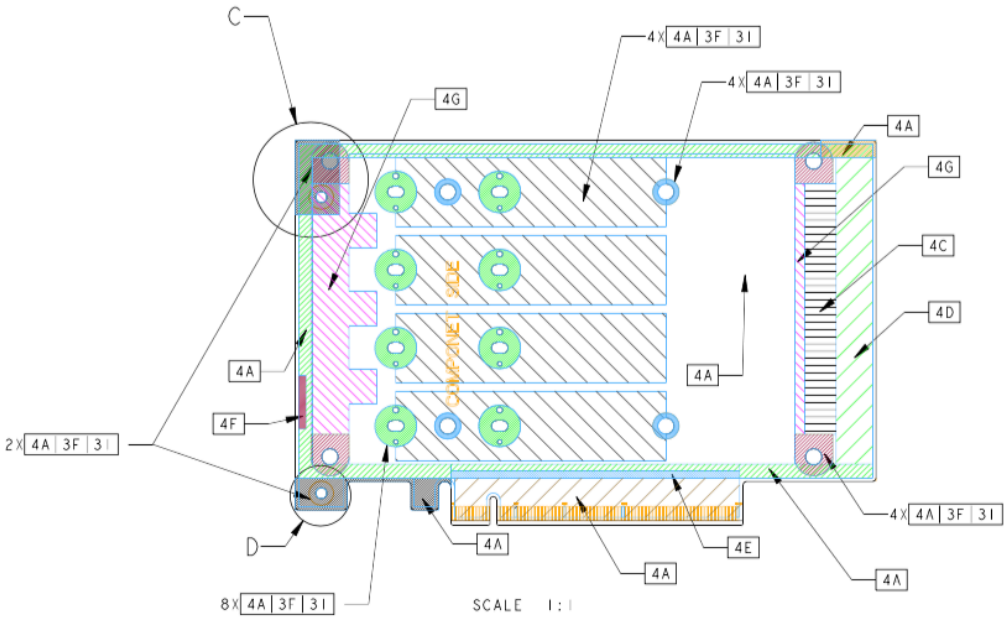


Figure 10 M.2 mounting hole dimensions

6.3 M.2 Thermal Interface

The card shall support a keepout area under the M.2 modules, with a copper pour to help conduct heat from the modules into the PCB using a thermal pad. An appropriate thermal interface material (TIM) shall be used between the M.2 module and the PCB surface. The design shall support optimization of thermal conductivity by maximizing via stitching to the solid GND copper planes on the internal layers of the board.

Because the TIM will have a different dielectric constant from air, high speed traces are not to be routed such that they are in a layer that touches the TIM.



NOTE: (UNLESS OTHERWISE SPECIFIED):

1. MATERIAL: 1.57+/-.13 MM THICK , NEMA GRADE FR-4 ,

2. COMPONENTS DIMENSIONED TO PIN 1.

3. INDICATED AREA SHALL BE:
   A- COPPER FREE
   B- COMPONENT FREE
   C- CONDUCTOR FREE
   D- THROUGH HOLE COMPONENT FREE.
   E- COPPER PAD COVERED WITH SOLID SOLDER MASK CONNECTED TO GROUND . (GROUND PAD)(W/VIA)
   F- COPPER PAD COVERED WITH SOLID SOLDER MASK CONNECTED TO GROUND . (GROUND PAD)
   G- COMPONENT FREE, EXCEPT FOR INDICATED CONN.
   H- VIA FREE.
   I- TRACE FREE

4. COMPONENT HEIGHT IN THIS AREA SHALL BE:
   A- 0.00MM MAX.
   B- 2.67MM MAX.
   C- 5.00MM MAX.
   D- 11.00MM MAX.
   E- 0.5MM MAX.
   F- 0.6MM MAX.
   G- 2.0MM MAX.

5. DRAWING FOR ECAD DESINGER REFERENCE ONLY . ECAD LAYOUT SHALL MATCH LATEST PRO-E IDF FILE

Figure 11. Component Keepout - Top Side

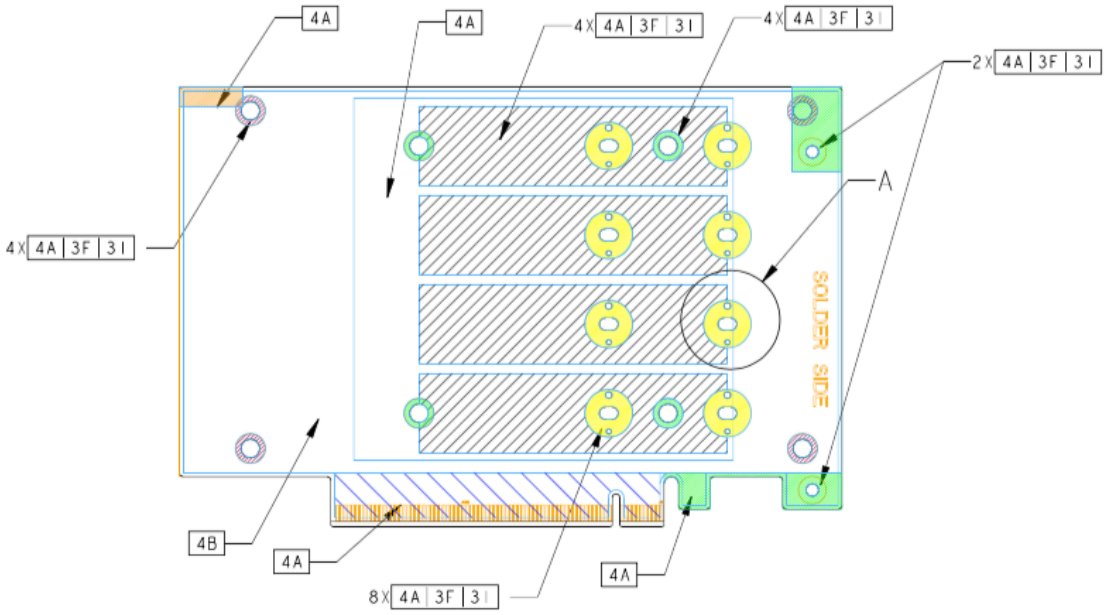


Figure 12. Component Keepout – Bottom Side

6.5 Air guides and Heatsinks

The card shall support air guides to minimize air bypass into the system, and maximize the cooling over critical components of the modules. The air guides are shown in Figure 13.

[To be determined]

Figure 13. PCIe Card with Air Guides

7 Environmental

7.1 Shock & Vibration

This carrier card shall meet the same shock & vibration requirements specified at the system level.

7.2 Regulatory

This carrier card shall meet CE, CB, FCC Class A, WEEE, and ROHS requirements.

8 Labels and Markings

The carrier card shall have the following barcoded labels in visible locations where they can be easily scanned during integration. Vendor and Facebook will have an agreement for the label locations.

- Vendor P/N, S/N, REV (revision would increment for any approved changes)
- Facebook P/N (or OCP customer P/N)
- Date code (industry standard: WEEK/YEAR)
- The assembly shall be marked “THIS SIDE UP”, “TOP SIDE”, “UP ^” or other approved marking in bright, large characters in a color to be defined by ODM and Facebook (or OCP customer). This printing may be on the PCB itself, or on an installed component such as an air baffle. The label should be clear and easy to read in low light conditions, when viewed from above or below from 2 feet away and at an angle of approximately 60 degrees off horizontal.

9 Revision History

Author	Description	Revision	Date
Chris Petersen / Dominic Cheng	Initial draft spec	0.1	1/29/2016
Mark/Dominic/Chris	Lots of changes	0.2	3/1/2016
Mark/Dominic/Chris	1st OCP release	0.3	4/11/2016