

SO-DIMM 2GB ECC

DDR3 (Ch A)

Clock Gen
Clock Buffer

DC/DC

SSD card
SATA Gen3
1

2x6 Header
LPC (Port80)

64Mb Flash
128Mb Flash
MUX
SPI

INTEL
Rangeley

UART
2
MUX
To B2B Connector
1x4 Header

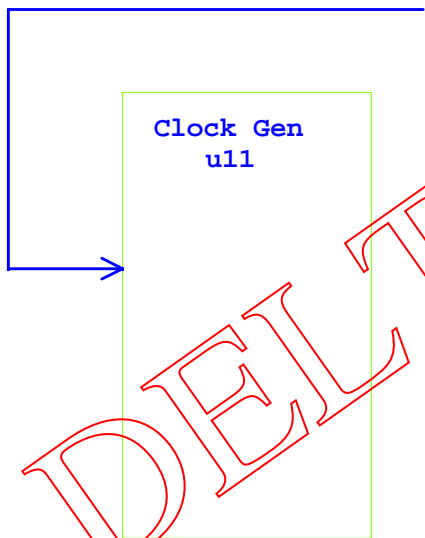
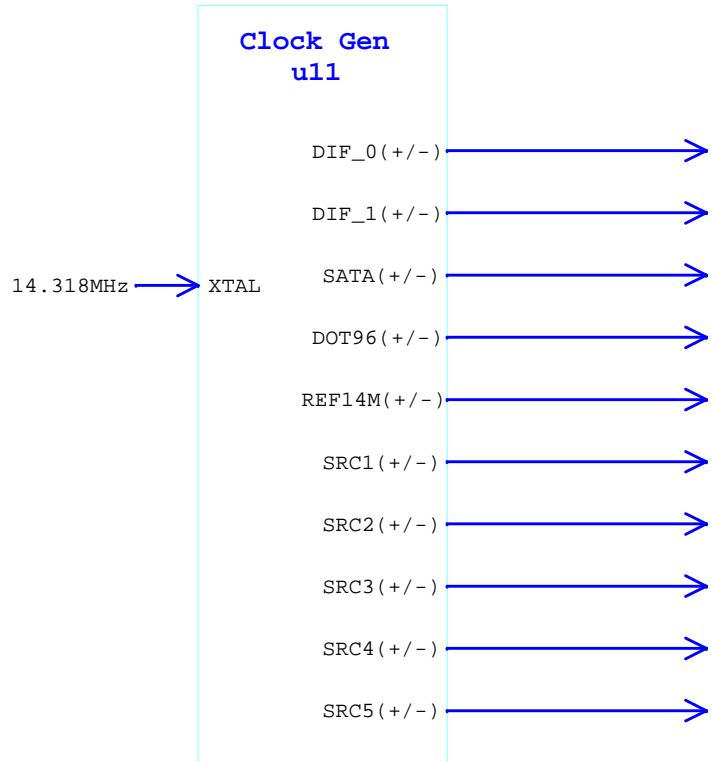
USB 2.0
2
To B2B Connector

To B2B Connector
PCIe Gen2
4

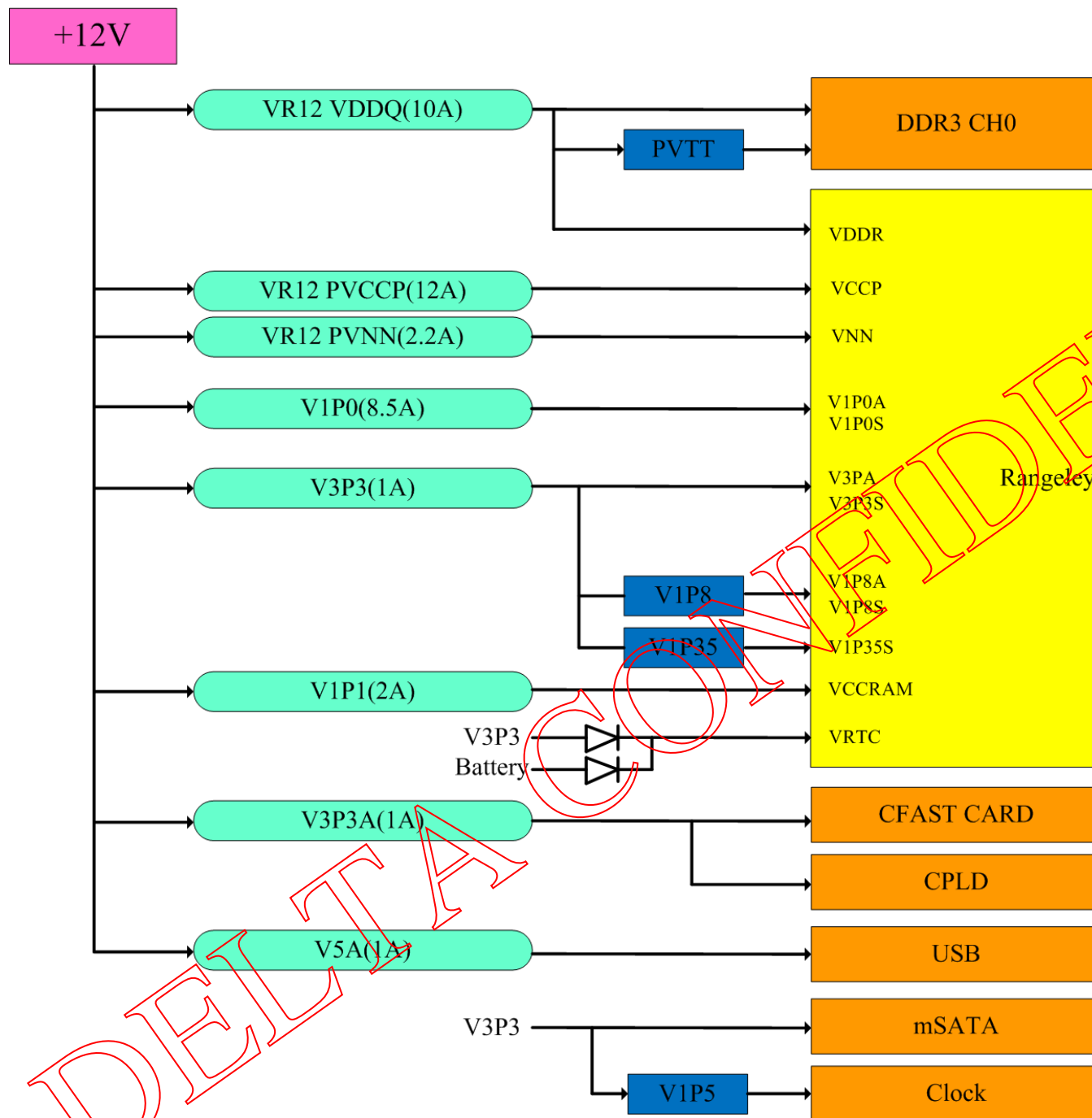
CPLD

B2B Connector(120 pins)

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Title			
02_Function Block			
Size	Document Number	Rev	
C	1ADSS-0XXXXX	00	
Date:	Thursday, May 17, 2018	Sheet	2 of 33



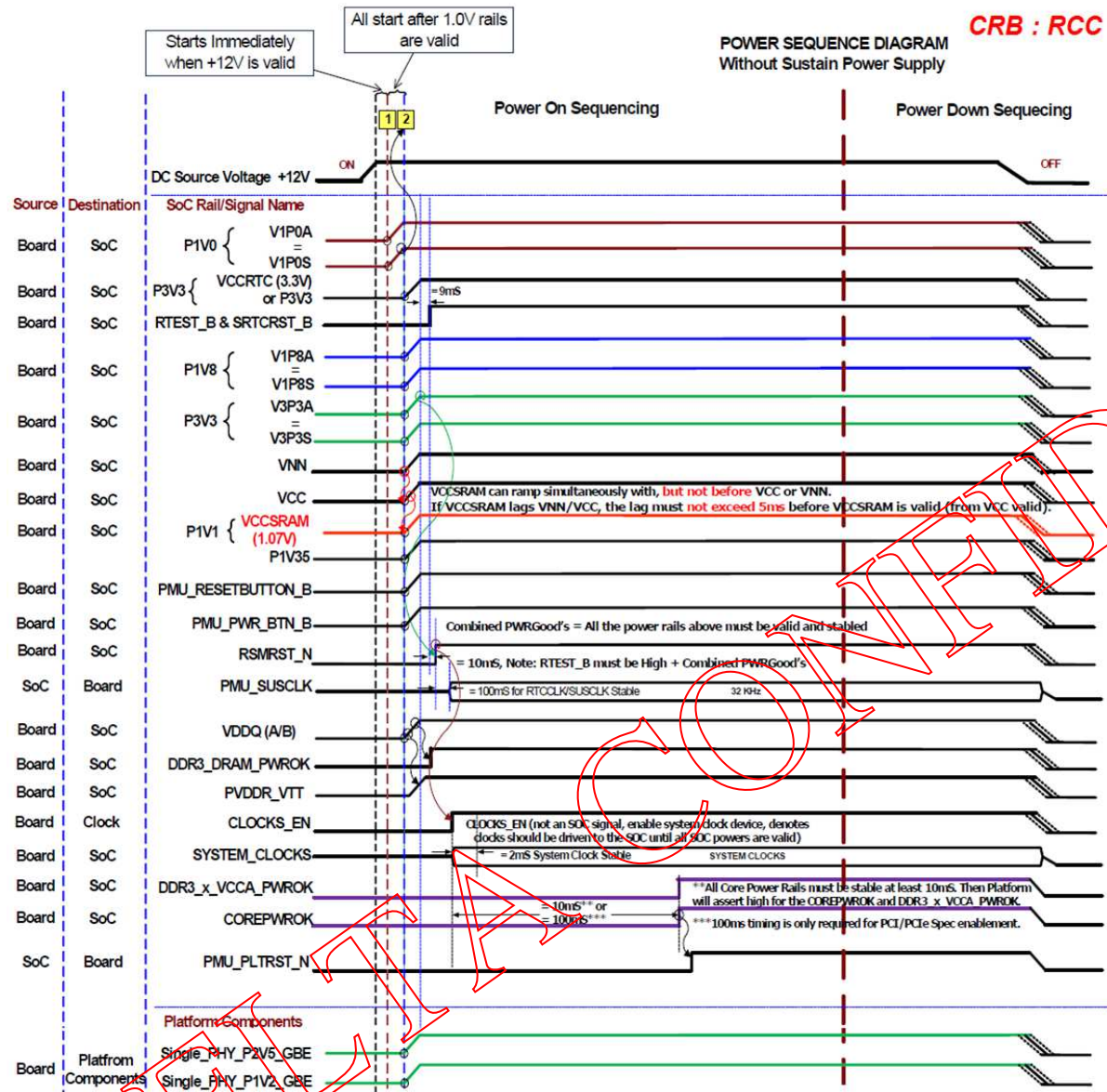
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Title03_Clock Diagram		
SizeC	Document Number1ADSS-0XXXXX	Rev00
Date: Thursday, May 17, 2018	Sheet3 of 33	

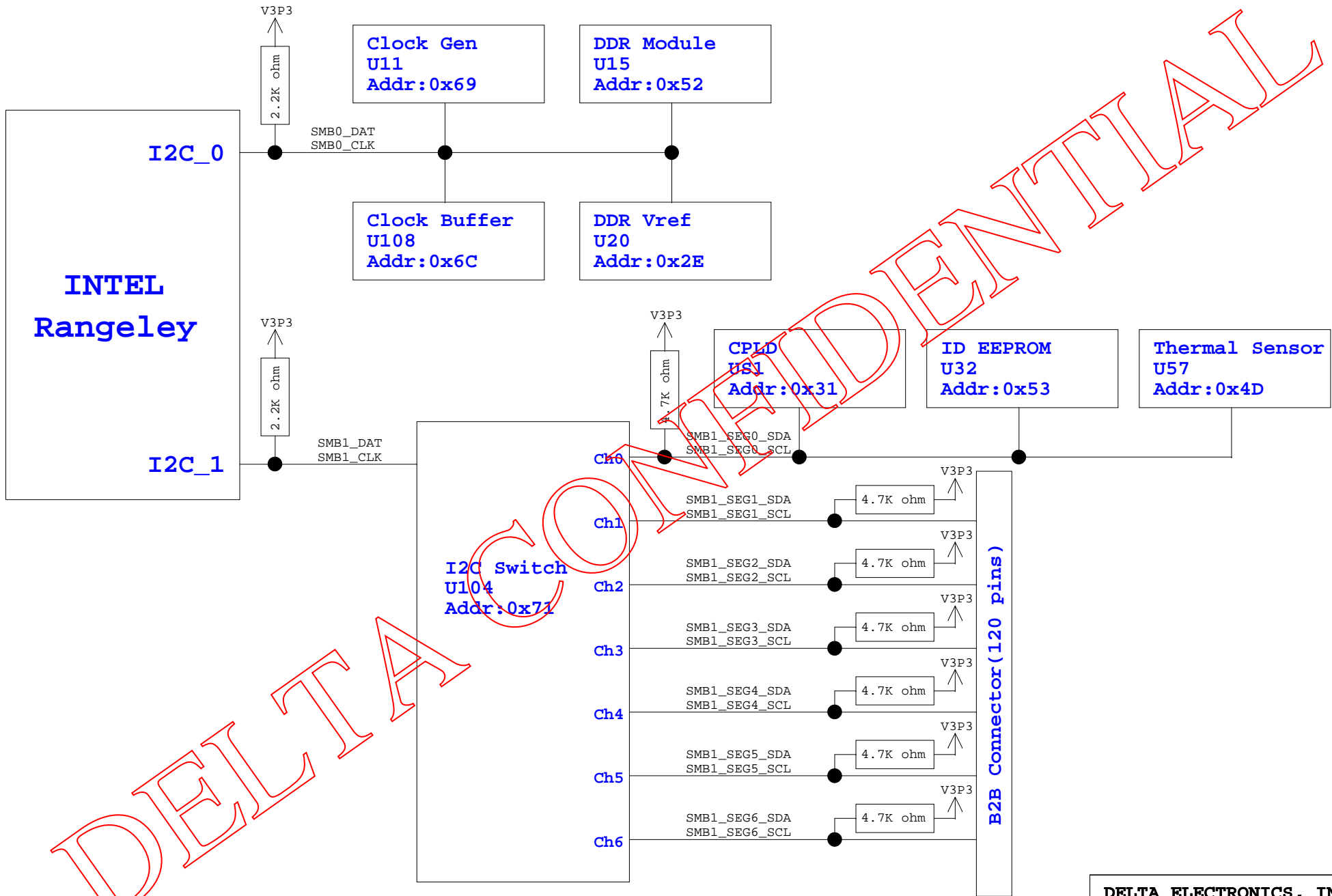


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Title		
04_Power Distribution		
Size	Document Number	Rev
C	1ADSS-0XXXXX	00
Date:	Thursday, May 17, 2018	Sheet 4 of 33





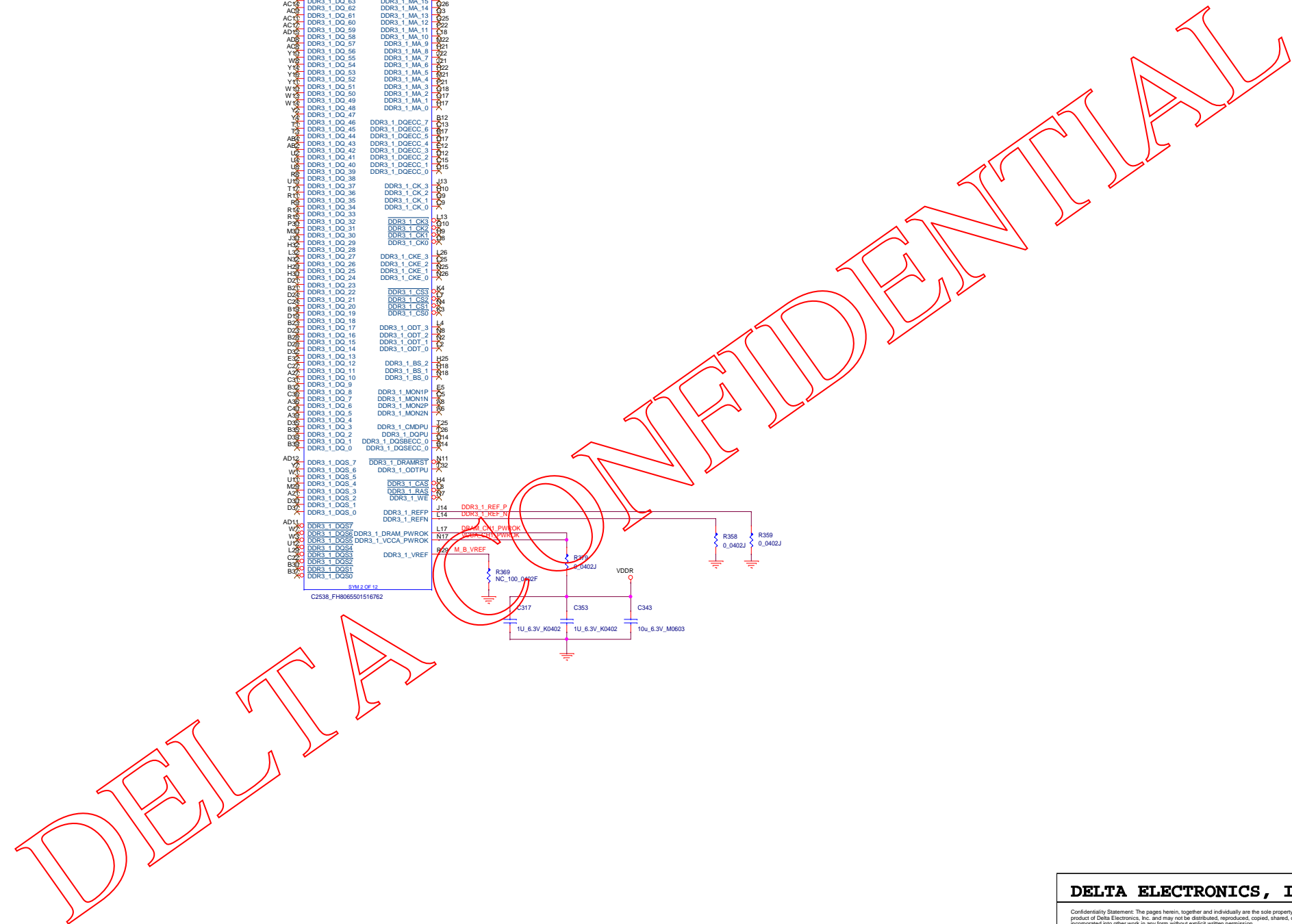
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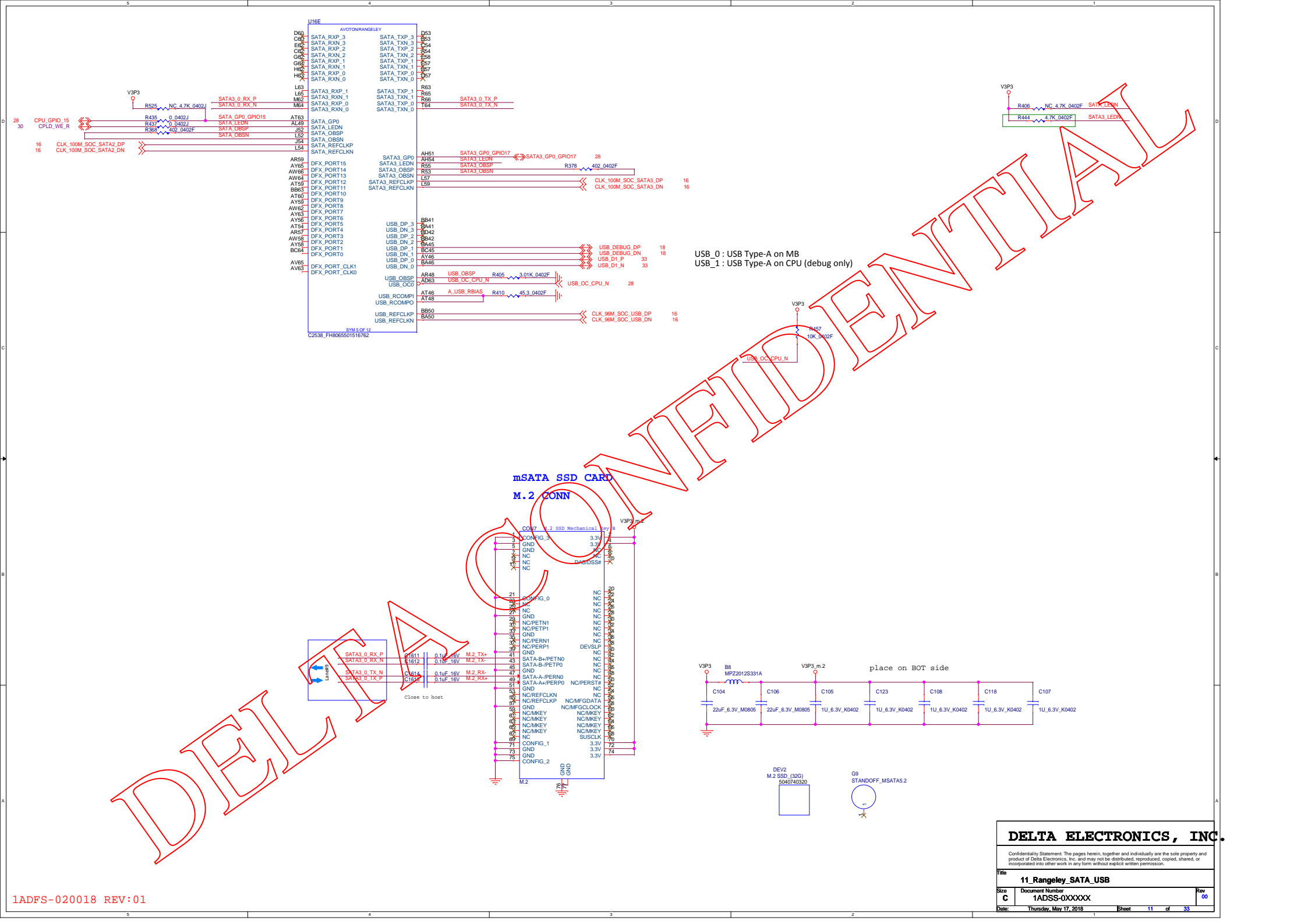
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Title		
06_SMBus Diagram		
Size	Document Number	Rev
C	1ADSS-0XXXXX	00
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Title 07_GPIO Map		
Size C	Document Number 1ADSS-0XXXXX	Rev 00
Date Thursday, May 17, 2018	Sheet 7	of 33





USB_0 : USB Type-A on MB
USB_1 : USB Type-A on CPU (debug only)

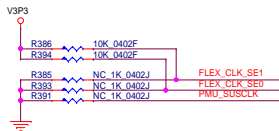
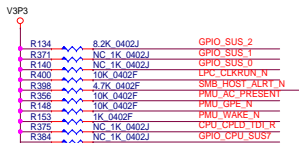
mSATA SSD CARD
M.2 CONN

place on BOT side

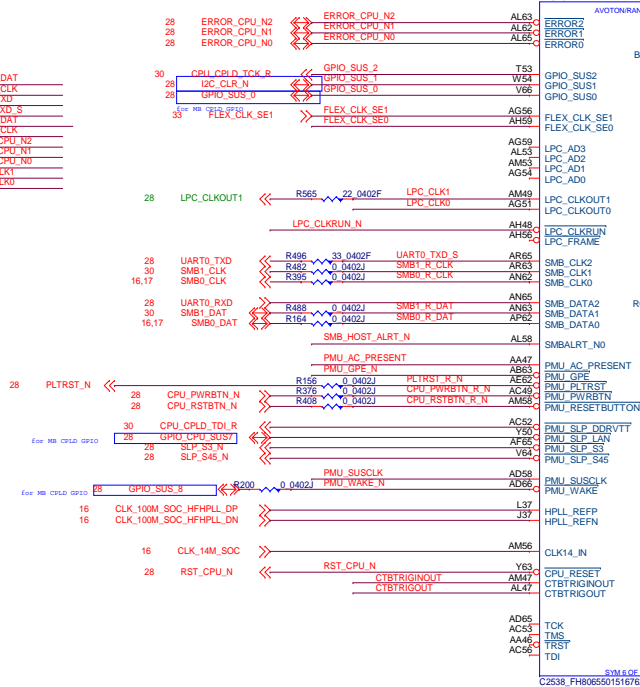
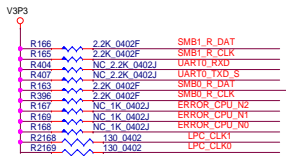
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Title		
11_Rangeley SATA_USB		
Size	Document Number	Rev
C	1ADSS-0XXXXX	00
Date:	Thursday, May 17, 2018	Sheet 11 of 33

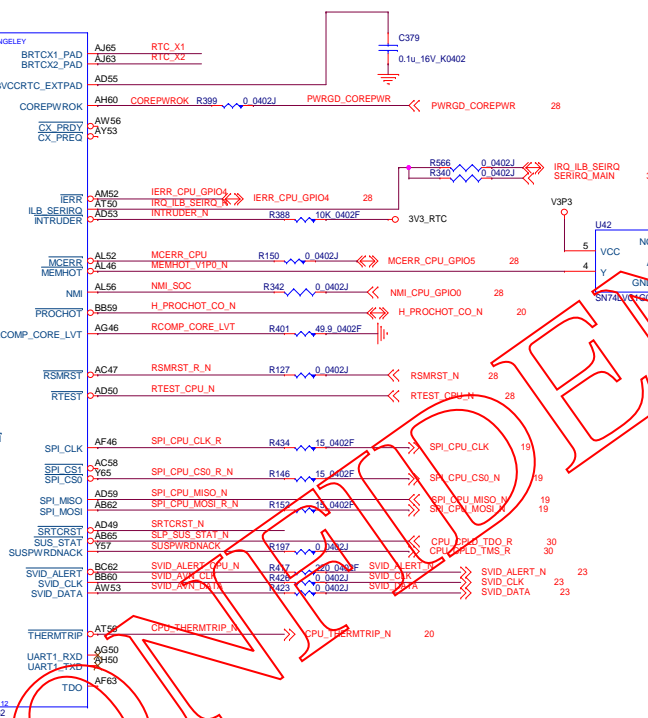
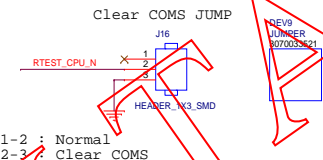


FLEX_CLK_SE0 : BOOT Select, 0 = LPC, 1 = SPI
FLEX_CLK_SE1 : TOP SWAP ACTIVE

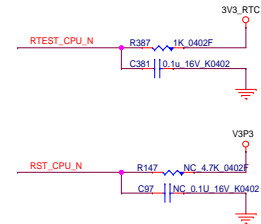
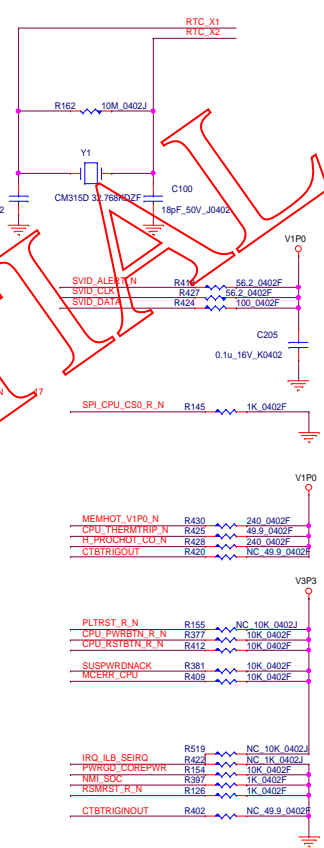
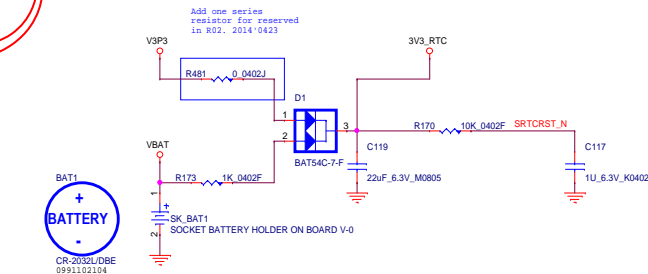


For MB CPU2 GPIO

For MB CPU2 GPIO



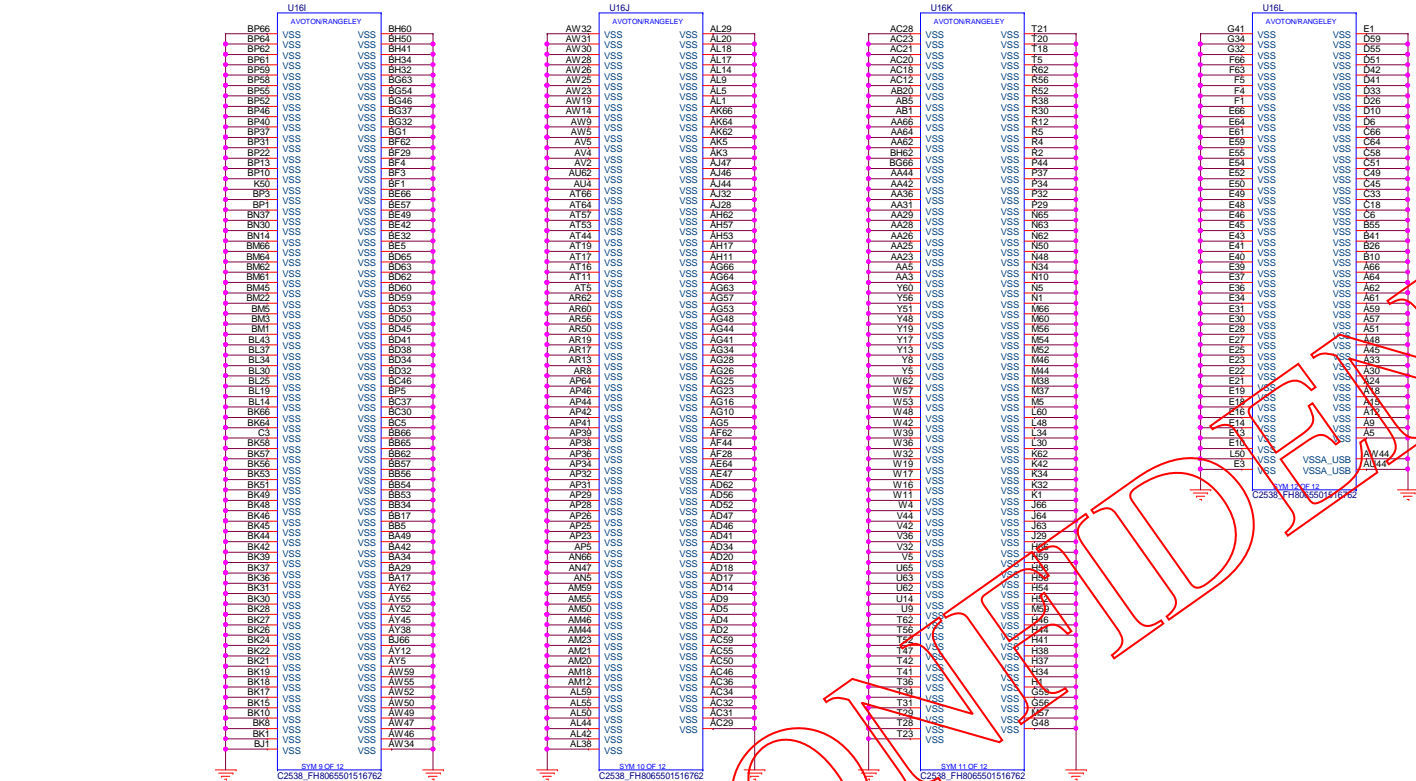
SVMS OF 12
C2538_FH0665501516762



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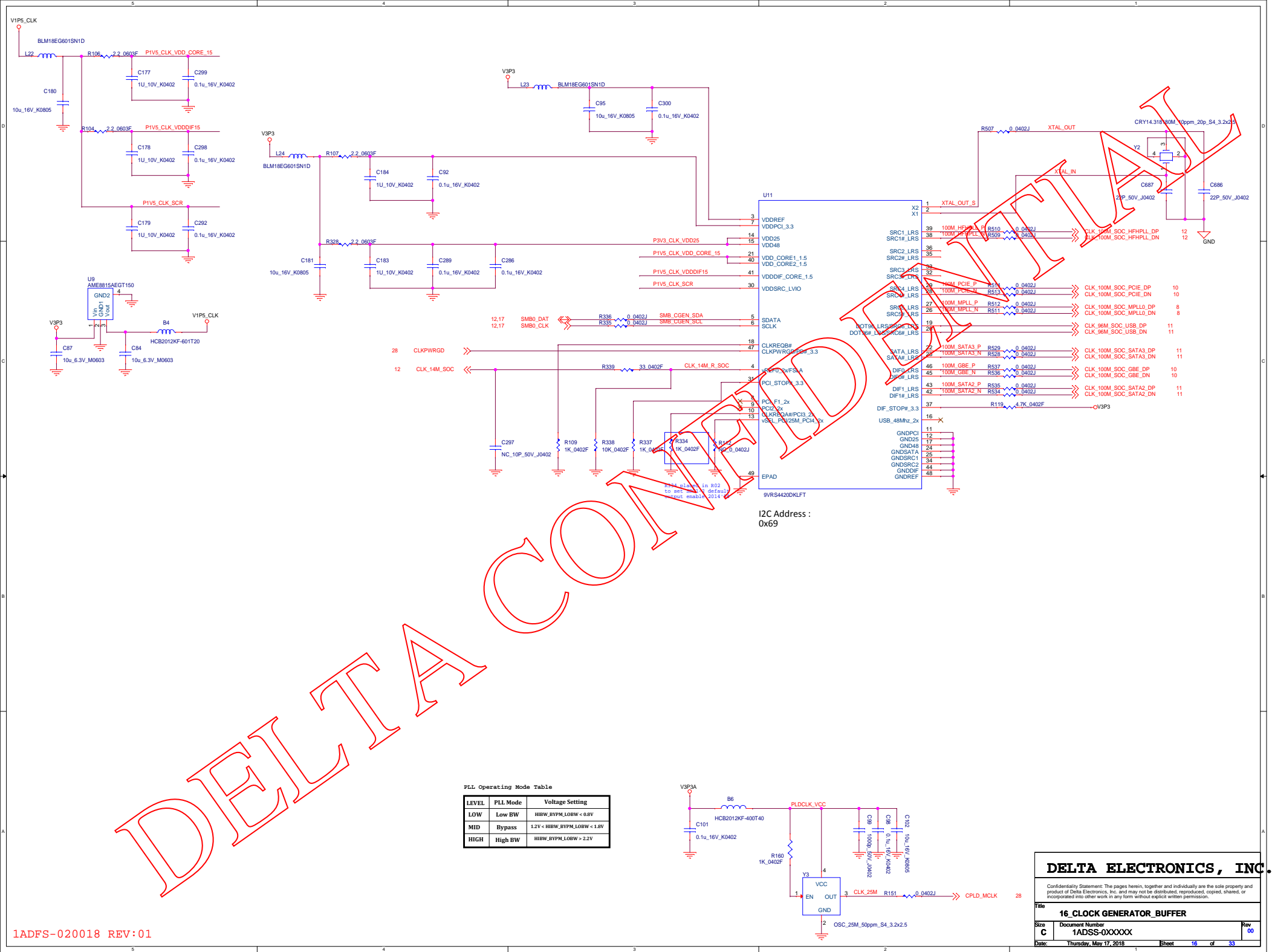
File		
12_Rangeley LPC SMB_MISC		
Size	Document Number	Rev
C	1ADSS-0XXXXX	00
Date:	Thursday, May 17, 2018	Sheet 12 of 33



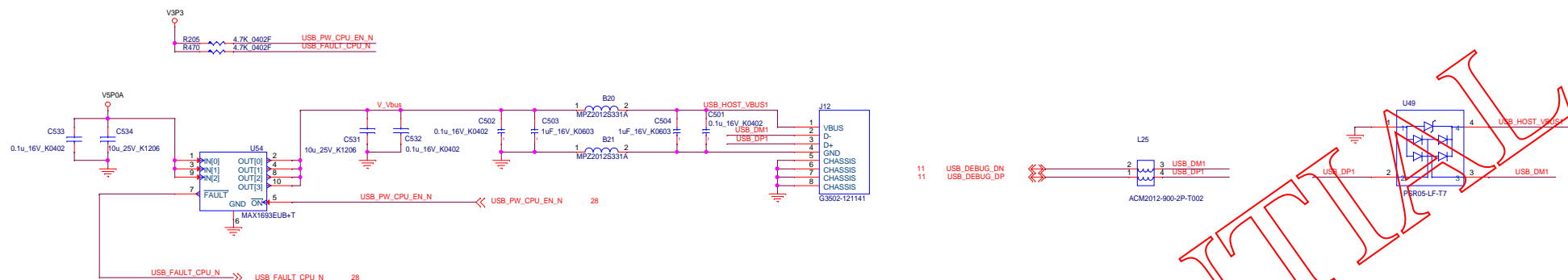
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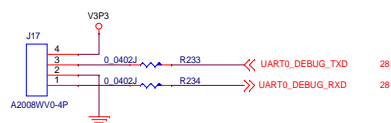
Title		
15_Rangeley_GND		
Size	Document Number	Rev
C	1ADSS-0XXXXX	00
Date:	Thursday, May 17, 2018	Sheet 15 of 33



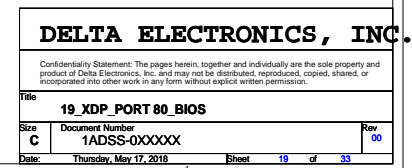
USB Port

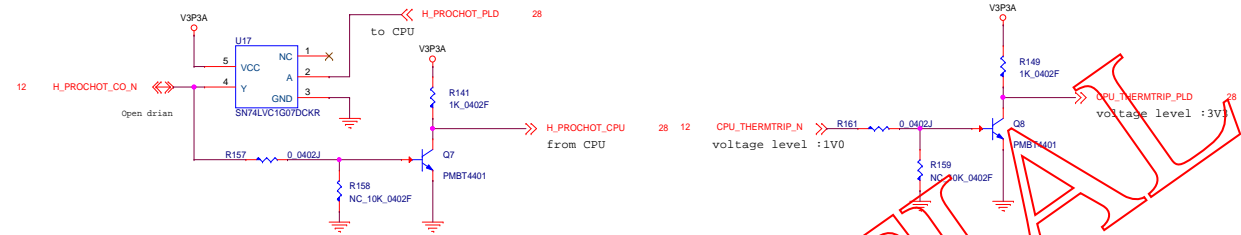
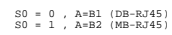


Console Port (RJ45)

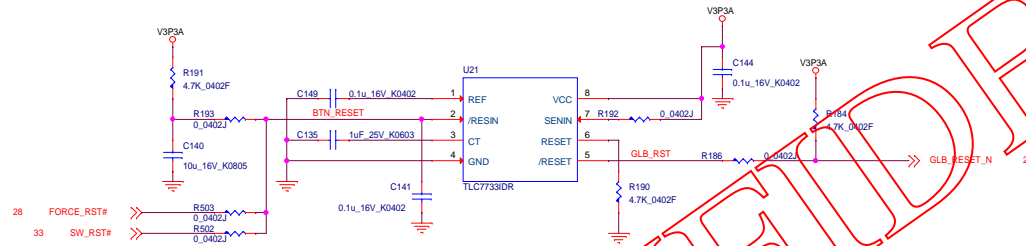


1ADFS-020018 REV:01





Reset IC

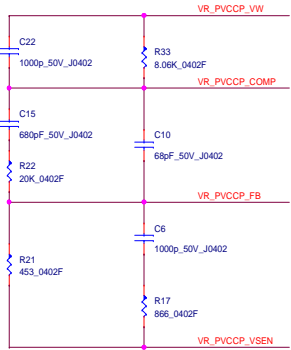


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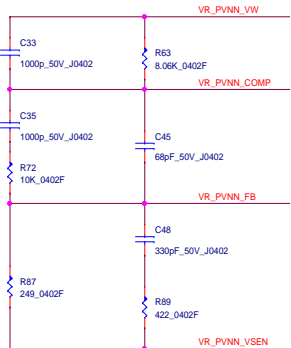
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Title			
20_MISC_RESET_DB-LED_UART_MUX			
Size	Document Number	Rev	
C	1ADSS-0XXXXX	00	
Date:	Thursday, May 17, 2018	Sheet	20 of 33

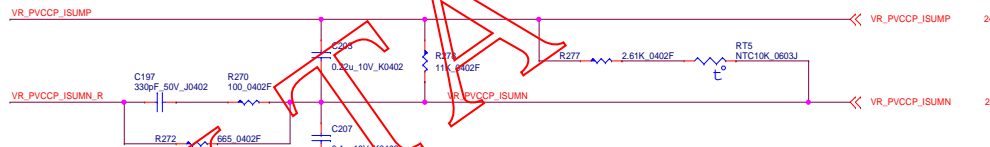
VCCP compensate



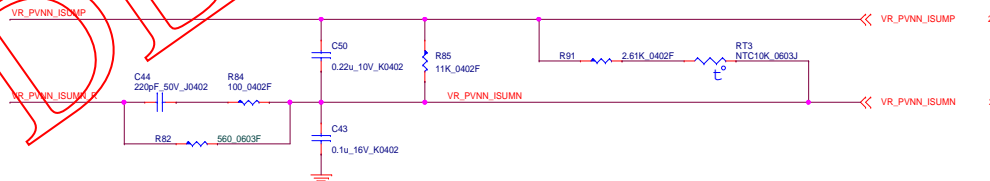
VNN compensate



VCCP Isense compensate

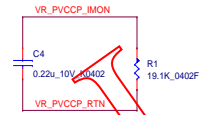


VNN Isense compensate



Set Vboot = 0.9V

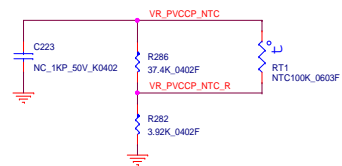
VCCP IMON



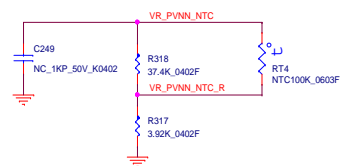
VNN IMON



VCCP TSENSE



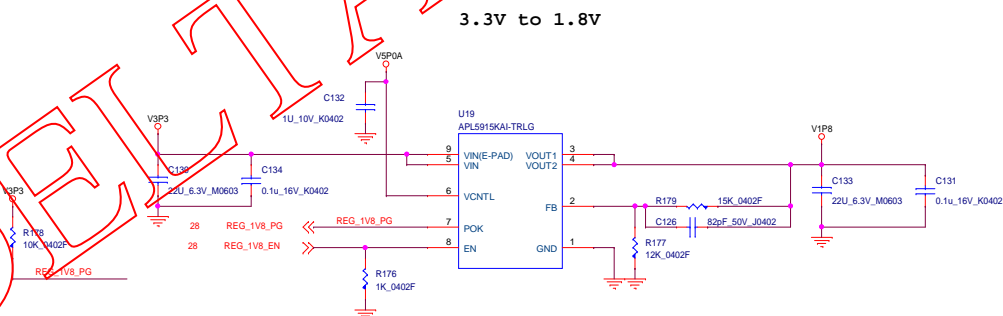
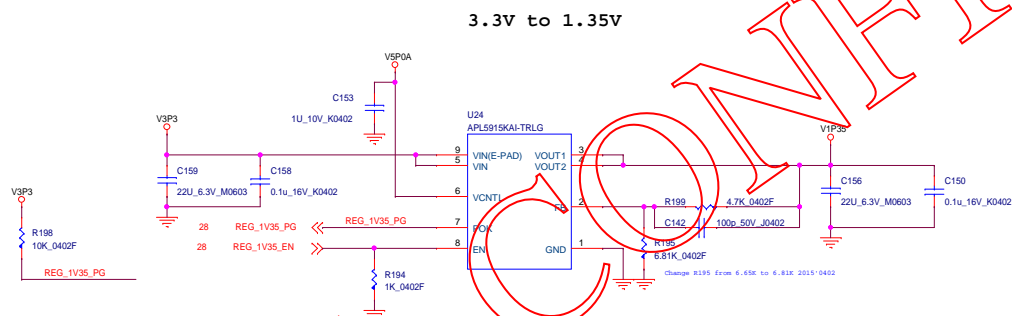
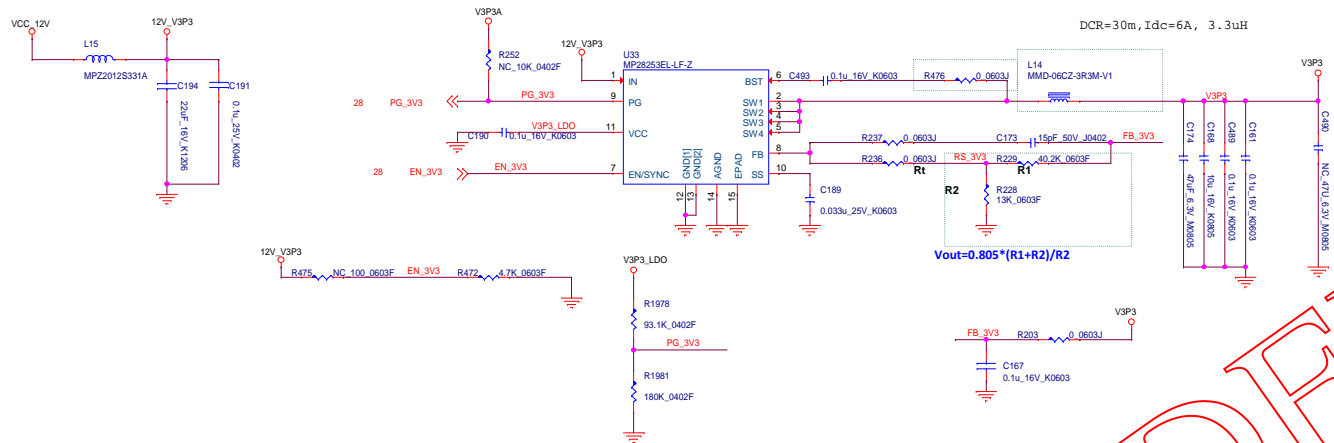
VNN TSENSE



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File		23_POWER_CPU_VCCP_VNN_1	
Size	Document Number	1ADSS-0XXXXX	Rev 00
Date	Thursday, May 17, 2018	Sheet 23 of 33	



5V_early @ 1A

PWM Frequency	500 kHz
MAX Current	1A
OCV	5.6 A
Output Voltage	5V
OVP	6.5V

3.3V_early @ 1A

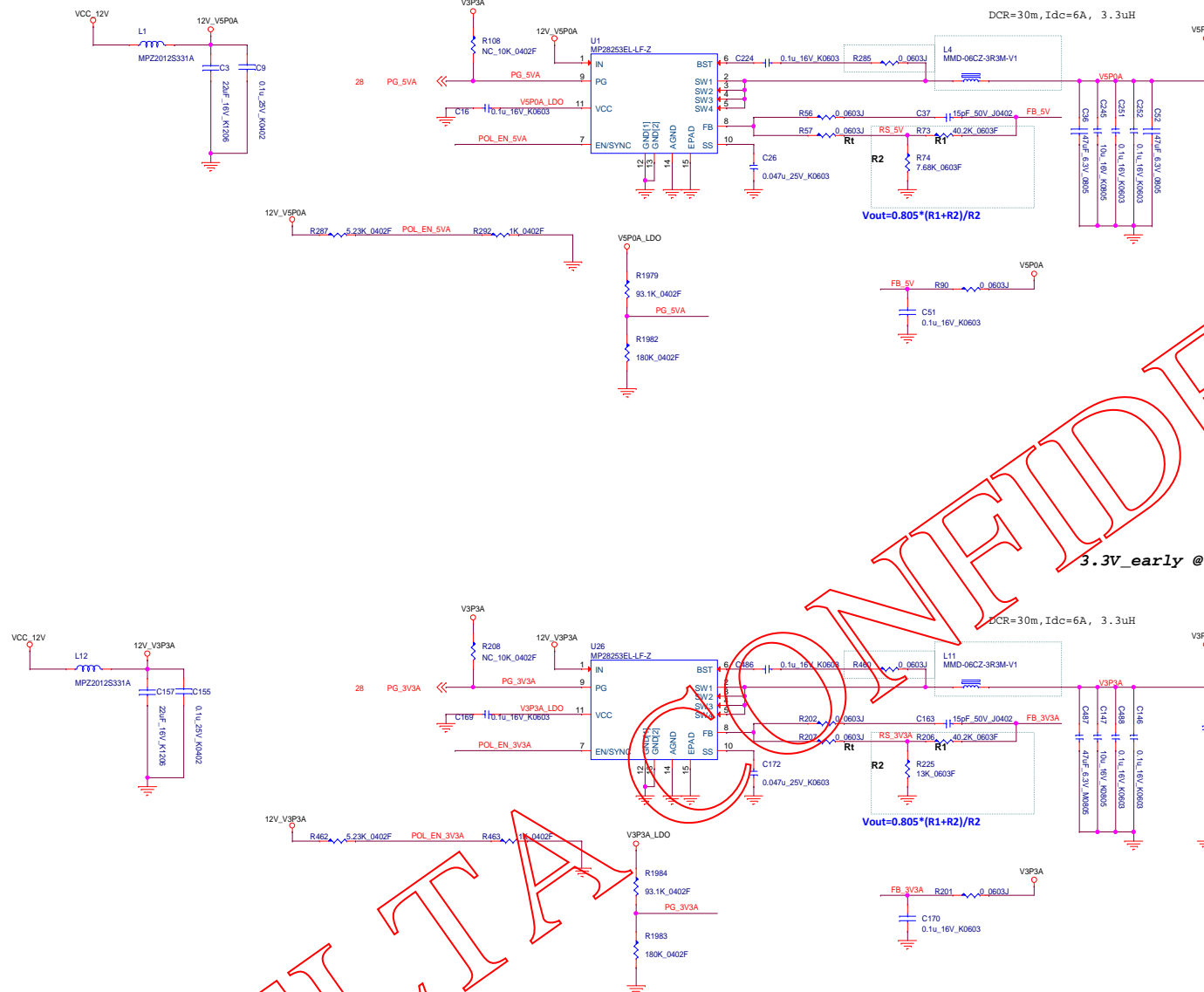
FOR Debug board

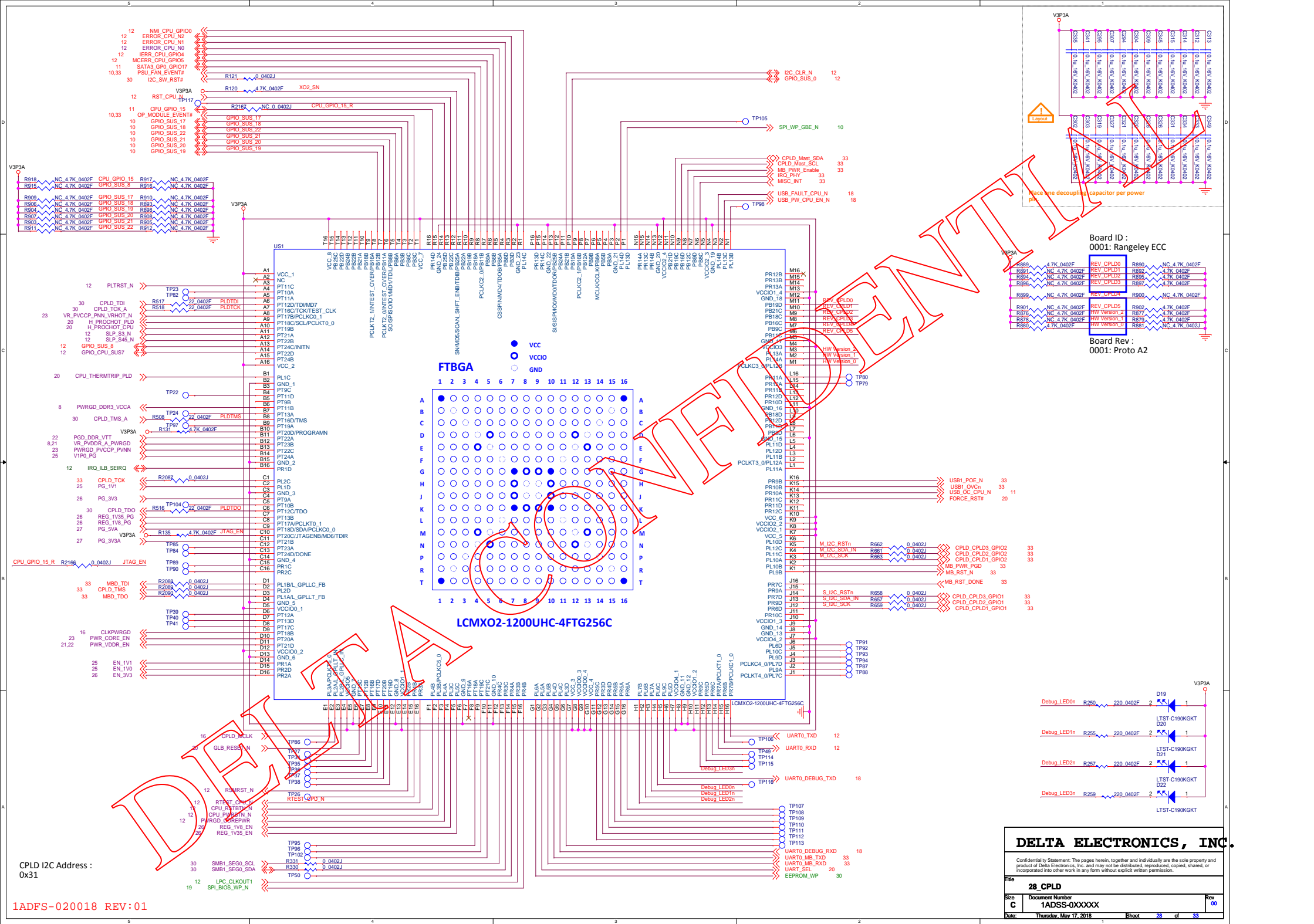
PWM Frequency	500 kHz
MAX Current	1A
OCV	5.6 A
Output Voltage	3.3V
OVP	4.29V

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Title		
27_POWER_CPU_5V0A_3V3A		
Size	Document Number	Rev
C	1ADSS-0XXXXX	00
Date:	Thursday, May 17, 2018	Sheet 27 of 33

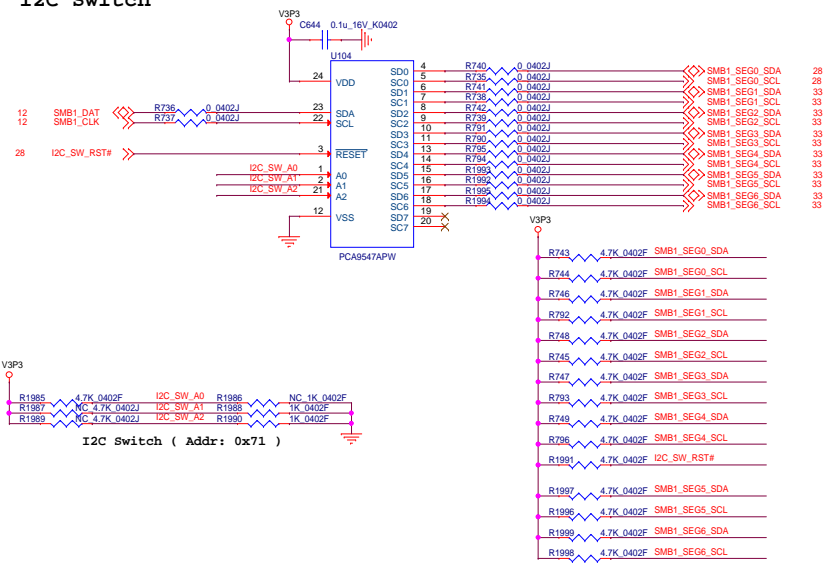




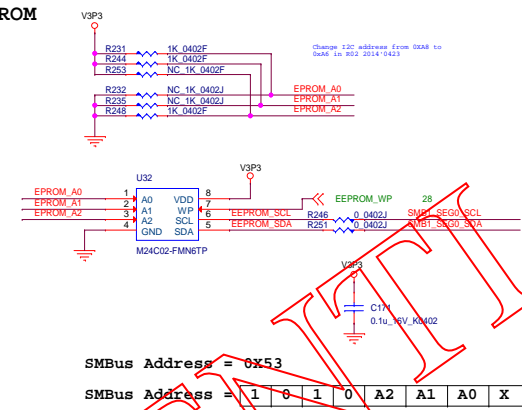
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Title 29_B2B_Connector		
Size C	Document Number 1ADSS-0XXXXX	Rev 00
Date: Thursday, May 17, 2018 Sheet 29 of 33		

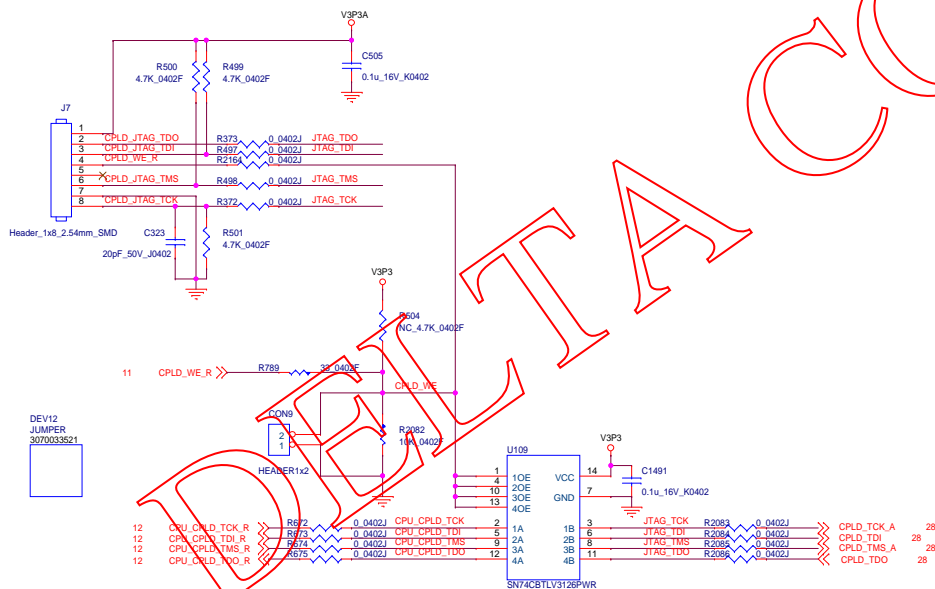
I2C Switch



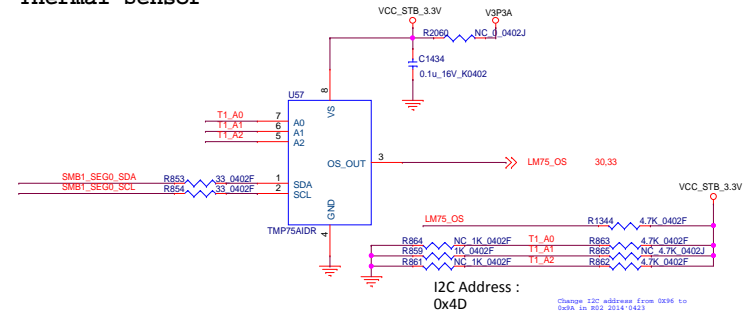
ID EEPROM



SW UPGRADE CPLD CIRCUITS



Thermal Sensor



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Title		
30_I2C_SW_TEMP Sensor_ID EEPROM		
Size	Document Number	Rev
C	1ADSS-0XXXXX	00
Date:	Thursday, May 17, 2018	Sheet 30 of 33

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Title		
31_Debug_GbE_UART		
Size	Document Number	Rev
C	1ADSS-0XXXXX	00
Date:	Thursday, May 17, 2018	Sheet 31 of 33

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Title 32_POWER_ETH_2V5_1V2		
Size C	Document Number 1ADSS-0XXXXX	Rev 00
Date: Thursday, May 17, 2018 Sheet 32 of 33		

