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DELTA AGC7648A Switch Specifications

Revision .01

DELTA ELECTRONICS, Inc.

Fremont CA

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Revision	Description	Data
0.1	- Initial draft	Sep, 2016

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DELTA ELECTRONICS, Inc.

2. Overview

The platform support up to 48 port 10G and 6 port 40/100G switching bandwidth as below

- 48 port x 10G SFP^+
- 6 port x 40/100G QSFP28

Feature

- External Serial MGMT & Console port (RJ45 type).
- 48 port 10Gbps for SFP^+ transceiver.
- 6 port 40/100Gbps for QSFP transceiver
- Management RJ45 supports 10M/100M/1G speeds
- Front panel LED display for System, FAN, and Power status indication.
- Temperature monitoring & overheat shutdown. (TMP75).
- Software readable thermal monitor.
- RTC time clock support.
- Hot plugging redundant power supply.
- Current monitoring for Power management.
- FAN removable and monitoring.
- Standard 1U chassis high

The platform support up to 48 port 10G and 6 port 40/100G switching bandwidth as below

- ***Major Component***

Component	Description
CPU	Rangeley C2538
DDR3	8G
SSD (M.2)	APM2T42P10032GAN-W1TM1G
MAC	BCM88370
TCAM	BCM88659
PHY / (OOB Port)	54616s
PSU	AC 650W *2 or 800W *2
FAN Module	GFC0412DS-SM06XMP *4

Table 1: Major Component

3. Block Diagram of 48 port SFP plus / 6 port QSFP

Block diagram shows connection of important features:

MAC: BCM88370

CPU: C2538

TCAM: NL88659

48 x 10G SFP+ and 6 x 40G/100G QSFP

DDR5 4GB

GMT: N/A

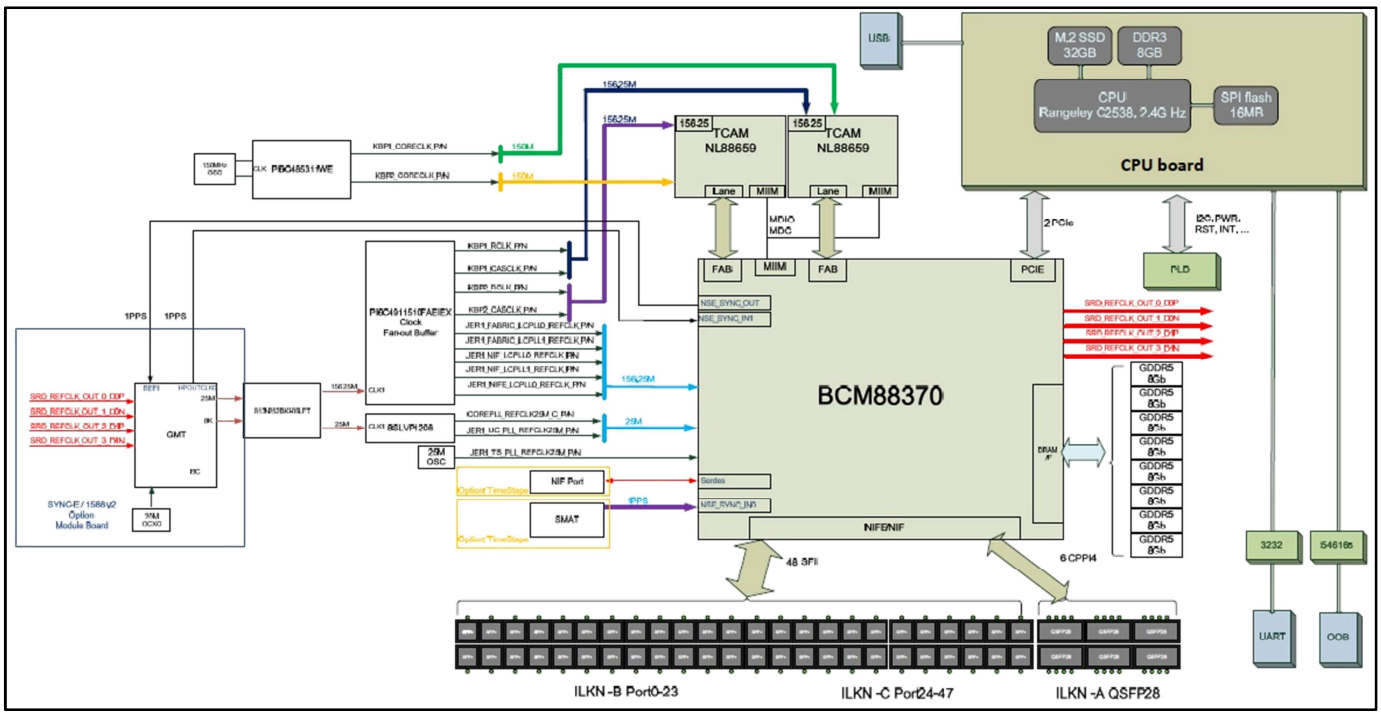
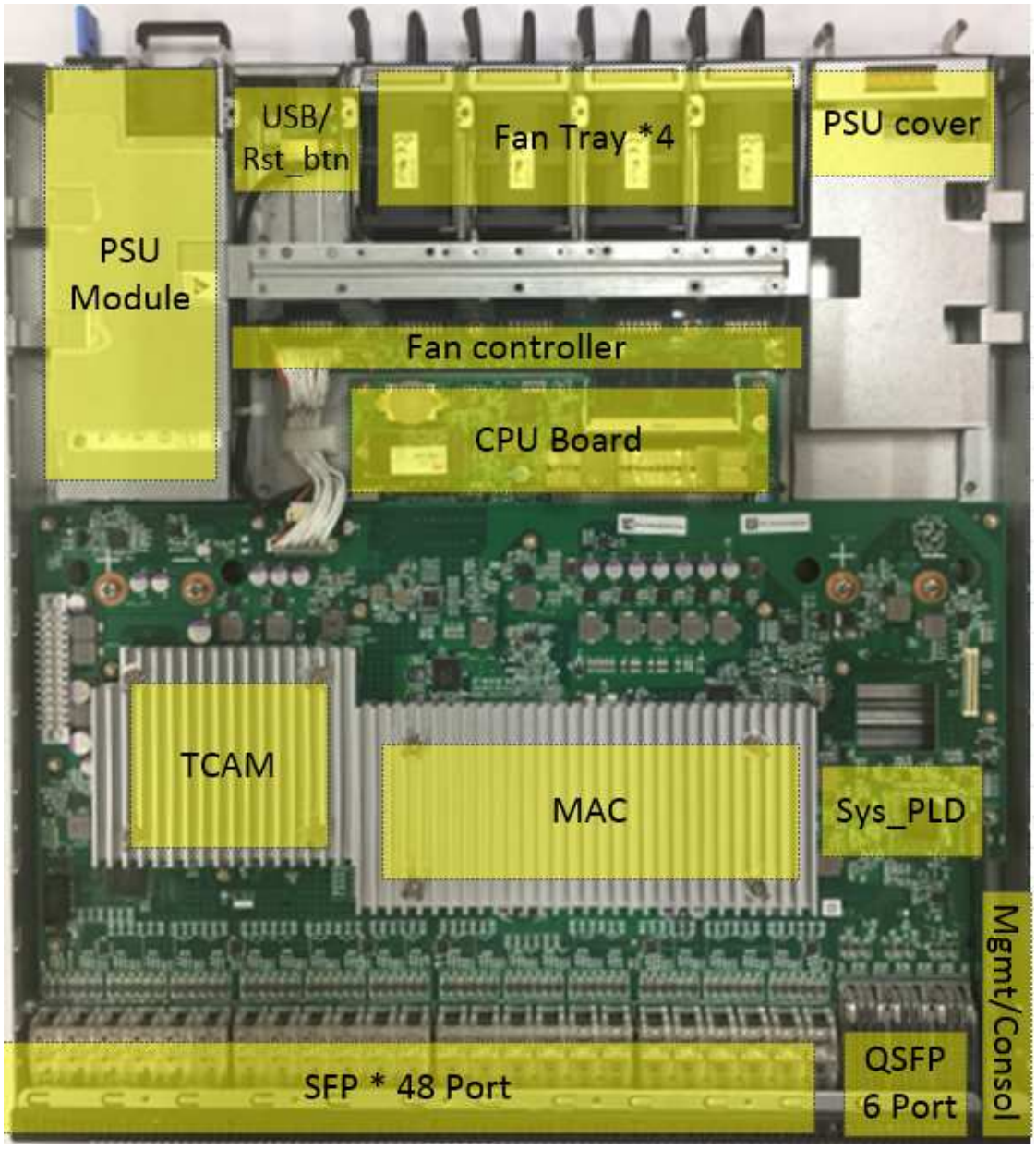


Figure 1: 48 x 10G SFP+ and 6 x 40G/100G QSFP, Block diagram

3.1. Physical Dimensions

440 x 496 x 44 mm (W x D x H)

17.32 x 19.52 x 1.73 inch



4. CPU / MAC PHY/ KBP subsystem

4.1.1. **CPU Block Diagram**

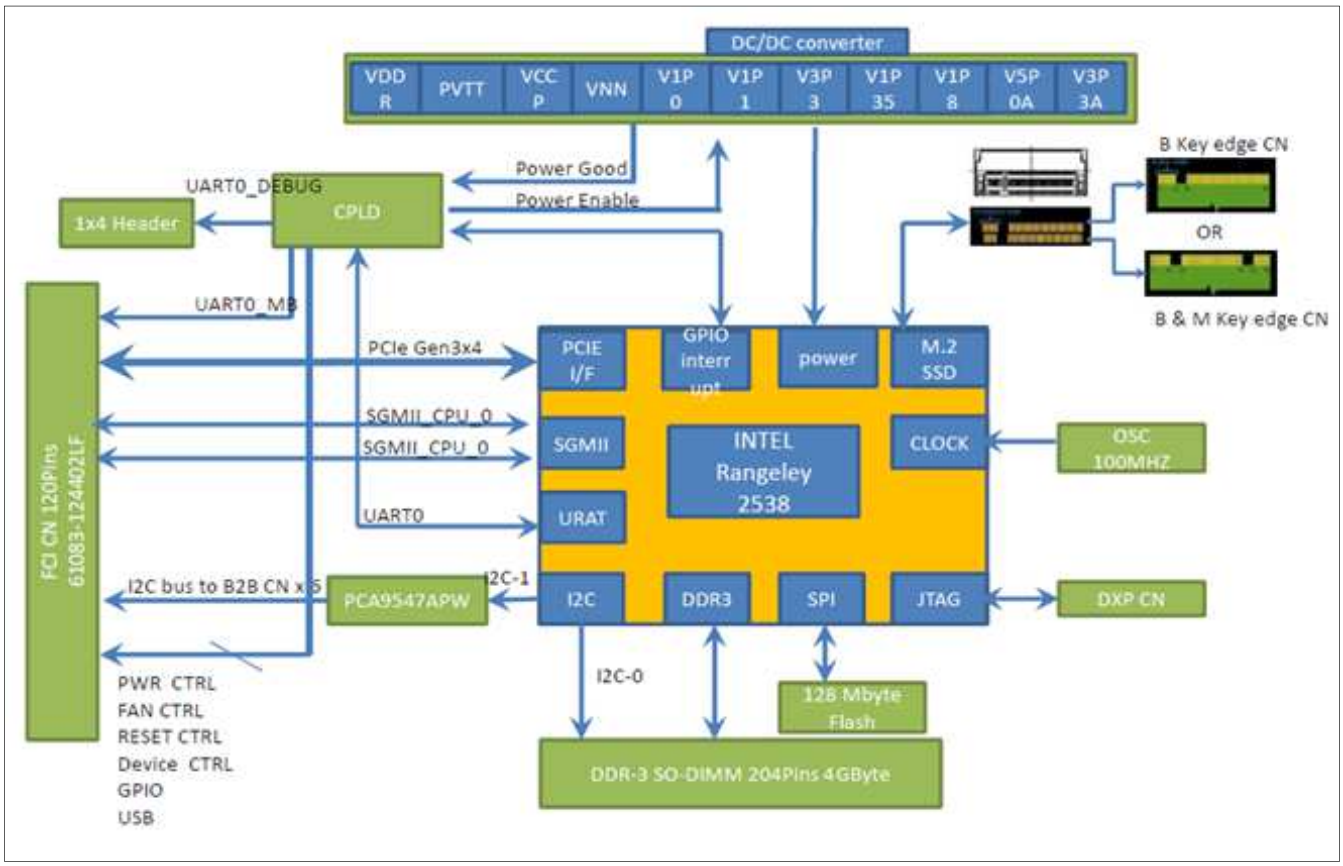


Figure 2: C2538, CPU board Block Diagram

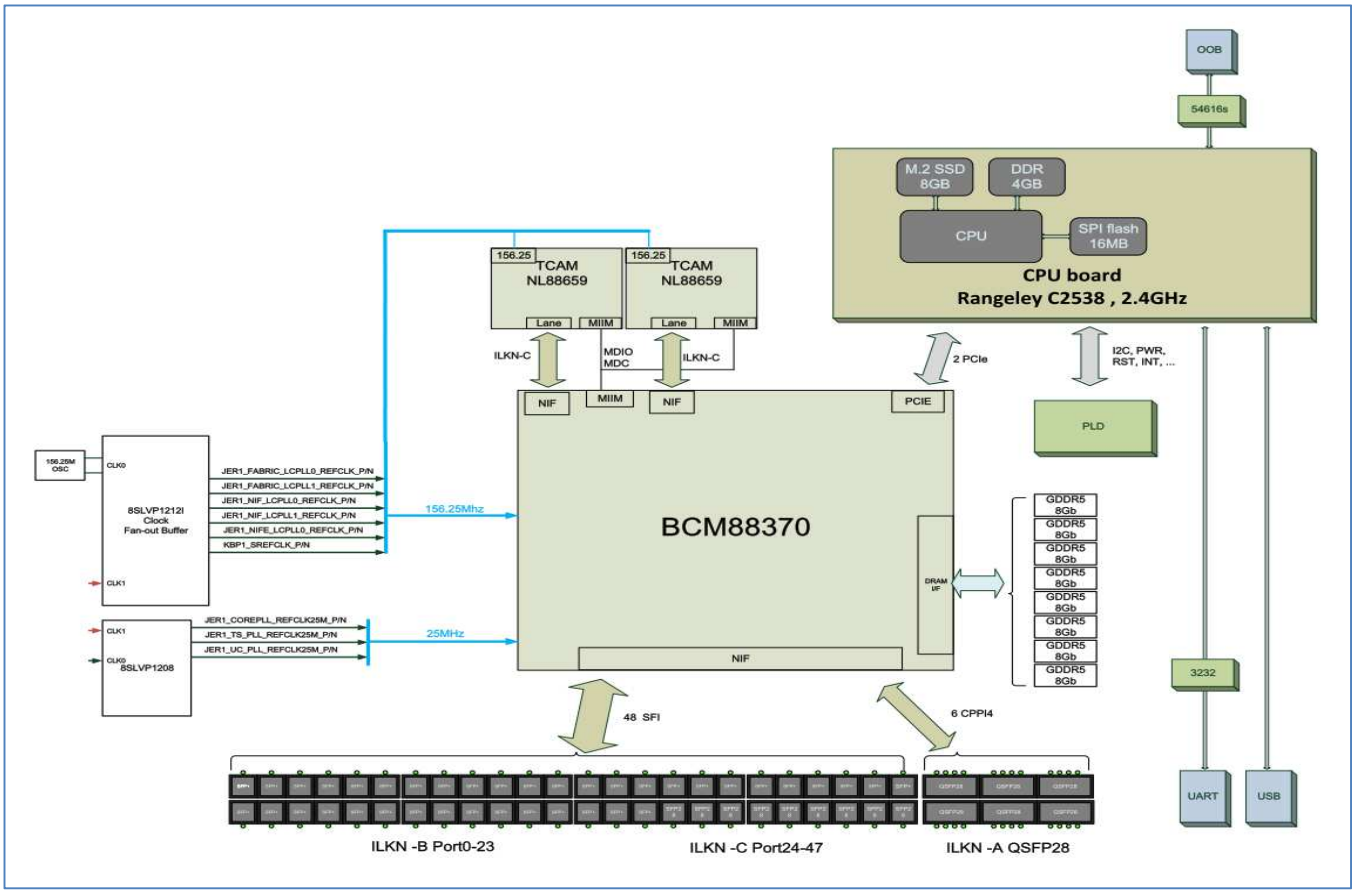
Switch Subsystem – BCM88375

4.1.2. Switch Engine

The Broadcom® BCM88375 family is a class of high-performance, high-connectivity network switching devices.

There are total of 72 SerDes including 24 SerDes with rate up to 25.78125 Gbps and 48 SerDes with rate up to 12.5Gbps.

- 24 SerDes with rates up to 25.78125 Gb/s each, supporting the following protocol blocks:
  - Interlaken: Two Interlaken interface up to 12 lanes, or a single Interlaken interface up to 24 lanes.
  - 24 * 10GbE, over XFI
  - 12 * 40GbE, over XLAUI-2/XLAUI
  - 6 * 100GbE, over CAUI-4 4-lane.
- 48 SerDes with rates up to 12.5 Gb/s each, supporting the following protocol blocks:
  - Interlaken: Four Interlaken interface up to 12-lane, or two Interlaken interface up to 24-lane.
  - 64 * GbE , over QSGMII(only 16 SerDes out of the 48 supports QSGMII)
  - 72 * GbE, over SGMII
  - 48 * 10 GbE, over XFI/XAUI /RXAUI.
  - 12 * 40 GbE, over XLAUI 4-lane.



KBP Subsystem – NL88659

NL88659

4.1.3. Knowledge Based Processor Engine

This family of KBPs addressed next-generation classification needs through high performance, parallel decisions and improved entry storage capabilities. Up to 4 parallel operations allow the device to reach decision speeds of up to 2.0 Billion Decisions Per Second (BDPS). Embedded Error Correction Circuitry (ECC) improves system testability and operational reliability. The key processor unit (KPU) and the context buffer enable efficient interface transfers with flexible search key construction.

4.1.4. General Feature of KBP

- Dual Port enable two hosts to connect on KBP
- Device available in 2048K/1024K/512K 40b database entries.
- KBP table width configurable as 80/160/320/640 bits.
- User Data Array for associated data, width configurable as 32/64/128/256 bits.
- Context Buffer organized as 4096 x 640b.
- 4 parallel compares enable up to 4 results per operation.

4.1.5. Architecture Overview of KBP

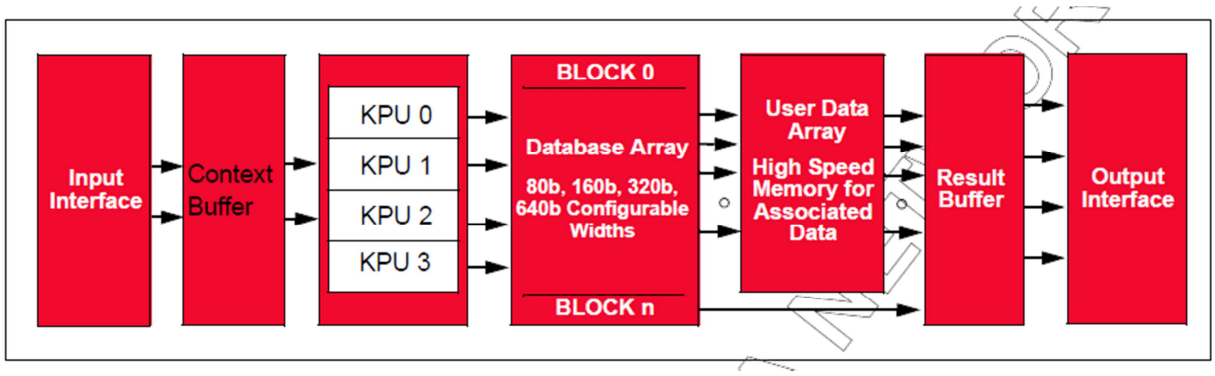


Figure 12: Architecture of KBP

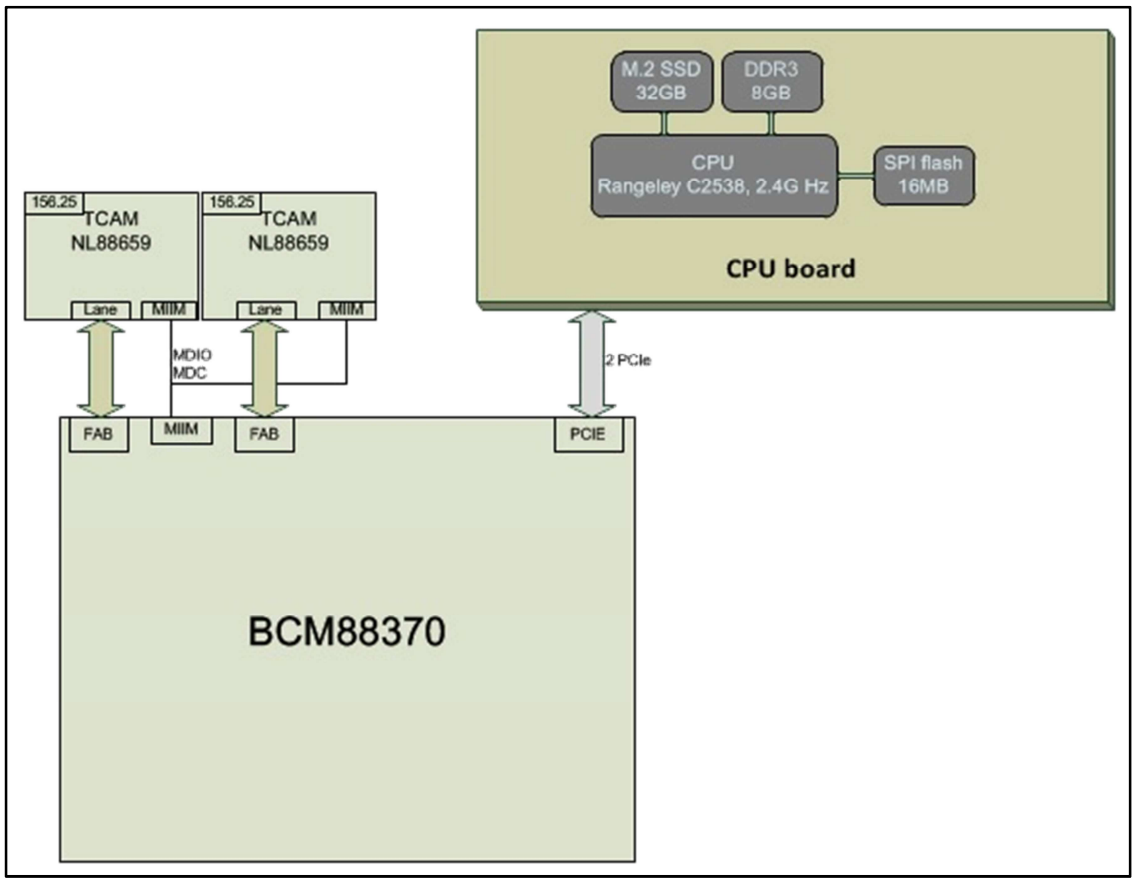


Figure 13: KBP Block Diagram

5. FAN Subsystem

System FAN tray speed control

The FAN system supports fan speed control for different environment temperature workable. EMC2305 is a Multiple RPM-Based PWM FAN Controller for 4 Fans. There are two “EMC2305” on board for fan speed controller.

FAN Connection Diagram

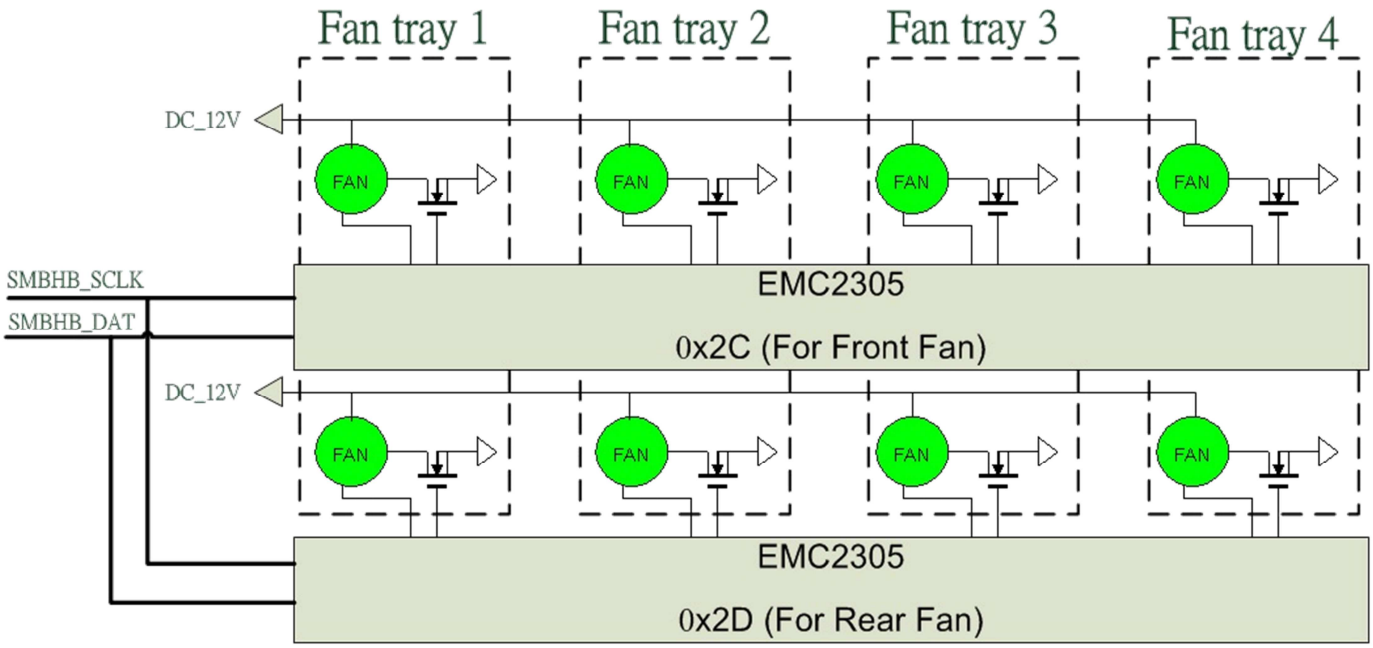


Figure 3: FAN unit, Block Diagram

The EMC2305 is selected on Fan Speed Control Mode for operation.

The thermal *shutdown* implementation on P2 Stage .

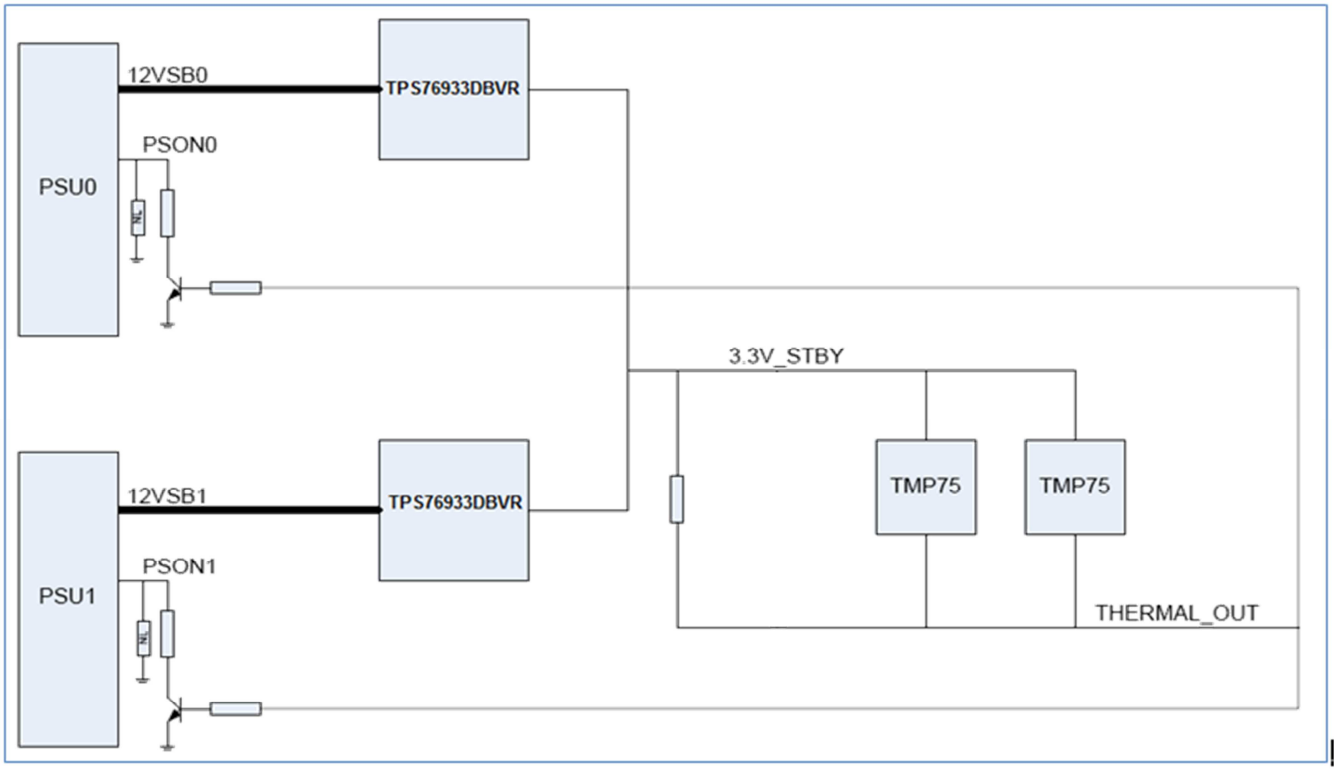


Figure 4: Thermal *shutdown* implementation on P2 Stage

PSU FAN speed control

There is an internal FAN at 800W PSU. The FAN speed rate is 23,000rpm maximum. And PSU's FAN control function is defined on PMBUS protocol by I2C control. The below chart is for example of command to use this protocol from PMBUS user's guide.

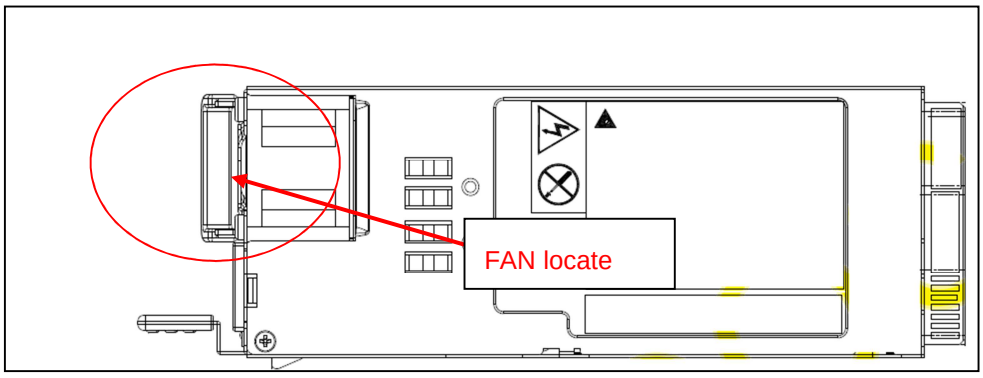


Figure 5: FAN on PSU

LED

5.1.1. **System, Management, PSU LED**

Feature	Description	Comment
Power LED	**Solid Green** – Power Supply is supplied to the switch & operating normally **Solid Amber** – POST in progress. **Off** – Power is Disconnected.	Front
System LED	**Off** – No Power **Blinking Green** – Booting, or System in Diagnostic mode **Solid Green** – Normal operation **Solid Amber** – Critical Alarm **Blinking Amber** – Non-critical Alarm	Front
FAN Status LED	**Green** – FAN operating normally. **Amber** – FAN failed.	Front
1 RJ-45 port *One LED /port*	**Link/ACT LED:** **Off** –No link is established on the port. **Orange** - A valid link at 10/100Mbps is established on the port. **Solid Green** – A valid link at 1000Mbps is established on the port.	Front
PSU LED	**Solid gree**n –AC input OK. **OFF**– NO AC input.	Rear
FAN Status LED	**Green** – FAN operating normally. **Red** – FAN failed.	Rear

Table 2: System LED

5.1.2. SFP+ 10G & QSFP28 40G/100G LED

The Fiber port LEDs was decoding by BCM88375 LED interface for 10G/40G/100G ports. This chapter defined speed and Link/Activity, breakout status LED signals from BCM88375 LED shift out.

BCM88375 provides three two-wire LED interface and can be applied for TTL shift register IC to indicate system LEDs.

Feature	Description	Comment
LED_CLK_A/DATA_A	The LEDs of QSFP28 Port 1 – 6	From MAC
LED_CLK_B/DATA_B	The LEDs of SFP+ Port 1 – 24	
LED_CLK_C/DATA_C	The LEDs of SFP+ Port 25 – 48	

SFP+ LED Indication

Feature	Description	Comment
LED1	**OFF**: No Link **Blinking Green**: Packet transmission or reception is occurring.	Bottom side SFP+ Port
LED2	**OFF: No Link** **Blinking Green: Packet transmission or reception is occurring.**	Top side SFP+ Port
LED3	**OFF: No Link** **Solid Green: A valid 10G link is established on the port.** **Solid Amber: A valid 1G link is established on the port.**	Bottom side SFP+ Port
LED4	**OFF: No Link** **Solid Green: A valid 10G link is established on the port.** **Solid Amber: A valid 1G link is established on the port.**	Top side SFP+ Port

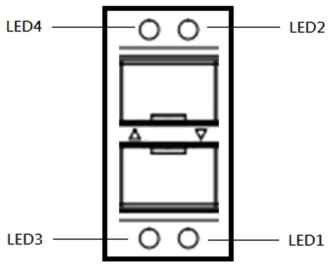


Figure 6: SFP+ LED Indication

QSFP28 LED Indication

Feature	Description	Comment
LED1	**(Solid Lighting – Linkup; Blinking – Activity)** **Green** – 100G Operation **White** – 50G Operation **Amber** – 40G Operation **Blue** – 25G Operation **Purple** – 10G Operation **Off** – No Link	At front side

LED2	*Working in breakout cable 1 to 4 Pairs only.* **(Solid Lighting – Linkup; Blinking – Activity)** **Blue** – 25G Operation **Purple** – 10G Operation **Off** – No Link	At front side
LED3	*Working in breakout cable 1 to 4 Pairs only.* **(Solid Lighting – Linkup; Blinking – Activity)** **White –** 50G Operation **Blue** – 25G Operation **Purple** – 10G Operation **Off** – No Link	At front side
LED4	*Working in breakout cable 1 to 4 Pairs only.* **(Solid Lighting – Linkup; Blinking – Activity)** **Blue** – 25G Operation **Purple** – 10G Operation **Off** – No Link	At front side

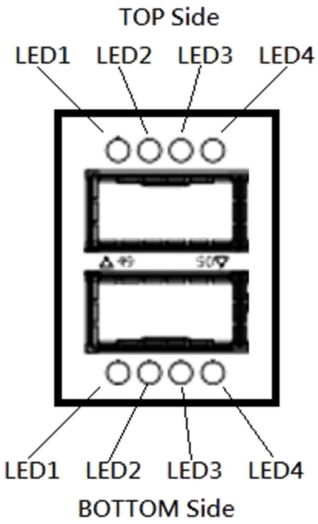
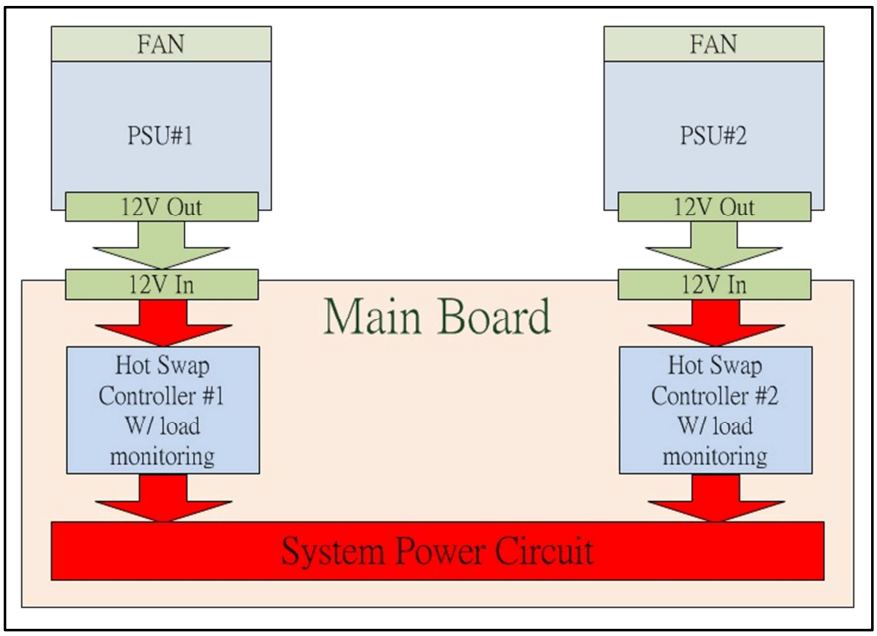


Figure 7: QSFP28 LED Indication

Power Management

The system has two Hot Swap control ICs (LTC4215) to protect PSU be safely inserted or removed.

The LTC4215 Hot Swap controller using an external N-channel pass transistor, board supply voltage and inrush current are ramped up at an adjustable rate. Also it provides the I2C bus and interrupt function for system.



Current Monitoring

The LTC4215 incorporates an 8-bit A/D converter that continuously monitors three different voltages. The SOURCE pin has a 1/12.5 resistive divider to monitor a full scale voltage of 15.4V with 60mV resolution. The ADIN pin is monitored with a 1.235V full scale and 4.82mV resolution, and the voltage between the VDD and SENSE pins is monitored with a 38.45mV full scale and 151µV resolution. Results from each conversion are stored in registers E (Sense), F (Source) and G (ADIN), as seen in Tables 6, and are updated 10 times per second. It can calculate the current to get the power consumption.

6. Software Support

AGC7648A support ONIE.

7. Technical Specs and Environmental Requirements

Technical Specifications

Network Protocol and Standards Compatibility

IEEE802.3 CSMA/CD

IEEE802.3u 100BaseTx

IEEE802.3z 1000BaseSX

IEEE802.3z/ab 1000BaseT

IEEE802.3ae 10Gbit/s

IEEE802.3by 25Gbit/s

IEEE802.3bj/bm 100Gbit/s

SFF-8431

SFF-8079

IEEE802.3x flow control

Interface

USB connector (USB to DB9)

Physical Dimensions

440 x 493 x 44 mm (W x D x H)

17.32 x 19.24 x 1.73 inch

Electromagnetic Emission

- FCC Class A, CE Class A, VCCI Class A

Safety Agency approval

- UL, CUL

~ end of document ~