Revision History	Date
0.1	
0.2 1. Change U3 from MS08 packet to SO8 packet. 2. Add Resister R7708,R7709,R7710,R7711	

Page Descriptions

Note:

1.All of resistors are 5%, 0603 SMD except other specified description.
2.All of capacitors are 50V except other specified description.
3.All of aluminous capacitors are 105 degree C except other specified description.
4. # for LOW active signals(name#)

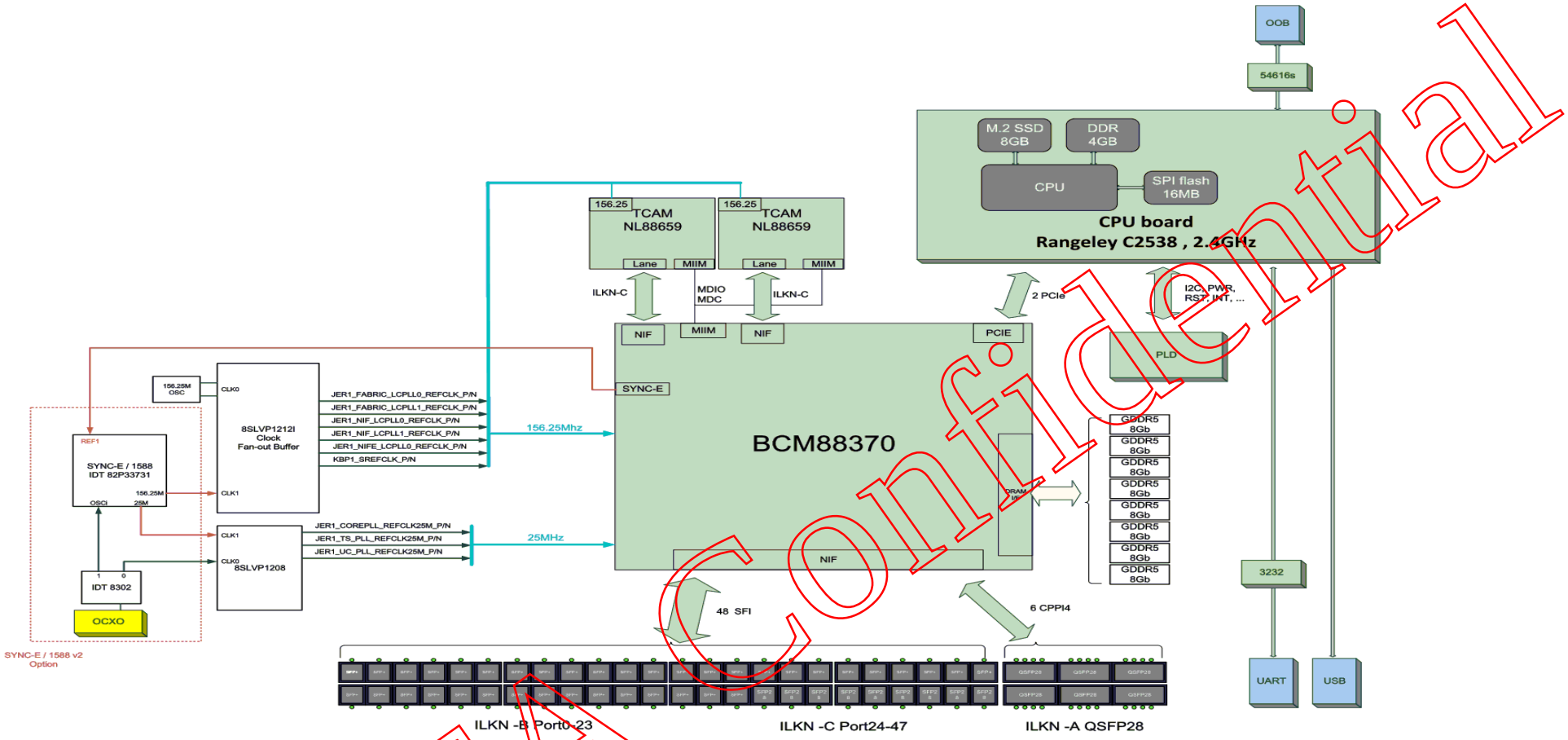
SCHEMATICS OF	FILE NAME	DRAWN	DESIGNED	CHECKED	APPROVED	DELTA ELECTRONICS, INC.
ET-7648BCRC-R	ET-7648BFRC_MB	SAMUEL.FU	SAMUEL.FU	SAMUEL.FU	COOPER.LEE	

Title: 01. Root

Size: C | Document Number: 1ADSS-0XXXXX | Rev: 0.1

Date: Thursday, May 17, 2018 | Sheet 1 of 53

Block diagram:



Power Comsuption:

ET7648BFRB

Device	Qty	Current per each Voltage Rail									Total per each Voltage Rail									Subtotal
		0.9V	AVS 1V	1.2	1.25V	1.35V	1.8V	3.3V	5V	12V	0.9	1.00	1.20	1.25	1.35	1.80	3.30	5.00	12.00	
CPU Board, Rangeley (4core)	1									3,290							0	0	3,290	39.48
BCM88370	1	0	102,744		192	385	135	195		0	0	102,744	0	192	385	135	195	0	0	104.15
NL88659	2	56,170	0		0		477	0	0		112,340	0		0		954	0	0	0	102.82
BCM54616	1			310	0			240	0		0	0	310	0			240	0	0	0.79
DDR5 EDY4016AABG-JD	8					850			0	0	0	0		0	6,800		0	0	0	9.18
USB Port	1								900		0	0		0	0	0	0	900	0	4.50
10G SFP	48							456			0	0		0			21,888		0	72.23
zQSFP+ (5W)	6							1,520	0		0						9,120			30.10
LED	104								10		0	0		0			0	1,040	0	5.20
FAN	4									1,820	0	0		0			0	0	7,280	87.36
Other(ICs, OSCs,...)	1							1,000			0	0		0			1,000	0	0	3.30
Load Total Current per Voltage [A]:											112.34	102.744	0.31	0.19	7.19	1.09	32.44	1.94	10.57	
Load Power Dissipation per Voltage [W]:											101.11	102.74	0.37	0.24	9.70	1.96	107.06	9.70	126.84	459.72
DCDC Loss (85%)											17.84	18.13	0.07	0.04	1.71	0.35	18.89	1.71	22.38	81.12
PWM Input [W]											118.95	120.87	0.44	0.28	11.41	2.31	125.95	11.41	149.22	540.84
Total power comsuption (include efficiency of PWM) [W]:											540.84									

Title: 02. BLOCK_DIAGRAM

Size: C | Document Number: 1ADSS-0XXXXX | Rev: 0.1

Date: Thursday, May 17, 2018 | Sheet 2 of 53

Power Sequence:

PSU	12V 12V_STB

→

VCC_3V_A	IR3846
VCC_3V_B	IR3846
VCC_1V2	APL5930KAI-TRG
VCC_2V5_B	AMS1117-ADJ

↓

VCC_5V	MPQ8632GL-12

↓

VDD_0V9	IR3595
VCCA_0V9	MPQ8632GL-12
VDDS_0V9	APL5930KAI-TRG

↓

VCC_1V8	MPQ8632GL-12

↓

VDDC_1V	IR3595

↓

VCCTR_1V	IR3846

↓

VCC_1V35	MPQ8632GVE-20-Z

↓

VCC_1V25	MPQ8632GL-12

Clock Tree:

25MHz:

FD2500048 (Y2) — 651MLFT (U47)

BCM88375 (U2):SYS_CLOCK25M
5M1270ZF256 (U134):CPLD_25M_CLK_A
5M1270ZF256 (U215):CPLD_25M_CLK_B

25MHz Diff:

OSC713500 (Y3) — ICS8535AGI (U48)

BCM88375 (U2):COREPLL_REFCLK25M_C_P
COREPLL_REFCLK25M_C_N
BCM88375 (U2):JER_TS_PLL_REFCLK25M_P
JER_TS_PLL_REFCLK25M_N
BCM88375 (U2):JER_UC_PLL_REFCLK25M_P
JER_UC_PLL_REFCLK25M_N

100MHz Diff:

XTL571150-G47 (Y4) — NB3N51034DTR2G (U49)

BCM88375 (U2):JER_DDR_AB_PLL_REFCLK_P
JER_DDR_AB_PLL_REFCLK_N
BCM88375 (U2):JER_DDR_CD_PLL_REFCLK_P
JER_DDR_CD_PLL_REFCLK_N
BCM88375 (U2):JER_DDR_EF_PLL_REFCLK_P
JER_DDR_EF_PLL_REFCLK_N
BCM88375 (U2):JER_DDR_GH_PLL_REFCLK_P
JER_DDR_GH_PLL_REFCLK_N

100MHz PCIE:

PDA000009J (Y9)

BCM88375 (U2):PCIE_REFCLK_P
PCIE_REFCLK_N

156.25MHz Diff (NIF/NIFE/FABRIC):

PBF620038J (Y11) — 853S111BYILFT (U246)

BCM88375 (U2):JER_NIFE_LCPLL1_REFCLK_P
JER_NIFE_LCPLL1_REFCLK_N
BCM88375 (U2):JER_FABRIC_LCPLL1_REFCLK_P
JER_FABRIC_LCPLL1_REFCLK_N
BCM88375 (U2):JER_FABRIC_LCPLL0_REFCLK_P
JER_FABRIC_LCPLL0_REFCLK_N
BCM88375 (U2):JER_NIF_LCPLL_REFCLK_P
JER_NIF_LCPLL_REFCLK_N
BCM88375 (U2):JER_NIFE_LCPLL0_REFCLK_P
JER_NIFE_LCPLL0_REFCLK_N

156.25MHz Diff (KBP1/KBP2):

PBF620038J (Y11) — 853S111BYILFT (U246)

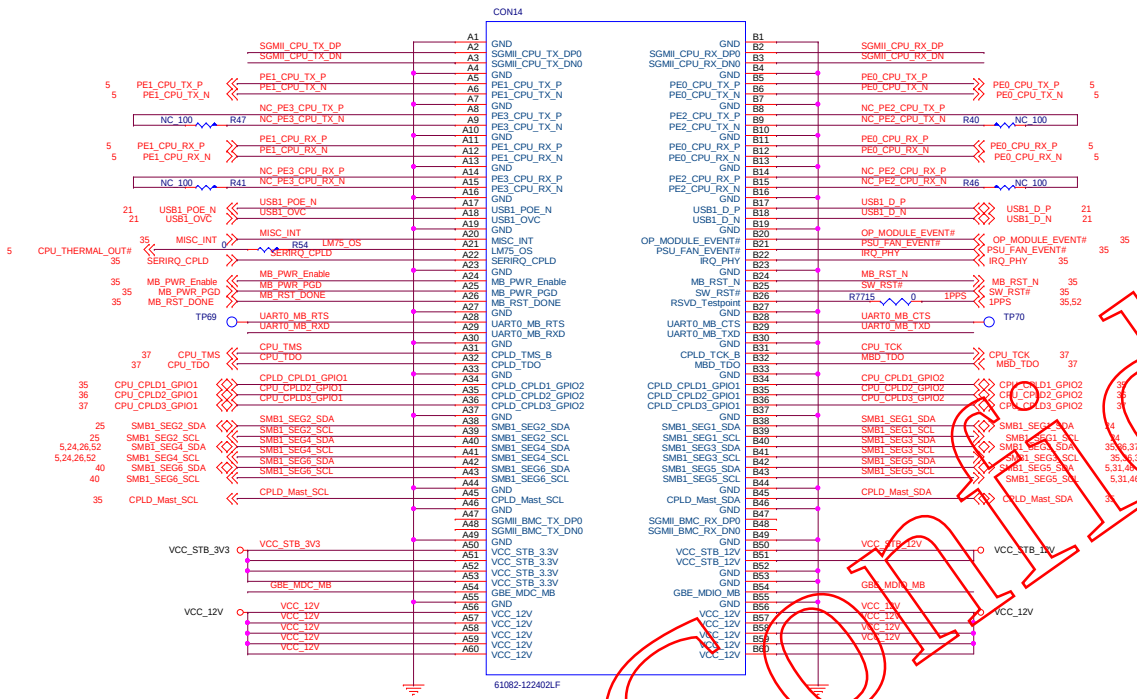
NL88659 (U1):KBP1_RCLK_P
KBP1_RCLK_N
NL88659 (U1):KBP1_CORECLK_P
KBP1_CORECLK_N
NL88659 (U1):KBP1_CASCLK_P
KBP1_CASCLK_N
NL88659 (U19):KBP2_RCLK_P
KBP2_RCLK_N
NL88659 (U19):KBP2_CASCLK_P
KBP2_CASCLK_N
NL88659 (U19):KBP2_CORECLK_P
KBP2_CORECLK_N

DELTA ELECTRONICS, INC.

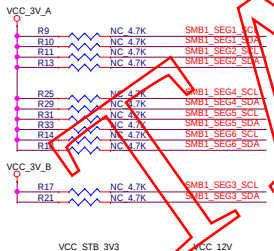
Title: 03. Power Consumption

Size: C | Document Number: 1ADSS-0XXXXX | Rev: 0.1

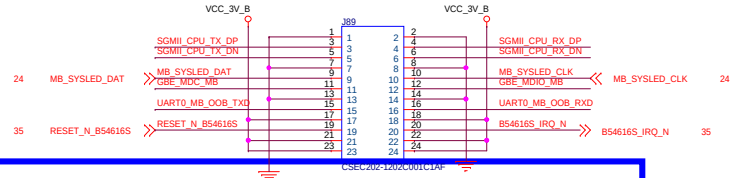
Date: Thursday, May 17, 2018 | Sheet 3 of 53

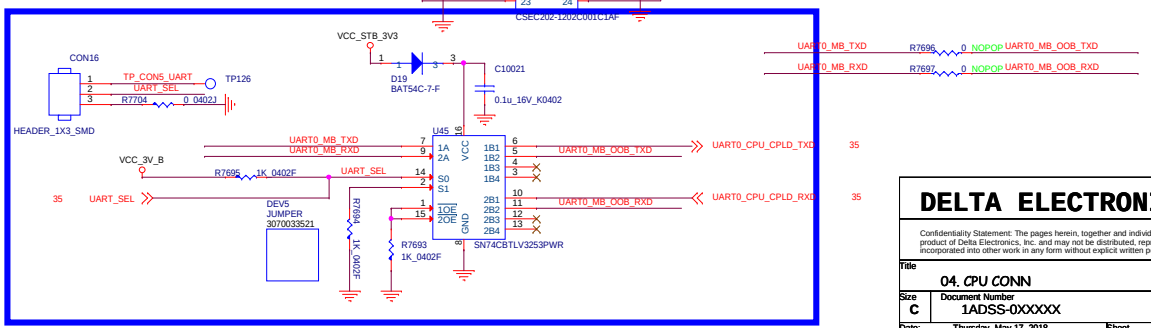


DESIGN NOTE !!!
Pull-high CPU to MB I2C bus



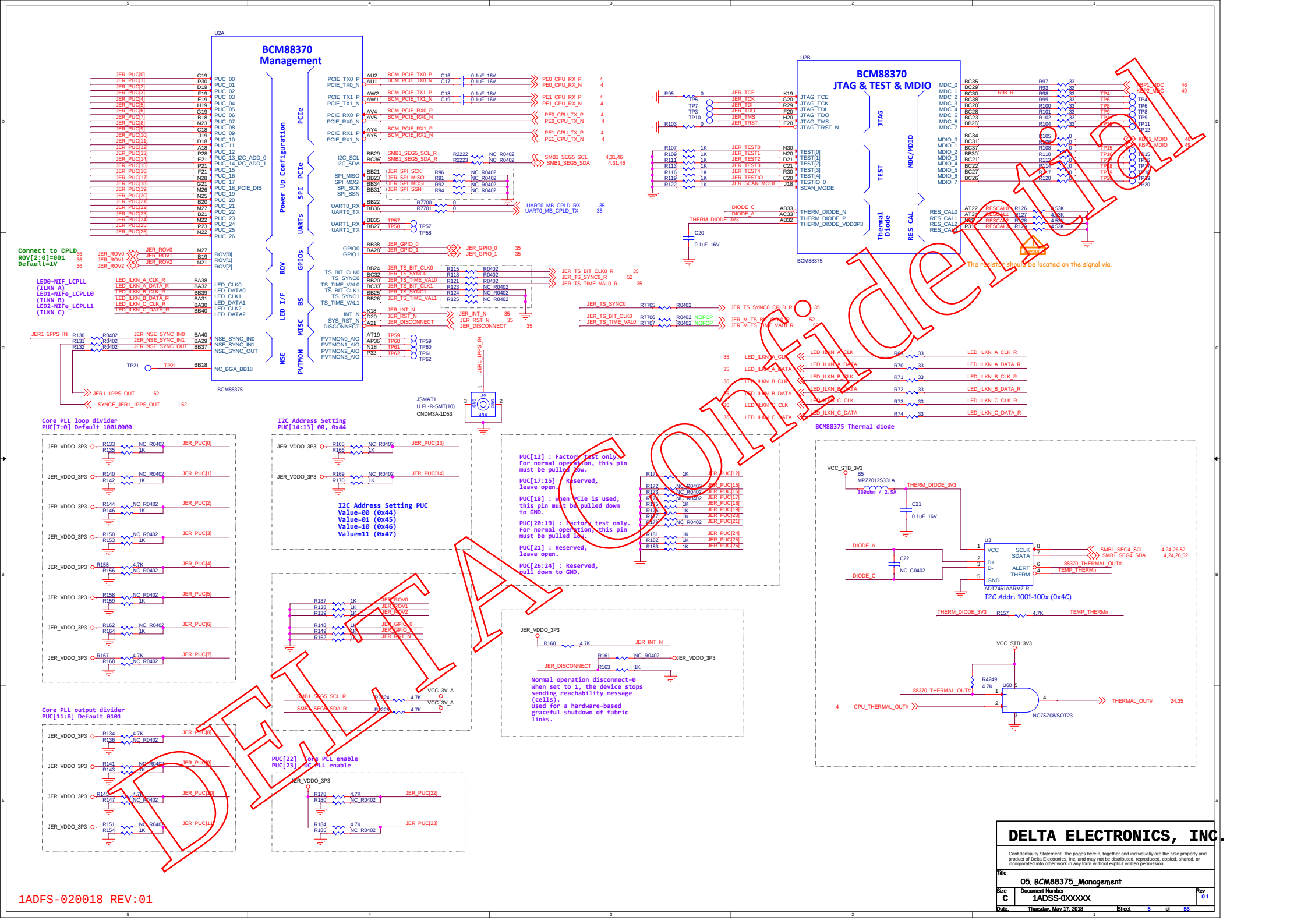
OOB and Console Connector





DELTA ELECTRONICS, INC.

Title	04. CPU CONN	
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 4 of 53	


BCM88370 Management
BCM88370 JTAG & TEST & MDIO
Power Up Configuration
PCIe
SPI
UARTs
GPIOs
LED I/F
BS
MISC
NSE
PVTMON
JTAG
TEST
MDC/MDIO
Thermal Diode
RES CAL
Connect to CPLD
ROV[2:0]=001
Default=1V
LED0-NIF_LCPLL (ILKN A)
LED1-NIF_LCPLL0 (ILKN B)
LED2-NIfe_LCPLL1 (ILKN C)
Core PLL loop divider
PUC[7:0] Default 10010000
I2C Address Setting
PUC[14:13] 00, 0x44
I2C Address Setting PUC
Value=00 (0x44)
Value=01 (0x45)
Value=10 (0x46)
Value=11 (0x47)
PUC[12] : Factory test only. For normal operation, this pin must be pulled low.
PUC[17:15] : Reserved, leave open.
PUC[18] : When PCIe is used, this pin must be pulled down to GND.
PUC[20:19] : Factory test only. For normal operation, this pin must be pulled low.
PUC[21] : Reserved, leave open.
PUC[26:24] : Reserved, pull down to GND.
BCM88375 Thermal diode
ADT7461AARMZ-R
I2C Addr: 1001-100x (0x4C)
Core PLL output divider
PUC[11:8] Default 0101
PUC[22] Core PLL enable
PUC[23] DC PLL enable
Normal operation disconnect=0
When set to 1, the device stops sending reachability message (cells).
Used for a hardware-based graceful shutdown of fabric links.
DELTA Confidential
DELTA ELECTRONICS, INC.
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.
Title
05. BCM88375_Management
Size C
Document Number 1ADSS-0XXXXX
Rev 0.1
Date: Thursday, May 17, 2018
Sheet 5 of 53
1ADFS-020018 REV:01

CLOCK25 Reference Clock

The CLOCK25 is a CMOS 3.3V input. The required voltage levels are specified in Table 16 "DC Specifications for CMOS 3.3V I/O," on page 123.

Table 41: CLOCK25 Specifications

Parameters	Symbol	Conditions	Min	Typ	Max	Unit
Reference Clock Frequency	F_{REF}	–	–	25	–	MHz
Reference Clock Accuracy	ACC_{REF}	–	-100	–	+100	ppm
Duty Cycle	F_{DC}	–	40	–	60	%
Rise/Fall time	T_R/T_F	20%–80%	–	–	4.0	ns
Input peak-to-peak Jitter	J_{IN}	–	–	–	100	ps

Core/UC PLL Reference Clocks

The Core PLL and UC PLL use the same type of LCPLL and share the same clock requirements. Table 42 lists the specifications of the Core/UC reference clocks.

Table 42: Core/UC LCPLL Reference Clock Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Reference Clock frequency	F_{REF}	–	25	–	MHz
Reference clock accuracy[a]	ACC_{REF}	–25	–	+25	PPM
Duty Cycle	F_{DC}	40	–	60	%
Input differential swing[b]	$V_{IN-DIFF}$	500	–	2000	mVppd
Differential input termination	R_{TERM}	–	100	–	Ω
Rise/fall time (10%–90%)	T_R / T_F	–	–	1[c]	nsec/Vppd
Input Jitter (RMS)[d]	J_{IN}	–	–	1	psec

DRAM Reference Clocks

There are eight DRAM interfaces. Each DRAM interface is composed of 32 data bits and supports DDR4 and GDDR5. There are four DRAM reference clocks—one clock for every two interfaces. This reference clock drives the DRAM internal PLL which generates the required frequency to match the interface data rate. All four DRAM reference clocks share the same requirements. Table 44 lists the specifications of the DRAM reference clock.

Table 44: DRAM Reference Clock Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Reference Clock frequency	F_{REF}	–	100	–	MHz
Reference clock accuracy	ACC_{REF}	-100	-	+100	PPM
Duty Cycle	F_{DC}	40	–	60	%
Input differential swing[a]	$V_{IN-DIFF}$	800	–	1600	mVppd
Rise/fall time (10% - 90%)	T_R / T_F	–	0.1	0.2	nsec
Input Jitter (RMS)[b]	J_{IN}	–	–	1	psec

Fabric and NIF SerDes Reference Clocks

All SerDes use the same type of LCPLL and share the same clock requirements. Table 45 lists the specifications of the SerDes (Fabric, NIF, NIFe) LCPLL reference clock.

Table 45: SerDes LCPLL Reference Clock Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Reference Clock frequency	F_{REF}	–	125/156.25	160	MHz
Reference clock accuracy	ACC_{REF}	–25	–	+25	PPM
Duty Cycle	F_{DC}	40	–	60	%
Input differential swing[a]	$V_{IN-DIFF}$	500	–	2000	mVppd
Differential input termination	R_{TERM}	–	100	–	Ω
Rise/fall time(10% - 90%)	T_R/T_F	–	–	1[b]	nsec/Vppd
Input Jitter (RMS)[c]	J_{IN}	–	–	0.3	psec

TS PLL Reference Clock

Table 43 lists the specifications of the TS PLL reference clock.

Table 43: TS PLL Reference Clock Specifications

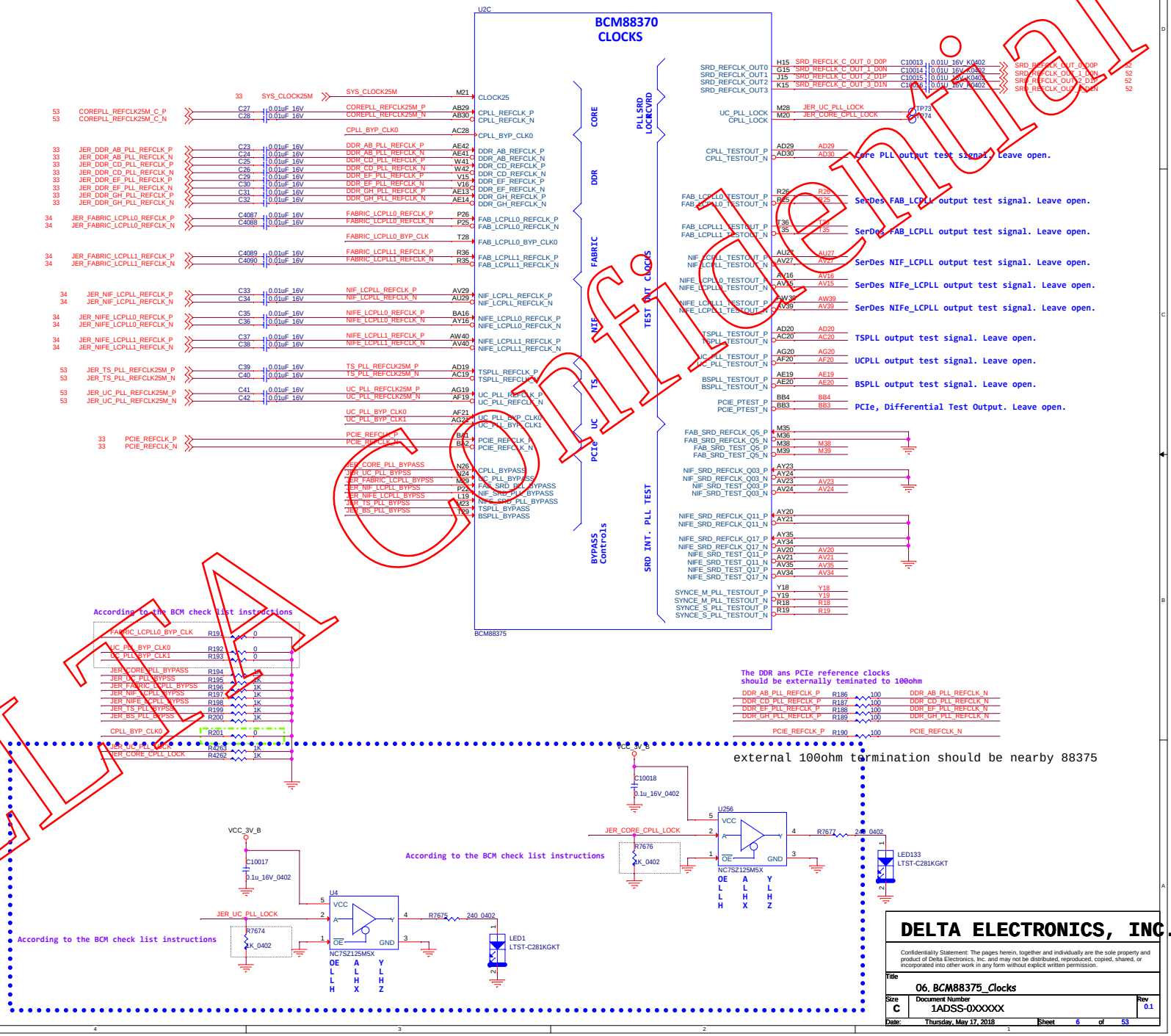
Parameter	Symbol	Min	Typ	Max	Unit
Reference Clock frequency	F_{REF}	–	25	–	MHz
Reference clock accuracy	ACC_{REF}	–100	–	+100	PPM
Duty Cycle	F_{DC}	40	–	60	%
Input differential swing[a]	$V_{IN-DIFF}$	500	–	2000	mVppd
Differential input termination	R_{TERM}	–	100	–	Ω
Rise/fall time (10%–90%)	T_R / T_F	–	–	1[b]	nsec/Vppd
Input Jitter (RMS)[c]	J_{IN}	–	–	30	psec

PCIe PLL Reference Clock

Table 40 lists the specifications of the PCIe PLL reference clock.

Table 40: PCIe PLL Reference Clock Specifications

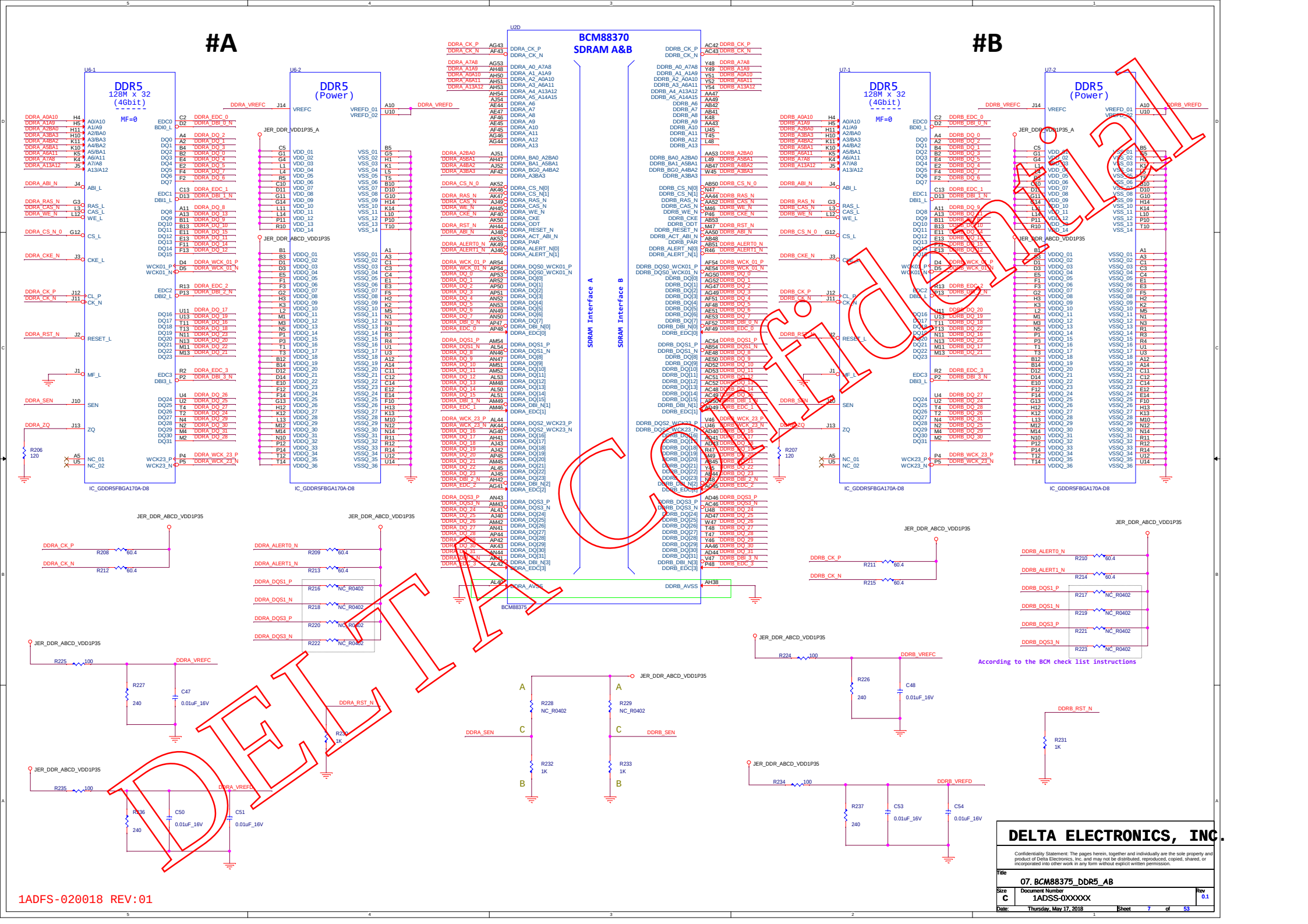
Parameter	Symbol	Min	Typ	Max	Unit
Reference clock frequency	F_{REF}	–	100	–	MHz
Reference clock offset	ACC_{REF}	–300	–	+300	PPM
Reference duty cycle	F_{DC}	40	–	60	%
Reference clock Common Mode	V_{IN-CM}	–	0.5	–	V
Input differential swing[a]	$V_{IN-DIFF}$	300	–	1600	mVppd
Rise/fall time (20% – 80%)	T_R/T_F	–	–	500	psec
Reference clock jitter (RMS)[b]	J_{IN}	–	–	3	psec
Reference clock jitter (RMS)[c]	J_{IN}	–	–	3.1	psec

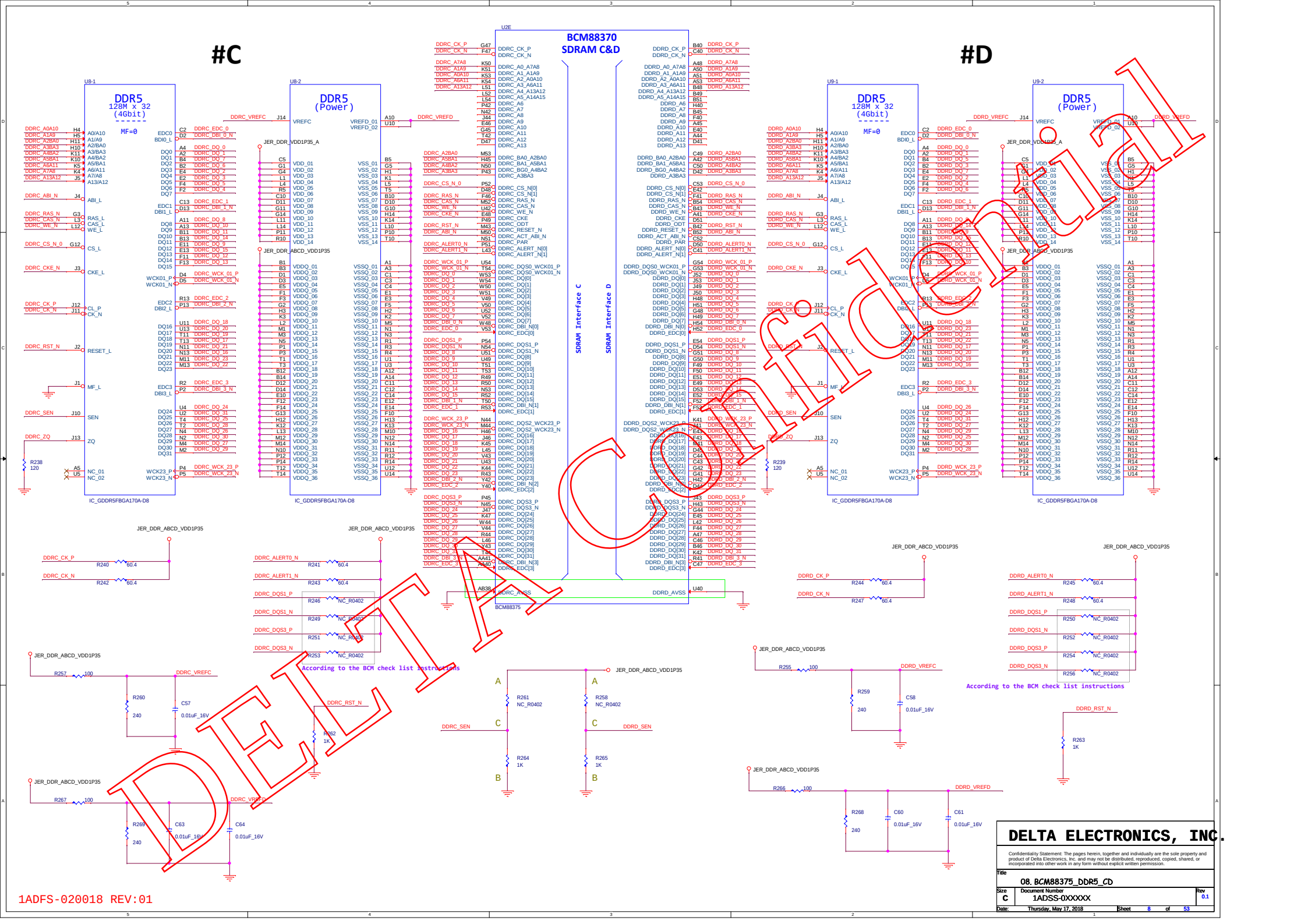


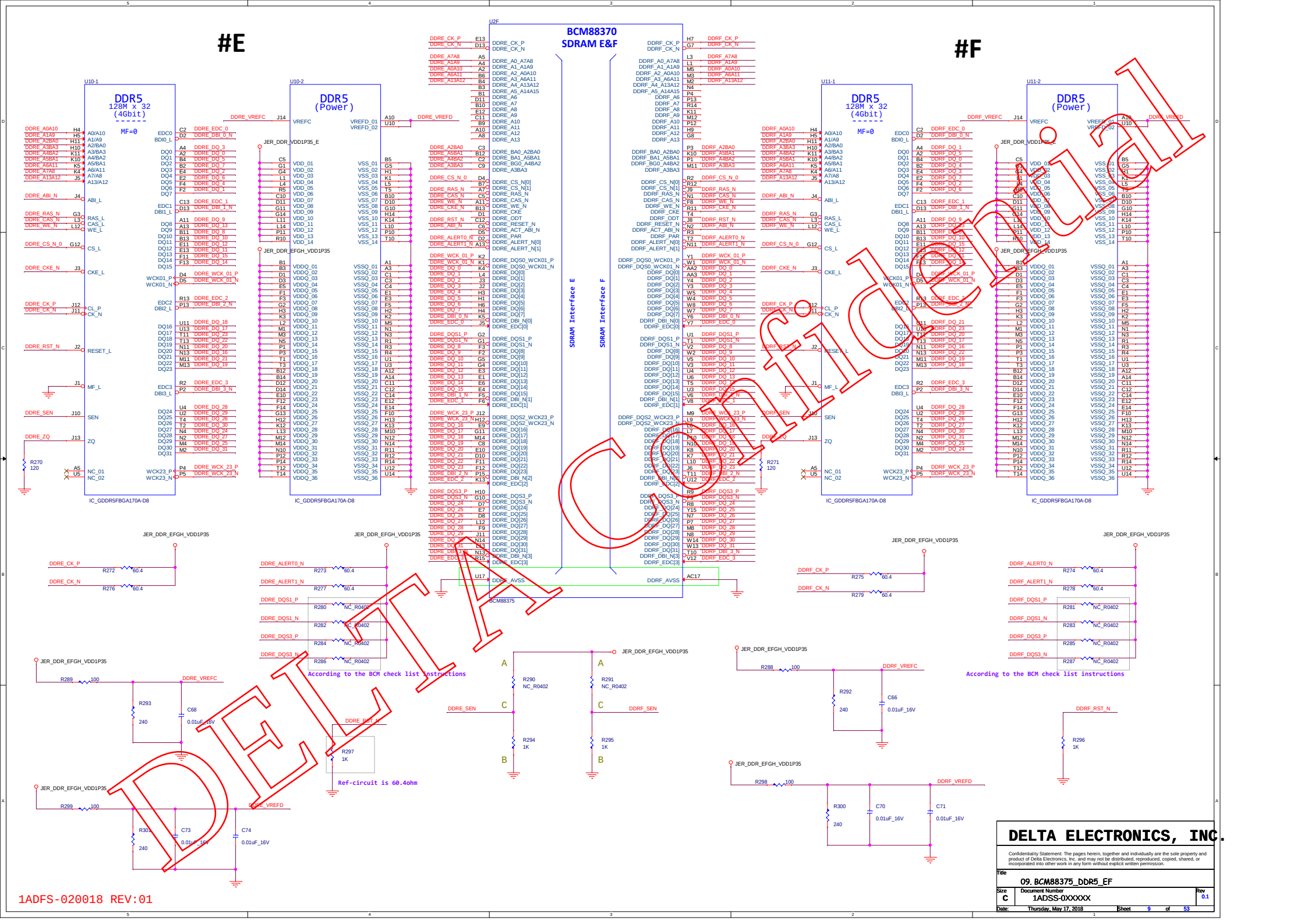
1ADFS-020018 REV:01

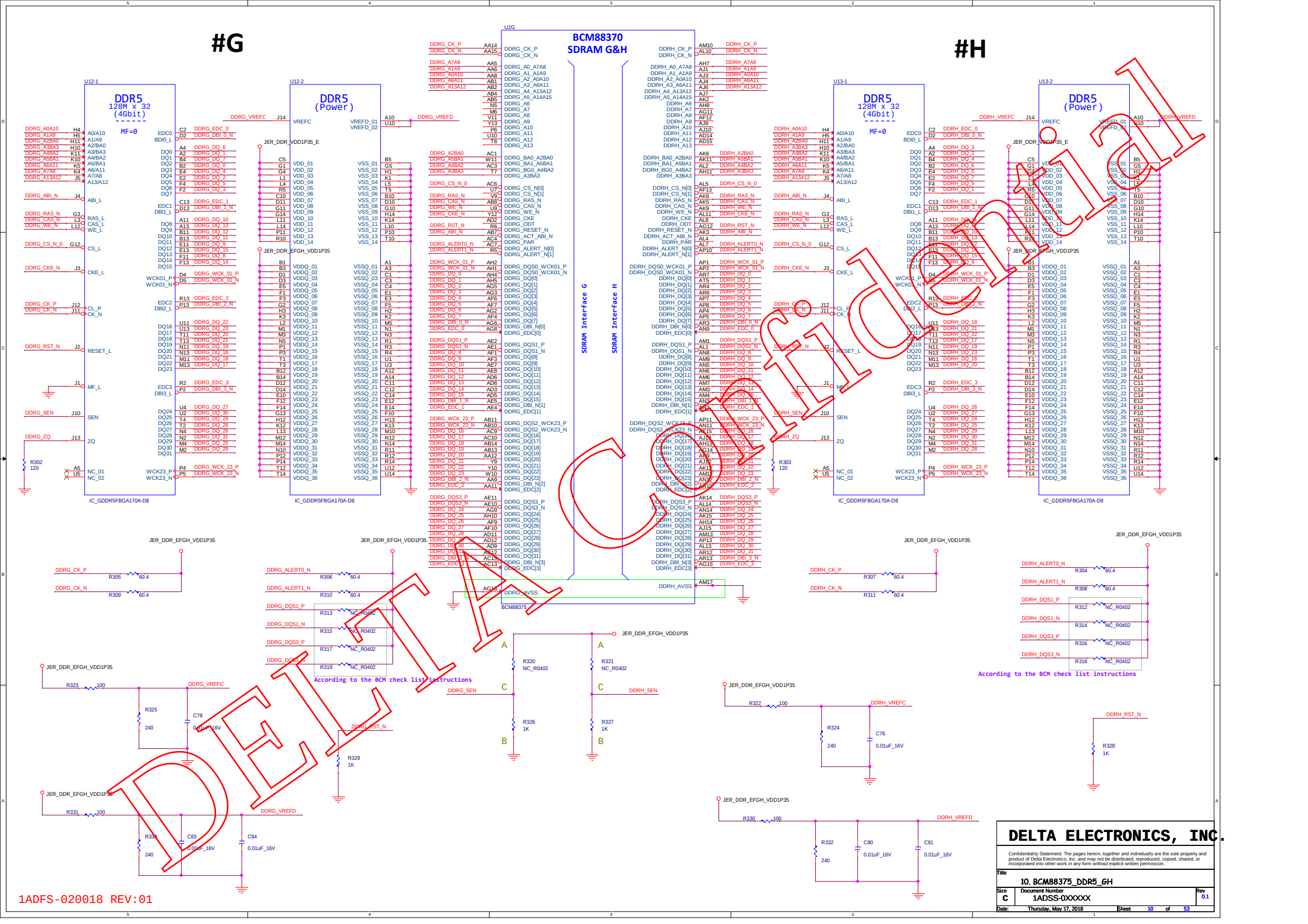
DELTA ELECTRONICS, INC.

Title	06. BCM88375_Clocks	
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 6 of 53	

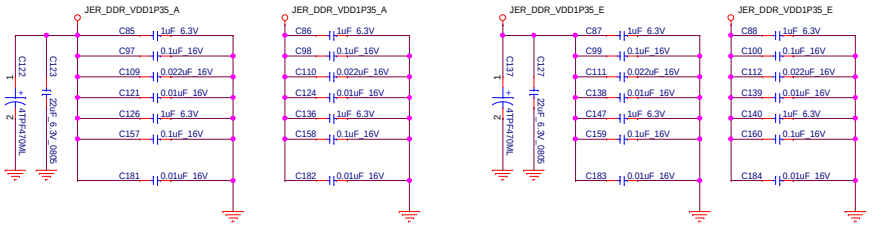

#A
#B
BCM88370
SDRAM A&B
SDRAM Interface A
SDRAM Interface B
DDR5
128M x 32
(4Gbit)
MF=0
DDR5
(Power)
IC_GDDR5FBGA170A-D8
BCM88375
JER_DDR_ABCD_VDD1P35
JER_DDR_VDD1P35_A
DDRA_VREFC
DDRA_VREFD
DDRB_VREFC
DDRB_VREFD
DDRA_RST_N
DDRB_RST_N
DDRA_SEN
DDRB_SEN
DDRA_ZQ
DDRB_ZQ
DDRA_AVSS
DDRB_AVSS
According to the BCM check list instructions
DELTA CONFIDENTIAL
DELTA ELECTRONICS, INC.
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.
Title
07. BCM88375_DDR5_AB
Size C
Document Number 1ADSS-0XXXXX
Rev 0.1
Date: Thursday, May 17, 2018
Sheet 7 of 53
1ADFS-020018 REV:01


#C
#D
BCM88370
SDRAM C&D
SDRAM Interface C
SDRAM Interface D
DDR5
128M x 32
(4Gbit)
MF=0
DDR5
(Power)
IC_GDDR5FBGA170A-D8
BCM88375
JER_DDR_VDD1P35_A
JER_DDR_ABCD_VDD1P35
According to the BCM check list instructions
DELTA CONFIDENTIAL
DELTA ELECTRONICS, INC.
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.
Title
08_BCM88375_DDR5_CD
Size C
Document Number 1ADSS-0XXXXX
Rev 0.1
Date: Thursday, May 17, 2018
Sheet 8 of 53
1ADFS-020018 REV:01

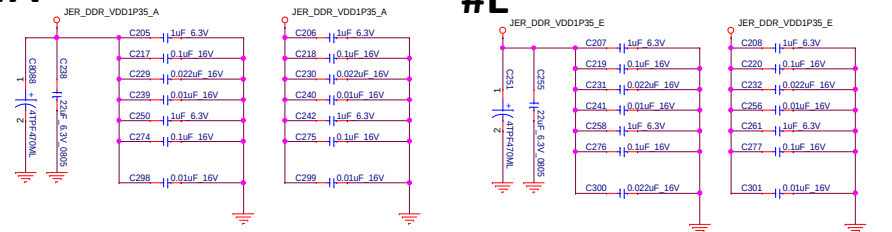

#E
#F
BCM88370
SDRAM E&F
SDRAM Interface E
SDRAM Interface F
U2F
U10-1
U10-2
U11-1
U11-2
DDR5
128M x 32
(4Gbit)
MF=0
DDR5
(Power)
IC_GDDR5FBGA170A-D8
JER_DDR_VDD1P35_E
JER_DDR_EFGH_VDD1P35
BCM88375
U17
DELTA CONFIDENTIAL
According to the BCM check list instructions
Ref-circuit is 60.4ohm
DELTA ELECTRONICS, INC.
09. BCM88375_DDR5_EF
1ADFS-020018 REV:01


#G
#H
U2G
BCM88370
SDRAM G&H
SDRAM Interface G
SDRAM Interface H
U12-1
U12-2
U13-1
U13-2
DDR5
128M x 32
(4Gbit)
MF=0
DDR5
(Power)
IC_GDDR5FBGA170A-D8
JER_DDR_VDD1P35_E
JER_DDR_EFGH_VDD1P35
BCM88375
DELTA CONFIDENTIAL
According to the BCM check list instructions
According to the BCM check list instructions
DELTA ELECTRONICS, INC.
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.
Title
10. BCM88375_DDR5_GH
Size
C
Document Number
1ADSS-0XXXXX
Rev
0.1
Date:
Thursday, May 17, 2018
Sheet
10
of
53
1ADFS-020018 REV:01

-- DRAMs VDD --

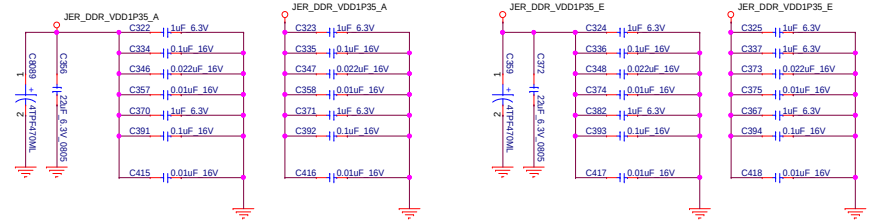


#A



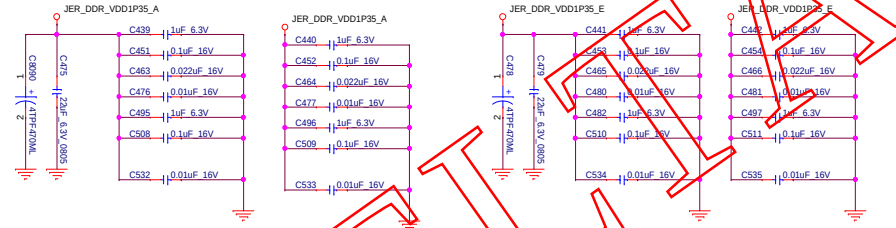
#E

#B



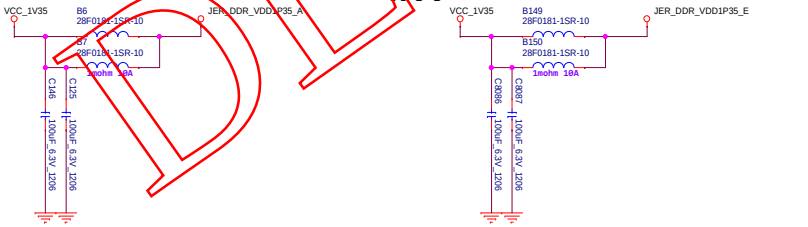
#F

#C



#G

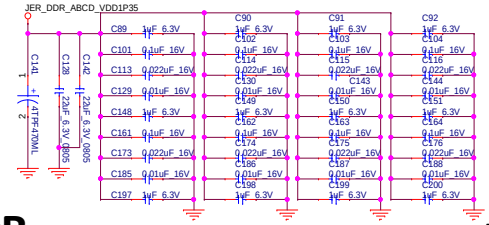
#D



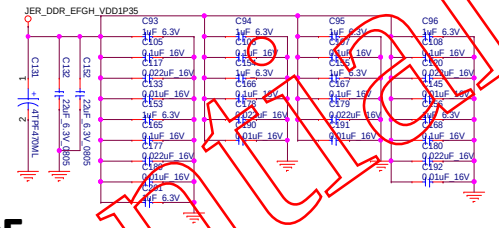
#H

-- DRAMs VDDQ --

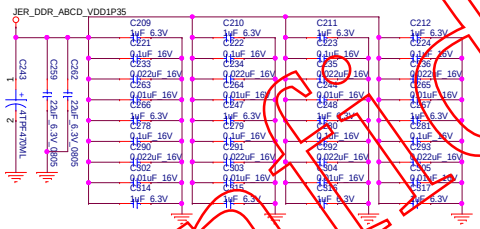
#A



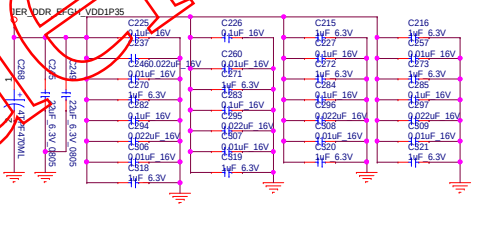
#E



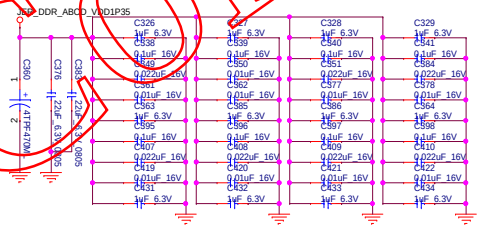
#B



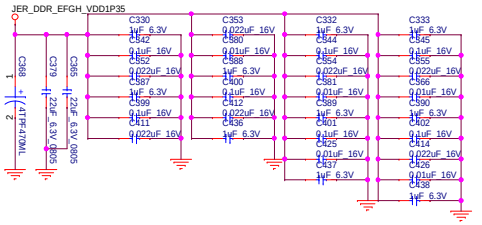
#F



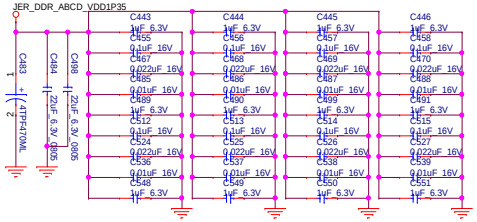
#C



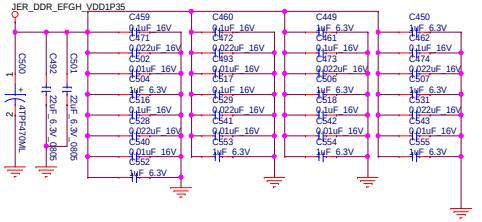
#G



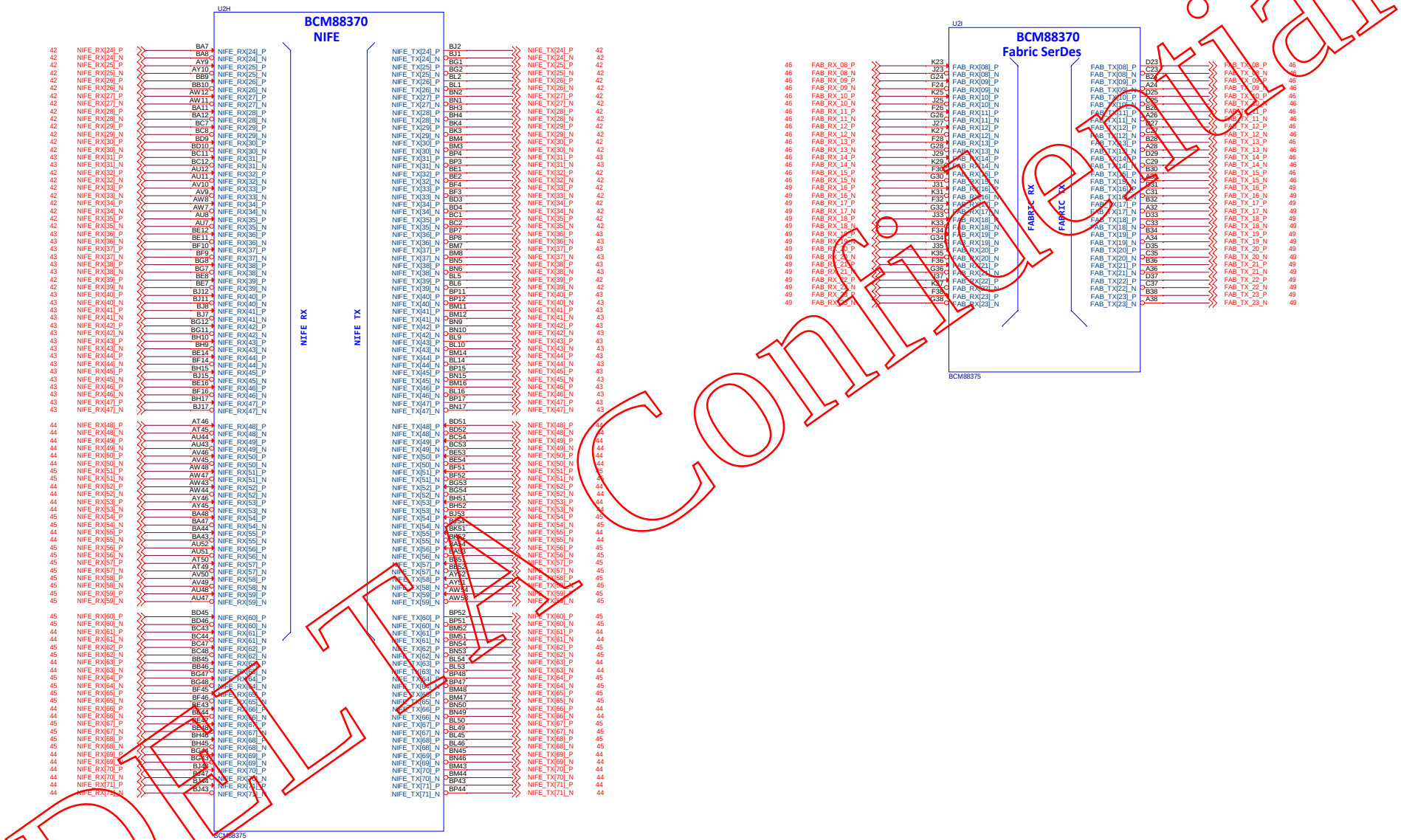
#D



#H



DELTA ELECTRONICS, INC.		
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.		
Title: 11. BCM88375_SDRAM_PWR		
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 11 of 53	



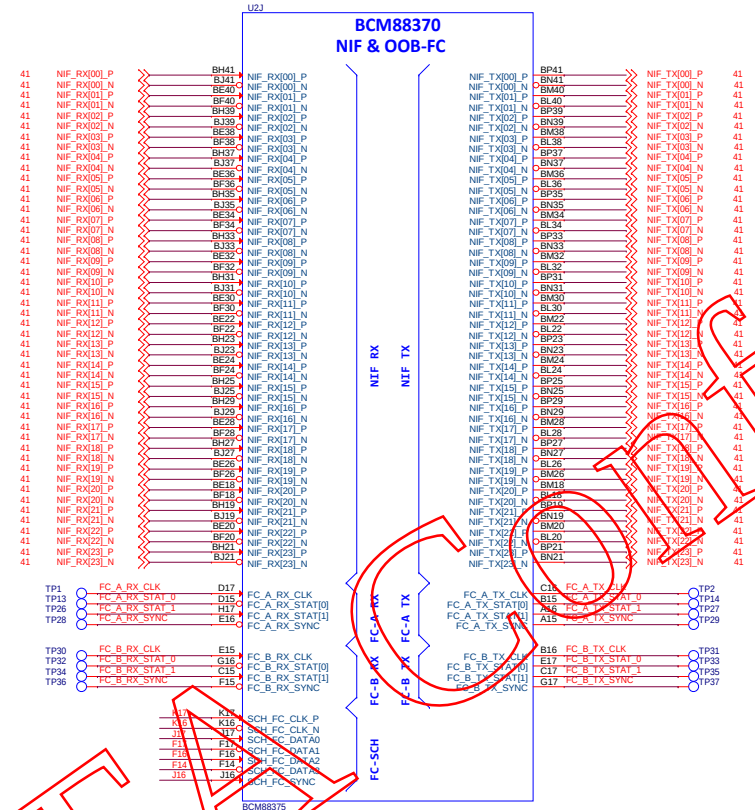
DELTA ELECTRONICS, INC.

Title: 12. BCM88375_FAB_NIFE

Size	Document Number	Rev
C	1ADSS-0XXXXX	0.1

Date: Thursday, May 17, 2018 Sheet 12 of 53

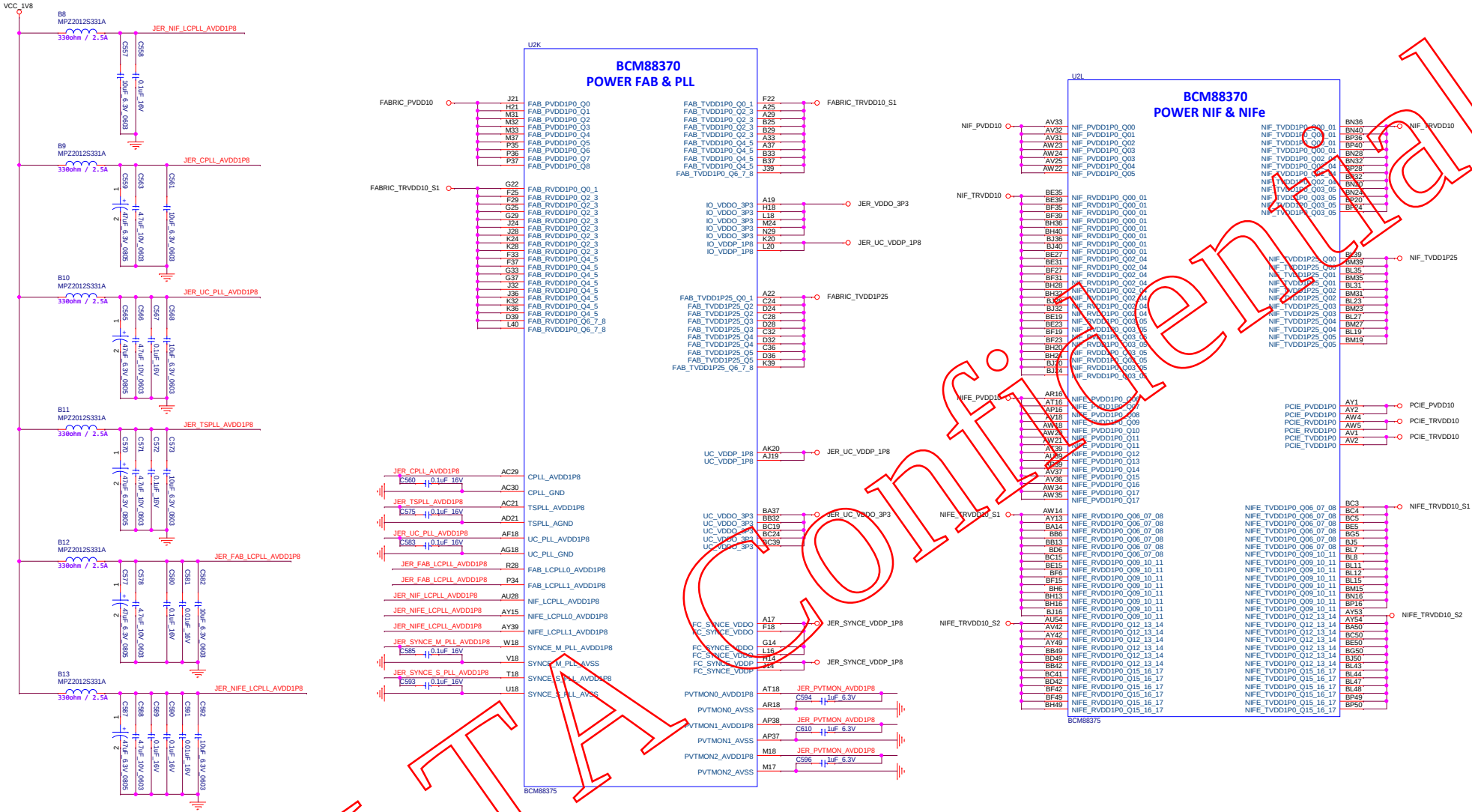
1ADFS-020018 REV:01



1ADFS-020018 REV:01

DELTA ELECTRONICS, INC.

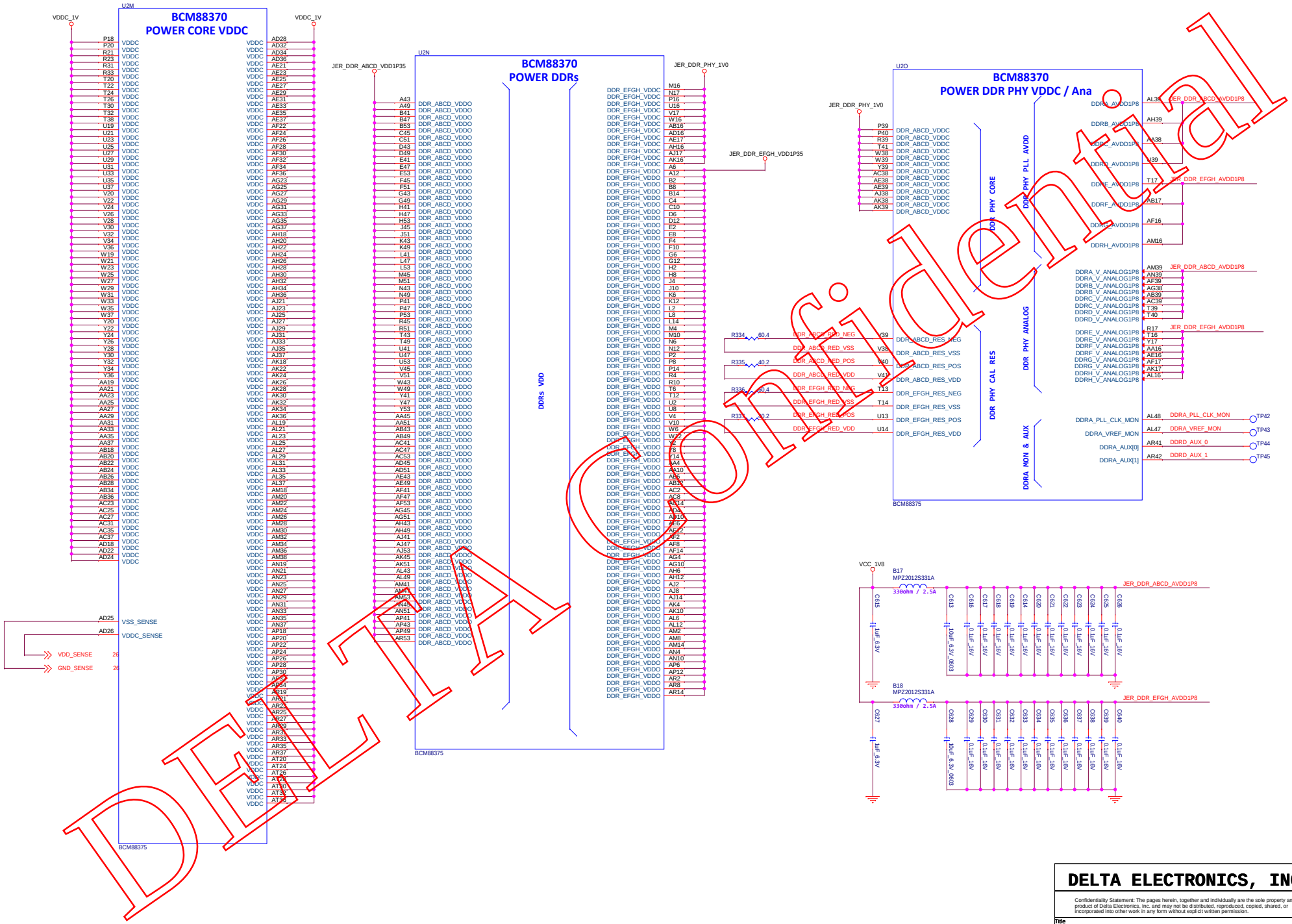
Title	13. BCM88375_NIF	
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 13 of 53	



1ADFS-020018 REV:01

DELTA ELECTRONICS, INC.

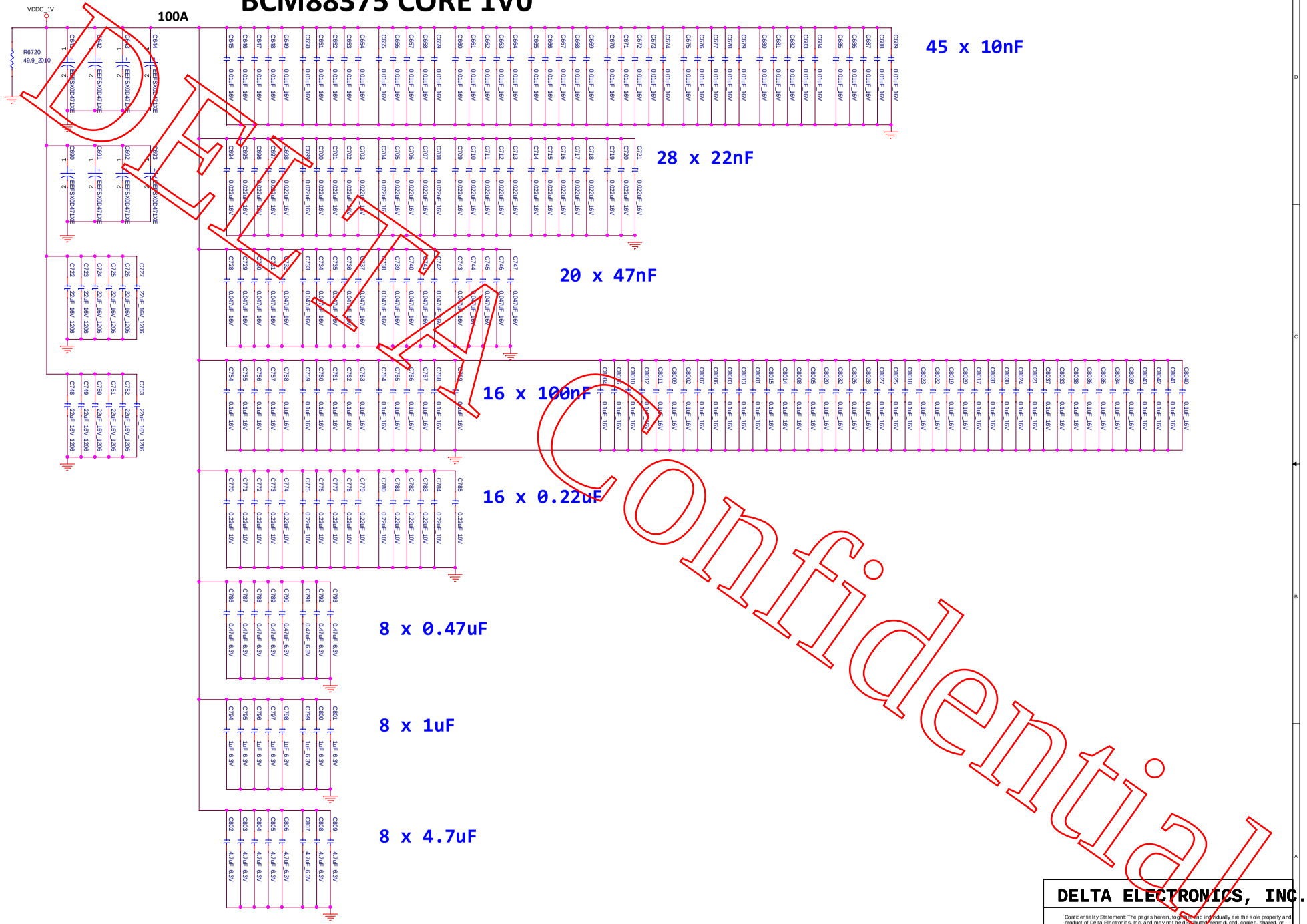
Title	14. BCM88375_PWR_FAB_NIF	
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 14 of 53	



DELTA ELECTRONICS, INC.	
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.	
Title	15. BCM88375_PWR_VDDC_DDR
Size: C	Document Number: 1ADSS-0XXXXX
Rev: 0.1	
Date: Thursday, May 17, 2018	Sheet 15 of 53

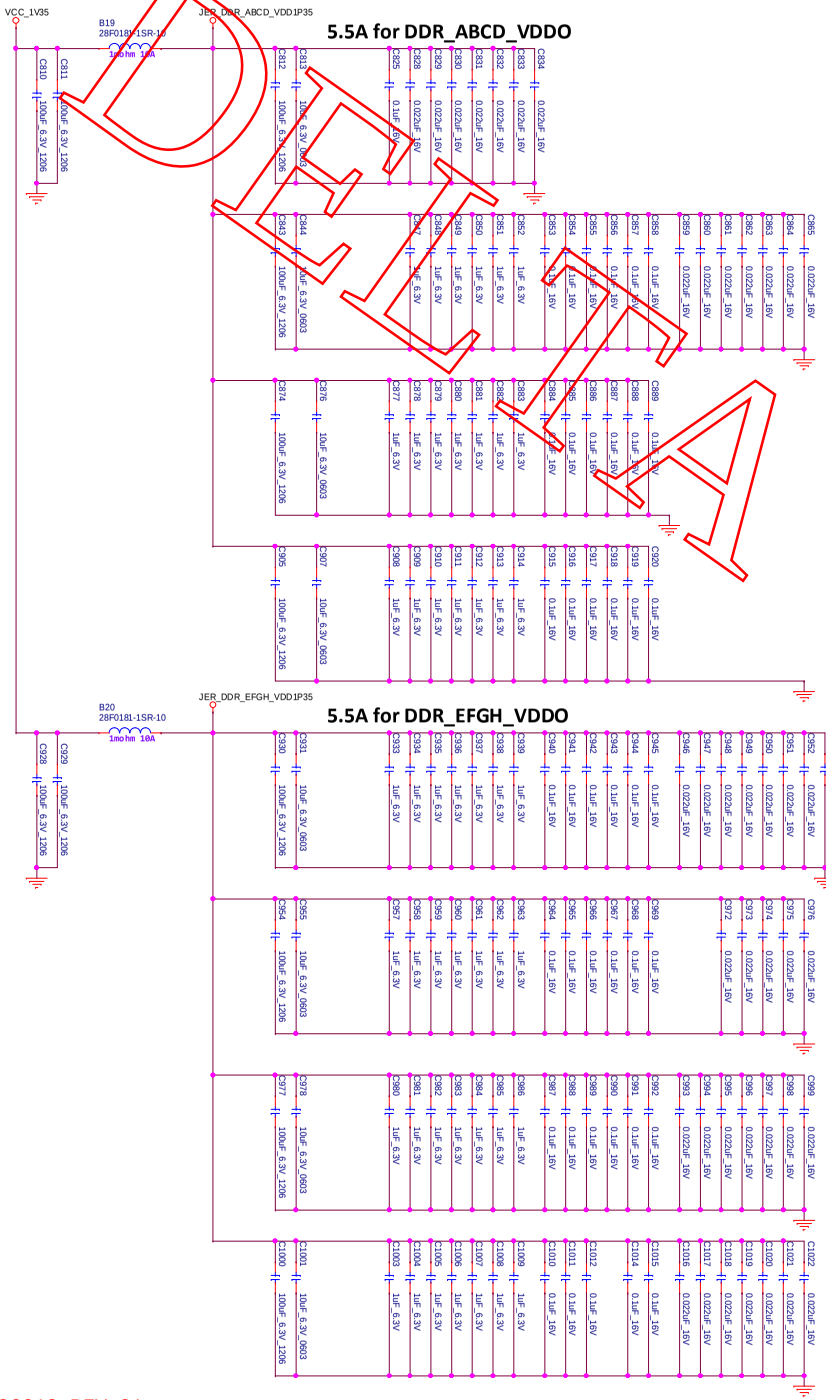
1ADFS-020018 REV:01

BCM88375 CORE 1V0



DELTA ELECTRONICS, INC.		
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.		
Title	16. BCM88375_PWR_DECOUP1	
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 16 of 53	

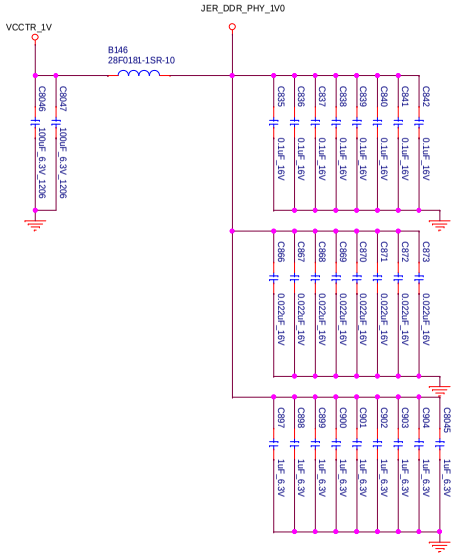
BCM88375 1V35 GDDR5 VDDO



BCM88375 1VD DDR PHY VDDC

DDR_VDDC 24 power pins

5.6A, Max Current 700mA per BCM88375 I/F



8 x 0.1uF

8 x 0.022uF

8 x 1uF

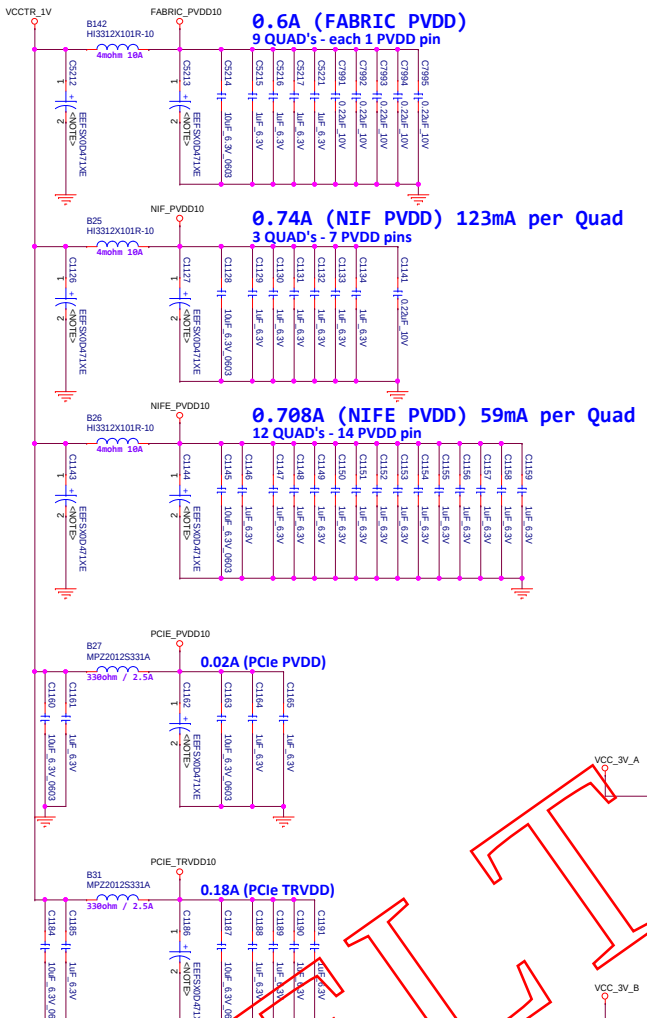
DELTA ELECTRONICS, INC.		
Confidentiality Statement: The pages herein, however and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without expressed written permission.		
Title: 17. BCM88375_PWR_DECOUP2		
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 17 of 53	

BCM88375 1V0 TRVDD

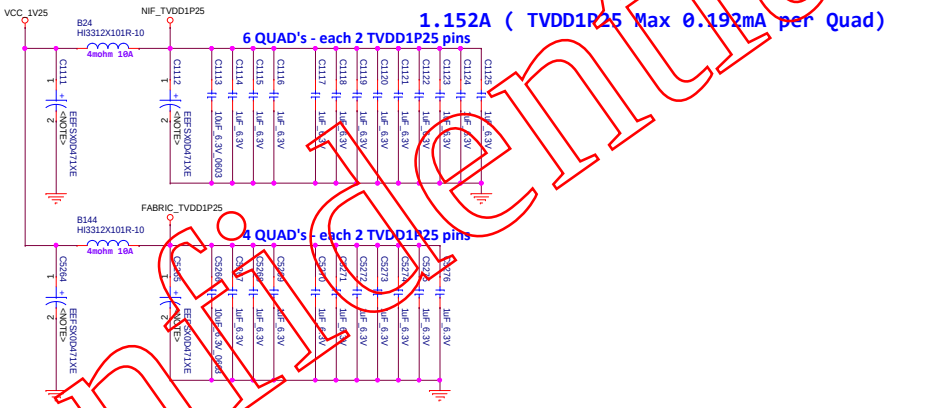
DELTA ELECTRONICS, INC.

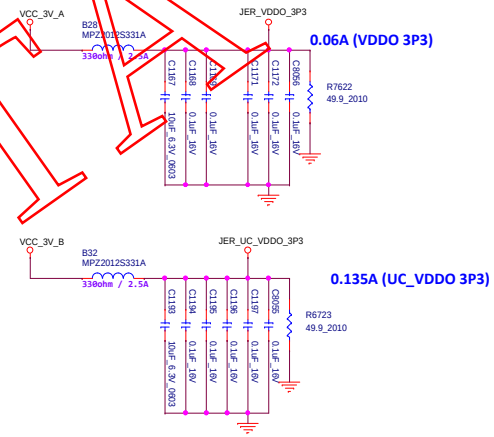
Title	18. BCM88375_PWR_DECOUP3	
Size C	Document Number 1ADSS-0XXXXX	Rev 0.1
Date: Thursday, May 17, 2018	Sheet 18 of 53	

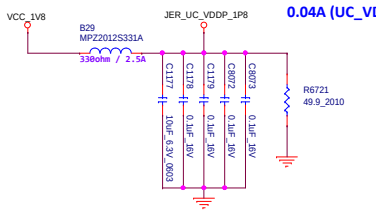
BCM88375 1V0 PVDD

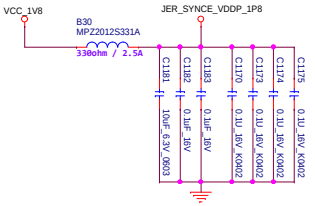


BCM88375 TVDD1P25

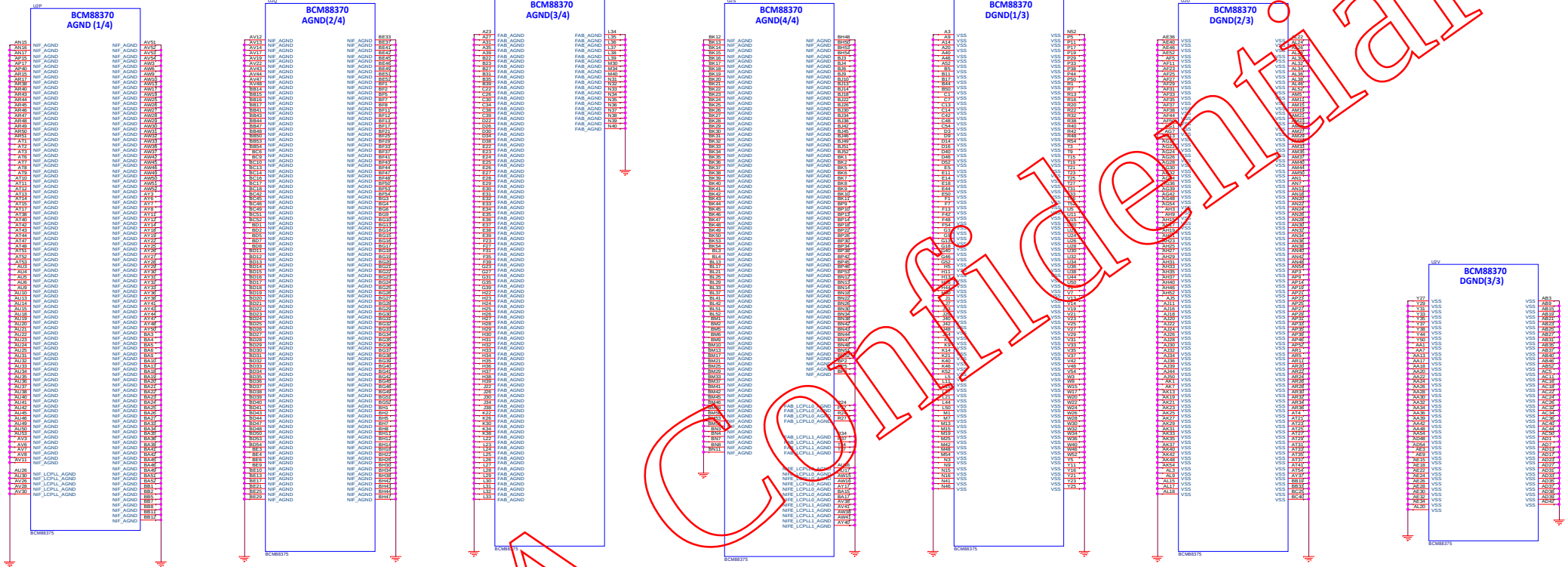








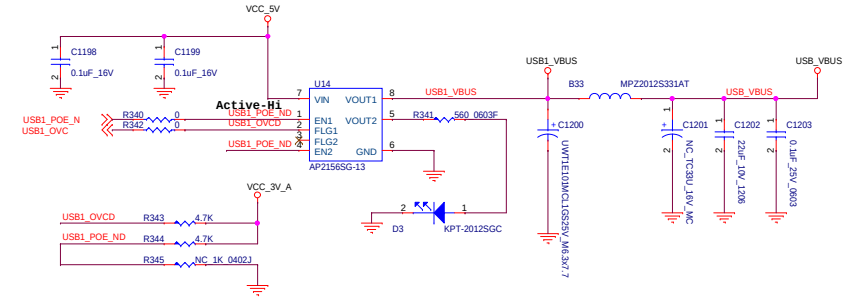
DELTA ELECTRONICS, INC.		
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.		
Title: 19. BCM88375_PWR_DECOUP4		
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 19 of 53	



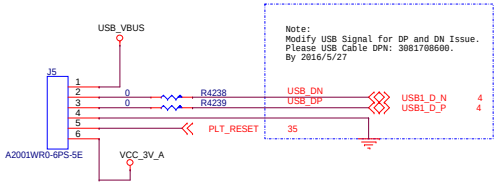
DELTA ELECTRONICS, INC.

Title	20. BCM88375_GND	
Size: D	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 20 of 53	

USB TypeA (HOST)



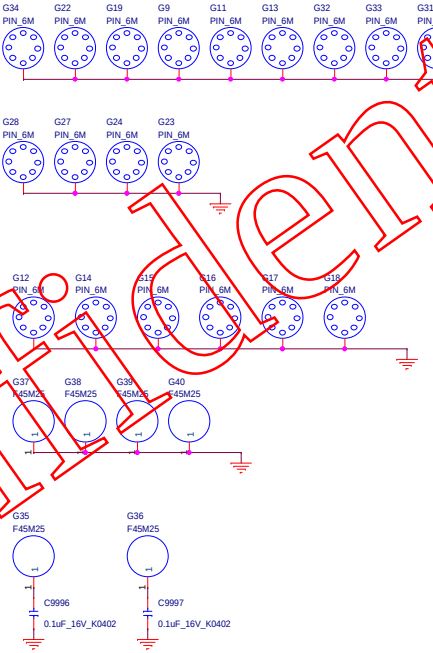
USB Board



BCM88375 heatsink

NL88659 heatsink

IR3555 heatsink



DELTA ELECTRONICS, INC.

Title	21. USB [Type A]	
Size C	Document Number 1ADSS-0XXXXX	Rev 0.1
Date: Thursday, May 17, 2018	Sheet 21 of 53	

DELTA ELECTRONICS, INC.

Title: 22. Reserved		
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 22 of 53	

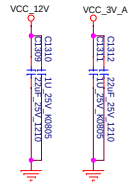
DELTA ELECTRONICS, INC.

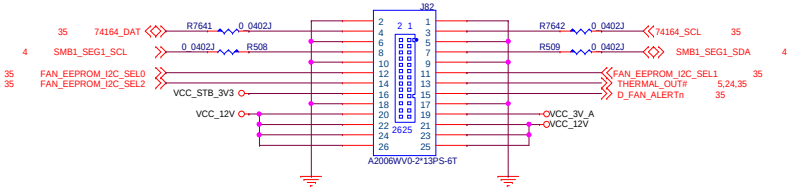
Title: 23. Reserved

Size	Document Number	Rev
C	1ADSS-0XXXXX	0.1

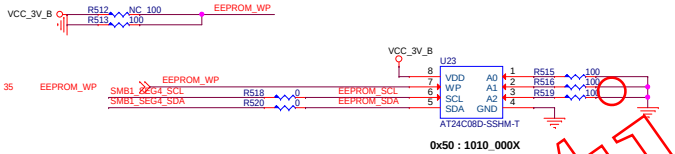
Date: Thursday, May 17, 2018 Sheet 23 of 53

FAN Connector

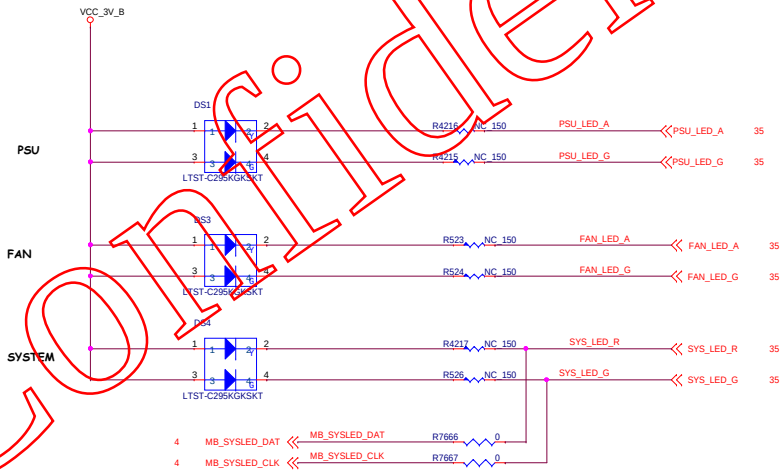




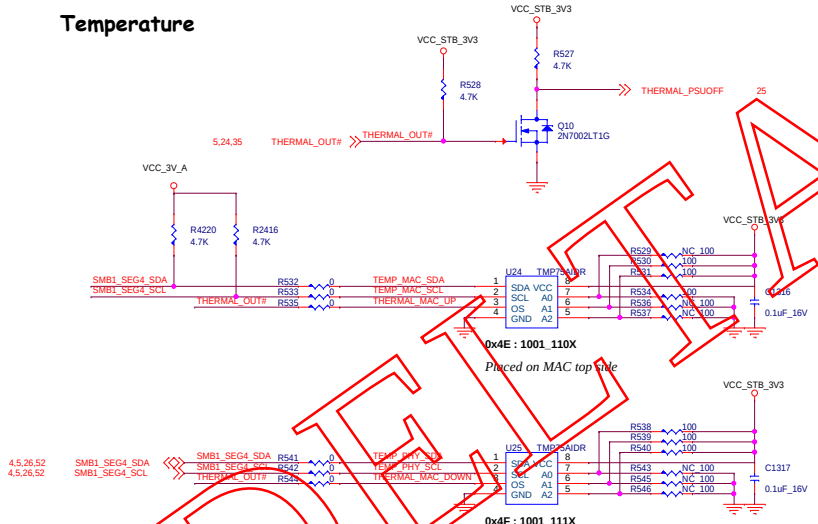
EEPROM

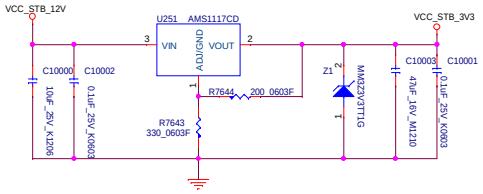


SYS LED



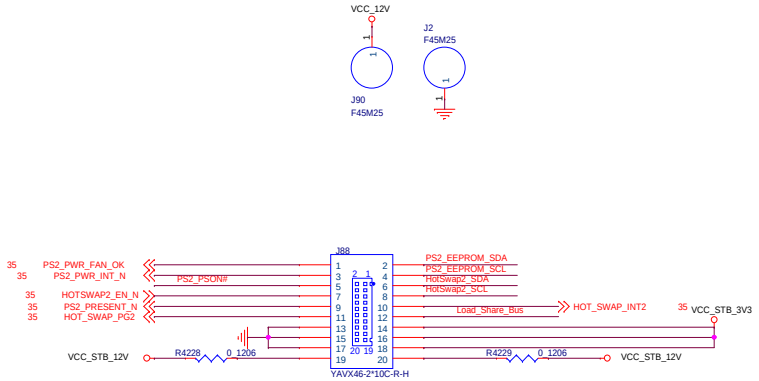
Temperature

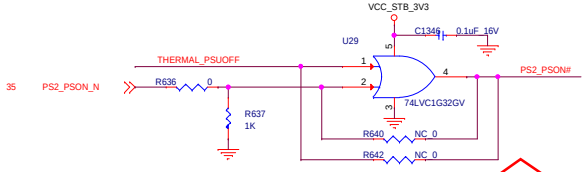


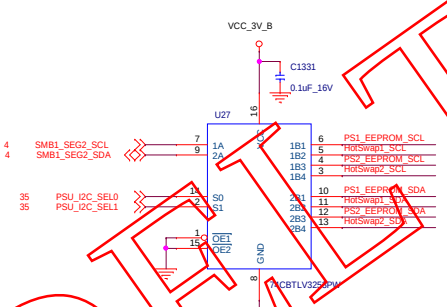


DELTA ELECTRONICS, INC.		
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.		
Title: 24. FANCN_TMP75_EEPROM		
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 24 of 53	

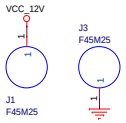
PSU2 Board to Board PWR connect

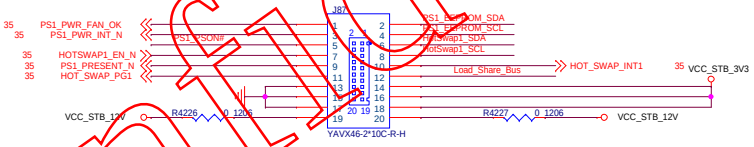


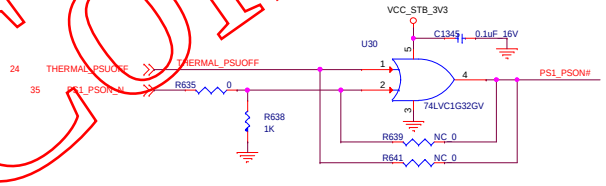




PSU1 Board to Board PWR connect





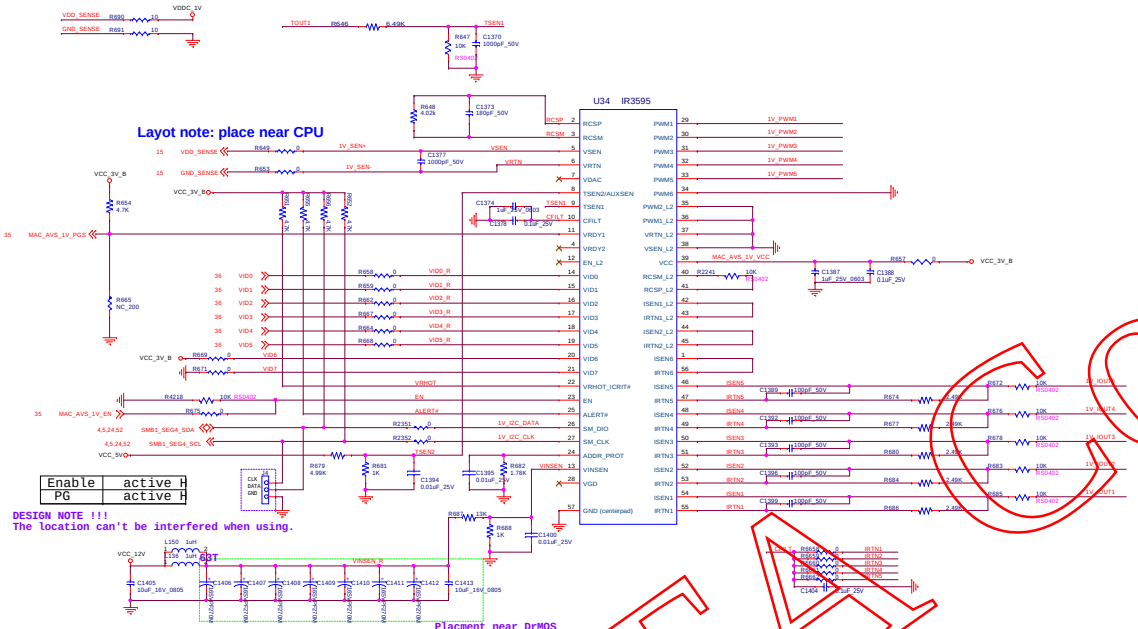


DELTA ELECTRONICS, INC.

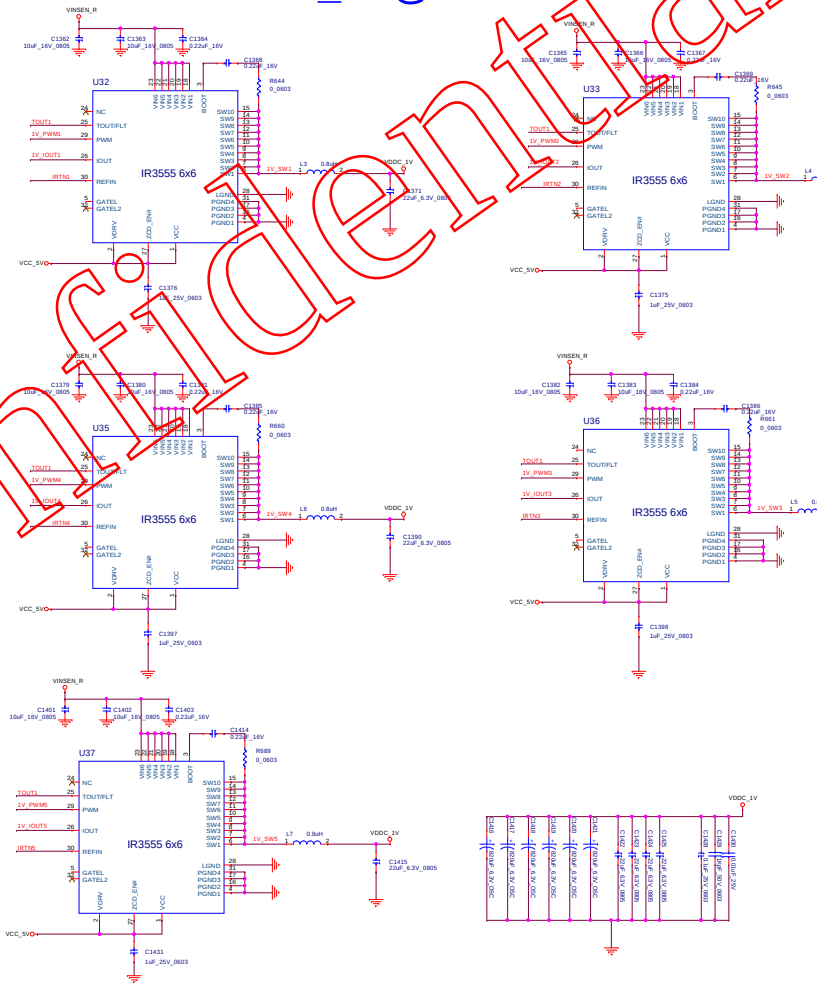
Title	25. PSU [CONN & HotSwap]	
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 25 of 53	

Core Power 1.0V

VCC_1V@ MAX:100A



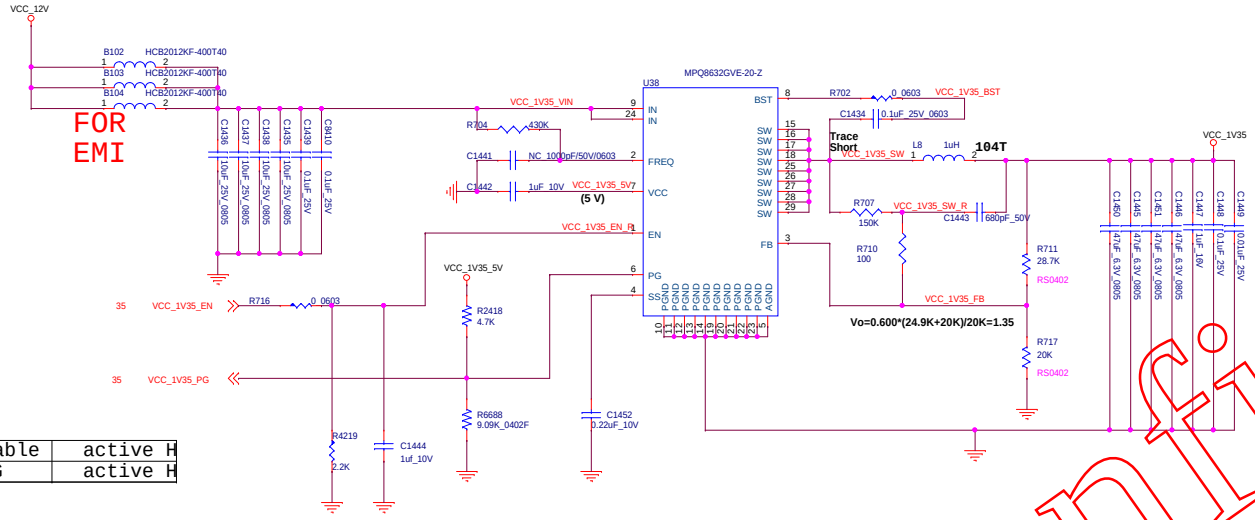
Vout	VID0	VID1	VID2	VID3	VID4	VID5	VID6	VID7
1.04375	1	1	0	1	1	0	1	0
1	0	1	0	0	0	1	1	0
0.95	0	1	0	1	0	1	1	0



DELTA ELECTRONICS, INC.

Title	26_PWR_1V0	
Size D	Document Number 1ADSS-0XXXXX	Rev 0.1
Date: Thursday, May 17, 2018	Sheet 26 of 53	

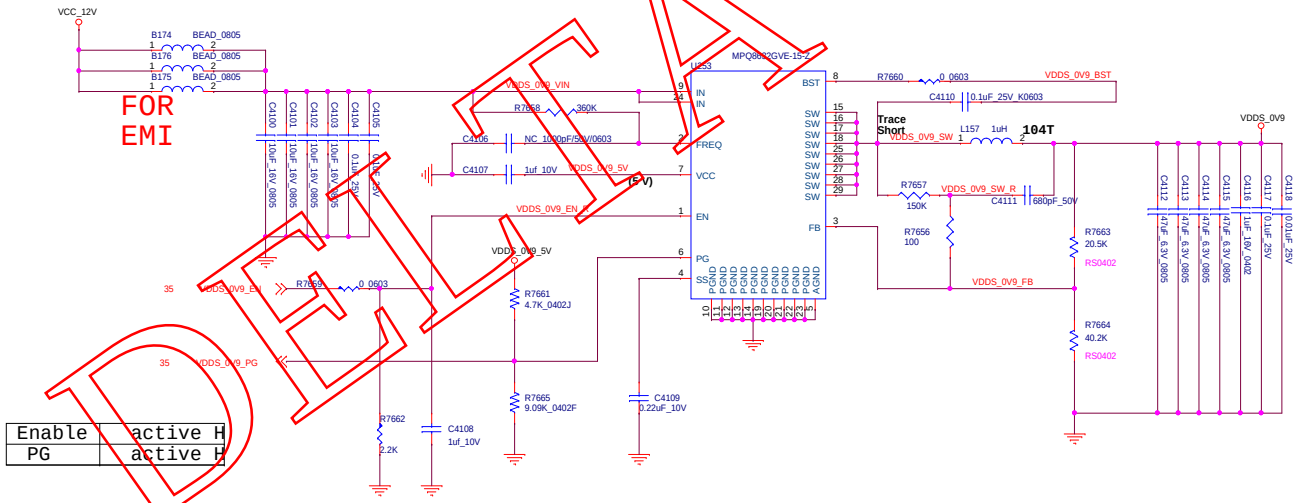
GDDR5 1.35V



PWM Frequency	300Khz
MAX Current	17.185A
OCP	30A
Output Voltage	1.35V
VFB	0.6V

Enable	active H
PG	active H

VDDS_0V9



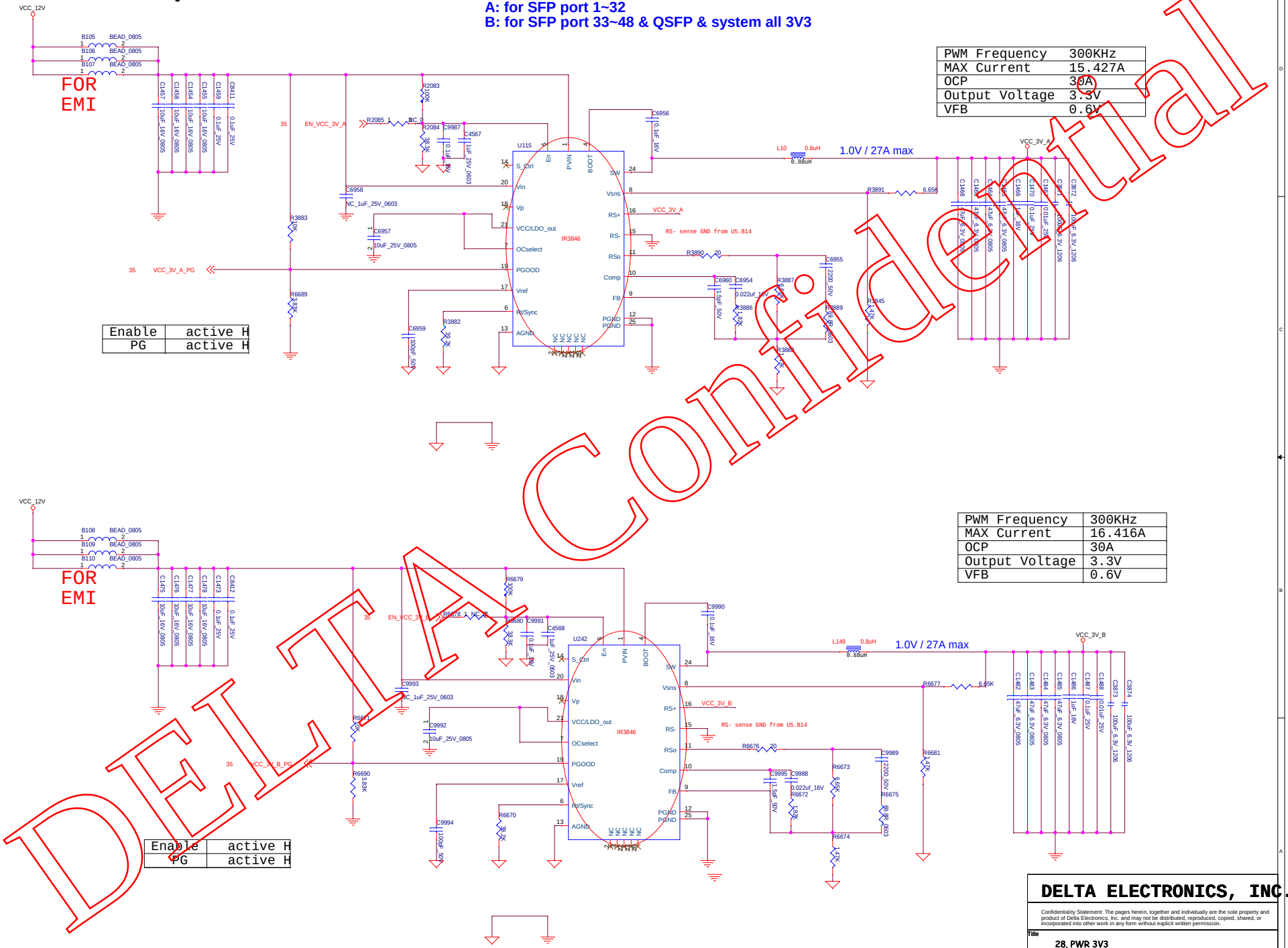
PWM Frequency	500KHz
MAX Current	15A
OCP	
Output Voltage	0.9V
VFB	

Enable	active H
PG	active H

DELTA ELECTRONICS, INC.		
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.		
Title: 27. PWR 1V35_DDRVTT		
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 27 of 53	

-- For All Chip I/Os VCC 3.3V --

A: for SFP port 1~32
B: for SFP port 33~48 & QSFP & system all 3V3



Enable	active H
PG	active H

PWM Frequency	300KHz
MAX Current	15.427A
OCP	30A
Output Voltage	3.3V
VFB	0.6V

Enable	active H
PG	active H

PWM Frequency	300KHz
MAX Current	16.416A
OCP	30A
Output Voltage	3.3V
VFB	0.6V

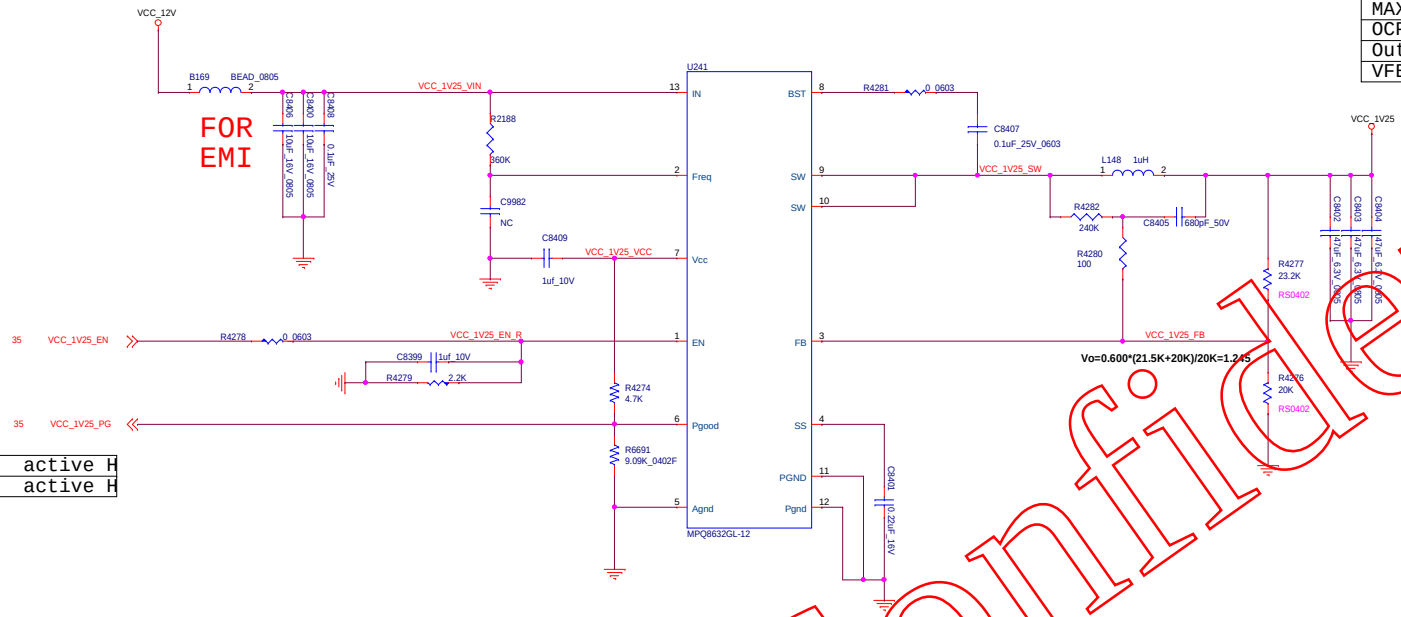
DELTA ELECTRONICS, INC.

Title: 28. PWR 3V3

Size: C | Document Number: 1ADSS-0XXXXX | Rev: 0.1

Date: Thursday, May 17, 2018 | Sheet 28 of 53

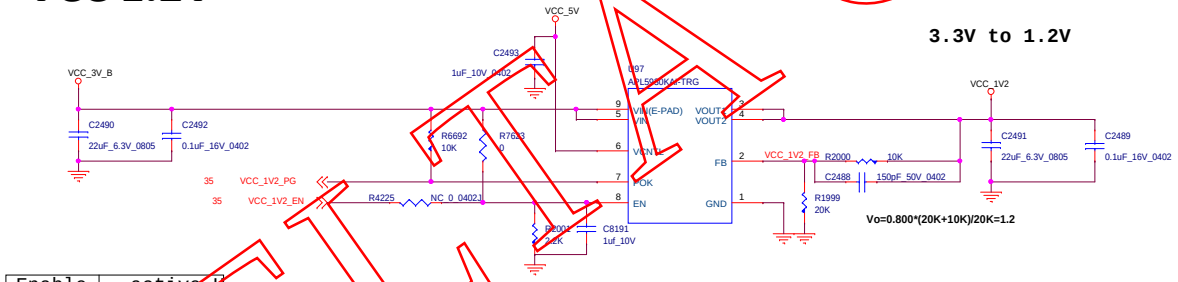
TVDD1P25 1.25V



PWM Frequency	500KHz
MAX Current	1.54A
OCP	7.6A
Output Voltage	1V25
VFB	0.6V

Enable	active H
PG	active H

VCC 1.2V



PWM Frequency	
MAX Current	0.46A
OCP	4.2A
Output Voltage	1.2V
VFB	0.8V

Enable	active H
PG	active H

DELTA ELECTRONICS, INC.

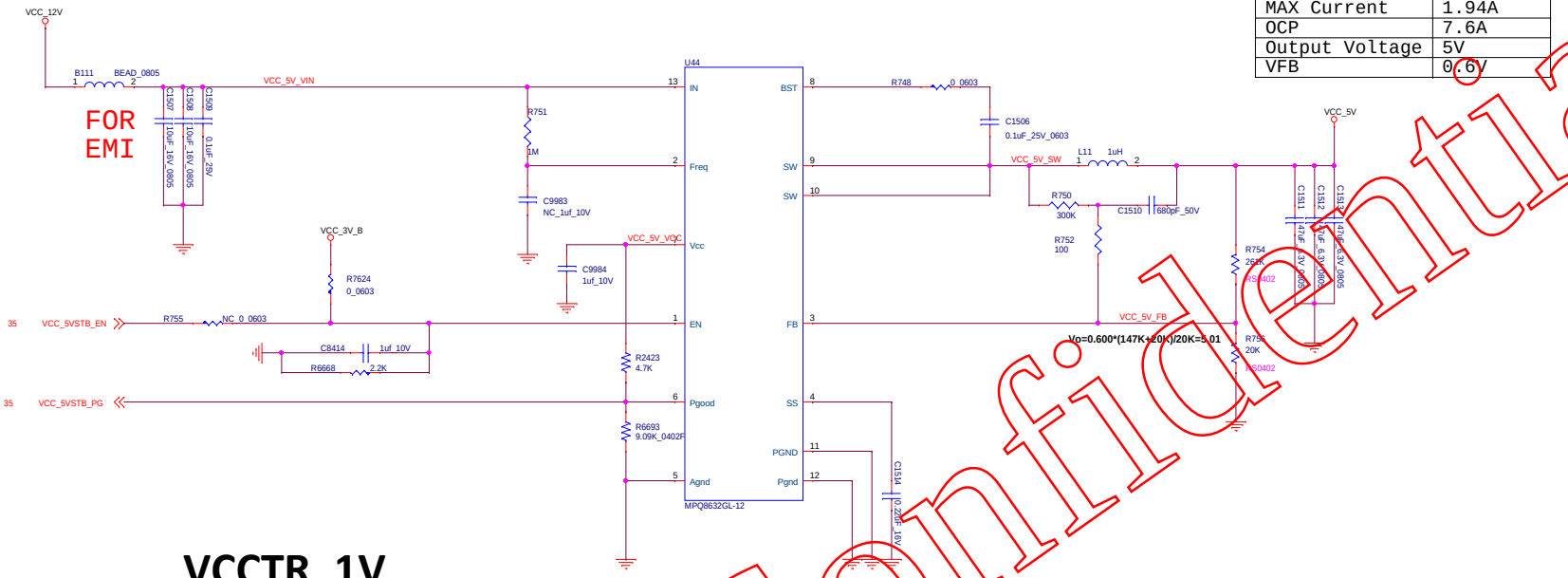
Title: 29. PWR 1V25_ 0V9_ 1V2

Size: C | Document Number: 1ADSS-0XXXXX | Rev: 0.1

Date: Thursday, May 17, 2018 | Sheet 29 of 53

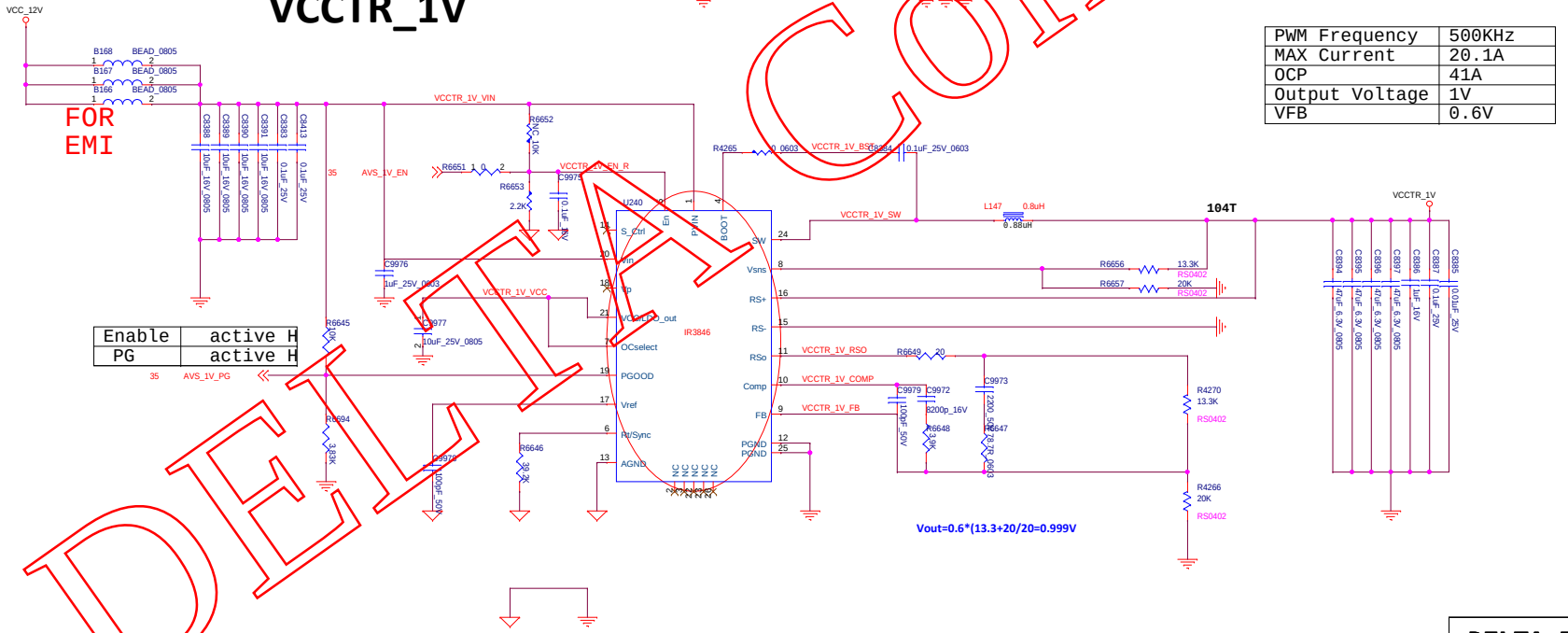
-- USB 5.0V --

PWM Frequency	500KHz
MAX Current	1.94A
OCP	7.6A
Output Voltage	5V
VFB	0.6V



VCCTR_1V

PWM Frequency	500KHz
MAX Current	20.1A
OCP	41A
Output Voltage	1V
VFB	0.6V



Enable	active H
PG	active H

35 AVS_1V_PG

DELTA ELECTRONICS, INC.

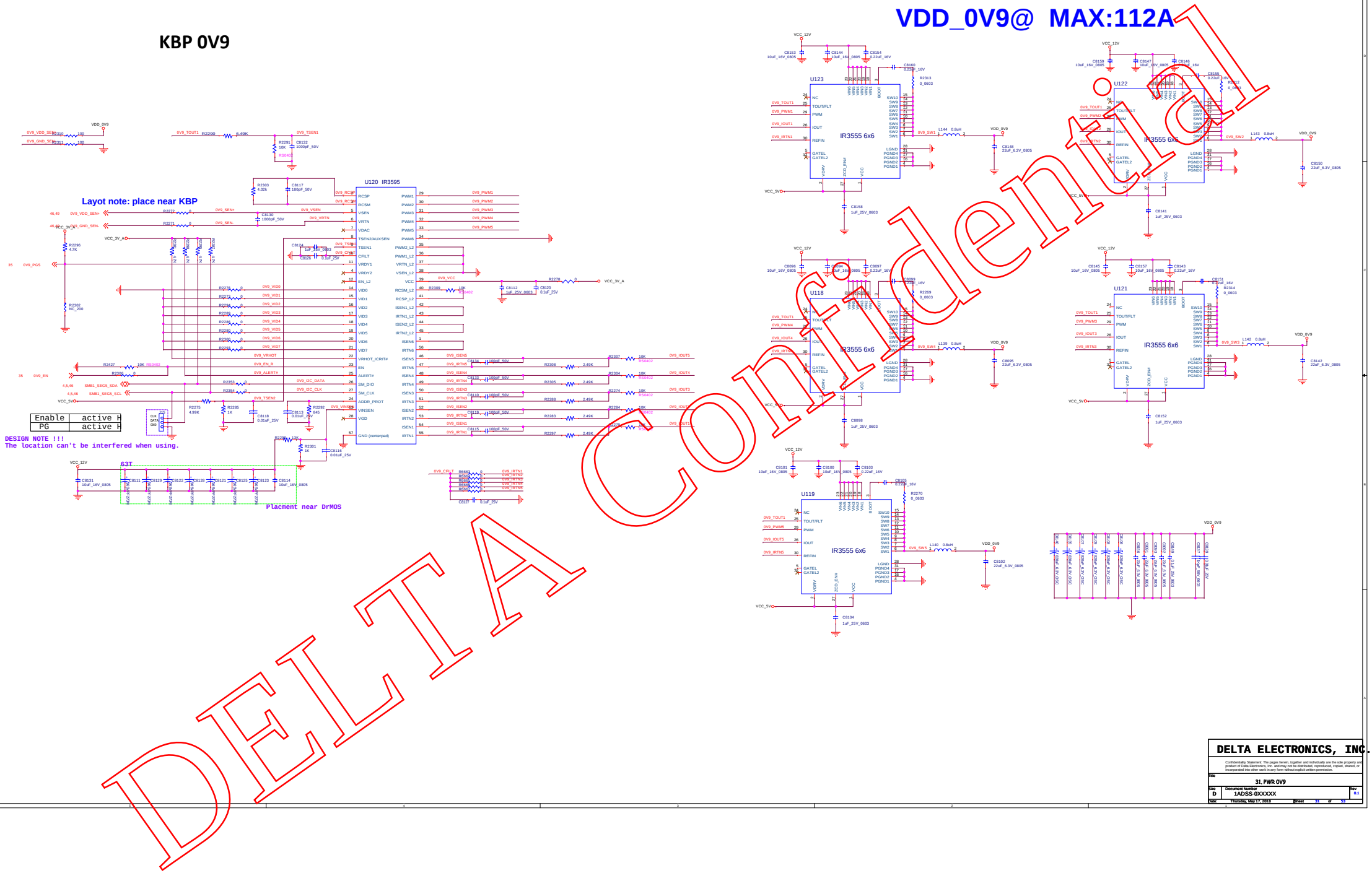
Title: 30. PWR 5V_AVS_1V

Size: C | Document Number: 1ADSS-0XXXXX | Rev: 0.1

Date: Thursday, May 17, 2018 | Sheet 30 of 53

KBP 0V9

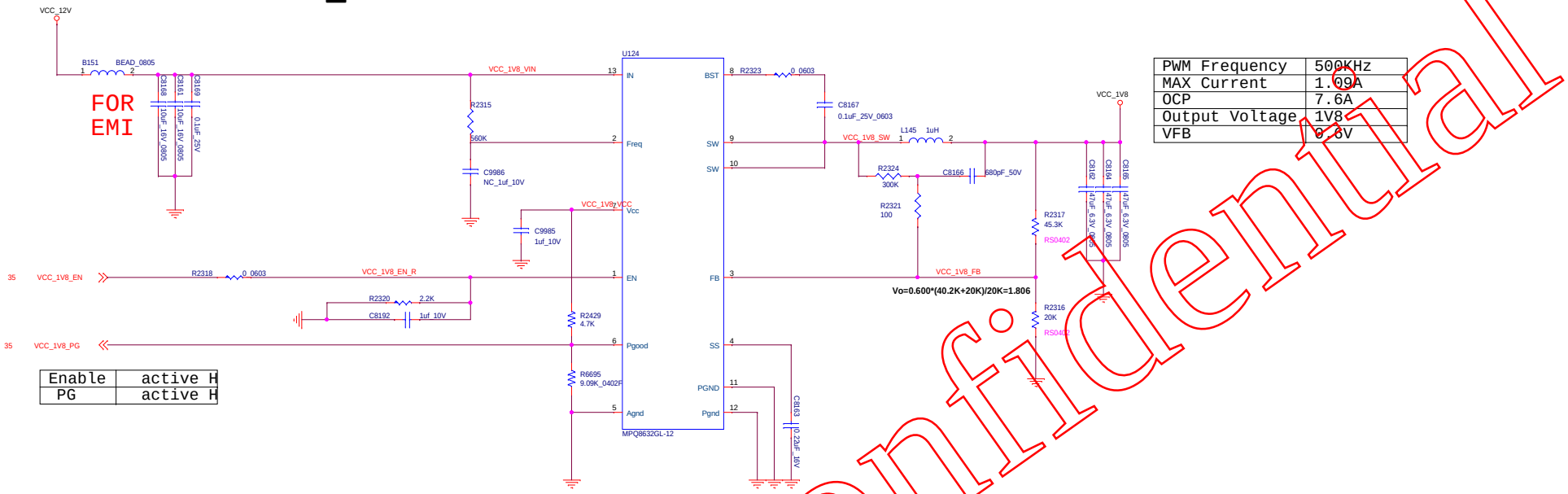
VDD_0V9@ MAX:112A



DELTA ELECTRONICS, INC.

Title	31. PWR 0V9	
Size: D	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 31 of 53	

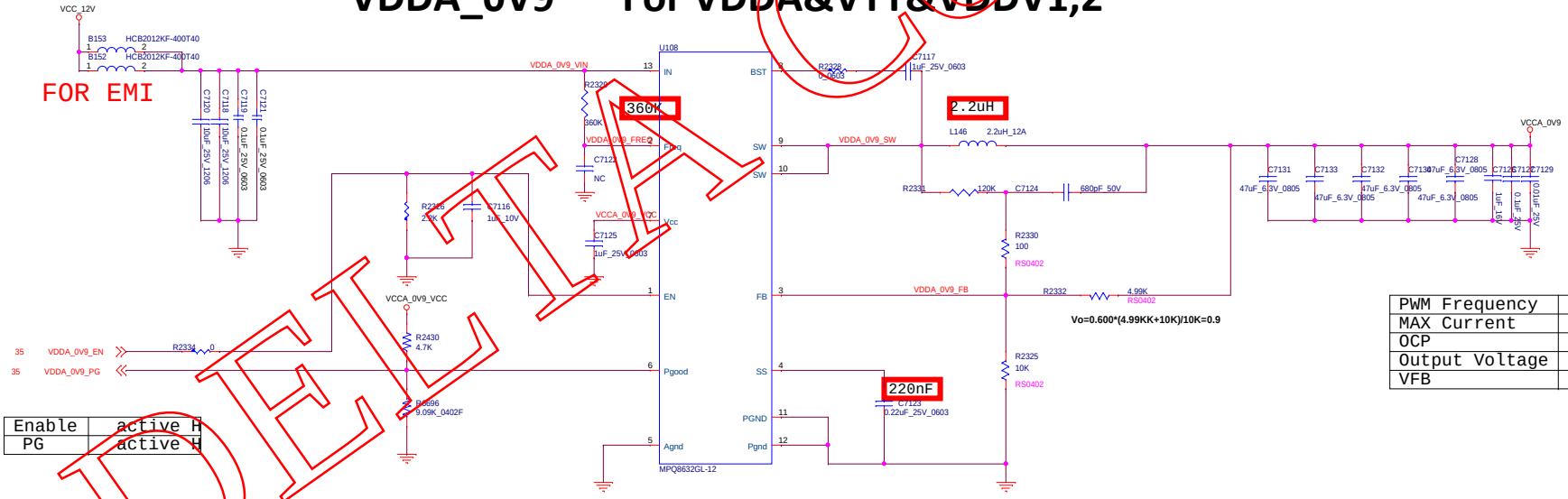
VCC_1V8



Enable	active H
PG	active H

PWM Frequency	500KHz
MAX Current	1.09A
OCP	7.6A
Output Voltage	1V8
VFB	0.6V

VDDA_0V9 For VDDA&VTT&VDDV1,2



Enable	active H
PG	active H

PWM Frequency	500KHz
MAX Current	6.7A
OCP	13.6A
Output Voltage	0V9
VFB	0.6V

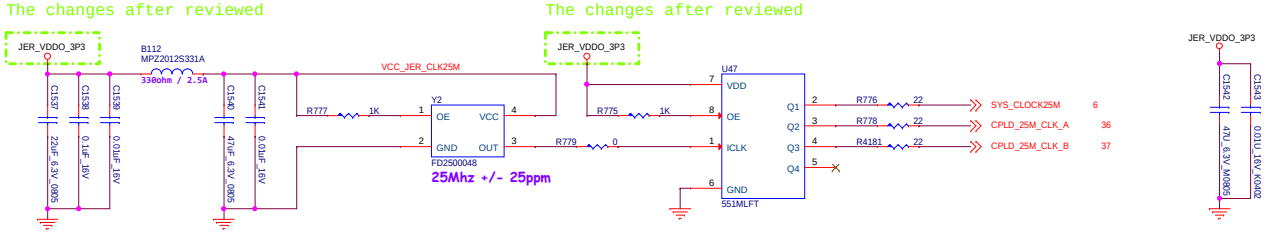
DELTA ELECTRONICS, INC.

Title: 32. PWR 1V8_VDDA_0V9

Size: C | Document Number: 1ADSS-0XXXXX | Rev: 0.1

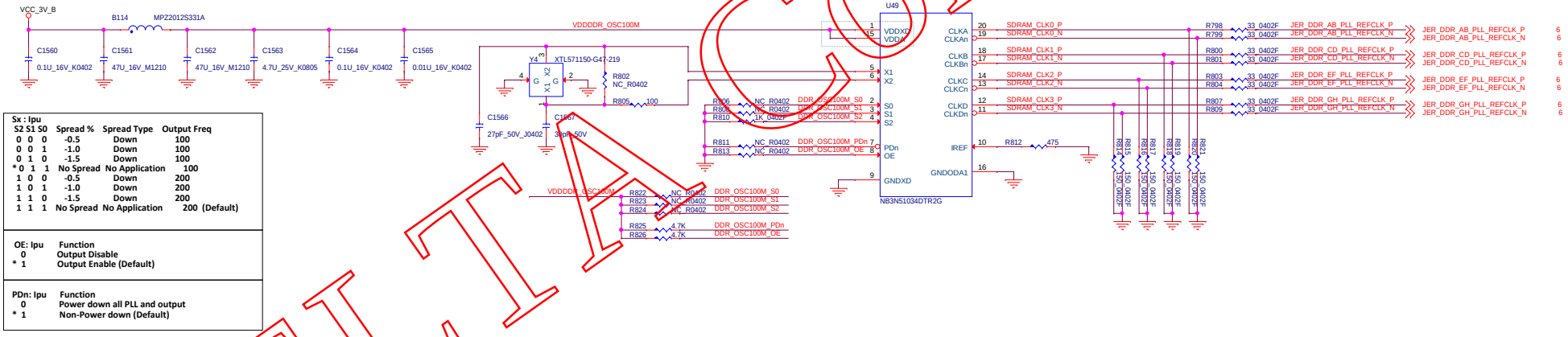
Date: Thursday, May 17, 2018 | Sheet 32 of 53

-- System & CPLD single-end 25M clock --



-- 25MHz Differential Clock for BCM88375 Core Clock --

-- 100MHz Differential Clock for BCM88375 SDRAM Clock --

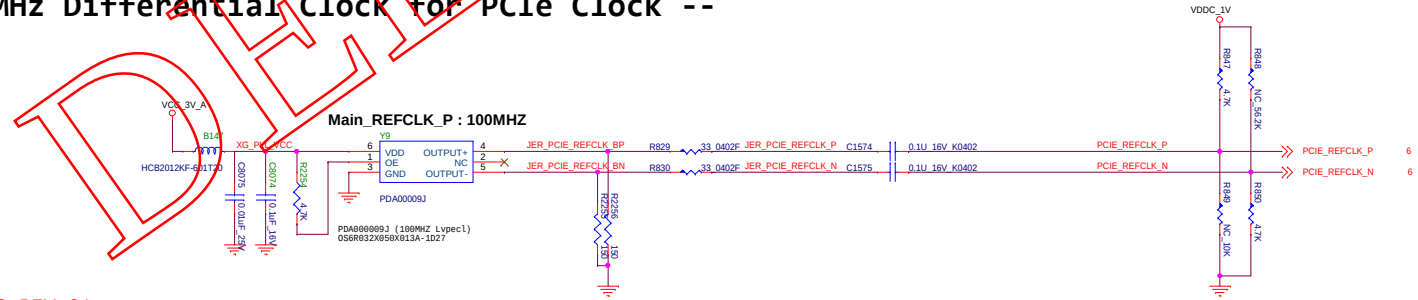


Sx : Ipu					
S2	S1	S0	Spread %	Spread Type	Output Freq
0	0	0	-0.5	Down	100
0	0	1	-1.0	Down	100
0	1	0	-1.5	Down	100
* 0	1	1	No Spread	No Application	100
1	0	0	-0.5	Down	200
1	0	1	-1.0	Down	200
1	1	0	-1.5	Down	200
1	1	1	No Spread	No Application	200 (Default)

OE: Ipu	Function
0	Output Disable
* 1	Output Enable (Default)

PDn: Ipu	Function
0	Power down all PLL and output
* 1	Non-Power down (Default)

-- 100MHz Differential Clock for PCIe Clock --



1ADFS-020018 REV:01

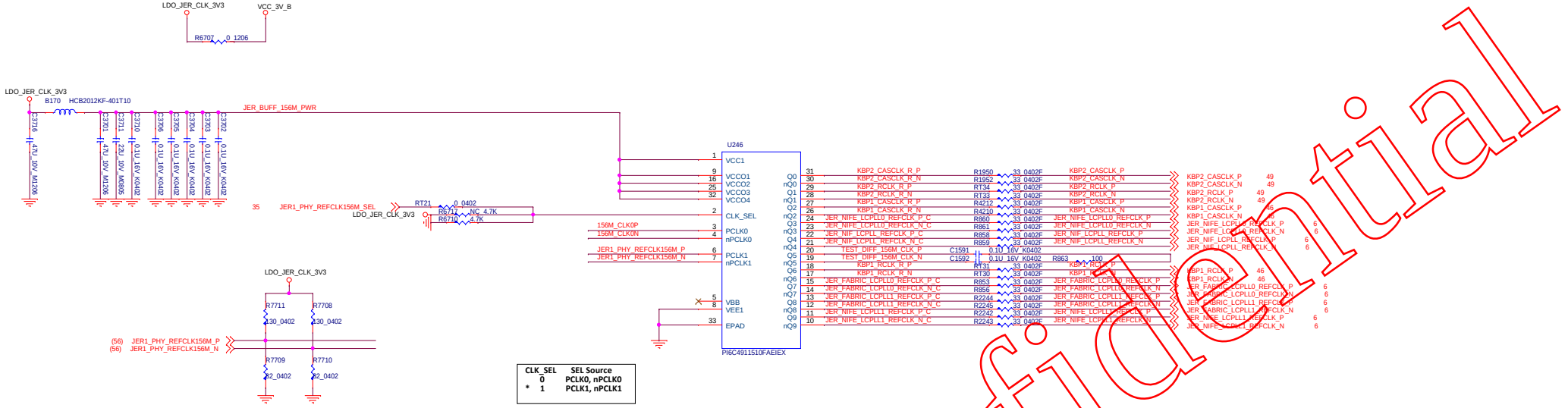
DELTA ELECTRONICS, INC.

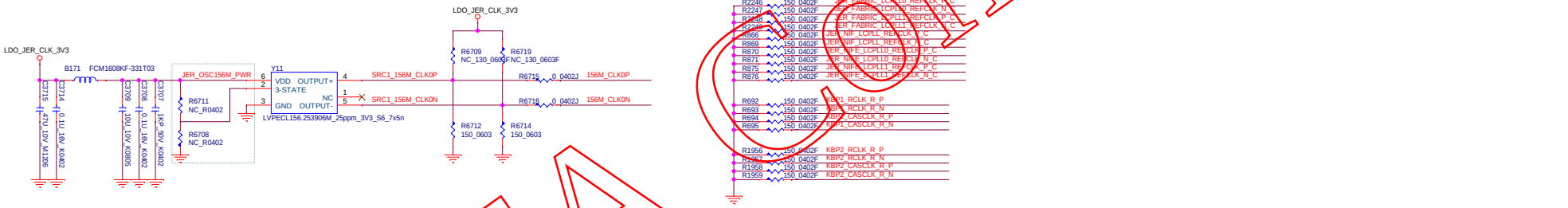
Title: 33. CLK_1 [25MHz & 100MHz]

Size: C | Document Number: 1ADSS-0XXXXX | Rev: 0.1

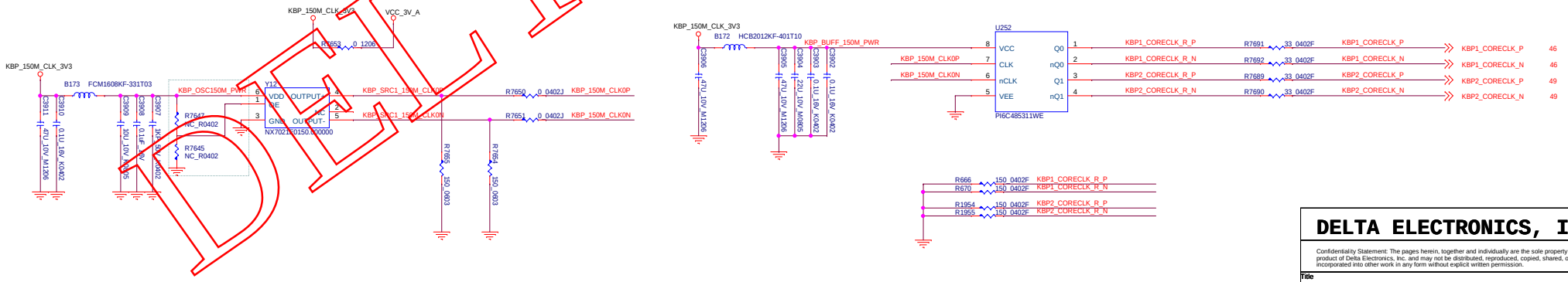
Date: Thursday, May 17, 2018 | Sheet 33 of 53

-- 156.25MHz Differential Clock for NIF/NIFE --





-- 150MHz Differential Clock for NL CORE CLK --



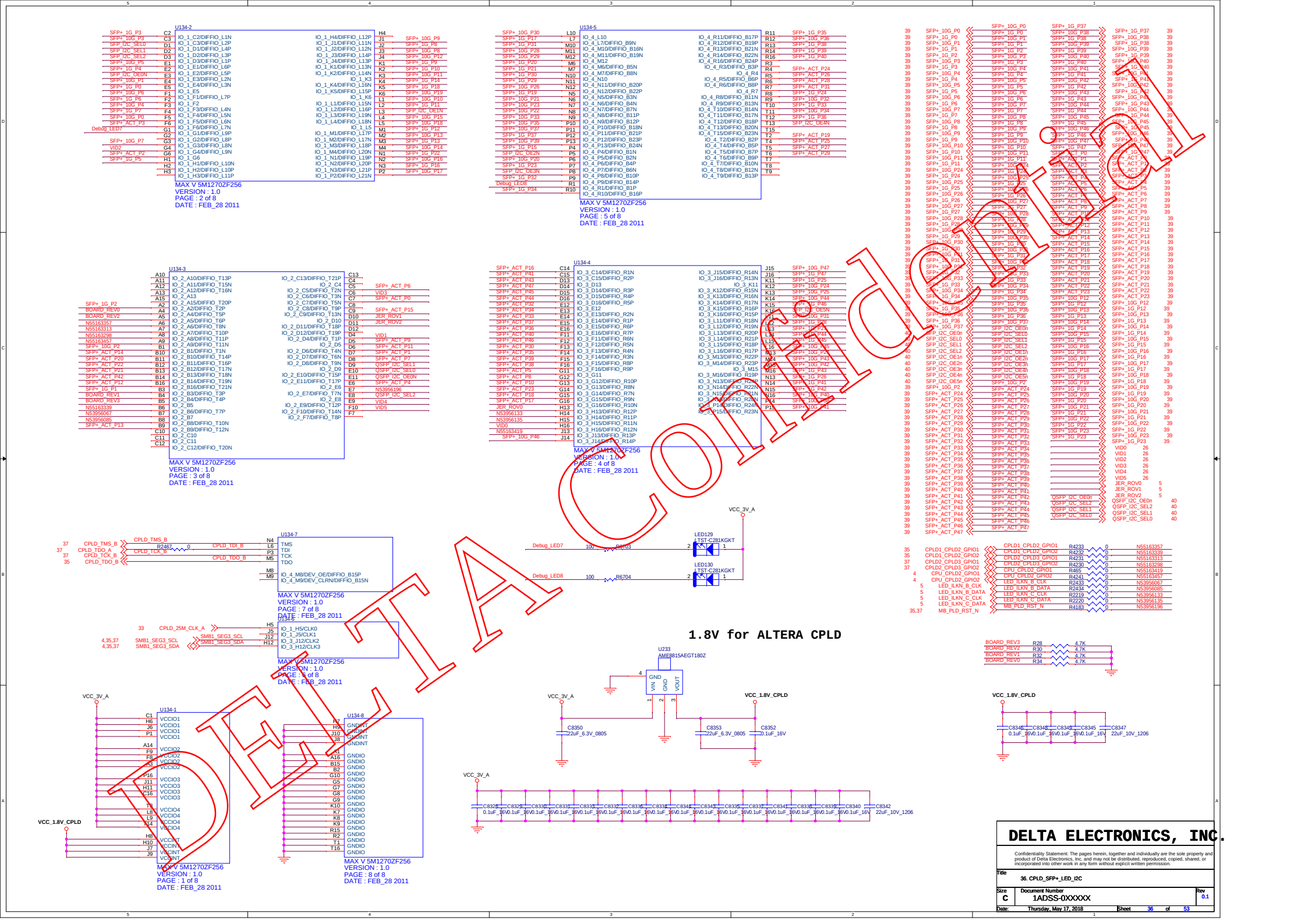
DELTA ELECTRONICS, INC.			
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.			
Title: 34. CLK_2 [100MHz & 156.25MHz]			
Size: C	Document Number: 1ADSS-0XXXXX		Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 34 of 53		

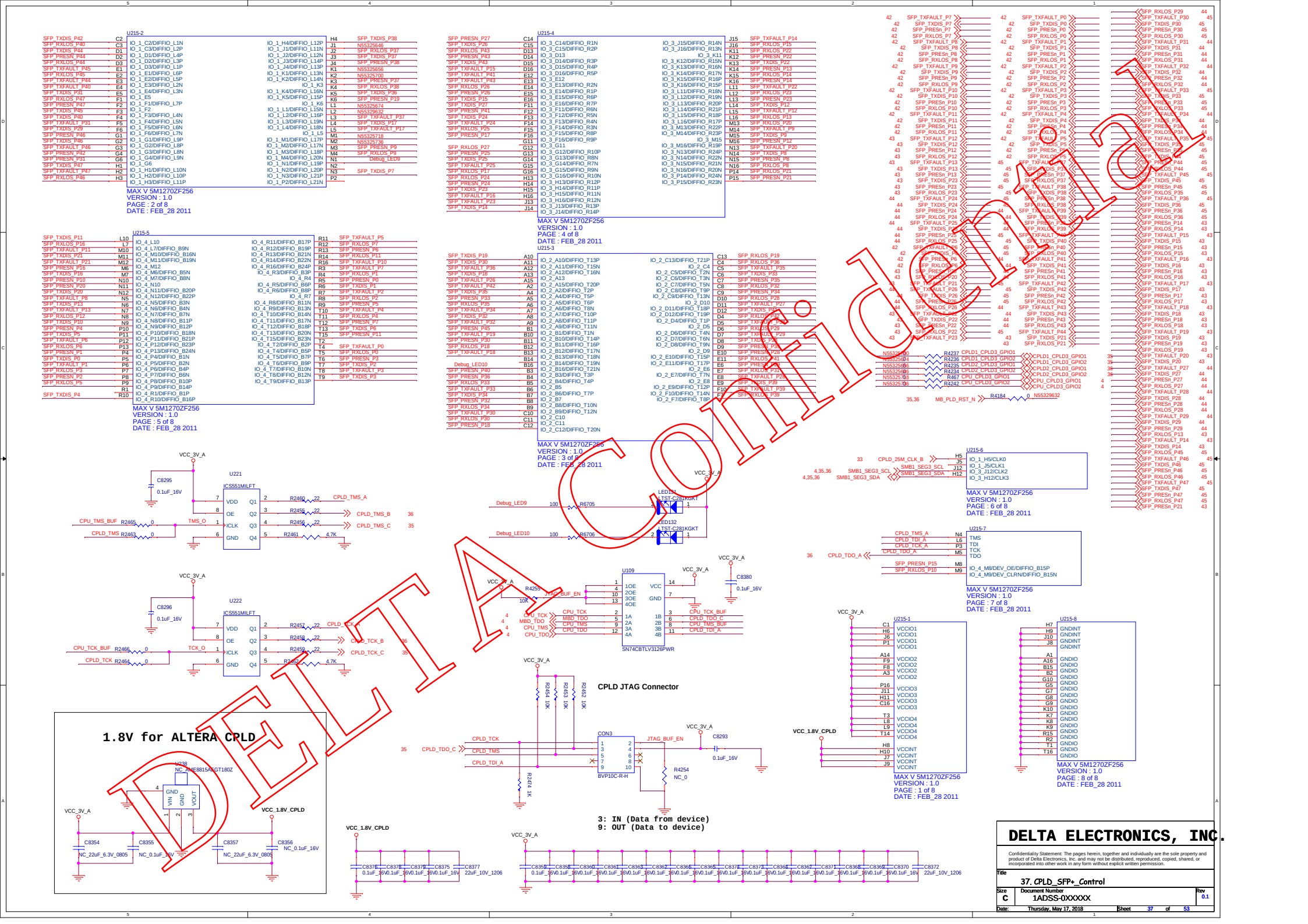
DELTA ELECTRONICS, INC.

Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.

Title	35. CPLD_SYS_QSFP*	
Size: D	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 35 of 53	

1ADFS-020018 REV:01


U134-2
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 2 of 8
DATE : FEB_28 2011
U134-5
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 5 of 8
DATE : FEB_28 2011
U134-3
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 3 of 8
DATE : FEB_28 2011
U134-4
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 4 of 8
DATE : FEB_28 2011
U134-7
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 7 of 8
DATE : FEB_28 2011
U134-6
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 6 of 8
DATE : FEB_28 2011
1.8V for ALTERA CPLD
U233
AME8815AEGT180Z
U134-1
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 1 of 8
DATE : FEB_28 2011
U134-8
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 8 of 8
DATE : FEB_28 2011
VCC_3V_A
VCC_1.8V_CPLD
DELTA ELECTRONICS, INC.
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.
Title
36. CPLD_SFP+_LED_I2C
Size C
Document Number 1ADSS-0XXXXX
Rev 0.1
Date: Thursday, May 17, 2018
Sheet 36 of 53


U215-2
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 2 of 8
DATE : FEB_28 2011
U215-4
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 4 of 8
DATE : FEB_28 2011
U215-5
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 5 of 8
DATE : FEB_28 2011
U215-3
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 3 of 8
DATE : FEB_28 2011
U215-6
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 6 of 8
DATE : FEB_28 2011
U215-7
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 7 of 8
DATE : FEB_28 2011
U215-1
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 1 of 8
DATE : FEB_28 2011
U215-8
MAX V 5M1270ZF256
VERSION : 1.0
PAGE : 8 of 8
DATE : FEB_28 2011
U221
U222
ICS551MILFT
U109
SN74CBTLV3126PWR
CPLD JTAG Connector
1.8V for ALTERA CPLD
U238
NC_AME8815AEGT180Z
3: IN (Data from device)
9: OUT (Data to device)
DELTA CONFIDENTIAL
DELTA ELECTRONICS, INC.
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.
Title
37. CPLD_SFP+_Control
Size C
Document Number 1ADSS-0XXXXX
Rev 0.1
Date: Thursday, May 17, 2018
Sheet 37 of 53

DELTA ELECTRONICS, INC.

Title: 38. LED Decode & Array ILKN A

Size	Document Number	Rev
C	1ADSS-0XXXXX	0.1

Date: Thursday, May 17, 2018 Sheet 38 of 53

DELTA ELECTRONICS, INC.

Title

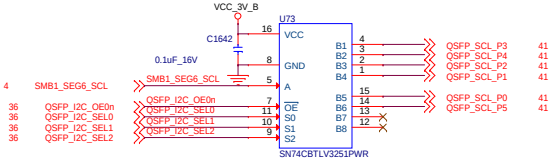
39. LED Decode & Array ILKN B&C

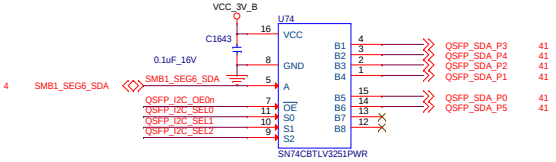
Size	Document Number	Rev
C	1ADSS-0XXXXX	0.1

Date: Thursday, May 17, 2018 Sheet 39 of 53

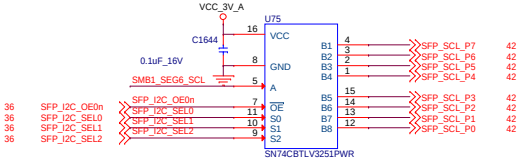
SMB1_SEG3 I2C BUS for zQSFP+ CAGE

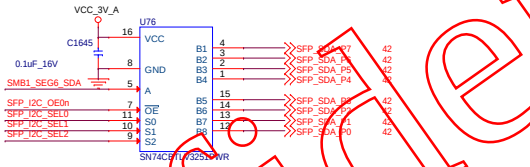
DESIGN NOTE !!!
All I2C addresses are set as 7-bit

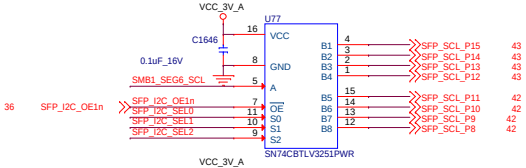


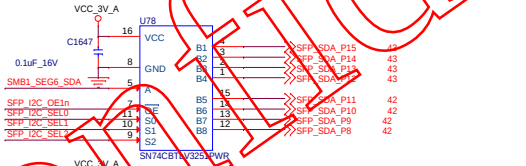


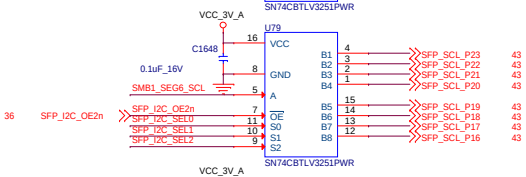
SMB1_SEG4 I2C BUS for SFP+ CAGE

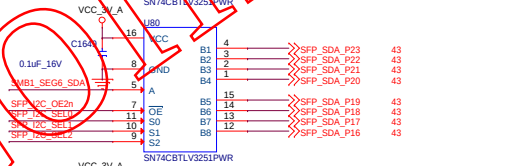


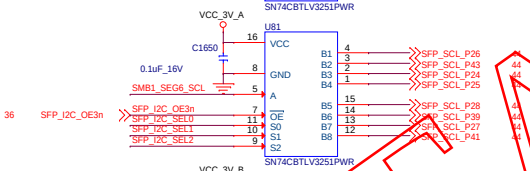


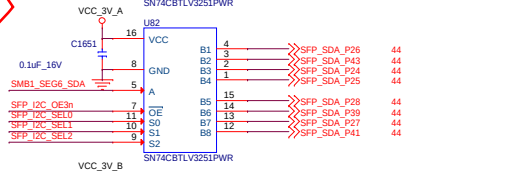


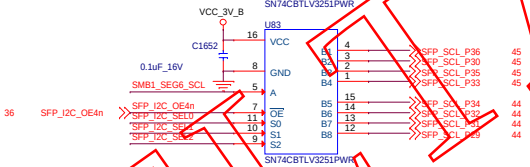


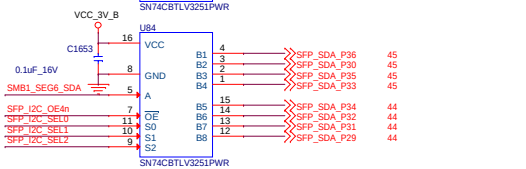


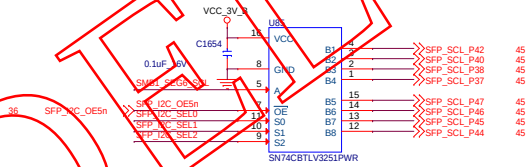


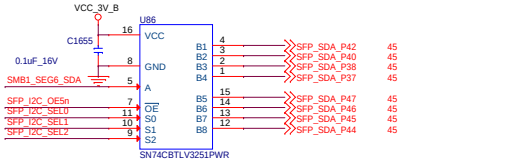






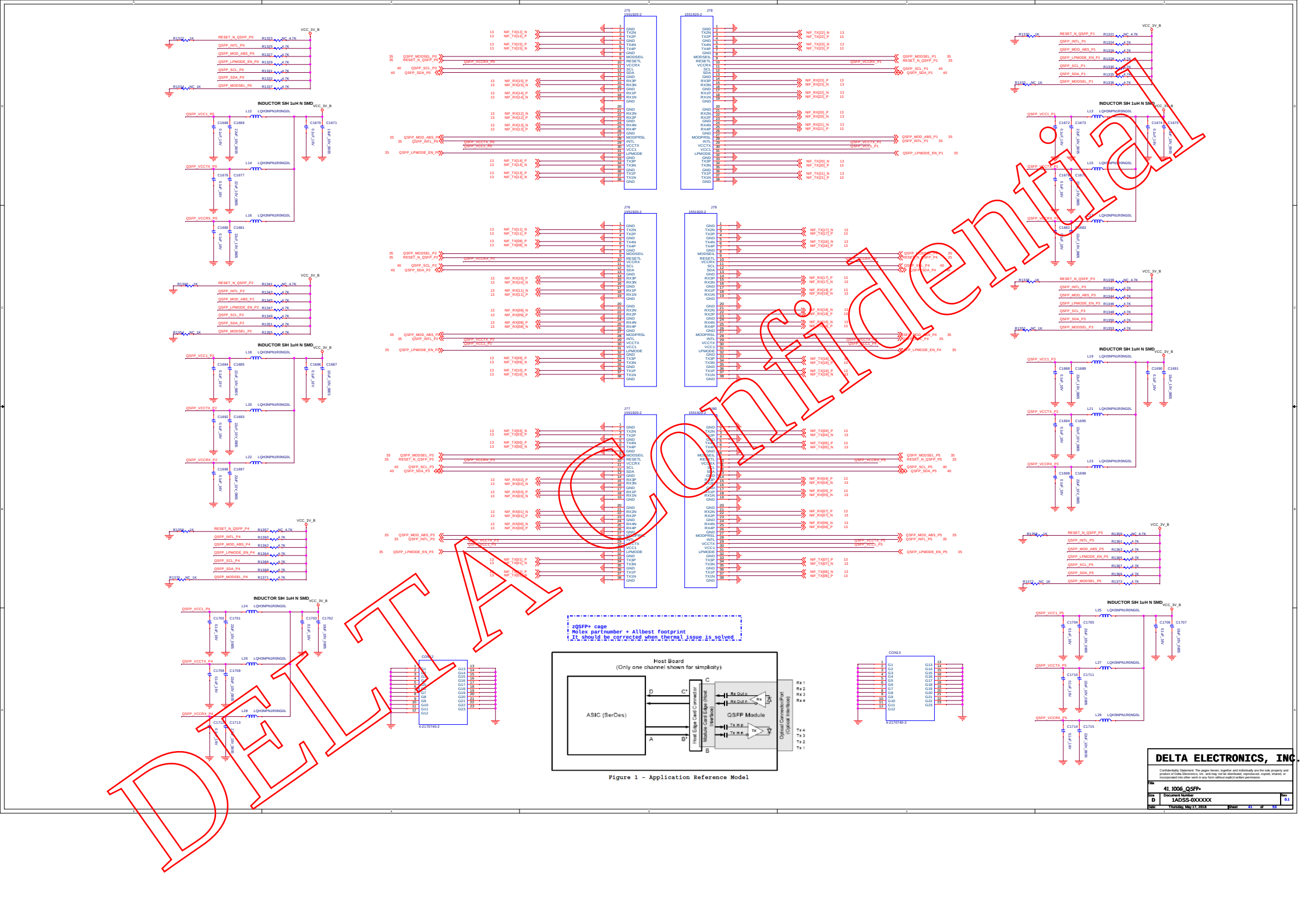


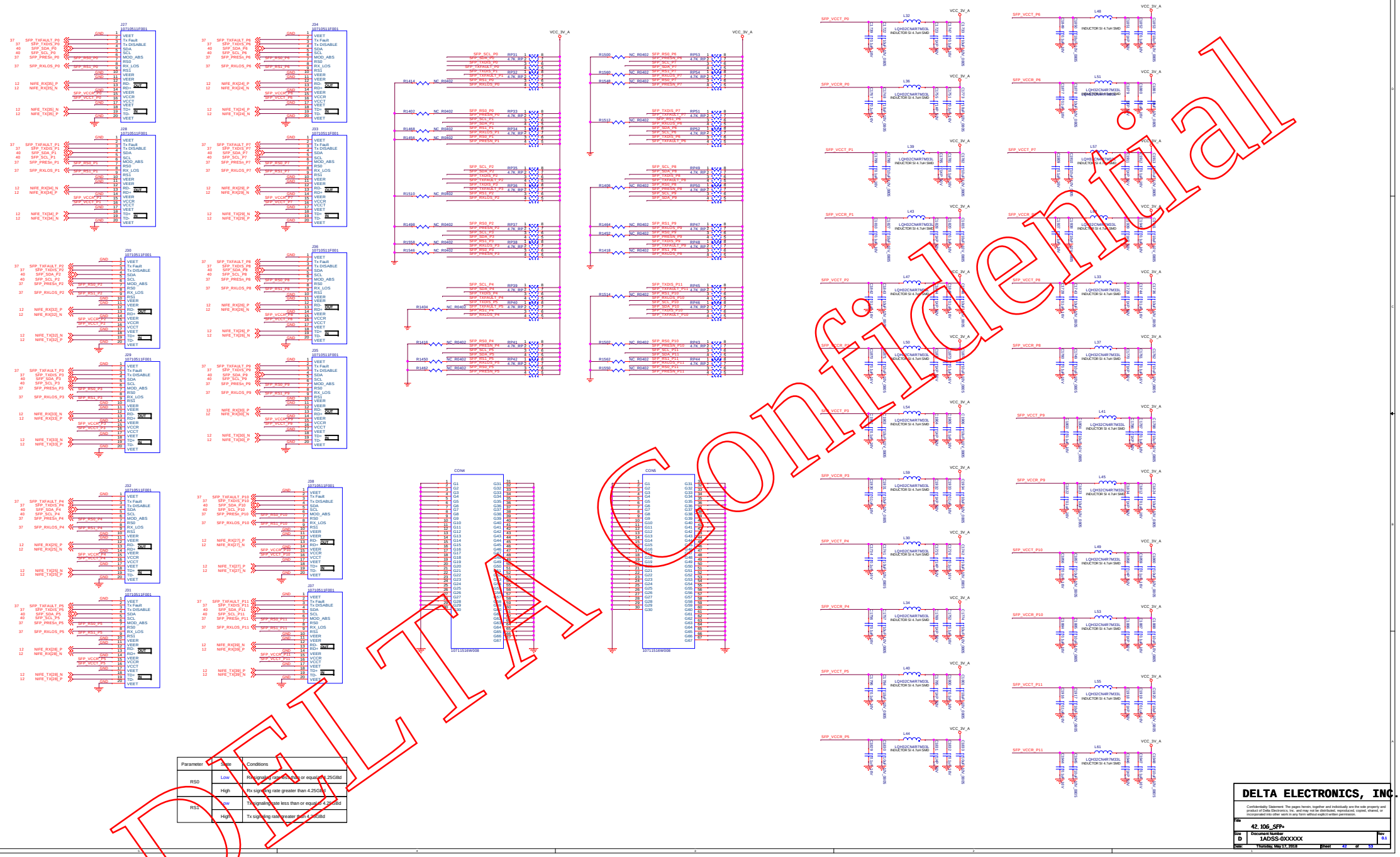




DELTA ELECTRONICS, INC.

Title	40. SFP+_QSFP_I2C	
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 40 of 53	

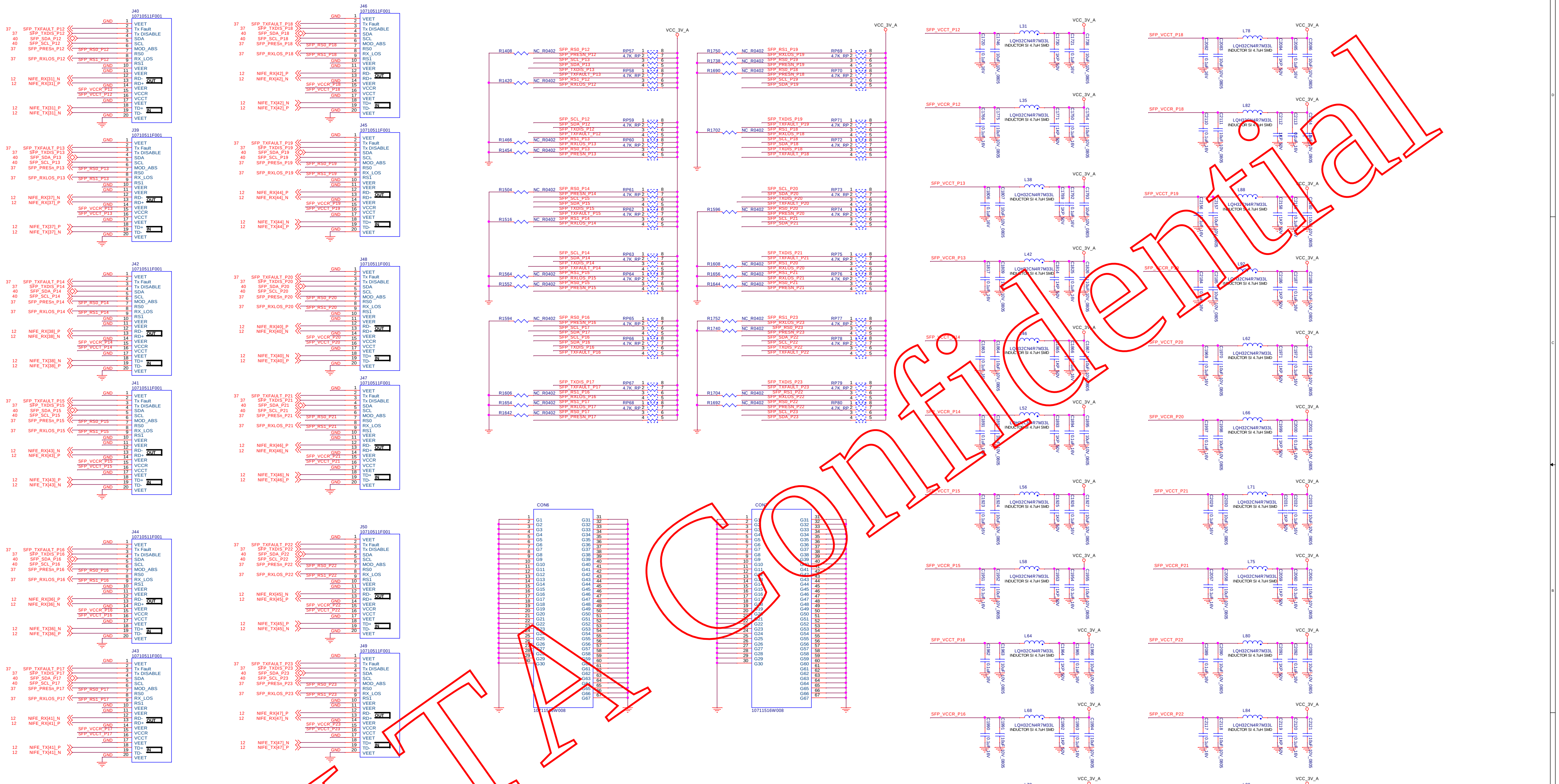

zQSFP+ cage
Molex partnumber + Allbest footprint
It should be corrected when thermal issue is solved
Host Board
(Only one channel shown for simplicity)
ASIC (SerDes)
Host Edge Card Connector
(Module Card Edge (Host Interface))
QSFP Module
Optical Connector/Port
(Optical Interface)
Figure 1 - Application Reference Model
DELTA ELECTRONICS, INC.
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.
41.1006_QSFP+
1ADSS-0XXXXX
Thursday, May 17, 2018
41 of 53
Confidential



Parameter	State	Conditions
RS0	Low	Rx signaling rate less than or equal to 4.25GBd
	High	Rx signaling rate greater than 4.25GBd
RS1	Low	Tx signaling rate less than or equal to 4.25GBd
	High	Tx signaling rate greater than 4.25GBd

DELTA ELECTRONICS, INC.

Title	42_10G_SFP+	
Size: D	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 42 of 53	



Parameter	State	Conditions
RS0	Low	Rx signaling rate less than or equal to 4.25GBd
	High	Rx signaling rate greater than 4.25GBd
RS1	Low	Tx signaling rate less than or equal to 4.25GBd
	High	Tx signaling rate greater than 4.25GBd

DELTA ELECTRONICS, INC.

Title: 43. 10G_SFP+		
Size: D	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 43 of 53	

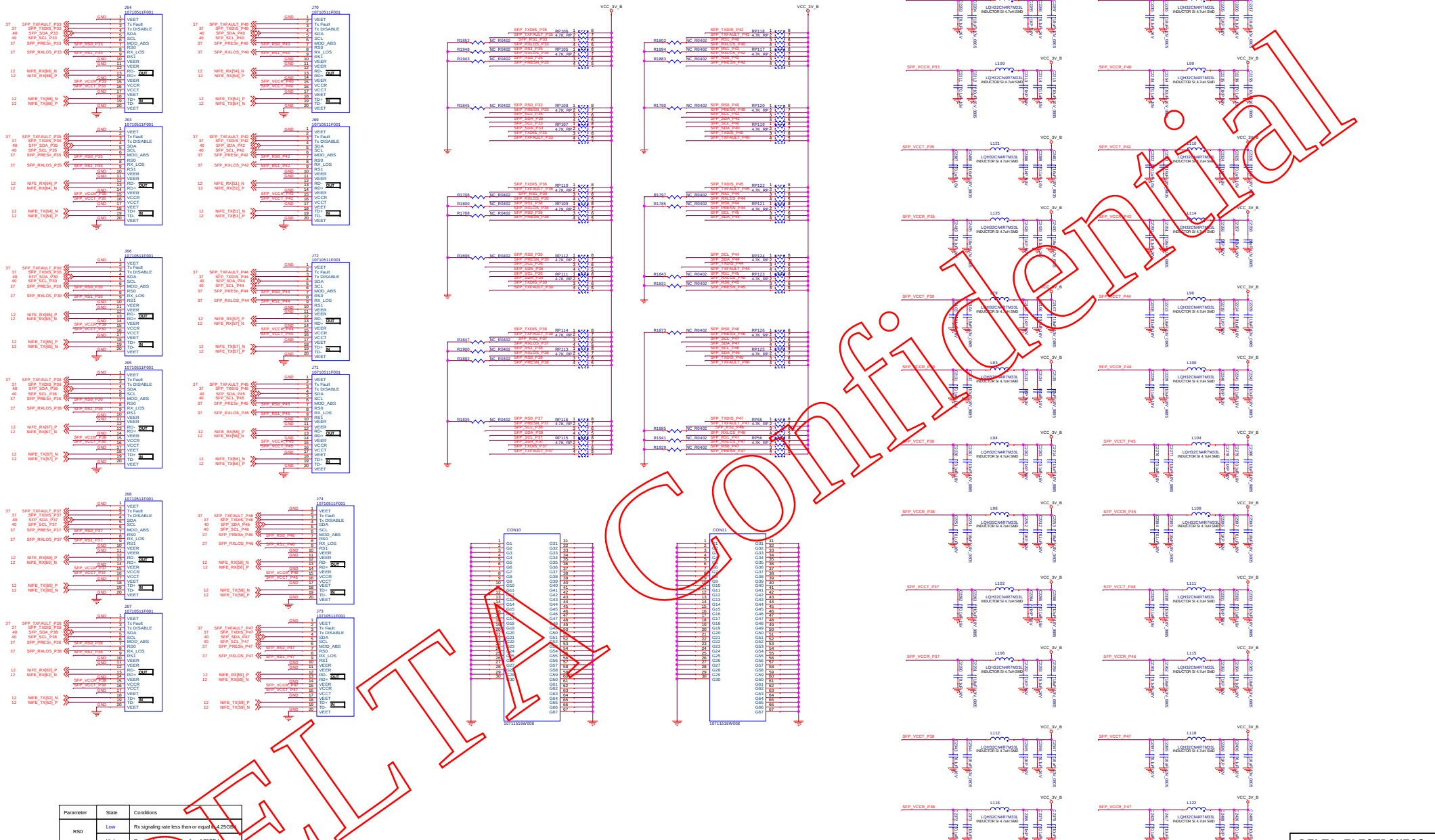
DELTA ELECTRONICS, INC.

Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.

Title: 44.10G_SFP+

Size: D | Document Number: 1ADSS-0XXXXX | Rev: 0.1

Date: Thursday, May 17, 2018 | Sheet 44 of 53



Parameter	State	Conditions
RS0	Low	Rx signaling rate less than or equal to 4.25GBd
	High	Rx signaling rate greater than 4.25GBd
RS1	Low	Tx signaling rate less than or equal to 4.25GBd
	High	Tx signaling rate greater than 4.25GBd

DELTA ELECTRONICS, INC.

Title	45_10G_SFP+	
Size: D	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 45 of 53	

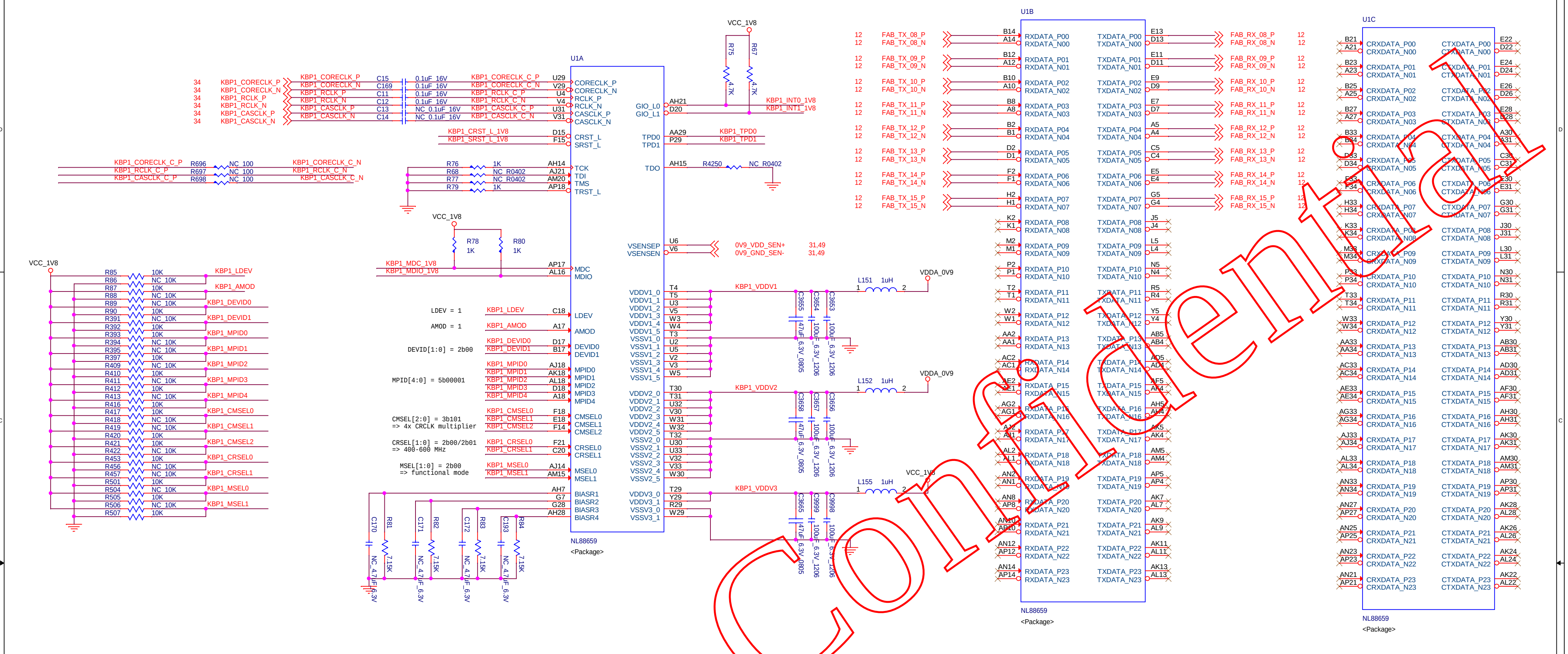


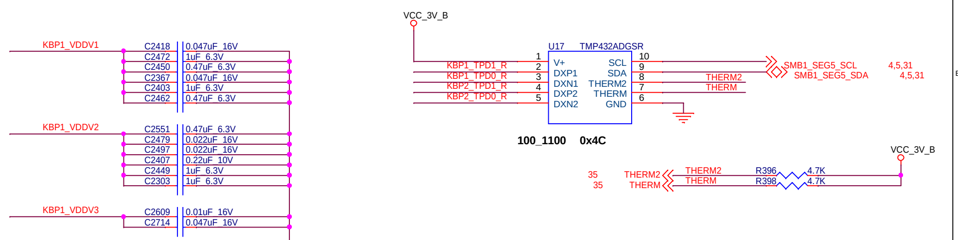
Table 360: Reference Clock Specifications

Name	Description	Min.	Nom.	Max.	Units
f_{REF}	Reference clock frequency	–	156.25 [a]	–	MHz
f_{TOL}	Reference clock frequency tolerance	–100	–	100	ppm
$t_{R,REF}$, $t_{F,REF}$	Reference clock 20% - 80% rise/fall time	–	–	600	ps
$Ref_{DutyCyc}$	Reference clock duty cycle	–10	–	+10	%
$V_{SW,REF}$	Reference clock voltage swing (differential, peak-to-peak)	0.4	–	1.6	V
θREF	Reference clock integrated phase noise[b]	-	–	1	ps_{RMS}

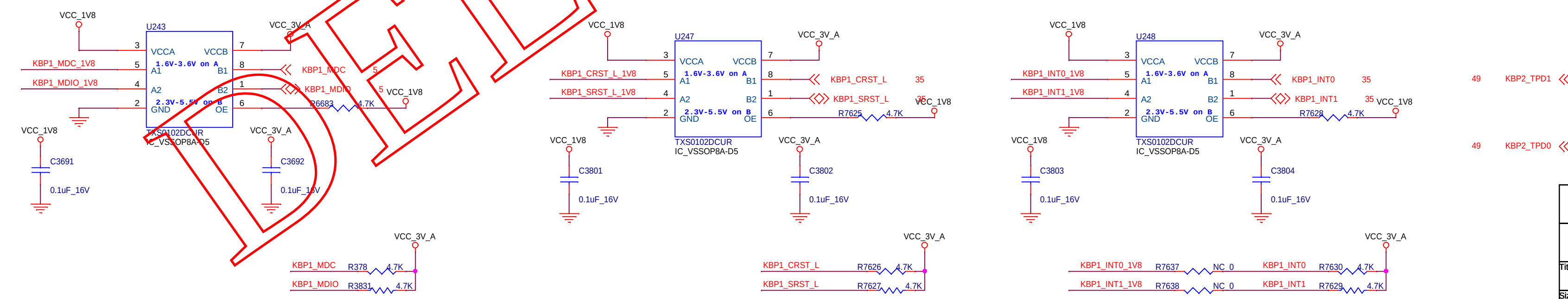
a. For RCLK and CASCLK only. For CORECLK, $f_{REF\text{-}MIN}$ = 75 MHz and $f_{REF\text{-}MAX}$ = 600 MHz.
b. Integrated from 12 kHz to 20 MHz

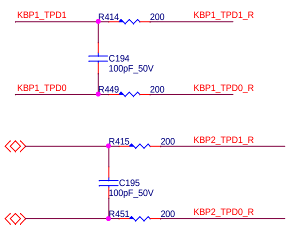
Table 20: Clock, Configuration, and Reset Pin Descriptions

Parameter	Symbol	Type	No. Pins	Description
Core Frequency Mode Select	CMSEL[2:0]	I	3	Determines core frequency operating mode of PLLs. These are static signals which are used to select the core operating frequency mode for the on-chip PLL. This field is encoded as follows: CMSEL[2:0] = 3'b011 = Core clock is equal to CORECLK. CMSEL[2:0] = 3'b100 = Core clock is equal to 2x CORECLK. CMSEL[2:0] = 3'b101 = Core clock is equal to 4x CORECLK. CMSEL[2:0] = 3'b110 = PLL Bypass Mode (Debug Only). All other combinations are reserved. Connection to these input pins is required. These pins do not have On Die Termination (ODT).



MDC MDIO
Need 1.8V device or Level shift





1ADFS-020018 REV:01

DELTA ELECTRONICS, INC.

Title: 46. KBP1_Configuration_Serdes
Size: C | Document Number: 1ADSS-0XXXXX | Rev: 0.1
Date: Thursday, May 17, 2018 | Sheet 46 of 53

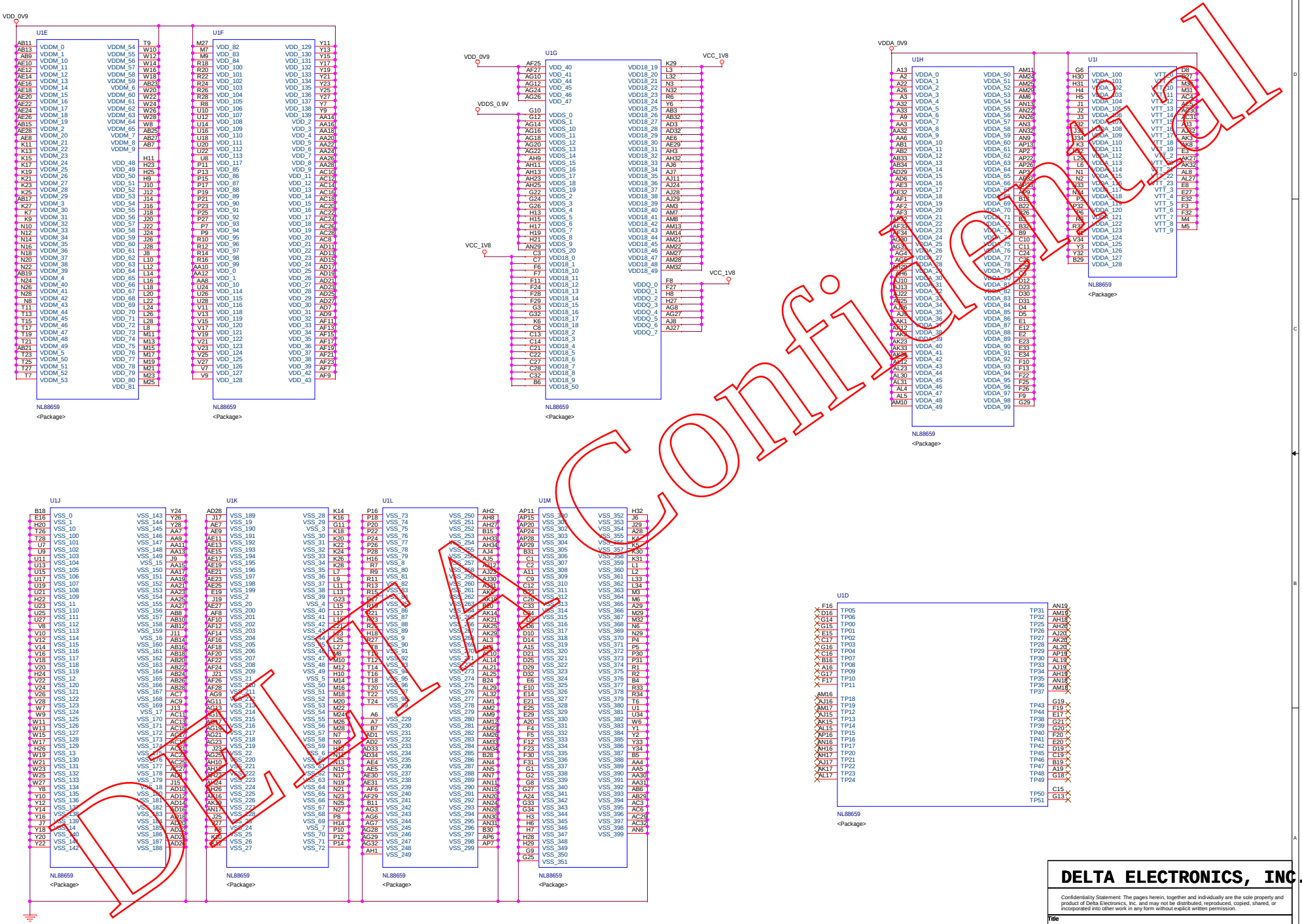
DELTA ELECTRONICS, INC.

Title: 47. KBP1_Power decoupling

Size	Document Number	Rev
C	1ADSS-0XXXXX	0.1

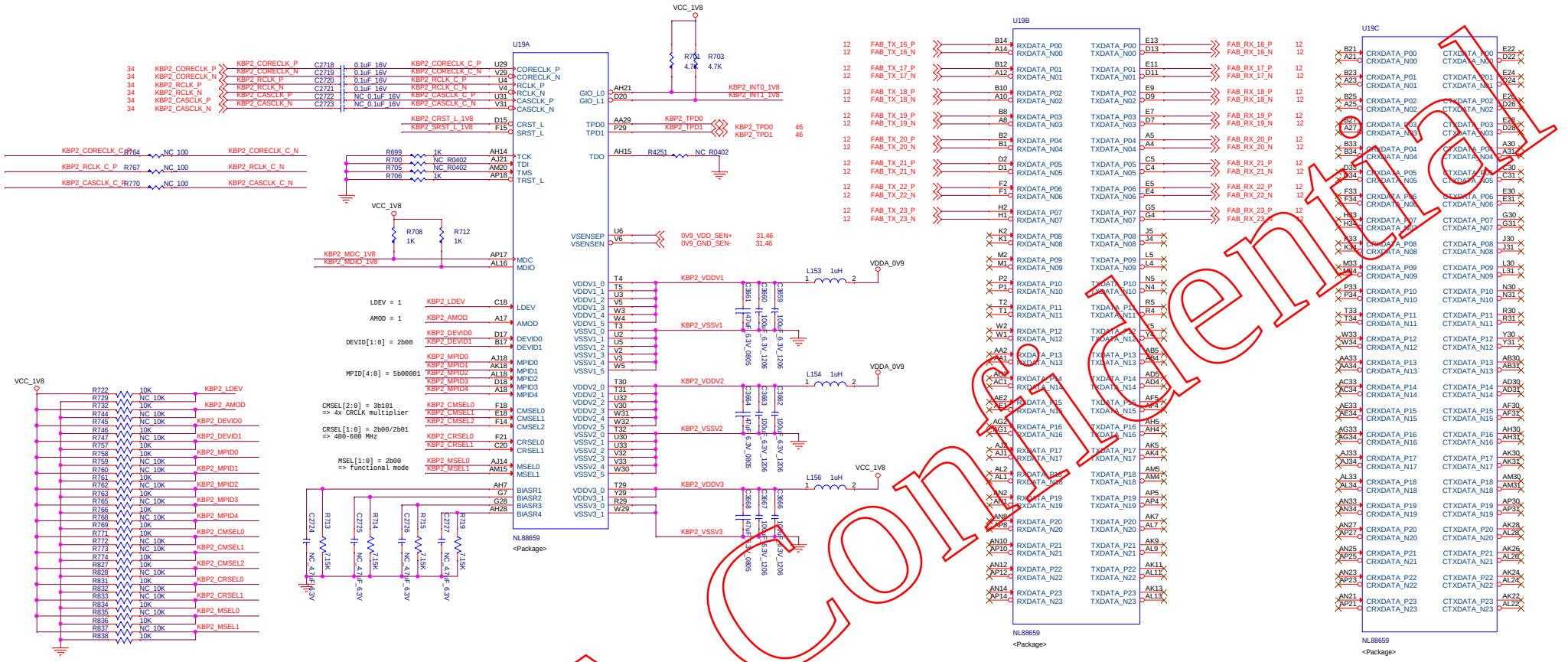
Date: Thursday, May 17, 2018 Sheet 47 of 53

03 Voltage Rails



DELTA ELECTRONICS, INC.

Title	48. KBP1_Power_GND	
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 48 of 53	



MDC MDIO
Need 1.8V device or Level shift

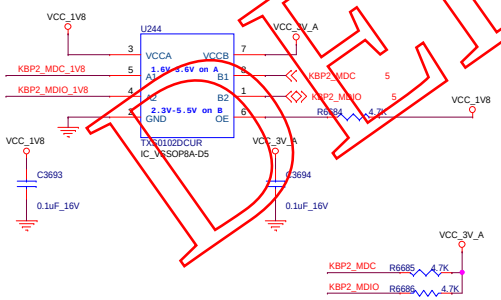


Table 360: Reference Clock Specifications

Name	Description	Min.	Nom.	Max.	Units
f_{REF}	Reference clock frequency	–	156.25 [a]	–	MHz
f_{TOL}	Reference clock frequency tolerance	–100	–	100	ppm
$t_{R,REF}$, $t_{F,REF}$	Reference clock 20% - 80% rise/fall time	–	–	600	ps
$Ref_{DutyCyc}$	Reference clock duty cycle	–10	–	+10	%
$V_{SW,REF}$	Reference clock voltage swing (differential, peak-to-peak)	0.4	–	1.6	V
θ_{REF}	Reference clock integrated phase noise[b]	-	–	1	ps_{RMS}

a. For RCLK and CASCLK only. For CORECLK, $f_{REF-MIN}$ = 75 MHz and $f_{REF-MAX}$ = 600 MHz.
b. Integrated from 12 kHz to 20 MHz

Table 20: Clock, Configuration, and Reset Pin Descriptions

Parameter	Symbol	Type	No. Pins	Description
Core Frequency Mode Select	CMSEL[2:0]	I	3	Determines core frequency operating mode of PLLs. These are static signals which are used to select the core operating frequency mode for the on-chip PLL. This field is encoded as follows: CMSEL[2:0] = 3'b011 = Core clock is equal to CORECLK. CMSEL[2:0] = 3'b100 = Core clock is equal to 2x CORECLK. CMSEL[2:0] = 3'b101 = Core clock is equal to 4x CORECLK. CMSEL[2:0] = 3'b110 = PLL Bypass Mode (Debug Only). All other combinations are reserved. Connection to these input pins is required. These pins do not have On Die Termination (ODT).

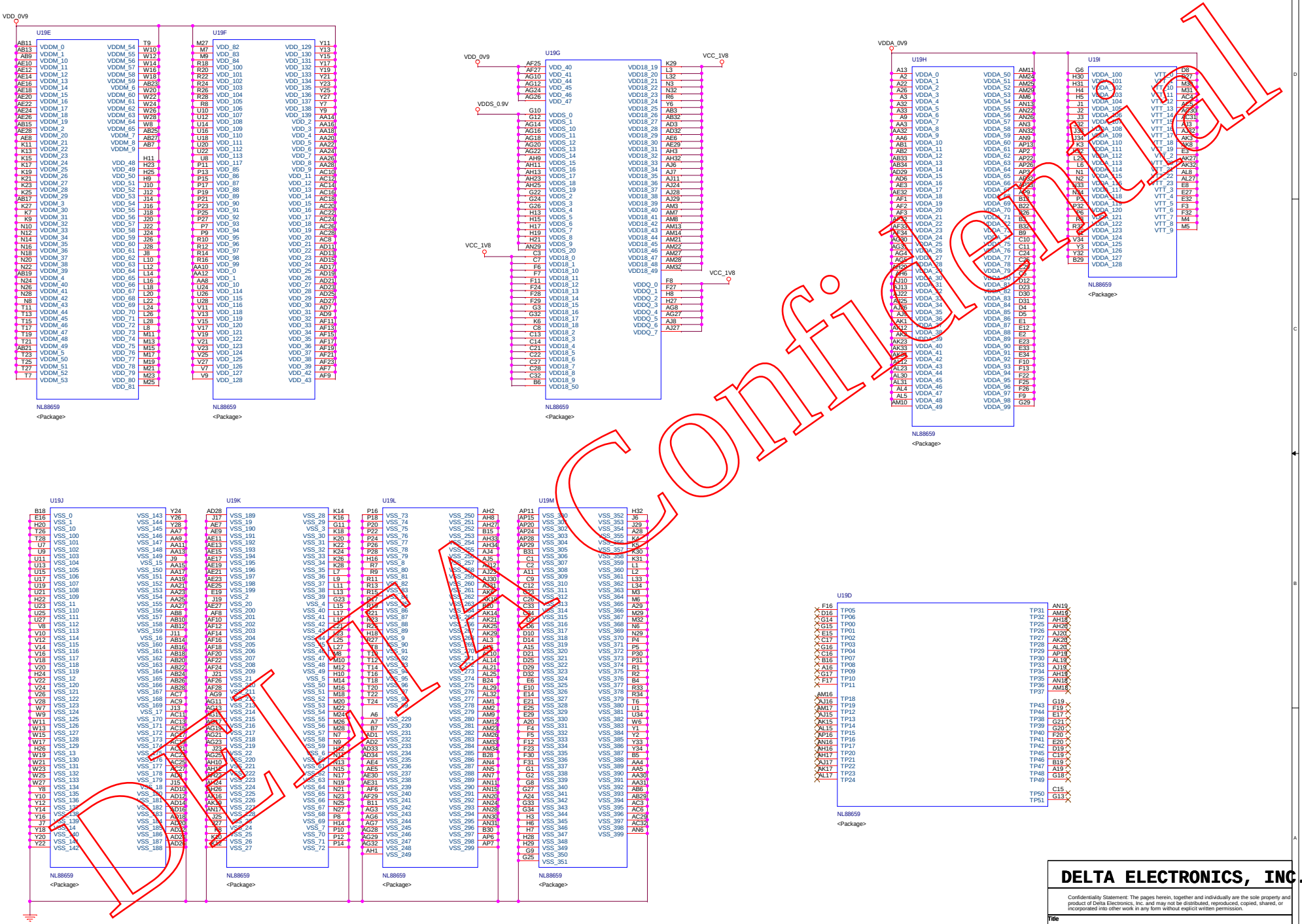
Title	49. KBP2_Configuration_Serdes
Size	C
Document Number	1ADSS-0XXXXX
Rev	0.1
Date:	Thursday, May 17, 2018
Sheet	49 of 53

DELTA ELECTRONICS, INC.

1ADFS-020018 REV:01

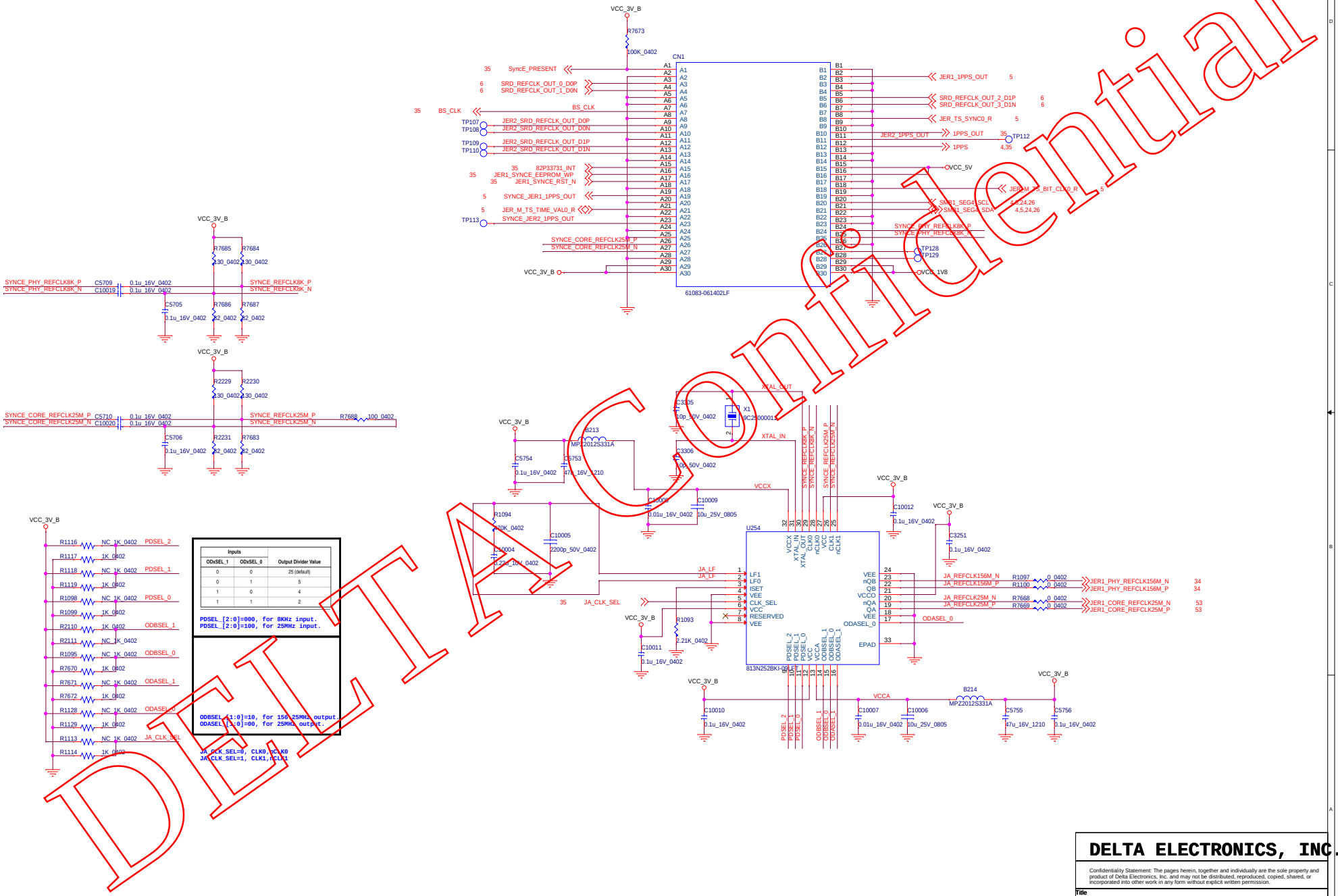
DELTA ELECTRONICS, INC.			
Confidentiality Statement: The pages herein, together and individually are the sole property and product of Delta Electronics, Inc. and may not be distributed, reproduced, copied, shared, or incorporated into other work in any form without explicit written permission.			
Title: 50. KBP2_Power decoupling			
Size: C	Document Number: 1ADSS-0XXXXX		Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 50 of 53		

O3 Voltage Rails



DELTA ELECTRONICS, INC.

Title	51. KBP2_Power_GND
Size	C
Document Number	1ADSS-0XXXXX
Rev	0.1
Date:	Thursday, May 17, 2018
Sheet	51 of 53



DELTA ELECTRONICS, INC.

Title	52. CLK [SyncE / 1588]	
Size: C	Document Number: 1ADSS-0XXXXX	Rev: 0.1
Date: Thursday, May 17, 2018	Sheet 52 of 53	

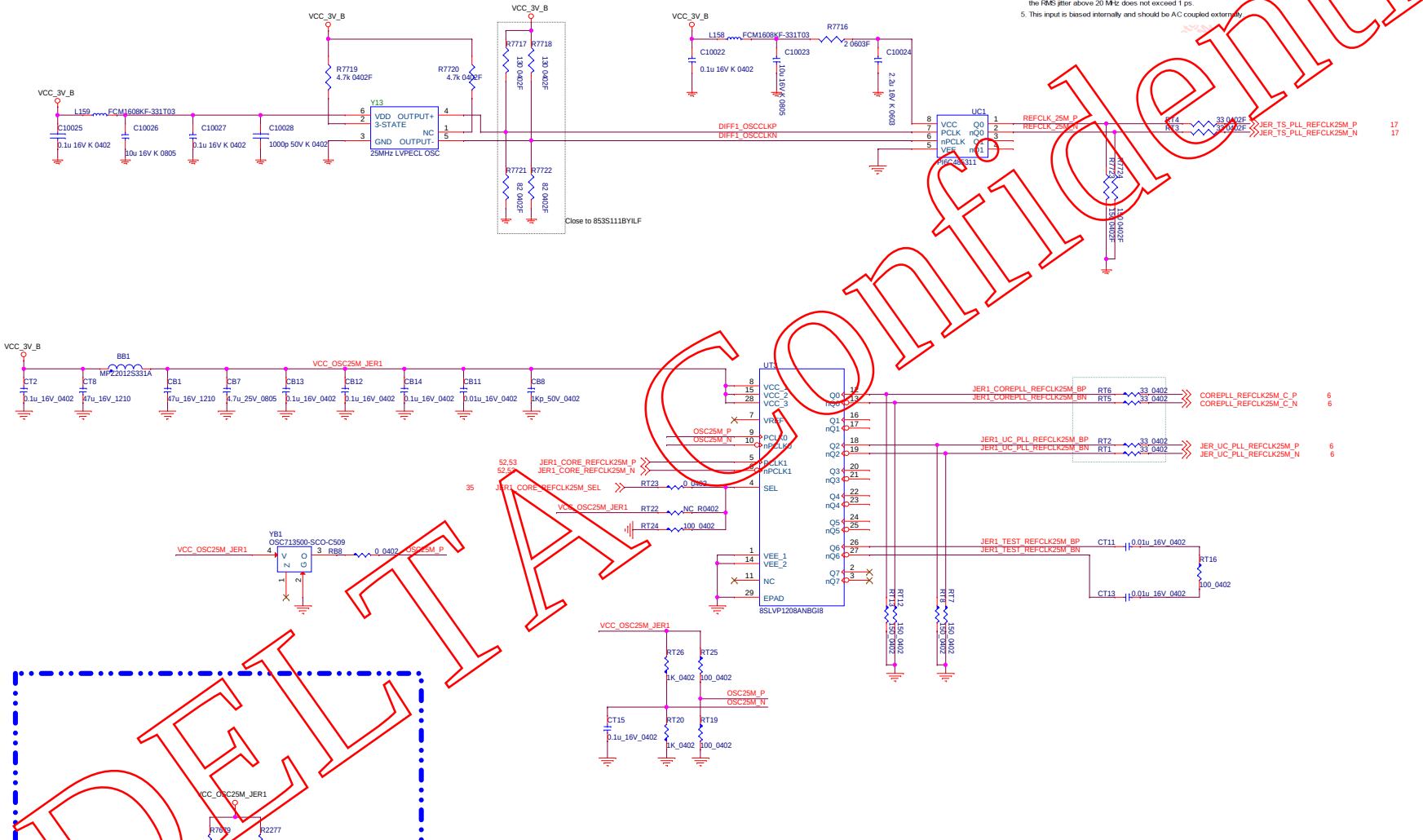
Table 46: Differential Reference Clock Characteristics

Description	Symbol	Min	Max	Units	Notes
Input clock frequency	fCK	156.25		MHz	-
Input clock accuracy	-	-100	100	ppm	-
Input clock duty cycle	DCrefclk	0.4	0.6	tCK	-
Input clock differential slew rate	SRrefclk	1.0	-	V/ns	1
Input clock common voltage	VCMrefclk	See note #5		V	5
Input resistance	RIN	80	120	Ohm	-
Input clock differential voltage (peak-to-peak)	VDIFrefclk	600	-	mV	-
Input clock single-ended voltage	VSErefclk	-0.3	AVDD + 0.3	V	-
RMS phase jitter	tJRMS	-	1.0	ps	2
Broadband jitter (RMS)	tJBRMS	-	3.0	ps	3,4

Notes:

General Comment: tCK = 1/fCK.

1. Differential Slew -Rate defined from -200 mV to +200 mV.
2. Defined from 12 kHz to 20 MHz.
3. For example, the peak-to-peak random jitter, with less than 1e-12 probability of being exceeded, is 14.07 times tJBRMS.
4. To limit the high frequency jitter content, Marvell recommends that the RMS jitter above 20 MHz does not exceed 1 ps.
5. This input is biased internally and should be A.C coupled externally.



1ADFS-020018 REV:01

DELTA ELECTRONICS, INC.

Title: 53. CLK_1 [25MHz & 100MHz]

Size: C | Document Number: 1ADSS-0XXXXX | Rev: 0.1

Date: Thursday, May 17, 2018 | Sheet 53 of 53