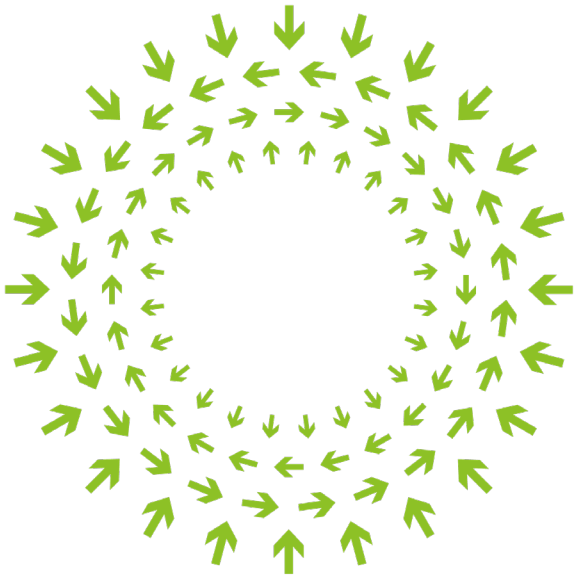

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Compute Project

Hawk Motherboard Design Specification

Revision 1.0

Author: Ampere Computing™

Date: April 22, 2020

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2. Scope

This document provides the technical specification for the Ampere Computing™ Hawk motherboard powered by Ampere's Arm® 64-bit eMAG™ 8180 multi-core processor. The Hawk board is targeted for high density telco, edge, and data center deployments. The motherboard is compatible with half-width openEDGE servers.

3. Overview

The Ampere Hawk board is an eMAG 8180-based 1U half-width single socket server board targeted for high-density telco, edge, and datacenter deployments. The board is designed to fit into the OCP openEDGE chassis.

This flexible and efficient server platform enables diverse applications requiring low latency and high data-processing capabilities for edge computing.

With a powerful and efficient 32-core eMAG 8180 processor, up to 8 DIMM slots and 4 native SATA ports that can be used to connect SATA-compliant mass storage devices with a maximum transfer rate of 6 Gb/s, this extremely flexible platform offers tremendous total cost of ownership (TCO) value with the best performance per dollar and best performance per watt to customers using high volume servers, and for customers using servers for edge, storage, and web server applications.

Two direct-connect M.2 NVMe ports on the board provide ultra-fast reads/writes while loading the OS from an NVMe drive, and reduces costs by eliminating PCIe adapters.

For network connectivity, the Hawk board provides an integrated 1 GbE port and an OCP Mezzanine card connector supporting 10/40/100 GbE NIC.

Table 1 lists the features of the Hawk board.

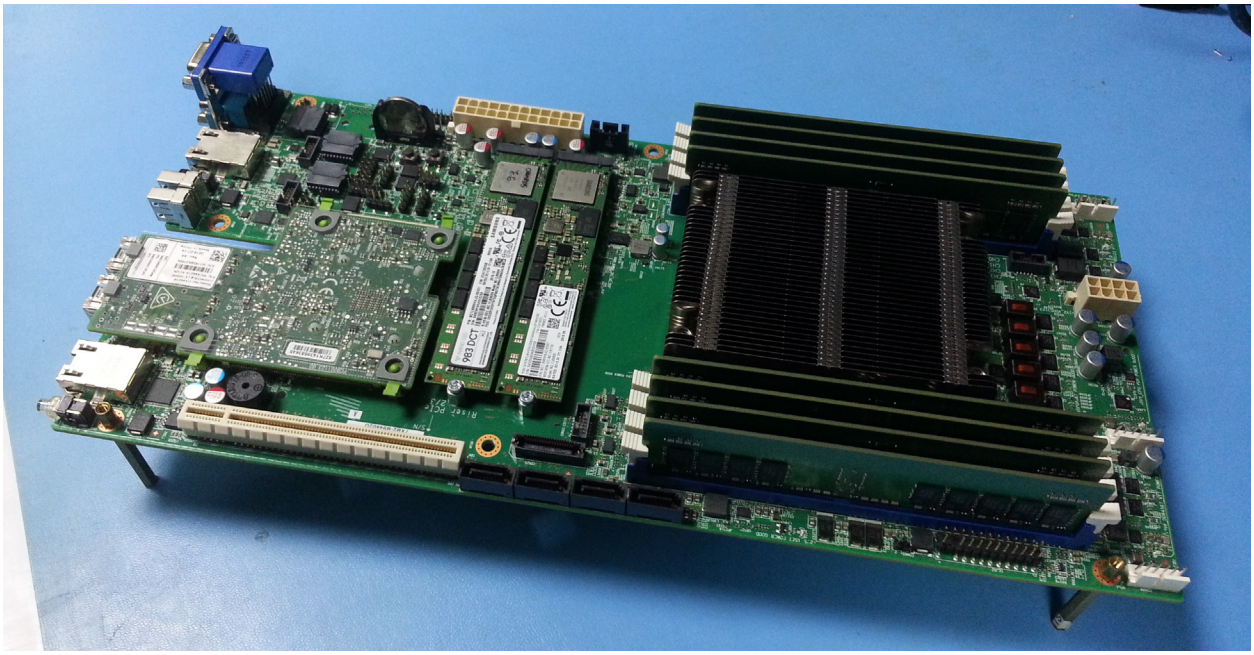
Table 1: Hawk Motherboard Features

ITEM	DESCRIPTION
Form Factor	Designed to fit into the OCP openEDGE Chassis
Number of Processors	1 x Ampere eMAG 8180 CPU with 32 x ARMv8 64-bit CPU cores at 3.30 GHz with Turbo
Memory	Up to 256 GB in 8x slots using 32 GB DIMMs; 2666 MHz DDR4 RDIMM (1DPC)
Expansion Slots	1 x PCIe x16 (PCIe 2)
Rear Panel I/O Ports	• 1 x Power Control Button • 1 x UID Button • 1 x RJ45 (BMC) • 1 x RJ45 for 1 GbE NIC • 1 x VGA (DB15) • 1 x Serial Port (DB9) • 2 x USB 2.0

ITEM	DESCRIPTION
Internal I/O Connectors	• 4 x SATA 6.0 Gb/s Connectors • 2 x NVMe M.2 (PCIe 4, 5) • 1 x OCP Mezzanine Card 2.0 (Conn. A and Conn. B) supporting 10/40/100 GbE NIC • 2 x PCIe (PCIe 0, 1) • 3 x 6-Pin Hot Plug Fan Connector supporting single/dual rotor fans • 1 x 24-pin Multi-Input ATX Power Connector • 1 x 8-pin 12 V Power Connector
Network Interfaces	• 1 x RJ45 for BMC • 1 x RJ45 for 1 GbE
System Management	IPMI 2.0, iKVM
Installed Operating System	CentOS 7.x
UEFI	AMI Aptio® V
BMC	AMI MegaRAC®
Others	GCC and LLVM tool chain bundled with latest eMAG software release
Dimensions	22.10 mm (H) × 165.1 mm (W) × 351.79 mm (D) / 0.87” (H) × 6.5” (W) × 13.85” (D)

Figure 1 shows the Hawk board with the OCP 2.0 Mezzanine Card.

Figure 1: Hawk Board with OCP 2.0 Mezzanine Card

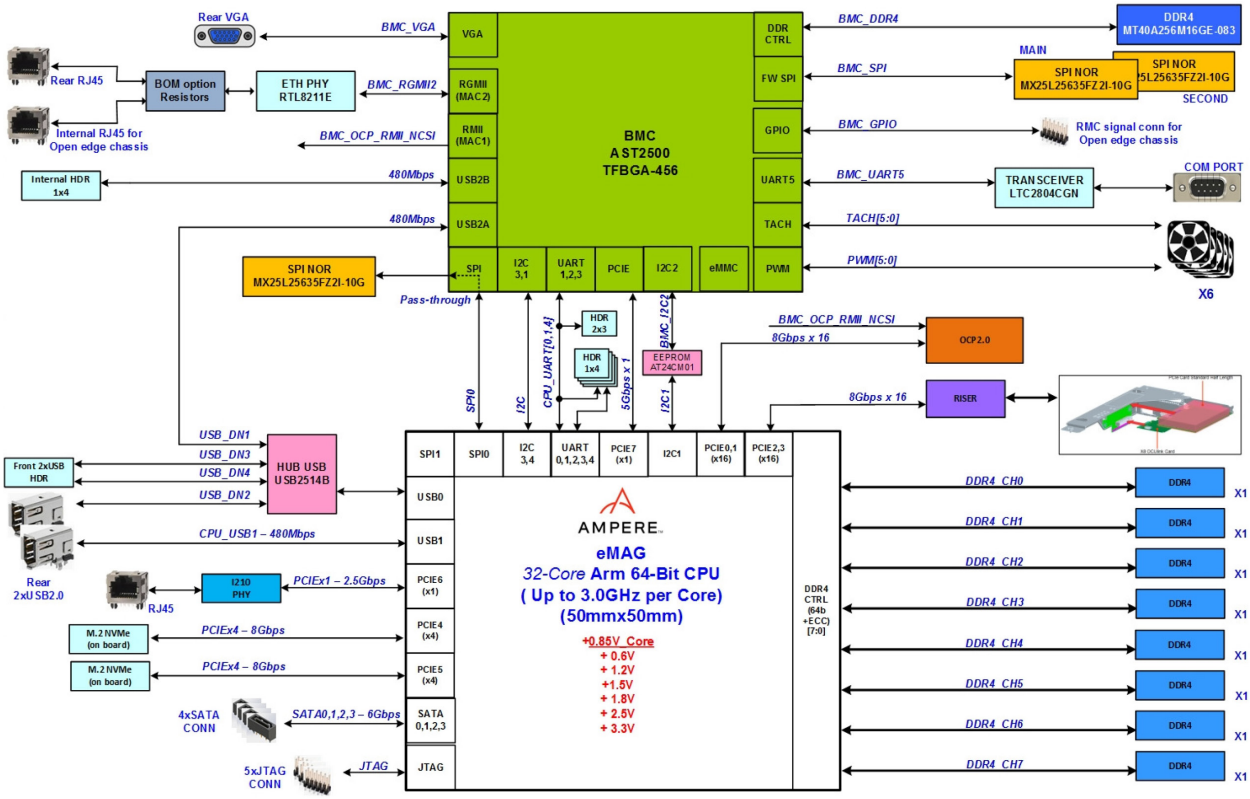


4. Overview of the Hawk Board

4.1. Block Diagram

Figure 2 illustrates the Hawk board's block diagram.

Figure 2: Hawk Board Block Diagram



4.2. Component Placement and Form Factor

The Hawk board is designed as a 6.5” × 13.85” motherboard to fit into a chassis conforming to the openEDGE Chassis Specification. *Figure 3* illustrates the Hawk board dimensions and form factor.

Figure 3: Hawk Board Form Factor

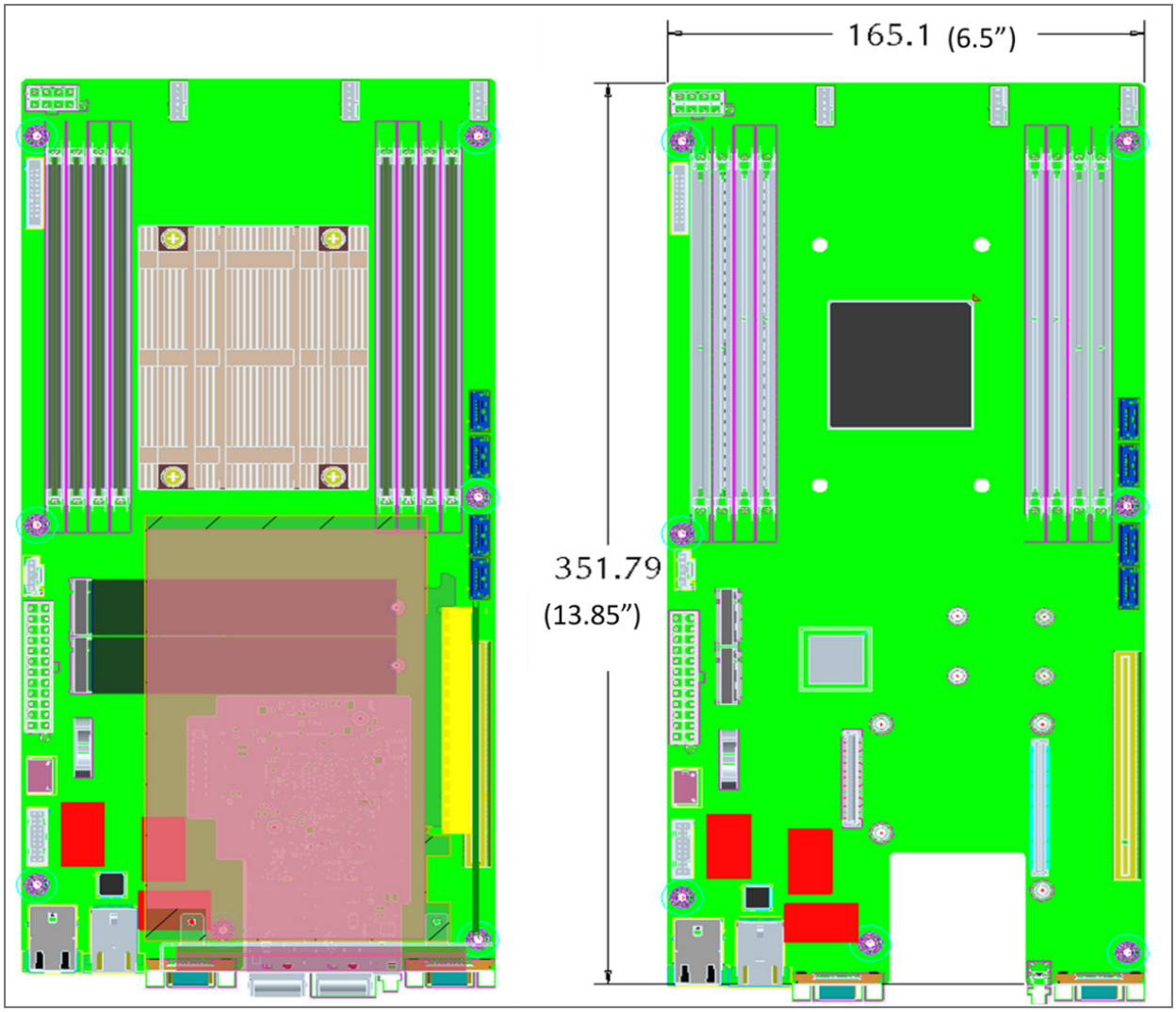


Figure 4 shows the top-view of the Hawk board.

Figure 4: Hawk Board Top-view

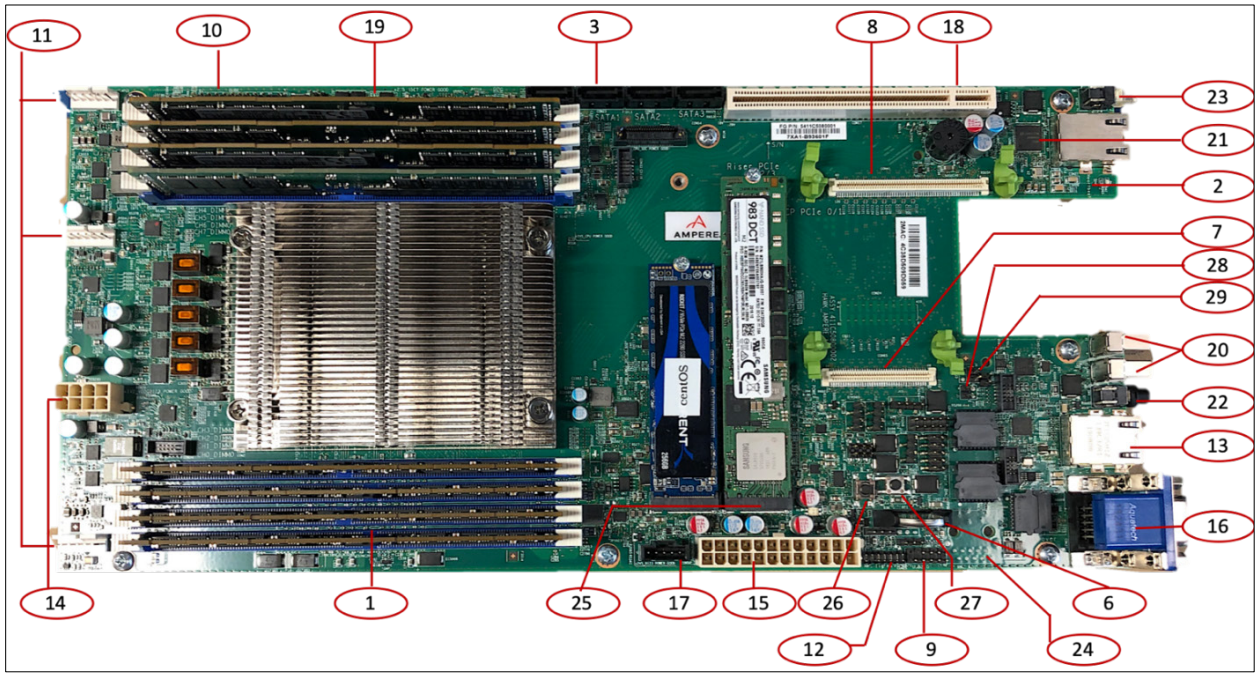


Table 2 lists the jumpers and connectors on the Hawk board shown in *Figure 4*.

Table 2: Hawk Board Jumpers and Connectors

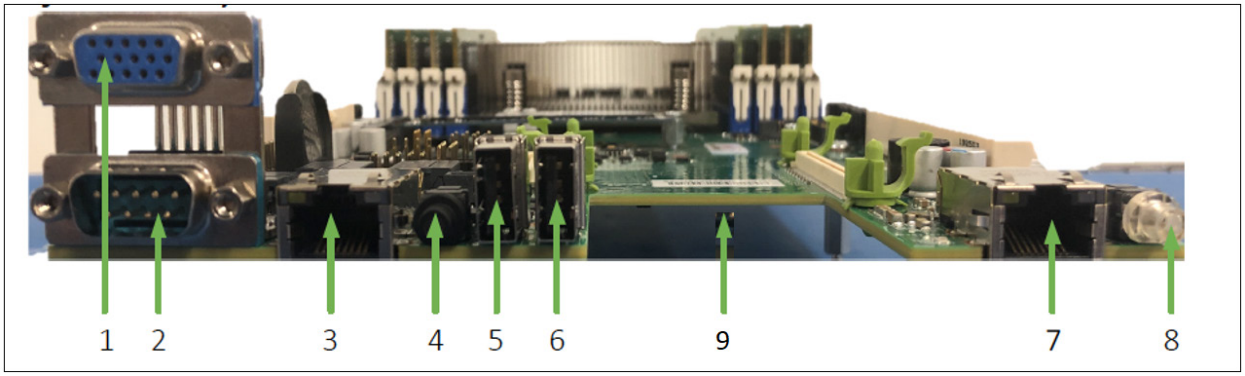
#	JUMPERS AND CONNECTORS	ITEM
1	CON2, CON4, CON6, CON8, CON10, CON12, CON14, CON16	DDR4-RDIMM (8)
2	D42	BMC (Baseboard Management Controller) heartbeat LED
3	CON21, CON22, CON23, CON54	SATA connector (4)
6	BT1	Coin-Battery
7	CON65	OCP Mezzanine 2.0 connector B
8	CON41	OCP Mezzanine 2.0 connector A
9	CON47	USB 2.0 header (front USB port)
10	CON52	Front panel IO header
11	CON68, CON69, CON70	Fan connector
12	CON67	RMC signal header (OpenEdge)
13	CON38	RJ45 management port
14	CON40	8-pin CPU power connector
15	CON39	24-pin main power Connector

#	JUMPERS AND CONNECTORS	ITEM
16	CON37	VGA and serial port DB9 connector
17	CON50	BMC ATX PMBus connector
18	CON17	Standard PCIe x16 connector
19	CON60	Intrusion sensor connector
20	CON71, CON72	USB 2.0
21	U5002	Intel Ethernet controller I210-AT and RJ45 Port
22	SW4	ID Switch/LED
23	SW5	Power Switch/LED
24	CON63[1]	RMC MDI (OpenEdge)
25	CON19, CON62	NVMe M.2 connector
26	SW2	BMC_RST# button
27	SW1	System reset button
28	J1	Power supply on
29	J4	PCIe spread spectrum

4.2.1. I/O Connectors and Switches on the Rear

Figure 5 shows the connectors and switches on the rear side of the Hawk board and *Table 3* provides the list of these connectors and switches.

Figure 5: I/O Connectors and Switches on the Rear Side of the Hawk Board



[1] CON63 may not be populated by default. For more information, contact technical support at https://connect.amperecomputing.com/help

Table 3: I/O Connector and Switches on the Rear

ITEM	DESCRIPTION	ITEM	DESCRIPTION
1	VGA Port	2	DB9 Connector (BMC Console)
3	RJ45 Management Port	4	ID Switch / LED
5	USB 2.0 (CPU)	6	USB 2.0 (USB Hub)
7	Intel I210 GbE (System Console)	8	Power Switch / LED
9	OCP 2.0 Mezzanine LAN Card	–	–

4.2.2. Hawk Board Power Connectors

The Hawk board has the following power connectors populated on-board:

- Baseboard main power connector: 24-pin Molex 44472 family equivalent
- Processor power connector: 8-pin Molex 44472 family equivalent

There are two power domains from the ATX power connector:

- ATX domain includes +12V_ATX, +5V_ATX and +3V3_ATX
- Standby domain includes +5VSB_ATX

The following are the power connections on the Hawk board:

- All +12V_ATX power pins are connected into a single 12V_ATX plane on the Hawk board
- PCIe connectors are powered by +12V_ATX and +3V3_ATX
- +5V_ATX is used for VRM regulators and USB VBUS
- +12V_ATX is used for VRM and CPU's power regulators
- +5VSB_ATX is used for BMC's power regulators

4.2.3. Hawk Board Thermal Considerations

The Hawk board requires active air flow for cooling the CPU and memory modules. It is provisioned to support 6 system fans (each operating at 12 V). BMC controls the system fan speeds via PWM, without which, the fans will run at full speed.

Hawk uses a customized LGA2011 socket heat sink, with screws and springs that are modified for use with a soldered eMAG CPU with a backplate. See section *11.3* for a list of supported heat sinks.

The Hawk board provides multiple temperature sensors and thermal measurement test points as listed below:

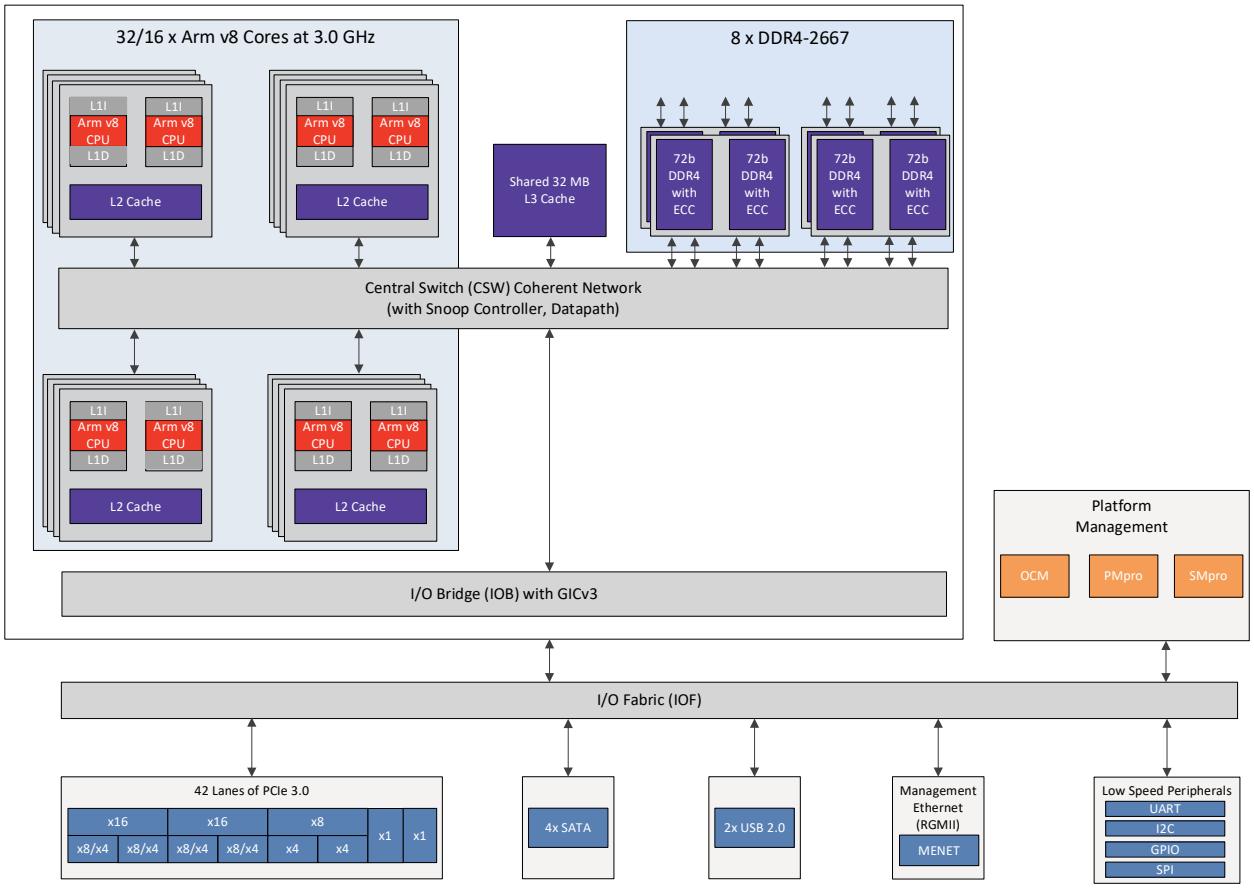
- On-die temperature sensors for the eMAG CPU
- DIMM module temperature sensors
- Motherboard temperature sensors

4.3. CPU and Memory

The Hawk board is powered by the Ampere Computing eMAG 8180 64-bit, custom designed, multi-core processor targeting today's cloud workloads and future data center requirements by providing a large number of high-performance cores, high-memory bandwidth and capacity, general purpose high-bandwidth I/O, and a high level of integration—all within an efficient power envelope.

Figure 6 shows the eMAG processor block diagram.

Figure 6: eMAG 8180 Processor Block Diagram



Processor Subsystem

- Thirty-two eMAG processor cores operating at up to 3.30 GHz with Turbo
  - Arm®v8 compliant 64-bit processor cores
  - 32 KB L1 data cache, 32 KB L1 instruction cache per core
  - Floating Point and SIMD Unit per core
- Shared 256 KB L2 cache per each pair of cores
- ECC protection on caches
- Shared 32 MB L3 cache
- Arm® Generic Interrupt Controller (GICv3)
- Four DDR4 memory controllers with ECC (72-bit)
- IO virtualization (SMMUv2)

- Enterprise server-class RAS
  - End-to-end data poisoning
  - Error containment and isolation
  - Background L3 and DRAM scrubbing

Connectivity

- 42 lanes of PCIe Gen3, with 8 controllers:
  - x16 or two x8/x4
  - x16 or two x8/x4
  - x8 or two x4
  - Two x1
- 4 x SATA Gen3 ports
- 2 x USB 2.0 ports

Other Interfaces

- Six I2C ports
- Five UARTs
- GPIOs
- Two SPI
- JTAG / Trace

Memory Subsystem

- Shared 32 MB L3 cache
- Eight DDR4-2667 channels
- ECC, Symbol-based ECC, and DDR4 RAS features
- Up to 16 DIMMs and 1 TB/socket
- Follows the updated JEDEC DDR4 specification with 288-pin DIMM socket
- Supports DDR4 protocol (1.2 V) at up to DDR4-2667 speed grade
- 72-bit DRAM interface (64 data bits and 8 ECC bits)

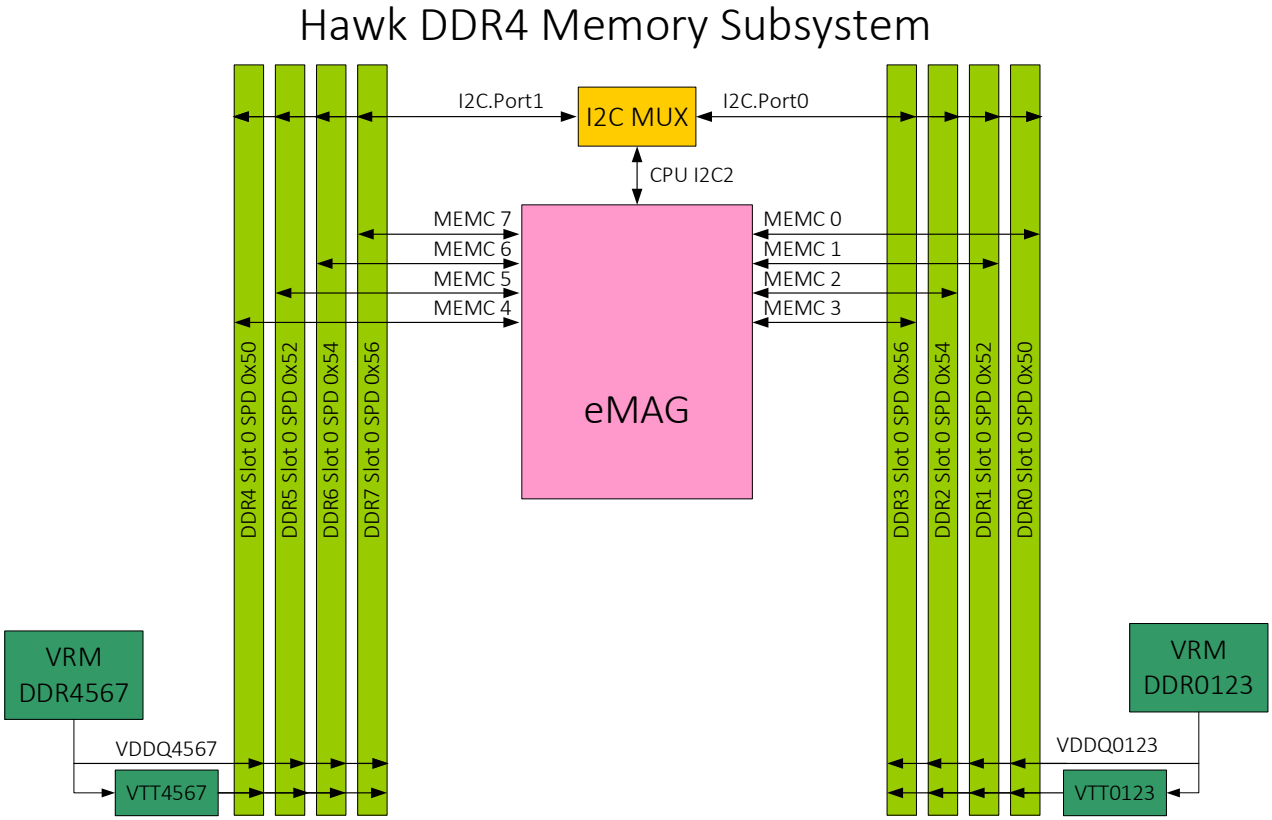
Hawk supports up to 8 x 32 GB 2667 MT DDR4 RDIMM at 1 DIMM per Channel (1DPC) configuration.

Functionality

- ARM Server Base System Architecture (SBSA) Level 3
- ARM Server Base Boot Requirements Compliant
- Advance Power Management
  - Dynamic estimation, Turbo, Voltage drop mitigation
- Two dedicated 32-bit Cortex-M3 processor (with 128 KB I/D RAM and debug port), PMpro and SMpro for power and system management, respectively.

4.3.1. DDR4 Memory Controller Architecture

Figure 7: Hawk DDR4 Functional Block Diagram



As shown in *Figure 7*, Hawk DDR4 memory subsystem comprises of 8 DDR4 memory channels each supporting a single 288-pin DDR4 DIMM socket. Total system capacity is 8 DDR4 DIMM slots with up to 256 GB of DDR4 memory using 32 GB memory modules.

Memory channels have similar functional connectivity to corresponding DIMM slots; each side has its own VTT regulator for eight DIMM slots.

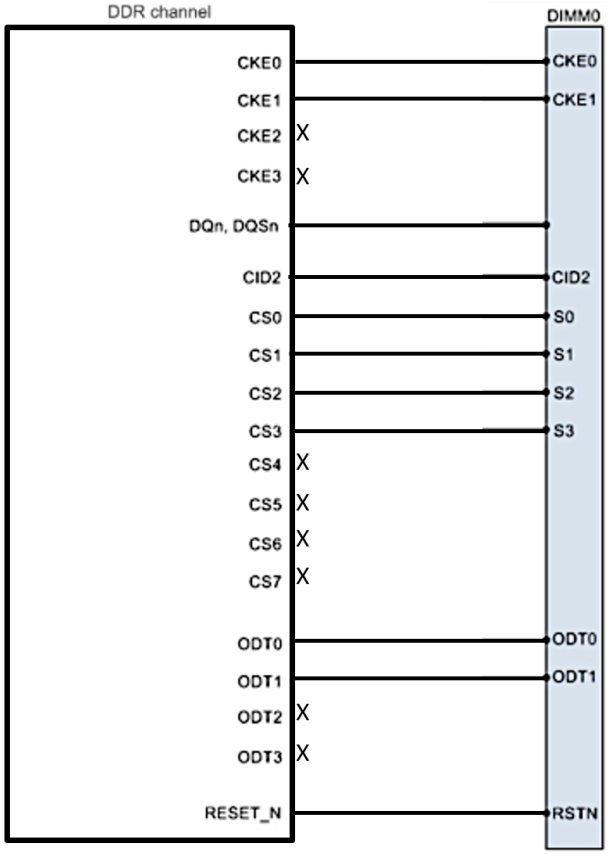
Memory channels on the right and left side of eMAG have separate power planes on the package. This plane separation is also provided on the board, so that left side DIMMs and controller pins are powered from one VRM, and right side DIMMs and controller pins from another VRM.

DIMM slot I2C bus is connected to dedicated eMAG I2C2 bus through I2C bus mux.

4.3.2. DDR4 CK, CKE, CS, and ODT Connections in Two Slot Systems

On Hawk, only one DDR slot is implemented for each memory channel. Unused DIMM1 signals (CKE2, CKE3, CS4, CS5, CS6, CS7, ODT2, ODT3, CLK2_N, CLK2_P, CLK3_N, CLK3_P) are left unconnected as shown in *Figure 8*.

Figure 8: DDR4 Memory Channel Connections to Slots on Hawk



4.4. DIMM Memory Population Sequence

Hawk supports up to eight memory channels. It also supports six, four, and two memory controller configurations, but only as per the configuration options listed in *Table 4*. Each channel provides DDR connections for one DIMM memory module.

Table 4: Hawk Board DIMM Memory Population Sequence

CONN	2	4	6	8	10	12	14	16
2 RDIMM	✓				✓			
4 RDIMMs	✓	✓			✓	✓		
6 RDIMMs	✓	✓	✓		✓	✓	✓	
8 RDIMMs	✓	✓	✓	✓	✓	✓	✓	✓

4.5. DIMM Sockets

The motherboard has 8 DIMM sockets and each slot requires a 15 µ-inch gold contact for the DDR4 SMT DIMM socket. This socket incorporates a blue housing with a white/nature latch for the DIMM in DDR channel. The vendor must announce if the color selection will increase the cost of the DIMM socket.

4.6. Network Interfaces

4.6.1. Dedicated Network Ports

The Hawk board provides two 10/100/1000 Ethernet ports accessible in the I/O connector area:

- Dedicated 10/100/1000 Ethernet port (through an onboard Intel® I210 Ethernet Controller)
- Dedicated BMC Management 10/100/1000 Ethernet port

BMC implements BMC Management 10/100/1000 Ethernet port using MAC2 RGMII and PHY. PHY MDIO Address is set to 0x1.

4.6.2. Management Ethernet

The Hawk board supports two options of management network interfaces for the BMC connection.

- 10/100/1000 MDI connected to RJ45 from Realtek RTL8211E driven by BMC through RGMII
- 10/100 NCSI connected from OCP 2.0 Mezzanine NIC driven by BMC through RMII

4.6.3. Add-on NIC Cards

Additional add-on NIC cards can be enabled either through the onboard PCIe expansion slot (x16) or through the OCP 2.0 connector.

4.7. PCI Express (PCIe) Interfaces

The Hawk board provides one x16 PCIe connector and one OCP 2.0 Mezzanine Card connector (with support for x16 lanes). All Hawk PCIe interfaces support Gen1, Gen2, and Gen3 data transfer speeds.

Note: There is no PCIe hot-swap circuit implemented on the Hawk board.

Table 5 lists the PCIe modes, lane bifurcations and usage of the PCIe ports on the Hawk board.

Table 5: Hawk Board PCIe Modes, Lane Bifurcations, and Usage

Hawk PCIe PORT	BIFURCATION	LANES	MODE	SYSTEM USAGE
0/1	x8x8	x16	Root Complex	OCP 2.0 Mezzanine Card
2/3	x8x8	x16	Root Complex, Endpoint	GPU/NIC
4/5	x4x4	x8	Root Complex, Endpoint	Storage
6	–	x1	Root Complex	On Board NIC
7	–	x1	Root Complex	BMC

4.7.1. PCIe Reference Clock (Differential)

PCIe reference clock for any eMAG PCIe port can be sourced either from the non-spread spectrum SYS_REFCLK1 (see *Figure 9*) or from spread spectrum capable SYS_REFCLK2 (see *Figure 10*).

Figure 9: Hawk PCIe Reference Clocks – Non Spread Spectrum

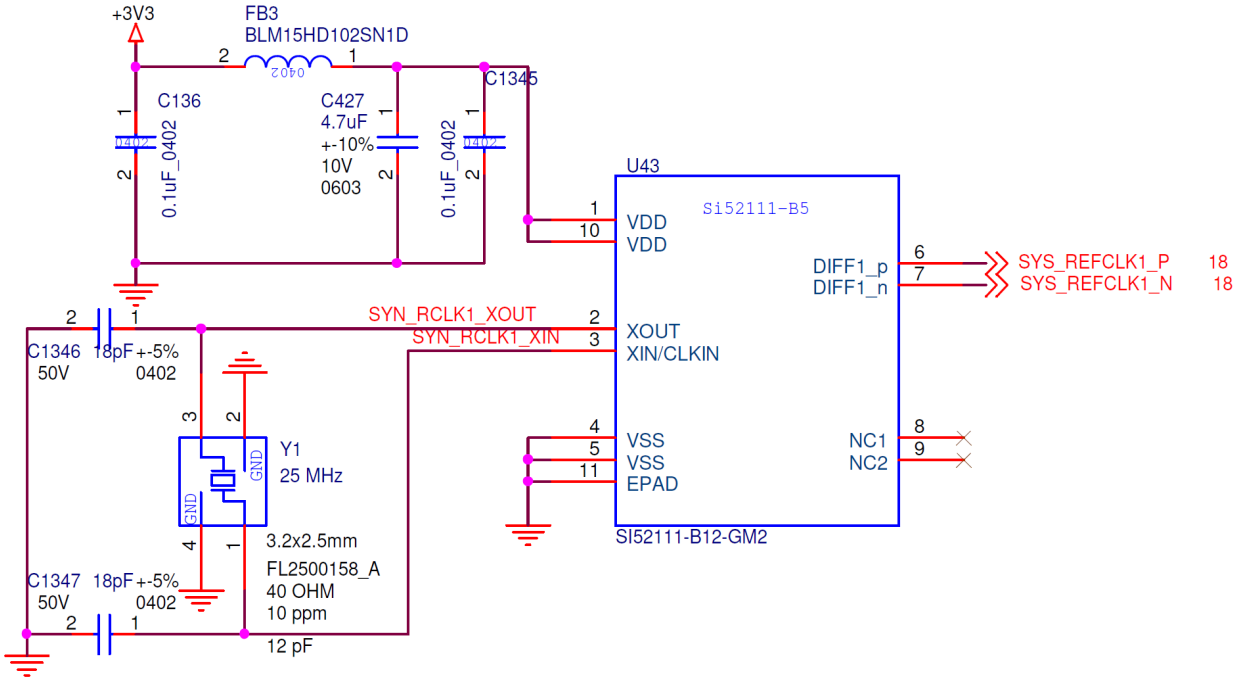
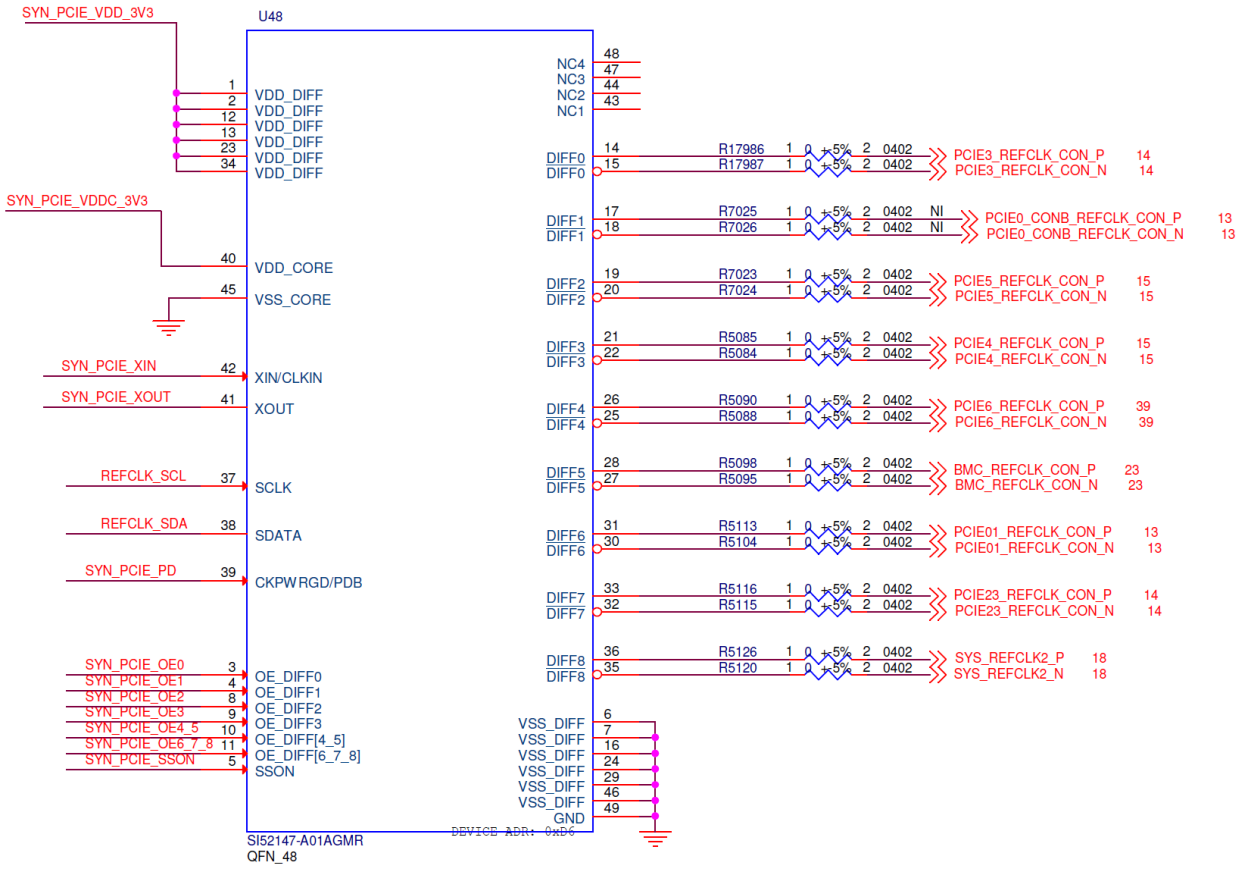


Figure 10: Hawk PCIe Reference Clocks – Spread Spectrum



eMAG takes two differential clocks (both of which are PCIe Gen4 compliant) as inputs. SYS_REFCLK1 pair is non-spread spectrum, while SYS_REFCLK2 is spread spectrum. Internally, any SerDes can be connected to either of the clock inputs, giving the system designer flexibility on supporting a mix of spread spectrum and non-spread spectrum ports.

The Hawk board implements differential system reference clocks using SiLabs PCIe Gen4 compliant clock generators Si52111-B5 (non-spread spectrum) and Si52147 (spread spectrum). All PCIe connectors and BMC derive their PCIe clock from a spread spectrum capable generator. The board implements a jumper to enable/disable spread spectrum clocking to test different modes as listed below.

Jumper J4 is used to enable spread spectrum for SYS_REFCLK2 and for reference clocks to PCIe expansion slots. It is disabled by default. Insert the J4 cap (jumper on) to enable spread spectrum.

Hawk PCIe reference clock architecture allows testing the following modes defined in the *PCI Express Base Specification Revision 3.1*:

- PCIe Ports 0-7 as Root Complex with Common Clock Architecture.
- PCIe Ports 0/2/4 as Endpoint with Common Clock Architecture if Host and Endpoint ports are connected with PCIe cable adapter on the same board.
- PCIe Ports 0-6 as Root Complex/Endpoint with Separate Refclk No SSC (SRNS) architecture.
- PCIe Ports 0-6 as Root Complex/Endpoint with Separate Refclk with Independent SSC (SRIS) architecture.
- Separate clock architectures SRNS and SRIS are supported using two eMAG system reference clocks (SYS_REFCLK1 and SYS_REFCLK2). Each PCIe port inside eMAG can be connected to one of two differential system reference clocks. If one port is connected to SYS_REFCLK1 and

another to SYS_REFCLK2, separate clock architecture is enabled. Enabling SSC on SYS_REFCLK2 sets SRIS mode, while disabling it sets SRNS mode.

- PCIe Port 7 is connected to BMC module, which is based on AST2500 and supports only PCIe Gen2, and is compliant with *PCI Express Base Specification Revision 2.0*.

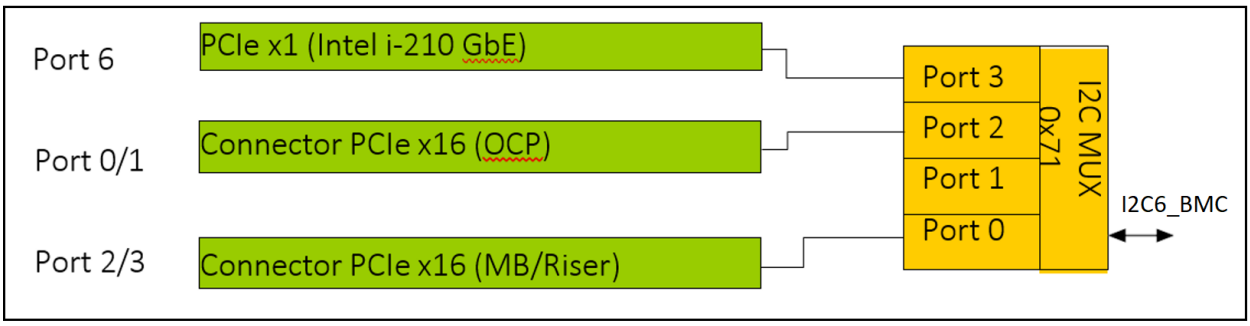
4.7.2. Miscellaneous PCIe Signals

The Hawk board provides special provisions for miscellaneous PCIe signals: PCIe reference clocks, I2C, WAKE#, PRESENT_DETECT, PERST#. These provisions allow the board to be configured for Root Complex or Endpoint on Ports 0/1, 2/3, 4/5 as well as common and separate clock architecture (SRNS and SRIS).

4.7.2.1. I2C for PCIe Connectors

Hawk implements an I2C mux to provide access from eMAG I2C2 bus to each of the four PCIe vertical connectors, as shown in *Figure 11*.

Figure 11: I2C for PCIe Mux on Hawk



4.7.2.2. PCIe Wake#

Hawk connects Wake# signal from PCIe slots to interrupt signal of corresponding port of I2C mux at address 0x71 on CPU I2C6_BMC bus. If Wake# is asserted, interrupt will be propagated by the mux to I2C6_ALERT_L signal. eMAG must poll I2C6 mux registers to find out which port had the interrupt asserted.

4.7.2.3. PCIe Present Detect

Hawk connects Present Detect signal from each of four PCIe connectors to GPI pin. eMAG firmware can detect board presence by checking status of GPI pins.

4.7.2.4.PCIe PERST#

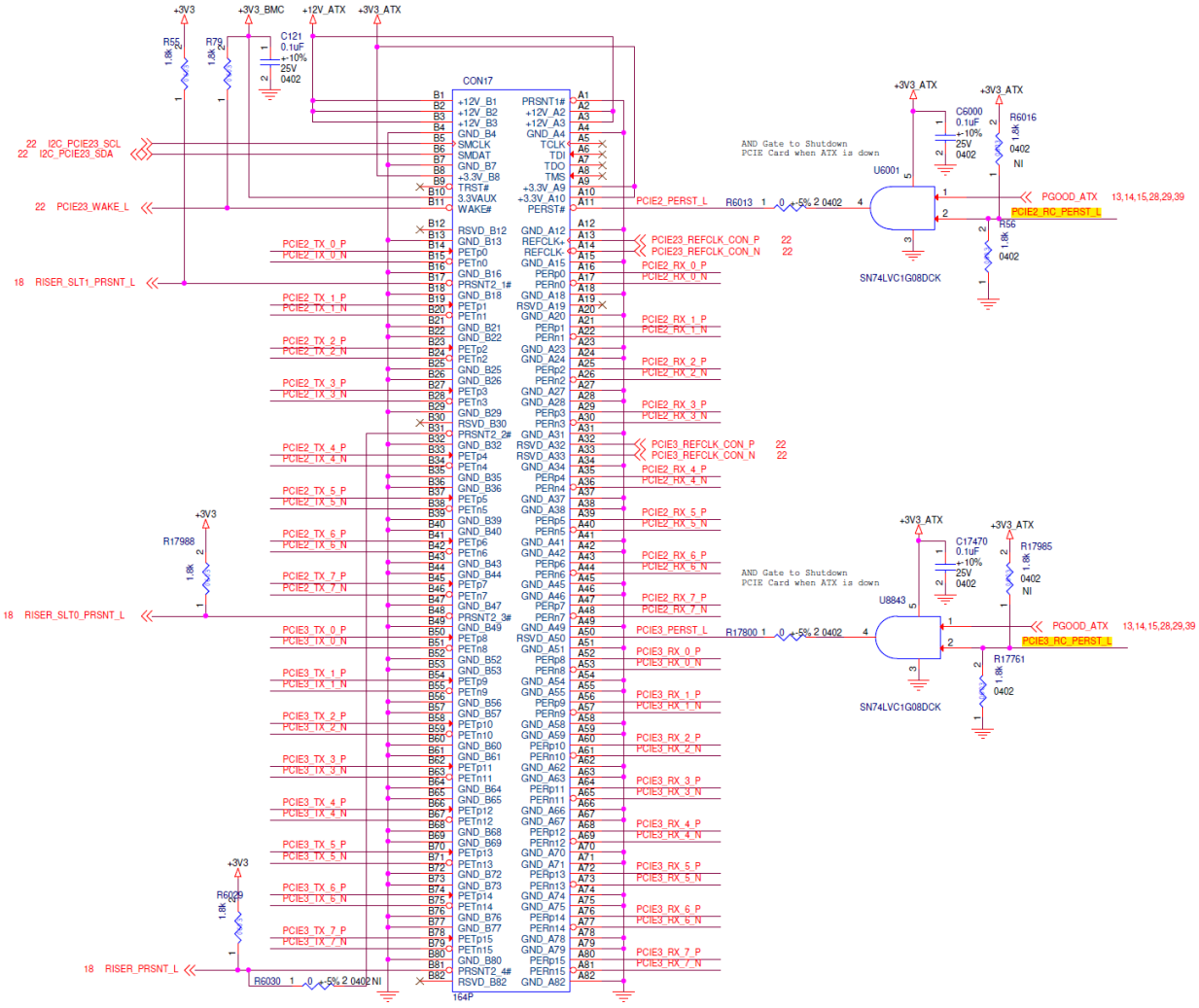
In Hawk form-factor, all PCIe ports are set as Root Complex. By default, output RC_PERST# signal from eMAG port is connected to PERST# pin of corresponding PCIe connector.

eMAG supports bifurcation on ports 0/1, 2/3, 4/5 and has another RC_PERST# signal for the second port. eMAG also supports Endpoint mode on ports 0, 2, 4 and has input EP_PERST# pins.

See *Figure 12*. For PCIe x16 slot on Hawk board using PCIE23:

- PCIE2_RC_PERSTN is connected directly to PCIe connector pin A11.
- PCIE3_RC_PERSTN is connected to PCIe connector reserved pin A50. It is used as a reset signal for the second PCIe x8 slot on a PCIe riser card when a PCIe riser card with two PCIe x8 slots are used.

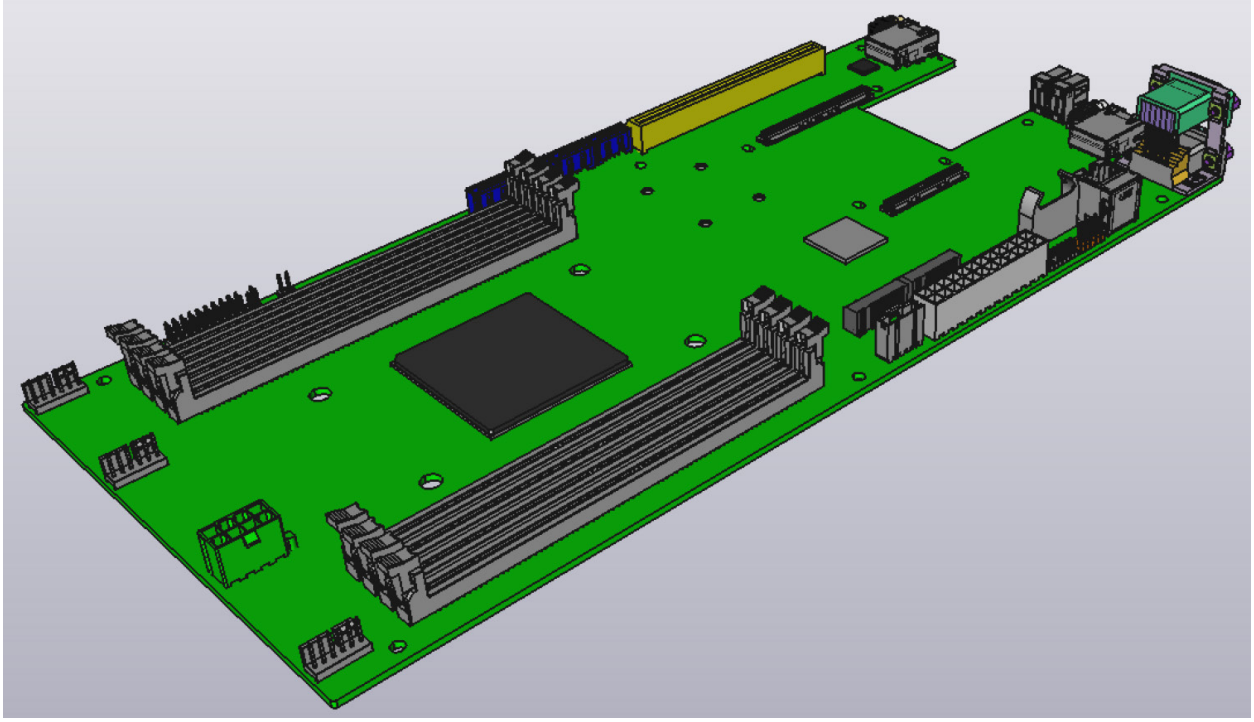
Figure 12: PCIe Port 0 PERST# Connection Header



4.8. PCIe x16 Slot/Riser Card

The motherboard has a single, 1x socket to be used by PCIe Riser card x16 slot (164 pins) – used for x16 PCIe and power delivery (see *Figure 13*).

Figure 13: PCIe Riser Card on the Hawk Board



Slot location must follow mechanical requirement that are outlined in the DXF document. The PCIe x16 slot combines between PCIe2 x8 lanes (LOW byte) and PCIe3 x8 lanes (HIGH byte) of CPU (refer *Table 6*).

Table 6: PCIe Connector Pin Descriptions for the Hawk Board

PIN	SIDE B CONNECTOR		SIDE A CONNECTOR	
#	NAME	DESCRIPTION	NAME	DESCRIPTION
1	+12 V	+12 volt power	PRSNT#1	Hot plug presence detect
2	+12 V	+12 volt power	+12 V	+12 volt power
3	+12 V	+12 volt power	+12 V	+12 volt power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK
6	SMDAT	SMBus data	JTAG3	TDI
7	GND	Ground	JTAG4	TDO
8	+3.3 V	+3.3 volt power	JTAG5	TMS
9	JTAG1	+TRST#	+3.3 V	+3.3 volt power
10	3.3Vaux	+3.3 V volt power	+3.3 V	+3.3 volt power

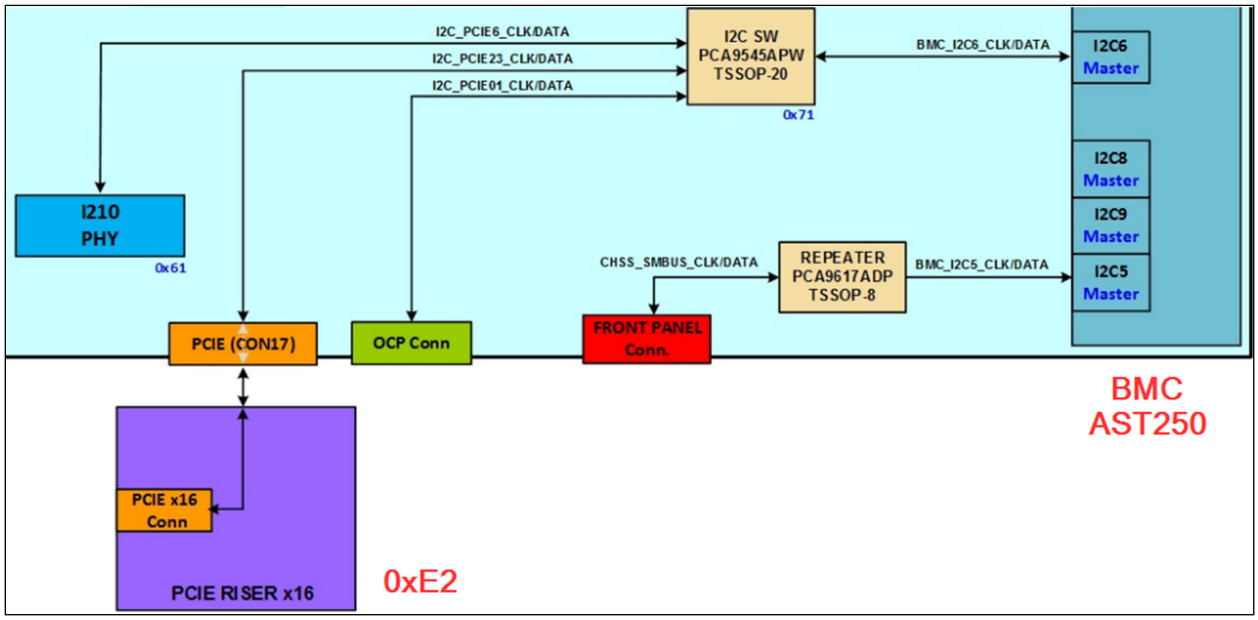
PIN	SIDE B CONNECTOR		SIDE A CONNECTOR	
#	NAME	DESCRIPTION	NAME	DESCRIPTION
11	WAKE#	Link Reactivation	PWRGD	Power Good
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	Reference Clock
14	HSOp(0)	Transmitter Lane 0,	REFCLK-	Differential pair
15	HSOn(0)	Differential pair	GND	Ground
16	GND	Ground	HSIp(0)	Receiver Lane 0,
17	PRSNT#2	Hotplug detect	HSIn(0)	Differential pair
18	GND	Ground	GND	Ground
19	HSOp(1)	Transmitter Lane 1,	RSVD	Reserved
20	HSOn(1)	Differential pair	GND	Ground
21	GND	Ground	HSIp(1)	Receiver Lane 1,
22	GND	Ground	HSIn(1)	Differential pair
23	HSOp(2)	Transmitter Lane 2,	GND	Ground
24	HSOn(2)	Differential pair	GND	Ground
25	GND	Ground	HSIp(2)	Receiver Lane 2,
26	GND	Ground	HSIn(2)	Differential pair
27	HSOp(3)	Transmitter Lane 3,	GND	Ground
28	HSOn(3)	Differential pair	GND	Ground
29	GND	Ground	HSIp(3)	Receiver Lane 3,
30	RSVD	Reserved	HSIn(3)	Differential pair
31	PRSNT#2	Hot plug detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	HSOp(4)	Transmitter Lane 4,	RSVD	Reserved
34	HSOn(4)	Differential pair	GND	Ground
35	GND	Ground	HSIp(4)	Receiver Lane 4,
36	GND	Ground	HSIn(4)	Differential pair
37	HSOp(5)	Transmitter Lane 5,	GND	Ground
38	HSOn(5)	Differential pair	GND	Ground
39	GND	Ground	HSIp(5)	Receiver Lane 5,
40	GND	Ground	HSIn(5)	Differential pair
41	HSOp(6)	Transmitter Lane 6,	GND	Ground

PIN	SIDE B CONNECTOR		SIDE A CONNECTOR	
#	NAME	DESCRIPTION	NAME	DESCRIPTION
42	HSOn(6)	Differential pair	GND	Ground
43	GND	Ground	HSIp(6)	Receiver Lane 6,
44	GND	Ground	HSIn(6)	Differential pair
45	HSOp(7)	Transmitter Lane 7,	GND	Ground
46	HSOn(7)	Differential pair	GND	Ground
47	GND	Ground	HSIp(7)	Receiver Lane 7,
48	PRSNT#2	Hot plug detect	HSIn(7)	Differential pair
49	GND	Ground	GND	Ground
50	HSOp(8)	Transmitter Lane 8,	RSVD	Reserved
51	HSOn(8)	Differential pair	GND	Ground
52	GND	Ground	HSIp(8)	Receiver Lane 8,
53	GND	Ground	HSIn(8)	Differential pair
54	HSOp(9)	Transmitter Lane 9,	GND	Ground
55	HSOn(9)	Differential pair	GND	Ground
56	GND	Ground	HSIp(9)	Receiver Lane 9,
57	GND	Ground	HSIn(9)	Differential pair
58	HSOp(10)	Transmitter Lane 10,	GND	Ground
59	HSOn(10)	Differential pair	GND	Ground
60	GND	Ground	HSIp(10)	Receiver Lane 10,
61	GND	Ground	HSIn(10)	Differential pair
62	HSOp(11)	Transmitter Lane 11,	GND	Ground
63	HSOn(11)	Differential pair	GND	Ground
64	GND	Ground	HSIp(11)	Receiver Lane 11,
65	GND	Ground	HSIn(11)	Differential pair
66	HSOp(12)	Transmitter Lane 12,	GND	Ground
67	HSOn(12)	Differential pair	GND	Ground
68	GND	Ground	HSIp(12)	Receiver Lane 12,
69	GND	Ground	HSIn(12)	Differential pair
70	HSOp(13)	Transmitter Lane 13,	GND	Ground
71	HSOn(13)	Differential pair	GND	Ground
72	GND	Ground	HSIp(13)	Receiver Lane 13,
73	GND	Ground	HSIn(13)	Differential pair

PIN	SIDE B CONNECTOR		SIDE A CONNECTOR	
#	NAME	DESCRIPTION	NAME	DESCRIPTION
74	HSOp(14)	Transmitter Lane 14,	GND	Ground
75	HSOn(14)	Differential pair	GND	Ground
76	GND	Ground	HSIp(14)	Receiver Lane 14,
77	GND	Ground	HSIn(14)	Differential pair
78	HSOp(15)	Transmitter Lane 15,	GND	Ground
79	HSOn(15)	Differential pair	GND	Ground
80	GND	Ground	HSIp(15)	Receiver Lane 15,
81	PRSNT#2	Hot plug present detect	HSIn(15)	Differential pair
82	RSVD#2	Hot Plug Detect	GND	Ground

The riser card must implement I2C to GPIO expander (PCA9545) to be accessed by BMC on motherboard to tell which ICs are currently on each slot. Vendor must follow the SMBUS addresses defined in *Figure 14* to avoid address conflicts. The PCIe x16 slot's SMBus connects to downstream channel 0 of SMBUS switch IC – PCA9545, the SCL/SDA upstream connects to BMC I2C6 and the 8 bit address of this PCA9545 is 0xE2.

Figure 14: I2C to GPIO Expander Implementation on the Hawk Board



4.9. SATA Connectivity

Hawk provides four SATA connectors. SATA0-3 are standard 7-pin vertical connectors intended to be used with SATA cable.

The vertical SATA connector needs to be placed near the I/O side of the motherboard for easy access. HDDs attached to all SATA connectors need to follow spin-up delay requirements as described below.

When a hard drive spins up after power on, it draws excessive current on both 12 V and 5 V. The peak current may reach 1.5 A ~ 2 A range on the 12 V rail. Based on the number of hard drives in the system,

all hard drives must spin up in a sequential manner. The BIOS must implement a 5-second delay between each hard drive spinning up. In order to do this, the SATA hard drive's power cable must have pin 11 as NC (No Connection) to enable hard drive's spin-up delay function.

4.10. M.2 Connectivity

The motherboard has 2x M.2 NVMe connectors with Key ID=M and H6.7 Type. M.2 connector has an optional connection of PCIe x4 from CPU. The onboard M.2 connector supports both 2280 and 22110 card form factors with both single-sided and double-sided contacts.

The PERST# signal must go active before the power on M.2 connector is removed per the *PCI Express Card Electromechanical Specification*.

The vendor must add SMBUS and Alert connections to the CPU base on the latest M.2 specification. Please be aware that the M.2 SMBUS is at 1.8 V level. The vendor must use a shunt regulator to create 1.8 V for SMBUS pull-up and add a level shifter to connect it to the CPU.

4.11. USB 2.0 Connectivity

The motherboard has two external Type-A, vertical, right angle USB 2.0 ports and two 5x2 USB 2.0 headers located on the right side of the board. The BIOS must support the following USB devices:

- USB keyboard and mouse
- USB flash drive (bootable)

The 5x2 header is used for two front panel USB 2.0 ports. A USB extension cable is required in this case.

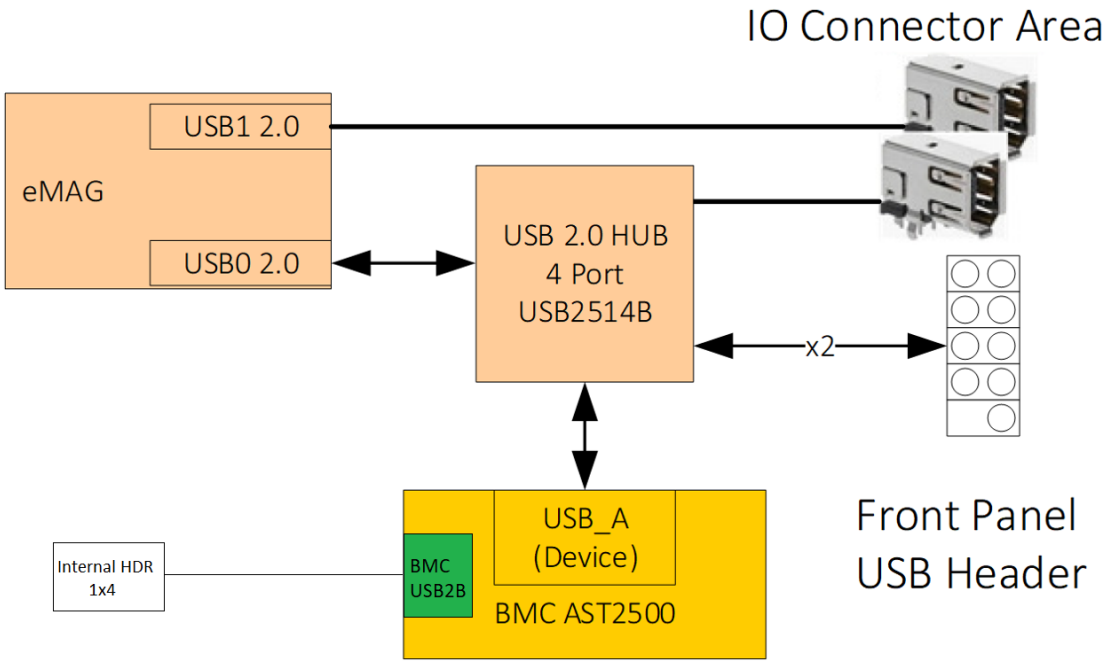
As shown in *Figure 15*, the eMAG CPU has two USB 2.0 ports.

USB0 is connected to a 4 port USB 2.0 hub. The hub's downstream ports are connected to BMC USB_B port, front panel USB header (two USB ports) and USB connector in I/O connector area.

USB1 is directly connected to USB connector in I/O connector area.

Every USB port is equipped with a USB LDO with overcurrent protection and can support devices with up to 500 mA VBUS current limit.

Figure 15: USB Subsection Implementation on the Hawk Board



4.12. UART Connectivity

The UART connectivity on the Hawk board is shown in *Figure 16*.

Figure 16: CPU UART[0,4] and BMC UART[1-3,5] Connectivity on the Hawk Board

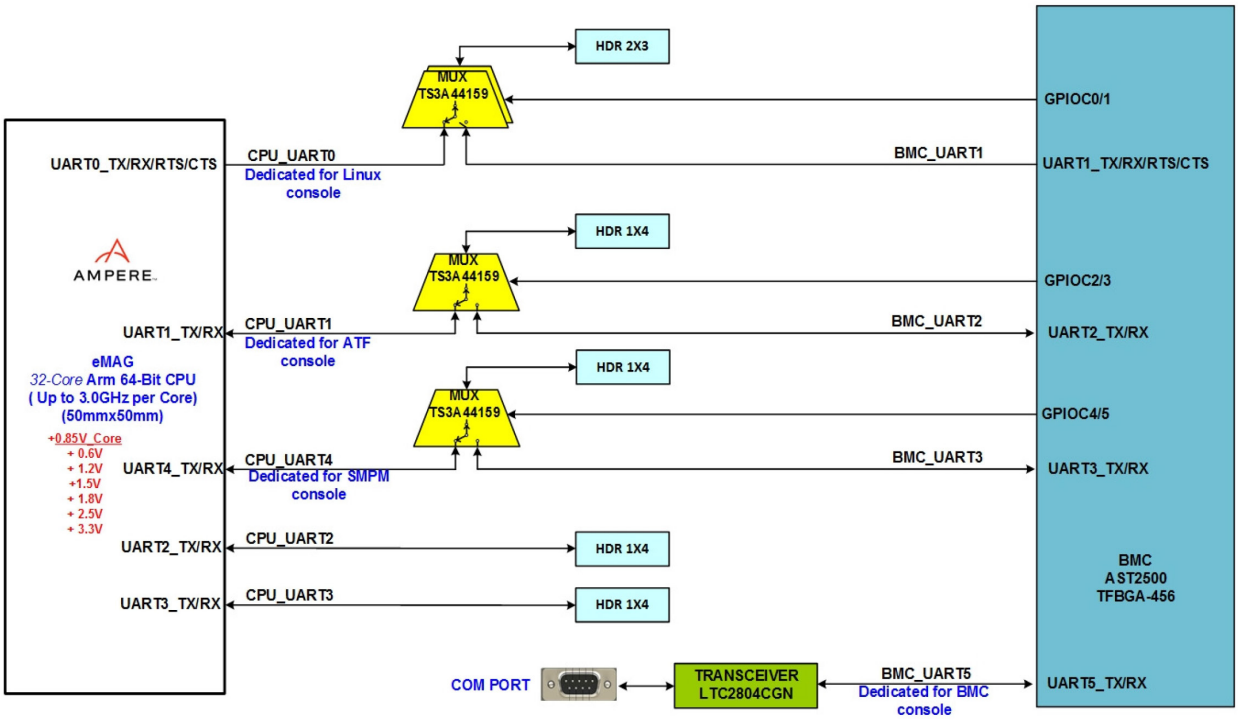
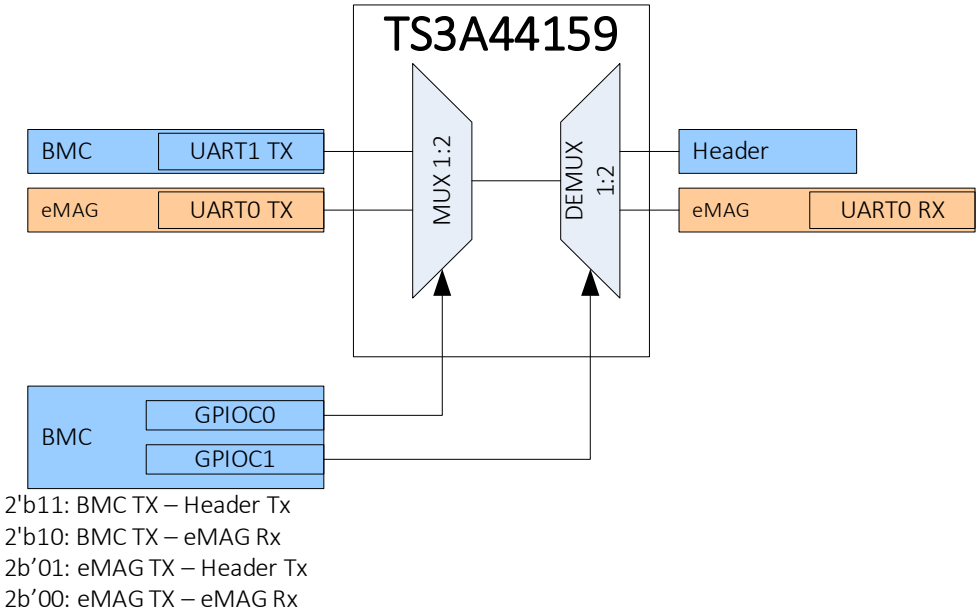


Figure 17 illustrates the 4-way multiplexer/demultiplexer implementation for the eMAG/BMC UARTs on the Hawk board.

Figure 17: 4-Way Mux/Demux for eMAG/BMC UARTs on the Hawk Board



BMC UART5 (debug console) is connected directly through a transceiver to DB9 in I/O area.

A four-way mux/demux is powered from BMC standby voltage and is power sequenced together with BMC. eMAG CPU pins are in “No Connect” mode unless BMC drives the correct control signals to it.

Table 7 lists the 4-pin UART0 header 2x3 on the Hawk board.

Table 7: UART0 2x3 Header Pinout on the Hawk Board

PIN #	SIGNAL	PIN #	SIGNAL
1	+3V3	2	UART_TXVR_TXD0
3	UART_TXVR_RTS0	4	GND
5	UART_TXVR_CTS0	6	UART_TXVR_RXD0

Table 8 lists the 2-pin UART1, 2, 3, 4 header 1x4 on the Hawk board.

Table 8: UART1, 2, 3, and 4 1x4 Header Pinout on the Hawk Board

PIN #	SIGNAL	PIN #	SIGNAL
1	+3V3	2	UART_RXDx
3	UART_TXDx	4	GND

4.12.1. UART Channel Selection

BMC UART5 (debug console) is connected directly through transceiver to DB9 in IO area.

A four-way mux/demux is powered from BMC stand-by voltage and is power sequenced together with BMC. eMAG CPU pins are in No Connect mode unless BMC drives the correct control signal state to it.

The four-way mux/demux is controlled by BMC GPIOC0-5 interface. Control can be overridden by installing UART control override jumpers on the UART header.

Table 9 lists the UART mode control signals.

Table 9: UART Mode Control Signals on the Hawk Board

BMC SIGNALS	UART MODE	CONTROL STATE	UART MODE
GPIOC[1:0]	UART0_MODE[1:0]	2b’00	eMAG UART0 Loopback
GPIOC[1:0]	UART0_MODE[1:0]	2b’01	eMAG UART0 > IO Area Header
GPIOC[1:0]	UART0_MODE[1:0]	2b’10	BMC UART1 > eMAG UART0
GPIOC[1:0]	UART0_MODE[1:0]	2b’11	BMC UART1 > IO Area Header
GPIOC[3:2]	UART1_MODE[1:0]	2b’00	eMAG UART1 Loopback
GPIOC[3:2]	UART1_MODE[1:0]	2b’01	eMAG UART1 > IO Area Header
GPIOC[3:2]	UART1_MODE[1:0]	2b’10	BMC UART2 > eMAG UART1
GPIOC[3:2]	UART1_MODE[1:0]	2b’11	BMC UART2 > IO Area Header
GPIOC[5:4]	UART4_MODE[1:0]	2b’00	eMAG UART4 Loopback
GPIOC[5:4]	UART4_MODE[1:0]	2b’01	eMAG UART4 > IO Area Header
GPIOC[5:4]	UART4_MODE[1:0]	2b’10	BMC UART3 > eMAG UART4
GPIOC[5:4]	UART4_MODE[1:0]	2b’11	BMC UART3 > IO Area Header

4.12.2. UART Summary and Schematics

- eMAG UART0: Non-secure 4-way switch to BMC UART1 and I/O header
- eMAG UART4: Secure 4-way switch to BMC UART3 and I/O header
- eMAG UART1: SMpro console, 4-way switch to BMC UART2 and I/O header
- BMC UART1: 4-way switch to eMAG UART0 and I/O header
- BMC UART2: 4-way switch to eMAG UART1 and I/O header
- BMC UART3: 4-way switch to eMAG UART4 and I/O header
- BMC UART5: BMC debug console, connected to transceiver and I/O header

Figure 18 and *Figure 19* illustrate the UART schematics for the Hawk board.

Figure 18: Hawk Board UART Schematics – 1

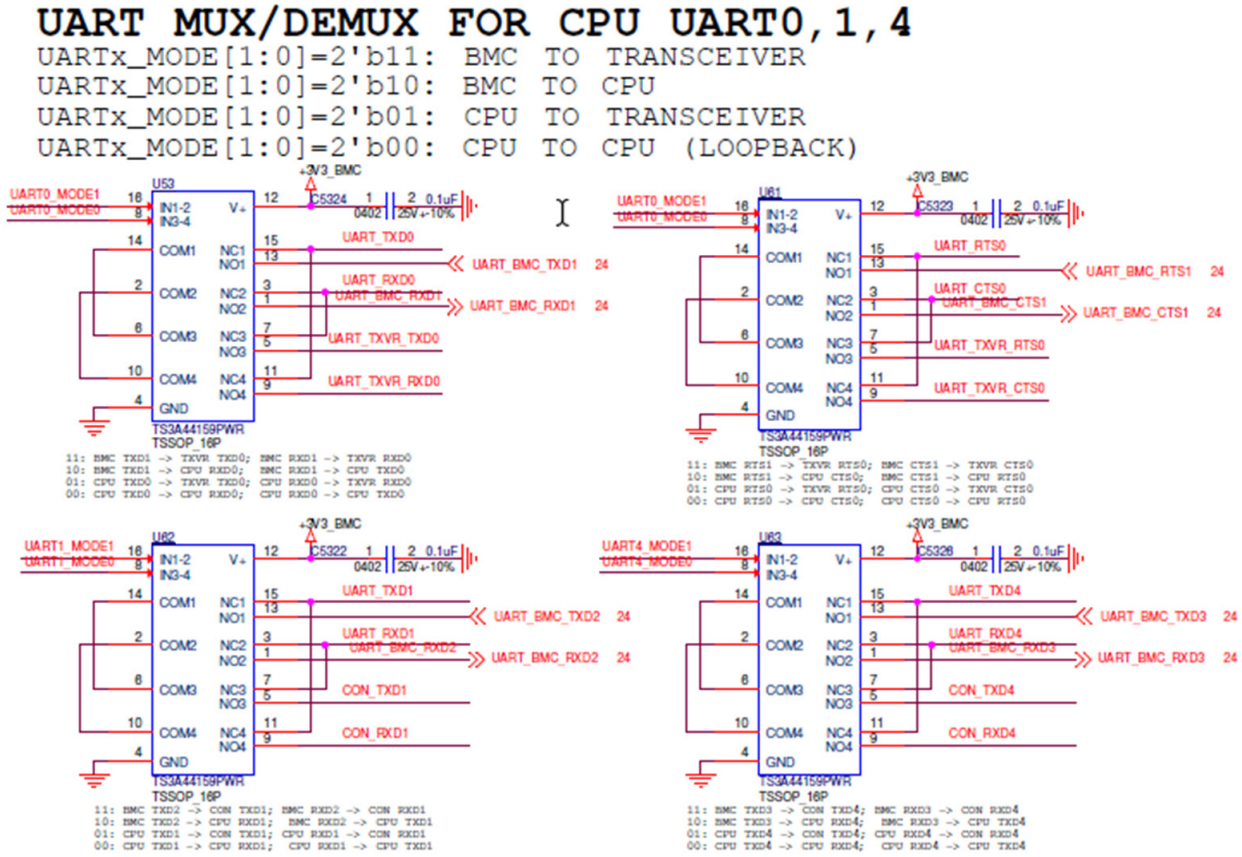
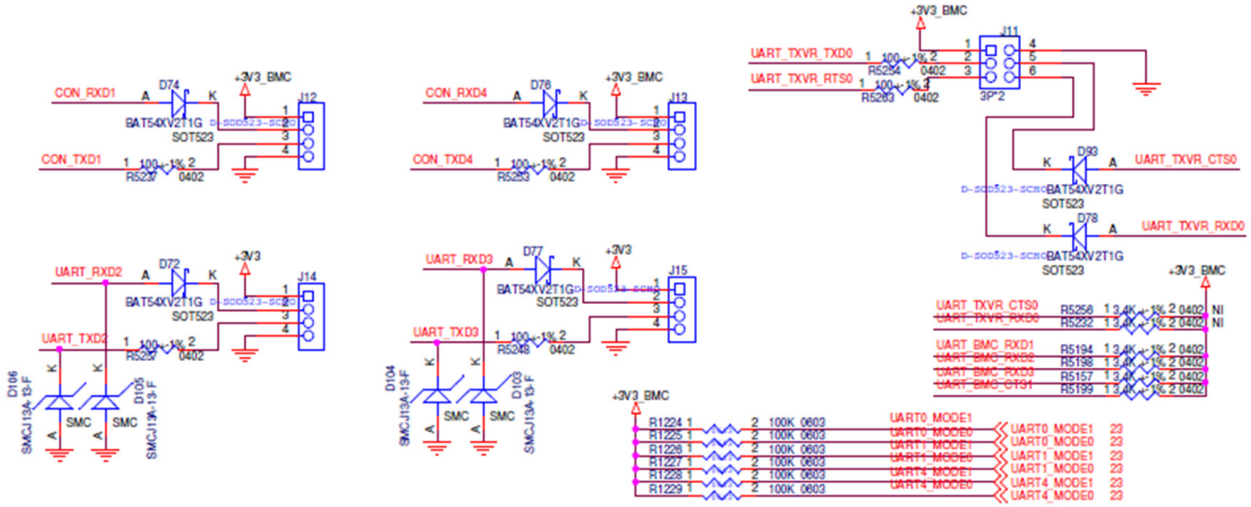


Figure 19: Hawk Board UART Schematics – 2



4.13. Fan Connectivity

The Hawk board has three system dual fan connectors. Fan connector signals must follow *4-Wire Pulse Width Modulation (PWM) Controlled Fans Specification Revision 1.3* (dated September 2005) published by Intel Corporation. Each fan connector has six pins, which is compatible with a standard 4-wire fan connector, and can also be used to support a dual rotor fan with independent PWM control signals as well as tachometer (TACH) signals. The fan connector pin definitions are listed in *Table 10*. Note that the fan power needs to be turned off during S5.

Table 10: Hawk Fan Connector Pinout

PIN	DESCRIPTION	PIN	DESCRIPTION
1	GND	4	Control #1
2	+12 V	5	Sense #2
3	Sense #1	6	Control #2

4.14. VGA Connector

The Hawk board has a right edge type DB15 VGA connector on the motherboard side. *Table 11* lists the signal assignments.

Table 11: Standard Female DB9 VGA Connector Pinout

PIN	DESCRIPTION	PIN	DESCRIPTION	PIN	DESCRIPTION
1	Red video	2	Green video	3	Blue video
4	Reserved since E-DDC, formerly monitor ID. Bit 2	5	Ground (HSync)	6	Red return
7	Green return	8	Blue return	9	+5 V DC (powers EDID EEPROM chip on some monitors), formerly key

PIN	DESCRIPTION	PIN	DESCRIPTION	PIN	DESCRIPTION
10	Ground (VSync, DDC)	11	Reserved since E-DDC, formerly monitor ID. Bit 0	12	I²C data since DDC2, formerly monitor ID. Bit 1
13	Horizontal sync	14	Vertical sync	15	I²C clock since DDC2, formerly monitor ID. Bit 3

4.15. SPI Interface

eMAG supports two SPI interfaces (SPI0 and SPI1). Only SPI0 is used on Hawk to interface with the SPI NOR.

eMAG SPI0 is connected to BMC host SPI interface, which supports pass-through mode for normal CPU booting (refer *Figure 20*). BMC can update SPI NOR image by taking over control of the bus and providing Remote Firmware Upgrade (RFU) capability to the system.

Figure 20: eMAG SPI0 Boot Bus

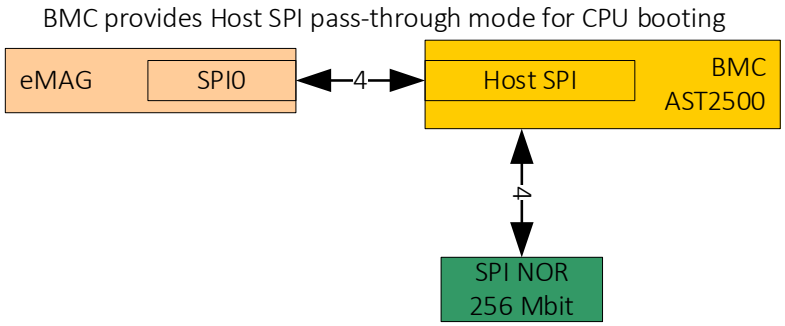


Table 12 lists the devices connected to the SPI bus on the Hawk board.

Table 12: SPI Devices on the Hawk Board

BUS NAME	SELECT	FUNCTION	PART NUMBER
SPI0	CS0	Boot SPI NOR flash, 256 Mbit	MX25L25635FMI-10G

4.16. I2C (IIC) Buses

eMAG CPU provides five I2C buses. *Table 13* lists the eMAG SoC specification with I2C bus allocation for different system functions.

Table 13: eMAG I2C Buses Available on the Hawk Board

IIC DEVICE #	SMB_ALERT	FREQ	MASTER/ SLAVE	LOCATION	ACCESSIBILITY	USAGE	IIC OWNER
IIC4	Yes (in)- EVENT# (wired-OR)	1 MHz pt-pt	Master	AHBC	All Optionally S or NS	External BMC – SMpro responds to BMC requests, Board Temp Sensors, Sys EEPROM, and any other I2C devices. (SFP+, RTC etc.)	SMpro
IIC3	Yes (in)- EVENT# (wired-OR)	1 MHz pt-pt	Slave	AHBC	All Optionally S or NS	External BMC – SMpro receives BMC requests	SMpro
IIC2	Yes (in)- EVENT# (wired-OR)	1 MHz pt-pt	Master	AHBC	All Optionally S or NS	DDR DIMMs SPD (with an external I2C mux chip when more than 8 SPDs and/or other devices as well, need to be attached)	PMD, SMpro
IIC1+ BSC	No	400 kHz	Master	SMpro secure boundary	Private to SMpro	EEPROM for bootstrap vector or SMpro code	SMpro
IIC0	Yes (in)- VR ALERT output	1 MHz	Master	PMpro	All Secure only	VRs/VRMs	PMpro

Table 14: eMAG I2C Devices Available on the Hawk Board

CPU ADDRESS MAP TABLE			
BUS NAME	I2C ADDRESS (7b)	I2C ADDRESS (8b)	PART NUMBER
IIC0 (I2C/PMbus)	0x68	0xD0	TPS53659 (VDDQ0123)
	0x6A	0xD4	TPS53659 (VDDQ4567)
	0x58	0xB0	TPS53679 (CPU_PCP)

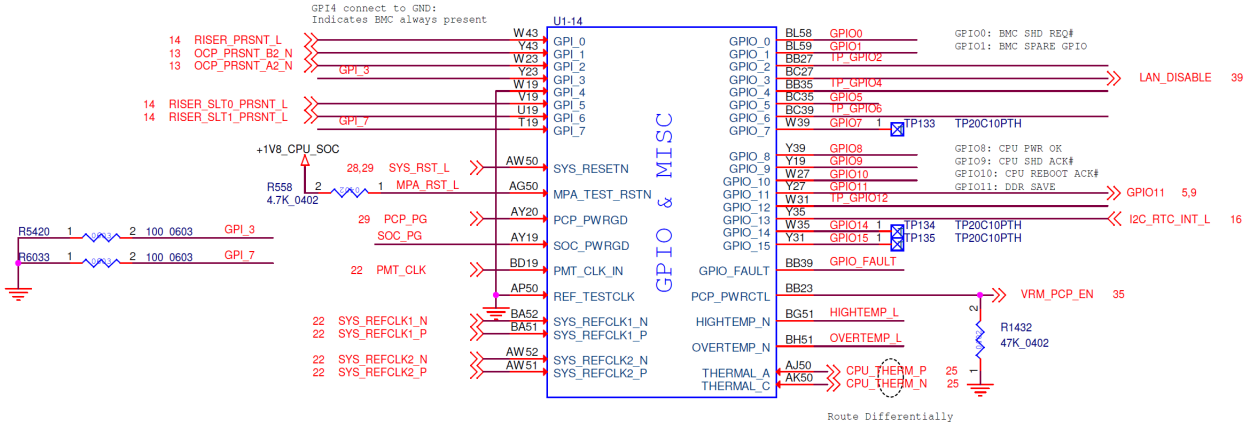
CPU ADDRESS MAP TABLE			
BUS NAME	I2C ADDRESS (7b)	I2C ADDRESS (8b)	PART NUMBER
	0x18	0x30	TPS544B20RVFR (CPU_SOC)
IIC1	0x52, 0x53	0xA4, 0xA6	EEPROM AT24CM01
	0x51	0xA2	RTC PCF85063TP/1Z
IIC2	0x70	0xE0	I2C SW PCA9545APW
	0x50	0xA0	DIMM#0 (PCA9545APW SW CH0)
	0x52	0xA4	DIMM#1 (PCA9545APW SW CH0)
	0x54	0xA8	DIMM#2 (PCA9545APW SW CH0)
	0x56	0xAC	DIMM#3 (PCA9545APW SW CH0)
	0x50	0xA0	DIMM#4 (PCA9545APW SW CH1)
	0x54	0xA4	DIMM#5 (PCA9545APW SW CH1)
	0x54	0xA8	DIMM#6 (PCA9545APW SW CH1)
	0x56	0xAC	DIMM#7 (PCA9545APW SW CH1)
	TBD	TBD	M.2_0 (PCA9545APW SW CH2)
	TBD	TBD	M.2_1 (PCA9545APW SW CH3)
IIC3	TBD	TBD	BMC I2C3
IIC4	TBD	TBD	BMC I2C1
IIC5	TBD	TBD	TBD
BMC ADDRESS MAP TABLE			
BUS NAME	I2C ADDRESS (7b)	I2C ADDRESS (8b)	PART NUMBER
IIC1	TBD	TBD	CPU I2C4
IIC2	0x52, 0x53	0xA4, 0xA6	EEPROM AT24CM01
	0x51	0xA2	RTC PCF85063TP/1Z
IIC3	TBD	TBD	CPU I2C3
IIC4	0x50	0xA0	CAT24C64WI
	0x19	0x32	LM95231CIMM-1
	0x48	0x90	TMP75A
	0x49	0x92	TMP75A
	0x4A	0x94	TMP75A
IIC5	TBD	TBD	FRONT PANEL CONNECTOR

BMC ADDRESS MAP TABLE			
BUS NAME	I2C ADDRESS (7b)	I2C ADDRESS (8b)	PART NUMBER
IIC6	0x71	0xE2	I2C SW PCA9545PW
	TBD	TBD	PCIE (CON17/RISER) (PCA9545A PW SW CH0)
	0x61	0xC2	PCIE (ONBOARD INTEL I210 CONTROLLER) (PCA9545A PW SW CH1)
	TBD	TBD	OCP (CON41/OCP) (PCA9545A PW SW CH2)
IIC7	TBD	TBD	BMC AUX PMBUS CONNECTOR
IIC8	TBD	TBD	RMC SIGNAL CONNECTOR
IIC9	TBD	TBD	TBD

4.17. GPIO Signals

Figure 21 lists eMAG GPI and GPIO that are assigned some special Hawk board functions.

Figure 21: eMAG GPIO Signal Schematics



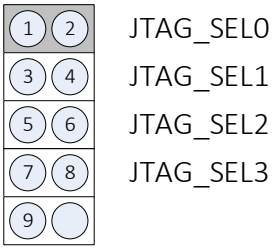
4.18. JTAG Debug Interfaces

The Hawk board provides four JTAG connectors as debug ports to different eMAG JTAG chains: SMpro [CON33], PMPro [CON34], SoC [CON35], and DAP [CON32]. All JTAG interfaces are 1.8 V as shown in *Figure 22*.

All JTAG connectors are directly compatible with Arm JTAG debuggers such as BDI. JTAG Select header [J2] is provided to control JTAG_SEL[0:3]. By default, JTAG_SELx signals have on board pull-ups to 1.8 V. To set it low, install corresponding jumper on header J2.

- CON33 supports SMpro debug with BDI3000 debugger
- CON32 supports DAP debug for CPU with OCD (on chip debugger)
- CON34 supports PMpro debug with BDI3000 debugger
- CON35 supports SOC debug with OCD (on chip debugger)

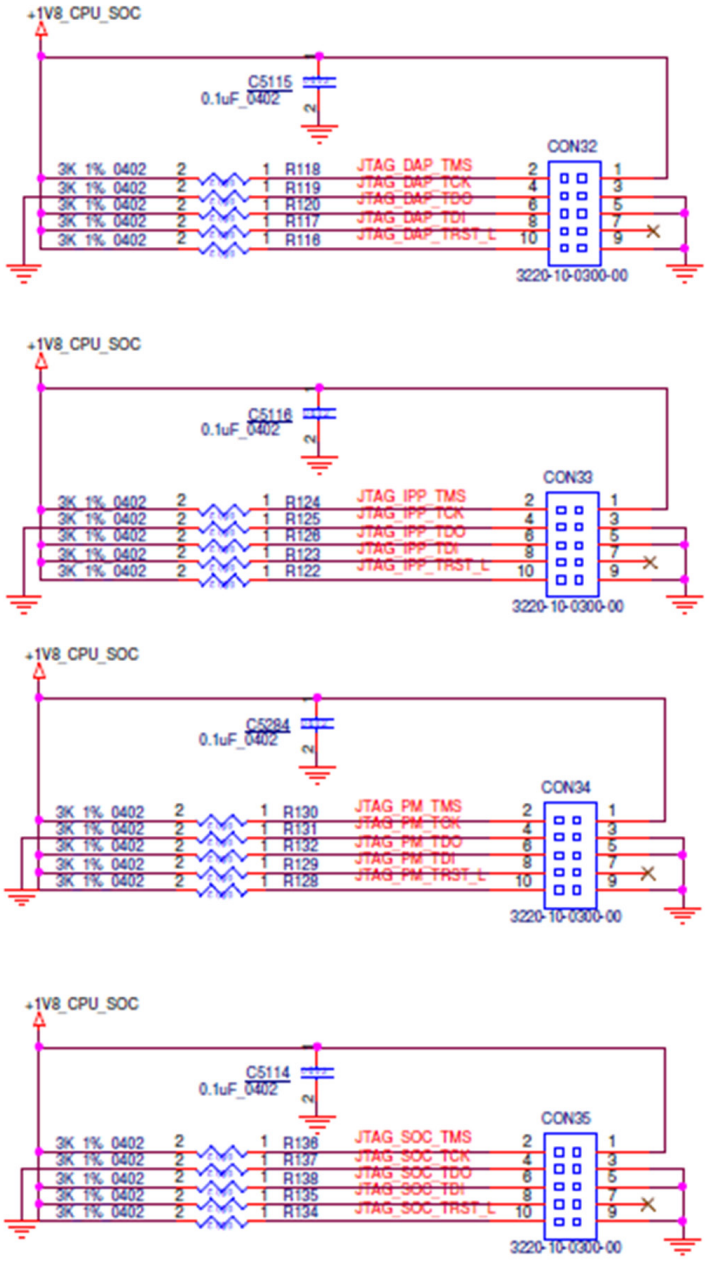
Figure 22: Hawk JTAG Select Header (J2) Pinout



Note: Parallel Trace is not supported by any of the JTAG connectors.

Figure 23 shows the JTAG schematics on the Hawk board.

Figure 23: eMAG JTAG Schematics on the Hawk Board



4.19. Serial Console

The output stage of the system BMC's serial console must be contained on the board. It is provided with a RS-232 transceiver and a female DB9 connector (see *Figure 5*) with pin definitions listed in *Table 15*.

Table 15: Hawk Board Serial Port DB9 Female Pin Connector Pinout

PIN	SIGNAL NAME	PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	NC	4	NC	7	NC
2	RxD	5	GND	8	NC
3	TxD	6	NC	9	NC

4.20. Serial Trace Debug Interface

The Hawk board provides a serial trace debug connector (Samtec ASP-130367-01). Only 2 Tx lanes and GND on selected pins are connected on this connector (refer *Table 16*).

Table 16: Serial Trace Connector Pinout on the Hawk Board

SIGNAL NAME	PIN(S)
STRC0_TX_P	13
STRC0_TX_N	15
STRC1_TX_P	25
STRC1_TX_N	27
GND	11, 17, 23, 29, 41, 42

5. PCB Stack-up Guidelines

The PCB stack-up parameters listed in *Table 17*, *Table 18*, *Table 19*, and *Table 20* are recommended for the board design. The vendor must fine tune the impedances based on these impedance control tables before starting the PCB design.

Table 17: Hawk Board PCB Stack-up

LAYER	TYPE	STRUCTURE	Cu TYPE	THICKNESS (mils)	RC%	Dk (1G)	Df (1G)	REF LAYERS
	SM	SM		0.5				
L1	TOP		STD	2.1				L2
pp		1080*1		2.54	63%	3.79	0.02	
L2	GND1		RTF	1.2				
Core		2116*1		4		4.22	0.02	
L3	IN1		RTF	1.2				L2/L4
pp		1067*2		4.8	76%	3.44	0.02	
L4	GND2		RTF	1.2				
Core		2116*1		4		4.22	0.02	

LAYER	TYPE	STRUCTURE	Cu TYPE	THICKNESS (mils)	RC%	Dk (1G)	Df (1G)	REF LAYERS
L5	IN2		RTF	1.2				L4/L5
pp		1067*2		4.8	76%	3.44	0.02	
L6	GND3		RTF	1.2				
Core		1080*1		3		3.78	0.02	
L7	IN3		RTF	1.2				L6/L8
pp		2113*2		6.8	61%	3.93	0.02	
L8	PWR1		RTF	1.2				
Core	2-Ply	106*2		4		3.61	0.02	
L9	PWR2		RTF	1.2				
pp		2113*2		6.8	61%	3.93	0.02	
L10	IN4		RTF	1.2				L9/L11
Core		1080*1		3		3.78	0.02	
L11	GND4		RTF	1.2				
pp		1067*2		4.8	76%	3.44	0.02	
L12	IN5		RTF	1.12				L11/L13
Core		2116*1		4		4.22	0.02	
L13	GND5		RTF	1.2				
pp		1067*2		4.8	76%	3.44	0.02	
L14	IN6		RTF	1.2				L13/L15
Core		2116*1	3	4		4.22	0.02	
L15	GND6		RTF	1.2				
pp		1080*1		2.54	63%	3.79	0.02	
L16	BOT		STD	2.1				L15
	SM	SM		0.5				
Total Thickness (mil)		Total		**85.8**				
Total Thickness (mm)					2.179324359			

Table 18: Motherboard PCB Impedance Control – 1

LAYER		40 Ω SINGLE-ENDED				50 Ω SINGLE-ENDED			
#	TYPE	DESIGN		SIMULATED		DESIGN		SIMULATED	
		TARGET Zo (Ω)	LW (mil)	TARGET Zo (Ω)	LW (mil)	TARGET Zo (Ω)	LW (mil)	TARGET Zo (Ω)	LW (mil)
	SM								
L1	TOP	40±15%	6.7	40.03	6.1	50±10%	4.2	49.92	3.9
pp									
L2	GND1								
Core									
L3	IN1	40±10%	5.2	40.17	5.4	50±10%	3.7	49.97	3.4
pp									
L4	GND2								
Core									
L5	IN2	40±10%	5.2	40.17	5.4	50±10%	3.7	49.97	3.4
pp									
L6	GND3								
Core									
L7	IN3	40±10%	5.4	40.09	5.2	50±10%	3.5	50.14	3.2
pp									
L8	PWR1								
Core	2-Ply								
L9	PWR2								
pp									
L10	IN4	40±10%	5.4	40.09	5.2	50±10%	3.5	50.14	3.2
Core									
L11	GND4								
pp									
L12	IN5	40±10%	5.2	40.17	5.4	50±10%	3.7	49.97	3.4
Core									
L13	GND5								
pp									
L14	IN6	40±10%	5.2	40.17	5.4	50±10%	3.7	49.97	3.4
Core									

LAYER		40 Ω SINGLE-ENDED				50 Ω SINGLE-ENDED			
#	TYPE	DESIGN		SIMULATED		DESIGN		SIMULATED	
		TARGET Zo (Ω)	LW (mil)	TARGET Zo (Ω)	LW (mil)	TARGET Zo (Ω)	LW (mil)	TARGET Zo (Ω)	LW (mil)
L15	GND6								
pp									
L16	BOT	40±15%	6.7	40.03	6.1	50±10%	4.2	49.92	3.9
	SM								

Table 19: Motherboard PCB Impedance Control – 2

LAYER		80 Ω DIFFERENTIAL PAIR				85 Ω DIFFERENTIAL PAIR			
#	TYPE	DESIGN		SIMULATED		DESIGN		SIMULATED	
		TARGET Zo (Ω)	LW/LS (mil)	TARGET Zo (Ω)	LW/LS (mil)	TARGET Zo (Ω)	LW/LS (mil)	TARGET Zo (Ω)	LW/LS (mil)
	SM								
L1	TOP	80±10%	5.5/9	79.95	5.5/9	85±10%	5.2/8.8	84.77	4.9/9.1
pp									
L2	GND1								
Core									
L3	IN1	80±10%	5.0/6.5	80.19	4.9/6.6	85±10%	4.4/6.5	85.19	4.3/6.6
pp									
L4	GND2								
Core									
L5	IN2	80±10%	5.0/6.5	80.19	4.9/6.6	85±10%	4.4/6.5	85.19	4.3/6.6
pp									
L6	GND3								
Core									
L7	IN3	80±10%	5.0/7.5	79.88	4.8/7.7	85±10%	4.4/7.5	84.99	4.2/7.7
pp									
L8	PWR1								
Core	2-Ply								
L9	PWR2								
pp									

LAYER		80 Ω DIFFERENTIAL PAIR				85 Ω DIFFERENTIAL PAIR			
#	TYPE	DESIGN		SIMULATED		DESIGN		SIMULATED	
		TARGET Zo (Ω)	LW/LS (mil)	TARGET Zo (Ω)	LW/LS (mil)	TARGET Zo (Ω)	LW/LS (mil)	TARGET Zo (Ω)	LW/LS (mil)
L10	IN4	80±10%	5.0/7.5	79.88	4.8/7.7	85±10%	4.4/7.5	84.99	4.2/7.7
Core									
L11	GND4								
pp									
L12	IN5	80±10%	5.0/6.5	80.19	4.9/6.6	85±10%	4.4/6.5	85.19	4.3/6.6
Core									
L13	GND5								
pp									
L14	IN6	80±10%	5.0/6.5	80.19	4.9/6.6	85±10%	4.4/6.5	85.19	4.3/6.6
Core									
L15	GND6								
pp									
L16	BOT	80±10%	5.5/9	79.95	5.5/9	85±10%	5.2/8.8	84.77	4.9/9.1
	SM								

Table 20: Motherboard PCB Impedance Control – 3

LAYER		90 Ω DIFFERENTIAL PAIR				100 Ω DIFFERENTIAL PAIR			
#	TYPE	DESIGN		SIMULATED		DESIGN		SIMULATED	
		TARGET Zo (Ω)	LW/LS (mil)	TARGET Zo (Ω)	LW/LS (mil)	TARGET Zo (Ω)	LW/LS (mil)	TARGET Zo (Ω)	LW/LS (mil)
	SM								
L1	TOP	90±10%	4.6/9.4	90.66	4.3/9.7	100±10%	3.6/9.4	100.35	3.4/9.6
pp									
L2	GND1								
Core									
L3	IN1	90±10%	3.8/6.3	90.56	3.7/6.4	100±10%	3.1/7.5	100.61	3/7.6
pp									
L4	GND2								

LAYER		90 Ω DIFFERENTIAL PAIR				100 Ω DIFFERENTIAL PAIR			
#	TYPE	DESIGN		SIMULATED		DESIGN		SIMULATED	
		TARGET Zo (Ω)	LW/LS (mil)	TARGET Zo (Ω)	LW/LS (mil)	TARGET Zo (Ω)	LW/LS (mil)	TARGET Zo (Ω)	LW/LS (mil)
Core									
L5	IN2	90±10%	3.8/6.3	90.56	3.7/6.4	100±10%	3.1/7.5	100.61	3/7.6
pp									
L6	GND3								
Core									
L7	IN3	90±10%	3.8/6.7	89.69	3.6/6.9	100±10%	3.1/8.5	99	3/8.6
pp									
L8	PWR1								
Core	2-Ply								
L9	PWR2								
pp									
L10	IN4	90±10%	3.8/6.7	89.69	3.6/6.9	100±10%	3.1/8.5	99	3/8.6
Core									
L11	GND4								
pp									
L12	IN5	90±10%	3.8/6.3	90.56	3.7/6.4	100±10%	3.1/7.5	100.61	3/7.6
Core									
L13	GND5								
pp									
L14	IN6	90±10%	3.8/6.3	90.56	3.7/6.4	100±10%	3.1/7.5	100.61	3/7.6
Core									
L15	GND6								
pp									
L16	BOT	90±10%	4.6/9.4	90.66	4.3/9.7	100±10%	3.6/9.4	100.35	3.4/9.6
	SM								

6. Bootstrap Configuration

After initial power up, eMAG requires bootstrap configuration, following which, SMpro reads I2C bootstrap EEPROM connected to I2C1 at device address 0x52. The EEPROM image contains detailed parameters for eMAG initialization.

Bootstrap EEPROM is connected to eMAG through an I2C isolator. It is also connected to BMC I2C2 bus and can be updated from BMC. Refer to the section titled *Bootstrap EEPROM* in this document for details.

6.1. Bootstrap EEPROM Reset

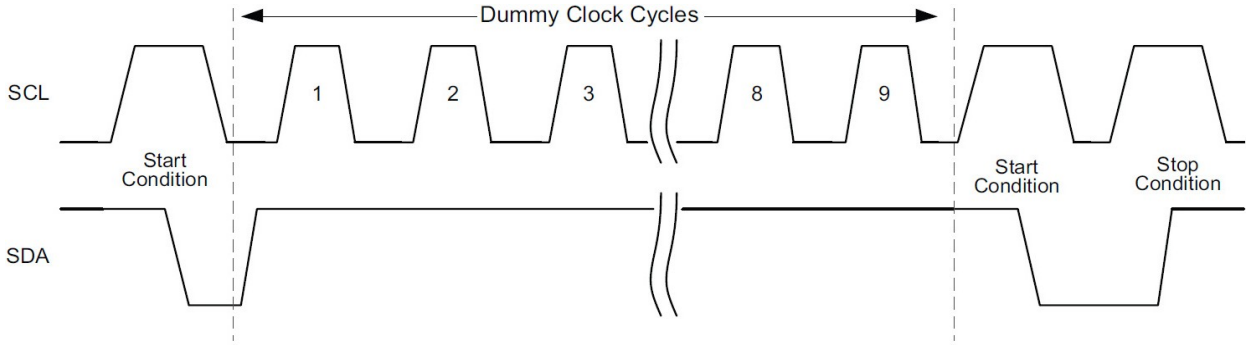
A special condition can be created if SYS_RESET is asserted while eMAG is loading data from bootstrap EEPROM. In such a case, EEPROM buffer address is left at the last read register. If eMAG attempts to load configuration again, it will start fetching bootstrap code from an invalid location and will hang.

To resolve this issue, I2C software reset must be implemented.

6.1.1. Bootstrap EEPROM Software Reset

After an interruption in protocol, power loss, or system reset, any 2-wire part can be protocol reset by following these steps: (a) Create a start bit condition, (b) clock 9 cycles, (c) create another start bit followed by a stop bit (see *Figure 24*). The device is ready for the next communication after the above steps have been completed.

Figure 24: Bootstrap EEPROM Software Reset Sequence



6.1.2. Software Requirements for Bootstrap EEPROM Software Reset

- Upon power on, before BMC enables eMAG power by asserting ATX_PSON_L, it issues bootstrap EEPROM software reset.
- In normal operation mode, if eMAG hang is detected, BMC issues bootstrap EEPROM software reset followed by SYS_RESET.

7. Secure Boot Support

The Hawk board provides two headers to support secure boot. Secure boot requires setting TEST_TMM_ENABLE signal high. External EFUSE_TMM_VDDQ1P8 power supply is required for fuse programming.

Header J8 is used to control TEST_TMM_ENABLE signal (pulled-down to GND by default).

Header J3 can be used to connect external power supply to provide the required 1.8 V for fuse programming.

8. Clocking

eMAG requires two differential and three single-ended clocks.

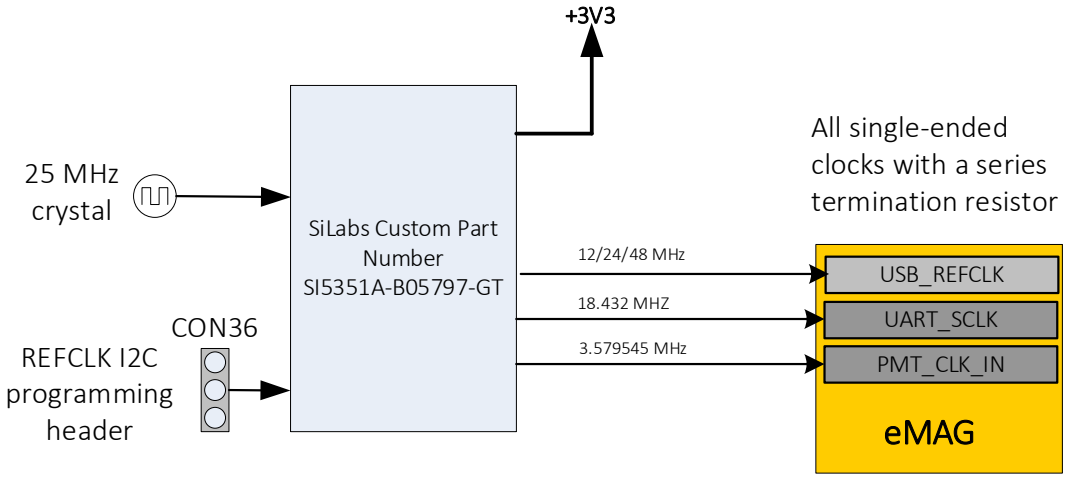
8.1. System Reference Clocks (Differential)

Refer the section titled *PCIe Reference Clock (Differential)* in this document for information on the differential reference clocking scheme used by eMAG on the Hawk board.

8.2. Miscellaneous Reference Clocks (Single-ended)

The Hawk board provides three miscellaneous reference clocks from a SiLabs SI5351A clock generator (refer *Figure 25*). Pre-programmed custom part number is provided for SiLabs device. USB reference clock can be programmed through I2C connector to 12 MHz or 24 MHz (default is 48 MHz). Programming is volatile; it will default to 48 MHz at system power cycle.

Figure 25: Miscellaneous Reference Clocks on the Hawk Board



9. Power Supply and Reset

This section provides detailed information on the power supply sections of the Hawk board.

9.1. eMAG Power Domains and Power Sequencing

Table 21 provides a snapshot of all power rails required for eMAG.

Table 21: eMAG Power Domains and Power Sequencing

POWER BALL	VOLTAGE, V	SEQ #	DOMAIN
VDDC_SOC	0.87	1	SoC
VDDC_PCP	0.93	1A	PCP
VDD18_SOC	1.8	2	SoC
VDD18_PCP	1.8	2A	PCP
VDDQ_DDR0123	1.1, 1.2, 1.35 or 1.5	3	SoC
VDDQ_DDR4567	1.1, 1.2, 1.35 or 1.5	3	SoC
VDD15_SOC	1.5	3	SoC
VDD33_SOC	3.3	3	SoC

These two domains can either be combined or separated. If combined, the following power rails are connected together:

VDDC_PCP > *VDDC_SOC*

VDD18_PCP > *VDD18_SOC*

Every eMAG domain (combined or separated) must observe this power sequence. For separate SoC and PCP domains (implemented on the Hawk board), the following two sequences are observed:

VDDC_SOC > *VDD18_SOC* > *VDDQ_DDR0123, VDDQ_DDR4567* > *VDD15_SOC* >

VDD33_SOC > *SOC_PG* > *SYS_RST_L*

PCP_PWRCTL > *VDDC_PCP* > *VDD18_PCP* > *PCP_PWRGD*

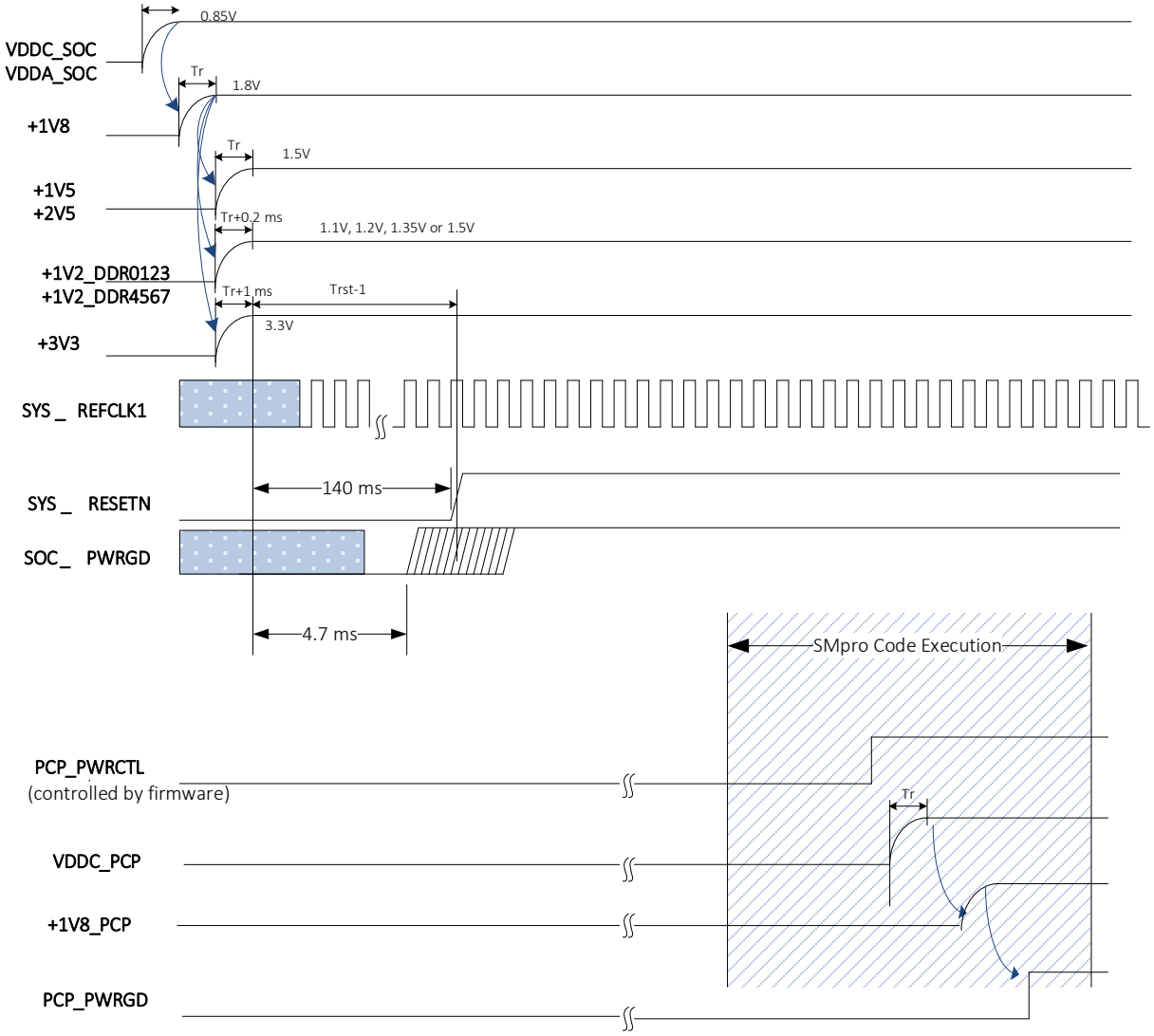
SoC domain power sequence is enabled by the BMC. SoC domain power sequence, in addition to ramping up power supplies, requires providing two system signals: SoC PowerGood to SOC_PWRGD pin of eMAG and System Reset (generated by voltage monitor) SYS_RST_L.

PCP domain power sequence is controlled by SMpro code and is enabled by PCP_PWRCTL pin (VRM_PCP_EN signal). PCP_PWRGD pin requires PowerGood signal from PCP regulators after PCP power sequence is completed.

9.2. eMAG CPU Power Sequencing on the Hawk Board

Figure 26 illustrates the power sequencing for the eMAG CPU on the Hawk board.

Figure 26: Hawk Board Power Sequencing



The Hawk board implements a cascaded regulator power sequencing scheme. PowerGood of one regulator is used to enable next regulator in the chain.

Power on/off is controlled by BMC which is powered from the ATX +5 V standby power.

The Hawk board follows eMAG power sequencing with an additional delay of 0.2 ms for DDR VDDQ VRM and 1 ms for 3.3 V regulator. Additional delay for DDR VDDQ VRM is required to meet DDR4 power sequence requirements (VPP must be ramped before or together with VDDQ). Additional delay for +3.3 V is required as VRMs (+2.5 V and VDDQ) have longer ramp-up time than +3.3 V regulator.

9.3. System Power Chart

Figure 27 provides the typical power numbers for a Hawk board-based system.

Figure 27: Power Chart for a Typical Hawk Board-based System

Hawk / Power Budget / Rev01 / 1 Node		Section		Linear Regulator		Switching regulator										
			Input Rails	P3V3SB	P3V3SB	P5VSB	P12V	P5VSB	P12V	P12V	P12V	P12V	P12V	VDDQxxx_0/1	P12V	P12V
			Input Voltage (V)	3.3	3.3	5.0	12.0	5.0	12.0	12.0	12.0	12.0	12.0	1.2	12.0	12.0
			PWR Efficiency	36%	76%	80%	80%	95%	85%	95%	85%	80%	90%	80%	90%	85%
			Output Voltage (V)	1.2	2.5	1.1	1.5	3.3	1.8	3.3	1.8	0.87	0.93	0.6	1.2	2.5
			Tolerance	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%
	Major Devices	Q'ty	Utility	P1V2_BMC_AUX	P2V5_BMC_AUX	P1V1_BMC_AUX	VDD1V5_SOC	P3V3SB	VDD1V8_SOC	VDD3V3_SOC	VDD1V8_PCP	VDD0V85_SOC	VDD0V85_PCP	VTTxxx_0/1	VDDQxxx_0/1	VPPxxx_0/1
Mother Bo…	eMAG 125 W	1	84%				2.00		1.00	1.00	1.00	6.00	140.00		13.00	
	DDR4 LR-DIMM QRx4 2667 16Gb	8	100%											6.00	50.00	10.00
	BMC AST2500	1	80%	0.50	0.35	0.62		0.12								
	Mezzanine Card x16 PCIe(OCP)	1	100%					0.10								
USB, HDD, PCIe…	USB 2.0	4	50%													
	I210	1	100%													
	PCIe Gen3 x8 (14.4W)	2	40%					0.75								
	SATA 3.5"(Typical 9W)	10	100%													
	SATA 2.5"(Typical 5W)	2	100%													
	NVME SSD(25W)	2	82%													
	M.2	1	95%													
	FAN	6	100%													
	Sections			Linear Regulator		Switching Regulator										
	Summary		Max. total Current (A)	0.50	0.35	0.62	2.00	1.82	1.00	1.00	1.00	6.00	140.00	6.00	66.75	10.00
			Designed Current (A)	0.50	0.40	0.70	2.00	3.00	2.00	1.00	1.00	20.00	140.00	6.00	80.00	10.40
			Solution	PS74801DR	PS74801DR	MP3620A	MP3620A	MP3630	MP3620A	MP3620A	FDS6690A	TPS544B20 RVFR	TPS53679 + CSD95490 x 5	TPS53317	TPS53659 + CSD95496 x 3	MP8733B

Hawk	Directly				Power Supply Rails (AC)				Power (Watt)		
Input Rails	5VSB	3.3V	5V	12V	5VSB	3.3V	5V	12V	Devices Power	Power Dissipation	Power Deliveried
Input Voltage (V)	5	3.3	5	12	5	3.3	5	12			
PWR Efficiency	100%	100%	100%	100%	100%	100%	100%	100%			
Output Voltage (V)	5	3.3	5	12	5	3.3	5	12			
Tolerance	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%	+/-5%			
Major Devices	P5VSB	P3V3	P5V	P12V	P5VSB	P3V3	P5V	P12V			
eMAG 125 W								12.60	135.17	16.01	151.19
DDR4 LR-DIMM QRx4 2667 16Gb								8.42	88.60	12.48	101.08
BMC AST2500		0.19			0.67	0.15			2.55	1.33	3.87
Mezzanine Card x16 PCIe(OCP)		0.60		2.40	0.07	0.60		2.40	31.11	0.02	31.13
USB 2.0			2.00				1.00		5.00		5.00
I210		0.15				0.15			0.48		0.48
PCIe Gen3 x8 (14.4W)		6.00		4.20	0.21	2.38		1.66	28.80	0.05	28.85
SATA 3.5"(Typical 9W)			8.10	4.10			8.10	4.10	89.70		89.70
SATA 2.5"(Typical 5W)			2.00				2.00		10.00		10.00
NVME SSD(25W)		0.00		4.90		0.00		4.02	48.22		48.22
M.2		2.40				2.28			7.52		7.52
FAN				10.08				10.08	120.96		120.96
Sections					PSU Deliveried MaximumCurrent (A)				Total TDP Power (DC)		598 W
Max. total Current (A)		9.34	12.10	25.68	0.95	5.56	11.10	43.28	Max. TDP Power		598 W
Designed Current (A)											
Solution									Deratng 80%		478.40

Figure 27 provides the full system power-up values. Note that CPU power is provided for Turbo Mode. CPU TDP will be limited by cooling capabilities of the system design and is expected to be around 125 W.

DDR power consumption is calculated using Micron Technologies' power calculation spreadsheet.

Note: Total system power consumption is based on a specific Hawk application, which include 1 OCP x16 card, 1 x8 PCIe RAID card, 1 x8 PCIe Ethernet card, 10 SATA 3.5" HDDs, 2 SATA 2.5" HDDs, 2 NVMe SSDs, and 1 NVMe M.2 SSD. If a GPU card (75 W) is used, the system will include 4 SATA HDDs/NVMe, 1 M.2 NVMe card, and 1 x16 PCIe GPU card. The power consumption in this case is lower than the specific application above.

9.4. Power Regulator Capabilities

Table 22 lists the power regulator margins for the Hawk board.

Table 22: Hawk Board Power Regulator Margins

RAIL	SOC	PCP	+1V5	+1V8	+2V5	+3V3	+VDDQxxx0/1	+VTTxxx0/1
Voltage	0.87	0.93	1.5	1.8	2.5	3.3	1.2	0.6
Required Current (A)	6	140	2	2	10	1.82	66.75	6
Capability Current (A)	20	140	2	2	10.4	3	80	6

9.5. System Power Supply Requirements

Based on the system power chart, power numbers are calculated for ATX power supply, the breakdown for which is provided in *Table 23*. An ATX Gold Series 650 W (or above) PSU is recommended.

Table 23: ATX Gold 650 W Power Supply Unit for Hawk (with HDD Storage or GPU)

ATX POWER RAILS	+12 V DC	+5 V DC	+3.3 V DC	+5 V SB
Hawk, A	43.3	11.1	5.6	0.95
650 W ATX, A	54.1	15	15	2.5
650 W ATX, W	649.2	100		12.5

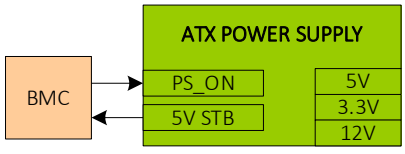
As the table indicates, an 800 W ATX Gold Series power supply meets the requirements for a Hawk board-based eMAG EVK system.

9.6. Power Supply Block Diagrams

9.6.1. Power Supply for the BMC Subsystem

Refer *Figure 28*. The Hawk board powers BMC and its subsystem for ATX +5 V standby rail. BMC is always on as soon as ATX supply standby power is provided. BMC controls PS_ON signal for ATX to power up or power down the rest of the system.

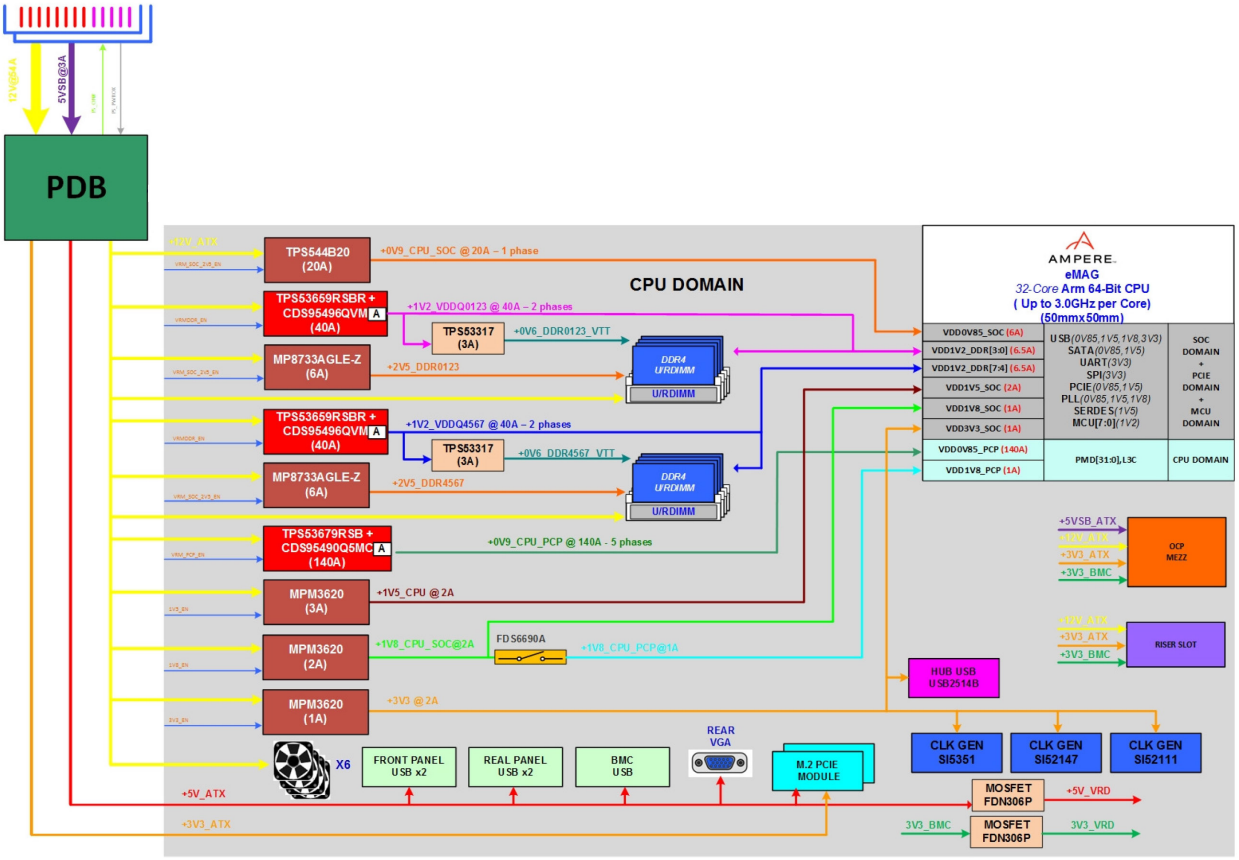
Figure 28: ATX PSON



9.6.2. Power Supply for the SoC and PCP Domains

Figure 29 illustrates the power supply scheme for the SoC and PCP domains on the Hawk board.

Figure 29: Hawk Board SoC and PCP Domain Power Supplies

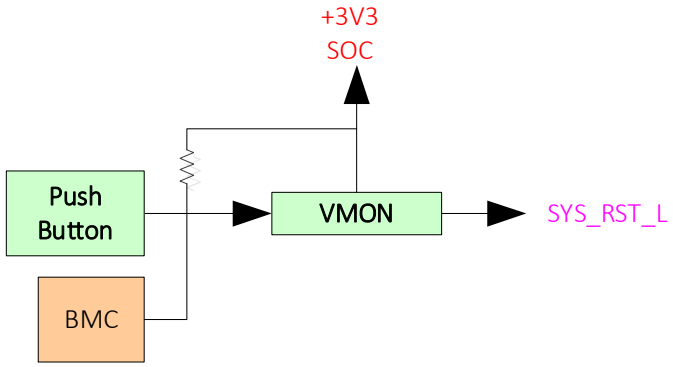


9.7. eMAG System Reset Schematics

Refer *Figure 30*. An eMAG system reset can be asserted from three sources:

- From 3.3 V SoC voltage monitor (when drops below 3.08 V)
- By pressing the Reset push-button switch
- Via BMC using GPIOC6

Figure 30: eMAG System Reset Schemes on the Hawk Board



10. Baseboard Management Controller (BMC)

The Hawk board is equipped with an ASPEED Technology AST2500 Baseboard Management Controller (BMC) which is implemented as a module plugged into a SODIMM socket.

Table 24 lists the features supported by the BMC on the Hawk board.

Table 24: BMC Features Supported on the Hawk Board

#	FEATURE	DESCRIPTION	HAWK
1	IPMI support	–	IPMI/I2C
2	System event log	–	Yes
3	Asset information	–	Yes
4	Sensor monitoring	Voltage, temperature, fans, power supply	Yes
5	Fan speed control	–	Yes
6	Remote management through LAN	Remote power on/off, read SEL, sensor status	Yes
7	Serial Over Lan (SoL)	Console redirection over LAN	Yes
8	SNMP traps	LAN alerts and platform event filtering	Yes
9	Email alerts	–	Yes
10	Remote management through serial	–	Yes
11	Auto recovery from hangs during boot	BMC watchdog timer	Yes
12	Power management	Power capping through node manager based on PMBus	Yes
13	Remote KVM	–	Yes
14	Remote media support	–	Yes
15	Remote firmware upgrade	–	Yes
16	Systems Management Architecture for Server Hardware (SMASH)	Ability to remotely manage a platform independent of machine state, operating system state, server system topology or access method	Yes

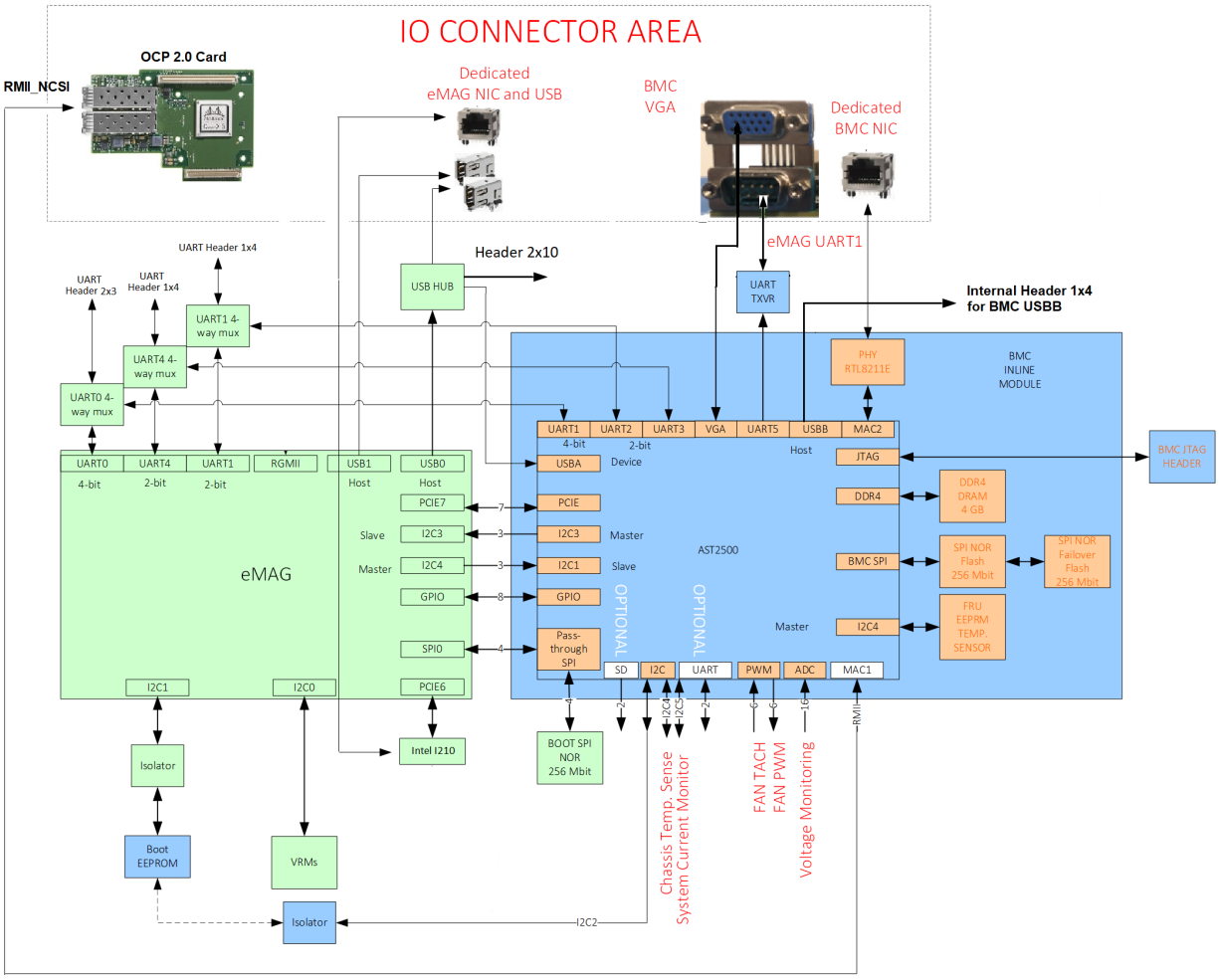
The Hawk board, in general, follows the standard AST2500 System Application, with the exception that it does not utilize any bridge chipsets, but connects the BMC to the CPU SoC peripheral buses.

For more information, please refer the documentation for AST2500 at https://www.aspeedtech.com.

10.1. BMC Block Diagram

Figure 31 shows the connectivity between the eMAG CPU and the BMC on the Hawk board.

Figure 31: eMAG – BMC Connectivity on the Hawk Board



The following features are implemented on the BMC module:

- 512 MB DDR4 Memory
- 256 Mbit BMC boot SPI flash
- 256 Mbit BMC failover boot SPI flash
- MAC2 in RGMII mode with RTL8211E PHY
- FRU EEPROM and BMC module temperature sensor

The following dedicated BMC interfaces are accessible from the Hawk I/O connector area:

- Dedicated BMC gigabit Ethernet port (MAC2 through PHY in RGMII mode)
- Dedicated BMC COM port (UART5)
- Dedicated BMC USB 2.0 host port (port 2B)
- Dedicated BMC out of band (OOB) management port (MAC1 though OCP card in NCSI mode)

The following dedicated BMC interfaces are available as debug headers on the Hawk board:

- BMC JTAG connector with ARM ICE support
- BMC SPI1 programming header

The following main interfaces are used for BMC – eMAG interconnection:

- eMAG I2C3 to BMC I2C3 (BMC Master, CPU Slave), including I2C3_Alert# as output from CPU to BMC
- eMAG I2C4 to BMC I2C1 (BMC Slave, CPU Master), including I2C4_Alert# as input to CPU from BMC
- PCIE7 for graphics over BMC
- BMC USB 2A port is connected in device mode through USB hub to eMAG USB0 port
- eMAG UART0 4 bit to BMC UART1 (can be re-directed 4-way to I/O area connector)
- eMAG UART1 2 bit to BMC UART2 (can be re-directed 4-way to I/O area connector)
- eMAG UART4 2 bit to BMC UART3 (can be re-directed 4-way to I/O area connector)
- Eight GPIOs
- eMAG SPI0 connected through BMC pass-through SPI interface to boot SPI NOR
- eMAG boot EEPROM is connected through a pair of bus isolators to eMAG and BMC. BMC controls which isolator is enabled. In default boot mode, isolator to eMAG is enabled and eMAG reads EEPROM bootstrap data. In remote update mode, eMAG isolator is disabled, and BMC isolator is enabled, allowing BMC to overwrite bootstrap EEPROM content.
- System reset can be generated either by the BMC or via a push-button switch.

The following optional interfaces are supported by BMC module for additional system management:

- 16 channel ADC (is used on Hawk as system voltage monitor).
- Fan PWM and tachometer support: total 8 PWM and 8 TACH signals so that up to 8 system fans can be implemented.
- MAC1 RGMII interface to support NCSI capable network controllers, connected to OCP card
- Three additional UARTs: UART3 (4-bit), and UART4 and UART6 (2-bit each)
- Four additional I2C buses: I2C bus 6-9
- Two SD cards interfaces (assigned GPIO function on Hawk)
- Unused UARTs (3, 4, 6), I2C (6-9), and SD card interfaces can be used as spare GPIO pins

10.2. BMC GPIO Signals

Table 25 lists BMC GPIO signals used on the Hawk board. Signal direction is identified from the BMC's perspective.

Table 25: BMC GPIO Signals Used on the Hawk Board

#	HAWK NET NAME	BMC	eMAG PIN	DIR	ACT.	DESCRIPTION
1	BMC_GPIOG0_CPU_PWROK	GPIOG0	GPIO8	In	High	Set by eMAG to inform BMC that SMpro configuration is done
2	BMC_GPIOG1_BMC_SHD_REQ_L	GPIOG1	GPIO0	Out	Low	Set by BMC to initiate a "graceful shutdown"
3	BMC_GPIOG2_CPU_SHD_ACK_L	GPIOG2	GPIO9	In	Low	Set by eMAG to acknowledge a "graceful shutdown" complete
4	BMC_GPIOG3_CPU_OVERTEMP_L	GPIOG3	OVERTEMP_N	In	Low	Set by eMAG to notify BMC of over-temp. BMC must initiate an eMAG power down
5	BMC_GPIOJ0_HIGHTEMP_L	GPIOJ0	HIGHTEMP_N	In	Low	Set by eMAG to warn BMC of high temp.
6	BMC_GPIOJ1_CPU_FAULT	GPIOJ1	GPIO_FAULT	In	High	Set by eMAG to indicate a non-recoverable failure
7	BMC_GPIOJ2_BMC_SPARE_GPIO	GPIOJ2	GPIO1	TBD	TBD	Spare GPIO between BMC and CPU
8	BMC_GPIOJ3_CPU_REBOOT_ACK_L	GPIOJ3	GPIO10	In	Low	Set by eMAG to notify BMC that software reboot executed from OS
9	I2C3_ALERT_L	SALT3	ALERT3_N	In	Low	Set by eMAG to notify BMC of an event
10	I2C4_ALERT_L	SALT1	ALERT4_N	Out	Low	Set by BMC to notify eMAG of an event on the SSIF interface

#	HAWK NET NAME	BMC	eMAG PIN	DIR	ACT.	DESCRIPTION
11	UART0_MODE0	GPIOC0	–	Out	NA	Selects UART0 4-way mux/ demux mode
12	UART0_MODE1	GPIOC1	–	Out	NA	Selects UART0 4-way mux/ demux mode
13	UART1_MODE0	GPIOC2	–	Out	NA	Selects UART1 4-way mux/ demux mode
14	UART1_MODE1	GPIOC3	–	Out	NA	Selects UART1 4-way mux/ demux mode
15	UART4_MODE0	GPIOC4	–	Out	NA	Selects UART4 4-way mux/ demux mode
16	UART4_MODE1	GPIOC5	–	Out	NA	Selects UART1 4-way mux/ demux mode
17	BMC_GPIOC7_SYS_ATX_PSON_L	GPIOC7	–	Out	Low	ATX supply PSON: BMC asserts Low to enable ATX power supply
18	BMC_GPIOC6_SYS_COLD_RST_L	GPIOC6	–	Out	Low	BMC asserts this signal to generate SYS_RST_L. Signal is input to Hawk +3V3 voltage monitor
19	CHSS_PWR_SW	GPIOD0	–	In	Low	Chassis front panel power switch. When pushed, initiates a “graceful shutdown”. When held for 8 secs, shuts down ATX power supply (SYS_ATX_PSON_L asserted)

#	HAWK NET NAME	BMC	eMAG PIN	DIR	ACT.	DESCRIPTION
20	CHSS_RST_SW	GPIOD1	–	In	Low	Chassis front panel reset Switch. When pressed, initiates a CPU warm reset. When held for 8 secs, asserts SYS_COLD_RST_L to generate a CPU "cold" reset
21	CHSS_FAULT1_LEDC	GPIOD2	–	Out	High	Front panel fault LED1 cathode. BMC asserts this signal to drive system fault LED1
22	CHSS_FAULT2_LEDC	GPIOD3	–	Out	High	Front panel fault LED2 cathode. BMC asserts this signal to drive system fault LED2
23	CHSS_INTRUSION	GPIOD4	–	In	High	Front panel intrusion. Input to BMC, when high indicates that chassis is open
24	CHSS_SYSID_SW	GPIOD5	–	In	Low	Front panel ID switch. Input to BMC from system ID switch. When pressed, BMC sends ID message
25	CHSS_SYSID_LEDC	GPIOD6	–	Out	High	Front panel ID LED cathode. BMC asserts this signal when system ID request is received
26	CHSS_HDD_LEDC	GPIOD7	–	Out	High	Front panel HDD activity LED cathode. BMC toggles this signal when storage activity detected

10.3. BMC – eMAG I/O Isolation

To accommodate for POD (pseudo open-drain) I/O types on eMAG, no eMAG pin can be exposed to high level when the device is not powered up. The Hawk board supports BMC standby mode when only BMC is powered, and full eMAG EVK system is off (ATX supply is powered down). To avoid I/O conflict in this case, provisions listed in the following sections are made.

10.3.1. UART0/UART1/UART4 Isolation

UART0, UART1 and UART4 implement bus re-direction circuit based on analog mux/demux. By default, upon power on, mux/demux is configured to disconnect eMAG UART0, 1 and 4. BMC must assert valid code to enable UART0/UART1 connection. See *Table 7* for valid codes that connect CPU UARTs.

10.3.2. I2C Bus (SCL, SDA)

I2C bus translators/isolators are used for all I2C buses connected between eMAG and BMC (eMAG I2C3 and I2C4).

I2C2 from BMC (I2C1 on eMAG) is used for bootstrap EEPROM. To enable EEPROM remote update, it is connected to BMC 3.3 V and is powered from standby power. I2C1 bus from eMAG is isolated from bootstrap EEPROM unless eMAG SoC 3.3 V is present.

10.3.3. Bootstrap EEPROM

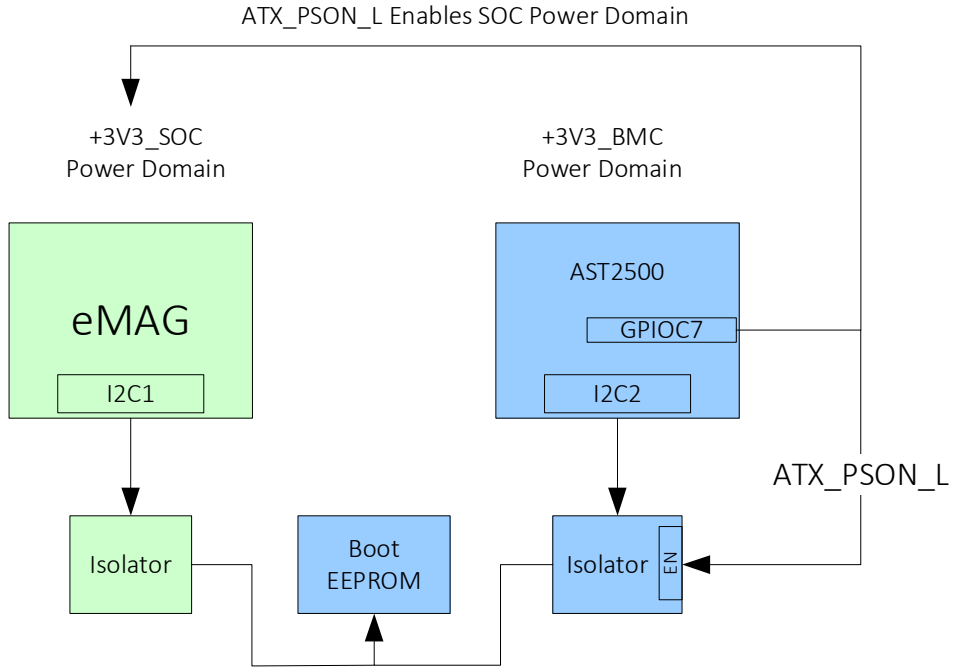
The Hawk board implements bootstrap EEPROM with a provision to update it from BMC (see *Figure 32*).

Bootstrap EEPROM is powered from BMC power domain and can be updated from BMC when the rest of the system is powered down.

When BMC asserts ATX_PSON_L signal to enable ATX power supply (and consequently, eMAG power domains), it disables I2C isolator to bootstrap EEPROM. This way BMC cannot access EEPROM when eMAG power is ON.

eMAG has I2C isolator on its side. This isolator is enabled when eMAG +3.3 V SoC power is present.

Figure 32: Bootstrap EEPROM System Connectivity on the Hawk Board

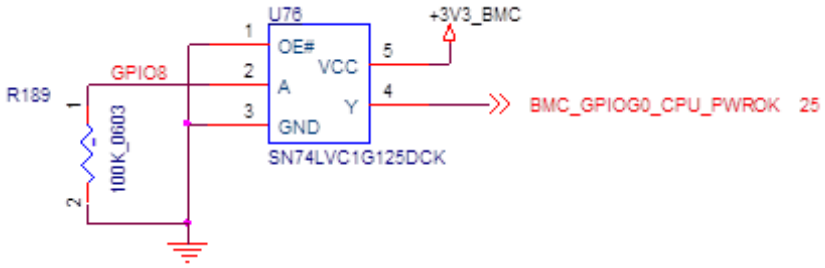


10.3.4. GPIO Isolation

Eight GPIO signals are connected from BMC to eMAG (see *Table 25*). Bus isolator is used so that GPIO signals are disconnected from CPU side unless eMAG SoC 3.3 V is present.

On BMC side, all signals except CPU_POWEROK are pulled up. A special buffer is used for CPU PWROK signal (see *Figure 33*).

Figure 33: CPU PWROK Isolation Circuit



CPU PWROK has a special circuit as this signal is not driven by eMAG until boot EEPROM is read on power up and eMAG is initialized. At power up, pull-down on eMAG GPIO8 signal holds it low. When initialization is complete, eMAG GPIO8 is driven high and overrides the pull-down.

10.3.5. USB and PCIe

PCIe is an AC coupled interface and does not need isolation.

USB port is connected to BMC through USB hub that provides isolation function.

10.3.6. SPI

SPI is connected to pass through interface on BMC. BMC connects to SPI device that is powered from 3.3 V BMC. Three SPI signals (CS, CLK, TX) are output from eMAG and input to BMC; no isolation is needed.

SPI_RX is input from BMC to eMAG. However, SPI MISO signal is tri-stated unless it receives valid command code from SPI host. No isolation is required on SPI_RX signal.

10.3.7. BMC Fan Control

BMC provides fan control functions and can control up to 8 fans. However, the Hawk board supports only 6 fans.

10.3.8. BMC Voltage Monitoring

BMC provides 16 ADC inputs that are used for system level voltage monitoring.

Monitored voltages above 1.8 V must be scaled down to fit 1.8 V ADC full-scale range. The Hawk board implements resistor dividers to scale the voltages to 1.8 V range with head-room for voltage margining (refer *Table 26*).

Table 26: BMC ADC to Hawk Power Net Mapping and Scaling Factors

HAWK POWER NET NAME	ADC	SCALING
+0V9_CPU_SOC	BMC_ADC0	1:1
+1V8_CPU_SOC	BMC_ADC1	1:2
+1V5_CPU	BMC_ADC2	1:1
+2V5	BMC_ADC3	1:2

HAWK POWER NET NAME	ADC	SCALING
+1V2_VDDQ0123	BMC_ADC4	1:1
+1V2_VDDQ4567	BMC_ADC5	1:1
+3V3	BMC_ADC6	1:3
+3V3_CPU	BMC_ADC7	1:3
+0V9_CPU_PCP	BMC_ADC8	1:1
+1V8_CPU_PCP	BMC_ADC9	1:2
+5V_BMC	BMC_ADC10	1:4
+3V3_BMC	BMC_ADC11	1:3
+0V6_DDR0123_VTT	BMC_ADC12	1:1
+0V6_DDR4567_VTT	BMC_ADC13	1:1

10.4. Standard BMC Features

The following tables list the standard BMC features currently supported on the Hawk board, as provided by AMI's MegaRAC software. Feature changes or additions for Hawk are also noted.

10.4.1. Platform Support

Table 27 lists the features that are supported by the Hawk platform.

Table 27: Platform Features Supported by the BMC

FUNCTIONS	SUPPORT	DESCRIPTION	NOTES
DCMI	Y	Supports DCMI revision 1.5	–
IPMI	Y	Supports IPMI 2.0 specification	–
Redfish	Y	Supports Redfish revision 1.5a	–
Remote KVM	Y	Supports HTML5 rKVM aka Remote KVM over LAN	–
SOL	Y	Supports Serial-Over-Lan	–
Multi SOL	Y	Supports for multiple SOL sessions	For CPU, SCP firmware, and ATF
vMedia	Y	Supports virtual drive and USB redirection	Remote media only
Access Method	Y	+ BMC serial console + IPMI 2.0 + Redfish + Browser	–

10.4.2. Networking

Table 28 lists the networking features that are supported by the Hawk platform.

Table 28: Networking Features Supported by the Hawk Board

FUNCTIONS	SUPPORT	DESCRIPTION	NOTES
IPV4	Y	–	–
IPV6	Y	–	–
VLAN	Y	–	–
DHCP	Y	–	–
Static IP	Y	–	–
Ethernet configuration	Y	Provides support for configuring the following: + Link auto-negotiation or specific Link Speed and Duplex Mode + MAC address configuration	–
MAC address storage	Y	Supports persistent MAC address storage (e.g. reading from preconfigured MAC addresses, say from EEPROM)	MAC addresses are stored in FRU EEPROM
DNS	Y	Supports DNS-related configuration	–
DNS registration	Y	Supports registering BMC with DNS server	–
SNMP	Y	Supports SNMP v2/v3	–
SMTP	Y	Supports SNMP trap	–
HTTPS	Y	Support HTTPS only	–
NFS	Y	Supports NFS protocol for mounting external directory (e.g. for storing of logging data)	–
NTP	Y	Supports Network Time Protocol	–
NCSI	Y	Supports Network Connectivity Status Indicator (NCSI) protocol	–
Shared/Dedicated/Failover Management Interface	Y	–	–

10.4.3. Access Control

Table 29 lists the access control features that are supported by the Hawk platform.

Table 29: Access Control Features Supported by the Hawk Board

FUNCTIONS	SUPPORT	DESCRIPTION
User administration	Y	Supports BMC user configuration via WebUI and IPMI
User privilege levels	Y	Supports different user access privileges, e.g. Administrator vs. Operator

FUNCTIONS	SUPPORT	DESCRIPTION
LDAP authentication	Y	Supports authentication via LDAP server
Active Directory authentication	Y	Supports authentication via Microsoft AD server
Radius authentication	Y	Supports authentication via Radius server
SOL security	Y	Supports encryption of SOL sessions
SSL	Y	Supports SSL encryption and certificate management
SSH	Y	Supports remote access to BMC using SSH
Secure web access	Y	Supports HTTPS protocol and WebUI authentication
BMC system firewall	Y	Supports enabling/disabling/configuring BMC system firewall

10.4.4. Security Features

Table 30 lists the security features that are supported by the Hawk platform.

Table 30: Security Features Supported by the Hawk Board

FUNCTIONS	SUPPORT	DESCRIPTION	NOTES
SSL/TLS	Y	Supports SSL/TLS encryption and certificate management	Insecure TLS 1.0 and 1.1 are disabled. TLS 1.2 are used by default
SSH	Y	Supports remote access to BMC using SSH	SSH is disabled by default. Users can enable it from WebUI or IPMI
Secure web access	Y	Supports HTTPS protocol and WebUI authentication	–
BMC system firewall	Y	Supports enabling/disabling/ configuring BMC system firewall	–
SOL security	Y	Supports encryption of SOL sessions	–
SSL/TLS	Y	Supports SSL/TLS encryption and certificate management	Insecure TLS 1.0 and 1.1 are disabled. TLS 1.2 are used by default
SSH	Y	Supports remote access to BMC using SSH	Root access is disabled by default. Users can enable root access via IPMI command.
Secure web access	Y	Supports HTTPS protocol and WebUI authentication	–
BMC system firewall	Y	Supports enabling/disabling/ configuring BMC system firewall	–
IPMI security	Y	Supports only IPMI secure encryption	Remove insecure cipher suites (CS0) completely. Enable CS3, CS17 by default. Disable CS1, CS2, CS6, CS7, CS8, CS11, CS12, CS15 and CS16 by default. Users can enable them if required.

10.4.5. Firmware Update and Configuration Management

Table 31 lists the firmware update and configuration management features that are supported by the Hawk platform.

Table 31: Firmware and Configuration Management Features Supported by the Hawk Board

FUNCTIONS	SUPPORT	DESCRIPTION	NOTES
BMC firmware upgrade	Y	Supports upgrading BMC firmware via BMC WebUI and Yafuflash	–
Configuration preservation	Y	Supports options for preserving all or selected configuration during firmware upgrade. This must include (but is not limited to) the following: + SDR + FRU + SEL + User settings + Network settings + BMC syslog + Other BMC settings	–
Configuration backup	Y	Supports backing-up current configurations and logs to persistent storage	–
Configuration restore	Y	Supports restoring backed up configurations from persistent storage	–
Host firmware upgrade	Y	Supports upgrading host UEFI and SCP firmware via BMC WebUI and IPMI	`$ ipmitool hpm upgrade`
BMC reset	Y	Supports rebooting BMC using IPMI	`$ ipmitool mc reset cold`

10.4.6. Date and Time Management

Table 32 lists the date and time management-related features that are supported by the Hawk platform.

Table 32: Date and Time Management Features Supported by the Hawk Board

FUNCTIONS	SUPPORT	DESCRIPTION
System time configuration	Y	Supports manually configuring date and time
Time zone	Y	Supports configuring time zone
Read date/time directly from RTC	Y	Read date/time from RTC when BMC is booting.
NTP configuration	Y	Supports configuring NTP: Enable/disable, server selection

10.4.7. SDR and Logging

Table 33 lists the SDR and logging features that are supported by the Hawk platform.

Table 33: SDR and Logging Features Supported by the Hawk Board

FUNCTIONS	SUPPORT	DESCRIPTION	NOTES
Support for IPMI access to BMC SEL and SDR	Y	–	–
Support for WebUI access to BMC SEL and SDR	Y	–	–
Support for SEL filtering and clearing	Y	–	–
Support for storing event logs locally and remotely	Y	–	–
SOL console log capture	Y	Supports capturing SOL console log	CPU console log only

10.4.8. FRU Support

Table 34 lists the FRU support features that are supported by the Hawk platform.

Table 34: FRU Support Features Provided on the Hawk Board

FUNCTIONS	SUPPORT	DESCRIPTION
FRU initialization	Y	Supports FRU table initialization via WebUI and IPMI
FRU table format	Y	System/Product Information: - Manufacturer - Product Name - Product Model Number - Serial Number - Asset Tag
	Y	Board Information: - Manufacturer - Board Name - Board Revision - Serial Number - Asset Tag

10.4.9. Hardware Health Detection and Monitoring

Table 35 lists the hardware health detection and monitoring features that are supported by the Hawk platform.

Table 35: Hardware Health Detection and Monitoring Features Supported by the Hawk Board

FUNCTIONS	SUPPORT	DESCRIPTION	NOTES
Hardware health monitoring	Y	Via WebUI and IPMI	–
On-board temperature sensors	Y	–	–
On-board power sensors	Y	–	–
On-board voltage sensors	Y	–	–
Chassis temperature	Y	–	–
Chassis power	Y	–	–
Fan speed monitoring	Y	Supports displaying individual fan speeds	–
Fan control	Y	Supports auto and manual fan control	Ampere default fan algorithm is implemented. OEM/ODM will support their own fan algorithm depending on chassis type. Manual fan control is provided via IPMI command

10.4.10. Chassis Control

Table 36 lists the chassis control features that are supported by the Hawk platform.

Table 36: Chassis Control Features Supported by the Hawk Board

FUNCTIONS	SUPPORT	DESCRIPTION	NOTES
System power on/off	Y	Supports powering on/off the chassis via WebUI and IPMI	`$ ipmitool chassis power on/off/cycle/ reset`
System graceful shutdown	Y	Supports graceful shutdown of the system	–
System immediate shutdown	Y	Supports immediate shutdown of the system	–
Power button	Y	Supports powering on/off chassis via power button	–
Host shutdown command	Y	Supports graceful shutdown via host “power off” or “shutdown” command	–

FUNCTIONS	SUPPORT	DESCRIPTION	NOTES
System soft reset	Y	Supports system reset	Equivalent to reset command from host kernel
System power cycle	Y	Supports power cycling the system	Equivalent to a graceful shutdown followed by a power on
Power loss policy	Y	Supports the following power loss policy: + Always on [Default] + Always off + Previous	Configurable via Aptio® V
LED control	Y	Provide controls of UID and system error LEDs	–

10.4.11. Alerts and Notifications

Table 37 lists the alerts and notifications related features that are supported by the Hawk platform.

Table 37: Alerts and Notifications-related Features Supported by the Hawk Board

FUNCTIONS	SUPPORT	DESCRIPTION
LAN alert via SNMP trap	Y	–
Email alert	Y	–
Alert policy configuration	Y	Provides support for enabling/disabling alert types and alert level prioritization

10.4.12. WebUI

Table 38 lists the WebUI features that are supported by the Hawk platform.

Table 38: WebUI Features Supported by the Hawk Board

FUNCTIONS	SUPPORT	DESCRIPTION	NOTES
Dashboard	Y	Show firmware and network information	HTML5 WebUI
FRU information	Y	Display FRU contents	–
Sensor reading report	Y	Display all sensor status and their current values	–
Event log report	Y	Display all event log. Support option to save or clear event log	–
System and audit log	Y	Display system log and audit log	–
Network configuration	Y	Configure IPV4, DNS, …	–
Image redirection	Y	Supports remote media only.	–
Console redirection	Y	Supports HTML5 console redirection	H5Viewer only
Server power control	Y	Supports reset, power on/off, power cycling the server	–
Auto video recording	Y	–	–

FUNCTIONS	SUPPORT	DESCRIPTION	NOTES
Configuration preservation/ restoration	Y	Supports preserving/backing up and restoring BMC configuration	–
System administrator	Y	Allows the user to enable/disable access and change the password for the system administrator account.	–
Firmware update	Y	Supports updating BMC, SCP and UEFI firmware	–
Dual image configuration	Y	Configure which image is booted.	–

10.5. eMAG – BMC Connectivity and Communication

This section describes the high-level interface specification for supporting a BMC on the eMAG-based Hawk platform. The specification focuses on the high-level hardware and software requirements to support a BMC on Hawk.

BMC designs are, in general, a result of system-level architectural requirements. These are intended merely as guidance and do not represent requirements of the eMAG processor.

10.5.1. eMAG to BMC Hardware Connectivity

The generic hardware connectivity requirements between eMAG and the BMC involve the following:

1. An SMBus-based **I2C_0**[2] bus must be configured as a master and attached to an I2C port of the BMC configured as slave. This is a link between the processor and the BMC for host-initiated requests. This interface is used as the SMBus System interface (SSIF) between the processor and the BMC.
2. For SSIF connection between eMAG and the BMC, the eMAG I2C_0's ALERT_N[3] input must be connected to a BMC's output (BMC_I2C_ALERT_L) which functions as an SMBALERT (ALERT_N) signal from the BMC. The BMC will use this signal to alert the eMAG host when it wants to send a message to the host over the SSIF interface.[4]
3. A second SMBus-based **I2C_1** bus must be used to connect the eMAG processor to another I2C bus of the BMC. The processor's I2C_1 port is configured as an I2C slave and a BMC's I2C port is configured as a master. This is a point-to-point link between the BMC and the processor for BMC-initiated requests.
4. The eMAG I2C_1's SMBALERT (ALERT_N) output pin is used as the SMBALERT signal to alert the BMC of critical events or errors.
5. The processor's UART0 must be used to pipe the processor's console output to the BMC to support the Serial Over LAN (SOL) functionality with a remote management station.
6. An eMAG GPIO output (CPU_PWROK_L), acting as a "Software Ready" signal, must be connected to an input GPIO of the BMC to tell the BMC that the system is ready for communications with the BMC.

[2] The numbering of I2C busses is used for illustration purpose. The actual bus used depends on the hardware design.
[3] The ALERT_N mnemonic is used generically to denote the I2C SMBALERT# input or output pins.
[4] In case the I2C controller does not support the SMBALERT# signal, this can be replaced with the GPIO signal.

7. The IRQ_IN_0 input signal must be connected to an output GPIO (BMC_SHD_REQ_L) of the BMC which functions as a graceful shutdown request signal from the BMC. On receiving this signal, the processor will perform a graceful shutdown.
8. A processor's GPIO output (CPU_SHD_ACK) is to be connected to a GPIO interrupt input of the BMC. This is used to inform the BMC that eMAG has completed a graceful shutdown, either previously triggered by the BMC via the BMC_SHD_REQ_L mentioned above, or by the software. The BMC in turn must power of the PSU on receipt of this signal.
9. A processor's GPIO output (CPU_REBOOT_ACK_L) is to be connected to a GPIO interrupt input of the BMC. This is used to inform the BMC that eMAG reboot executed from the OS.
10. The processor's $\overline{\text{SYS\_RESET}}$ signal must be connected to the BMC, so it can reset the processor.
11. The $\overline{\text{OVERTEMP}}$ output signal from the processor must be connected to the BMC to alert it of a critical temperature condition requiring a power shutdown.
12. A GPIO output of eMAG (CPU_HIGHTEMP_L) also known as *Internal HIGHTEMP*, must be connected to a BMC's GPIO interrupt input. The processor uses this pin to alert the BMC of a HIGHTEMP condition as monitored by the processor. The processor monitors the HIGHTEMP condition by sampling its on-die sensors and determined by the highest temperature among those. When this temperature reaches the HIGHTEMP threshold, the processor will pull low this GPIO and scale the CPU frequency down in steps of 100 MHz every 15 ms until reaching 400 MHz. If the temperature goes below the threshold during this time, the processor will drive this GPIO high to signal the clearing and start scaling up its frequency in 100 MHz-steps every 15 ms until the CPU reaches normal operating frequency again.
13. The $\overline{\text{HIGHTEMP}}$ signal of the processor (also known as *External HIGHTEMP*) is bidirectional and is an input pin by default. This signal must be connected to the BMC's GPIO output, and it is used by the BMC to notify the processor of a HIGHTEMP condition as determined by the BMC. The $\overline{\text{HIGHTEMP}}$ signal is also driven by the SoC VRD's and PMD VRD's $\overline{\text{VRHOT}}$ signals. When eMAG detects the external HIGHTEMP signal, it will scale the CPU frequency down to 400 MHz until the signal is cleared.
14. When operating in bi-directional mode (in which case the CPU_HIGHTEMP_L above is not needed), this signal driven as an output by the CPU only when the firmware detects a high temperature condition.

10.5.2. GPIO Table

Table 39 provides a more detailed description of the signals described in the previous section.

Table 39: GPIO Assignments

MNEMONICS[5]	SIGNAL	ALT	DIR FROM eMAG	LEVEL	COMMENTS
CPU_PWROK	GPIO	–	OUT	HIGH	Set by the host to inform the BMC of the host's power status: HIGH if host power is OK
BMC_SHD_REQ_L	IRQ_IN_0	None	IN	LOW	Input to host from BMC to request a "graceful shutdown", LOW level triggered
CPU_SHD_ACK_L	GPIO	–	OUT	LOW	Output from host to BMC. Asserted LOW to acknowledge shutdown request from BMC. eMAG also asserts this when it completes a soft shutdown request from the OS.
CPU_REBOOT_ACK_L	GPIO	–	OUT	LOW	Output from host to BMC. Asserted LOW to notify BMC that software reboot executed from OS.
CPU_OVERTEMP_L	OVERTEMP	–	OUT	LOW	Output LOW from host to BMC to indicate an OVERTEMP event, which will initiate a power off sequence for the entire SoC.
BMC_SYS_COLD_RST_L	SYS_RESET	–	IN	LOW	Input to host from the BMC or reset push button. Asserted LOW to reset host.
CPU_I2C_ALERT	ALERT_N	–	OUT	LOW	Output from host to BMC to notify the BMC of an event on the I2C slave bus.
CPU_HIGHTEMP_L	GPIO	–	OUT	LOW	Output HIGH from host to BMC to alert a HIGHTEMP condition.

[5] Mnemonics might not match but are similar to schematics names.

MNEMONICS[5]	SIGNAL	ALT	DIR FROM eMAG	LEVEL	COMMENTS
BMC_HIGHTEMP_L	HIGHTEMP	–	IN	LOW	BMC drives the signal LOW to trigger a HIGHTEMP condition to host Note: This signal also may be connected to BMC's input pin to inform this VRD's high temp event to BMC.
BMC_I2C_ALERT_L	ALERT_N	–	IN	LOW	LOW level triggered from BMC to host to notify the host of an event on the SSIF interface.
CPU_FAULT	GPIO	–	OUT	HIGH	HIGH level triggered from host to BMC to indicate a major CPU fault. Currently not implemented.

10.6. Other Design Considerations

- The boot EEPROM must be connected to an I2C bus configured as Master on the processor's side, preferably on its own bus by itself.
- There might be board-specific requirements to allow the BMC to access the boot EEPROM for firmware upgrade. In this case, additional circuitry might be needed to allow the boot EEPROM to be connected to one of the BMC's master I2C interface.
- The BMC must be connected directly to the I2C_X bus and not through any I2C mux or expander.
- Slave devices accessible and controlled directly by the BMC are to be connected to a BMC's I2C bus configured as Master. Examples of these devices include the fan controller, FRU EEPROM, ambient temperature sensor, and other additional on-board thermal and power sensors.
- Slave devices accessible and controlled directly by the eMAG processor are to be connected to a processor Master I2C bus. These devices include, but are not limited to, the SFP+ modules, RTC, or GPIO expander, etc.
- The RTC device, if present, needs to be connected to a processor's Master I2C bus under the control of SMpro.
- LED controller, if present, needs to be connected to a processor's Master I2C bus under the control of SMpro.
- The $\overline{\text{EVENT}}$ output signal from SPD DDR EEPROM is to be connected to an ALERT_N (I2Cx_ALERT_L) input of eMAG to notify it of any DDR critical temperature events.
- The $\overline{\text{ALERT}}$ output signals from the SoC VRD, PMD VRD, and DDR VRD(s) must be connected to the PMBUS_ALERT_L input signal to alert eMAG of critical power conditions.
- The $\overline{\text{VRHOT}}$ output signals from the DDR VRD(s) are also to be connected the PMBUS_ALERT_L signal.

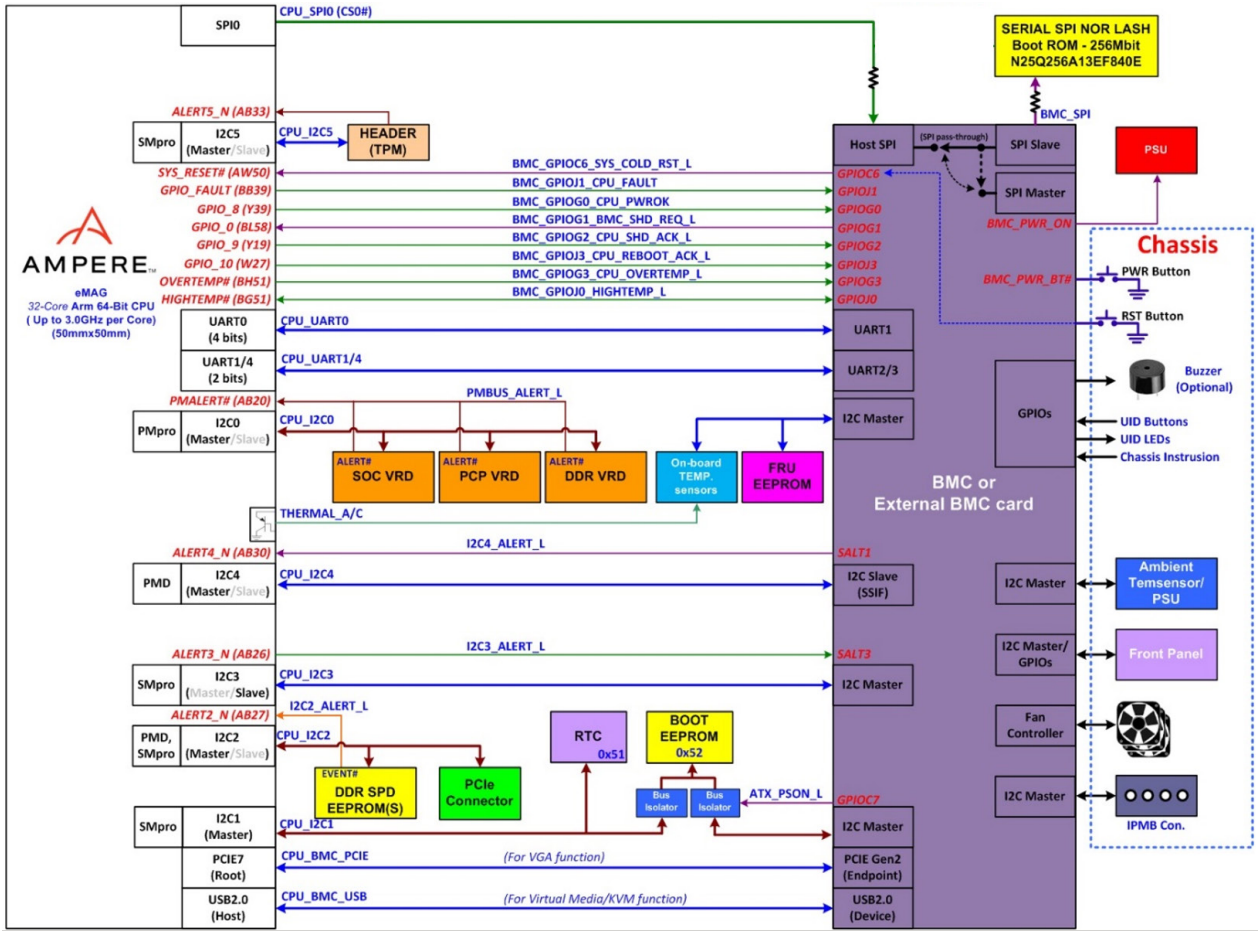
Table 40 summarizes the use of the alert signals in addition to the ones mentioned in *Table 39* above.

Table 40: Additional Alert Signals

MNEMONICS	SIGNAL	ALT	DIR FROM eMAG	LEVEL	COMMENTS
PMBUS_ALERT_L	PMALERT	–	IN	LOW	LOW level triggered to be used to notify the host about events from I2C device(s) connected to I2C1 bus such as VRD's high temp.
I2Cx_ALERT_L	ALERT_N	–	IN	LOW	Alert signal input from DIMM's $\overline{\text{EVENT}}$ pin(s) that indicate DIMM temperature is higher than warning threshold.

Figure 34 illustrates the eMAG to BMC connectivity requirements.

Figure 34: eMAG BMC Hardware Connectivity



10.7. eMAG to BMC Communication

10.7.1. SMBus

The System Management Bus (SMBus) is a two-wire interface by which various system components can communicate with each other.

As described previously, the eMAG processor must be connected to the BMC via its I2C slave interface on the SMBus. The BMC must always be an I2C master and eMAG must always be an I2C slave on this bus. To the BMC, eMAG is seen as an I2C slave device providing a set of I2C registers for the BMC to query different thermal sensors and VRD telemetry data such as VRD output power, VRD temperature, or sensors/system event configuration as supported by the eMAG software. Since the BMC is the I2C master and eMAG is the slave, the BMC will always issue I2C Master read requests and eMAG will respond to those requests in the same read transaction.

The eMAG processor must also be connected to another I2C interface of the BMC using another I2C bus. eMAG will be the I2C master and the BMC I2C slave on this bus. To the eMAG processor, the BMC is seen as one of an I2C slave devices on this I2C bus. This connectivity will be used for any host-initiated communications with the BMC.

The SMBus standard specifies an optional signal, $\overline{\text{SMBALERT}}$, which is an interrupt line for devices that want to trade their ability to master for a pin. $\overline{\text{SMBALERT}}$ is an active-low wired-OR signal just like the $\overline{\text{SMBCLK}}$ and the $\overline{\text{SMBDAT}}$ signals are. $\overline{\text{SMBALERT}}$ is used in conjunction with the SMBus General Call Address. Whenever eMAG needs to initiate communication with the BMC, it asserts the $\overline{\text{SMBALERT}}$ interrupt to the BMC.

When multiple processors are controlled by a single BMC, there will be only one interrupt line per eMAG, with the multiple interrupt lines wire-ORed to the BMC for $\overline{\text{SMBALERT}}$. The BMC will process the interrupt and simultaneously access all $\overline{\text{SMBALERT}}$ devices through the Alert Response Address (ARA). Only the device(s) which pulled $\overline{\text{SMBALERT}}$ low will acknowledge the ARA. In the one device per interrupt case, it will be the same eMAG device that always acknowledges the ARA.

10.7.2. Out-of-band Communication

As per the Intelligent Platform Management Interface (IPMI) specification, in the out-of-band communication mode, a remote management station connects to the BMC via the BMC's "out-of-band" interfaces (e.g., LAN port).

eMAG does not support Intelligent Platform Management Bus (IPMB). Access to the on-board BMC is via the BMC's management Ethernet or serial port. For example, the network manager could run remote management software or IPMI-related tools such as IPMItool on his/her workstation and send an IPMI command to a specific BMC. The remote software opens-up a network connection directly to the BMC and works on standard RMCP (Remote Management Control Protocol) for the given commands.

10.7.3. In-band Communication

As per the IPMI Specification, in the in-band communication mode, access to the BMC is via the processor's "system" interfaces. IPMI defines standardized system interfaces that system software can use to pass IPMI messages to the BMC. These interfaces are KCS, SMIC, BT and SSIF. eMAG only supports SSIF over I2C/SMBus.

In the In-band mode of operation as defined by IPMI, applications need to communicate with the BMC using the `/dev/i2c-x` SSIF interface provided by eMAG Linux kernel.

10.8. Detailed Software Functions

10.8.1. Host-to-BMC Communications

Communications between host applications and the BMC is to be made using IPMI over the SSIF `/dev/i2c-0`[6] interface using the BMC's slave address.

10.8.2. BMC-to-eMAG Communications

Communications between BMC and eMAG are accomplished via the eMAG Register Map. The BMC can query for sensor data and status by reading the eMAG Register Map over its I2C master interface connected to the eMAG I2C slave.

10.8.3. Error Detection and Reporting

eMAG will notify the BMC of critical or catastrophic errors by triggering a SMBALERT. Errors/events that would trigger an alert to the BMC are:

- System events such as platform booting/reset etc.
- Thermal and power events
- PMD/CPU errors
- Memory errors
- PCIe errors
- SATA errors
- Other I/O errors
- ACPI state changes

On receipt of the alert, the BMC will need to access the Register Map's General-Purpose Interrupt (GPI) source register to identify the source of the errors and then read the associated GPI Status Register to learn about the details of the error.

[6] Software needs to be implemented such that the kernel would enumerate the I2C bus used for SSIF communications as `/dev/i2c-0` for consistency across all boards.

10.8.4. Fail Safe

During the boot-up process, the system may not be able to boot-up correctly if there are any hardware issues such as:

- Wrong voltage level of PMD/SOC/DRAM (changed manually)
- Incorrect DRAM parameters (speed/interleaving mode etc.) resulting in incorrect configuration

This would affect the processor's boot-up process without any scope for recovery. Hence, in order to mitigate such a situation, software implements the fail-safe[7] feature in which the system will boot itself with the default settings after a certain number of boot failures.

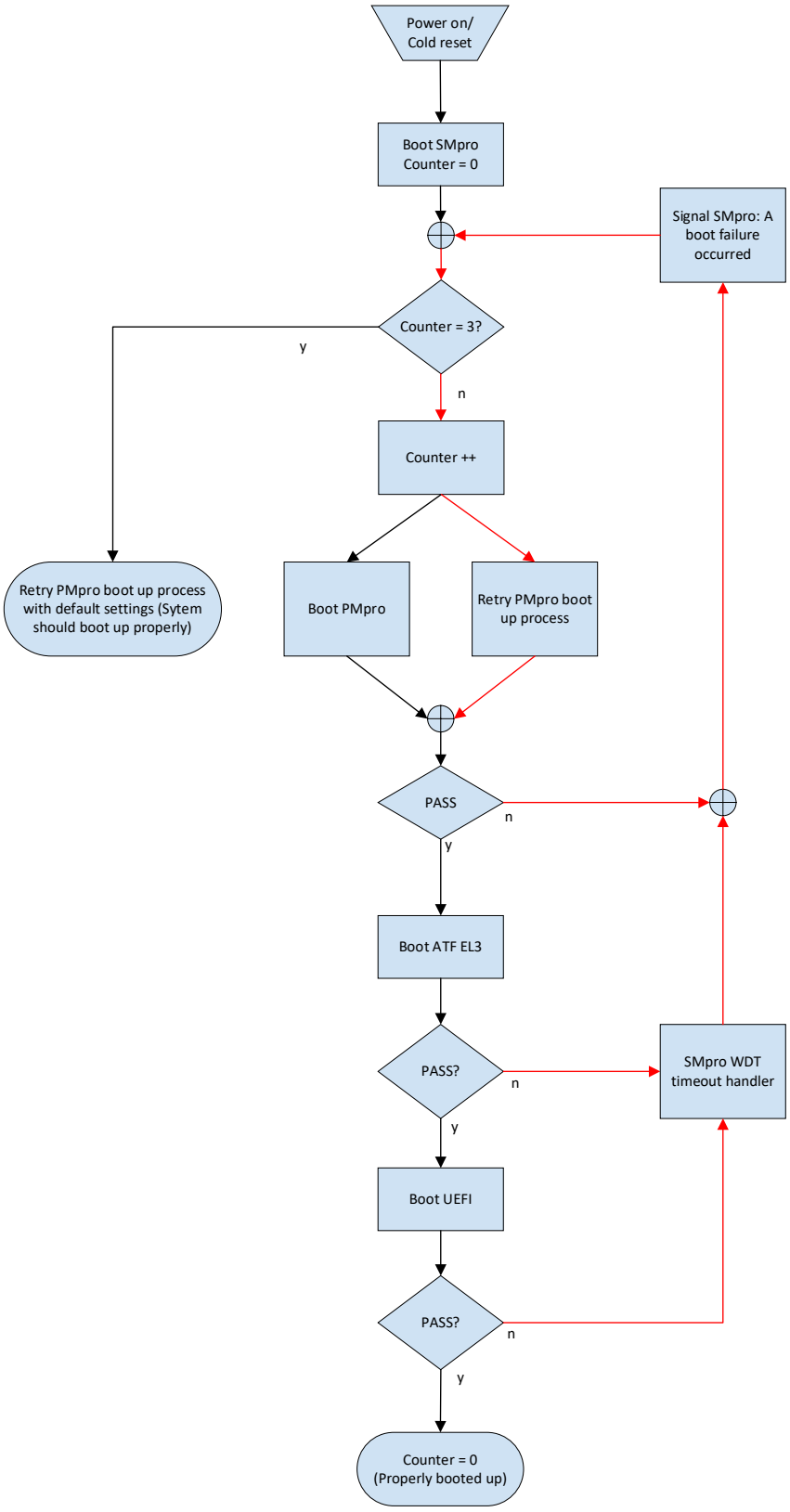
The failsafe feature is implemented on SMpro which will always boot. SMpro maintains a counter, which is initialized to 0 upon either power on or cold reset. After SMpro boots up properly and is ready to boot PMpro, the counter is set to 1. If the system boots up in a clean manner to a stage which is considered good (and which is now defined at the end of the UEFI BIOS stage in the boot process), the counter is cleared, and this indicates that the system has booted successfully. If the boot failure reaches its maximum set limit, SMpro restarts the boot process in fail-safe mode. This failsafe boot mode state is propagated to all the software components in the boot process – PMpro, ARM TF and UEFI.

The boot failure limit is stored in non-volatile storage. By default, the retry count is 3.

[7] Fail Safe is a new feature of BMC and it is available for the eMAG processor only.

Figure 35 illustrates the sequence of the Failsafe operation.

Figure 35: Fail-Safe Operation Sequence



10.9. eMAG Register Map

10.9.1. Logical Sensor Definitions

eMAG firmware provides the framework for accessing sensors using a functional model where board-specific firmware reports logical sensor data via the eMAG I2C Register Map. This is to help with faster migration of existing BMC firmware to supporting eMAG-based boards as well as the ability to leverage the same BMC firmware for different eMAG-based boards.

Table 41 lists the logical sensor definitions.

Table 41: Logical Sensor Definitions

SENSOR NAME	SENSOR TYPE	COMMENTS
SoC temp	Temp	Average temperature in °C as reported by the SoC on-die sensors.
PMD VRD temp	Temp	Highest temperature in °C as reported by the VRD controllers providing power to the PMD voltage rail
SoC VRD temp	Temp	Highest temperature in °C as reported by the VRD controllers providing power to the SOC voltage rail
DIMM VRD temp	Temp	Highest temperature in °C as reported by the VRD controllers providing power to the DIMMs
CH0 DIMM temp	Temp	Highest temperature in °C as reported by the DIMMs on CH0
CH1 DIMM temp	Temp	Highest temperature in °C as reported by the DIMMs on CH1
CH2 DIMM temp	Temp	Highest temperature in °C as reported by the DIMMs on CH2
CH3 DIMM temp	Temp	Highest temperature in °C as reported by the DIMMs on CH3
CH4 DIMM temp	Temp	Highest temperature in °C as reported by the DIMMs on CH4
CH5 DIMM temp	Temp	Highest temperature in °C as reported by the DIMMs on CH5
CH6 DIMM temp	Temp	Highest temperature in °C as reported by the DIMMs on CH6
CH7 DIMM temp	Temp	Highest temperature in °C as reported by the DIMMs on CH7
PMD VRD power	Power	Total power output in watt as reported by the VRD controllers providing power to the PMD voltage rail
PMD VRD power mW	Power	The milliwatt portion of the PMD VRD power above
SoC VRD power	Power	Total power output in watt as reported by VRD controller providing power to the SOC voltage rail
SoC VRD power mW	Power	The milliwatt portion of the SoC VRD Power output above
DIMM VRD1 power	Power	Total Power output in Watt as reported by the first VRD controller providing power to the DIMMs
DIMM VRD1 power mW	Power	The milliwatt portion of DIMM VRD1 Power above
DIMM VRD2 power	Power	Total Power output in Watt as reported by the second VRD controller providing power to the DIMMs
DIMM VRD2 power mW	Power	The milliwatt portion of DIMM VRD2 Power above

SENSOR NAME	SENSOR TYPE	COMMENTS
PMD VRD voltage	Voltage	Voltage in millivolt reported by VRD controllers providing the voltage to PMD voltage rail
SoC VRD voltage	Voltage	Voltage in millivolt reported by VRD controllers providing the voltage to SoC voltage rail
DIMM VRD1 voltage	Voltage	Voltage in millivolt reported by first VRD controllers providing the voltage to DIMM voltage rail
DIMM VRD2 voltage	Voltage	Voltage in millivolt reported by second VRD controllers providing the voltage to DIMM voltage rail

10.9.2. Extended LM75 Format

The command/address (offset) format and access mechanism from the BMC to I2C registers as provided by the eMAG register map is based on the National Semiconductor LM75 format.

However, the LM75 format imposes two limitations:

- The specification of the Pointer Register (to select which registers to read/write) only allows 2 bits for this selection, limiting the number of accessible registers to 4.
- The returned value for a temperature is only one byte, allowing for reported temperature within the range of 0-125.

To accommodate a wider range of (logical) functions and customer requirements, eMAG I2C register maps remove the above restrictions.

- The Pointer Register can use up to 8 bits allowing the selection of up to 256 registers
- The data value uses 2 bytes instead of 1 byte

Refer *Table 44* for more information.

10.9.3. I2C Register Map Definitions

Note: Each register is 16-bit (2-bytes) wide.

10.9.3.1. System GUID

The system GUID is not included in the Register Map but is documented in *Table 42* as a reference.

Table 42: System GUID

DEVICE	GUID
eMAG	bb32a94e-5482-4680-ab64-5cf5984f429c

10.9.3.2. Capability Registers

The Capability registers provide various types of product or model information about the underlying hardware and firmware. This includes firmware version, Register Map version, and the functions currently supported by the firmware.

Table 43 describes the Capability registers in detail.

Table 43: Capability Registers

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x0	Register spec version	0x4	R	0	Major version of this specification (in hex). For example, if the version of this spec is 4.0, then this value would be 0x04.
		0x0	R	A	Minor version of this specification (in hex) For example, if the version of this spec is 4.10, then this value would be 0x0A.
0x1	SMpro version	–	R	0	Major firmware version (in hex) of SMpro firmware version with BMC support.
		–	R	1	Minor firmware version (in hex) of SMpro firmware version with BMC support.
0x2	Manufacturer ID	–	R	0	Manufacturer ID, LSB first, binary encoded. This is the IANA 'Private Enterprise' ID following IPMI spec for Manufacturing ID. For example, the ID for Ampere is 1458 decimal, which ix 0x5B2, which would be stored in this record as 0xB2, 0x05 respectively.
		–	R	1	–
0x3	Device ID	0x2	R	0	Device ID: 0x4 for eMAG
		0x0	R	1	Reserved
0x4	Product ID	0x8840	R	0..1	Byte 0-1: Product ID, LSB First. This field can be used to provide a number that identifies a specific board from a specific manufacturer (as specified by the Manufacturer ID field)
0x5	Analog sensor support	–	R	0	Analog Sensor Support 0: Reserved 1: SoC VR temp 2: DIMM VR temp 3: PMD VR temp 4: DIMM temp 5..7: Reserved
		–	R	1	0: MemHot Threshold 1: SoC VR Hot Threshold 2..7: Reserved

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x6	Analog power sensor support	–	R	0	0: DIMM VR1 power 1: DIMM VR2 power 2: PMD_VR_Power 3: SoC_VR_Power 4...7: Reserved
		–	R	1	Reserved
0x7	Analog voltage sensor support	–	R	0	0: DIMM VR1 voltage 1: DIMM VR2 voltage 2: PMD VR voltage 3: SoC VR voltage 5...7: Reserved
		–	R	1	Reserved
0x8	Other capabilities	–	R	0	0: ACPI P-State support 1: ACPI CPPC support 2..7: Reserved Note: ACPI P-State support and ACPI CPPC support are mutually exclusive features. Only one of them can be supported at a time. These feature bits must only be checked after the OS boots up, since P-State or CPPC support depends on the OS configuration.
		–	R	1	Reserved
0x9 – 0xF	–	–	–	–	Reserved

10.9.3.3. Sensor Registers

The Sensor registers of the Register Map provide information about the logical sensors.

Note: Make sure to read the associated Analog Sensor Support registers above to determine if a sensor is supported (analog sensor support bit set to 1). If the sensor is supported, then bit 7 of byte 1 of the corresponding sensor register is used to indicate whether the value is valid (0) or invalid (1).

A sensor is invalid if:

- It is not supported (per Analog Sensor Support register bit)
- It is not present (such as a missing DIMM) or if the sensor is not supported by the (replaceable) device (such as lack of support by the DIMM type for temperature reading)
- 0xFFFF value is returned when reading this sensor value

Table 44 describes the Sensor registers in detail.

Table 44: Sensor Registers

REGISTER ADDRESS	REGISTER NAME	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x10	SoC temperature	R	0	9-bit temperature in °C, range from -255 to 256 Byte0: LSB of the temperature Bit 0-7: Temperature
		R	1	Byte1: MSB of the temperature Bit 0: Temperature Bit 1-7: Reserved
0x11	SoC VRD temp	R	0..1	Same format as I2C register (SoC temperature) Highest temperature as reported by the SoC VRDs
0x12	DIMM VRD temp	R	0..1	Same format as I2C register (SoC temperature) Highest temperature as reported by the DIMM VRDs
0x13	PMD VRD temp	R	0..1	Same format as I2C register (SoC temperature) Highest temperature as reported by the PMD VRDs
0x14	CH0 DIMM temp	R	0..1	Highest temperature among DIMM0 and DIMM1 on CH0 Same format as I2C register (SoC temperature)
0x15	CH1 DIMM temp	R	0..1	Highest temperature among DIMM0 and DIMM1 on CH1 Same format as I2C register (SoC temperature)
0x16	CH2 DIMM temp	R	0..1	Highest temperature among DIMM0 and DIMM1 on CH2 Same format as I2C register (SoC temperature)

REGISTER ADDRESS	REGISTER NAME	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x17	CH3 DIMM temp	R	0..1	Highest temperature among DIMM0 and DIMM1 on CH3 Same format as I2C register (SoC temperature)
0x18	CH4 DIMM temp	R	0..1	Highest temperature among DIMM0 and DIMM1 on CH4 Same format as I2C register (SoC temperature)
0x19	CH5 DIMM temp	R	0..1	Highest temperature among DIMM0 and DIMM1 on CH5 Same format as I2C register (SoC temperature)
0x1A	CH6 DIMM temp	R	0..1	Highest temperature among DIMM0 and DIMM1 on CH6 Same format as I2C register (SoC Temperature)
0x1B	CH7 DIMM Temp	R	0..1	Highest temperature among DIMM0 and DIMM1 on CH7 Same format as I2C register (SoC Temperature)
0x1C – 0x1F	–	–	–	Reserved
0x20	PMD VRD power	R	0..1	10-bit power consumption in watts ranging from 0 to 1023 Byte 0: (LSB) 0..7: Power consumption Byte 1: (MSB) 0..1: Power consumption 2..7: Reserved
0x21	SoC VRD power	R	0..1	Same format as I2C register (PMD VRD power)
0x22	DIMM VRD1 power	R	0..1	Same format as I2C register (PMD VRD power)
0x23	DIMM VRD2 power	R	0..1	Same format as I2C register (PMD VRD power) Power as reported by the second DIMM VRD (if present)
0x24 – 0x25	–	–	–	Reserved
0x26	PMD VRD power mW	R	0..1	Same format as I2C register (PMD VRD power). This is the mW portion (remainder) of PMD VRD power. The total PMD VRD power is calculated as sum of registers 0x20 and 0x26.

REGISTER ADDRESS	REGISTER NAME	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x27	SoC VRD power mW	R	0..1	Same format as I2C register SoC VRD power. This is the mW portion (remainder) of SoC VRD power. The total SoC VRD power is calculated as the sum of registers 0x21 and 0x27.
0x28	DIMM VRD1 power mW	R	0..1	Same format as I2C register DIMM VRD1 power. This is the mW portion (remainder) of DIMM VRD1 power. The total DIMM VRD1 power is calculated as the sum of registers 0x22 and 0x28.
0x29	DIMM VRD2 power mW	R	0..1	Same format as I2C register DIMM VRD2 power. This is the mW portion (remainder) of DIMM VRD2 power. The total DIMM VRD2 power is calculated as the sum of 0x23 and 0x29.
0x2A – 0x31	–	–	–	Reserved
0x32	MEM HOT threshold	R/W	0..1	Same format as above MEM HOT Threshold is the value at which DIMM will trigger its MEMHOT event when its temperature exceeds the threshold. This event is triggered via the PM_ALERT for Sensor Event including DIMM Event.
0x33	SoC VR HOT threshold	R/W	0..1	Same format as above
0x34	PMD VRD voltage	R	0..1	PMD voltage 15-bit voltage in mV
0x35	SoC VRD voltage	R	0..1	SoC voltage 15-bit voltage in mV
0x36	DIMM VRD1 voltage	R	0..1	DIMM VRD1 voltage 15-bit voltage in mV
0x37	DIMM VRD2 voltage	R	0..1	DIMM VRD2 voltage 15-bit voltage in mV
0x38 – 0x4E	–	–	–	Reserved
0x4F	–	R	0	0: CPU presence 1..15: Reserved
	–	–	1	Reserved

10.9.3.4. General Purpose Interrupt (GPI) Registers

GPI Mask Registers

These registers are used to control (enable or disable) different alert sources. Each bit indicates whether a particular status is enabled or disabled.

These registers are initialized to default values at boot time and can be updated by BMC. The BMC can set a particular bit in this register to '1' to enable or to '0' to disable the reporting of such alert. If an alert source is not supported, the corresponding bit will be shown as disabled, and any attempt to enable it will have no effect.

- 0: Disabled the alert of the corresponding source
- 1: Enabled the alert of corresponding source

Table 45 describes the GPI Mask registers in detail.

Table 45: GPI Mask Registers

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x50	GPI Control #0	0x00	R/W	0	0: SoC therm strip (OVERTEMP) 1: SoC HOT (HIGHTEMP) 2: SYS PWROK 3: Platform booting 4: Critical stop 5..7: Reserved
		–	–	1	Reserved
0x51	GPI Control #1	0x0F	R/W	0	0: SoC VR HOT 1: PMD VR HOT 2: DIMM VRD HOT 3..7: Reserved
		–	–	1	Reserved
0x52	GPI Control #2	0xFF	R/W	0	0: DIMM HOT 1..7: Reserved
		–	–	1	Reserved
0x53	GPI Control #3	0x7F	R/W	0	0: PMD/CPU errors 1: Memory errors 2: L3C errors 3: PCIe errors 4: SATA errors 5: Other SoC errors 6: ACPI state change 7: Boot errors
		–	–	1	0: RAS internal error 1-7: Reserved
0x54 – 0x5F	–	–	–	–	Reserved

GPI Source Registers

Each bit in the following registers denotes the presence or absence of a specific alert source.

A value of '1' indicates that an ALERT is present. An unsupported alert will be shown as '0'.

If any alert source is present, SMBALERT signal will be triggered to BMC to notify the alert.

When all present alert sources are cleared by BMC, eMAG will de-active the SMBALERT signal and continue updating the alert sources.

On receiving an SMBALERT signal from eMAG, the BMC needs to first read the GPI Data Set register to determine which GPI Data Set (Data Set #0/Data Set #1/ Data Set #2/ Data Set #3) register it must read next to determine the source of the alert(s).

In the case of GPI Data Set #0, each bit already indicates the associated status of the alert source.

In the case of GPI Data Set #1/#2/#3, the BMC needs to read the corresponding "GPI Status registers" to find out more details about the alerts.

After error sources are read, SMpro writes 0 to that register and clears the corresponding bit in the GPI Data Set.

Table 46: GPI Source Registers

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x60	GPI Data Set	0x0	R	0	Each bit in this register denotes the presence of one or more alerts in the Global Alert data sets below 0: Data set #0 1: Data set #1 2: Data set #2 3: Data set #3
				1	Reserved
0x61	GPI Data Set #0	0x0	R	0	0: SoC therm strip (OVERTEMP) 1: SoC HOT (HIGHTEMP) 2: SYS PWROK 3: Platform booting 4: Critical stop 5..7: Reserved
				1	Reserved
0x62	GPI Data Set #1	0x0	R	0	0: SoC VR HOT 1: PMD VR HOT 2: DIMM VR HOT 3..7: Reserved Note: User needs to read the "VRD Hot Error" to identity which VRD controller is HOT
				1	Reserved

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x63	GPI Data Set #2	0x0	R	0	0: DIMM HOT 1..: Reserved **Note**: User needs to read the "DIMM Hot Error" to identity which DIMM channel is HOT
				1	Reserved
0x64	GPI Data Set #3	0x0	R	0	0: PMD/CPU errors 1: Memory errors 2: L3C errors 3: PCIe errors 4: SATA errors 5: Other errors 6: ACPI state change 7: Boot errors
				1	0: RAS internal error 1-7: Reserved
0x65 – 0x6F	–	–	–	0..1	Reserved

Table 47 provides additional details about the behavior of these interrupts and lists the alerts that can be cleared by BMC.

Table 47: Alert Behaviors

GPI STATUS	MEANING	GPI BEHAVIOR
SoC thermal strip	OVERTEMP condition	Triggered by CPU when the OVERTEMP threshold is reached. eMAG will shut down. This is equivalent to the OVERTEMP signal. No SMB_ALERT is sent.
SoC HOT	HIGHTEMP condition	Triggered by CPU when the HIGHTEMP threshold is reached. This bit is persistent until HIGHTEMP condition is cleared. No SMB_ALERT is sent.
SYS PWROK	All power is OK	Triggered by CPU when all PMD, L3C power is up. eMAG is ready to communicate with BMC. This is equivalent to the CPU_POWER_OK signal. SMB_ALERT is sent only in the absence of CPU_POWER_OK signal in hardware.
Platform booting	eMAG is booting	Triggered by CPU when it starts bootloader.
Critical stop	CPU halts	Triggered by CPU when OS crashes or certain events cause the CPU to hang. **Note**: This function is currently not supported.
SoC VR Hot	VR for SoC is in HIGH TEMP	Triggered by CPU when VR for SoC is in HIGH TEMP.
PMD VR Hot	VR for PMD is in HIGH TEMP	Triggered by CPU when VR for PMD is in HIGH TEMP.

GPI STATUS	MEANING	GPI BEHAVIOR
DIMM VRD Hot	VRD for DIMM is in HIGH TEMP	Triggered by CPU when VRD1 for DIMM is in HIGH TEMP.
DIMM Hot	DIMM[y] at channel [x] is in HIGH TEMP	Triggered by CPU when any DIMM at any channel is in HIGH TEMP.
PMD/CPU errors	PMD/CPU has some errors	Triggered by CPU when PMD/CPU has any error.
Memory errors	Memory has some errors	Triggered by CPU when memory has any error.
L3C errors	L3C has some errors	Triggered by CPU when L3C has any error.
PCIe errors	PCIe has some errors	Triggered by CPU when any PCIe controller has any error.
SATA errors	SATA has some errors	Triggered by CPU when any SATA controller has any error.
Other errors	Run-time watchdog expired	Triggered by CPU when run-time watchdog expired
ACPI state change	ACPI state change	Triggered by CPU when it has any change of ACPI S-State. BMC must read register System State to determine the target state that the system has entered.
Boot errors	System cannot boot up properly	Triggered by CPU when system cannot boot up properly. BMC must read registers to determine the number of times boot has failed as well as the boot status.

GPI Status Registers

The GPI Source registers provide the alert source, while GPI Status register provides the exact description of the alert occurred on that source. The details of each are listed below.

When the BMC receives an alert notification, it is the responsibility of the BMC to read the corresponding "GPI Status registers", described in *Table 48*, to find out more details about the alert. Depending on the alert, it needs to handle the alert appropriately and clear the alert.

Table 48: GPI Status Registers

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x70	PMD error Set #0	0x0	R	0	Bit mask to identify which PMD has errors 0: PMD #0 has errors … 3: PMD #3 has errors 4: PMD #4 has errors 5: PMD #5 has errors 6: PMD #6 has errors 7: PMD #7 has errors
				1	0: PMD #8 has errors … 7: PMD #15 has errors

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x71	PMD error Set #1	0x0	R	0	Reserved for extension
				1	Reserved for extension
0x72	MCU error	0x0	R	0	Bit mask used to identify which MCU has errors. 0: MCU #0 DIMM #0 has errors[8] 1: MCU #0 DIMM #1 has errors 2: MCU #1 DIMM #0 has errors 3: MCU #1 DIMM #1 has errors 4: MCU #2 DIMM #0 has errors 5: MCU #2 DIMM #1 has errors 6: MCU #3 DIMM #0 has errors 7: MCU #3 DIMM #1 has errors
				1	0: MCU #4 DIMM #0 has errors[9] 1: MCU #4 DIMM #1 has errors 2: MCU #5 DIMM #0 has errors 3: MCU #5 DIMM #1 has errors 4: MCU #6 DIMM #0 has errors 5: MCU #6 DIMM #1 has errors 6: MCU #7 DIMM #0 has errors 7: MCU #7 DIMM #1 has errors
0x73	PCIe error	0x0	R	0	Bit mask to identify which PCIe controllers have errors 0: PCIE #0 has error 1: PCIE #1 has error 2: PCIE #2 has error 3: PCIE #3 has error 4: PCIE #4 has error 5: PCIE #5 has error 6: PCIE #6 has error 7: PCIE #7 has error
				1	Reserved

[8] DIMM #X indicates DIMM “channel” X belonging to the MCU and might not correspond to the physical DIMM slot on the board.

[9] eMAG supports 8 MCUs for a total of 16 DIMM channels/slots.

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x74	SATA error	0x0	R	0	Bit mask to identify which SATA controllers have errors 0..0: SATA #01 has error 1..1: SATA #23 has error 2..2: SATA #45 has error 3..7: Reserved
				1	Reserved
0x75	L3C error	0x0	R	0	Bit mask to identify which L3C instances have errors 0: L3C #0 has errors 1: L3C #1 has errors 2: L3C #2 has errors 3: L3C #3 has errors 4: L3C #4 has errors 5: L3C #5 has errors 6: L3C #6 has errors 7: L3C #7 has errors
				1	Reserved
0x76 – 0x78	–	–	–	–	Reserved
0x79	VRD Hot error	0x0	R/COR[10]	0	Identify which VRD controller has error 0: SOC VRD is HOT 1..3: Reserved 4: PMD VRD1 is HOT 5: PMD VRD2 is HOT 6: PMD VRD3 is HOT 7: Reserved
			R/COR	1	0: DIMM VRD1 is HOT 1: DIMM VRD2 is HOT 2: DIMM VRD3 is HOT 3: DIMM VRD4 is HOT 4..7: Reserved

[10] COR: Clear on Read

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x7A	DIMM Hot error	0x0	R/COR	0	Identify which DIMM channel has error 0: DIMM channel 0 is HOT 1: DIMM channel 1 is HOT 2: DIMM channel 2 is HOT 3: DIMM channel 3 is HOT 4: DIMM channel 4 is HOT 5: DIMM channel 5 is HOT 6: DIMM channel 6 is HOT 7: DIMM channel 7 is HOT
			R/COR	1	0..7: Reserved
0x7B	Boot #1 error	0x0	R/COR	0..1	Indicates how many times system failed to boot with normal configuration and defaulted to last known setting
0x7C	Boot #2 error	0x0	R/COR	0..1	Indicates how many times system failed to boot with last known configuration and reverted to factory defaults
0x7D	Watchdog status	0x0	R/COR	0..1	Indicates run-time watchdog expired 0: WDT expired 1..15: Reserved
0x7E	RAS internal error	0x0	R	0..1	0: Error from SMpro 1: Error from PMpro 2..15: Reserved
0x7F	–	–	–	–	Reserved

PMD/CPU and L3C Error Registers

Table 49 provides detailed information about PMD/CPU and L3C error registers.

Table 49: PMD/CPU Error Registers

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x80	PMD selection	0x0	R/W	0	Select which PMD to read the error information from based on the PMD error set in *Table 48*. Application will first need to write to this register 0x80 to select which PMD, and then read the next registers 0x81…0x84 for the PMD error information. Value: eMAG: 0..15 For example, to read the PMD errors for PMD#10, we first write 0xA to this register, then read the value from PMD error registers, the error for PMD#10 must be returned.
				1	Reserved
0x81	PMD L1 errors	0x0	R/COR	0	[0..7] CPU0 error bit fields 0: L1 ICF CErr 1: L1 ICF MultCErr 2: L1 LSU CErr 3: L1 LSU MultCErr 4: MMU CErr 5: MMU MultCerr 6..7: Reserved
				1	[0..7] CPU1 error bits: Same as above
0x82	PMD L2 errors #1	0x0	R/COR	0	[0..7] CPU0 L2 error bit fields: 0: CErr 1: UcErr 2: L2 RTOS (request timeout)
				1	[0..7] CPU1 L2 error bit fields: 0: CErr 1: UcErr 2: L2 RTOS (request timeout)
0x83 – 0x85	–	–	–	–	Reserved

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x86	L3C instance selection	0x0	R/W	0	Select which L3C instance to read the error information from based on the L3C error set in *Table 48*. Application will first need to write to this register 0x86 to select which L3C instance, and then read the next registers 0x8 for the L3C error information. Value: eMAG: 0..7 For example, to read the L3C errors for L3C #2, we first write 0x2 to this register, then read the value from L3C Error register below. The error for L3C #2 must be returned.
0x87	L3C errors	–	R/COR	–	L3C error bit fields: 0: CErr 1: UcErr 2..7: Reserved
–	–	–	–	–	0..7: Reserved
0x88 – x8F	–	–	–	–	Reserved

Memory Error Registers

Table 50 provides detailed information about Memory Error registers.

Table 50: Memory Error Registers

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x90	MCU DIMM selection	0x0	R/W	0..1	Select which MCU DIMM to read the error information from based on the MCU status in *Table 48*. Application will first need to write to this register 0x90 to select which MCU DIMM, and then read the next registers 0x91…0x93 for the PMD error information. Value: eMAG: 0..15 For example, to read the MCU errors for MCU#2, we first write 0x2 to this register, then read the values from MCU error registers at 0x91, 0x92 and 0x93.
0x91	MCU #X DIMM #Y errors	0x0	R/COR	0	[Byte 0] Error info: 0: CErr error 1: UcErr error 2..7: Reserved
				1	Reserved

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0x94 – 0x9F	–	–	–	–	Reserved

RAS Internal Error Registers

Table 51 provides detailed information about RAS internal error registers.

Table 51: RAS Internal Error Registers

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0xA0	SMpro RAS internal error type	0x0	R	0..1	0: Warning 1: Error 2: Error with data 3..15: Reserved
0xA1	PMpro RAS internal error type	0x0	R	0..1	0: Warning 1: Error 2: Error with data 3..15: Reserved
0xA2	SMpro RAS internal warning or error info	0x0	R/COR	0..1	The registers 0xA2 and 0xA3 store 32-bit value of warning or error info. 0xA2 stores the lower 16-bit value 0xA3 stores the higher 16-bit value
0xA3		0x0	R/COR	0..1	
0xA4	SMpro Extensive data of RAS internal error	0x0	R/COR	0..1	The register 0xA4 and 0xA5 store 32-bit value of extensive data. 0xA4 stores the lower 16-bit value 0xA5 stores the higher 16-bit value
0xA5		0x0	R/COR	0..1	
0xA6	PMpro RAS internal warning or error info	0x0	R/COR	0..1	The register 0xA2 and 0xA3 store 32-bit value of warning or error info. 0xA2 stores the lower 16-bit value 0xA3 stores the higher 16-bit value
0xA7		0x0	R/COR	0..1	
0xA8	PMpro extensive data of RAS internal error	0x0	R/COR	0..1	The register 0xA4 and 0xA5 store 32-bit value of extensive data. 0xA4 stores the lower 16-bit value 0xA5 stores the higher 16-bit value

PCIe Error Registers

Table 52 provides detailed information about PCIe error registers.

Table 52: PCIe Error Registers

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0xC0	PCIE0 error	0x0	R/W/COR	0..1	Bit mask indicating error categories: 0: Correctable 1: Uncorrectable Non-Fatal 2: Uncorrectable Fatal 3-7: Reserved Linux can write to this register. BMC read to clear this register.
0xC1		0x0	R/W/COR	0	Linux can write to this register. BMC read to clear this register. 0..2: PCIE Function # 3..7: PCIE Device #
				1	PCIE Bus #
0xC2	PCIE1 error	0x0	R/W/COR	0..1	Same as PCIE0 error
0xC3		0x0	R/W/COR	0..1	
0xC4	PCIE2 error	0x0	R/W/COR	0..1	Same as PCIE0 error
0xC5		0x0	R/W/COR	0..1	
0xC6	PCIE3 error	0x0	R/W/COR	0..1	Same as PCIE0 error
0xC7		0x0	R/W/COR	0..1	
0xC8	PCIE4 error	0x0	R/W/COR	0..1	Same as PCIE0 error
0xC9		0x0	R/W/COR	0..1	
0xCA	PCIE5 error	0x0	R/W/COR	0..1	Same as PCIE0 error
0xCB		0x0	R/W/COR	0..1	
0xCC	PCIE6 error	0x0	R/W/COR	0..1	Same as PCIE0 error
0xCD		0x0	R/W/COR	0..1	
0xCE	PCIE7 error	0x0	R/W/COR	0..1	Same as PCIE0 error
0xCF		0x0	R/W/COR	0..1	

SATA Error Registers

Table 53 provides detailed information about SATA Error registers.

Table 53: SATA Error Registers

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0xD0	SATA #01 errors	0x0	R/W	0	[Byte 0] SATA PORT 0 error info 0x00: Not connected 0x01: Connected, Normal 0x02: Connected. Error.
				1	[Byte 1] SATA PORT 1 error info 0x00: Not connected 0x01: Connected, Normal 0x02: Connected. Error.
0xD1	SATA #23 errors	0x0	R/W	0..1	Same as SATA #01 error
0xD2	SATA #45 errors	0x0	R/W	0..1	Same as SATA #01 error
0xD3 – 0xDF	–	–	–	–	Reserved

ACPI State Registers

Table 54 summarizes details for the ACPI states for system and PMDs on the eMAG processor. Additionally, the ACPI State of the system or individual PMDs can be changed through these writable registers.

Table 54: ACPI State Registers

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0xE0	System state	–	R/W	0	0..7: System power state On read, return the current System power state. On write, set the System power state to desired state The System power state encoding is show below: 0x00: S0, write 0x00 to wake up system from suspend 0x01: S1, equals to Standby state in Linux 0x02: S2, equals to Standby state in Linux 0x03: S3, equals to Suspend to Mem state in Linux 0x04: S4, hibernate (Suspend to Disk) => **NOT supported** 0x05: S5, power off state **Note**: In power-off state, the register map is no longer accessible. This state is documented here for completeness and applicable for external applications monitoring the system state.
				1	0: Indicates ACPI state has changed 1..7: Reserved
0xE1	P-State PMD selection	0x00	R/W	0	The application needs to write to this register to select which PMD to get/set its P-State using the PMD P-State register The P-State PMD selection and PMD Selection registers are only valid when the bit “ACPI P-State support” in the “Other Capabilities register is set to 1. When “ACPI P-State support” is set to 0, read/write to these registers are ignored.
				1	Reserved

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0xE2	P-State PMD Data register	–	R/W	0	0..3: Power State: On read, return the current PMD Performance state, On write, set the PMD Performance state to desired state. Note: The P-State setting will only take effect, when the CPU governor is set to “userspace”. From Linux shell: # cd /sys/devices/system/cpu/cpuX/cpufreq # cat scaling_governor # cat scaling_available_governors # echo “userspace” > scaling_governor P-States are encoded as below: 0x00: P0 0x01: P1 0x02: P2 0x03: P3 0x04: P4 0x05: P5 0x06: P6 0x07: P7 0x08: P8 Other: Reserved The CPU frequency that corresponds to the P-State is defined in the ACPI Table. eMAG: Px State is not supported. CPPC is used instead.
				1	Reserved
0xE3	CPPC PMD selection	0x00	R/W	0	The CPPC PMD Selection and PMD CPPC registers are only valid when the bit “ACPI CPPC support” in the “Other Capabilities register is set to 1. When “ACPI CPPC support” is set to 0, read/write to these registers will be ignored. Value: eMAG: 0..15
				1	Reserved

REGISTER ADDRESS	REGISTER NAME	INITIAL VALUE	ACCESS TYPE	BYTE	REGISTER DESCRIPTION
0xE4	CPPC PMD Data register	–	R/W	0	The CPPC PMD selection and PMD CPPC registers are only valid when the bit "ACPI CPPC support" in the "Other Capabilities register is set to 1. When "ACPI CPPC support" is set to 0, read/write to these registers will be ignored. Read from this register return the current frequency in MHz of the PMD indexed by CPPC PMD Index register Write to this register set the frequency of the PMD indexed by CPPC PMD Index register to specify MHz The valid frequency must be in the recommended range supported by the SoC eMAG: Min Frequency = 1000 MHz Max Frequency = 2800 MHz 0..7: CPU frequency lower byte
				1	0..7: CPU frequency upper byte
0xE5 – 0xFF	–	–	–	–	Reserved

10.9.4. Accessing the Register Map from Linux

The user can use the `i2ctools` utility to access the Register Map from Linux.

The format of the command is as follows:

```
i2cget -y <device #> <register map pseudo address> <0xYY> <offset> w
```

where:

- Device: Is the logical I2C device number of the "eMAG SMpro I2C Mailbox." This can vary from board to board depending on how Linux enumerates all I2C devices on the system.
- Register Map Pseudo Address: A pseudo address used by the Register Map to mimic an I2C device. This also might vary from board to board depending on whether there could be any conflict with some real physical I2C addresses.
- 0xYY: The register offset in eMAG register map.

For example,

```
$ i2cdetect -l
i2c-0     i2c     Synopsys DesignWare I2C adapter     I2C adapter
i2c-1     smbus   MAILBOX I2C                         SMBus adapter
i2c-2     i2c     i2c-0-mux (chan_id 0)               I2C adapter
i2c-3     i2c     i2c-0-mux (chan_id 1)               I2C adapter
i2c-4     i2c     i2c-0-mux (chan_id 2)               I2C adapter
i2c-5     i2c     i2c-0-mux (chan_id 3)               I2C adapter
```

From the above example, the device address is “1”, and in case of a Hawk board, the Register Map Pseudo Address is 0x2F. Hence, a command to read the SoC VRD temperature (register map offset 0x11) would be:

```
# i2cget -y 1 0x2f 0x11 w
0x0028
```

or 40°C.

All register maps can be read from Linux. However, only few registers can be written to from Linux. Refer the “Access Type” field in the tables in the preceding subsections for additional information.

11. Pinouts for Selected Connectors and LED Indicators

The tables in this section lists the pinouts for selected connectors, jumpers, and LED indicators on the Hawk board.

Table 55: CON47: USB 2.0 Header

CON47			
PIN	SIGNAL	PIN	SIGNAL
1	USBHUB_VBUS4	6	USBHUB_DP3_R
2	USBHUB_VBUS3	7	GND
3	USBHUB_DM4_R	8	GND
4	USBHUB_DM3_R	9	–
5	USBHUB_DP4_R	10	Not Connected

Table 56: CON52: Front Panel Header

CON52					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+3V3_BMC	9	CHSS_HDD_LEDC	17	GND
2	See Schematics	10	CHSS_FAULT2_LEDC	18	CHSS_SMBUS_SCL
3	Not available	11	CHSS_PWR_SW	19	CHSS_SYSID_SW
4	See schematics	12	CHSS_NIC1_LEDA	20	CHSS_INTRUSION
5	CHSS_PWR_LEDC	13	GND	21	CHSS_TEMPSENSE
6	CHSS_SYSID_LEDC	14	CHSS_NIC1_LEDC	22	CHSS_NIC2_LEDA
7	+3V3_ATX	15	CHSS_RST_SW	23	Open
8	CHSS_FAULT1_LEDC	16	CHSS_SMBUS_SDA	24	CHSS_NIC2_LEDC

Table 57: CON68, CON70, CON69: Fan Connector

CON68		CON70		CON69	
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	1	GND	1	GND
2	+12V_ATX	2	+12V_ATX	2	+12V_ATX
3	FAN_FTACH0	3	FAN_FTACH4	3	FAN_FTACH2
4	FAN_PWM0	4	FAN_PWM4	4	FAN_PWM2
5	FAN_FTACH1	5	FAN_FTACH5	5	FAN_FTACH3
6	FAN_PWM1	6	FAN_PWM5	6	FAN_PWM3

Table 58: CON67: RMC Signal Header (openEDGE)

CON67			
PIN	SIGNAL	PIN	SIGNAL
1	SLED_ADDR_0	8	BMC_I2C8_SDA
2	+3V3_BMC	9	RMC_GPIO_2
3	SLED_ADDR_1	10	SLED_PRSNT_N
4	SLED_ADDR_2	11	SLED_CHASS_INTRUSION
5	RMC_GPIO_0	12	–
6	BMC_I2C8_SCL	13	IRQ_RMC_ALERT_N
7	RMC_GPIO_1	14	BMC_SLED_READY_N

Table 59: CON40: 8-Pin CPU Power Connector

CON40			
PIN	SIGNAL	PIN	SIGNAL
1	GND	5	+12V_ATX
2	GND	6	+12V_ATX
3	GND	7	+12V_ATX
4	GND	8	+12V_ATX

Table 60: CON39: 24-Pin Main Power Connector

CON39					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	+3V3_ATX	9	+5VSB_ATX	17	GND
2	+3V3_ATX	10	+12V_ATX	18	GND
3	GND	11	+12V_ATX	19	GND
4	+5V_ATX	12	+3V3_ATX	20	–
5	GND	13	+3V3_ATX	21	+5V_ATX
6	+5V_ATX	14	–	22	+5V_ATX
7	GND	15	GND	23	+5V_ATX
8	PGOOD_ATX	16	ATX_PWRON_L	24	GND

Table 61: CON37: VGA and Serial Port DB9 Connector

CON37					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	CON_VGA_RED	9	+5V_VGA	17	CON_RXD5
2	CON_VGA_GRN	10	GND	18	CON_TXD5
3	CON_VGA_BLUE	11	–	19	–
4	–	12	CON_DAC_SDA	20	GND
5	GND	13	CON_VGA_HSYNC	21	–
6	GND	14	CON_VGA_VSYNC	22	–
7	GND	15	CON_DAC_SCL	23	–
8	GND	16	–	24	–

Table 62: CON50: BMC ATX PMBus Connector

CON50	
PIN	SIGNAL
1	BMC_I2C7_SCL
2	BMC_I2C7_SDA
3	SM_Bus _7 Alert
4	GND
5	Not Connected

Table 63: CON17 – Pins A1 to A82: Standard PCIe x16 Connector

CON17					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
A1	GND	A29	PCIE2_RX_3_P	A57	PCIE3_RX_1_N
A2	+12V_ATX	A30	PCIE2_RX_3_N	A58	GND
A3	+12V_ATX	A31	GND	A59	GND
A4	GND	A32	PCIE3_REFCLK_CON_P	A60	PCIE3_RX_2_P
A5	–	A33	PCIE3_REFCLK_CON_N	A61	PCIE3_RX_2_N
A6	–	A34	GND	A62	GND
A7	–	A35	PCIE2_RX_4_P	A63	GND
A8	–	A36	PCIE2_RX_4_N	A64	PCIE3_RX_3_P
A9	+3V3_ATX	A37	GND	A65	PCIE3_RX_3_N
A10	+3V3_ATX	A38	GND	A66	GND
A11	PCIE2_PERST_L	A39	PCIE2_RX_5_P	A67	GND
A12	GND	A40	PCIE2_RX_5_N	A68	PCIE3_RX_4_P
A13	PCIE23_REFCLK_CON_P	A41	GND	A69	PCIE3_RX_4_N
A14	PCIE23_REFCLK_CON_N	A42	GND	A70	GND
A15	GND	A43	PCIE2_RX_6_P	A71	GND
A16	PCIE2_RX_0_P	A44	PCIE2_RX_6_N	A72	PCIE3_RX_5_P
A17	PCIE2_RX_0_N	A45	GND	A73	PCIE3_RX_5_N
A18	GND	A46	GND	A74	GND
A19	–	A47	PCIE2_RX_7_P	A75	GND
A20	GND	A48	PCIE2_RX_7_N	A76	PCIE3_RX_6_P
A21	PCIE2_RX_1_P	A49	GND	A77	PCIE3_RX_6_N
A22	PCIE2_RX_1_N	A50	PCIE3_PERST_L	A78	GND
A23	GND	A51	GND	A79	GND
A24	GND	A52	PCIE3_RX_0_P	A80	PCIE3_RX_7_P
A25	PCIE2_RX_2_P	A53	PCIE3_RX_0_N	A81	PCIE3_RX_7_N
A26	PCIE2_RX_2_N	A54	GND	A82	GND
A27	GND	A55	GND	–	–
A28	GND	A56	PCIE3_RX_1_P	–	–

Table 64: CON17 – Pins B1 to B82: Standard PCIe x16 Connector

CON17					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
B1	+12V_ATX	B29	GND	B57	GND
B2	+12V_ATX	B30	–	B58	PCIE3_TX_2_P
B3	+12V_ATX	B31	PRSNT2_2_L	B59	PCIE3_TX_2_N
B4	GND	B32	GND	B60	GND
B5	I2C_PCIE23_SCL	B33	PCIE2_TX_4_P	B61	GND
B6	I2C_PCIE23_SDA	B34	PCIE2_TX_4_N	B62	PCIE3_TX_3_P
B7	GND	B35	GND	B63	PCIE3_TX_3_N
B8	+3V3_ATX	B36	GND	B64	GND
B9	–	B37	PCIE2_TX_5_P	B65	GND
B10	+3V3_BMC	B38	PCIE2_TX_5_N	B66	PCIE3_TX_4_P
B11	PCIE23_WAKE_L	B39	GND	B67	PCIE3_TX_4_N
B12	–	B40	GND	B68	GND
B13	GND	B41	PCIE2_TX_6_P	B69	GND
B14	PCIE2_TX_0_P	B42	PCIE2_TX_6_N	B70	PCIE3_TX_5_P
B15	PCIE2_TX_0_N	B43	GND	B71	PCIE3_TX_5_N
B16	GND	B44	GND	B72	GND
B17	RISER_SLT1_PRSNT_L	B45	PCIE2_TX_7_P	B73	GND
B18	GND	B46	PCIE2_TX_7_N	B74	PCIE3_TX_6_P
B19	PCIE2_TX_1_P	B47	GND	B75	PCIE3_TX_6_N
B20	PCIE2_TX_1_N	B48	RISER_SLT0_PRSNT_L	B76	GND
B21	GND	B49	GND	B77	GND
B22	GND	B50	PCIE3_TX_0_P	B78	PCIE3_TX_7_P
B23	PCIE2_TX_2_P	B51	PCIE3_TX_0_N	B79	PCIE3_TX_7_N
B24	PCIE2_TX_2_N	B52	GND	B80	GND
B25	GND	B53	GND	B81	RISER_PRSNT_L
B26	GND	B54	PCIE3_TX_1_P	B82	–
B27	PCIE2_TX_3_P	B55	PCIE3_TX_1_N	–	–
B28	PCIE2_TX_3_N	B56	GND	–	–

Table 65: CON60: Chassis Intrusion Sensor Connector

CON60	
PIN	SIGNAL
1	CHSS_INTRUSION
2	GND

Table 66: CON63: RMC MDI (openEDGE) Connector

CON63	
PIN	SIGNAL
R1	GE_RMC_MD0_P
R2	GE_RMC_MD0_N
R3	GE_RMC_MD1_P
R4	GE_RMC_MD1_N
R5	See Schematics
R6	See Schematics
R7	GE_RMC_MD2_P
R8	GE_RMC_MD2_N
R9	GE_RMC_MD3_P
R10	GE_RMC_MD3_N

Table 67: CON19: NVMe M.2 Connector

CON19					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	26	Not Connected	51	GND
2	+3V3_ATX	27	GND	52	CLK_M2_0_EN_N
3	GND	28	Not Connected	53	PCIE4_REFCLK_CON_N
4	+3V3_ATX	29	PCIE4_RX_1_N	54	Not Connected
5	PCIE4_RX_3_N	30	Not Connected	55	PCIE4_REFCLK_CON_P
6	Not Connected	31	PCIE4_RX_1_P	56	Not Connected
7	PCIE4_RX_3_P	32	Not Connected	57	GND
8	Not Connected	33	GND	58	Not Connected
9	GND	34	Not Connected	59	Not Defined
10	LED_M2_0_ACT_N	35	PCIE4_TX_1_N	60	Not Defined
11	PCIE4_TX_3_N	36	Not Connected	61	Not Defined

CON19					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
12	+3V3_ATX	37	PCIE4_TX_1_P	62	Not Defined
13	PCIE4_TX_3_P	38	Not Connected	63	Not Defined
14	+3V3_ATX	39	GND	64	Not Defined
15	GND	40	I2C_M2_0_SCL	65	Not Defined
16	+3V3_ATX	41	PCIE4_RX_0_N	66	Not Defined
17	PCIE4_RX_2_N	42	I2C_M2_0_SDA	67	Not Connected
18	+3V3_ATX	43	PCIE4_RX_0_P	68	Not Connected
19	PCIE4_RX_2_P	44	I2C_M2_0_ALT_L	69	Not Connected
20	Not Connected	45	GND	70	+3V3_ATX
21	GND	46	Not Connected	71	GND
22	Not Connected	47	PCIE4_TX_0_N	72	+3V3_ATX
23	PCIE4_TX_2_N	48	Not Connected	73	GND
24	Not Connected	49	PCIE4_TX_0_P	74	+3V3_ATX
25	PCIE4_TX_2_P	50	RST_M2_0_PERST_N	75	GND

Table 68: CON62: NVMe M.2 Connector

CON62					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	26	Not Connected	51	GND
2	+3V3_ATX	27	GND	52	CLK_M2_1_EN_N
3	GND	28	Not Connected	53	PCIE5_REFCLK_CON_N
4	+3V3_ATX	29	PCIE5_RX_1_N	54	Not Connected
5	PCIE5_RX_3_N	30	Not Connected	55	PCIE5_REFCLK_CON_P
6	Not Connected	31	PCIE5_RX_1_P	56	Not Connected
7	PCIE5_RX_3_P	32	Not Connected	57	GND
8	Not Connected	33	GND	58	Not Connected
9	GND	34	Not Connected	59	Not Defined
10	LED_M2_1_ACT_N	35	PCIE5_TX_1_N	60	Not Defined
11	PCIE5_TX_3_N	36	Not Connected	61	Not Defined
12	+3V3_ATX	37	PCIE5_TX_1_P	62	Not Defined
13	PCIE5_TX_3_P	38	Not Connected	63	Not Defined
14	+3V3_ATX	39	GND	64	Not Defined

CON62					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
15	GND	40	I2C_M2_1_SCL	65	Not Defined
16	+3V3_ATX	41	PCIE5_RX_0_N	66	Not Defined
17	PCIE5_RX_2_N	42	I2C_M2_1_SDA	67	Not Connected
18	+3V3_ATX	43	PCIE5_RX_0_P	68	Not Connected
19	PCIE5_RX_2_P	44	I2C_M2_1_ALT_L	69	Not Connected
20	Not Connected	45	GND	70	+3V3_ATX
21	GND	46	Not Connected	71	GND
22	Not Connected	47	PCIE5_TX_0_N	72	+3V3_ATX
23	PCIE5_TX_2_N	48	Not Connected	73	GND
24	Not Connected	49	PCIE5_TX_0_P	74	+3V3_ATX
25	PCIE5_TX_2_P	50	RST_M2_1_PERST_N	75	GND

Table 69: CON29: Serial Trace Probe Connector

CON29					
PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	NC	16	NC	31	NC
2	NC	17	GND	32	NC
3	NC	18	NC	33	NC
4	NC	19	NC	34	NC
5	NC	20	NC	35	NC
6	NC	21	NC	36	NC
7	NC	22	NC	37	NC
8	NC	23	GND	38	NC
9	NC	24	NC	39	NC
10	NC	25	STRC1_TX_P	40	NC
11	GND	26	NC	41	GND
12	NC	27	STRC1_TX_N	42	GND
13	STRC0_TX_P	28	NC	43	NC
14	NC	29	GND	44	NC
15	STRC0_TX_N	30	NC	–	–

Table 70: CON32: JTAG DAP (Debug Access Port) Interface

CON32			
PIN	SIGNAL	PIN	SIGNAL
1	+1V8_CPU_SOC	6	JTAG_DAP_TDO
2	JTAG_DAP_TMS	7	NC
3	GND	8	JTAG_DAP_TDI
4	JTAG_DAP_TCK	9	GND
5	GND	10	JTAG_DAP_TRST_L

Table 71: CON35: SoC JTAG Interface

CON35			
PIN	SIGNAL	PIN	SIGNAL
1	+1V8_CPU_SOC	6	JTAG_SOC_TDO
2	JTAG_SOC_TMS	7	–
3	GND	8	JTAG_SOC_TDI
4	JTAG_SOC_TCK	9	GND
5	GND	10	JTAG_SOC_TRST_L

Table 72: CON33: Serial Trace Probe Connector

CON33			
PIN	SIGNAL	PIN	SIGNAL
1	+1V8_CPU_SOC	6	JTAG_IPP_TDO
2	JTAG_IPP_TMS	7	–
3	GND	8	JTAG_IPP_TDI
4	JTAG_IPP_TCK	9	GND
5	GND	10	JTAG_IPP_TRST_L

Table 73: CON34: PMpro JTAG Interface

CON34			
PIN	SIGNAL	PIN	SIGNAL
1	+1V8_CPU_SOC	6	JTAG_PM_TDO
2	JTAG_PM_TMS	7	–
3	GND	8	JTAG_PM_TDI

CON34			
PIN	SIGNAL	PIN	SIGNAL
4	JTAG_PM_TCK	9	GND
5	GND	10	JTAG_PM_TRST_L

Table 74: D42: BMC Heartbeat LED

D42		
REFERENCE DESIGNATOR	DESCRIPTION	DEFINITION
D42	BMC Heartbeat LED	Blinking Green: BMC is functioning properly. OFF: BMC is not running or functioning properly.

Figure 36 shows the Hawk motherboard LEDs reference designator.

Figure 36: Hawk Motherboard LEDs Reference Designator

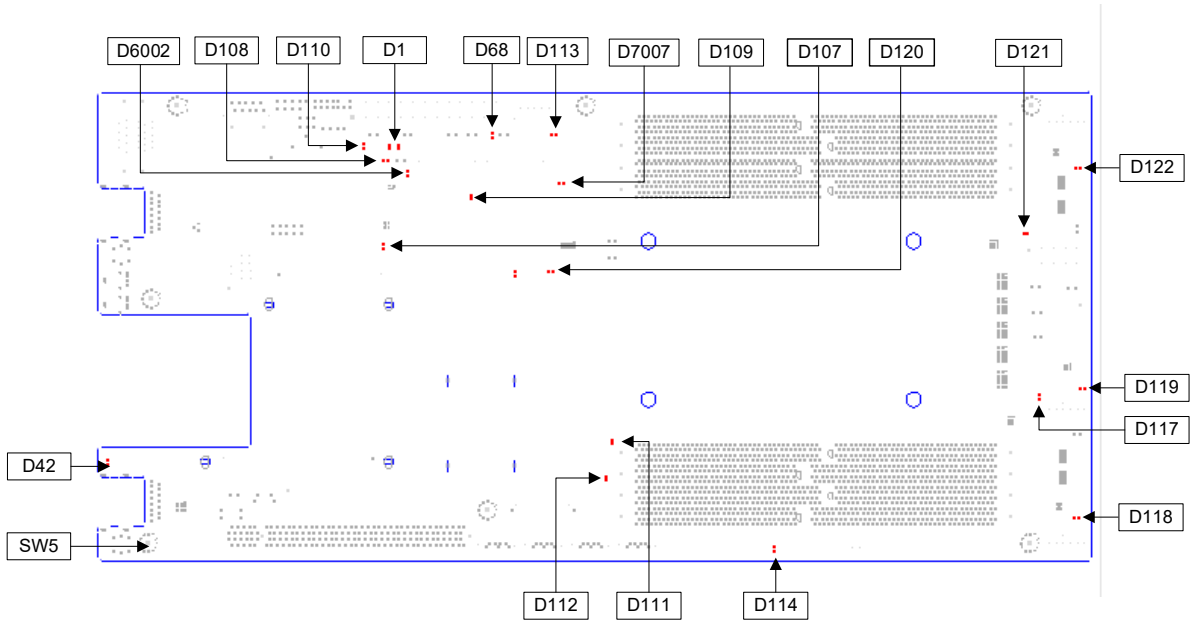


Table 75 lists the designators for the LEDs and switches on the Hawk board.

Table 75: Designators for LEDs and Switches on the Hawk Board

#	DESIGNATOR	DESCRIPTION
1	SW4	ID Switch / LED
2	SW5	Power Switch / LED
3	D1	• Red: Indicates CPU_RESTN is asserted • Green: Indicates ATX power supply passed self-test and its output has stabilized
4	D3	CPU high temperature LED (orange): • On: CPU temperature is high • Off: CPU temperature is normal
5	D24	Green: +3V3_CPU rail is available
6	D42	Green: BMC heartbeat
7	D68	Green: +3_3V_ATX rail (supplying to the M.2 connector CON19) is available
8	D107	Green: +2V5_BMC rail is available
9	D108	Green:+1V2_BMC_DDRVDDQ is available
10	D109	Green: +1V15_BMC rail is available
11	D110	Green: +3V3_BMC rail is available
12	D111	Green: +1V5_CPU rail is available
13	D112	Green: +1V8_CPU rail is available
14	D113	Green: +2V5 (for DDR channel 0, 1,2, 3) rail is available
15	D114	Green: +2V5 (for DDR channel 4, 5, 6, 7) rail is available
16	D117	Green: +1V2 (for DDR channel 4, 5, 6, 7) rail is available
17	D118	Green: +0V6 (for DDR channel 4, 5, 6, 7) rail is available
18	D119	Green: +0V9_CPU_PCP rail is available
19	D120	Green: +0V9_CPU_SOC rail is available
20	D121	Green: +1V2 (for DDR channel 0, 1, 2, 3) rail is available
21	D122	Green: +0V6 (for DDR channel 0, 1, 2, 3) rail is available
22	D6002	Green: +3V3_ATX rail (supplying to the M.2 connector CON62) is available
23	D7007	Green: +1V8_CPU_PCP rail is available

Table 76: Hawk Board Debug Ports

#	DESIGNATOR	DESCRIPTION
1	CON29	Serial Trace Probe Connector
2	J2	JTAG Select / Boundary Scan Option Select

#	DESIGNATOR	DESCRIPTION
3	CON32	JTAG DAP (Debug Access Port) Interface
4	CON35	SOC JTAG Interface
5	CON33	SMpro JTAG Interface
6	CON34	PMpro JTAG Interface
7	J11	Linux Console
8	J12	ATF
9	J13	SMpro

Table 77: SW4: ID Switch / LED

DESIGNATOR	DESCRIPTION	DEFINITION
SW4	System ID button with ID LED	1 : Steady blue light: the server is identified 0 : the server is not identified

Note: When correctly connected to the front panel, the switch can be used to activate ID Switch LED on front panel.

Table 78: SW5: Power Switch / LED

DESIGNATOR	DESCRIPTION	DEFINITION
SW5	Power button with power status LED	1. Steady green light: Server is ON 2. OFF: the server is OFF

Table 79: SW2: BMC Reset

DESIGNATOR	DESCRIPTION	DEFINITION
SW1	System Reset Button	BMC_RST# will be initiated when pressed
SW2	BMC Reset Button	BMC_RST# will be initiated when pressed

Table 80: PS ON Jumper

DESIGNATOR	DESCRIPTION	DEFINITION
J1	PS ON	ATX_PWRON_L will be active when jumper is closed

Table 81: J4: PCIe Spread Spectrum Jumper

DESIGNATOR	DESCRIPTION	DEFINITION
J4	PCIe Spread Spectrum ON/OFF	Enable –0.5% spread spectrum on PCIe clock when jumper is closed

Table 82: J2: JTAG Select / Boundary Scan Option Select

J2			
PIN	SIGNAL	PIN	SIGNAL
1	JTAG_SEL0	6	GND
2	GND	7	JTAG_SEL3
3	JTAG_SEL1	8	GND
4	GND	9	+1V8_CPU_SOC
5	JTAG_SEL2	10	JTAG_CMPL2

Table 83: J11: Linux Console

	PIN	SIGNAL NAME		PIN
J11	1	3V3_BMC	CONNECTED TO SERIAL PORT BREAKOUT ADAPTER	VCC
	2	UART_TXVR_TXD0		TX
	3	UART_TXVR_RTS0		NO CONNECT
	4	GND		GND
	5	UART_TXVR_CTS0		NO CONNECT
	6	UART_TXVR_RXD0		RX

Table 84: J12: ATF

	PIN	SIGNAL NAME		PIN
J12	1	3V3_BMC	CONNECTED TO SERIAL PORT BREAKOUT ADAPTER	VCC
	2	CON_RXD1		RX
	3	CON_TXD1		TX
	4	GND		GND

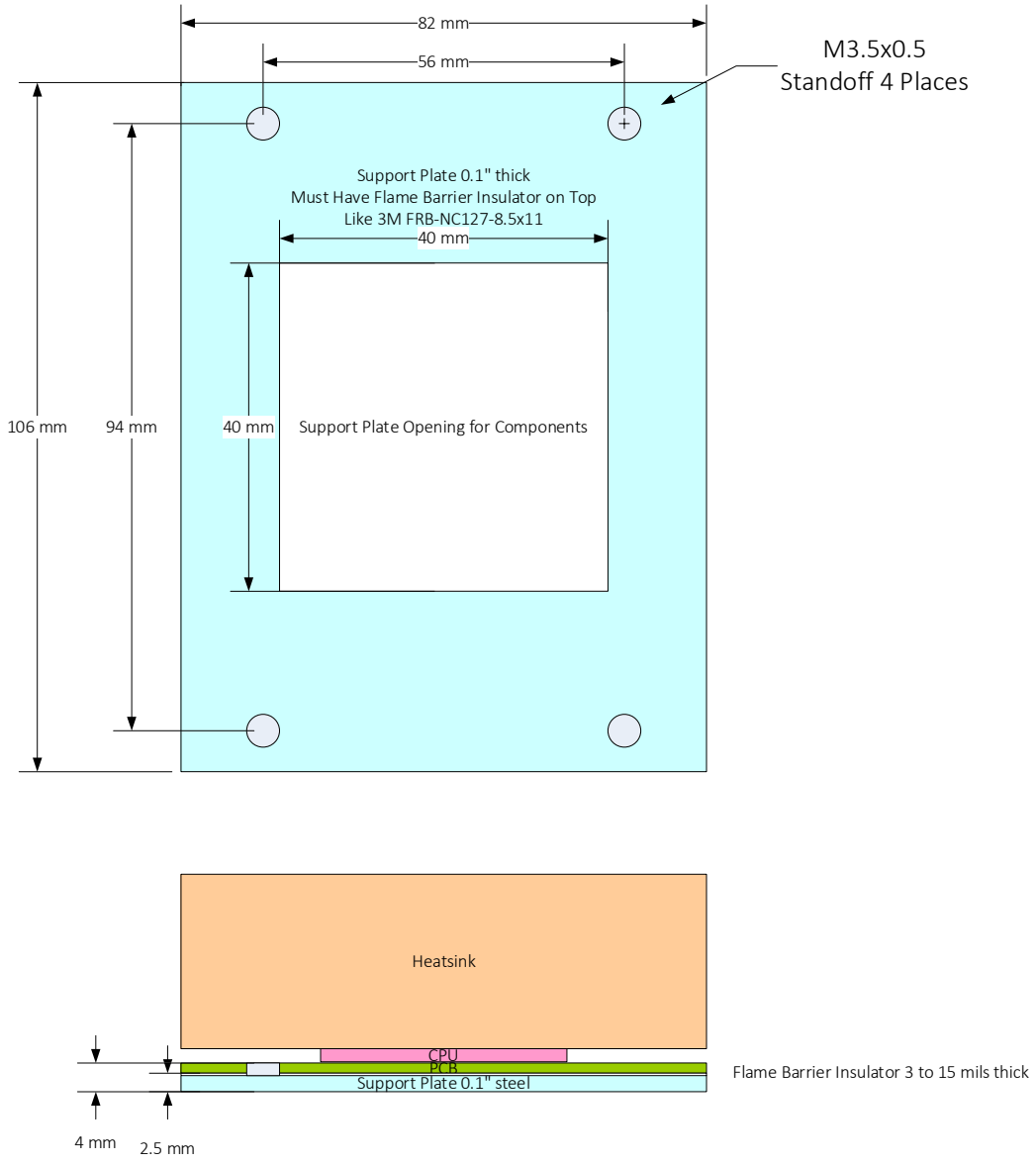
Table 85: J13: SMpro

	PIN	SIGNAL NAME		PIN
J13	1	3V3_BMC	CONNECTED TO SERIAL PORT BREAKOUT ADAPTER	VCC
	2	CON_RXD4		RX
	3	CON_TXD4		TX
	4	GND		GND

11.1. Heat Sink Footprint

The Hawk board provides mounting holes to support a 125 W TDP heat sink for the eMAG CPU as shown in *Figure 37*.

Figure 37: CPU Heat Sink Mounting Footprint for the Hawk Board



11.2. Standard LGA2011 Heat Sink Modifications

Heat sink for the Hawk board is a modified version of a standard LGA2011 socket heat sink similar to T318, or R31 from Dynatron, or MT0941 from Microloops.

The modification is required since a standard LGA2011 heat sink is mounted to the socket hardware. The Hawk board has a CPU soldered to the board and the heat sink must be mounted to the backplate.

Heat sink modifications require replacing standard heat sink mounting screws. Support backplate is required.

11.3. Approved Heat Sink Vendors and Part Numbers

Hawk supports the CPU heat sinks listed in *Table 86*.

Table 86: Approved Vendor and Part Number List for Hawk CPU Heat Sink

VENDOR	PART NUMBER	NOTES
Microloops	TSM-MT0941-HN	Heat Sink + Backplate
AIC/Dynatron	HSP-DY-BD-STV193	Heat Sink + Backplate

11.4. CPU Thermal Sensors

eMAG SMpro has access to three sets of thermal sensors:

- On-die thermal sensors inside the eMAG CPU that measure temperature at different die zones
- DIMM thermal sensors that are accessible through SPD I2C bus
- VRM thermal sensors for controller and every power phase (located within the PowerFETs)

This information is logged and can be reported to BMC.

The maximum allowable tolerance of thermal sensors on the motherboard is ±3°C

11.5. BMC Thermal Sensors

In addition to CPU thermal sensors, the Hawk board is equipped with multiple sensors accessible by BMC. BMC continuously polls thermal sensors and adjusts system fan speed, or can initiate a system thermal shutdown. The following sensors are available for BMC on BMC I2C bus 4:

- CPU thermal diode sense at address 0x19, Channel 1
- Inlet system temperature sensor (ambient temperature) at address 0x19, Channel 2
- Outlet system temperature sensor at address 0x4A
- CPU outlet system temperature sensor at address 0x48
- OCP inlet system temperature sensor at address 0x49

11.6. Inlet Temperature

The inlet air temperature will vary. The cooling system must cover inlet temperatures at 20°C, 25°C, 30°C, and 35°C. Cooling above 30°C is beyond operating specification but used during validation to demonstrate design margin. CPU throttling is not allowed to activate during the validation range of 20°C – 35°C.

11.7. Fan Redundancy

The server fans at N+1 redundancy must be sufficient for cooling server components to temperatures below their maximum spec to prevent server shutdown or to prevent either CPU or memory throttling.

11.8. System Airflow or Volumetric Flow

The unit of airflow (or volumetric flow) used for this spec is CFM (cubic feet per minute). The maximum allowable airflow per watt in the system must be 0.107. The desired airflow per watt is 0.1 or lower in the system at the mean temperature (plus or minus standard deviation).

11.9. Delta T

The delta T is the air temperature difference across the system or the temperature difference between outlet air temperature of system and inlet air temperature of system. The desired rack-level delta T must be greater than 13.9°C (25°F). The desired server-level delta T is 17°C (31°F) when the inlet air temperature to the system is equal to or lower than 30°C.

11.10. Thermal Margin

The thermal margin is the difference between the maximum theoretical safe temperature and the actual temperature. The board design operates at an inlet temperature of 35°C (95°F) outside of the system with a minimum 2% thermal margin for every component in the system. Otherwise, the thermal margin for every component in the system is at least 7% for temperatures up to 30°C.

11.10.1. Thermal Kit Requirements

Thermal testing must be performed at up to 35°C (95°F) inlet temperature to guarantee high temperature reliability.

11.11. System Fan

The system fan must be highly power-efficient with dual bearing. The propagation of vibration cause by fan rotation must be minimized and limited. ODM can propose larger frame size of fan if and only if there is alternative way to provide cost benefits. The maximum thickness of fan must not be greater than 38mm. Except for the condition when one fan (or one rotor) fails, the fan power consumption in system must not be exceeding 5% of total system power excluding the fan power. On Hawk mainboard, there are three 6-pin fan headers supporting 6-wire chassis couple fans.

System fan must not have back rush current in all condition. System fan must have an inrush current of less than 1 A on 12 V per fan. When there is a step change on fan PWM signal from low PWM to high PWM, there must be less than 10% of overshoot or no overshoot for fan input current. System must stay within its power envelope in all condition of fan operation.

11.12. Air Duct

The air duct needs to be part of the motherboard tray cover, and must be most energy efficient design. The air-duct design must be simple and easily serviceable. Using highly green material or reusable material for the air duct is preferred.

12. Installing the Hawk Board into a Chassis

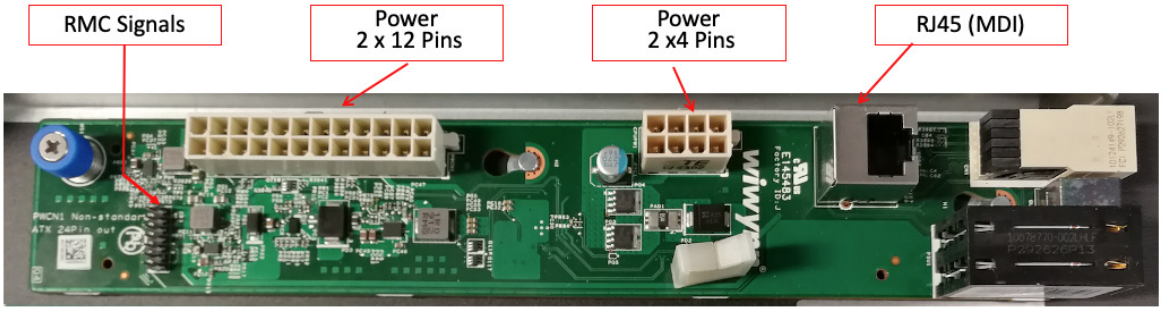
This section describes the steps involved in installing the Hawk board into a compatible chassis, such as openEDGE. It also covers aspects such as the tools required as well as the precautions to be taken during the installation process.

13. Interfacing the Hawk Board with a Sled Interposer

This section shows the connectivity between the Hawk motherboard and the Wiwynn interposer board.

See *Figure 38*. The interposer board provides the power delivery to the Hawk motherboard. It also provides connectivity between the Hawk motherboard and the chassis backplane for signaling between sleds and Rack Management Controller (RMC).

Figure 38: Interposer Board from Wiwynn



Hawk motherboard requires power to be delivered through both the 24-pin ATX power connector (CPU and I/O) and 8 pin 12 V connector (CPU). A 5 V source must also be present if SATA SSDs are used.

- Connect 2x12 power pins from the Interposer to Hawk CON39 (Main Power Connector)
- Connect 2x4 power pins from the Interposer to Hawk CON40 (8-pin CPU Power Connector)

Hawk exposes non-MDI, RMC signals through a header named CON17 (Vendor: Aquatech Corporation, Vendor Part Number: YNK12031-HPH-412070-B12).

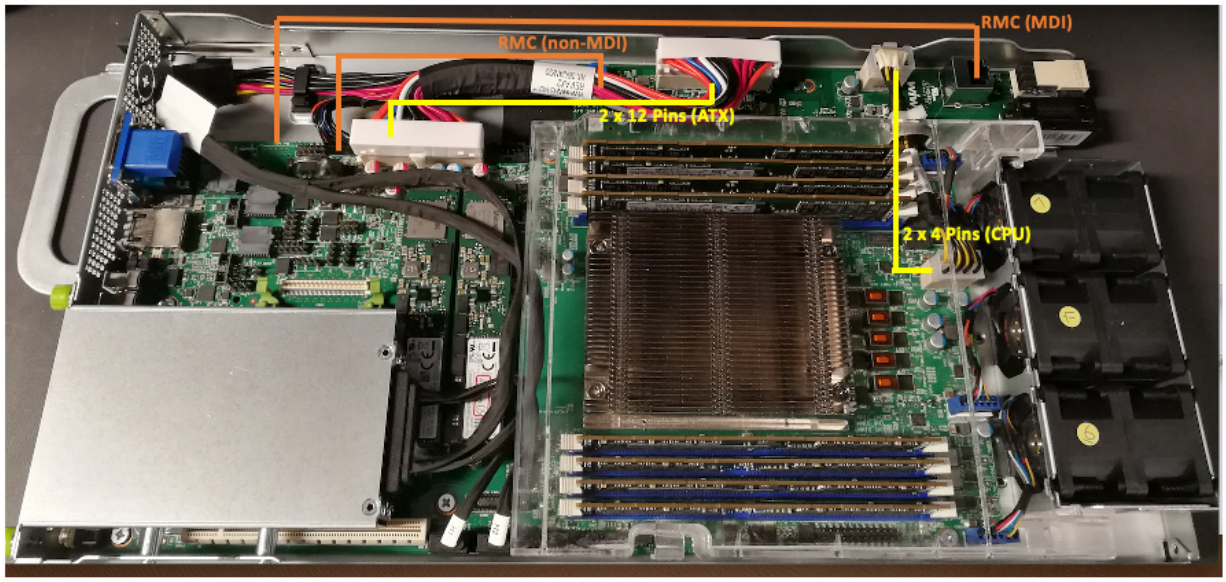
- Connect the cable between the RMC signal header on the Interposer to Hawk CON17

Hawk supports a dedicated network port (1 GbE RJ45) in the I/O area for system management. In the default shipping configuration, the RJ45 connector is not populated. A simple rework on the motherboard can be implemented to route system management signals (e.g. MDI signals) through RMC.

- Populate Hawk CON63 with a single port RJ45 modular jack
- Populate R7000, R7001, R7002, R7003, R7004, R7005, R7006, R7007 with 0 Ω resistors
- Connect a RJ45 Ethernet patch cable from the Interposer to Hawk CON63

Figure 39 shows a Hawk motherboard installed in the Wiwynn EP100 OpenEdge sled. It also shows the connectivity between the Hawk motherboard and the Wiwynn Interposer.

Figure 39: Hawk Motherboard Installed in the Wiwynn EP100 openEDGE Sled



13.1. Independent Loading Mechanisms (ILMs)

The Hawk board uses a standard LGA2011 heat sink, with the CPU soldered on the board, and the heat sink mounted to the backplate by 4 screws.

Figure 40 and *Figure 41* illustrate the Hawk board's heat sink assembly, along with its dimensions.

Figure 40: Hawk Board Heat Sink Assembly

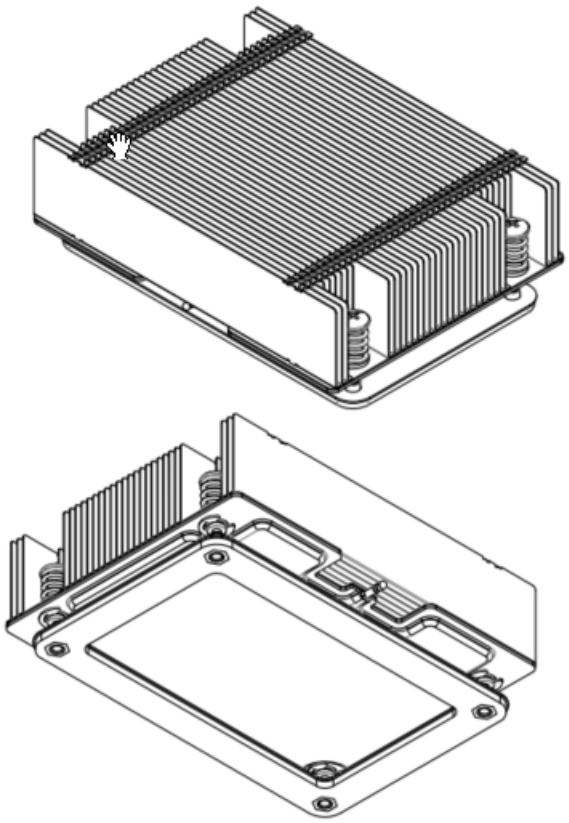
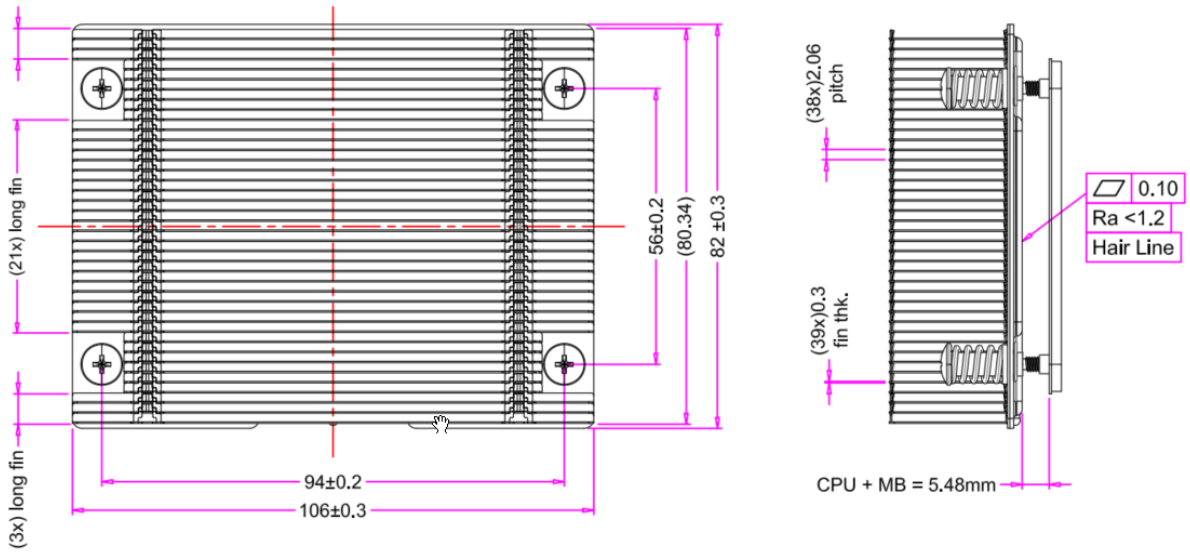


Figure 41: Hawk Board Heat Sink Dimensions



14. Board Power Supplies

14.1. Input Voltages

14.1.1. 12V_ATX Input Voltage Level

The nominal input voltage delivered by the power supply is 12 V DC nominal at light loading with a range of 11 V to 13 V. The motherboard must accept and operate normally with input voltage tolerance range between 10.8 V and 13.2 V when all under voltage related throttling features are disabled. Motherboard's under-voltage protection level must be less than 10.1 V.

14.1.2. 5V_ATX Input Voltage Level

The nominal input voltage delivered by the power supply is 5 V DC nominal at light loading. The motherboard must accept and operate normally with input voltage tolerance range between 4.5 V and 6.5 V.

14.1.3. 3V3_ATX Input Voltage Level

The nominal input voltage delivered by the power supply is 3.3 V DC nominal at light loading. The motherboard must accept and operate normally with input voltage tolerance range between 3 V and 3.6 V.

14.2. CPU Voltage Regulators

Table 87 lists the recommended IC components for providing stable CPU SoC voltages.

Table 87: Recommended ICs for Generating SoC Voltage Rails

POWER RAIL	OUTPUT (V)	CURRENT (A)	CONTROLLER IC
VDDC_SOC	0.87	15*	TPS544B20RVFR
VDD33_SOC	3.3	2	MPM3620AGQV-Z
VDD18_SOC, VDD18_PLL_SOC	1.8	2	MPM3620AGQV-Z
VDD18_PLL_SOC	1.8	2	MPM3620AGQV-Z

*** Note**: The normal operating current is about 6 A. However, the peak current is up to 12-13 A. Hence, it is recommended to use a regulator that can handle a peak current of at least 15 A.

14.3. SoC Voltage Regulator Efficiency

For SOC efficiency measurements:

- VID is set to 0.87 V
- Vin is set to 12.5 V
- Efficiency is measured from input inductor to socket
- Driver and controller loss must be included
- Output voltage is gathered from V_{Sense} of socket
- No additional air flow is supplied to the VR area other than the air flow caused by VRTT tool fan
- Test is done at room temperature (20°C~25°C)
- Voltage measurement is done by tool with 0.05% accuracy or better

- Current measurement is done by tool with 0.25% accuracy or better
- Efficiency curve is higher than the envelope defined below

Vendors are encouraged to exceed the above efficiency requirement and may propose higher efficiency VRMs that may come at additional cost. Power efficiency measured from 12 V input to CPU socket must also be analyzed and improved.

14.3.1. SoC Core Voltage Regulator Configuration

The vendor must use SoC core VR solution with all configurations stored in NVRAM without any external resistor strapping. Vendor must provide utility under CentOS to perform VR configuration change. Configuration change must take effect without AC cycling node. The guaranteed rewrite count of NVRAM must be greater than or equal to 15.

14.3.2. SoC Multi-Layer Ceramic Capacitor (MLCC) Co-Layout

There are capacitors for 0V9_CPU_SOC or VDDC_SOC power rail as listed in *Table 88*.

Table 88: 0.9 V SoC Power Rail Capacitors

POWER RAIL	CAPACITOR
0V9_CPU_SOC or VDDC_SOC	2 x 560 µF D5X9MM
	4 x 22 µF 0805
	3 x 10 µF 0402
	3 x 4.7 µF 0402
	6 x 2.2 µF 0402
	12 x 1 µF 0402
	6 x 0.22 µF 0402
	6 x 0.1 µF 0402

The vendor must perform simulation during design and testing during validation for Z profile of power rails.

14.4. DIMM Voltage Regulators

14.4.1. DIMM Maximum Power

The motherboard supports up to 8 slots DDR4 DIMM with 8 channel DDR0-7. The power can support 80 A x 1.2 V for 8 DIMM and this can up to 160 A x 1.2 V for 8 DIMM DDR4.

The vendor must follow the vendor's memory controller guidelines to design and validate DIMM power rail to support maximum power needed for this configuration, and support 1.2 V for DDR4 DIMM.

14.4.2. DIMM Voltage Regulator Optimizations

DIMM VR must support auto phase dropping for high efficiency across loading. DIMM VR must be compliant to latest VR specification and memory controller vendor's updated validation guideline, and pass test with margin.

Vendor must have different BOM options in VR area to optimize for Single sideboard DIMM slots and Double sideboard DIMM slots.

14.4.3. DIMM Voltage Regulator Efficiency

For DIMM VR efficiency measurements:

- VID is set to 1.2 V
- Vin is set to 12.5 V
- Efficiency is measured from input inductor to PCB near DIMM sockets
- Driver and controller loss must be included
- Output voltage is gathered from PCB at middle of furthest two DIMM slots from CPU
- No additional air flow is supplied to the VR area
- Test is done in room temperature (20°C~25°C)
- Voltage measurement is done by tool and method with 0.05% accuracy or better
- Current measurement is done by tool and method with 0.25% accuracy or better
- Efficiency curve must be higher than the envelope defined below

14.4.4. DIMM Voltage Regulator Configuration

DIMM VR has same configuration requirement as SoC VR, listed in section *0*.

14.4.5. DIMM Voltage Regulator Multi-Layer Ceramic Capacitor (MLCC) Co-Layout

There are capacitors for each DDR4 DIMM memory VR on the top layer of the board between DIMM fields (refer *Table 89*).

Table 89: DIMM Power Rail Capacitors

POWER RAIL	CAPACITOR
0V6_VTT	1 x 10 µF 0402
	1 x 4.7 µF 0402
2V5_VPP	1 x 4.7 µF 0402
	1 x 2.2 µF 0402
1V2_VDD	2 x 10 µF 0402
	2 x 4.7 µF 0402
	2 x 2.2 µF 0402
	1 x 1 µF 0402
	1 x 0.01 µF 0402

The vendor must perform simulation during design, and testing during validation for Z profile of power rails.

14.5. Processor Complex (PCP) VRM

Table 90 lists the power rails for the processor complex (PCP).

Table 90: PCP VRM Power Rails

POWER RAIL	OUTPUT (V)	CURRENT (A)	CONTROLLER IC	PHASES
VDDC_PCP	0.9	140	TPS53679RSBR	5
VDD18_PCP_EVEN, VDD18_PCP_ODD, VDD18_PLL_PCP_EVEN, VDD18_PLL_PCP_ODD	1.8	2	MPM3620AGQV-Z	–

14.6. PCP VRM Efficiency

For PCP efficiency measurement:

- VID is set to 0.93 V
- Vin is set to 12.5 V
- Efficiency is measured from input inductor to socket
- Driver and controller loss must be included
- Output voltage is gathered from V_{Sense} of socket
- No additional air flow is supplied to the VRM area other than the air flow caused by VRTT tool fan
- Test is done in room temperature (20°C~25°C)
- Voltage measurement is done by tool and method with 0.05% accuracy or better
- Current measurement is done by tool and method with 0.25% accuracy or better
- Efficiency curve is higher than the envelope defined below

Vendors are encouraged to exceed the above efficiency requirement and may propose higher efficiency VRMs that may come at additional cost. Power efficiency measured from 12 V input to CPU socket must also be analyzed and improved.

14.7. PCP Core VRM Configuration

The Vendor must use PCP core VRM solution with all configurations stored in NVRAM without any external resistor strapping. Vendor must provide utility under CentOS to perform VRM configuration change. Configuration change must take effect without AC cycling node. The guaranteed rewrite count of NVRAM must be greater or equal to 15.

14.7.1. PCP Multi-Layer Ceramic Capacitor (MLCC) Co-Layout

Table 91 lists the capacitors for the PCP power rails.

Table 91: PCP Power Rail Capacitors

POWER RAIL	CAPACITOR
0V9_PCP	14 x 470 µF 7343
	8 x 22 µF 0603
	13 x 10 µF 0402
	6 x 4.7 µF 0402
	22 x 2.2 µF 0402
	27 x 1 µF 0402
	18 x 0.22 µF 0402
	23 x 0.1 µF 0402

The vendor must perform simulation during design, and testing during validation for Z profile of power rails.

14.8. VRM Design Guidelines

For VRMs, the vendor must list the current budget for each power rail based on worst case loading case in all possible operation conditions. General requirements for VR component selection and VR design must meet 150% of this budget, and OCP must set to 200% of this budget. Vendors must do design check, inform purchasers about the actual OCP setting chosen for VRM, and explain the reason if it cannot meet this general requirement above.

For VRM that require firmware, power code, or configuration file, vendors must maintain version control to track all the releases and changes between each version and provide a method to retrieve version through application software during system run time.

All switching VRs must reserve testing hook for Bode plot measurement.

Hawk CPU, DIMM VR power stages are listed in *Table 92*.

Table 92: CPU and DIMM VR Power Stages

POWER RAIL	CURRENT (A)	# OF PHASES	HAWK PASS #1	HAWK PASS #2
VDDC_PCP	140	5	TPS53679RSBR	XDPE12284C
VDDC_SOC	6	–	TPS544B20RVFR	TPS53915RVET
VDD33_SOC	2	–	MPM3620AGQV-Z	TPS53915RVET
VDD18_SOC, VDD18_PCP_EVEN, VDD18_PCP_ODD, VDD18_PLL_PCP_EVEN, VDD18_PLL_PCP_ODD, VDD18_PLL_SOC	2	–	MPM3620AGQV-Z	TPS53915RVET
VDD15_SOC	2	–	MPM3620AGQV-Z	TPS53915RVET
1V2VDDQ_DDR	40	2	TPS53659RSBR	XDPE12284C

POWER RAIL	CURRENT (A)	# OF PHASES	HAWK PASS #1	HAWK PASS #2
0V6_VTT_DDR	3	–	TPS53317RGBR	TPS53317ARGB
2V5_VPPQ_DDR	6	–	MP8733AGLE-Z	TPS53915RVET

- Different BOM options and VR firmware can accommodate AVL with exceptions. The vendor's manufacture process must be able to handle different BOM, matching AVL of power stage.
- If different VR firmware is required to support different power stages, VR firmware must have unique ID in user specific area matching each power stage.

14.9. Hard Drive Power

Power for hard drives need to be obtained directly from the PSU. The motherboard does not support hard drive power.

14.10. System VRM Efficiency

Vendors must supply high efficiency VRMs for all other voltage regulators over 20 W not defined in this specification. All other voltage regulation modules must be 91% efficiency over the 30% to 90% load range. Vendors are encouraged to deliver systems with higher efficiencies. If higher efficiencies are available at additional cost, vendors must make those options known.

14.11. Power-on Conditions

Motherboard must be set to restore last power state during AC on/off. This means that, when AC does on/off cycle, the motherboard must power on automatically without requiring interaction with the power button. Only when motherboard is powered off on purpose, then motherboard must be kept powered off through AC on/off.

14.12. High Power Use Cases

High power use case means the system power is larger 504 W (42 A @ 12 V). This is not a typical use case, but support is required to enable testing of such a configuration. Typically, it is caused by fully populating Non-Volatile DIMM, high TDP CPU, and heavy load on PCIe slots, or a combination of the above. Motherboard design and power delivery must allow such use case with BOM change below:

- Populate both power connectors with Pressfit cables.
- Change R_{Sense} of HSC from 2 x 1 mΩ to 2 x 0.5 mΩ

The vendor must perform simulation during design and testing during validation for high power kit.

15. Acronyms and Abbreviations

Table 93 lists the commonly used acronyms and abbreviations used in this document.

Table 93: Acronyms and Abbreviations

TERM	DESCRIPTION
ANSI	American National Standards Institute
BIOS	Basic Input/Output System
BMC	Baseboard Management Controller
CFM	Cubic Feet Per Minute (Measure Of Volume/Flow Rate)

TERM	DESCRIPTION
CMOS	Complementary Metal Oxide Semiconductor
DCMI	Data Center Manageability Interface
DDR4	Double Data Rate Type 4
DHCP	Dynamic Host Configuration Protocol
DIMM	Dual Inline Memory Module
DPC	DIMMs Per Memory Channel
DRAM	Dynamic Random Access Memory
ECC	Error-Correcting Code
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electromagnetic Interference
FRU	Field Replaceable Unit
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
ILM	Independent Loading Mechanism
IPMI	Intelligent Platform Management Interface
KCS	Keyboard Controller Style
LAN	Local Area Network
LDO	Low-dropout
LPC	Low Pin Count
LUN	Logical Unit Number
MAC	Media Access Control
MTBF	Mean Time Between Failures
MUX	Multiplexer
NIC	Network Interface Card
OOB	Out Of Band
OU	Open Compute Rack Unit (48 mm)
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
POD	Pseudo Open-drain
POST	Power-On Self-Test
PSU	Power Supply Unit
PWM	Pulse-Width Modulation
PXE	Pre-boot Execution Environment

TERM	DESCRIPTION
QSFP	Quad Small Form-Factor Pluggable
RMC	Rack Management Controller
RU	Rack Unit (1.75”)
SAS	Serial-Attached Small Computer System Interface (SCSI)
SATA	Serial AT Attachment
SCK	Serial Clock
SCP	Secure Copy Protocol
SDA	Serial Data
SDR	Sensor Data Record
SEL	System Event Log
SFP	Small Form-Factor Pluggable
SMBIOS	Systems Management BIOS
SMBUS	Systems Management Bus
SMT	Surface Mount Technology
SOL	Serial Over Lan
SPI	Serial Peripheral Interface
SSD	Solid-State Drive
SSH	Secure Shell
TDP	Thermal Design Power
TOR	Top Of Rack
TPM	Trusted Platform Module
U	Rack Unit
UART	Universal Asynchronous Receiver/Transmitter
UEFI	Unified Extensible Firmware Interface
VRM	Voltage Regulator Module

16. Document Revision History

Table 94: Document Revision History

ISSUE	DATE	DESCRIPTION
1.0	April 22, 2020	Initial release.