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OAI

SERVER

Building on DC-SCM to support OAI

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Benefit of MBA

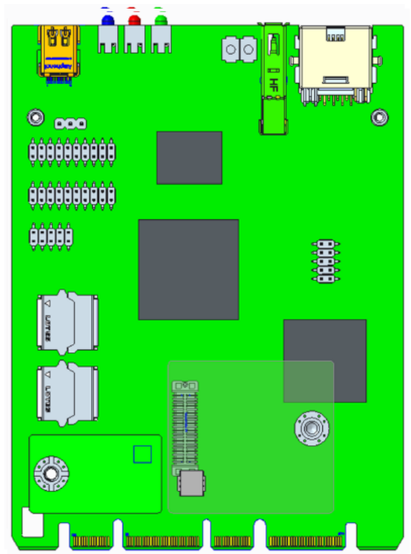
(Modular Building Block Architecture)

- Time to concept evaluation
- Time to market
- Reduce development costs/resources
- Optimize assembly and maintenance costs

Build OAI-SCM Based on DC-SCM

- The idea is to leverage DC-SCM design by re-mapping I/Os for OAI-SCM
- For ODMs who haven’t built OAI HIB with BMC, it gives an option to use DC-SCM for OAI system

Flexible Interfaces Defined on DC-SCM



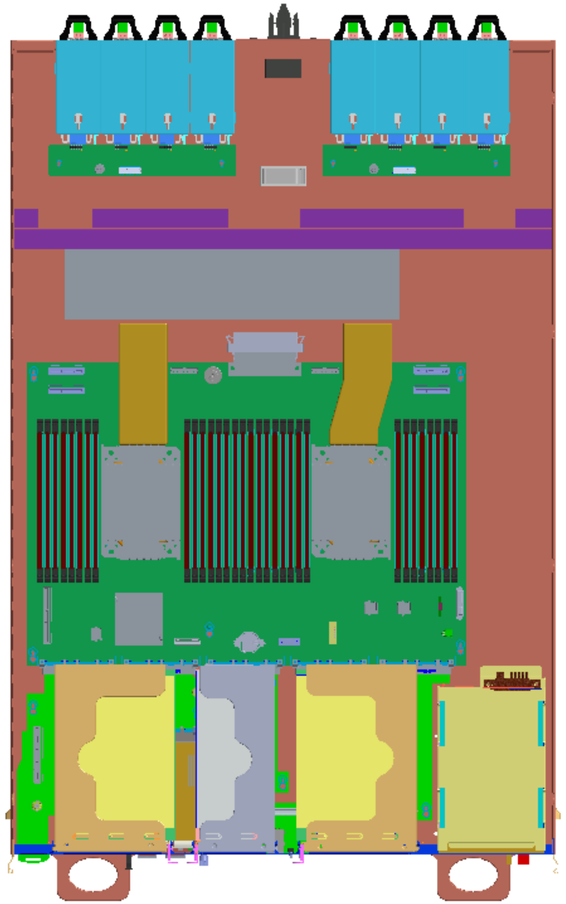
Signals on Golden Finger

- PCIE
- LPC/eSPI (slave)
- SPI (master)
- UART
- SGPIOs
- I2C
- USB2.0 (host/slave configurable)
- JTAG (Master)
- NC-SI
- Programmable IOs

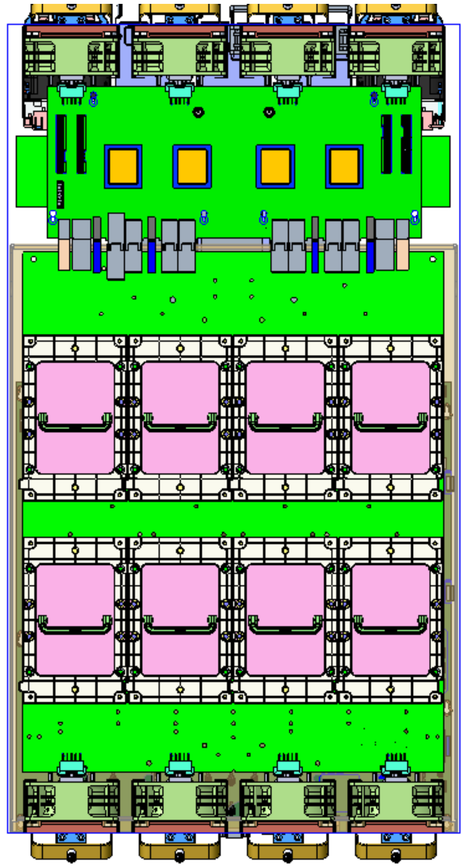
Dimension

- SCM size: 120.4mm x 90mm (4.74” x 3.55”)
- Standard OCP size: 115mm x 76mm (4.53” x 3”)

Server System



OAI System



Flow of Building on DC-SCM to Support OAI-SCM

Block Diagram Evaluation

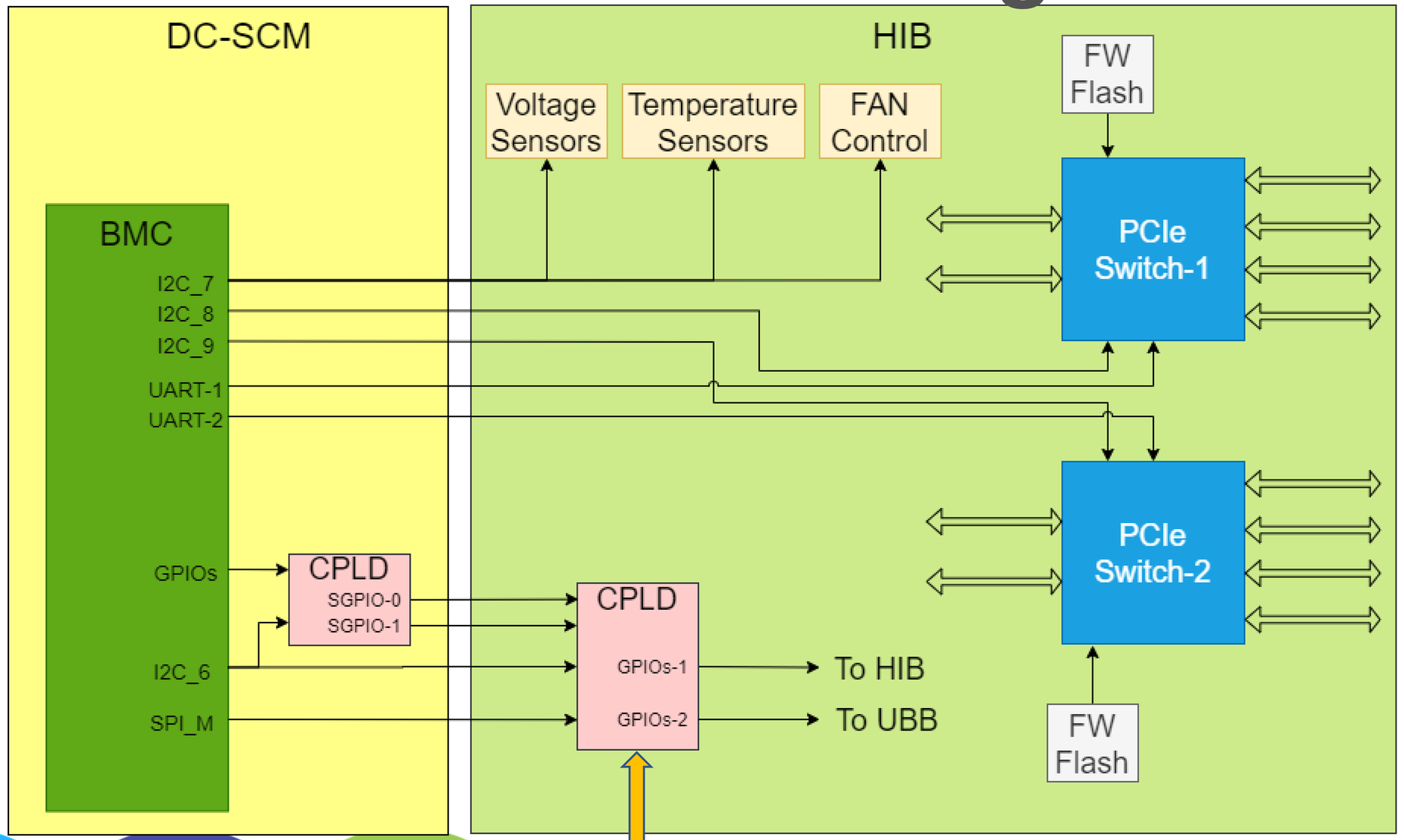
- I2C/smbus Topology
- HW monitor diagram
- Power control diagram
- Management data collection
- Management network

Physical Placement Evaluation

Interface and I/O Re-mapping

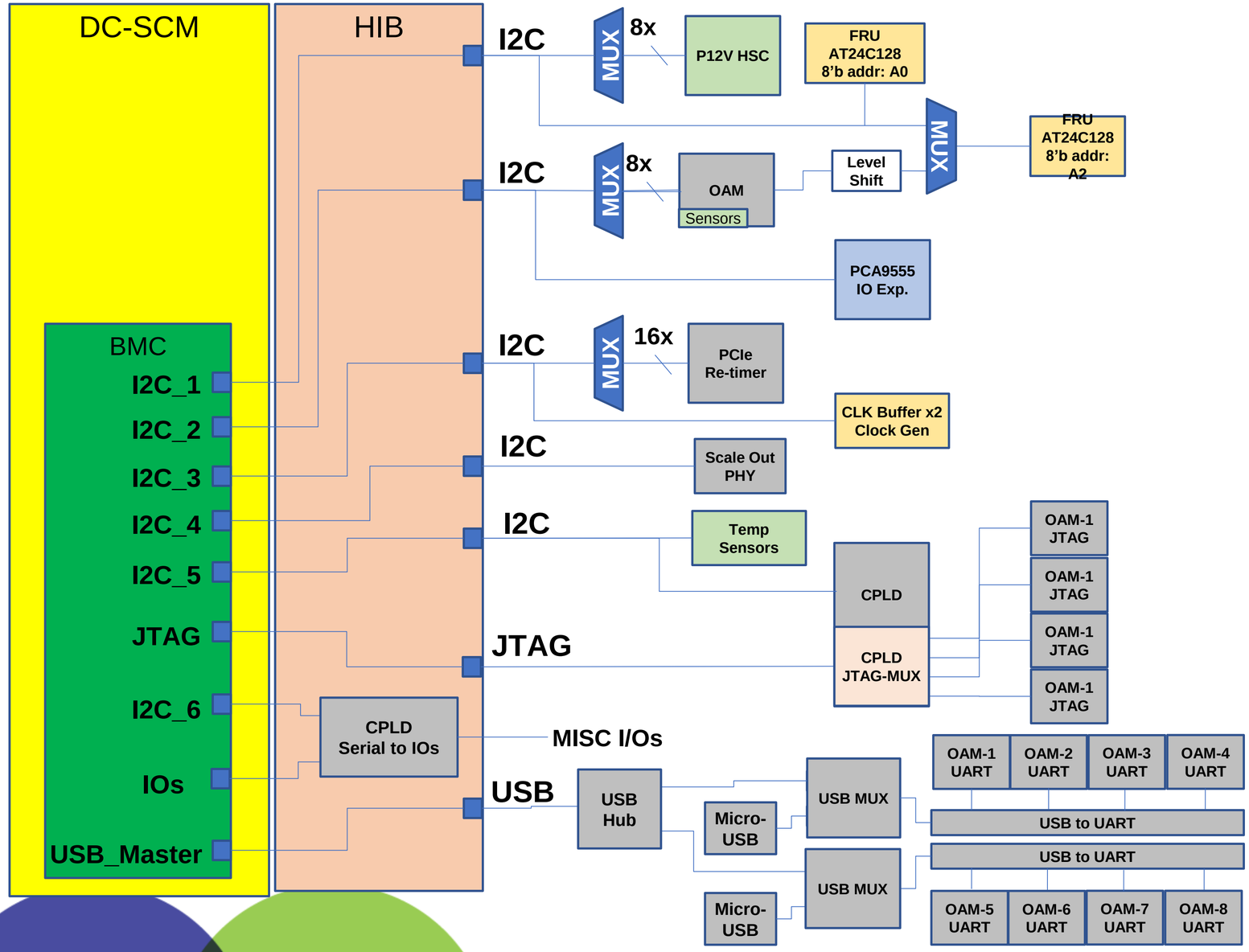
- Map I2C/smbus topology
- Map I/Os into SGPIO data bit
- Map Power control signals
- Map USB topology
- Map UART/JTAG topology
- Map NC-SI topology

Host-Interface-board Diagram



Remap I/O for HIB and UBB

DC-SCM I/O to UBB



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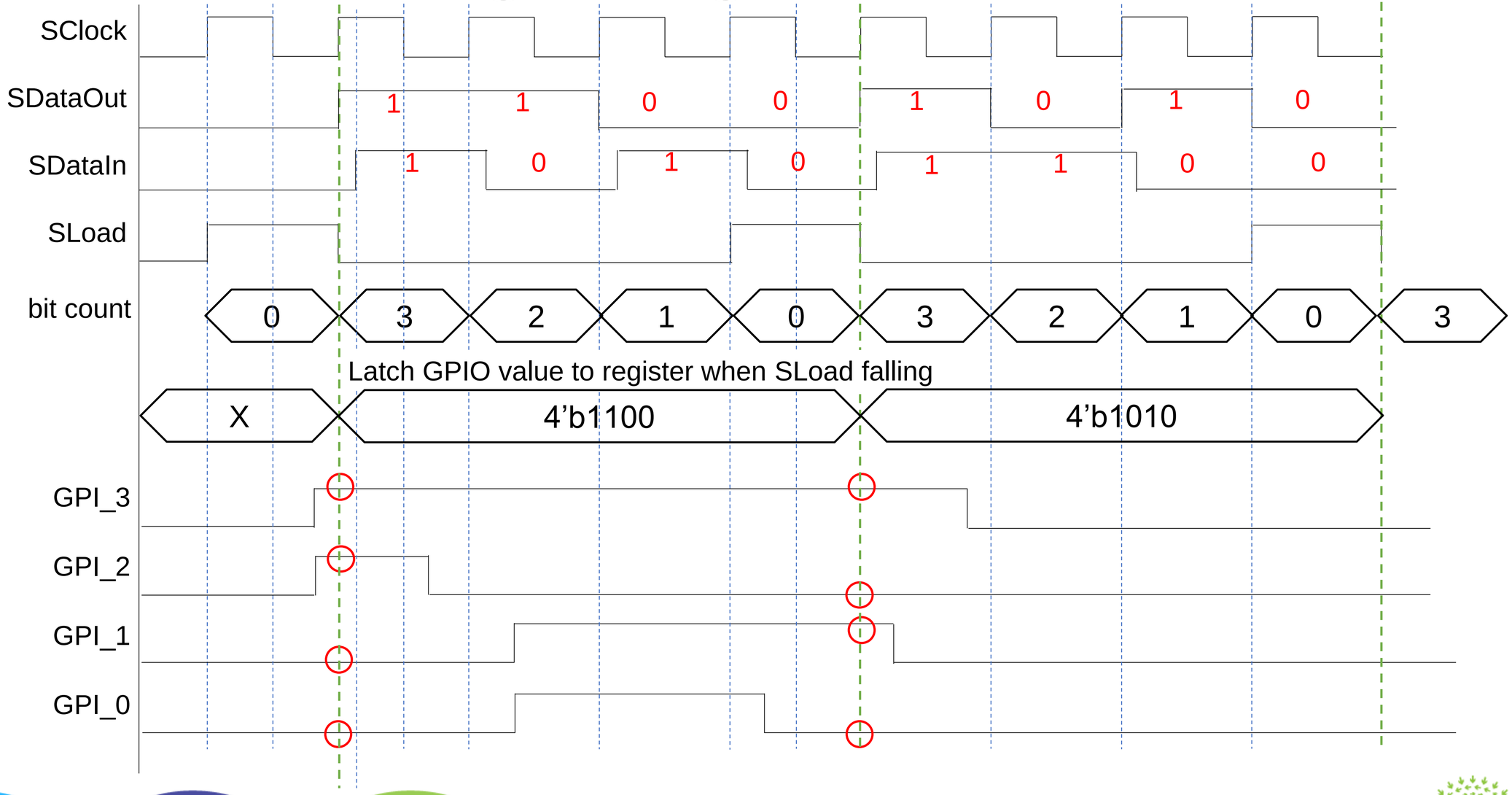
SGPIO-1 assignment on HIB CPLD

BIT	Direction	Signal	Description
Bit[1]	Output	UART_SEL_0	UART SEL bit0 to UBB
Bit[2]	Output	UART_SEL_1	UART SEL bit1 to UBB
Bit[3]	Output	UART_SEL_2	UART SEL bit2 to UBB
Bit[4]	Output	UART_MUX_EN_N	UART MUX enable to UBB
Bit[8:5]	Output	JTAG_MUX_EN_N	JTAG MUX Enable[4:1] to UBB
Bit[10:9]	Output	JTAG_MUX_SEL	JTAG MUX SEL[2:1] to UBB
Bit[14:11]	Output	JTAG_SEL[4:1]	JTAG SEL[4:1] to UBB
Bit[16:15]	Output	UBB_FRU[1:0]_WP	FRU Write protect bit[1:0] to UBB
Bit[18:17]	Output	USB_MUX_SEL_[1:0]	For USB Mux selection
Bit[19]	Output	FRU_SEL	Level shift IC enable to UBB
Bit[23:20]	Output	WARMRST#	Warm Reset bit[4:1], Vref output to UBB
Bit[27:24]	Output	SW[3:0]_PE_RESET_N	RSVD SW to UBB CPLD for PERESET_N
Bit[31:28]	Bi-directional	RSV_BMC_SEC_CPLD[3:0]	RSVD GPIO between BMC and CPLD
Bit[32]	Input	UBB_PWR_READY	UBB power ready to HIB BMC
Bit[48:33]	Bi-directional	RSV_BMC_PRI_CPLD[15:1]	RSVD GPIO between BMC and CPLD
Bit[49]	Output	CPLD_PRI_FW_UPDATE_EN_N	Enable PRI CPLD FW update
Bit[50]	Output	CPLD_SEC_FW_UPDATE_EN_N	Enable SEC CPLD FW update
Bit[51]	Input	UBB_DETECT_LOOP	UBB board PRSNT pin

SGPIO-2 assignment on HIB CPLD

BIT	Direction	Signal	Description
Bit[1]	Output	PWRBRK_N	DC-SCM PWRBRK signal from DC-SCM to HIB CPLD as one of the sources of UBB PWRBRK
Bit[2]	Input	I2C_OAM_SLAVE_AUX_ALERT_N	From UBB Slave I2C alert to HIB
Bit[3]	Input	I2C_CPLD_TEMP_AUX_ALERT_N	From UBB through HIB to SCM
Bit[4]	Input	I2C_EFUSE_FRU_AUX_ALERT_N	From UBB through HIB to SCM

SGPIO Timing Diagram



SDataIn arrived after SClock sent to Target and latched on the falling edge of SCLK

Summary

- DC-SCM provides flexible interfaces and it can be used as OAI-SCM by remapping interface
- To polish the architecture of modular design, we’re trying to use it into various applications and get feedbacks. It is similar to "the use or disuse theory" in evolutionary Biology. The part uses more will become more developed.

DC-SCM in an OAI System

02-25-2020

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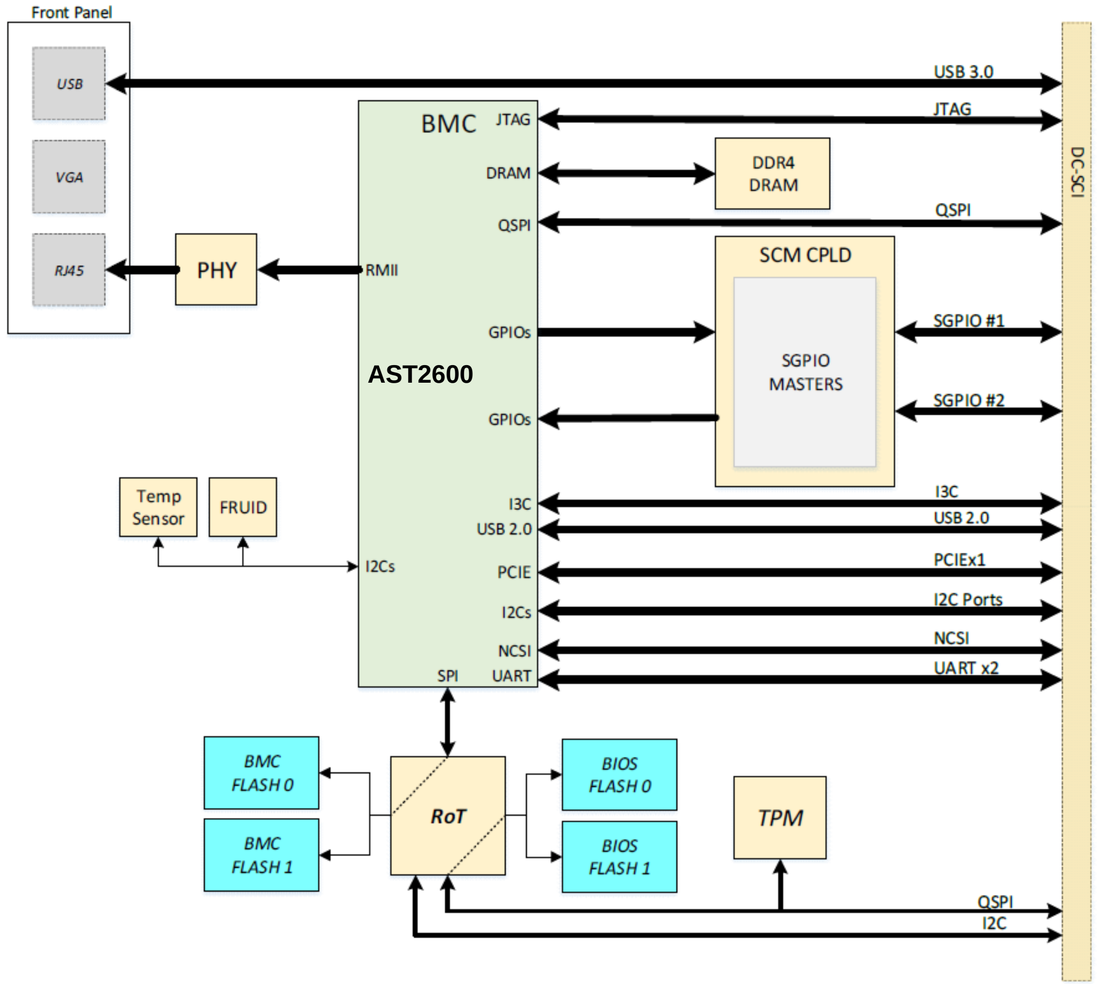
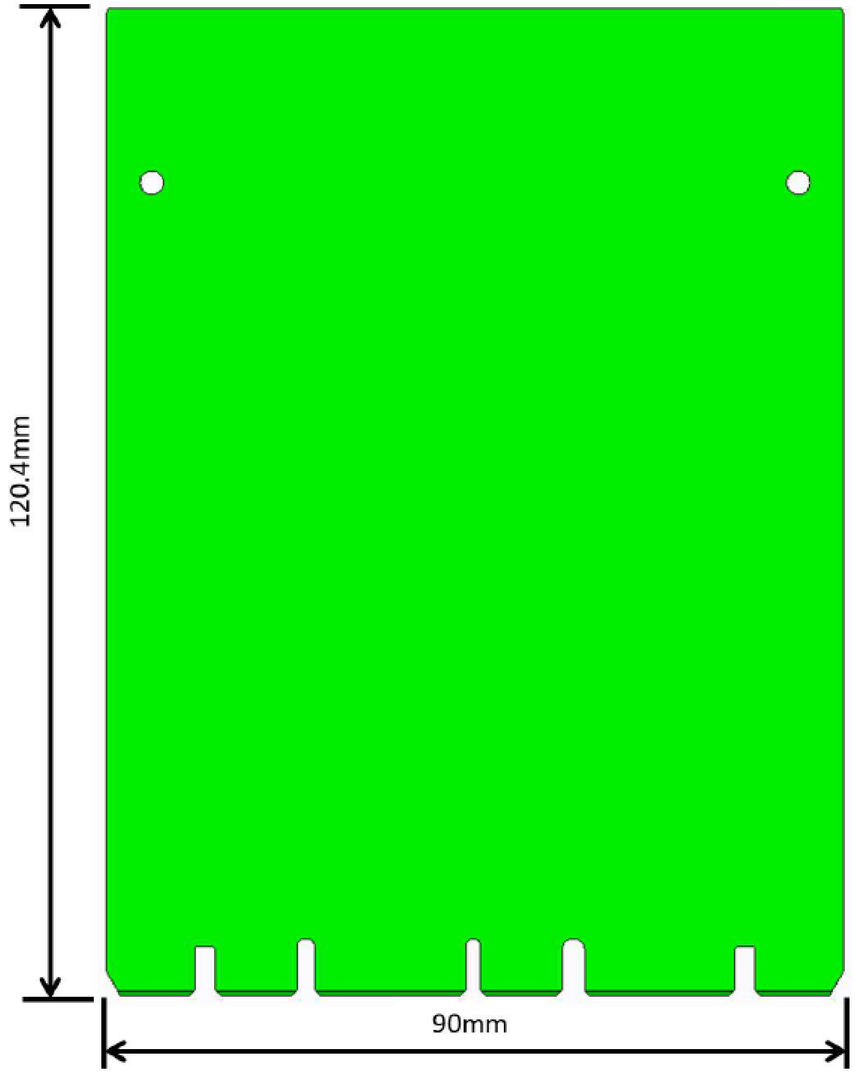
Architectural Evaluation of DC-SCM in ZT/IEC's OAI System

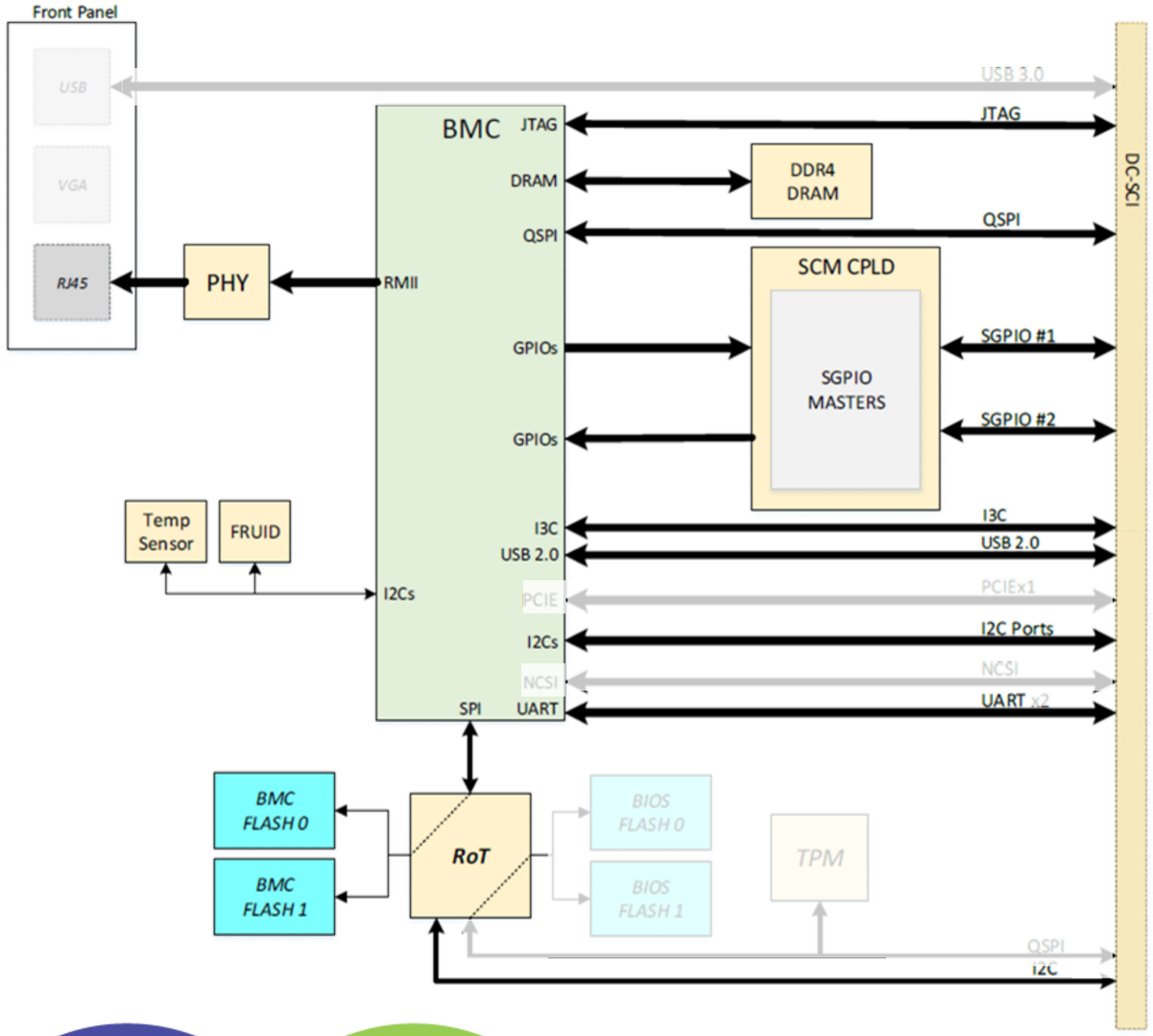
- Functional and Device Check
- Detailed Signal Comparison and Bus Topology
- SGPIO Signal Requirement
- Mechanical Assessment with SCM Placement

DC-SCM Block Diagram & PCB Dimension



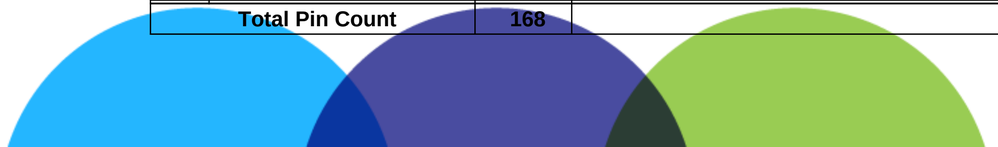


OAI-SCM for OAI-HIB Diagram



DC-SCM Signal List vs OAI Implementation

DC-SCI Pinout Signal Group				OAI Requirement (ZT/IEC)		
No.	Signal Function	Pin Count	Description	Usage	Signals	Pin Count
1	RoT	4	1. I2C[11] for Rot to MB FPGA 2. RoT_CPU_RST_N: CPU reset 3. RoT_CPU_RST_AUTH_N: connect to HPM FPGA	Yes	I2C[11]	2
2	GND	29	Power and signal return path.	Yes	All	29
3	I2C Bus	20	BMC I2C[10:1] bus to HPM	Yes	All	20
4	I3C	8	I3C[4:1] bus frequency is up to 12.5MHz for DDR5 DIMM	Yes	Through level shift device to I2C[14:11]	8
5	JTAG	5	JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, JTAG_TRST_N	Yes	All	5
6	LPC_ESPI	9	1. ESPI_LPC_SEL 2. ESPI_ALERT_N, CLK_ESPI_LPC, ESPI_RESET_N/LPC_RESET_N , ESPI_CS_N/LPC_FRAME_N 3. ESPI_IO[3:0]/LPC_LAD[3:0]	No		0
7	Misc	12	1. IRQ[1:0], IRQ_BMC_SMI_N 2. SYS_PWRBTN_N, SYS_PWROK, PCU_PWROK, PSU_AC_PWROK 3. RST_PLTRST_BUF_N, CPU_CAERR_N 4. DBP_PREQ_N, DBP_PRDY_N,. FBRK_N	Partial	2. SYS_PWRBTN_N, SYS_PWROK, PCU_PWROK, PSU_AC_PWROK 3. RST_PLTRST_BUF_N (reserved)	5
8	NCSI	8	NCSI_CLK, NCSI_CRS_DV, NCSI_TXEN, NCSI_TXD[1:0], NCSI_RXER, NCSI_RXD[1:0]	No		0
9	PCIe	7	1. BMC_PCIE_RST_N 2. CLK_100M_PCIE_DP/DN 3. PCIE_BMC_TX/RX_DP/DN	No		0
10	PECI	2	PECI_BMC, PVCCIO_PEC	No		
11	Power	4	Up to 28W	Yes	All	4
12	Reservation	17	Reserved in future.	??		
13	SGPIO	10	1. SGPIO0_DO, SGPIO0_CLK, SGPIO0_DI, SGPIO0_LD 2. SGPIO1_DO, SGPIO1_CLK, SGPIO1_DI, SGPIO1_LD 3. SGPIO_RESET_N, SGPIO_INTR_N	Yes	All	10
14	SPI Bus	16	1. SPI1_CLK, SPI1_CS_N, SPI1_MOSI, SPI1_MISO 2. QSPI1_CLK, QSPI1_CS_N, QSPI1_D[3:0] 3. QSPI2_CLK, QSPI2_CS_N, QSPI2_D[3:0]	No		0
15	STBY_Power Control	3	HPM_STBY_PG, HPM_STBY_EN, HPM_STBY_RST_N	Yes	HIB_STBY_PG, HIB_STBY_EN, HPM_STBY_RST_N	3
16	UART	4	1. UART1_TX/RX 2. UART2_TX/RX	Partial	UART1_TS/RX (Inspur only)	2
17	USB	10	1. USB2.0: USB[3:1]_DP/DN 2. USB3.0: USB1_TX+/-, USB1_RX+/-	Partial	USB2.0: USB2_DP/D USB2.0: USB3_DP/DN (ZT/IEC, Hyve only)	4
Total Pin Count		**168**				



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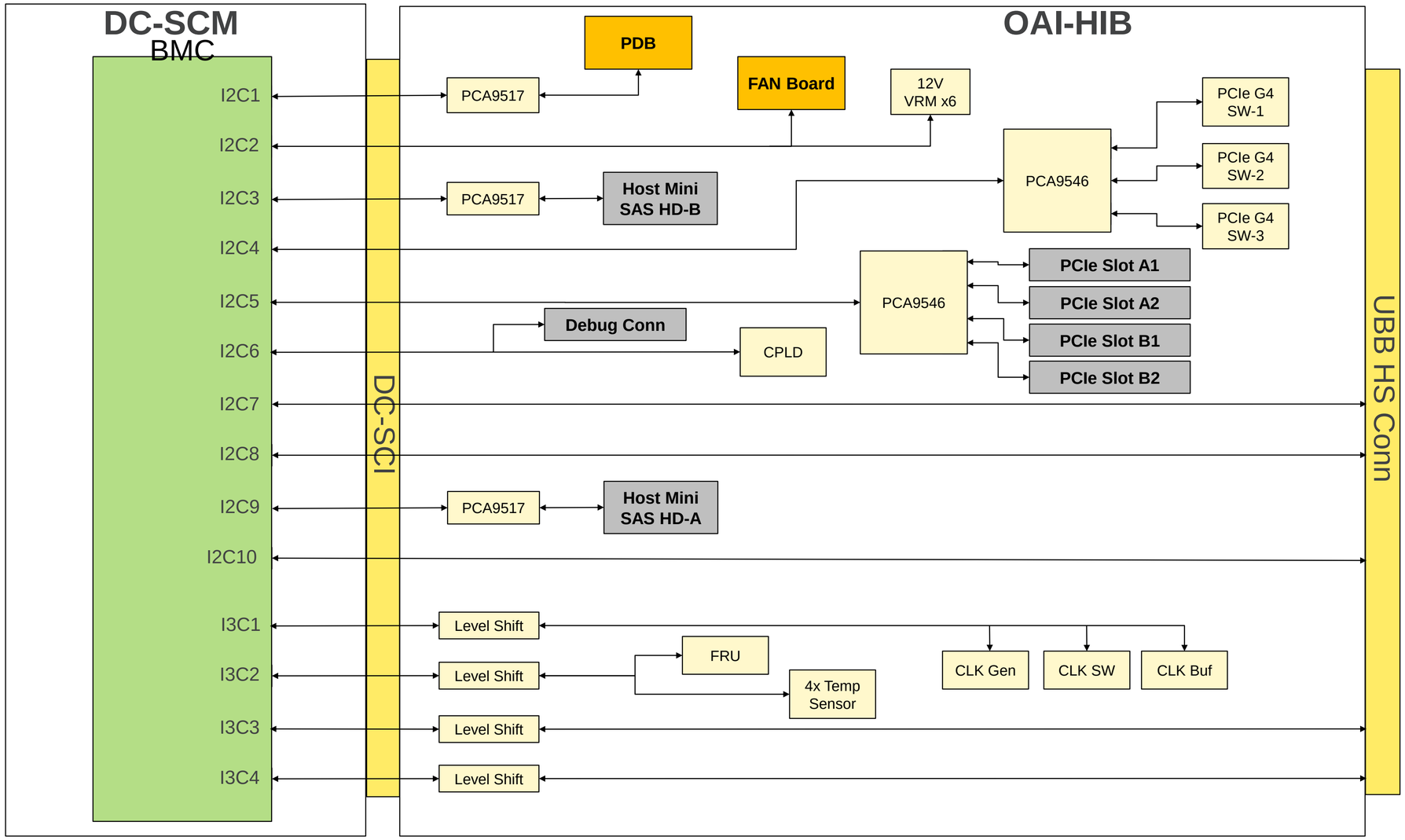
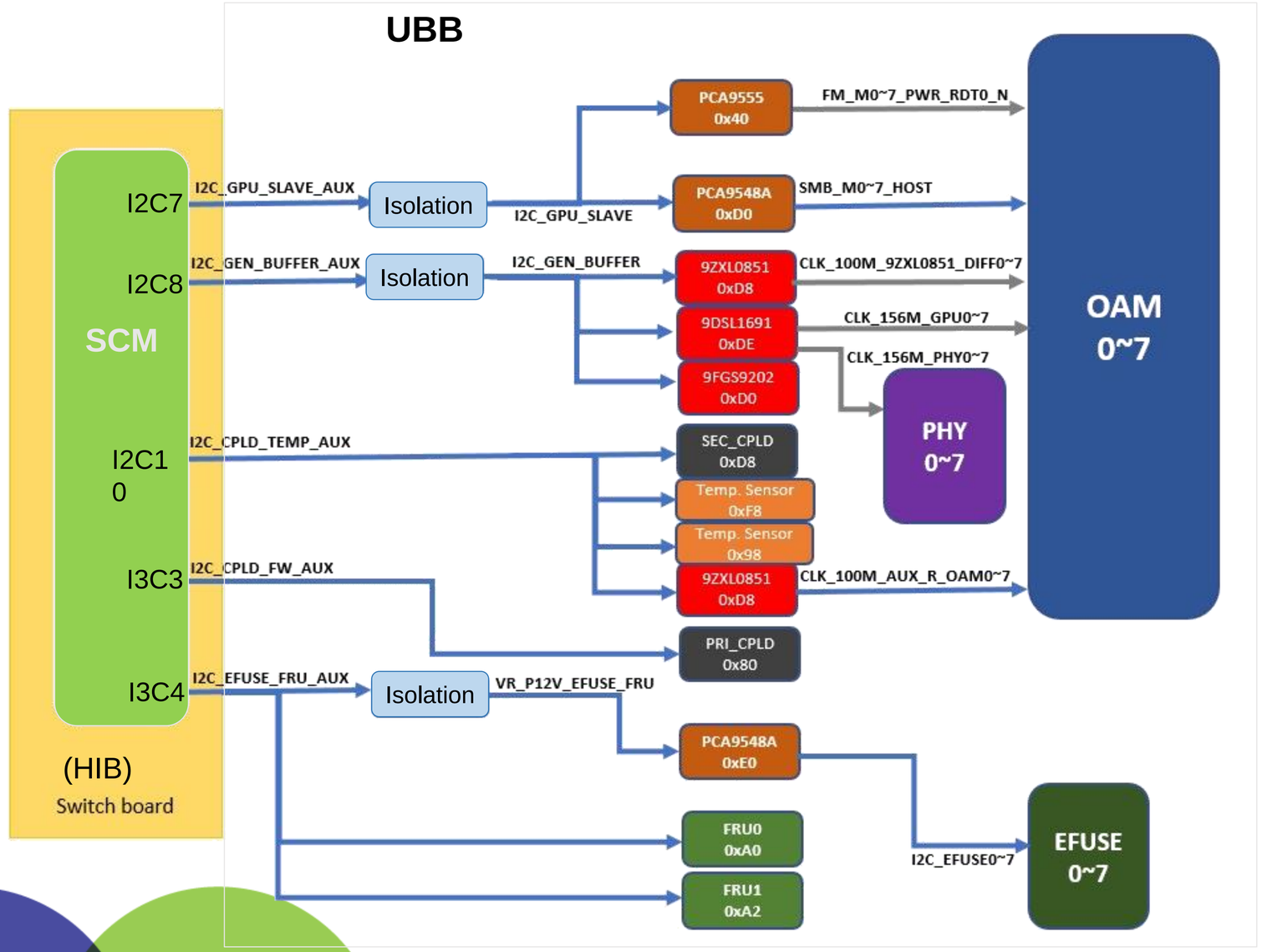
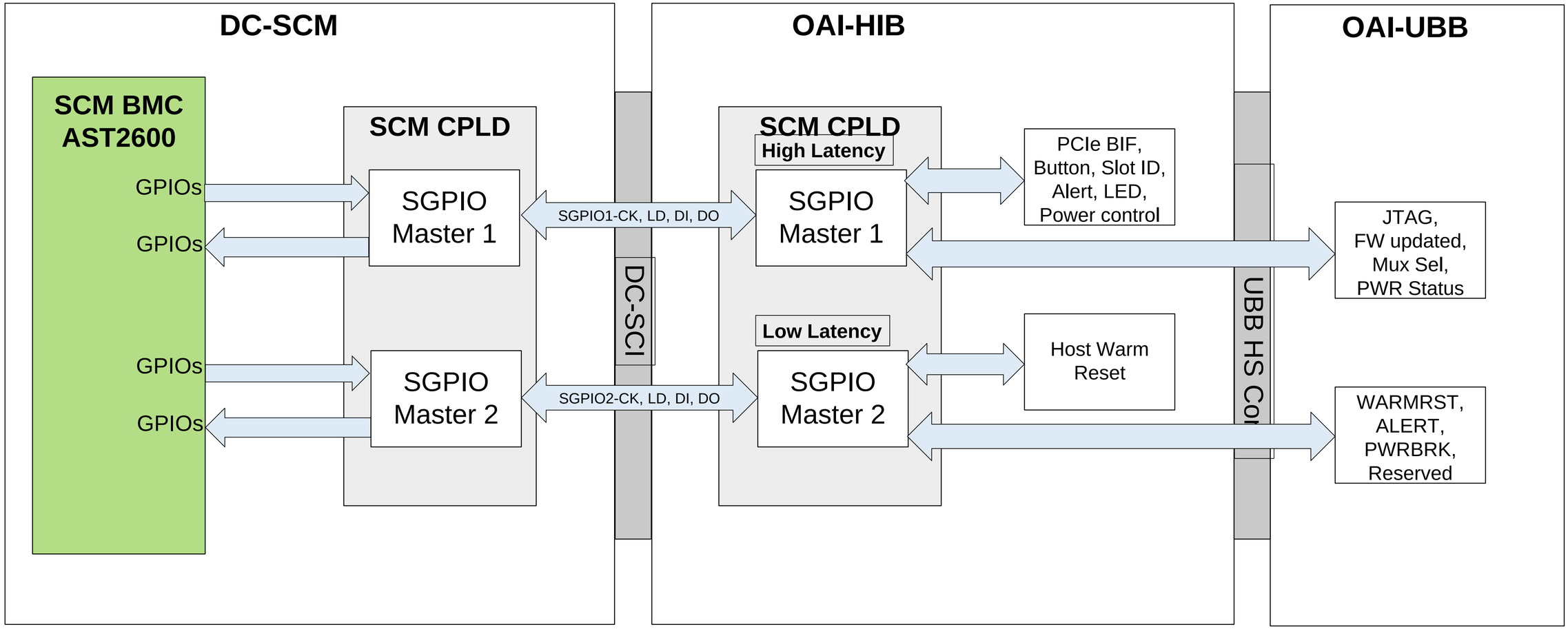
HIB I2C bus Topology



UBB I2C bus Topology



OAI-SCM SGPIO System Block Diagram



OAI-SCM SGPIO: UBB Signals

Direction	Signal	Pin Count	Description
Output	JTAG_MUX_EN_N[2:1]	2	JTAG MUX Enable[2:1] to UBB
Output	JTAG_MUX_SEL[2:1]	2	JTAG MUX SEL[2:1] to UBB
Output	JTAG_SEL[4:1]	4	JTAG SEL[4:1] to UBB
Output	EEPROM_WP[2:1]	2	EEPROM Write protect bit[2:1] to UBB
Output	FRU_WP[2:1]	2	FRU Write protect bit[2:1] to UBB
Output	FRU_SEL	1	Level shift IC enable to UBB
Output	WARMRST[4:1]_L	4	Warm Reset bit[4:1] output to UBB
Output	SW_RESET[4:1]	4	PCIe SW Reset Bit[4:1]to UBB
Bi-directional	RSV_BMC_SEC_CPLD	4	RSVD GPIO[4:1] between BMC and CPLD
Bi-directional	RSV_BMC_PRI_CPLD	15	RSVD GPIO[15:1] between BMC and CPLD
Output	CPLD_PRI_FW_UPDATE_EN_N	1	UBB Primary CPLD FW updated enable
Output	CPLD_SEC_FW_UPDATE_EN_N	1	UBB Secondary CPLD FW updaed enable
Input	SMB_ALERT	1	SMBus Alert
Output	PWR BRK	1	Power break from management or PSU
Input	PWR_BTN	1	Power Button input to DC-SCI's power BTN output
Input	UBB Present#	1	Detection UBB full connection
Input	USB_MUX_SEL_[2:1]	2	Inform BMC UART2USB controller-1/2 for local USB conn or BMC remote debug. (ZT/ICE, Hyve only)
Output	UART_MUX_EN_N	1	UBB's 8x OAM UART debug selection. (Inspur only)
Output	UART_SEL_[2:0]	3	UBB's 8x OAM UART debug selection. (Inspur only)
Input	UBB_PWR_READY	1	UBB power ready to inform BMC for OAI power ready reporting

OAI-SCM SGPIO: HIB Signals

Direction	Signal	Pin Count	Description
Output	9SDL_1691_SEL_A_B_N	1	HIB PCIe clock source selection
Input	BIF_HOSTA_ID[1:0]	2	PCIe bus bifucation from host via mini SAS HD conn-A
Input	BIF_HOSTB_ID[1:0]	2	PCIe bus bifucation from host via mini SAS HD conn-B
Output	BMC_BTN_SYSRST_N	1	OAI system reset button output
Output	BMC_BTN_UID_LED_N	1	OAI system UID button
Output	BMC_HOST[3:0]_WARM_RST_N	4	BMC asserts warm reset to UBB.
Output	BMC_PS_ON_N	1	BMC output PS-ON to CPLD
Output	BMC_PWR_BUT_LOCK_N	1	BMC lock power button in CPLD
Input	BUTTON_PWRON_RC_N	1	Power Button input
Input	BUTTON_UID_RC_N	1	UID button
Input	CABLE_PRSNT_HOSTA/B_[4:1]_N	4	Mini SAS HD Connector A/B present detection for PCIe G4 x16
Output	CPLD_BMC_PERST_N	1	BMC output PERST to HIB CPLD
Output	EN_BMC_CPLD_FW_N	1	HIB CPLD FW updated enable
Input	FM_SLOT_A1/2_ID[2:0]	6	Idetification PCIe card A1/2 type
Input	FM_SLOT_A1/2_PRSNT_N	2	Slot-A1/2 present detection
Input	FM_SLOT_B1/2_ID[2:0]	6	Idetification PCIe card B1/2 type
Input	FM_SLOT_B1/2_PRSNT_N	2	Slot-B1/2 present detection
Inputput	FM_WAKE_SLOT_N	1	PCIe slot wake signal
Output	LED_GPU[8:1]_GRN/RED	8	UBB OAM status LED on UBB
Input	P0V9_A/B/C_VR_HOT_N	3	PCIe SW device A power VR Hot alert
Input	PWR_IN_ALERT_P0V9_A/B/C_N	3	PCIe SW device A power VR alert
Input	PWRBRK_HOSTA/B_N	2	Host power break output via mini SAS HD cable-A/B
Input	RST_BTN_SYSRST_N	1	OAI system reset button input
Output	RST_SLOT_I2C_SWITCH_N	1	Rerst I2C swtich device (SW to 4 slots)
Input	WARMRST_HOSTA/B_N	2	Host warm reset output via mini SAS HD cable-A/B

Functional Compatibility Results

BMC Device

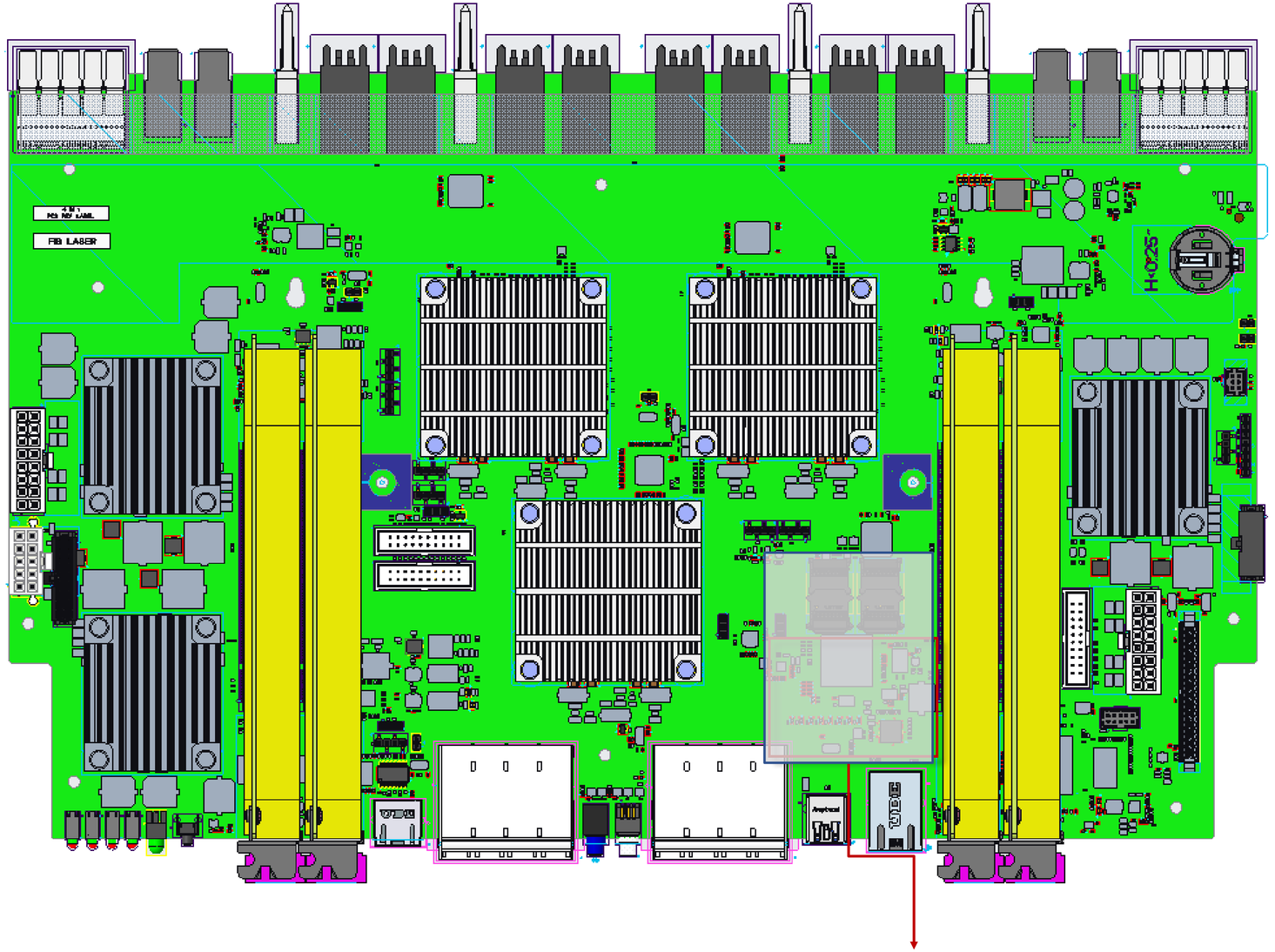
- The current HIB in the OAI system is using AST2500.
- DC-SCM BMC is using AST2600, which would require porting to a new code base.

MDC/MDIO

- BMC’s MDC/MDIO pins for PHY re-timer configuration are not defined on DC-SCI.
- Request made to DC-SCM team to add these to the reserved pins

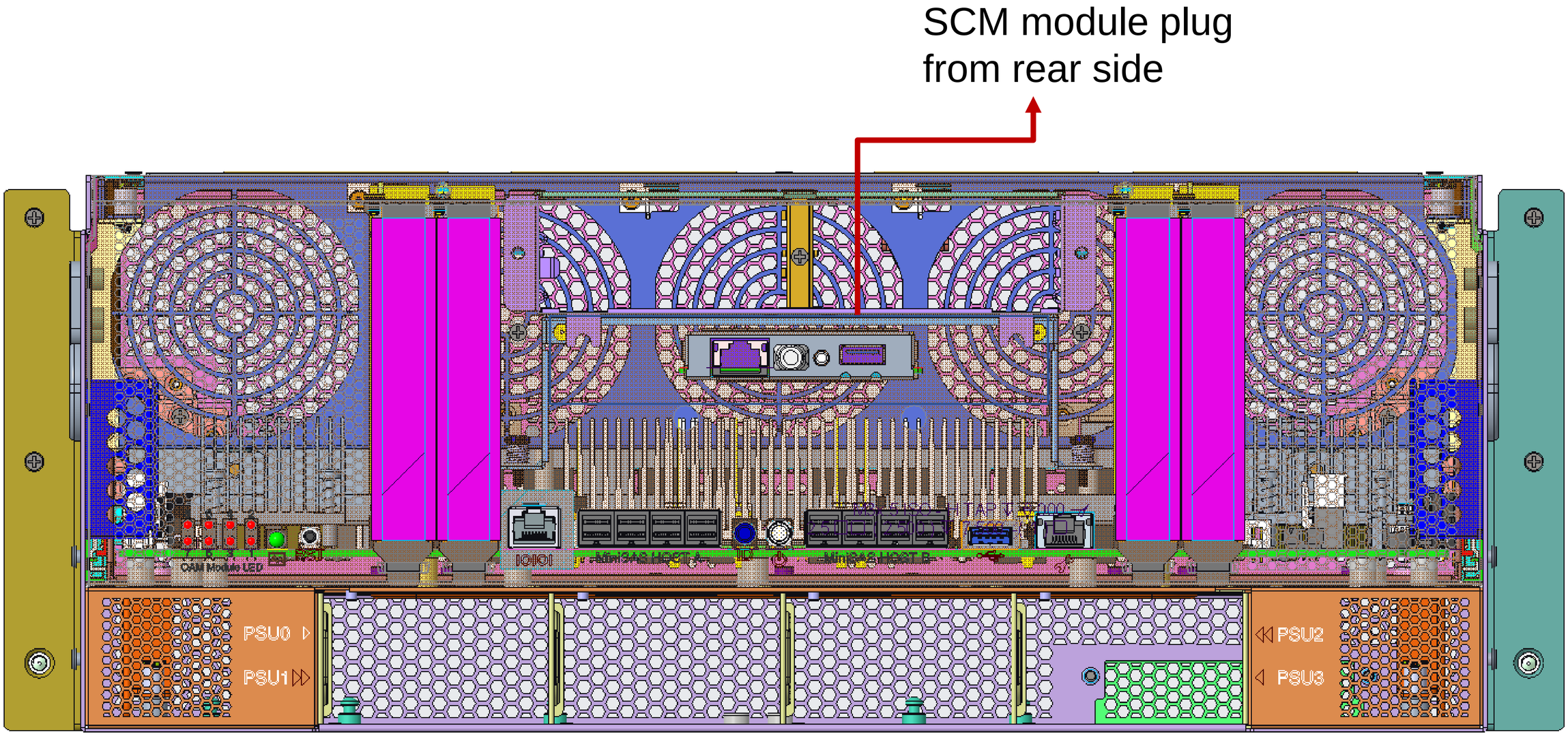
Preference for some signals such as PWRBRK to be routed directly across the SCI interface

HIB with SCM Placement

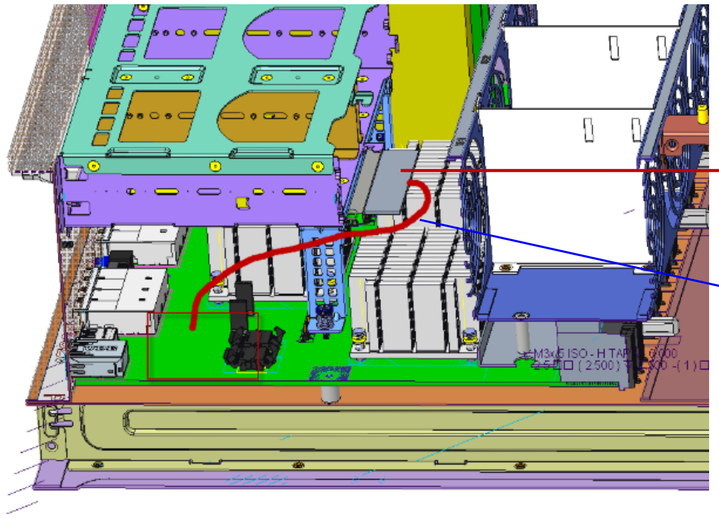


Remove the BMC related component and place the connectors of SFF1002 cable solution

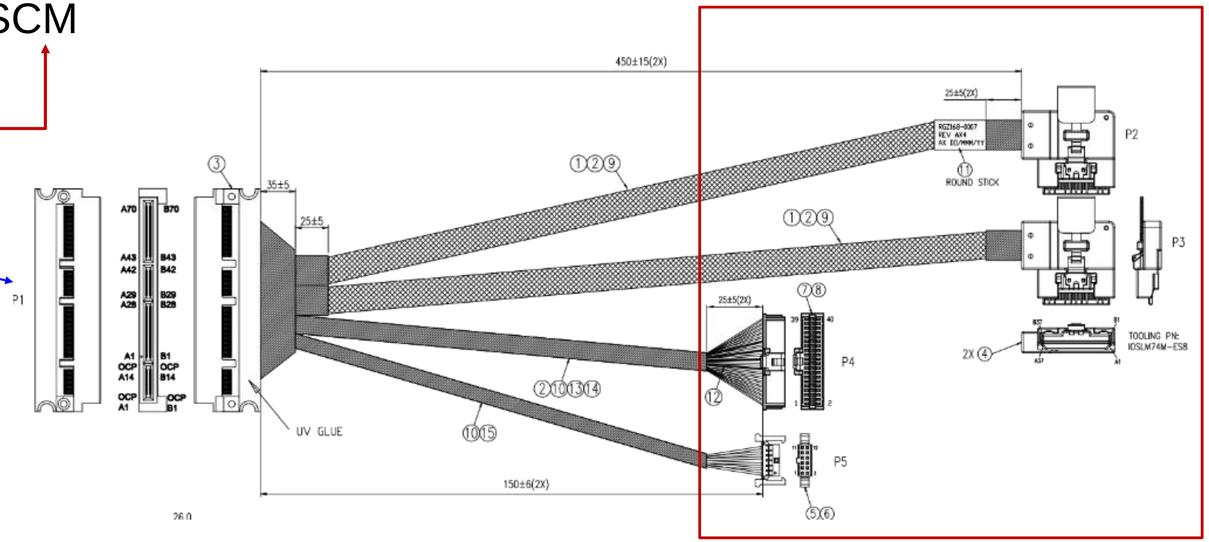
Mechanical Rear View



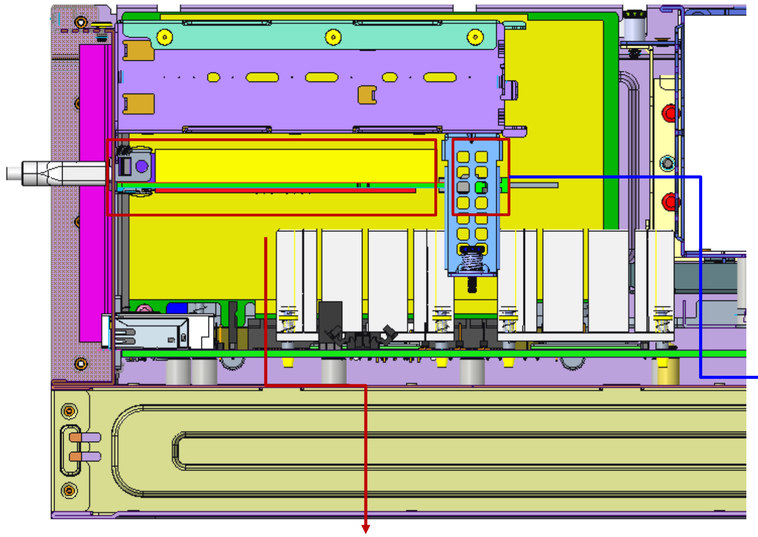
System side view

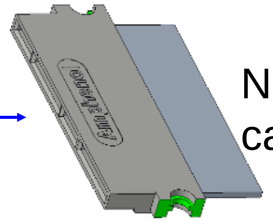


Cable solution from HIB to SCM



This cable solution is for OCP 3.0 NIC connection. We will redefine it for the SCM application.





Need to design mechanical feature fix the cable end

Need to design mechanical feature to support SCM plug in

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Call to Action

- Join OCP Server Project/OAI Sub-Project to share feedbacks
- Where to find additional information (URL links)

  Project Wiki with latest specification : https://www.opencompute.org/wiki/Server/OAI

  Mailing list: https://ocp-all.groups.io/g/OCP-OAI

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