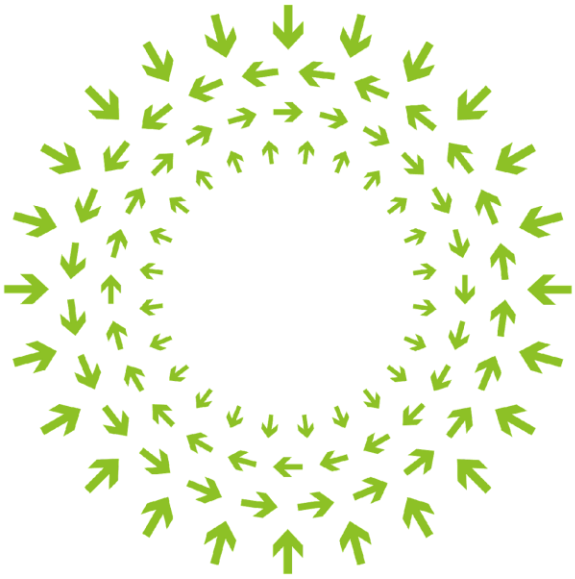

OPEN

Compute Project

Full Width HPM Form Factor (M-FLW) Base Specification

Part of the

Datacenter – Modular Hardware Systems (DC-MHS) Rev 1.0 Family

Version 0.80

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1.2. Acknowledgements

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2. Version Table

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Date	Version #	Description
4/22/2022	0.70	Initial Public Release
06/07/2022	0.75	• Added Spec Compliance Table Section 4 • Added 9.75mm to board under PSU Connectors • Moved OCP NIC Connector 6mm to left. (from 204.29mm to 210.29mm) • Moved IO Riser Connector #3 to left 5mm. Moved KOZ and Mount hole accordingly (From 136.02mm to 141.02mm) • Rotated PIC Power Connectors 180° • Defined Pins S1 & S12 on Pic Power Connectors and Rear Power Connectors and revised dimensioning scheme to Pin S1 • Figure 18, Defined IO Connectors Pin A1 & A77. • Defined Pins OB1 & B70 on NIC & DCSCM Connectors • Defined Pins OB1 & B70 and Pins B1 & B70 on Alternate NIC Connectors • Defined Control Panel Connector Pins A1 & A10 • New location for USB connector Zone • Moved Retention Hardware Height Restriction Zone note to Detail L • Combined 1U & 2U PCIE Mount Holes to one sheet • Revised references to “KIZ” to “Height Restriction Zone” • Revised Bottom Side KOZ shape for Tempan to rectangle. Revised Y-dimensioning scheme to center of rectangle • Added KOZ to Bottom side Mount Holes. Preliminary size at 13.8mm x 13.8mm. • Changed Figure 3 to support OCP NIC move of 6mm • Changed Figure 4 to show pads and KOZs around mounting holes • Updated Figure 6 for clarity • Changed Figure 10 to move OCP NIC by 6mm. • Changed Figure 11, Control panel connector orientation, and primary/secondary designations. • Changed Figure 12, USB Zone moved. • Combined Figure 17 and 18 into a new Figure 17. Moved 1U PCIe Riser Mount holes down 7.5mm and left 4mm. Added Mount Hole detail with Ø8.0mm Pad size, Ø16mm Component KOZ. • Changed Figure 21 to update Secondary size KOZs for mounting holes and chassis hooks • Updated Figure 29 for UBB outline updates

		• Added Figure 32 for UBB connector locations • Changed description of Adapted HPM in Section 13 • Figure 26 changed, rotating PIC Power connectors 180 degrees • Relocated power plane fusing requirements to M-PIC spec in Section 11.2 • Clarified minimum power plane recommendation in Section 11.2
06/27/2022	0.80	• Modified Table4 in Section 11.1 to describe zone power and range of supported power • Clarified minimum power plane recommendation in Section 11.2 • Renamed Figure 22 • Figure 19, Sec 10.13, Changed primary side height restriction zones • Sect 10.12, Figure 18 change KOZ around Riser retention holes • Sect 10.8, Figure 12, moved Intrusion connector to same zone as USB • Figure 21, updated MH KOZs on bottom / secondary side. • Updated UBB Adapted outline in Figure 29 to update cutout options for cabled HSIO at far edge. • Figure 33 updated, based on connector feature updates from vendors • Figure 35, updated text in drawing • Figure 25, updated title in drawing • Added Guide pin part number to Sect 13.1.6 • Added bullet 6 to section 10.10.1 • Figure 18, 19, updated KOZ around riser retention holes • Figure 22, updated Thermal solution Bracketry KOZ • Section 10.8, new section for PDB to HPM header • Moved section 12 into existing sections and deleted it • Moved section 13.1 into Section 12 “Adapted HPMs” for spec clarity.

3. Scope

This document defines technical specifications for the Server Product used in Open Compute Project. This document shall comprise the hardware product types complete technical specification. Any supplier seeking OCP recognition for a hardware product based on this spec must be 100% compliant with all features or requirements described in this specification.

3.1. Items Not in Scope of Specification

- Compute Core (CPU/Memory/Voltage Regulators/SMP routing between CPUs)
- JTAG/Debug connectors for the Compute Core
- CPU, Memory, Heatsink, Liquid and any other thermal solutions
- Reliability requirements and design-in details
- BOM Population requirements
- Cooling System Connections (Fans, etc).

3.2. Typical OCP Sections Not Applicable

Open Compute documents are typically expected and desired to contain common document Sections. The DC-MHS specifications are comprised of Base Form Factor Specifications and Supporting Platform Connectivity specifications, and are structured such that the typical OCP document structure does not apply to this Base Form Factor Spec. This specification will not contain the following Sections.

- Rack Compatibility (See **Section 13.1 Rack and Chassis Depth Stackup Assumptions**)
- Physical Specifications
- Thermal Design Requirements
- Rear Side Power, I/O, Expansion
- Onboard Power System
- Environmental Regulations/Requirements
- Prescribed Materials
- Software Support
- System Firmware
- Hardware Management
- Security

The content expected in these subject areas is expected to be documented in future private and/or public Design Specifications and/or Product Specifications.

4. Specification Compliance Table

240 The following table is intended summarize the list of attributes and requirements for a design to be DC-MHS M-FLW Base Specification compliant.

Table 1. Specification Compliance Summary Table

#	Technical Specification	Document Reference
1	Base Mechanical Outline	Figure 3 and Section 10.1
2	Minimum of 6 board mounting holes implemented	Figure 4, Section 10.2
3	Mounting Hole pad and KOZ requirements	Figure 4, Section 10.2
4	Maximum HPM Board thickness of 3.18mm, assuming 10% max tolerance	Section 10.3
5	Maximum allowable HPM thickness + backing plate stackup of 5.86mm	Section 10.3
6	Required Board hole for HPM retention to chassis	Section 10.4
7	KOZ required on top and bottom sides around HPM Retention hole	Section 10.4.1
8	HPM requires a hole at Far side for interface to mechanical handle	Section 10.5
9	HPM must fix OCP NIC R3 and DC-SCM R2 locations as defined	Section 10.6
10	HPM shall implement 2 instances of M-PIC Control panel connectors per defined locations	Section 10.7
11	HPM PDB Management Connector placement	Section 10.8
12	HPM Shall implement Internal USB connection and Intrusion Switch connectors in defined zone	Section 10.9
13	Boot Storage Peripheral connector required in defined zone	Section 10.10
14	HPM shall implement 6x Near IO connectors in defined locations (exceptions defined if not enough IO ports)	Section 10.11.1
15	X dimensions defined for Near IO connectors shall be followed.	Section 10.11.3
16	Y-location of Near IO connectors shall be between Datum A and Datum B limits	Section 10.11.3
17	Population requirements for Recommended Near IO connectors	Section 10.11.2
18	Y-location of Near IO connectors shall be between Datum A and Datum B limits	Section 10.11.3
19	Mounting hole requirements for IO module retention	Section 10.11.4
20	Primary side component height restriction zone shall be implemented	Section 10.13
21	Max height restrictions shall apply to mated connector heights, unless exception noted	Section 10.13
22	Secondary side universal height restriction of 1.6mm shall apply, with exceptions noted	Section 10.14.1, Figure 21
23	HPM shall support chassis to board bracketry (board pan) and associated Keepout Zones	Section 10.14.2, Figure 21
24	HPM Thickness + Backside components shall not exceed 5.86mm	Section 10.14.3
25	HPM shall implement KOZ's on Far side mounting holes for Thermal solution brackets	Section 10.15, Figure 22
26	HPM shall implement Cabling Enablement KOZ's	Section 10.16, Figure 1910.15
27	HPM CRPS connector placement	Section 11.1.1
28	HPM 2x6+12s PICPWR connector placement	Section 11.1.2
29	HPM Power Plane requirements	Section 11.2

5. Overview

The objective of this specification is to specify the requirements of a Full Width Host Processor Module (HPM). This is for use within products designed for minimum 19" rack, also known as compliant with EIA-310-D but can also accommodate larger 21" racks. This form factor enables a full width HPM usage for CPUs, DIMMs, and related features. This full width form factor generally allows for maximum IO of the CPUs to be offered and brought to accessible slots (although exceptions could occur in the future). This specification will NOT reference a specific CPU or memory technologies. The goals and success criteria of this specification is so that multiple generations of CPU/Memory (Compute Core) designs can be designed into this form factor specification, so that chassis and system designs can be reused as desired. This should have the benefits of reduced design investment, reduced validation investment, and faster development cycle time.

This specification shall define attributes and design requirements that are common and critical to the use and deployment of customers and vendors of Enterprise and Cloud Full Width Server rack products. Examples include mechanical form factor, placement guidance of common subsystems and placement guidance of motherboard Input-Output (IO) connections.

6. References

The **D**ata **C**enter – **M**odular **H**ardware **S**ystem (DC-MHS) family of specifications are written to enable interoperability between key elements of datacenter and enterprise infrastructure by providing consistent interfaces and form factors among modular building blocks. At the time of this publication there are the following specification workstreams:

- **M-FLW** (**M**odular Hardware System **F**ul**L W**idth Specification) – Host Processor Module (HPM) form factor specification optimized for using the full width of a Standard EIA-310-D Rack mountable server. The specification is not limited to use within the EIA-310 Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-DNO** (**M**odular Hardware System Partial Width **D**e**n**sity **O**ptimized Specification) – Host Processor Module (HPM) specification targeted to partial width (i.e. ½ width or ¾ width) form factors. Such form factors are often depth challenged and found not only in enterprise applications but also in Telecommunications, Cloud and Edge Deployments. While the EIA-310 Rack implementation is chosen as a key test case for use, the specification is not limited to use within the EIA-310-D Rack but is used to serve as a template for a common target where the design is expected to be utilized.
- **M-CRPS** (**M**odular Hardware System **C**ommon **R**edundant **P**ower **S**upply Specification) – Specifies the power supply solutions and signaling expected to be utilized by DC-MHS compatible systems.
- **M-PIC** (**M**odular Hardware System **P**latform **I**nfrastructure **C**onnectivity Specification) – Specifies common elements needed to interface a Host Processor Module (HPM) to the platform/chassis infrastructure elements/subsystems. Examples include power management, control panel and cooling amongst others.

- **M-XIO** (**M**odular Hardware System E**x**tensible **I**/**O**) – Specifies the high-speed connector hardware strategy. An M-XIO source connector enables entry and exit points between sources such as Motherboards, Host Processor Modules & RAID Controllers with peripheral subsystems such as PCIe risers, backplanes, etc. M-XIO includes the connector, high speed and management signal interface details and supported pinouts.
- **M-PESTI** (**M**odular Hardware System **Pe**ripheral **S**ideband **T**unneling **I**nterface) – Specifies a standard method for discovery of subsystems, self-describing attributes, and status (e.g., versus a priori knowledge/hard coding firmware and BIOS for fixed/limited configurations). Examples: vendor/module class, physical connectivity descriptions, add-in card presence, precise source to destination cable coupling determination.

To access additional DC-MHS specification please visit OCP Server WIKI

Additional References

This specification also relies on the following Open Compute Project specifications

- OCP Server Network Interface Card (NIC) R3.0 – Specifies NIC card form factors targeting a broad ecosystem of NIC solutions and system use cases.
  Mezz (NIC) » Open Compute Project

- OCP Datacenter Secure Control Module (DC-SCM) R2.0 – Specifies a SCM designed to interface to an HPM to enable a common management and security infrastructure across platforms within a data center.
  Hardware Management/Hardware Management Module - Open Compute

7. Terminology

Standardized Term	Meaning	Alternative Terms
Shall	Indicates a requirement for spec compliance	
HPM (Host Processor Module)	PCB or PCBA form-factor being defined by this spec	Motherboard, board
PCB	Printed Circuit Board	
DC-SCM	Datacenter Secure Control Module Rev 2.0 as defined by OCP DC-SCM Rev 2.0 spec	
CPU	Central Processing Unit	
IO	Input Output, commonly referring to high speed connections to a CPU socket.	
PCIe	Peripheral Component Interconnect Express	
CXL	Compute Express Link, open standard for CPU to device and CPU to Memory connections.	
Chassis-Board Bracket	Bracket that attaches to a HPM assembly, that enables a variety of board outlines and hole locations to change over time, and still fit within same chassis base.	Board Pan Sub-pan
Near	Board location or zone, related to section of board containing DC-SCM Rev 2.0, Management subsystem	
Far	Board location or zone, opposite of location of Management Subsystem	
Platform	Complete system including HPM, power, peripherals, etc	
Compute Core	Elements of board design that are critical to processor and memory support, inclusive of CPU and Memory sockets. Examples are Voltage Regulators, High Speed IO routing, High speed trace routing between multiple processors, high speed trace routing between processors and memory, etc	
Platform Custom Zone	Area of system board where space is allotted for Platform designers to implement custom features.	
HSIO	High Speed IO, commonly referring to PCIe routing, PCIe connectors, CXL routing/connectors, etc.	
OCP	Open Compute Project	
OEM	Original Equipment Manufacturer	Enterprise
Platform Infrastructure Connectivity Spec	A Specification that defines Platform Interconnect details for features that are common across many HPM Form Factors. Examples connectivity features include fans, backplanes, and control panels.	M-PIC spec
KOZ	Keepout Zone, a design term for PCB designs that defines area of a board design where no components may be placed, usually to enable mechanical attachments or mechanical features.	
Compliant HPM	An HPM which meets every item listed in the M-FLW specification compliance table.	
Adapted HPM	An HPM which has strong correlation to M-DNO requirements but does not meet every item in the M-DNO specification compliance table.	
HPM Designer	The person or organization designing an HPM (whether compliant or adapted) which implements the M-DNO specification.	
System Designer	The person or organization designing a system which incorporates M-DNO HPMs (whether compliant or adapted) into the system design.	

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8. Background and Assumptions

This Full Width HPM Form Factor specification is created to enable typical platform feature sets for both Front and Rear Management, in 1U and 2U chassis applications. Some of the platform features that are common in the industry, and influence the Form Factor constraints are:

a. Chassis installation within minimum EIA-310-D racks (but not limited to).
b. PCIe (Version 5.0 and future) Card configurations typically offered by Enterprise OEMs/Hyperscalers. See **Figure 38. Typical 1U and 2U PCIe Slot Configurations**.
c. In the 1U PCIe offering, only Half-Length PCIe cards (167.6mm) are considered. This does not prevent Three-Quarter Length (254mm) cards, but support for Three-Quarter Length cards would require more restrictive Compute Core placement (not defined).
d. HPM enabled minimum 75W of power per PCIe slot, with ability to scale up to 600W for some slots (likely 3~4).
e. The specification details support for the Open Compute peripherals directly connected to board
    a. OCP NIC R3.0
    b. DC-SCM R2.0
    c. *Note: A S*ystem is not limited to 1 device of each type; configurations with >1 OCP NIC R3.0 or DC-SCM R2.0 are possible, but outside the scope this specification will cover.
f. Thermal Design Points considerations includes keepout zone to enable air cooling thermal solutions that extend beyond the CPU and Memory sockets. Memory TDPs under consideration are 20W – 25W range.
g. Considerations for Liquid cooling solutions, including CPU cold plates and DIMM liquid cooling manifolds.
h. Considerations for Power Delivery to important chassis subsystems.

8.1. Rear Management (ie, OEM) Architecture Assumptions

a. Chassis depth constraints in consideration of
    a. Power Distribution Units placed approximately 780mm from front EIA mounting flange.
    b. Enterprise Storage and Fan subsystems requiring approximately 220mm.
    c. See **Figure 37. Rack Depth Constraints**
b. Sliding rack rails that require a max overall chassis width of 434mm, with interior chassis width/opening of minimum 427mm.
c. Considerations for Power and High-Speed IO Cabling
d. Considerations for Ease of Installation and Removal of motherboard in a chassis.
e. Adequate delivery power through HPM to enable typical Storage configuration power loads (See **Section 11 Power Delivery**)

8.2. Front Management (ie, Hyperscale) Architecture Assumptions:

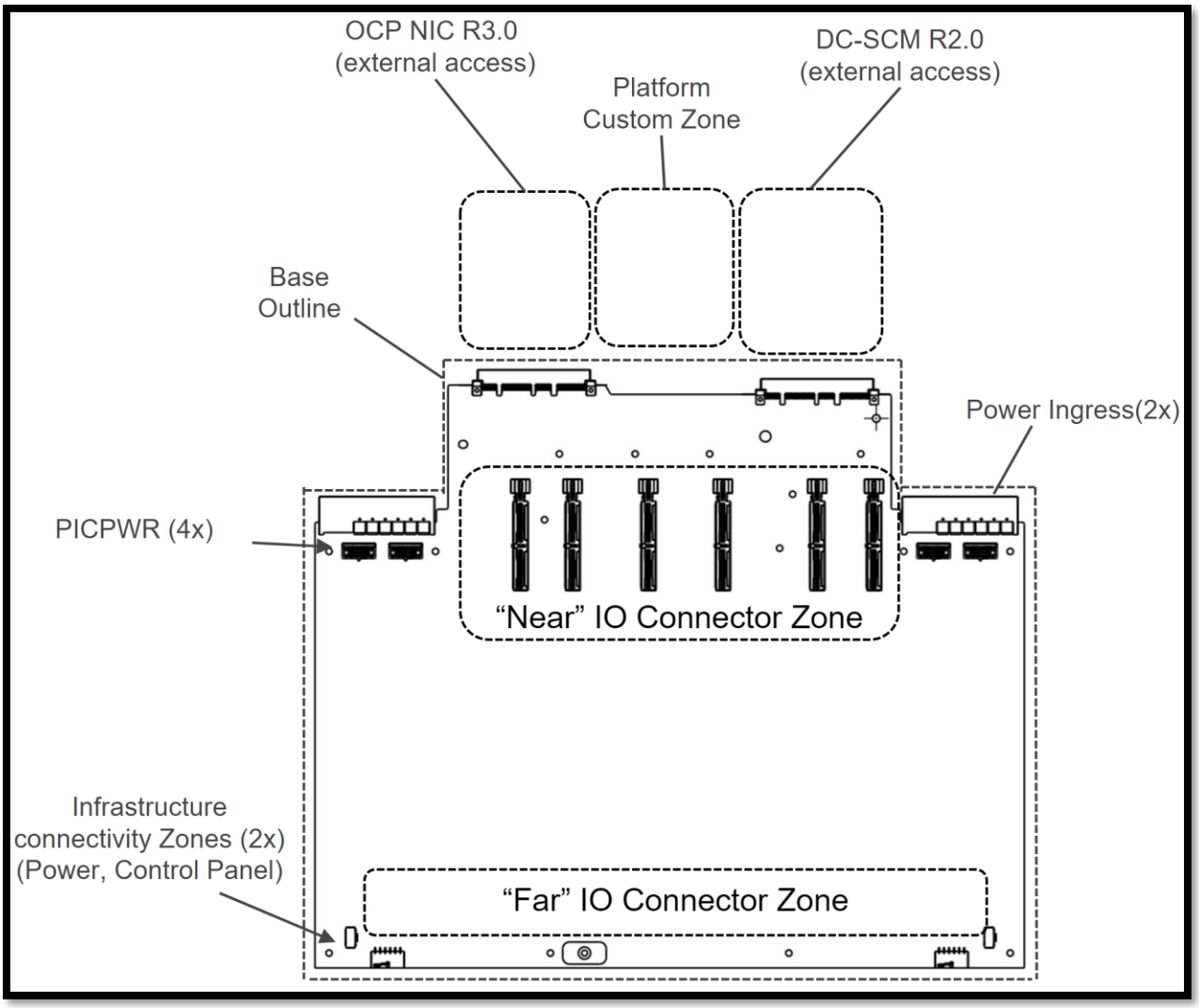
a. 1070mm rack depth
b. All IO generally on cold aisle but may also include some architectures with hot aisle IO. Assuming Front/Near end of system supports IO devices such as PCI CEM, OCP NIC R3.0, SSD's, etc
c. PCIe also distributed at Far end, such as to backplane, OAI – Universal Baseboard, and other items.
d. AC or DC rack power supplied by rack from the hot aisle
e. If PSUs are used, they are not hot serviceable

9. HPM Layout

The following **Figure 1** shows the layout and approximate locations of major subsystems in the Enterprise and Hyperscale M-FLW HPM.

"Near" and "Far" are reference naming conventions to the side of the board and Compute Core, as to orient the reader as to which portion of the board and Compute Core is being referred to. This specification refers to the Near Side as where DC-SCM R2.0 Management subsystem resides as a board peripheral. This is also typically referred to Rear IO location for Enterprise products, in which products are designed with IO in the hot aisle of a rack deployment (air exit). This is also typically referred to Front IO location for Hyperscale products, in which products are designed with IO in the cold aisle of a rack deployment (air inlet).

Figure 1. Full Width HPM Layout Diagram



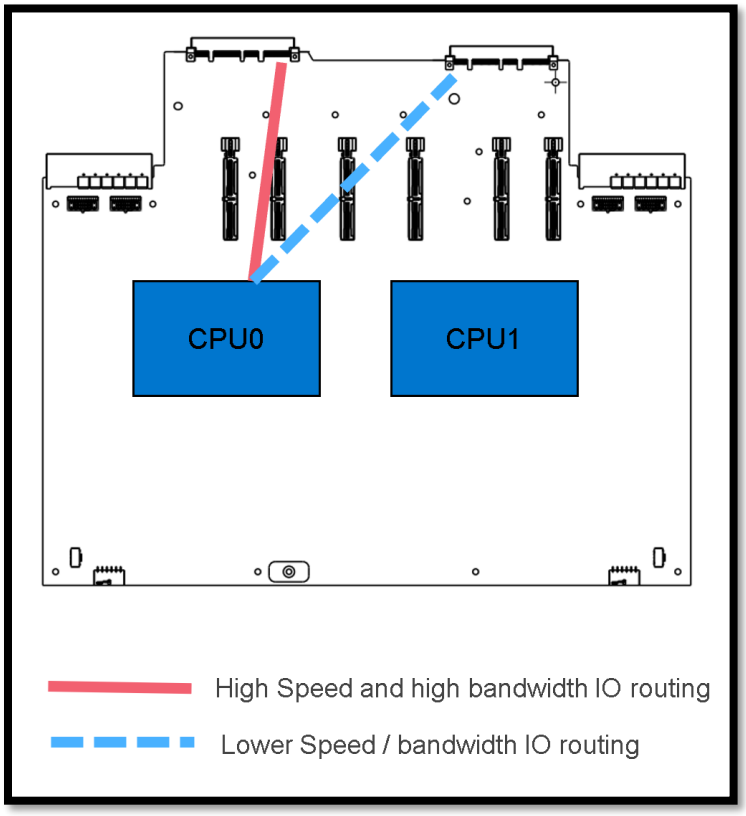
9.1. Two Socket (CPU) Assumptions

The OCP NIC R3.0 subsystem is positioned on the left based on two assumptions:

- In a 2S (CPU) system, the First/Boot CPU in a two CPU HPM is positioned on left.
- OCP NIC R3.0 is directly routed through the motherboard to the first/boot CPU.

The OCP NIC R3.0 is intended to be closer to this boot CPU to best enable the high-speed IO routing. The OCP NIC R3.0 will usually require higher bandwidth routing, and thus should be optimized for material selection and cost impacts. The routing from first/boot CPU to management subsystem (DC-SCM R2.0) has lower bandwidth requirements, and thus should not be the determining factor in board material selections and routing strategy. See **Figure 2**.

Figure 2. First CPU position relative to OCP NIC R3.0 and DC SCM R2.0



In this specification the CPU and Memory locations are intentionally not specified. This is for future flexibility in CPU/Memory quantities, locations, sizes, etc. The board area between DC-SCM R2.0 and OCP NIC R3.0 is designated as a “Platform Custom Zone”, as shown in **Figure 1. Full Width HPM Layout Diagram**. The goal is to provide board area and system volume for individual platforms to provide system specific features.

9.2. One Socket Assumptions

In theory, for a one socket (CPU) platform, the OCP NIC R3.0 location does not have a strong affinity to either side. *The OCP NIC R3.0 shall remain in the specified HPM location for chassis compatibility for all Full Width HPM products.*

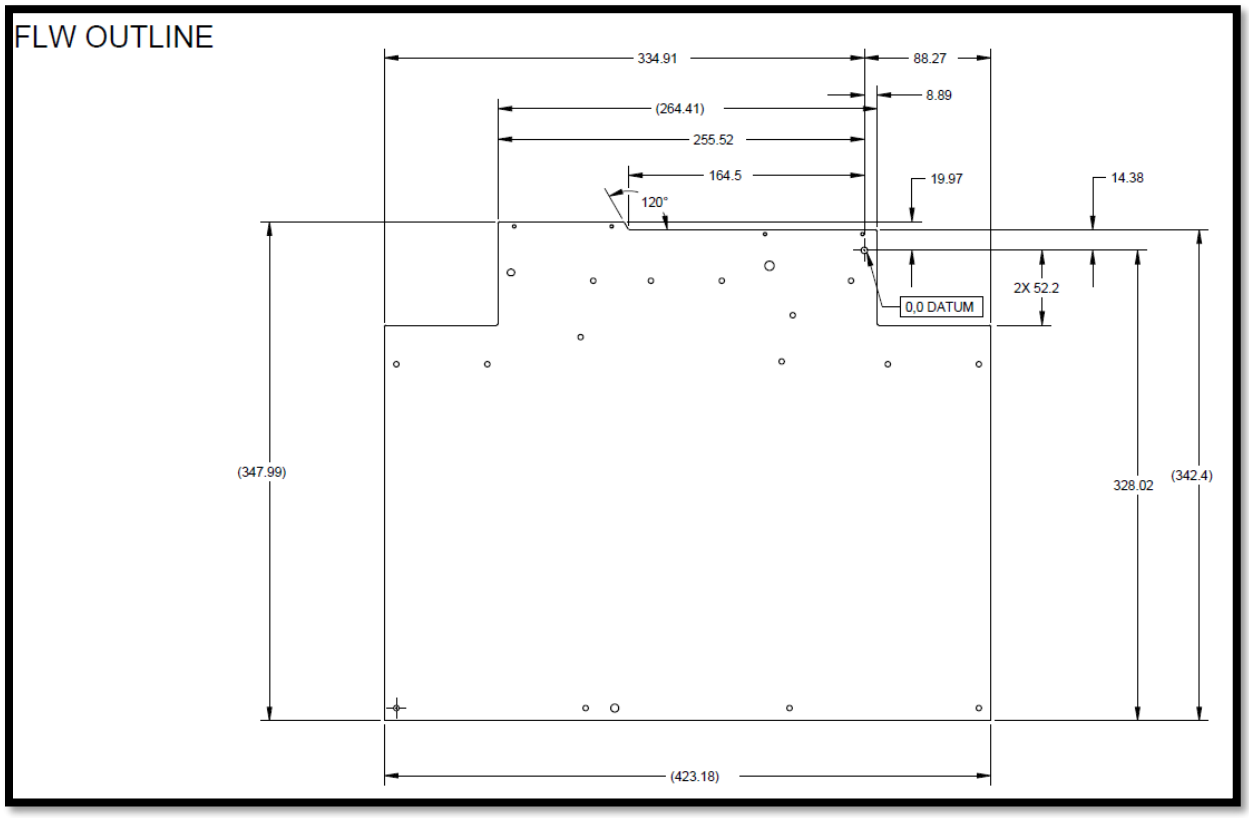
10. Mechanical Requirements

10.1. HPM Outline

*The Full Width HPM (M-FLW) outline is defined in **Figure 3** and shall be followed for a M-FLW Base Specification compliant HPM.* This defines the outline and peripheral locations to fit compute core and IO elements in an FLW compliant chassis. This is intended to fit a wide variety of platform and chassis applications.

The M-FLW HPM Outline is defined in **Figure 3** below. Units are Inches [mm]. The intent is to show overall dimensions of board outline. No tolerances are to be implied. DFX/CAD file link will be in **Section 13.7 CAD files** section and provided in future specification releases.

Figure 3. Full Width HPM Outline

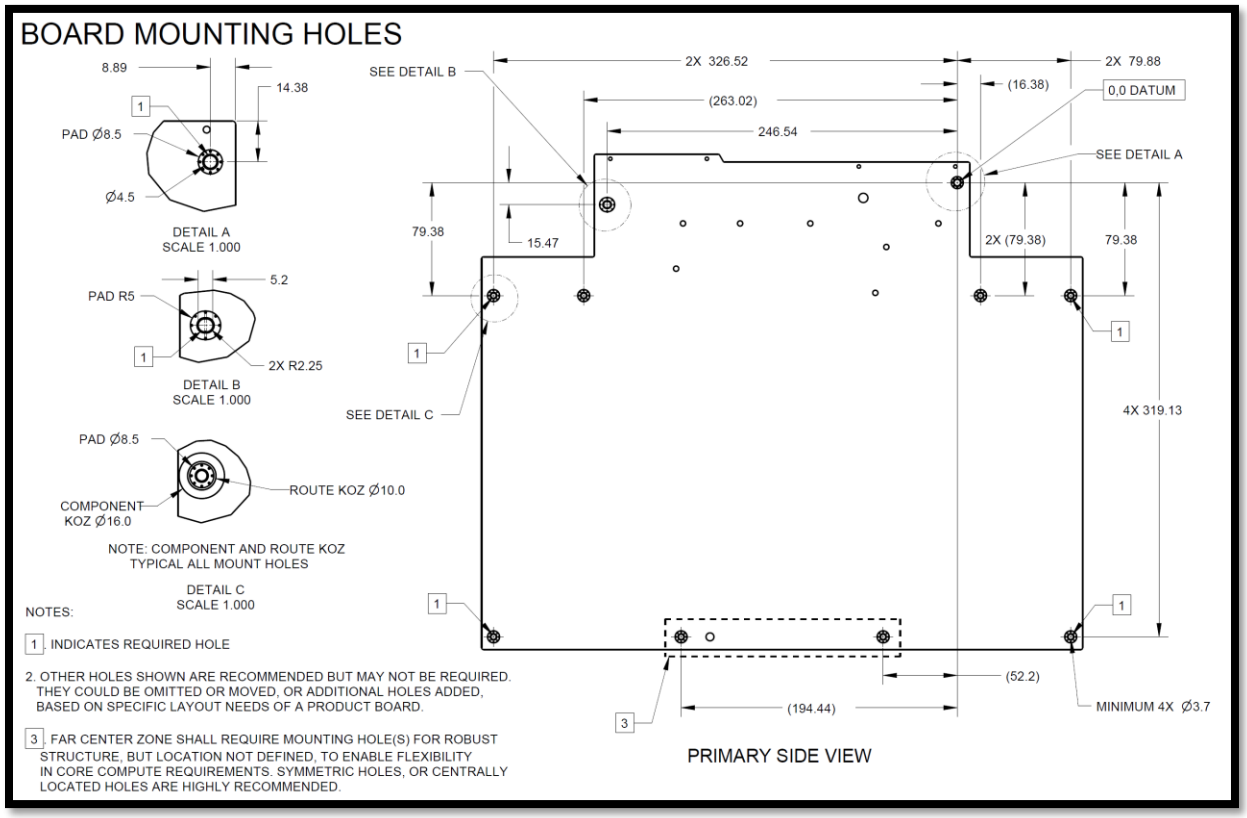


10.2. Board Datum and Mounting holes

*A set of six required board mounting holes specified shall be implemented around the board perimeter per **Figure 4** and represent the minimum mounting hole requirements.* These six boards mounting holes interface to the Chassis-to-Board Bracket (Board Pan). Additional mounting holes are allowed as needed, to ensure appropriate mechanical support of the Compute Core (not shown). These additional board holes are expected to interface to the board-chassis bracketry and should be designed in consideration of the bracket to chassis interface features, as defined in **Section 10.4 HPM to Chassis Retention.** A design should follow good engineering practices and in consideration of Platform Shock and Vibration requirements. Shock and Vibration requirements are not in scope of this specification.

*The mounting holes shall have a pad and component KOZ as defined in **Figure 4***. The component KOZ is intended to keep small components at risk of damage away from the hardware and assembly tools. If a component is larger than 10mm in any dimension, it is considered more robust, and an exception will allow such component to encroach on the Component KOZ's in **Figure 4**.

Figure 4. Board Mounting Holes with Pads and Keepout Zones (Top / Primary side view)

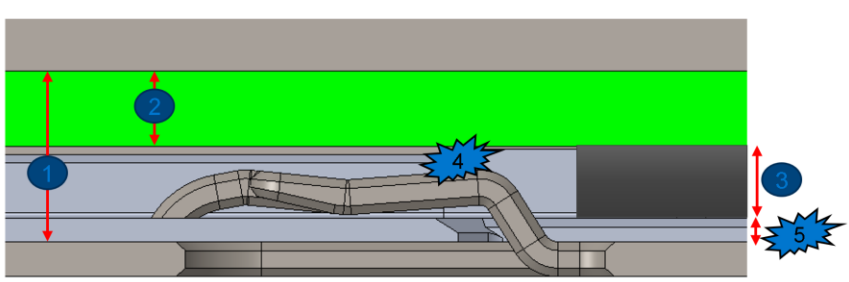


10.3. HPM Board and Assembly Thickness

The maximum board thickness allowed shall be 3.18mm nominal, assuming +10% max tolerance. HPM Thickness choices may have impacts on chassis stackup. HPM thickness must consider the backing plate thickness of a required Core Compute. *HPM designers shall consider that a recommended maximum allowable HPM thickness + backing plate stackup is 5.86mm.* Backing plates are assumed to be allowed to protrude thru cuts in the Chassis-to-Board bracketry.

Figure 5 and **Table 2** below demonstrate example scenarios HPM designers should consider when choosing HPM thickness.

Figure 5. Board and Chassis Stackup Considerations



1. HPM Top Surface Height to Chassis base
2. HPM Thickness
3. Backing Plate Thickness
4. Gap from HPM to Mounting hook
5. Gap to chassis base (may cut thru sub-pan

Table 2. Board and Chassis Stackup Scenarios

(Dimensions in mm)	1 HPM Height	2 HPM Thickness	3 Backplate	5 Gap Backplate to Base Chassis
Typical Nominal Range	5.0 - 5.86	1.57 - 3.18	2.0 – 2.6	
Scenario 1 Nominal	5.2	2.6	2.2	0.4mm
Scenario 2 Nominal	5.86	3.18	2.6	0.08mm
Worst case Gap 5 scenario	5.5	3.5	~2.0mm	0

NOTE: Gap 4 not shown as it depends on customer chassis geometry

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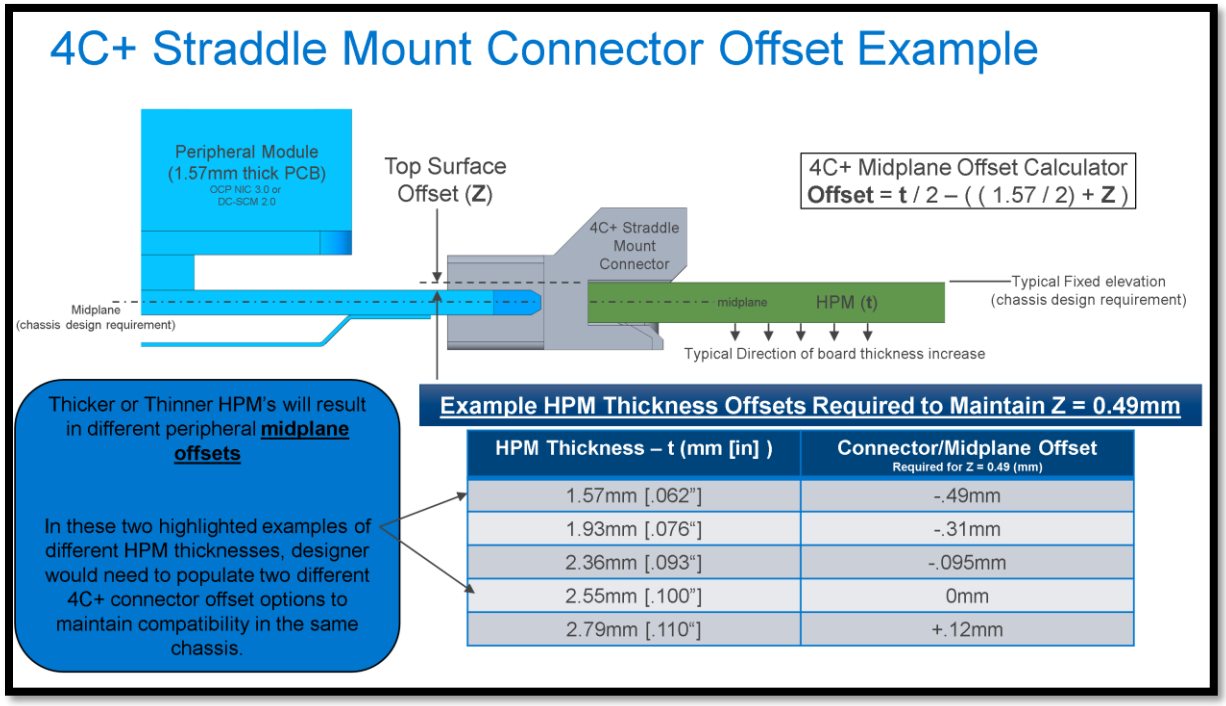
Implementors Note:

Designers should consider that variations in HPM thickness can result in variation of the offset locations of OCP NIC R3.0 and DC-SCM R2.0 peripherals (relative to fixed chassis openings).

A common chassis design intended to support two different thickness HPMs may have to populate different 4C+ connector offsets.

Designers may consult with vendors of SFF-TA-1002 4c+ to determine best options for their chassis application. See **Figure 6. HPM thickness and Straddle Mount Peripheral Offsets** below

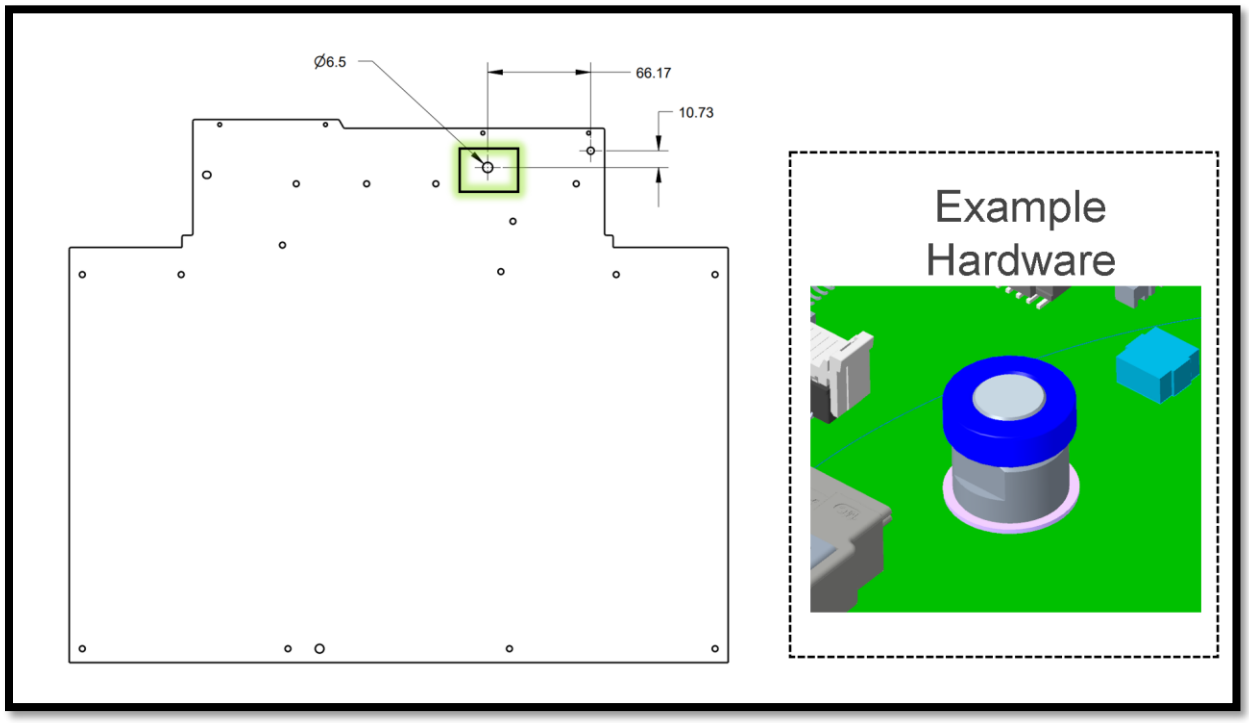
Figure 6. HPM thickness and Straddle Mount Peripheral Offsets



10.4. HPM to Chassis Retention

The HPM and Chassis-to-Board Bracket assembly requires retention to the chassis base. *There shall be a hole required in board to be used for HPM retention to the chassis.* The hole is sized for common retention methods such as plungers, thumbscrews, etc, as shown in **Figure 7** below.

Figure 7. HPM Assembly to Chassis Retention Enablement



10.4.1. Keepout Zone for Retention Hardware

A keepout zone shall be implemented on both topside and bottom side around the Retention Hardware hole.

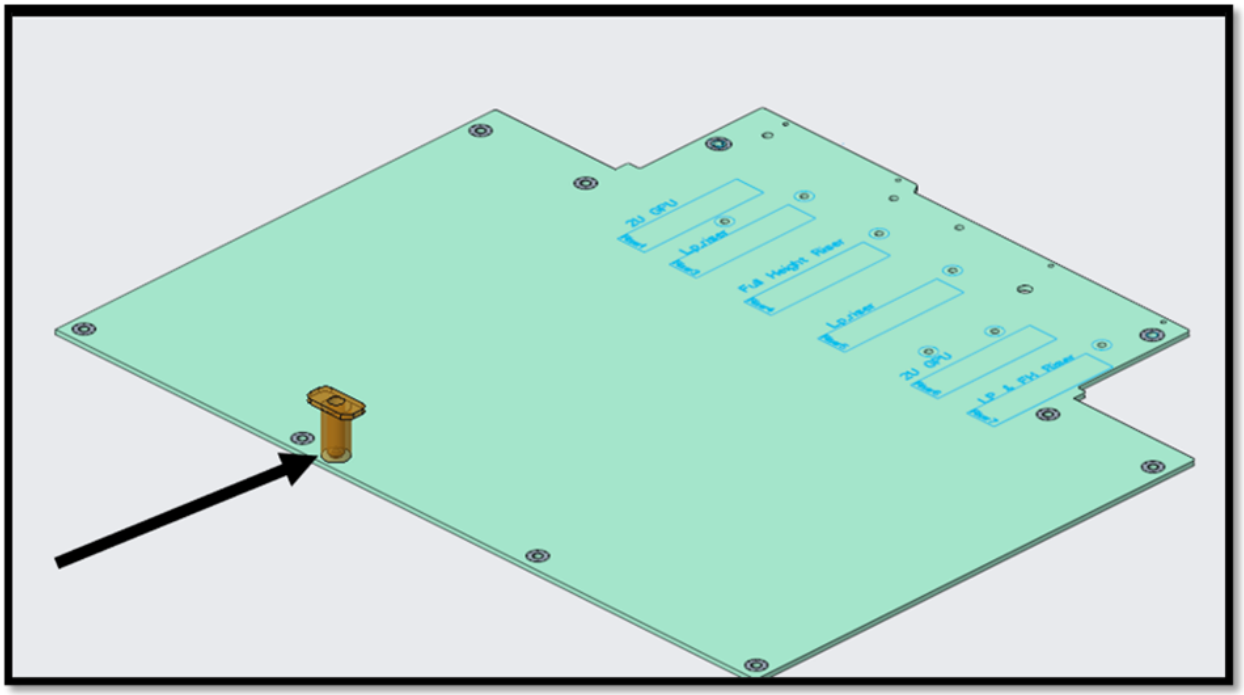
The Primary (or Topside) KOZ is defined in **Figure 19. Zones for Primary Side Component Height Restrictions**.

For Secondary side KOZ, refer to **Figure 21. HPM Secondary Side HPM Zero-Height Keepout Zones**

10.5. HPM Handling

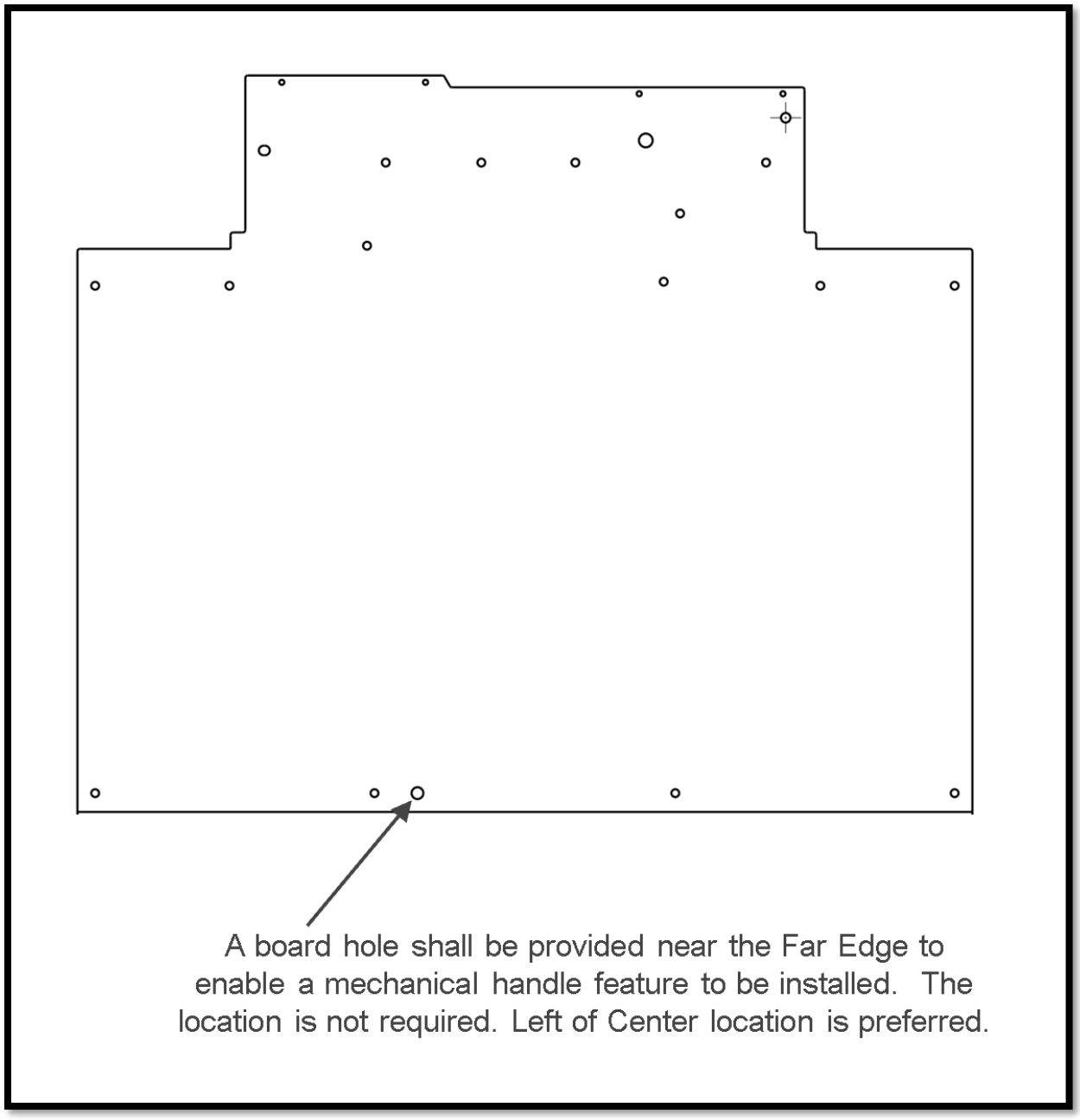
The FLW HPM shall require a hole interface to a mechanical handle. This handle solution may be implemented with but not limited to a plastic handle. An example is shown in **Figure 8.**

Figure 8. HPM Handling Feature



A HPM hole example is shown in **Figure 9**. *The hole location for this handle shall be provided near the Far Side edge of the Compute Core in the HPM.* The handle may utilize an existing Far side hole, except for the corners. The location of the hole on the Far side is not specified but should be placed considering Compute Core details, such as Far High-Speed IO cabling, and Thermal solution keepout. To balance handling of board with chassis retention feature (near DC-SCM R2.0), it is preferred to place the handle feature to left half of the HPM.

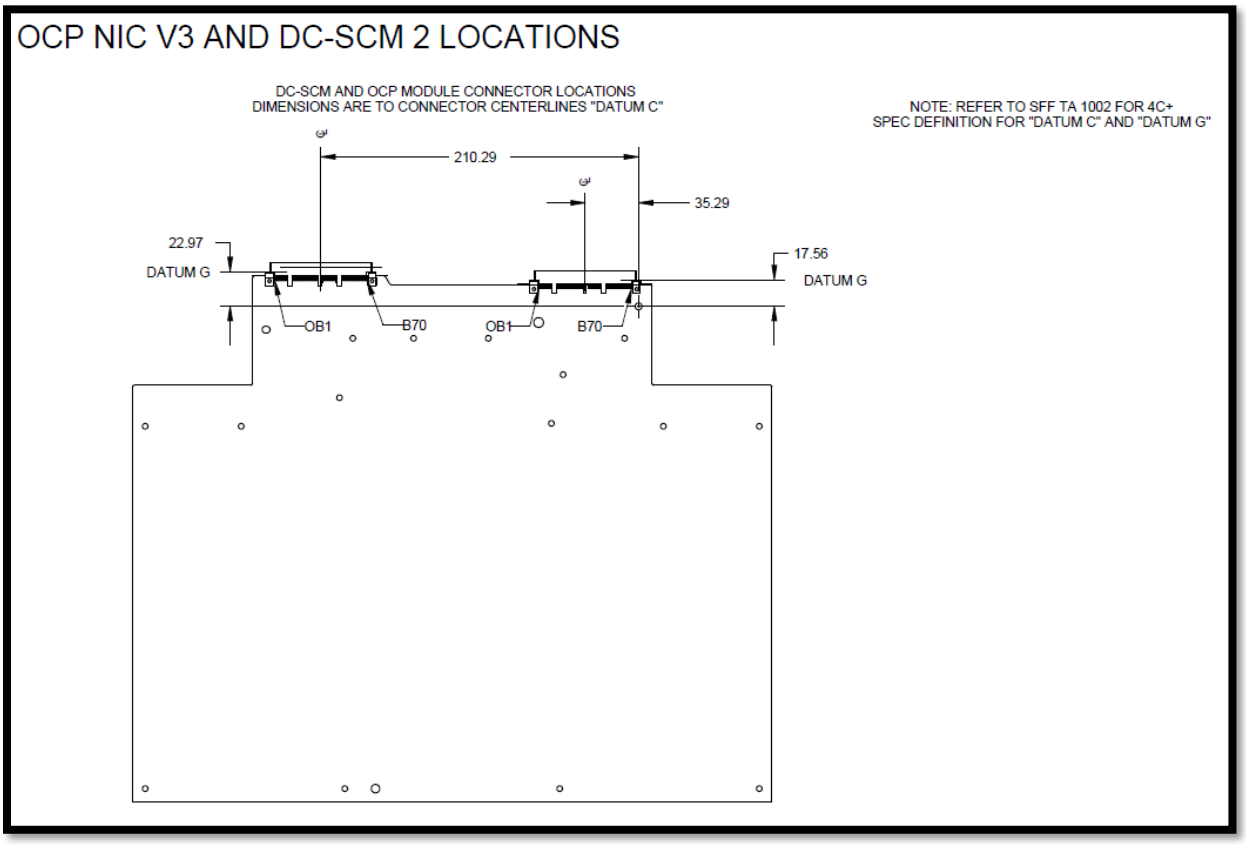
Figure 9. HPM Handling Feature Location



10.6. OCP NIC R3 and DC-SCM R2 at Near Edge Locations

The HPM Shall place the OCP NIC R3 and DC-SCM R2 at the locations defined by the centerline location of each of the connector subsystems in ***Figure 10****.* For further details of how the connector centerlines are defined, refer to SFF-TA-1002 specification.

Figure 10. Centerline Locations of OCP NIC R3.0 and DC-SCM R2.0



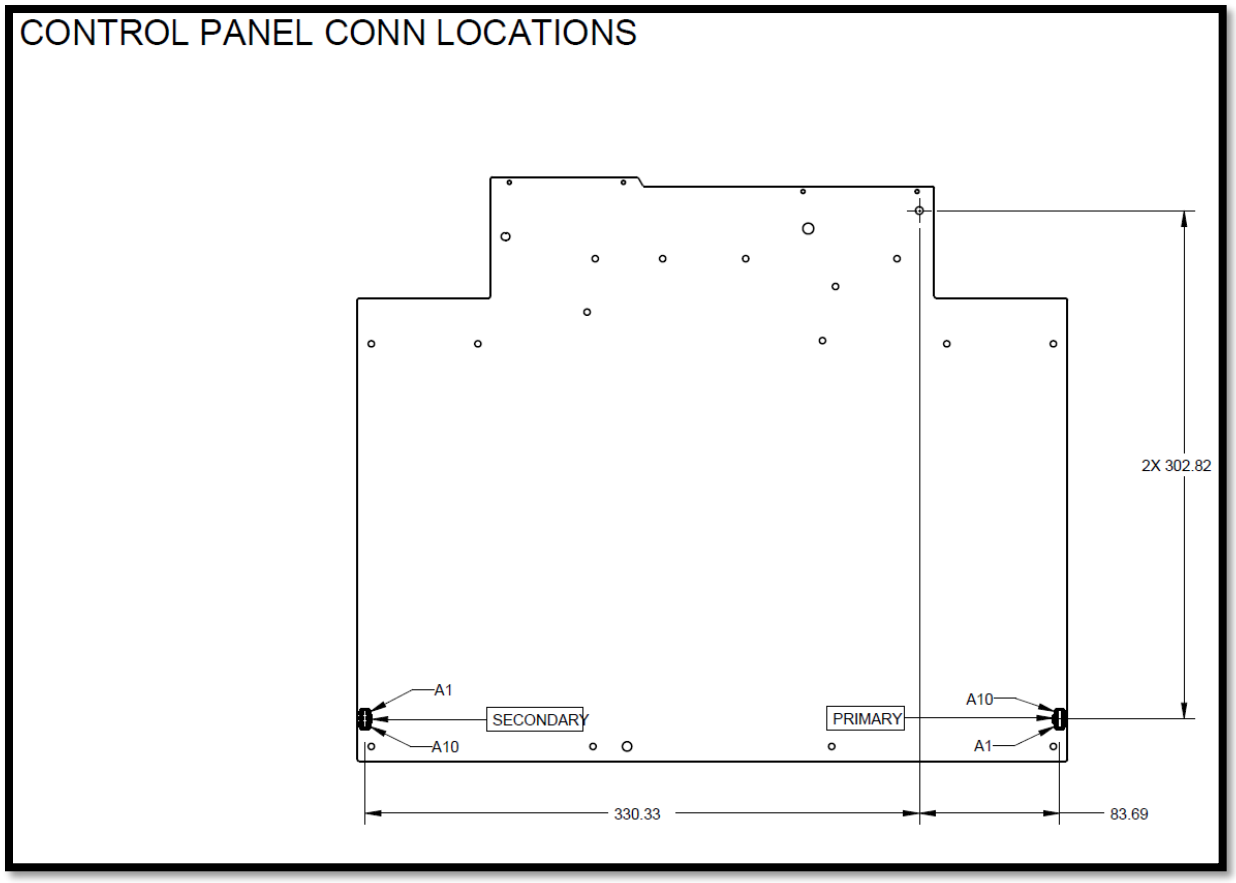
Note: M-FLW workgroup is currently investigating changes to the DC-SCM position of 35.29mm due to the M-CRPS bay sheetmetal and the DC-SCM rails. This will be closed in the next update.

10.7. Control Panel Connector Locations

505 *The HPM shall implement two instances of the M-PIC defined Control Panel connections as shown in **Figure 11.*** The Control Panel Connector details are further defined in M-PIC Section Reference: : “Control Panel Interfacing”.

Figure 11. Control Panel Connection Locations

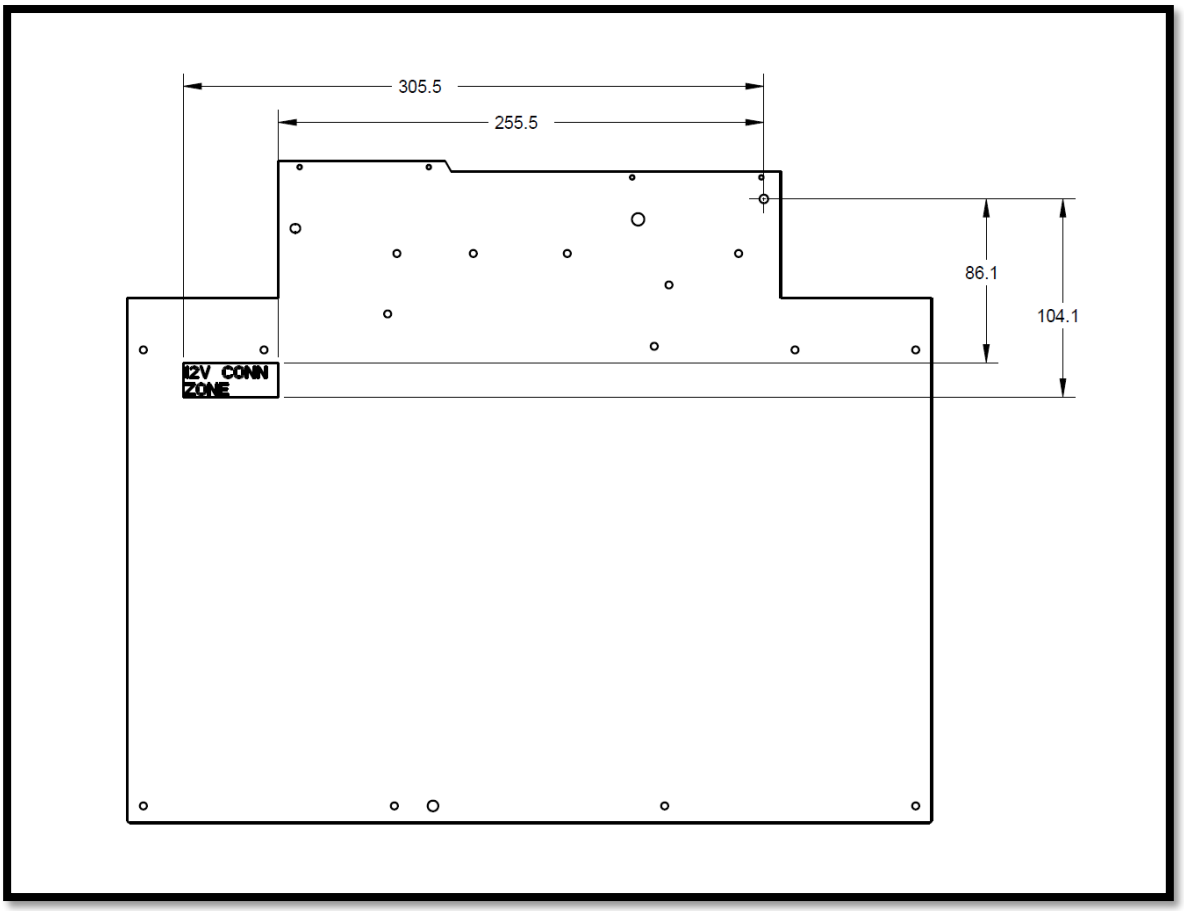
510



10.8. Zone for PDB Management Connector Header

The HPM shall implement a PDB Management Connector Header. The connector must be placed in the HPM within the zone defined in defined by **Figure 13** (but can be depopulated in assembly BOM at a Design Specification level guidance). The PDB Management Connector details are further defined in M-PIC Section Reference: “PDB Management Connector Header”.

Figure 12. PDB Management Connector Header Location

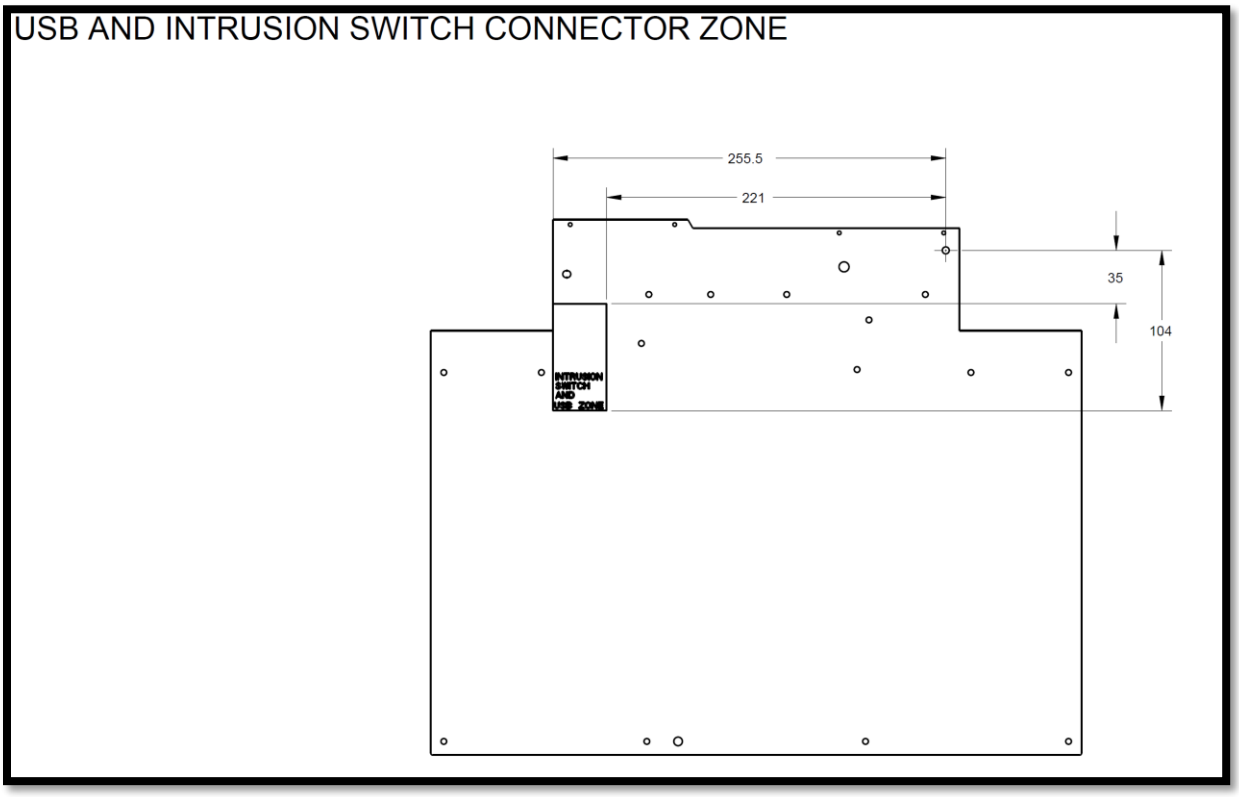


10.9. Zone for Intrusion Switch and Internal USB Connection

The HPM shall implement an internal USB3 connector. The connector must be placed in the HPM within the zone defined in defined by **Figure 13**. The USB Connector details are further defined in M-PIC Section Reference: “Internal Host USB3 Connector”.

The HPM shall implement an intrusion switch connector. The connector must be placed in the HPM within the zone defined in defined by **Figure 13**. The Intrusion Switch details are further defined in M-PIC Section Reference: “Intrusion Switch”.

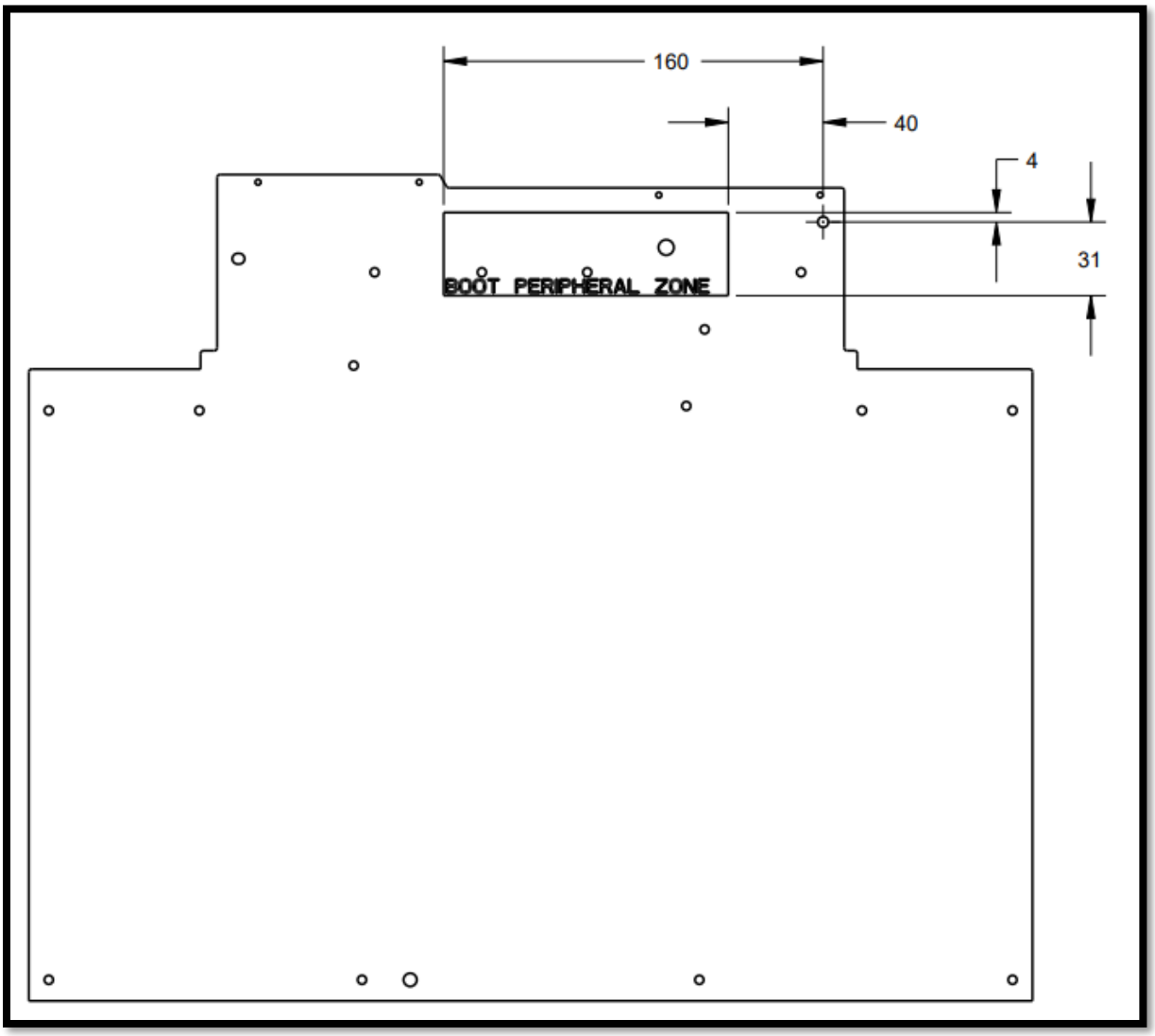
Figure 13. USB Connection Placement Zone



10.10. Boot Storage Peripheral Connection

The HPM is recommended to implement a Boot Storage Peripheral connector. The connector must be placed in the HPM within the zone defined by **Figure 14**. The Boot Storage Peripheral Connector details are further defined in M-PIC Section Reference: “Boot Storage Peripheral”.

Figure 14. Placement Zone for Boot Peripheral Connector



Note: M-FLW workgroup is currently investigating changes to the boot peripheral zone. This will be closed in the next update.

10.11. Near Side IO Connectors

The HPM definition includes High-Speed M-XIO connectors that are intended to be used for IO Riser subsystems or cabled High-Speed IO.

The following set of requirements and recommendations enable these benefits:

1. Blind mating and docking of riser cards
2. Chassis, Riser, or other IO mechanical subsystem reuse between generations of HPMs.
3. Future larger Compute Cores
4. Ability to cable High-Speed IO from these connectors, as an alternative to mechanical subsystems.

10.11.1. Choice of Near Side M-XIO Connectors

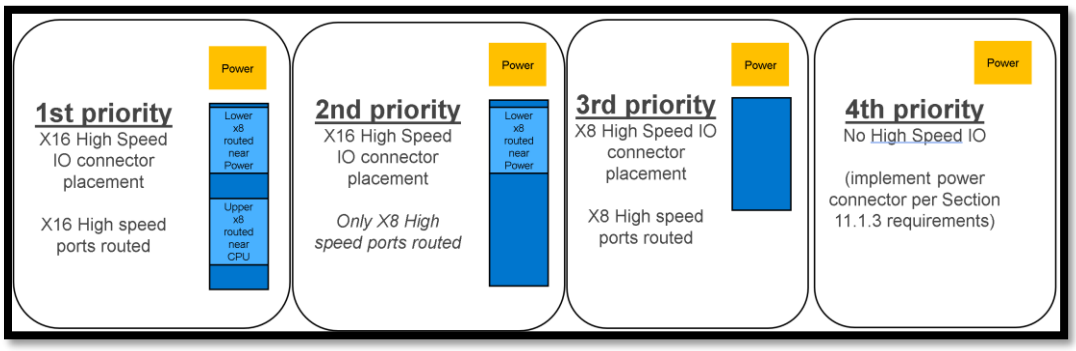
HSIO connector selections are strongly recommended but not required for compliance. Use of the recommended HSIO connectors will ensure broader compatibility with chassis, risers, and cable interfaces in the future. The selection is intentionally not stated as “required” so the specification allows for future selection of new connector technologies as may be required by IO speeds and bandwidth changes in future generations of HPM. Requirement: Connector Choices must be compliant M-XIO specification

	Recommended Connector	**Note**
Near Side	Amphenol G03V213X2HR	Appropriate for both cable and riser usage
Far Side	SFF-TA-1026	Appropriate due to low profile and ability to fit under thermal solutions

10.11.2. Population of Near Side M-XIO Connectors

Connector population and routing guidance is provided for HPM designers to help maximize subsystem reuse and compatibility across HPMs. For HPMs with less than 6x16 ports available for Near Side IO, HPM Designers may choose to populate fewer M-XIO connector segments.

Figure 15. Near Side IO connector Population Guidance with less than 6x16 ports



For an example scenario following this guidance, see **Figure 40. Example Near IO Connector Population Scenario** in the Supplemental Information section.

If a HPM contains more Near Side IO ports than the 6x required connectors, additional connectors may be placed in the Near Side IO area at discretion of the designer. Considerations should be made to ensure additional connectors can be accessed and cabled to the Far Side direction.

BOM Population Note:

Custom BOM population choices are made at the discretion of a customer and are not covered by this specification. (This includes any depopulation choices for cost savings.)

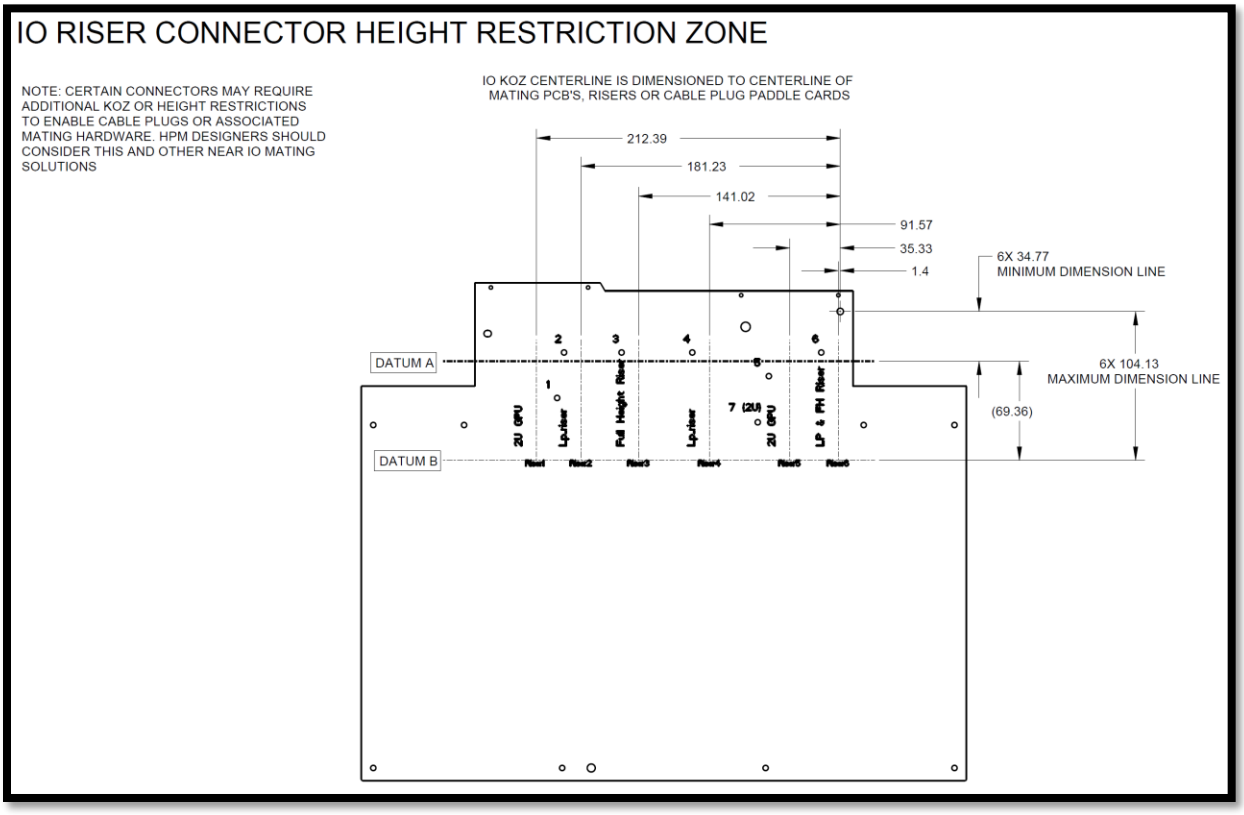
10.11.3. Location of Near Side M-XIO Connectors

1. *An HPM shall implement the 6x Near Side IO Riser-Cable connectors within the Near Side IO locations, defined in* ***Figure 16. Near Side IO Riser-Cable Connector Centerline and Position Limits.***

2. *The X dimension PCB Riser centerlines in* ***Figure 16. Near Side IO Riser-Cable Connector Centerline and Position Limits*** *shall be followed for specification compliance.* The X dimension on PCB Riser centerlines is fixed and cannot be changed.
    - This methodology ensures compatibility with assumed Typical PCIe Add-in-Card configurations, as well as future Compute Core fit within the M-FLW outline.
    a. These positions enable fixed riser positions, but a Platform Provider is not obligated to use fixed risers.
    b. Typical configuration assumptions and background information on these location choice requirements are detailed in **Section 13.2 1U and 2U PCIe Slot Typical Configurations**
    c. It is recommended that Near Side IO connectors with integrated power should be oriented with power bay closest to the Near Side edge and High-Speed IO closest to Far Side edge (near the Compute Core).
3. If a chosen connector centerline is offset from the PCB Riser card centerline, the designer must ensure connector location enables the PCB Riser centerlines.
4. An HPM design may enable a higher bandwidth connector choice than the recommended connectors x16 capability. (Example a x32 connector). These connector choices and placement must comply with the requirements in **Figure 16. Near Side IO Riser-Cable Connector Centerline and Position Limits**
5. The Y-location of the Near Side IO connectors shall be located between the Datum A and Datum B defined in **Figure 16. Near Side IO Riser-Cable Connector Centerline and Position Limits**. The Datum A and B (Y-direction) limits will enable future compatibility to 1U PCIe Add-in Cards and allow HPM layout room for future compute cores. Connector choice and Y-dimension attributes are left flexible in the spec to enable future technology

advances in IO (speed, bandwidth) to be supported with connector technology improvements and offerings.

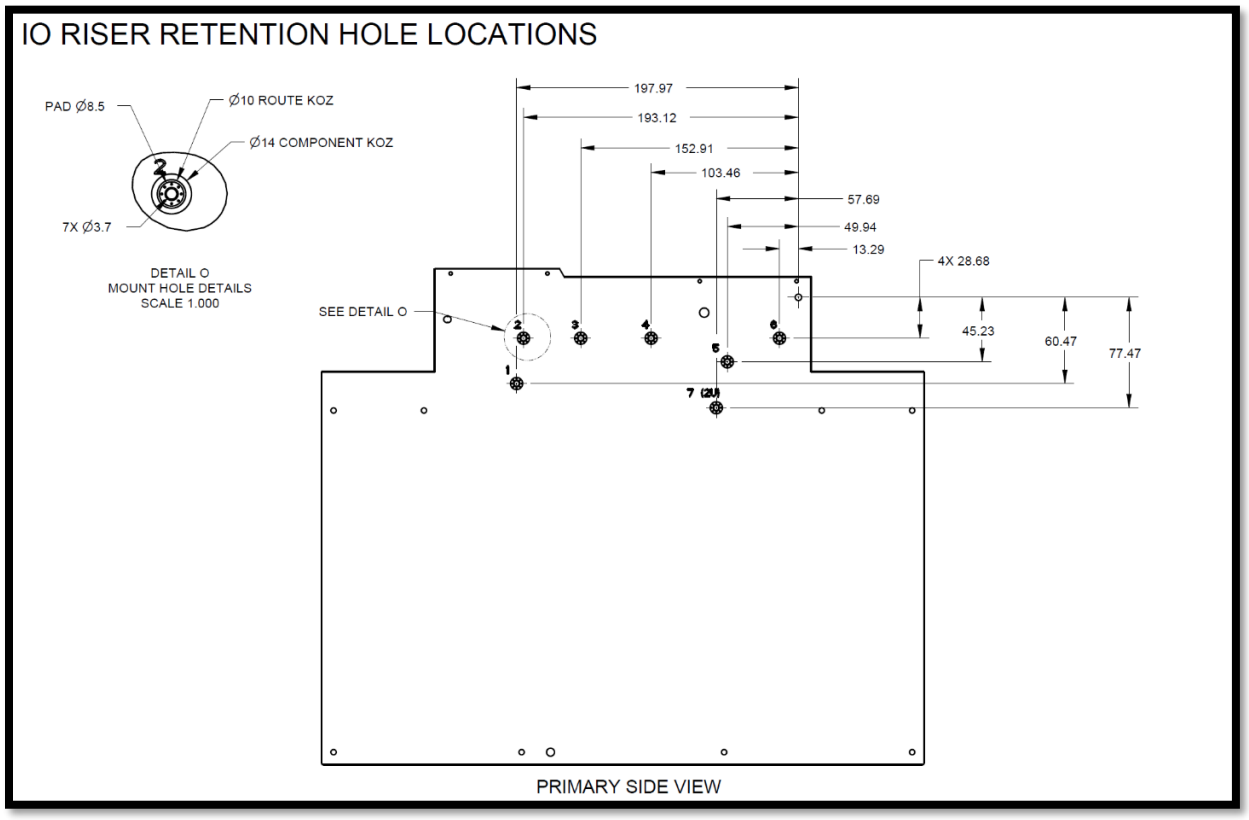
Figure 16. Near Side IO Riser-Cable Connector Centerline and Position Limits



10.11.4. Mounting Hole Requirements for Near Side Riser Retention

The HPM shall implement all mounting holes associated with each Near Side Riser location, as defined in ***Figure 17. 1U and 2U Near Side Riser Retention Enablement Holes***. These are intended to be used for mechanical module retention (such as PCIe Risers, or other modules that require mechanical retention in the HPM area). There is a total of 7x holes associated with the 6x IO connectors. These mounting holes are associated with both 1U and 2U PCIe Riser configurations. The riser retention holes are defined as a 3.7mm diameter hole, as shown in **Figure 17. 1U and 2U Near Side Riser Retention Enablement Holes**, along with associated pads and component KOZ. Chassis Designers may choose the hardware and utilization method for riser retention.

Figure 17. 1U and 2U Near Side Riser Retention Enablement Holes



635 For further explanation on which mounting holes are associated with its Near IO connectors, see **Figure 41. Riser Retention Holes and Associated Near XIO Locations** in the Supplemental Information section.

10.11.5. Summary of Near Side Connector Requirements

640 Fixed vs flexible choices in Near Side IO are summarized in **Table 3**

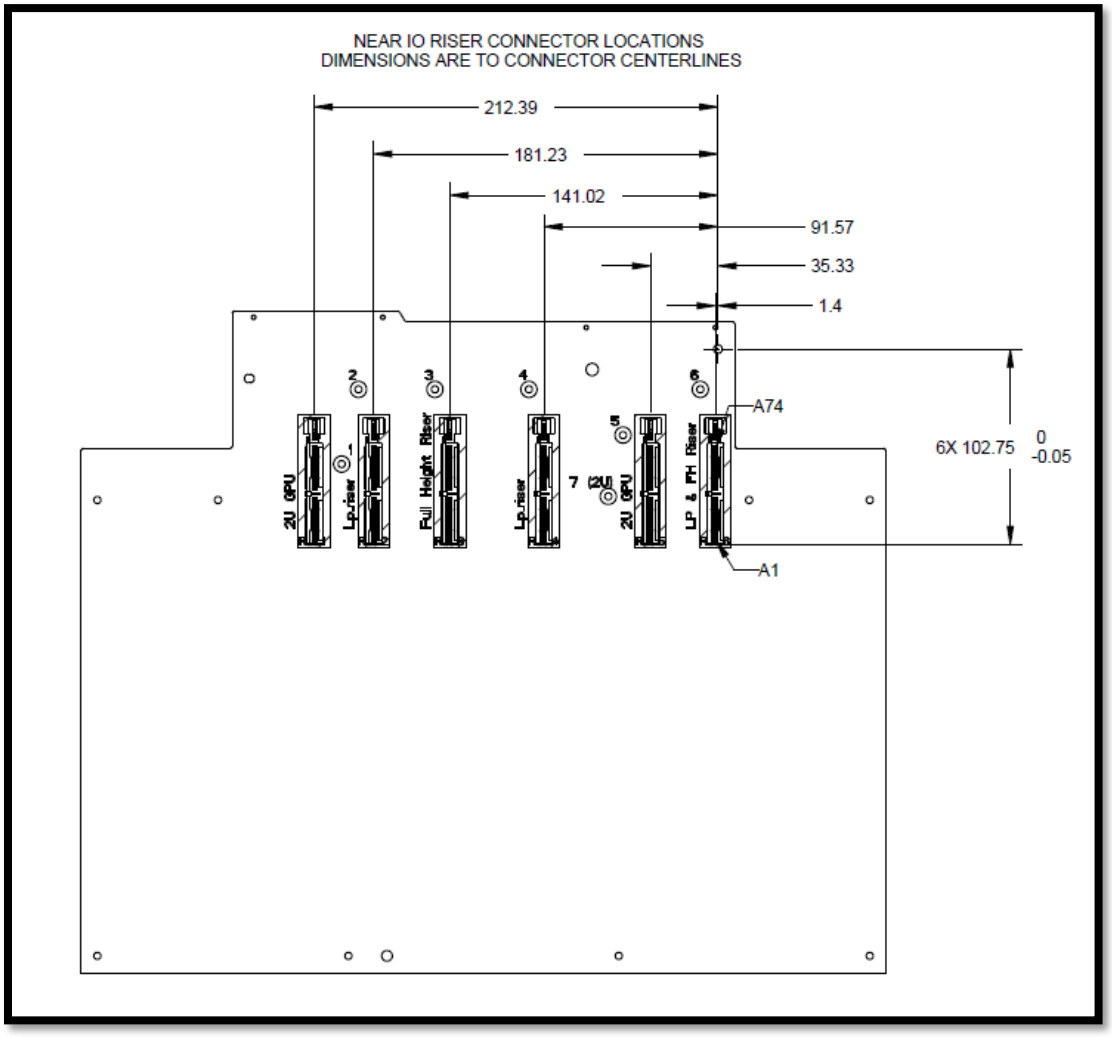
Table 3. Near Side IO Attribute Requirements

Item	Fixed	Flexible Choice
Connector Choice		X
X-dimension location	X	
Y-dimension location		X
Retention hole X-Y location	X	
Additional IO connector locations		X

10.11.6. Recommended Near Side IO Connector Selection and Placement

It is recommended that HPMs use Amphenol G03V213X2HR (or equiv). *When the recommended Near Side IO connector is used, the required placement is shown in* ***Figure 18***.

Figure 18. Reference Locations of Recommended Near Side IOs



10.12. Far Side IO Connector Placement

The Far Side IO connector locations referenced in **Figure 1. Full Width HPM Layout Diagram** are not specified because they are all assumed to be cable-only connections and will not have major dependencies to chassis or subsystem reuse compatibility.

10.13. Primary Side Component Height Restriction Zones

*A Component Height Restriction Zone shall be required, per **Figure 19. Zones for Primary Side Component Height Restrictions** which applies to all soldered components, including mated connectors with the exception of DIMM sockets or special exceptions specified per zone.*

The purpose for these height restrictions is to enable:

1. Thermal solutions to interface to Compute Core items such as CPU and DIMMs (not shown). Thermal solutions in scope include extended air heatsinks and liquid cooling solutions.
2. Cable routing channels along HPM edges
3. PCIe CEM cards on 1U risers

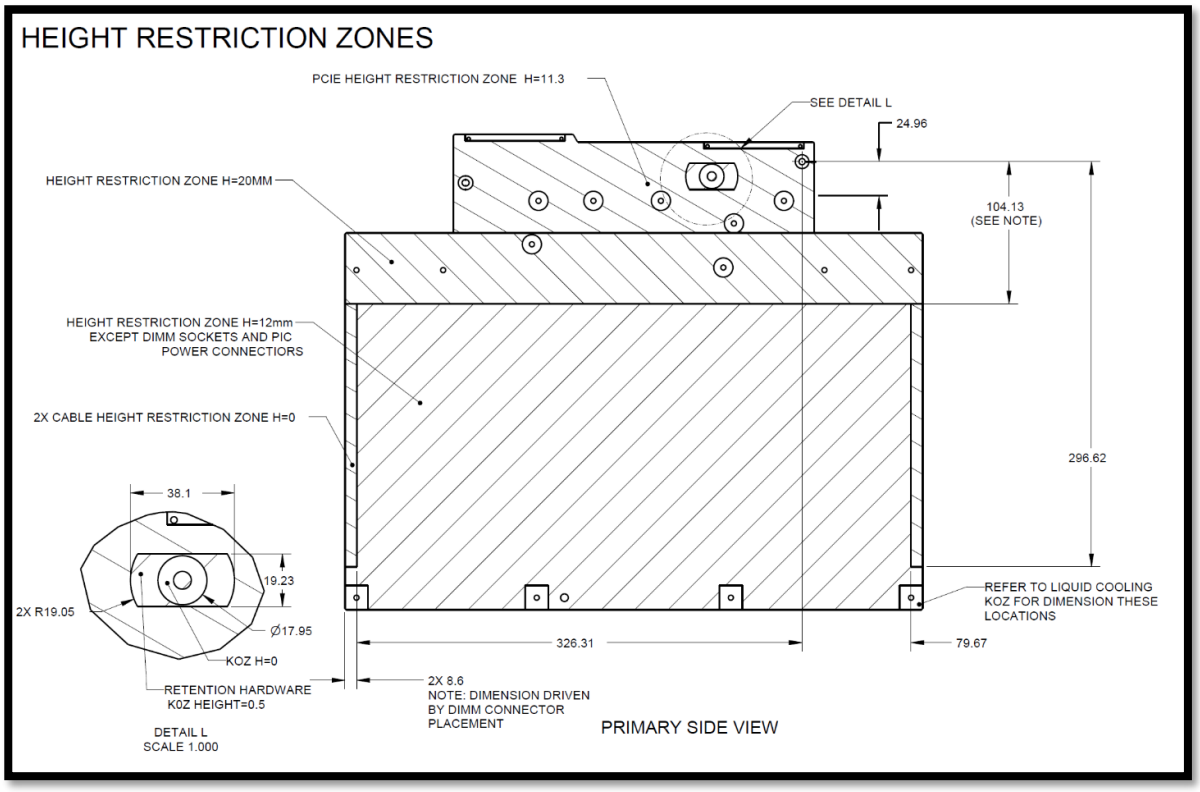
For thermal solutions, one must consider the allowable variance in numbers, types, and location of Compute Core items. Thus, a fixed 12mm for component height restriction in the Compute Core area is intended to allow air cooling heatsinks or liquid cooling hardware of any variance. DIMM sockets are exempt from the 12mm component height restriction. All other soldered board components must comply with exceptions noted in **Figure 19. Zones for Primary Side Component Height Restrictions**

If a cable connection (power, High speed IO, etc) is placed in the component height restriction zone, the max height restriction shall apply to the mated height of the plug and cable assembly.

Implementors Note on SFF-TA -1016 Connectors

SFF-TA-1016 Connectors have mated height options above and below 12mm. System Designers should take these options into account with respect to the height restriction zones, if selecting SFF-TA-1016 connectors for an HPM.

Figure 19. Zones for Primary Side Component Height Restrictions



Implementation Note:

The Height Restriction Zones defined in **Figure 19. Zones for Primary Side Component Height Restrictions** apply specifically to soldered circuit board components, mated connector heights or other mated assemblies of solder components. This does NOT apply to heatsinks of any kind, shrouds or other mechanical parts that are added to the board at a later integration stage.

It is assumed that items such as CPU heatsinks, VR heatsinks, and shrouds are all designed by System Designers. And thus, the height and location tradeoff between these items are assumed responsibilities of the System Designer and not the HPM designer. The HPM Designer should consider best practices when making component placement choices. This makes no assumptions on the compatibility of Chassis, Peripherals or Thermal solutions. For future chassis and HPM compatibility, a System Designer is advised NOT design elements that intersect with the Height Restriction zone (Fans, Heatsinks, Risers, etc).

10.14. Secondary Side KOZ and Height Restrictions

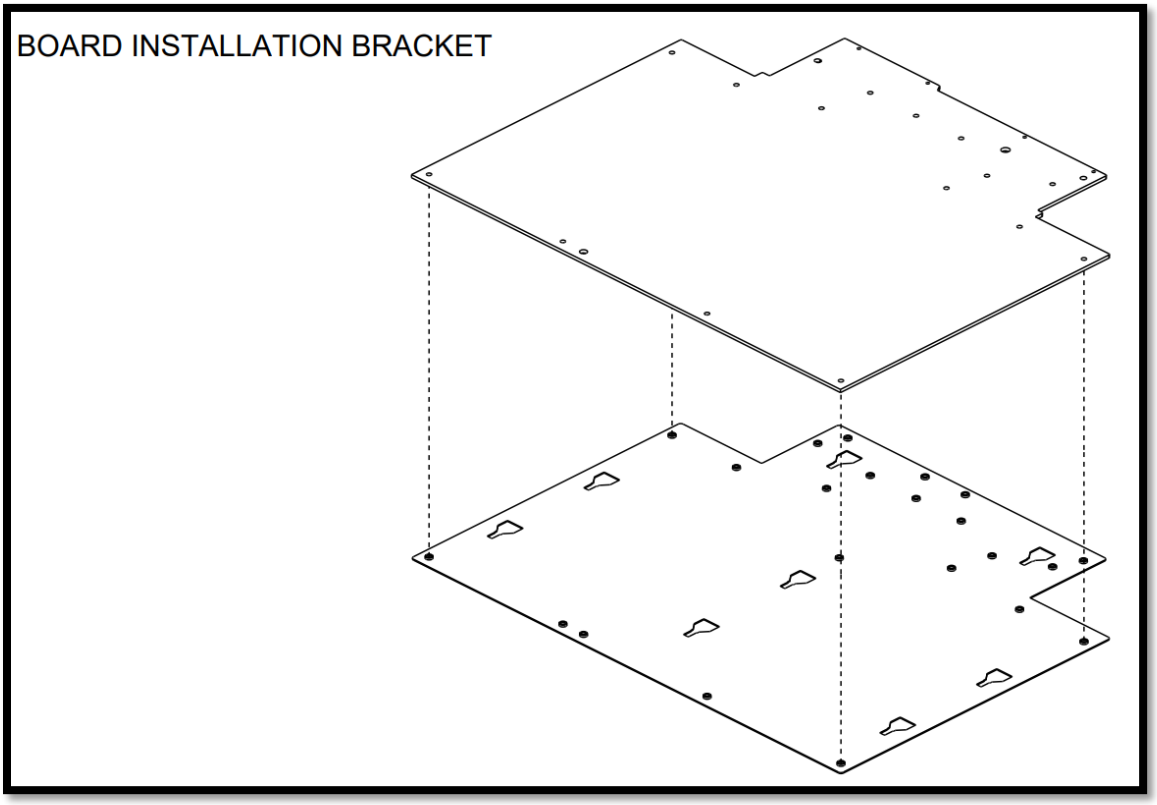
10.14.1. Overall Secondary side Keep-in-Zone Requirements

The back side or secondary side of the HPM shall have a universal height restriction of 1.6 mm, unless otherwise specified in the areas of 0 height zones. This is to ensure clearance to chassis componentry. This is especially important with a max allowable board thickness defined in **Section 10.3 HPM Board and Assembly Thickness.**

10.14.2. Chassis-to-HPM Bracket (Board Pan) Requirements, and KOZs.

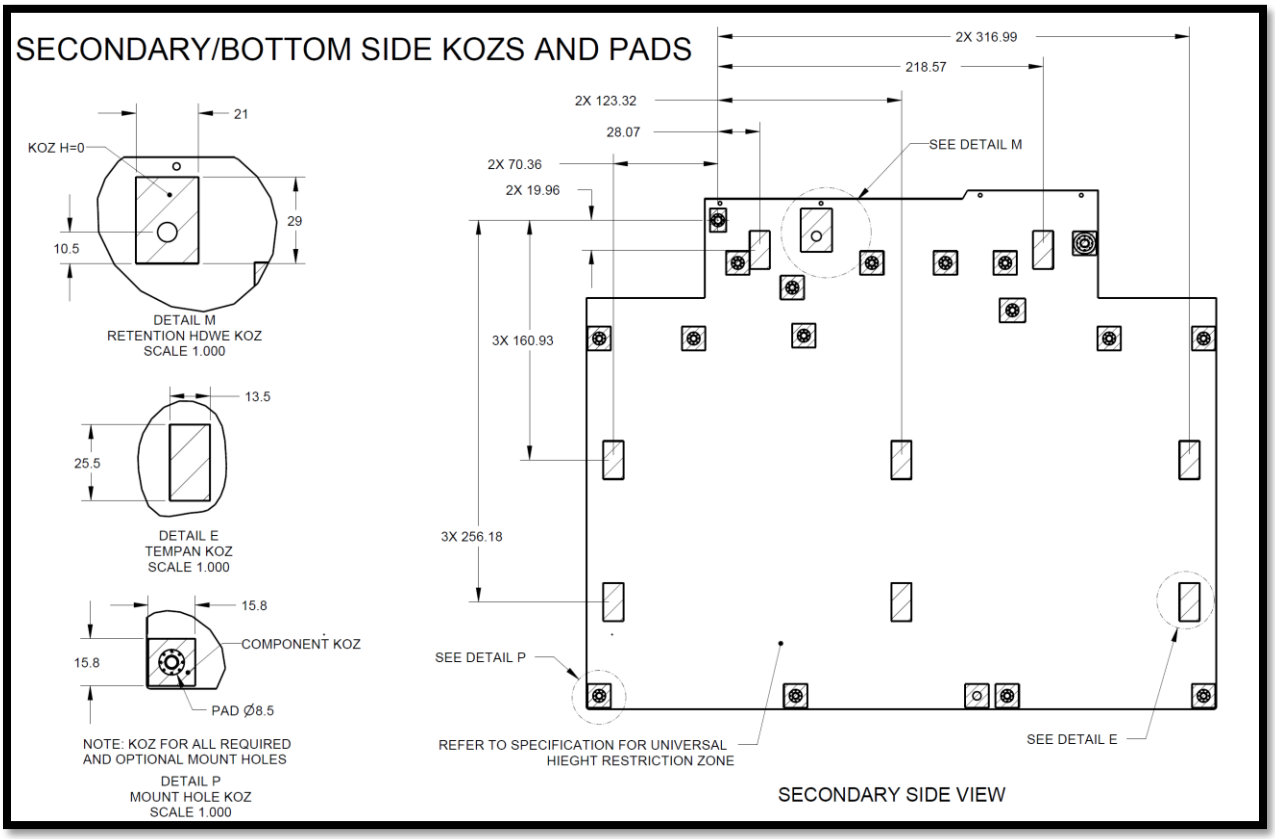
The M-FLW HPM shall be designed to fit a Chassis-to-HPM Bracket (Board Pan) that enables different board layouts and mounting hole locations between different Compute Core designs while still maintaining compatibility to a common chassis design. See **Figure 20**

Figure 20. Example of Chassis-to-HPM Bracket (Board Pan)



On the HPM, there will be required locations for chassis hook features that interface between chassis base and the Chassis-to-HPM Bracket. These hook locations require HPM secondary side (bottom side) zero-height keepout zones, as specified in ***Figure 21***

Figure 21. HPM Secondary Side HPM Zero-Height Keepout Zones



The Keepout Zones defined in Detail E of **Figure 21** are to allow chassis base hook geometry to interface the cutouts on the chassis to HPM bracket. See example in **Figure 43. Chassis Base Geometry to Interface Chassis-to-Board Bracketry**. The geometry of the HPM bracket is not specified and is a design choice for System Designer.

10.14.3. Secondary Side Tall Component Exceptions

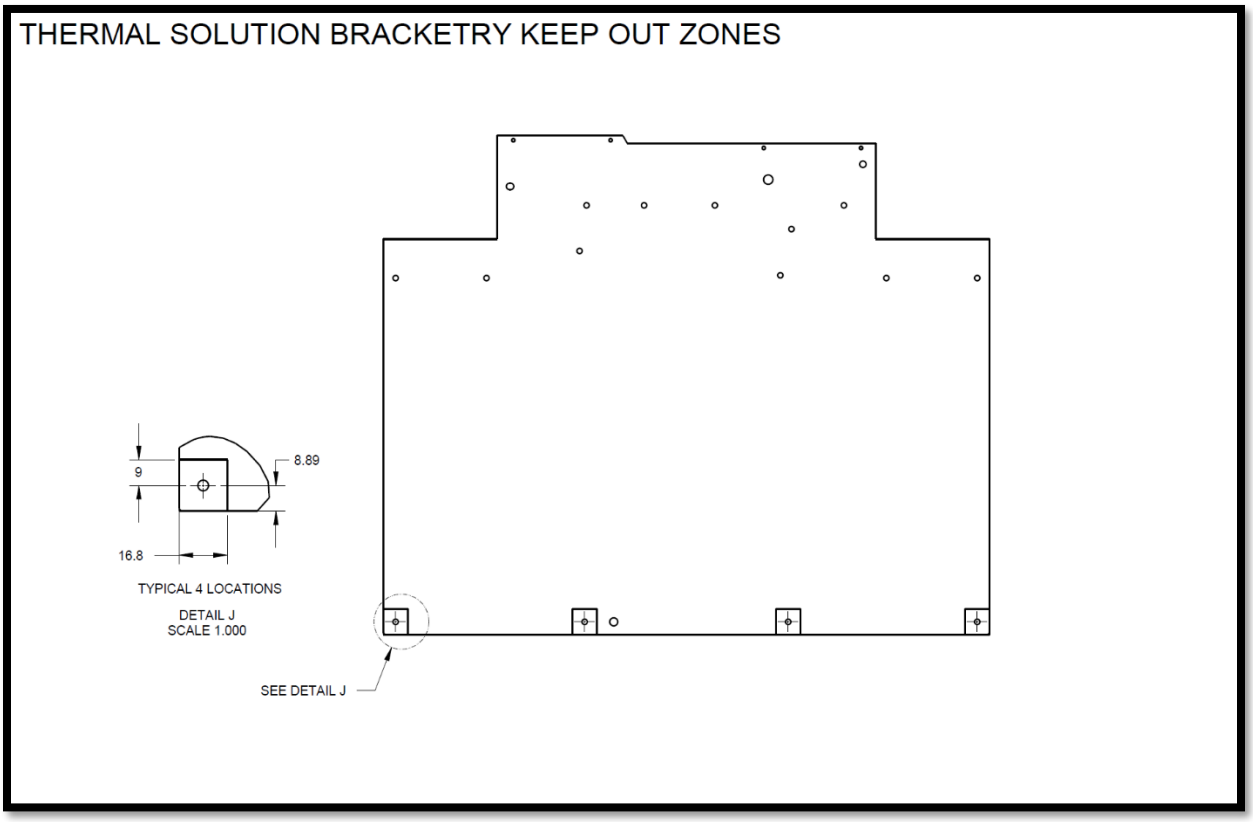
In some instances, an HPM Designer or System Designer, may desire tall secondary side components (such as special capacitors) that exceed the secondary side height restriction. Although this should be avoided, a HPM Designer may implement local exceptions if the following conditions can be met:

1) Exceptions are contained to small areas of the secondary side, not to exceed 400mm^2 area per instance.
2) No two instances of exception are closer than 10mm, as to not drive excess cutouts in Chassis-to-HPM bracketry
3) The Chassis-to-HPM bracketry can be cutout to accommodate these exceptions.
4) The HPM thickness + backside component shall not exceed 5.86mm

10.15. Thermal Solution Bracketry Keepout Zones

There shall be keepouts around the Far Side HPM mounting holes to enable bracket mounting to the HPM, as detailed in ***Figure 22***. These brackets may be needed for systems that wish to mount liquid cooling components, such as DIMM liquid manifolds, or large radiator assemblies.

Figure 22. Thermal Solution Bracket Keepouts



10.16. Cabling Enablement Keepout Zones

There shall be a keepout zone to left and right of outermost DIMM sockets with a minimum dimension to motherboard edge of 8.6mm. This keepout is to enable HSIO cabling, power cabling and other platform infrastructure cabling to traverse from Near Side to Far Side zones, as needed by Platform Designers. (Due to differences in DIMM socket widths from various vendors, DIMM placement restriction may also be considered as a minimum distance of 12.1mm to the centerline of the DIMM socket).

This Keepout Zone is shown in **Figure 19. Zones for Primary Side Component Height Restrictions**

Implementation Note:

In some cases, a Compute Core design may only be able to deliver a desired capability by violating the cable keepout zone. By doing so, an HPM will cause issue with a platform's ability to cable High-Speed IO and Power delivery. In this case, a HPM Designer should make efforts to collaborate with Platform Designers on:

1. Increasing Near Side to Far Side power delivery and power egress capability to mitigate loss of power cabling

2. Identify available cabling space for High-Speed IO to meet a given platform configuration

11. Power Delivery

The M-FLW HPM is powered from a 12V DC source. This Base Specification does not cover alternate PSU voltage sources (e.g., 48V DC implementations).

11.1. HPM Power Zones

The HPM supports multiple power zones where significant power delivery and connectivity is expected. **Figure 23** illustrates locations of power zones on the HPM. Details of each zone are described below, some are ingress, some are egress from the HPM.

Figure 23. HPM Power Zone locations

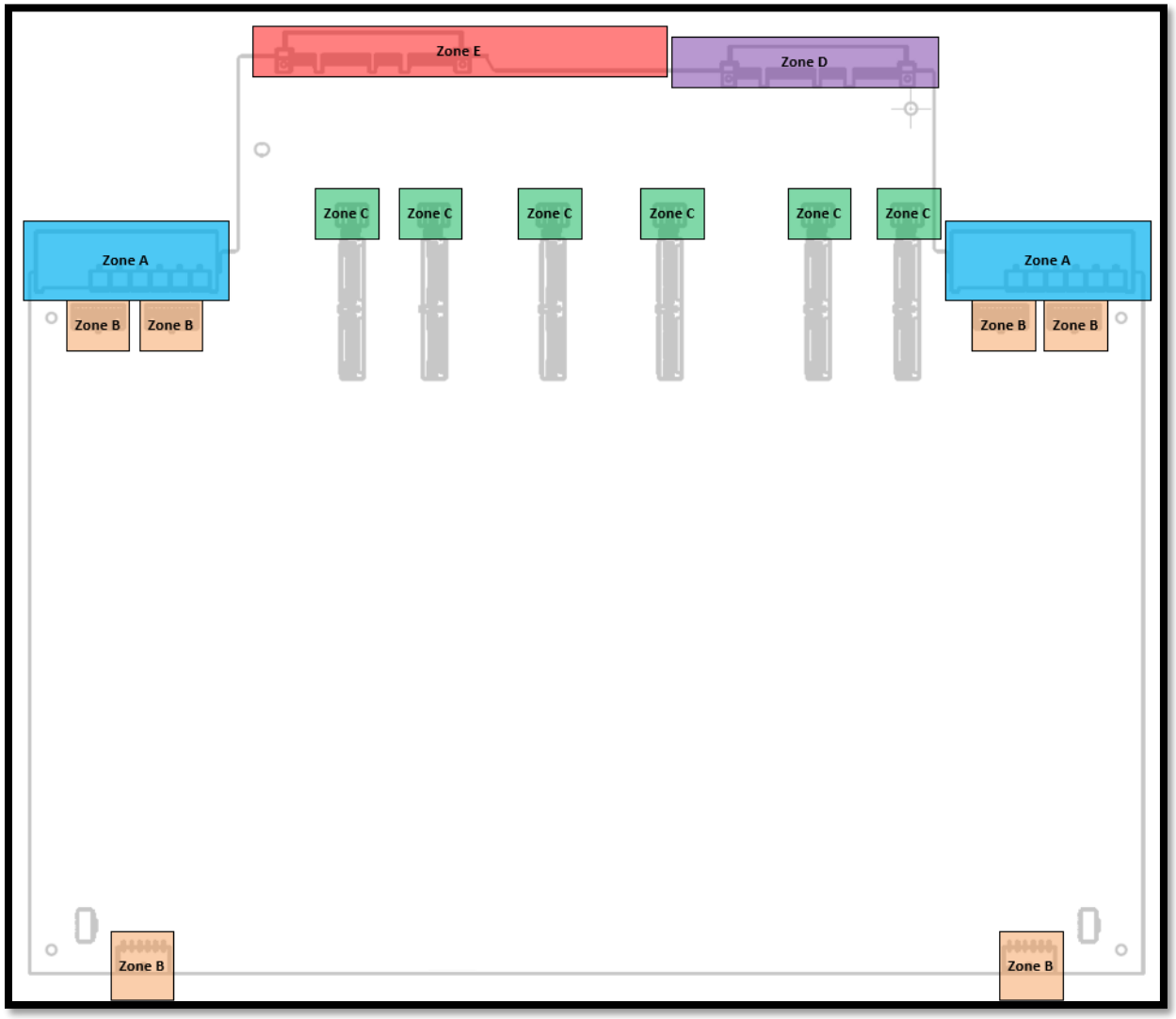


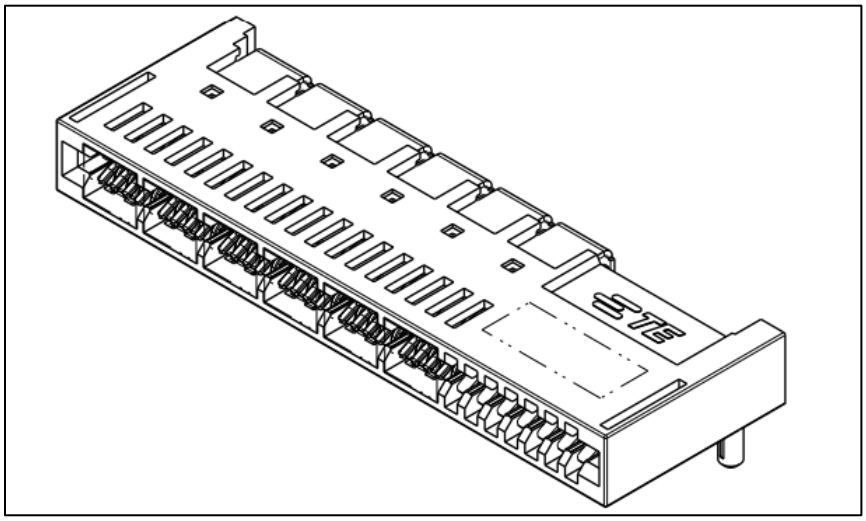
Table 4. Power Delivery Zones

Zone	Feature	Typical Usage	Zone Power Rating
Zone A	M-CRPS Connector	Ingress	up to 3200W
Zone B	2x6+12s PICPWR	Egress	up to 864W
Zone C	Near Side Riser PICPWR	Egress	up to 180W
Zone D	DC-SCM R2.0	Egress	up to 50W
Zone E	OCP NIC R3.0 + Platform Custom Zone	Egress	up to 150W

11.1.1. Zone A – M-CRPS Connector

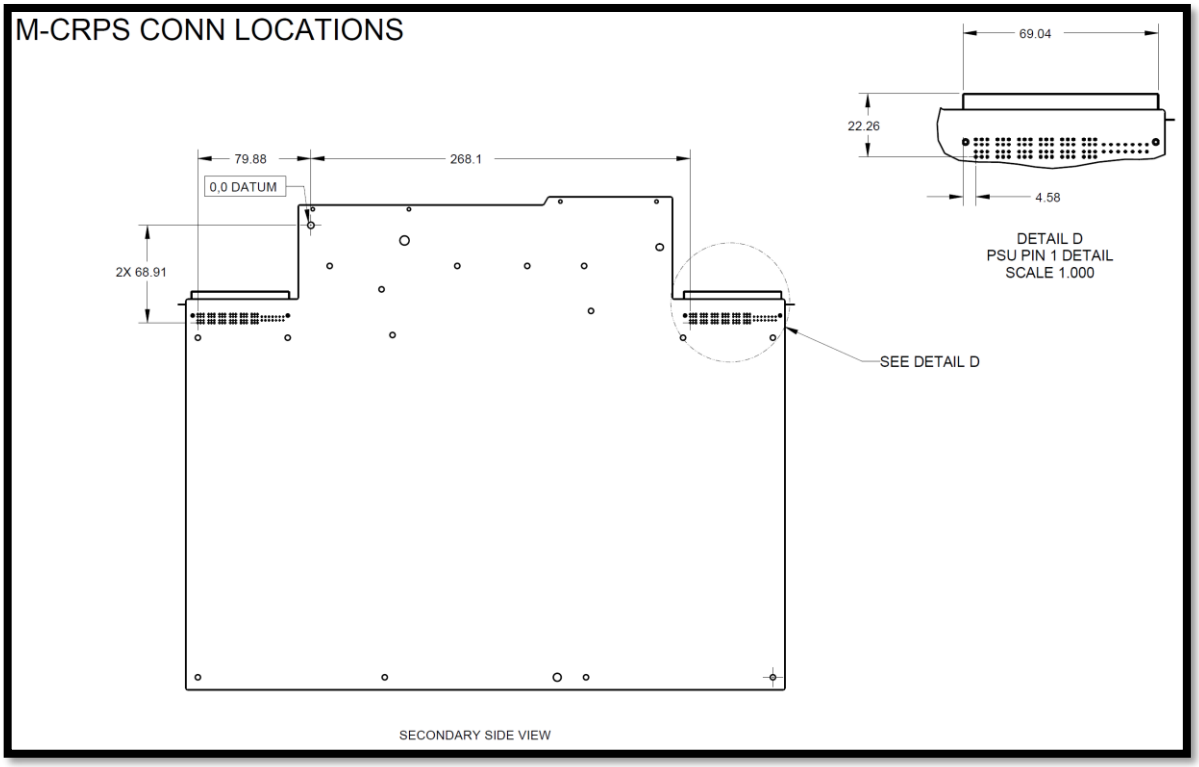
- Connector Power Rating: 3200W
- Typical usage: Power ingress
- Refer to M-PIC and M-CRPS Specification(s) for additional implementation details.

Figure 24. M-CRPS Power Connector



*Locations of M-CRPS connectors shall be placed as defined in **Figure 25***

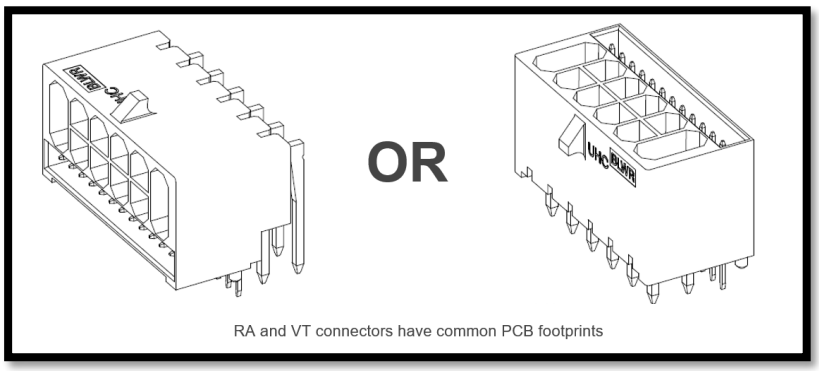
Figure 25. M-CRPS Connector Location Requirements



11.1.2. Zone B – 2x6+12s PICPWR

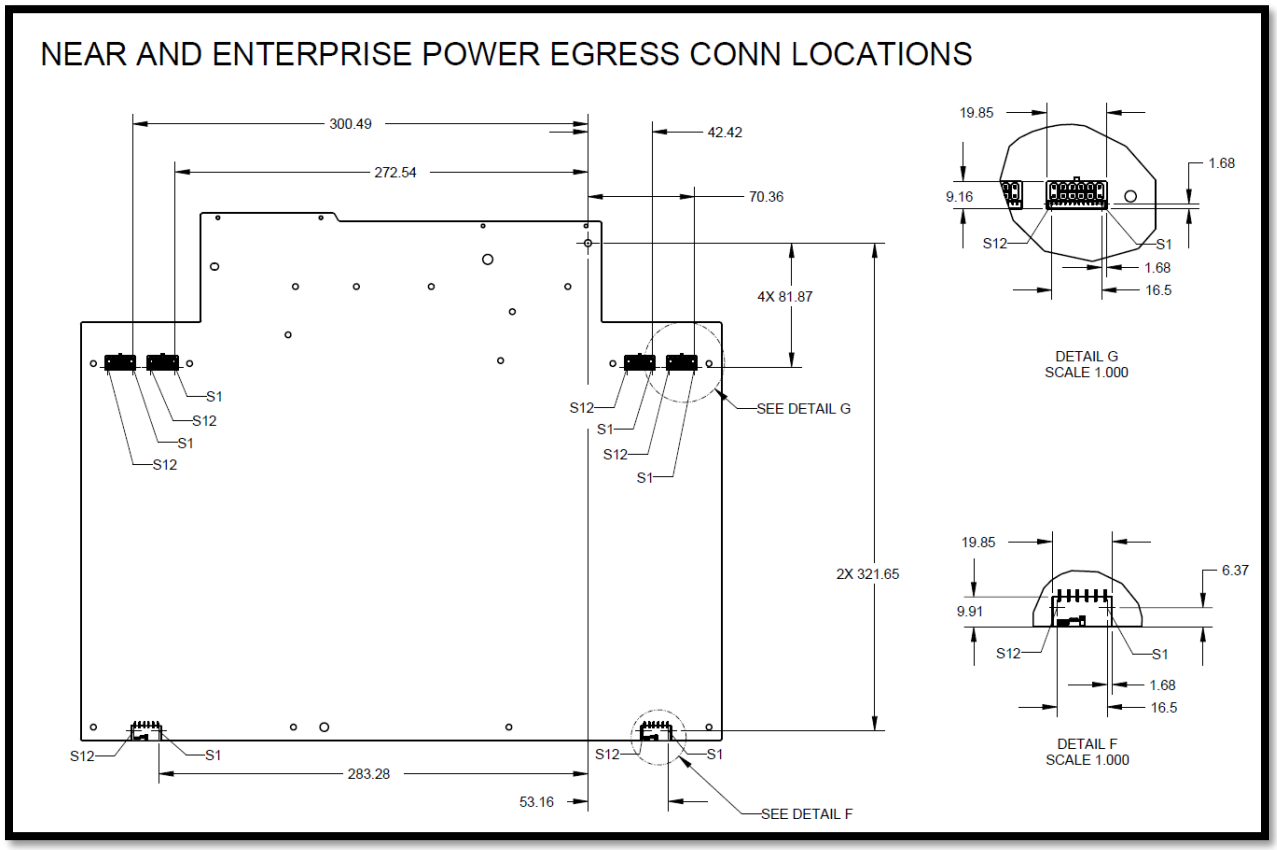
- Connector Power Rating: 864W
- Typical usage: Power egress to peripherals
- Refer to M-PIC Specification for additional details

Figure 26. 2x6+12s PICPWR Power Connectors



*The HPM shall implement 6x PICPWR connectors at locations defined in **Figure 27**.* Note: HPM shall implement these connector footprints (but can be depopulated in assembly BOM at a Design Spec level guidance.)

Figure 27 PICPWR connector (2x6+12s) Location Requirement (6 locations)



11.1.3. Zone C – Near Side Riser PICPWR Egress

- Connector Power Rating: 180W
- Typical usage: Power egress for up to 2x 75W CEM PCIe devices
- Refer to M-PIC Specification for additional details.
- Refer to **Section 10.11 Near Side IO Connectors** for additional details on Near Side connector and location.

The Egress Near Side Riser Power Zone provides power to PCIe devices on risers. This specification does not cover direct dock CEM implementation (non-riser approach). The HPM provides 12V_PRIMARY[1] to the Egress Near Riser Power Zone.

75W Slot power, detailed in **Table 5**, is provided for each PCIe CEM slot on all PCIe risers. The PCIe riser enables a +3.3Vaux and +3.3V (Vcc3_3) power sources derived from the 12V_PRIMARY source from the HPM

Table 5. Minimum HPM Power Supply Rail Requirements per PCIe CEM Slot

Power Rail	75 W Slot[2]
+3.3Vaux	Generated on PCIe riser. Derived from 12V_PRIMARY
+3.3V (V_{cc3_3})	Generated on PCIe riser. Derived from 12V_PRIMARY
12V_PRIMARY Voltage Current	 12V nominal 7.25A total: 5.5 A (CEM 5.0) + ~1.0A (VR conversion to V_{cc3_3}) + ~0.35A (VR conversion to +3.3Vaux) + ~0.40A (misc.)

Note 1: see M-PIC specification for definition of 12V_PRIMARY

Note 2: Additional power is provided to each CEM slot beyond PCIe CEM 5.0 specification to budget for miscellaneous logic on risers and VR conversion losses. Effective total power is 87W per slot.

11.1.4. Zone D – DC-SCM R2.0

- Connector Type: See OCP DC-SCM R2.0 specification
- Connector Power Rating: 50W

11.1.5. Zone E – OCP NIC R3.0 and Platform Custom Zone

- Power Connector Type: See OCP NIC R3.0 spec and M-PIC Boot Storage Connector
- Connector(s) Power Rating: 150W (combination OCP NIC R3 *and* the Boot Storage Connector defined in **Section 10.10 Boot Storage Peripheral Connection**)
- This is a maximum number, the two connectors OCP NIC R3 and Boot Connector may not consume maximum power.

11.2. HPM Power Planes

The HPM power planes (and supplementary power delivery mechanisms like cables) shall have the following features

- At maximum load, the HPM power shapes temperatures have a maximum of 30°C T-rise and do not exceed 100°C absolute
- At maximum load, the maximum HPM voltage drop (IR loss) between power sources and associated loads or connectors is less than or equal to 1%
- Any load (operating up to its maximum power rating) in the platform can be powered with a single operational power source (e.g. PSU), where the total of all loads does not exceed the capacity of the power planes as defined in defined in **Table 6. Minimum Power Plane Capacity Requirements.**
- It is not expected that all loads/connectors on the HPM will be operating at maximum power concurrently. However, it is recommended that, minimally, the power distribution be designed to allow any single load/connector to operate at max power rating.

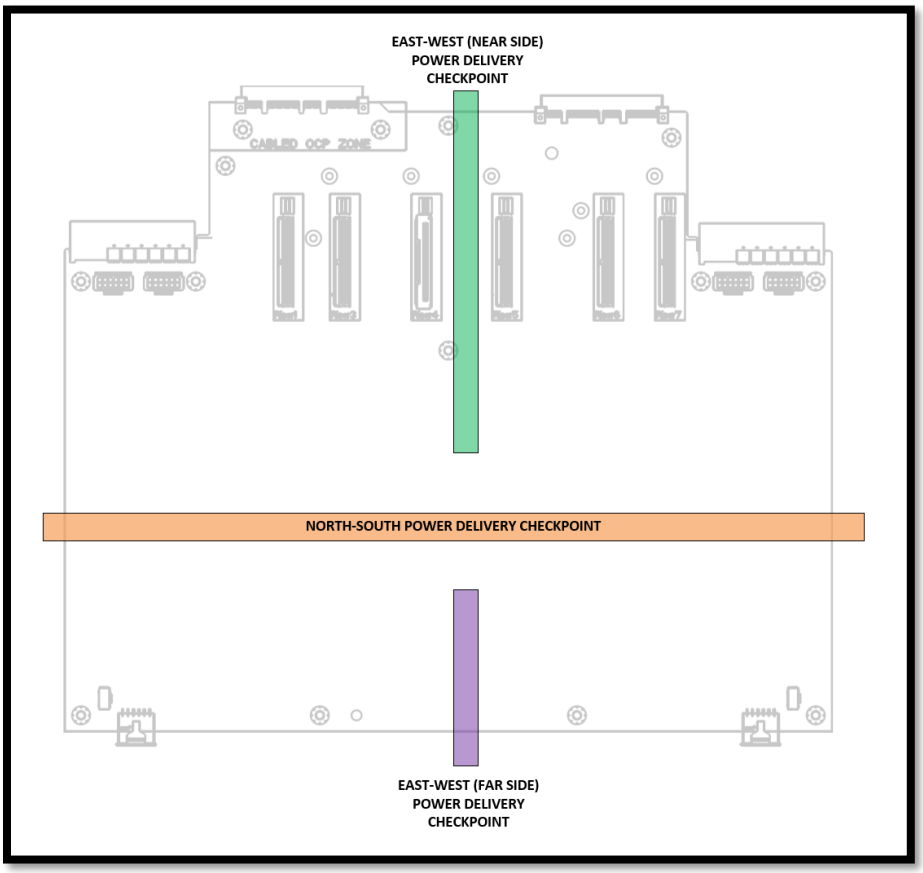
Implementation Note:

It is up to System Designers to understand use cases and loads in different system configurations to ensure that there is adequate power delivery within the HPM

Three checkpoint areas have been defined on the HPM, see **Figure 28**

1) NORTH-SOUTH power delivery checkpoint
2) EAST-WEST NEAR SIDE power delivery checkpoint
3) EAST-WEST FAR SIDE power delivery checkpoint

Figure 28 Power Plane (and Supplementary Power Delivery Mechanisms) Checkpoint Areas



*The sum of all 12V_PRIMARY[1] power planes (and supplementary power delivery mechanisms) INSIDE the cross-sectional areas of the HPM defined by the power delivery checkpoints must meet the minimum power delivery capacity requirements defined in **Table 6**.*

Table 6. Minimum Power Plane Capacity Requirements

Power Plane Checkpoint	Minimum Power Delivery Capacity
NORTH-SOUTH	2800W
EAST-WEST NEAR SIDE	2400W
EAST-WEST FAR SIDE	864W

Note 1: see M-PIC specification for definition of 12V_PRIMARY

12. Adapted M-FLW HPMs

This section shall define open and standardized adaptations of the M-FLW HPM specification.

1. Any additions to interior of form factor, that doesn't impact requirements table, is considered a base M-FLW compliant HPM.
2. If any design attributes of an HPM do not meet the items in **Section 4 Specification Compliance Table**, this results in an Adapted HPM may not be specification compliant, and may not fit existing chassis built to compliant boards.

Future Adapted HPMs will be documented in this section if productized and accepted in future M-FLW revisions.

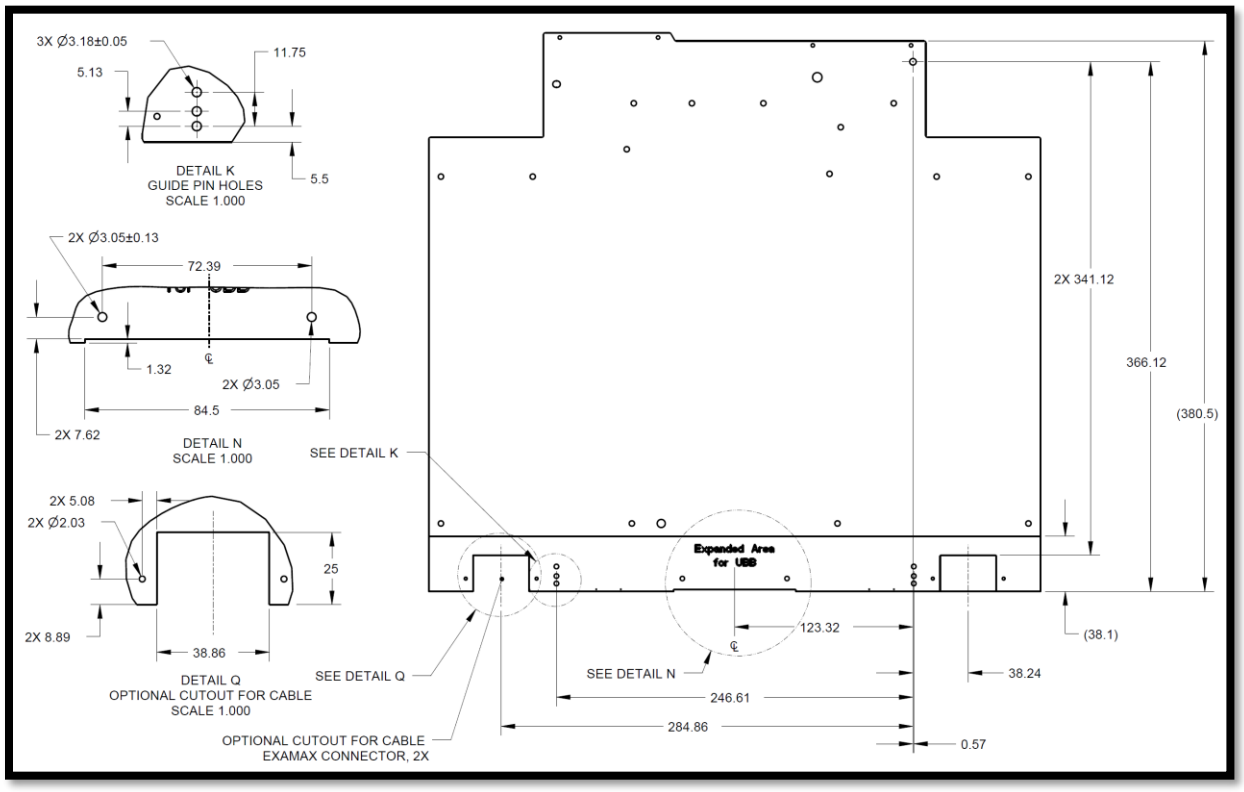
12.1. UBB / Blade FLW Adapted HPM Requirements

UBB Blade M-FLW Adapted HPM architecture leverages the base HPM specifications. Modifications for the UBB Blade Adaptation are focused on the Far Side area to optimize Power Delivery and IO connections meant for UBB Blade implementation. In UBB Blade implementation, blind-mate panel mountable connectors and their specific locations are required.

12.1.1. UBB Blade FLW HPM Outline

UBB Blade M-FLW HPM Outline is an extension of the base outline listed in **Section 10 Mechanical Requirements**. The Far Side dimension of the base outline is extended by 38.11mm [1.5”] to accommodate blind mate IO connectors, Power connector and Blind-mate guide pins to achieve reliable docking with panel-mount connections. This is shown in **Figure 29. Full Width HPM Outline for UBB and Blade.**

Figure 29. Full Width HPM Outline for UBB and Blade M-FLW



865 12.1.2. Blade High Speed IO connector

High Speed IO connector outline shown in **Figure 29** is based on Amphenol ExaMAX family or equivalent. There are seven 4x8 ExaMAX shown from left to right and the one in far right is shown as 6x8 ExaMAX to include extra clock and signals. The connector's pin-out would be
870 included in M-XIO specification. The specification defines the position of the ExaMAX connector to allow flexibility for implementors to select board or cable connector version to be chosen.

Table 7 Blade Far/South High-Speed IO Recommended Connectors

Connector family	Company	Configuration
ExaMAX / ExaMAX 2	Amphenol or Equivalent	4 pairs X 8 columns
ExaMAX / ExaMAX 2	Amphenol or Equivalent	6 pairs X 8 columns

Figure 30 ExaMAX 4x8 connector

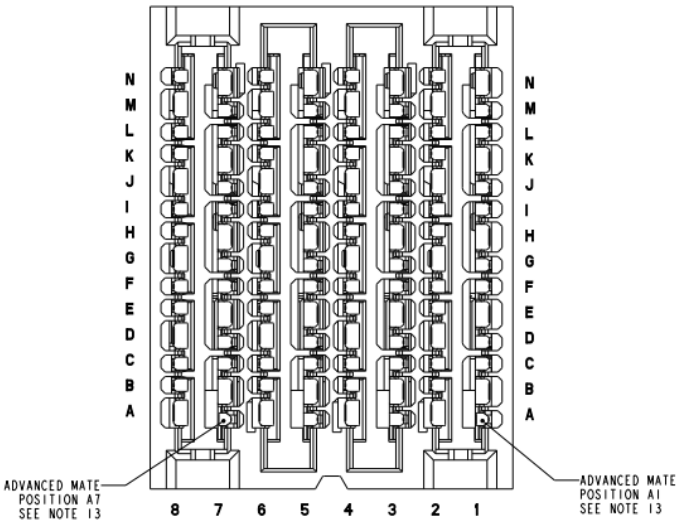
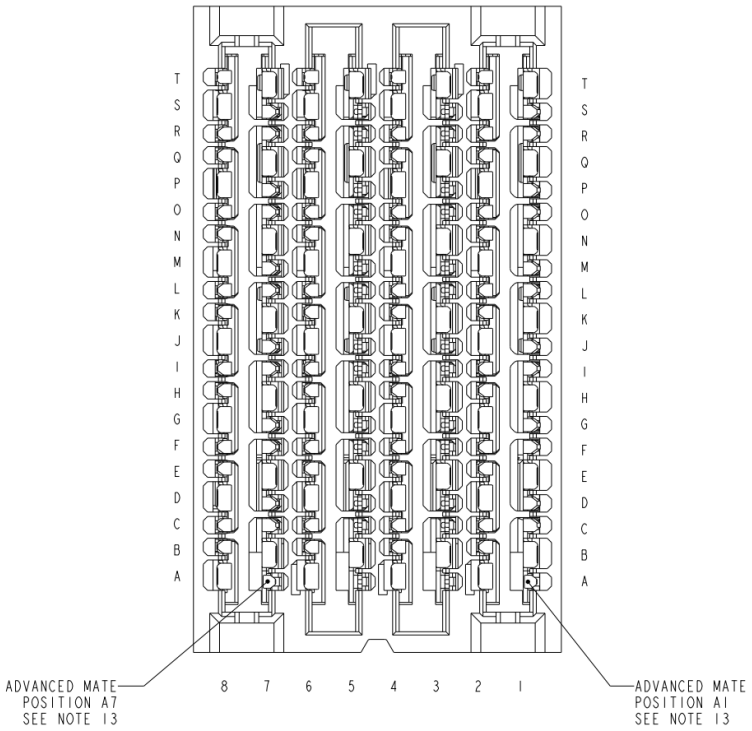


Figure 31 ExaMAX 6x8 connector



Refer to M-PIC Specification for additional details.

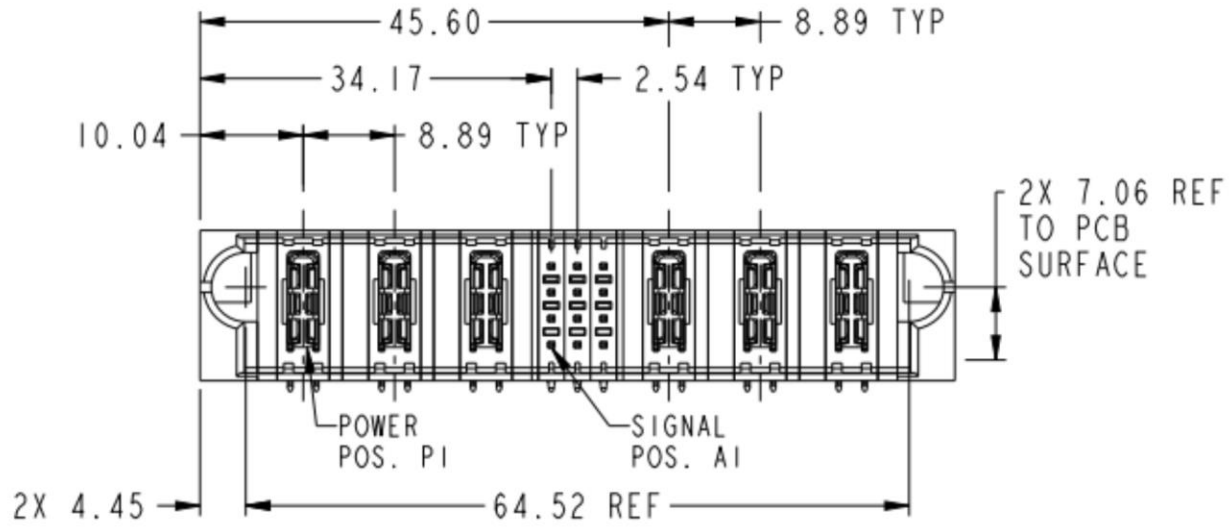
12.1.3. Ingress Power Connector

Far Side power connector shown in **Figure 32** is based on Amphenol PowerBlade+ or equivalent. The configuration is 3 high-power contacts on each side with 12 signal contacts in the middle. The connector is capable of up to 2000W with 12V input voltage. The connector pin-out would be included in M-PIC specification and leverage PICPWR connector pin definition.

Table 8 Blade Far/South Ingress Power Recommended Connector

Connector Family	Company	Configuration
PowerBlade+	Amphenol 10106263-6003003LF or equivalent	3 High Power + 12 Signals + 3 High Power

Figure 32 PowerBlade+ Ingress Power Connector

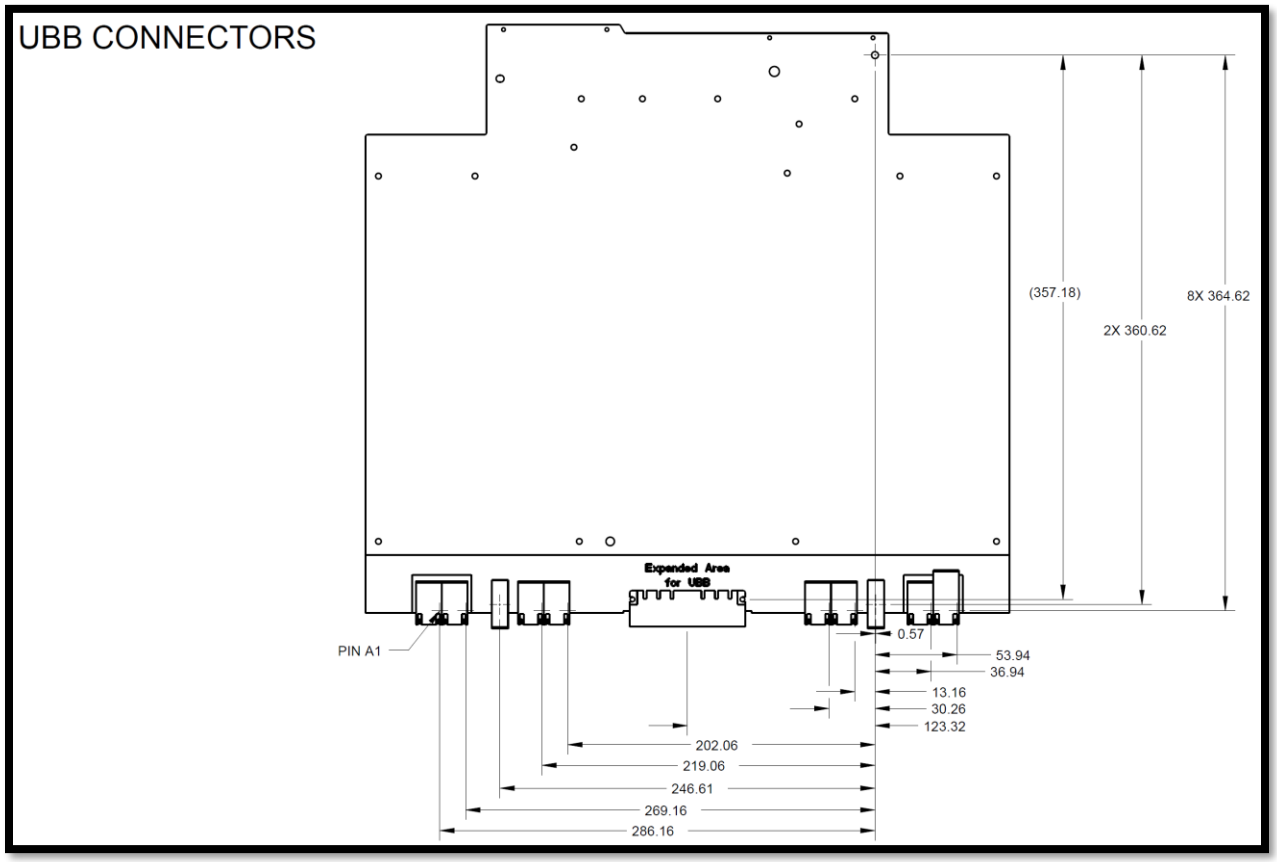


Refer to M-PIC Specification for additional details.

12.1.4. UBB Connector Locations for Power and High-Speed IO

The connector locations for the UBB Adapted M-FLW HPM are specified in **Figure 33**. The Adapted HPM shall comply with these connector locations.

900 **Figure 33. UBB M-FLW HPM Required Connector Locations**



*Note that the standard M-PIC Power connector locations that required in **Figure 27**, shall be maintained in UBB M-FLW Adapted HPMs.* BOM population choices can be made by System Designer.

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12.1.5. Blade Minimum Power Plane Capacity Requirements

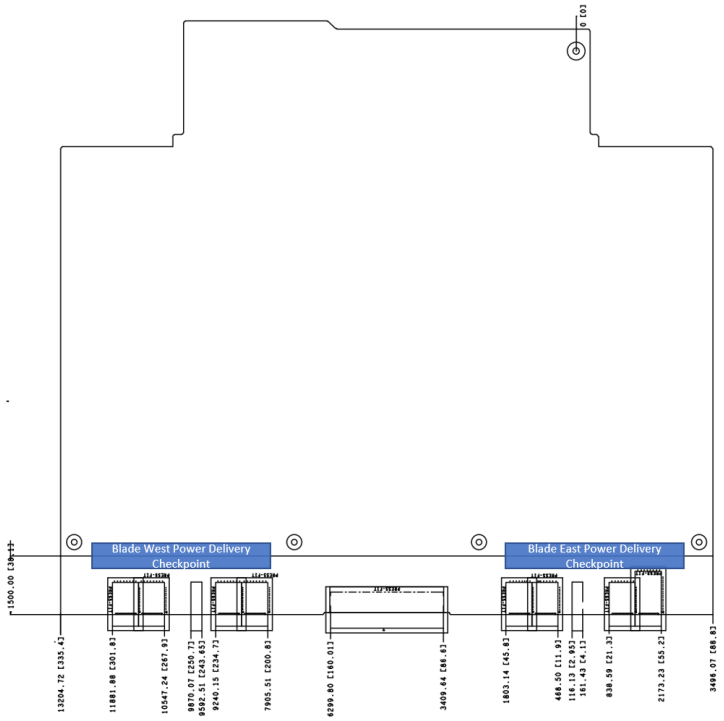
UBB Blade Far Side power delivery ingress is intended to heavily leverage existing power delivery capacity in base HPM definition. *As such, the bulk of power delivery capacity requirements shall follow requirements currently defined in Far Side PICPWR connector (see **11.1.2 Zone B – 2x6+12s PICPWR**). The PICPWR connectors at the Far Side must be de-populated.*

To ensure the UBB Blade Adaptation has sufficient power delivery capacity at the Far Side area, UBB Blade left and right, the Power Delivery Checkpoint area, and its minimum capacity requirements are defined in **Figure 34** and **Table 9**

Table 9 Blade Minimum Power Plane Capacity Requirements

Power Plane Checkpoint	Minimum Power Delivery Capacity
Blade West	1100W
Blade East	1100W

Figure 34 UBB Blade Power Plane Checkpoint Areas



12.1.6. Blade Mechanical Guide Pin

The outline shown in **Figure 29. Full Width HPM Outline for UBB and Blade M-FLW** also includes a position identified for a mechanical guide pin for blind mate alignment. *The HPM shall implement this feature for safe blind mate implementation. The part number to use for the guide pin is Amphenol 10037912-101LF or equivalent.*

12.2. Adapted HPM Outlines for OCP NIC R3.0

Adapted HPM outlines may be utilized by customers for unique requirements. These alternatives may not be compatible with chassis designed to the Base Specification M-FLW outline. These alternatives are intended to improve compatibility for chassis and HPMs that can align to these options.

Alt Outline Name	Key Difference from Base
Near Edge Cabled NIC Outline	HPM outline modification to detach OCP NIC R3.0
Near Edge OCP NIC LFF Support	HPM Outline modification to enable 2x of the OCP NIC R3.0 connectors for full support of LFF form factor (SFF-TA-1002, 4C+ connectors)

A Platform may wish to NOT have OCP NIC R3.0 direct dock to the HPM. For chassis compatibility, it is assumed the platform's OCP NIC R3.0 is to be cabled in the same mechanical location of a chassis that is compliant to this specification. In the outline cutout change (material removal) is prescribed to enable an OCP NIC R3.0 card.

The cable assembly (including PCB with OCP NIC R3.0 connector) is assumed to be placed and fixed in the same location Platform/chassis as the direct dock OCP NIC R3.0 placement required in **Figure 10. Centerline Locations of OCP NIC R3.0 and DC-SCM R2.0.**

Figure 35. Outline Cutout Modification to Enable Cabled OCP NIC R3.0 in Base Outline

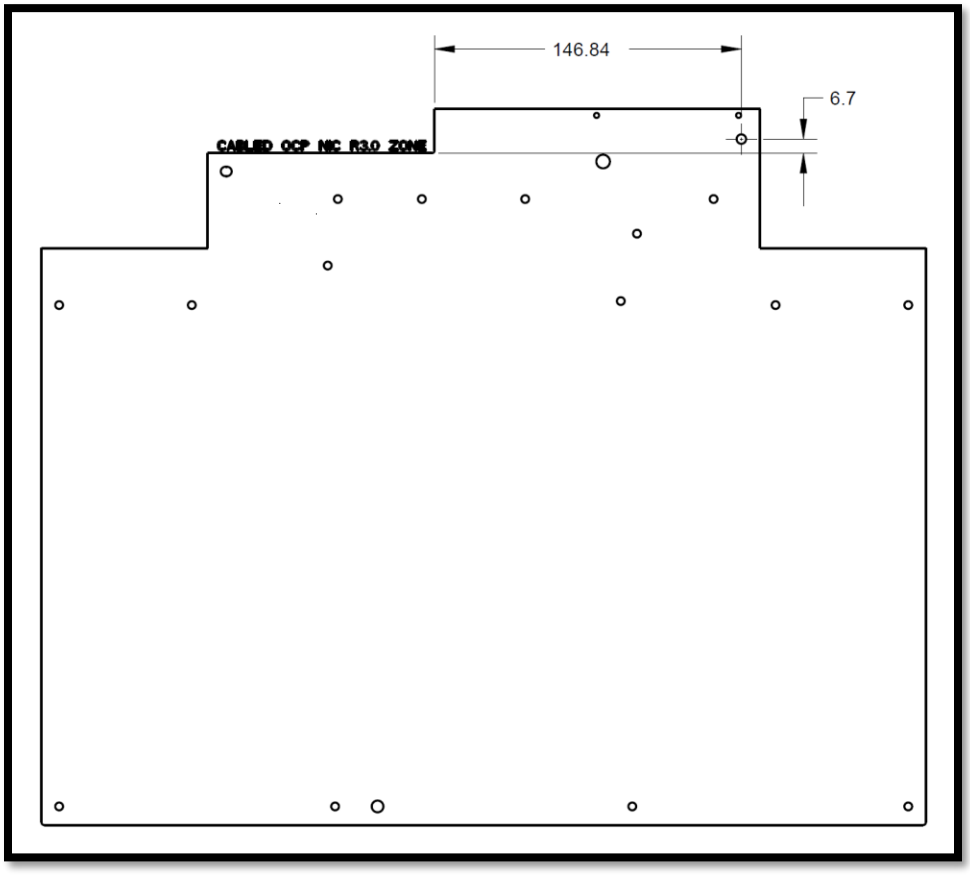
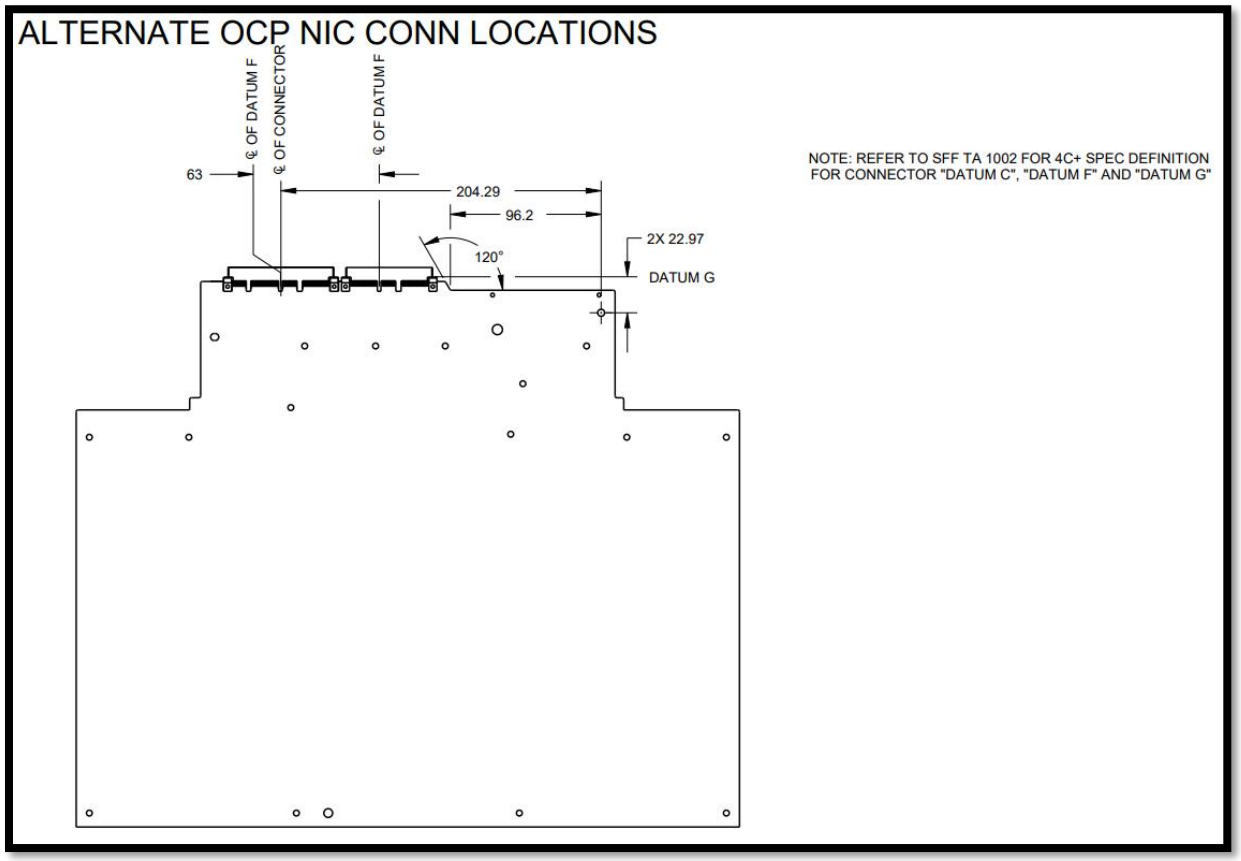


Figure 36. Alternate Outline to Enable OCP NIC R3.0 LFF

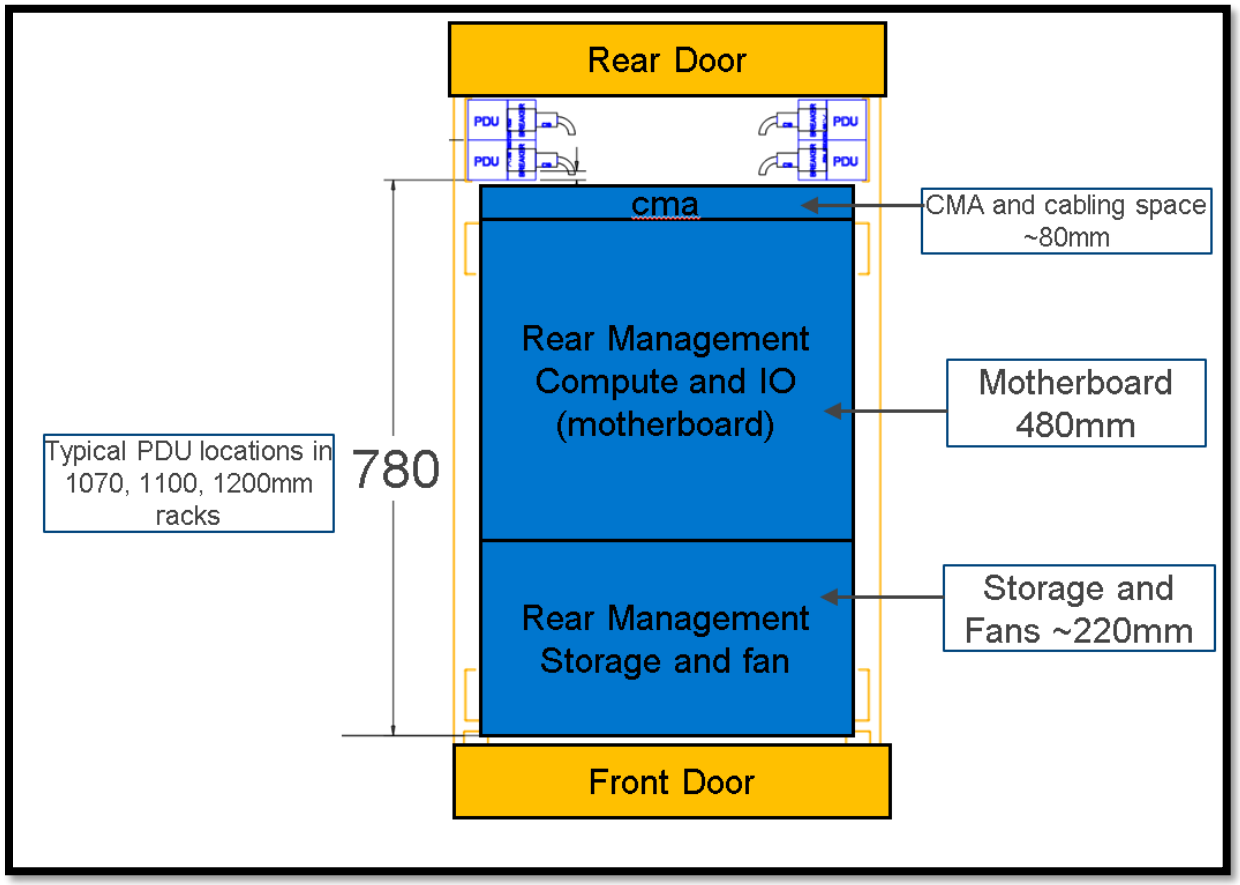


13. Supplemental Information

13.1. Rack and Chassis Depth Stackup Assumptions

The M-FLW HPM Base Specification is constructed under the considerations that the installation environment has a Power Distribution Unit approximately 780mm from the front EIA flange. Although platforms may vary in depth, the board size constraint is chosen to enable typical chassis storage systems using this M-FLW HPM spec to fit with a Cable Management arm in less than the 780mm PDU constraint.

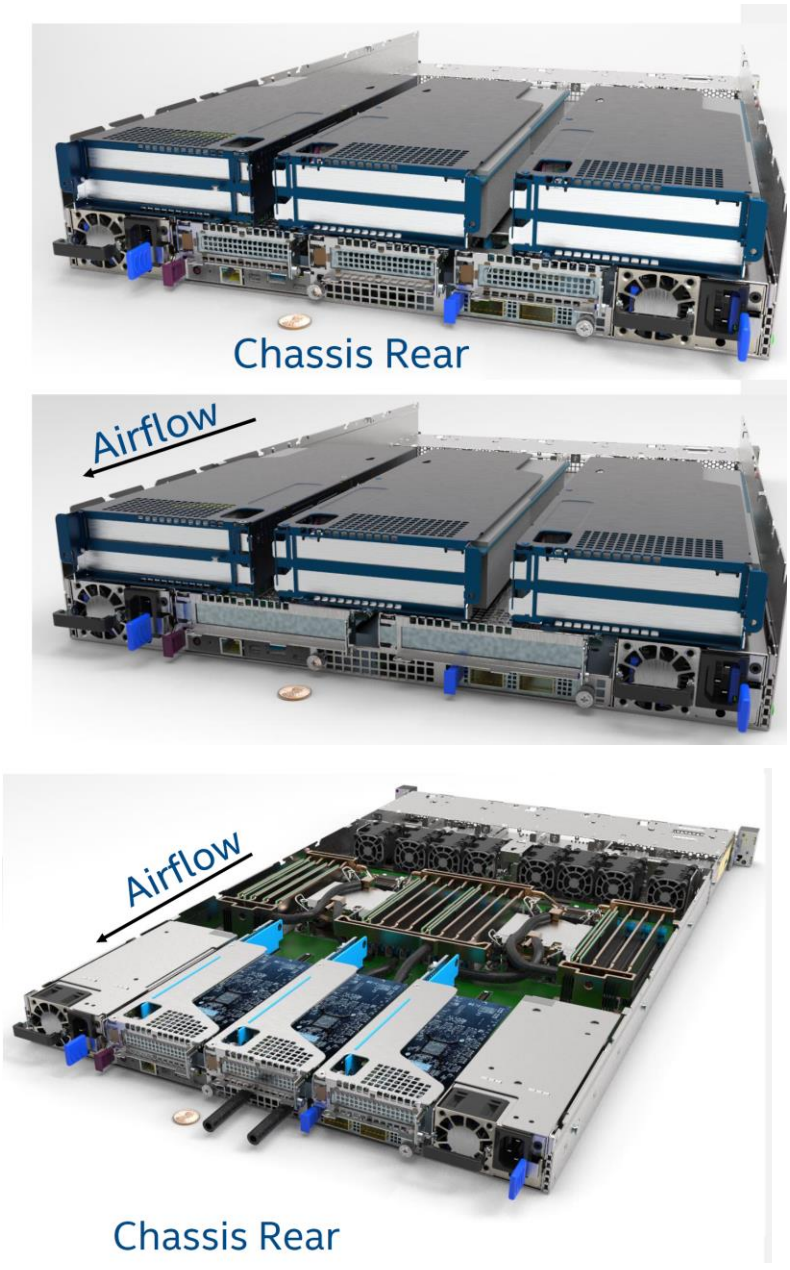
Figure 37. Rack Depth Constraints



13.2. 1U and 2U PCIe Slot Typical Configurations

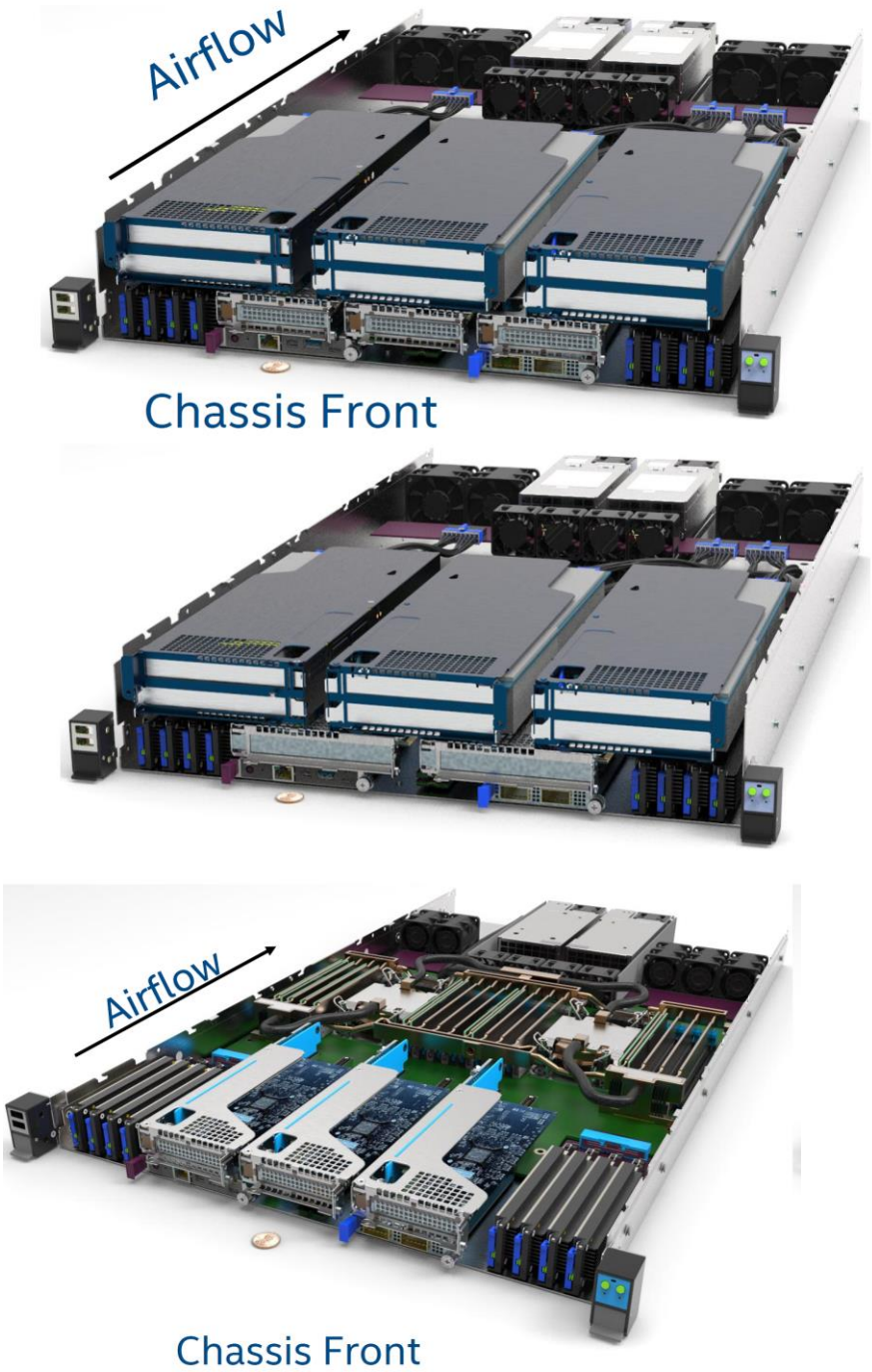
The following images in **Figure 38** are of typical Enterprise 1U and 2U PCIe Slot Configurations.

Figure 38. Typical 1U and 2U PCIe Slot Configurations for Rear Management System



The following images in **Figure 39** are of typical Hyperscale 1U and 2U PCIe Slot Configurations. Note, these are 19” FrontIO chassis like OCP Project Olympus. Also, the front can be shuffled around using an extra “adapter board” like **Figure 42** not covered by the HPM spec.

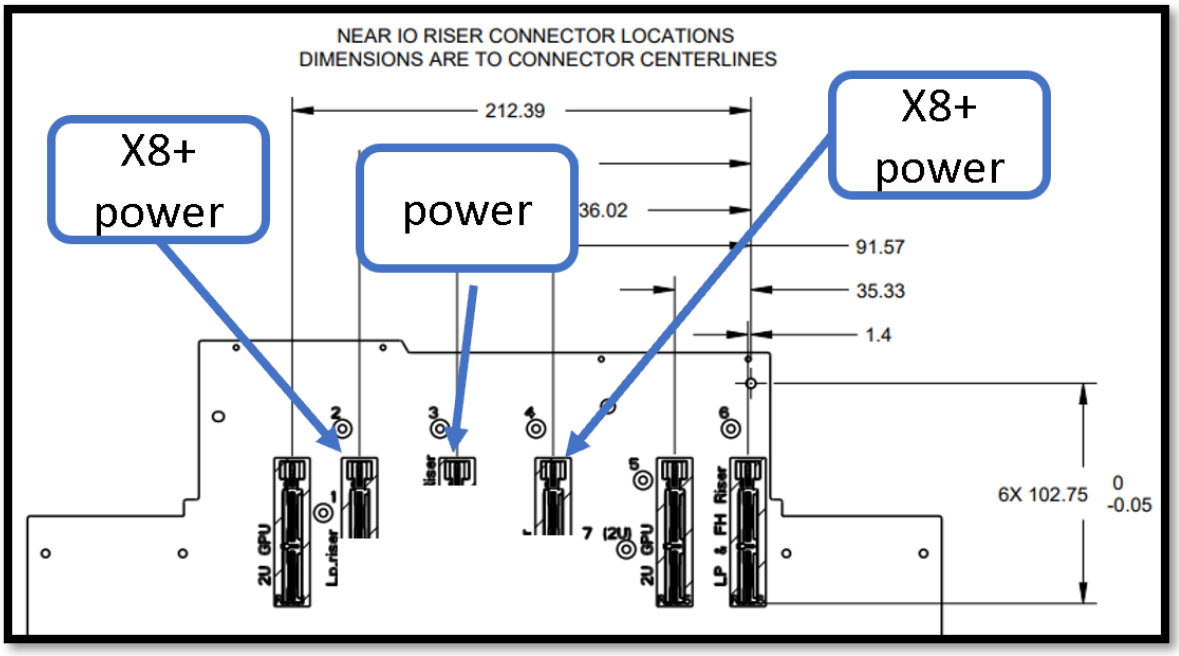
970 **Figure 39. Typical 1U and 2U PCIe Slot Configurations for Front Management System**



13.3. Example Scenario for Near IO Population with less than 6x16 ports

As shown in **Figure 40** the HPM Designer may elect to follow the rules shown in **Section 10.11.2 Population of Near Side M-XIO Connectors**. An example of this is shown below. HSIO might be cabled into the riser, but the riser still has the PICPWR portion of the connector for PCB applications.

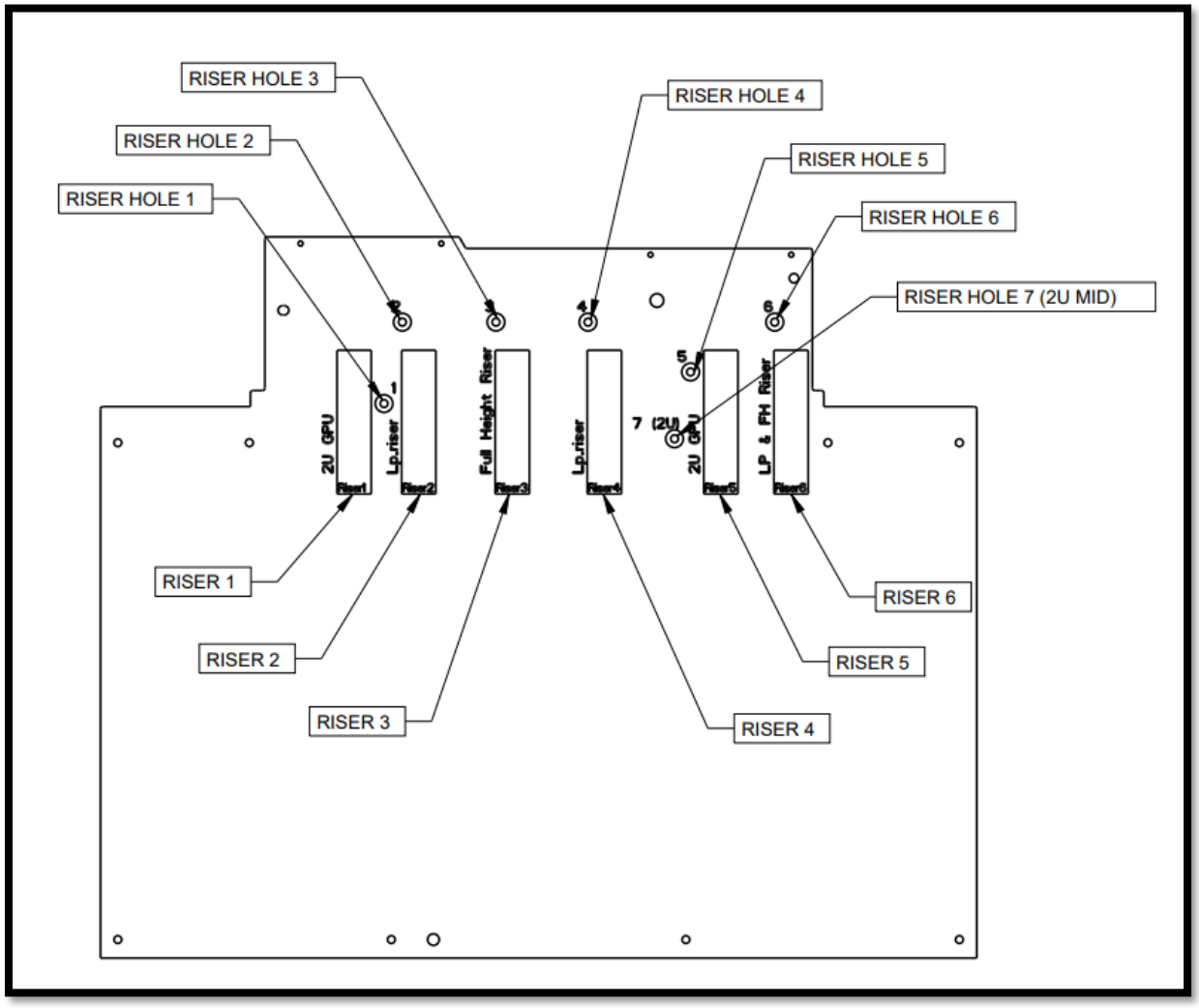
Figure 40. Example Near IO Connector Population Scenario



13.4. Additional Information on Near IO Riser Retention Holes

In a system configuration that uses riser cards in the Near IO, mechanical retention is enabled by holes in the HPM near each Near IO location. The following **Figure 41** demonstrates the riser retention holes and which Near IO position each hole is associated with.

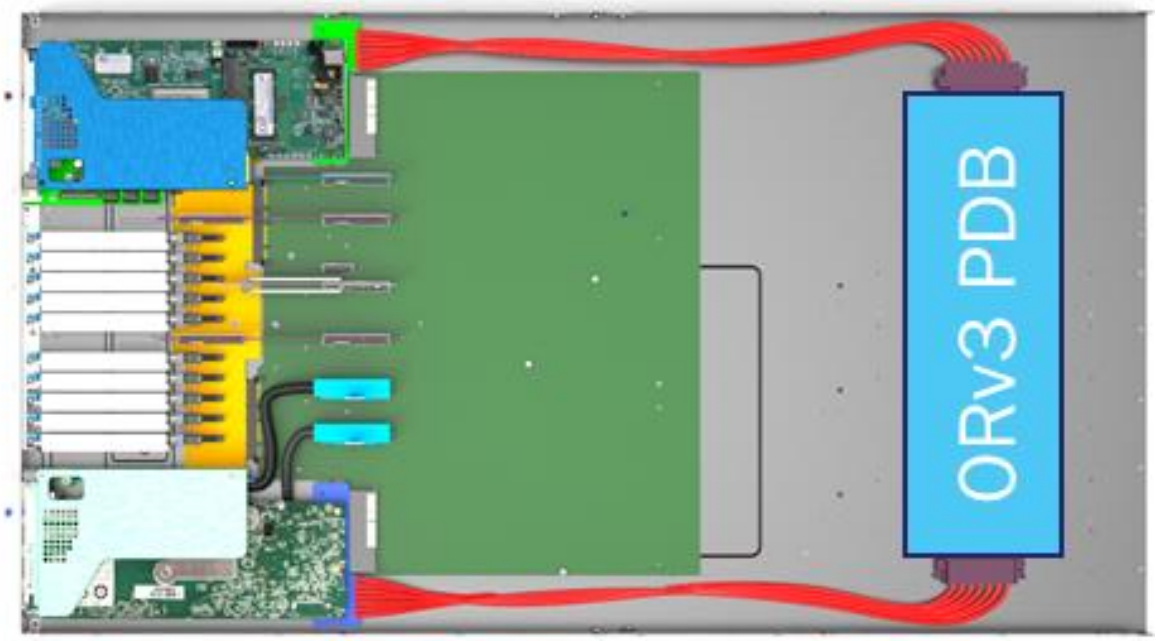
Figure 41. Riser Retention Holes and Associated Near XIO Locations



13.5. Reference System Architecture in 21” Chassis

Figure 42 shows how the Base Outline HPM can be utilized in a 21” chassis architecture, including if Power Supply Infrastructure is on the Far Side with cables to the near side power ingress.

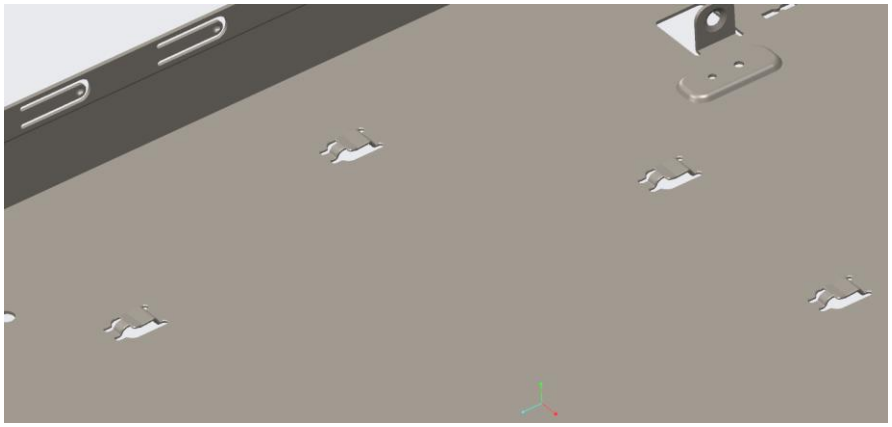
Figure 42. Base Outline HPM used in 21" Reference Chassis



13.6. Chassis Base Geometry for Chassis-to-Board Bracket interface

Figure 43 demonstrates example geometry required in the chassis base to interface to the Chassis-to-HPM bracketry in **Figure 20. Example of Chassis-to-HPM Bracket (Board Pan).** The exact geometry is not specified, but considerations must be made for maximum board thickness (see **Section 10.3 HPM Board and Assembly Thickness**) and HPM Keepout Zone sizes (See **Section 10.4.1 Keepout Zone for Retention Hardware**).

Figure 43. Chassis Base Geometry to Interface Chassis-to-Board Bracketry



13.7. CAD files

This will be filled out at version 1.0.

14. Appendix A - Checklist for IC approval of this specification (to be completed by contributor(s) of this Spec)

Complete all the checklist items in the table with links to the section where it is described in this spec or an external document.

This will be filled out at version 1.0.

15. Appendix B - <supplier name> - OCP Supplier Information and Hardware Product Recognition Checklist

(to be provided by each supplier seeking OCP recognition for a Hardware Product based on this specification)

This will be filled out at version 1.0.