EDGECORE Networks Corporation

Edgecore AS7316-26X

Programming Guide

Revision 1.0

OPEN

Compute Project

Revision History

Revision	Date	Author	Description
1.0	9/15/2018	Jeff Catlin	Initial Draft

Contents

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	AS7316-26X
CPU sub-system	CPU: Intel Xeon D1519 1.5G DDR SDRAM: 8GB x 2 2133MHz with ECC (SO-DIMM) DDR4 SPI Flash (Boot): 16MB x 2 mSATA: 128GB MLC TPM: SLB 9665XT2.0 FW5.63 INFINEON
Management	UART RS232 console port (RJ45), Out-band Management Ethernet port (RJ45)
MAC	Broadcom BCM88470, 300Gbs full duplex switching
Ethernet Ports	16x 10G SFP + 8x 25G SFP28 + 2x 100G QSFP28
BMC	AST2400
CPLD	Altera 5M2210ZF324I5N (FBGA324) and 5M1270ZF256I5 (FBGA256)
FPGA	Altera 10M16DCU324I7G
PCB	20-Layers, TU-883+TU-862HF (Hybrid material) for Mainboard 12-Layers, TG 180 for CPU module 10-Layers,TG 150 for Connection Board 4-Layers, TG 150 for FAN Board 8- Layers, TU-662、EM-825 for BMC Board
Power Supply	400W PSU, airflow direction is front to back, DC to DC, AC to DC, 1+1 redundant load-sharing, hot-swappable. Notes: The airflow is front to back from chassis system view.
Cooling	5 fan-tray modules with 5 pcs of 40mm x40mm x 28mm 12V fans, hot-swappable
Dimension	L(Depth):299.8±0.5mm (11.8031±0.0196inch) W(Width):438.4±0.5mm (17.259808 ± 0.0196 inch) H(Height):43.25±0.5 mm (1.7027±0.0196inch)

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Scope

This document outlines the technical specifications for the Edgecore AS7316-26X Open Switch Platform submitted to the Open Compute Foundation to aid in porting software to the hardware platform.

Overview

This document describes the technical specifications of the AS7316-26X Cell Site Gateway Router designed by Edgecore Networks Corporation. The AS7316-26X is a cost optimized design focused on the aggregation of 10G/25G cellular equipment and providing 100G backhaul connections. The AS7316-26X supports a broad set of IEEE 1588 /SyncE features geared towards 4G and 5G timing needs.

The AS7316-26X supports sixteen SFP+ ports, eight SFP28 ports, and two QSFP28 ports for network connectivity.

The AS7316-26X is a PHY-Less design with the network interface connections directly attaching to the Serdes interfaces of the Broadcom 88470 switching silicon providing the lowest cost, latency, and power. The AS7316-26X supports traditional features found in switches such as:

- Redundant field replaceable power supply and fan units
- Support for “Front to Back” air flow direction
- Supports a modular CPU card that allows flexibility in the CPU and/or memory configurations that can be offered.
- Support for AC or DC power supply units

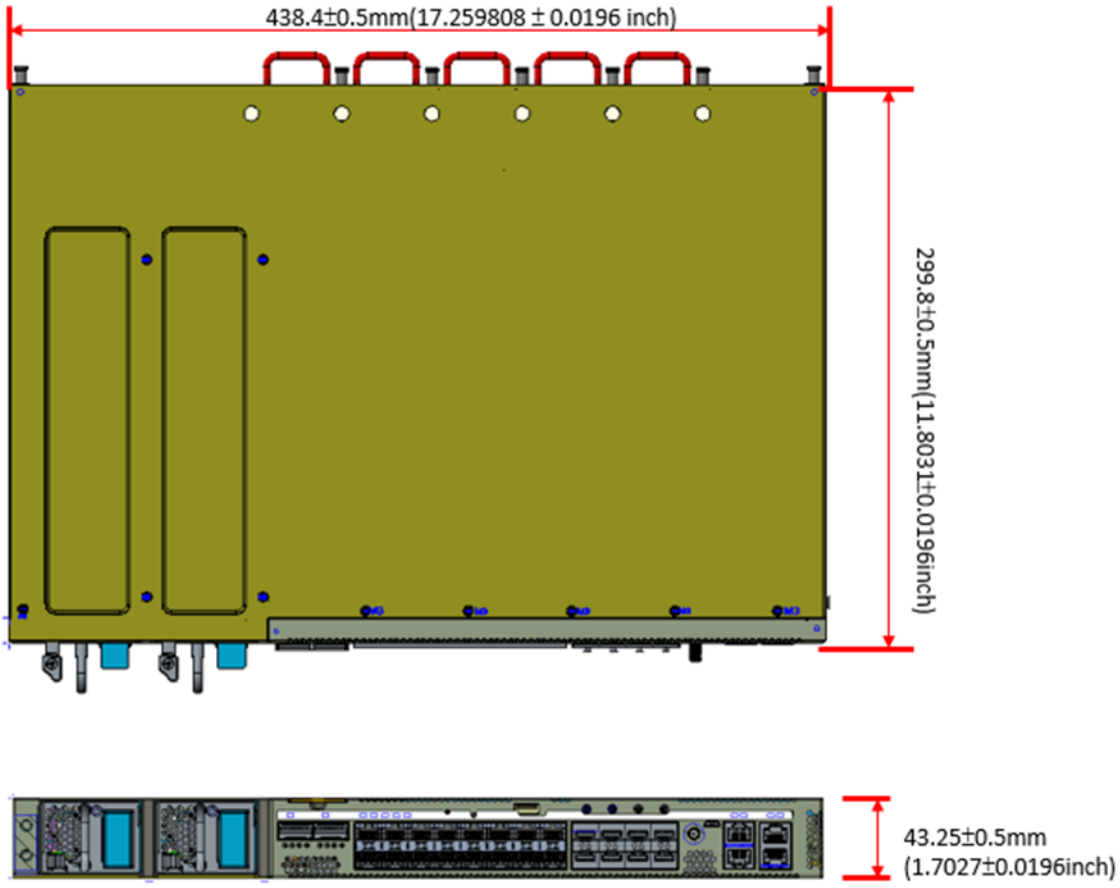
Physical Overview

Front View

Rear View

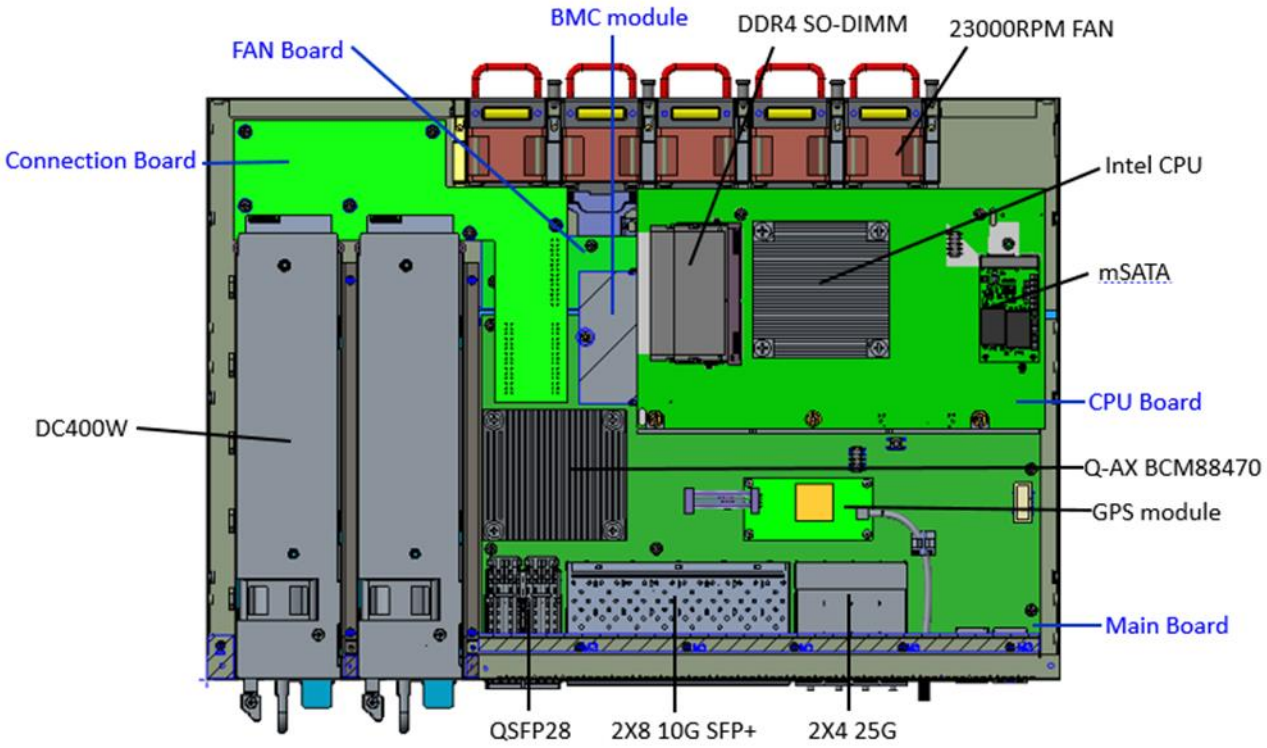
Dimensions

	Inches	Millimeters
Length	11.80	299.8
Width	17.26	438.4
Height	1.70	43.25

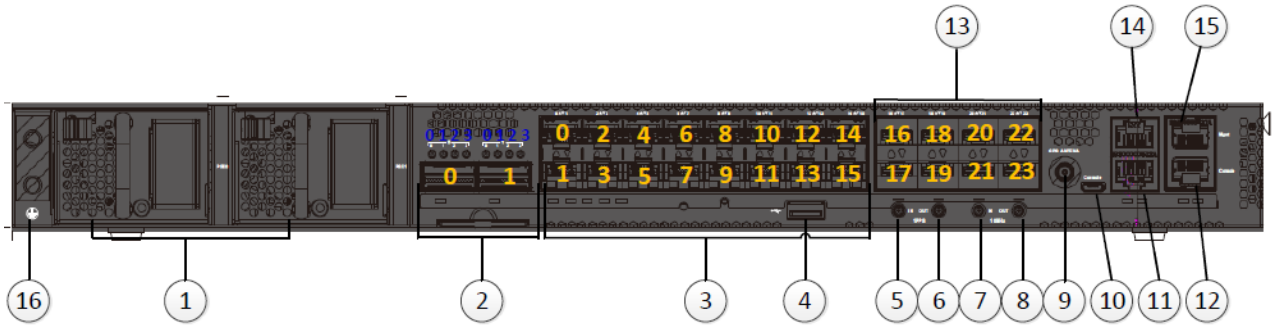


Top View

The top view of the AS7316-26X shows the PCBs and associated components in the AS7316-26X system



Front View Detail



The front panel view of the AS7316-26X includes the following key components:

Description	
1- Power Supplies	9- GPS antenna port
2-100 Gigabit Ethernet QSFP28 ports	10-Micro USB console port
3-10 Gigabit Ethernet SFP+ ports	11-Time of day (**ToD**) RJ45 port
4-USB storage port	12-RJ45 console port
5-1PPS input port	13-25 Gigabit Ethernet SFP28 ports
6-1PPS output port	14- Building-Integrated Timing System port (**BITS**)
7-10MHz input port	15-Management Ethernet port (**MGMT**)
8-10MHz output port	16-Grounding mark

Front Panel LEDs

Network / Timing LEDs

The status of port LED will not be affected when the switch is in configuration mode. Each port has its dedicated LED with QSFP28 and SFP+ connectors. The management port has dedicated LED to indicate Link and Activity. The ToD and BITS ports have dedicated LED to indicate Link status.

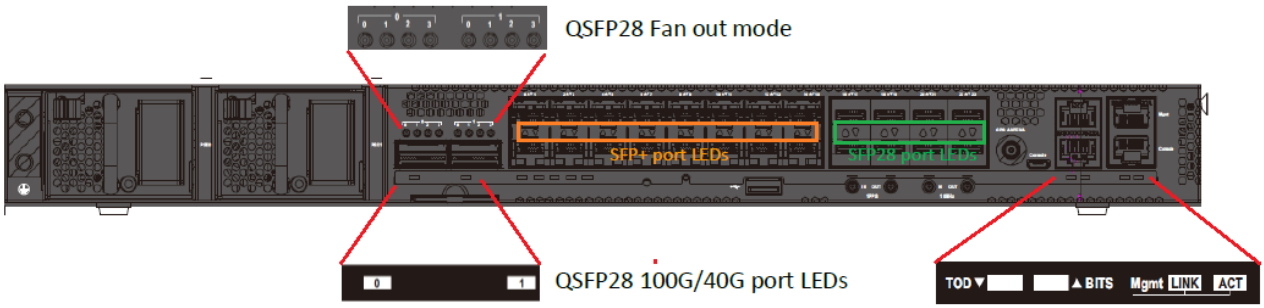


Figure 1 Network and Timing Port LEDs

Port LED Definition		
LED	CONDITION	STATUS
SFP+ Port LED (Port00 to Port15)	On/Flashing Green	SFP+ port has a valid activity at 10G mode and the flashing to indicate activity.
	On/Flashing Amber	SFP+ port has a valid activity at 1G mode and the flashing to indicate activity.
	Off	There is no link on the port.
SFP28 Port LED (Port16 to Port23)	On/Flashing Blue	SFP28 port has a valid activity at 25G mode and the flashing to indicate activity.
	On/Flashing Green	SFP28 port has a valid activity at 10G mode and the flashing to indicate activity.
	Off	There is no link on the port.
QSFP28 Port LED in 40G/100G Mode. (The LEDs are under the port24&port25 of QSFP28 cage)	On/Flashing Green	QSFP28 port has a valid activity at 100G mode and the flashing to indicate activity.
	On/Flashing Blue	QSFP28 port has a valid activity at 40 G mode and the flashing to indicate activity.
	Off	There is no link on the port.
QSFP28 Port LED in 25G Fan Out Mode. (With Breakout cable)	On/Flashing Amber	QSFP28 port has a valid link at 25G via break out cable. The LED on 100G QSFP28 end is also present OFF. Flashing indicates activity.
	Off	There is no link on the port.
QSFP28 Port LED in 10G Fan Out Mode. (With Breakout cable)	On/Flashing Purple	QSFP28 port has a valid link at 10G via break out cable. The LED on 40G QSFP28 end is also present OFF. Flashing indicates activity.
	Off	There is no link on the port.
OOB Port LED (Link)	On / Green	Port has a valid link
	Off	There is no link on the port

OOB Port LED (Activity)	Flashing / Green	Flashing indicates activity
	Off	There is no link on the port
ToD Status LED	On/Flashing Green	ToD port has an activity and the flashing to indicate activity.
	Off	There is no link on the port
BITS Status LED	On/Flashing Green	Bits port has activity and the flashing to indicate activity.
	Off	There is no link on the port

System LEDs

The system LEDs are used to indicate the status of power and system.

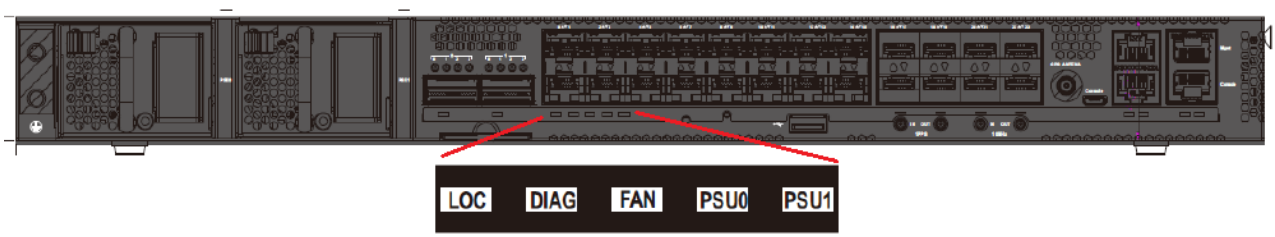


Figure 2 System LEDs

System LED Definition		
LED	CONDITION	STATUS
PSU0 (Power Supply Status)	Green	This power is operating normally.
	Amber	PWR present but not power on or this power is fault.
	Off	Power supply not present.
PSU1 (Power Supply Status)	Green	This power is operating normally.
	Amber	PWR present but not power on or this power is fault.
	Off	Power supply not present.
DIAG (Diagnostic)	Green	System self-diagnostic test successfully completed.
	Green Blink	System self-diagnostic test is in progress.
	Amber	System self-diagnostic test has detected a fault.
FAN	Green	System FAN operating normally.

	Green Blink	System FAN tray is power off when ambient temperature is less than 10 degree C.
	Amber	System FAN tray present but is fault.
LOC	Amber Flashing	Flashing by remote management command. Assists the technician in finding the right device for service in the rack.
	Off	Not a particular switch that technician need to find.

Front panel ports

- Micro USB port console port
  - Used for RS232 type management
- RJ45 Console Port
  - Used for RS232 type management
- RJ45 10/100/1000 Ethernet management port
  - Connected directly to the system CPU
- RJ45 ToD Port
- RJ45 BITs

Console Port

The console port interface conforms to the RJ45 electrical specification.

The interface supports asynchronous mode with default eight data bits, one stop bit, and no parity. The unit will operate at any one of the following baud rates:

•9600, 19200, 38400, 57600, **115200 (Default)**

Pin number	Pin name	Pin number	Pin name
1	RTS	**2**	UART_TXD
3		**4**	
5	GND	**6**	UART_RxD
7		**8**	CTS

Network ports

SFP+ Ports (sixteen in total)	Standard SFP / SFP+ MSA compliant modules supporting 1G and 10G options for copper and fiber
SFP28 Ports (eight in total)	Standard SFP / SFP+ MSA compliant modules supporting 1G and 10G options for copper and fiber Support for 25G Copper and fiber SFP28 modules

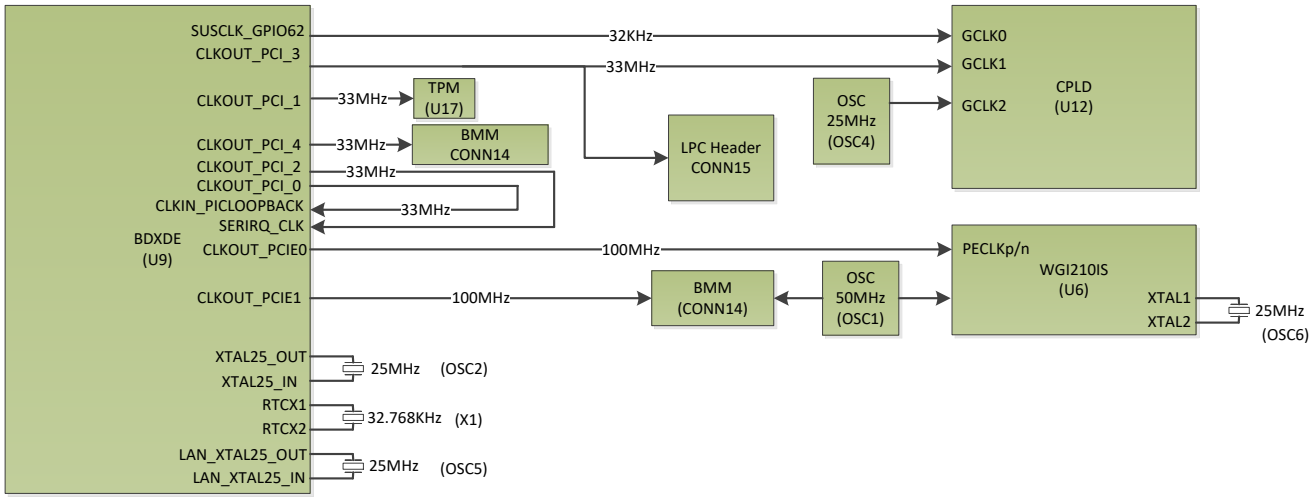
QSFP28 Ports (two in total)	Standard 40Gb QSFP+ modules including but not limited to: 40GBASE-SR4, 40GBASE-LR4, 40GBASE-ER, AOC Cables
QSFP28 Ports	Standard DAC cables including but not limited to: Passive cables up to 7m, QSFP<> QSFP DAC, QSFP<>SFP+ DAC Breakout
QSFP28 Ports	Support for all standards complaint QSFP28 XCVRS including but not limited to 100GBASE-SR4, 100GBASE-LR4
QSFP28 Ports	Standard DAC cables including but not limited to: Passive cables up to 3m, QSFP28<> QSFP28 DAC, QSFP28<>SFP28 DAC Breakout

Rear View

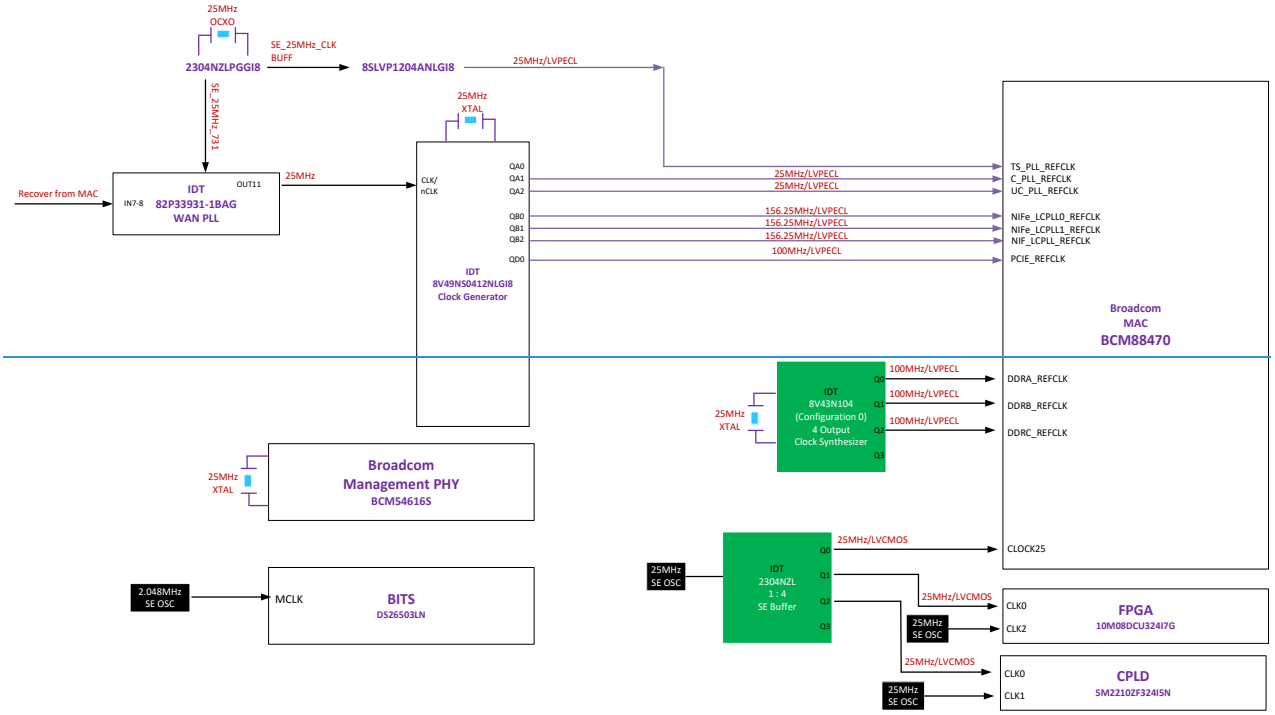
The rear view of the AS7316-26X includes the following key components:

- Five(4+1) redundant hot swappable fan modules
  - LED per fan module to indicate status
  - Color coding to indicate airflow direction
- Chassis Grounding Lug

Clock Tree

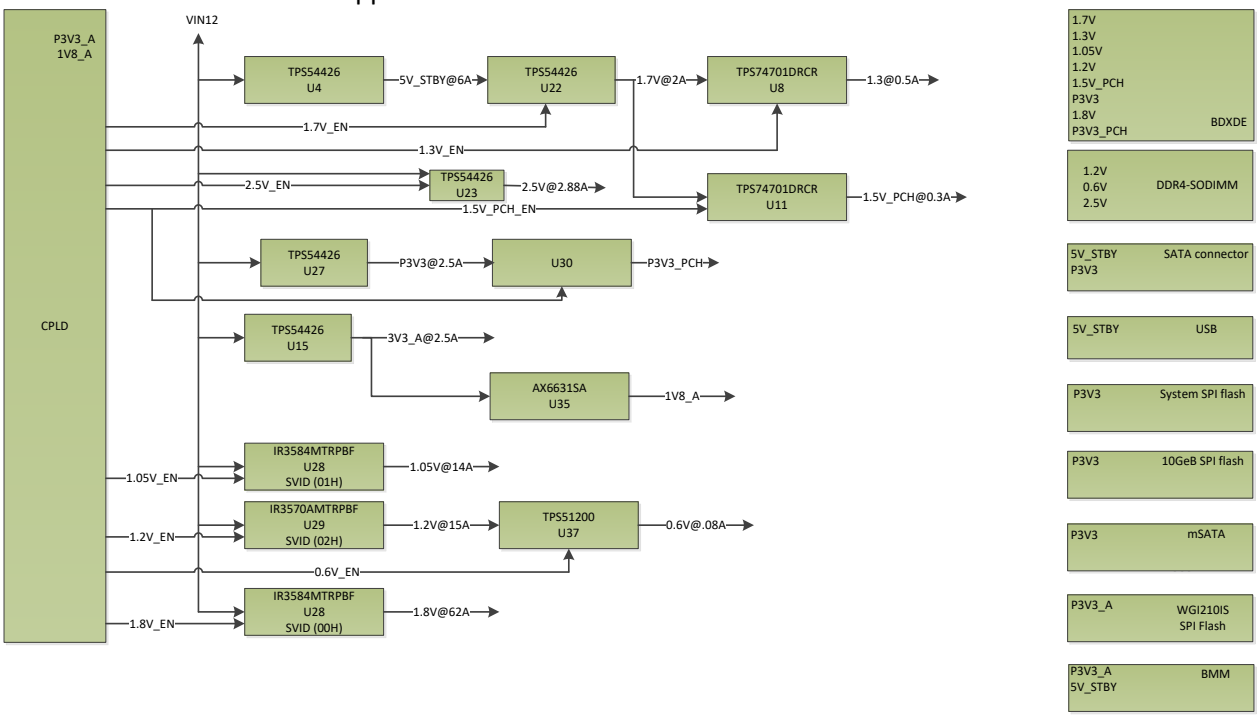


CPU Clock Tree

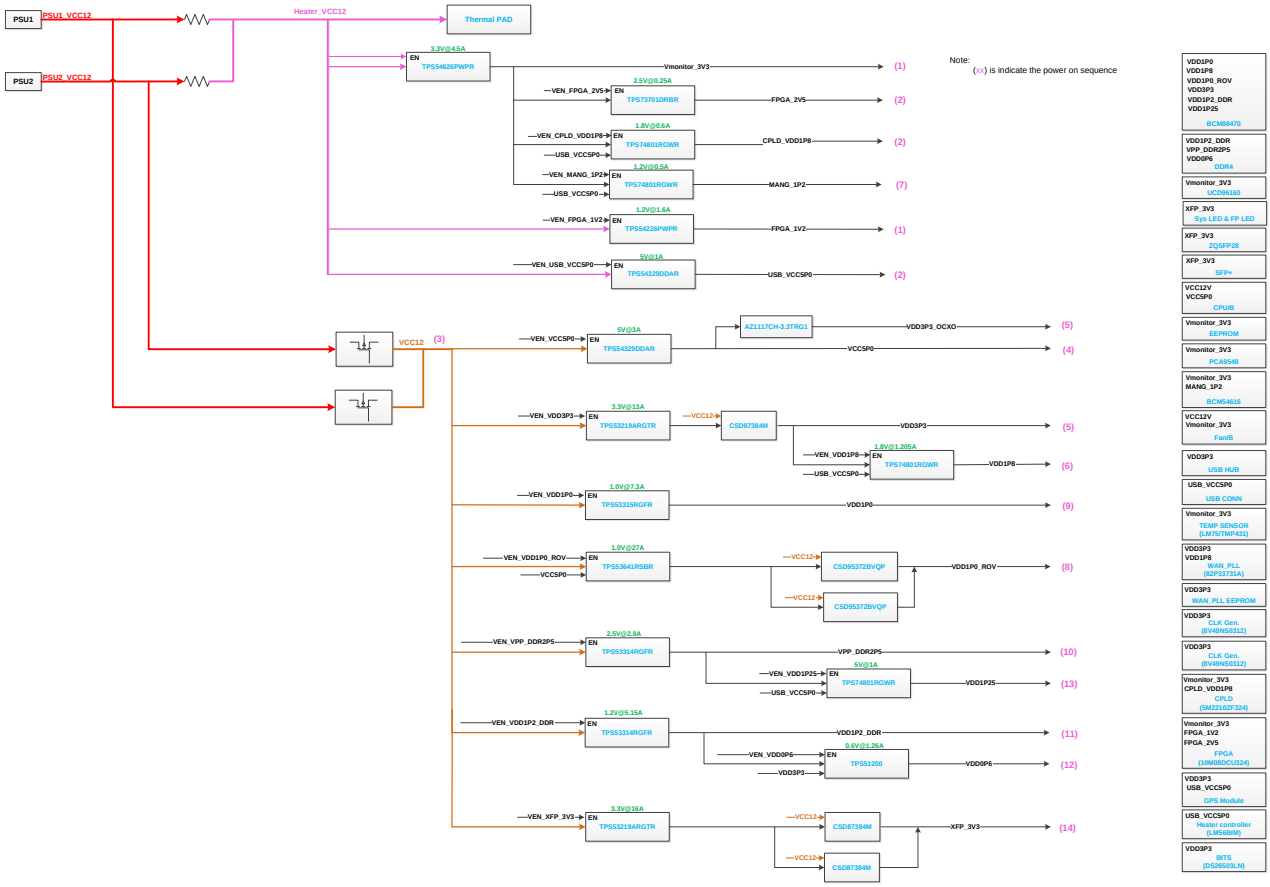


Power Tree

The power monitor and sequence controlled by the CPLD and there are three regulators that SVID interface need to support VR12.5 of Intel.

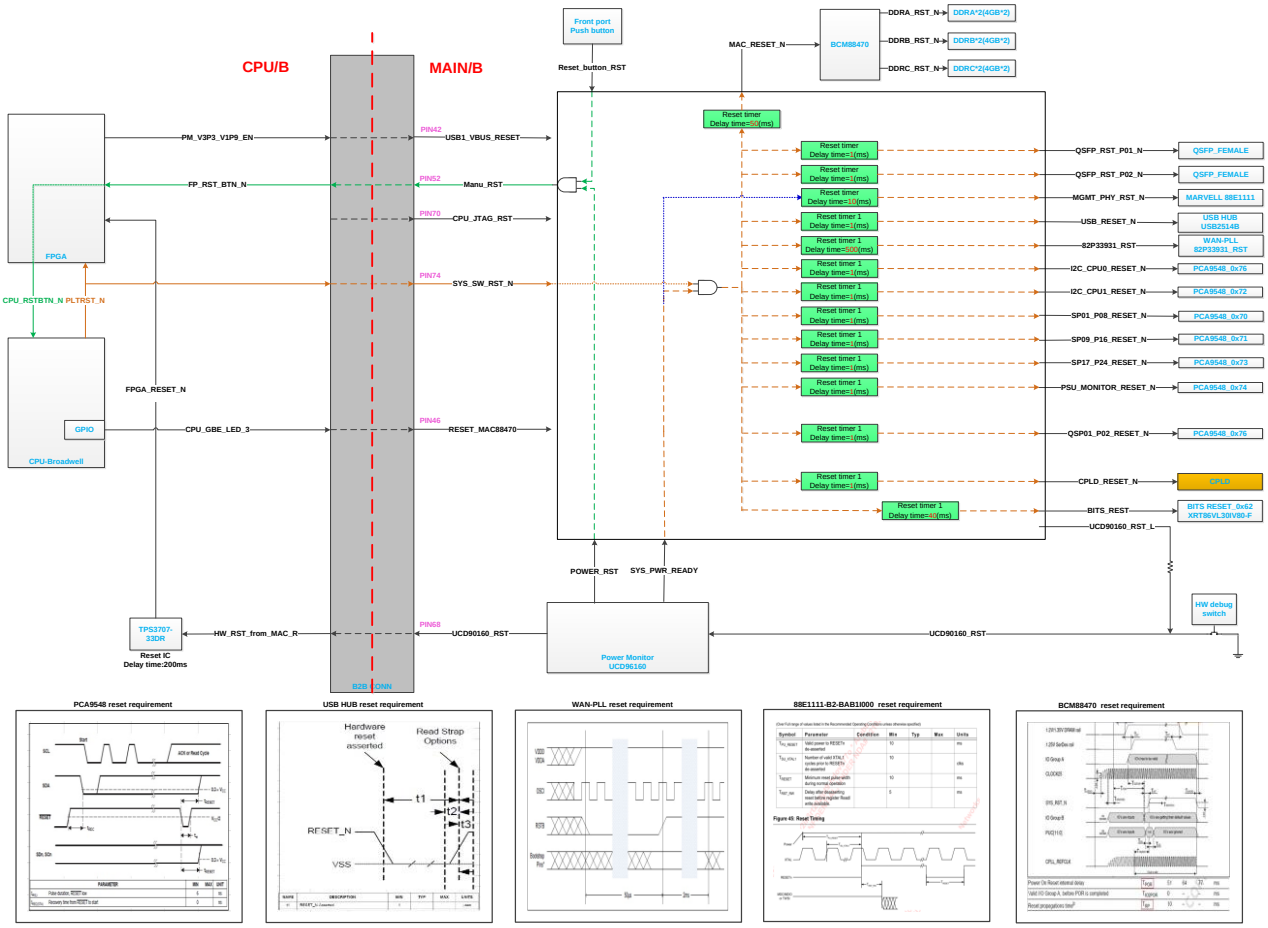


CPU Power Tree



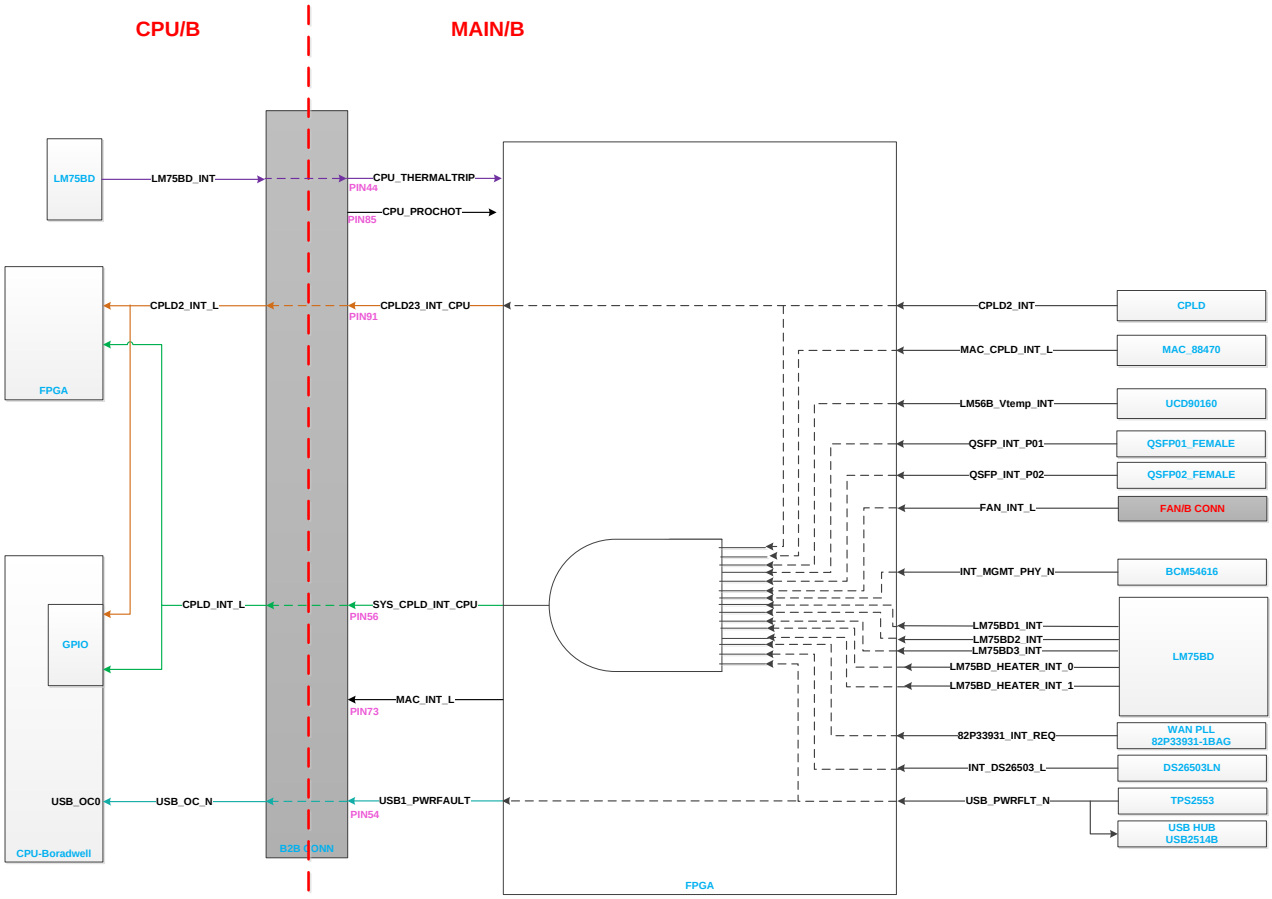
Mainboard Power Tree

Reset Tree



Reset Tree

Interrupt Tree



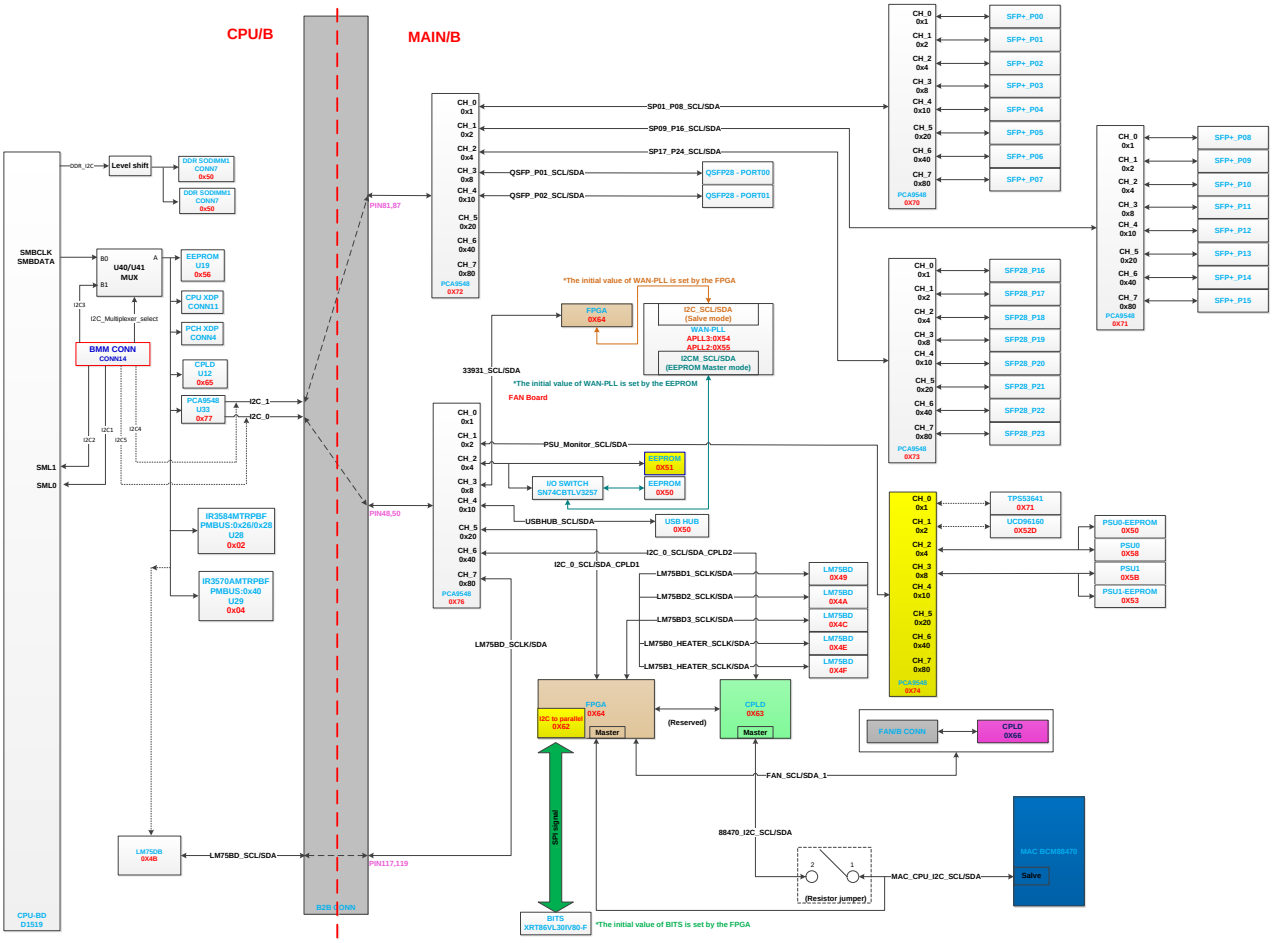
Main Board Interrupt Tree

I2C/SMBus Architecture

The SMbus from BDXDE can access the CPU board and main board device via SMBUS0.

The LM75 (0x4B) is accessed by the CPLD on main board.

The I2C information from DDR SPD EEPROM needs to read via another SMbus only used for DDR SPD.



I2C Architecture

1.1.1. Power-On Reset

The cores and uncore support the following reset types. Note PWRGOOD_CPU is driven by the PCH.

Cold reset is the first time when the platform asserts PWRGOOD_CPU and asserts RESET_CPU_N to the uncore. The platform has to wait for the Base Clock (BCLK) and the power to be stable before asserting PWRGOOD_CPU. This results in reset of all the states in the processor, including the sticky state that is preserved on the other resets. PLLs come up, I/O (DMI2, uncore PCI Express, and DDR) links undergo initialization and calibration. Components in fixed and variable power planes are brought up. Ring, router, SAD, and various lookup tables in the core/Cbo are initialized. Once the

uncore initialization has completed, then the power is enabled to the cores and cores are brought out of reset. BIOS is fetched from the PCH.

Warm reset is typically a platform wide event and is indicated by assertion and deassertion of the RESET_CPU_N signal on the socket while PWRGOOD_CPU remains asserted. This reset preserves the error log state and machine check bank states for use by platform debug. The warm reset preserves the error log state and machine check bank states for use by platform for post error event analysis. To maintain the DDR memory attached to the processor self refresh and sticky registers remain valid through out a warm reset, the "Reset_warn" message must complete by the processor. The "Reset_warn" is a message that gets issued from the PCH to all sockets prior to warm reset. BIOS will need to program the FlexRatioMSR/CSR in each socket and invoke the Warm Reset to the platform.

The reset flow is divided into the following 5 phases.

- **Phase 0**: Expectations from the platform (before assertion of PWRGOOD_CPU)
  - Initially PWRGOOD_CPU signal is deasserted and RESET_CPU_N is asserted to the socket. PWRGOOD_CPU cannot deassert until RESET_CPU_N is asserted.
  - PWRGOOD_CPU must be asserted no sooner than 2 ms after the IVR Vccin supply has fully ramped-up.
  - Vccioin may be brought up before Vccin for IVR is brought up if not at the same time. Vccioin is intended to source the PECI IO.
  - The PWRGOOD_CPU and RESET_CPU_N signals have "clean" edges.
  - The reference clock (BCLK) is stable.
  - All external power rails have ramped as follows: Vccin, Vccioin, VCCD are up and stable at their nominal values
  - Assert PWRGOOD_CPU (RESET_CPU_N still asserted) only after 2 msec of Vccin, Vccioin and VCCD at tolerance.
  - After the power rails are up and stable for 2 msec and reference clocks are stable, platform asserts PWRGOOD_CPU and continues to assert RESET_CPU_N signal to the socket.
  - PWRGOOD_CPU remains asserted as long as Vccin, Vccioin and VCCD remain stable.
  - No power sequencing between Vccin and VCCD is required.

- **Phase 1**: PCU bring-up
  - Phase 1a: Activity Leading to PCU Start-up
    - Assertion of PWRGOOD_CPU (the trigger to move from the end Phase 0 to the start of Phase 1a).
    - Processor starts a timer (using BCLK) for determinism interval.
    - The PECI and SVID interfaces are held in reset until IVR asserts its power good signal.
    - The PCU PLL is enabled.
  - Phase 1b: Pcode Controlled Preparing for Broad uncore Bring-Up
    - Starting at the sub-phase, all steps should be synchronous.
    - PCU micro controller comes out of reset to start reset pcode execution. This is the planned "re-entry" point for Warm Reset processing.
    - Early reset pcode determines that it is at the start of Phase 1b.
    - Pcode brings the rest of the PCU hardware out of reset.
    - Pcode determines the boot config.
    - Pcode issues SVID command to ramp Vccin to 1.8V for cold reset.
    - Pcode reads and compares Vccin MBVR ICCMAX limit (reg 21h) vs its own supported ICCMAX limit:
      - If VR's ICCMAX ≥ supported ICCMAX then bootup continues.
      - If VR's ICCMAX < supported ICCMAX then bootup halts and system shuts down. MSR 411h IA32_MC4_STATUS logs Error code 0x1e - MCA_VR_ICC_MAX_LESS_THAN_FUSED_ICC_MAX in field MSEC_FW.
    - Pcode sequences uncore non-boot IVRs to ramp up.
    - Pcode signals uncore power good to IIO, IMC.
    - Delivery of the uncore power good signals defines the transition from the end of phase 1b to the beginning of phase 1c.

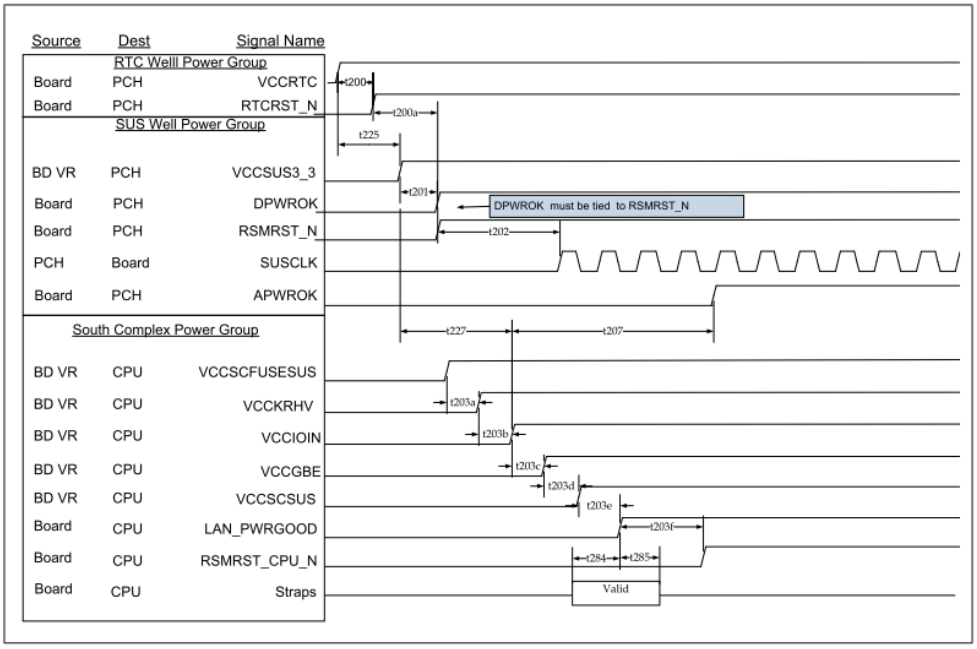
- Phase 1c: PLL locking and IO Calibration
  - Pcode initiates thermal sensors.
  - Pcode locks PLLs in the following order: IIO, and IMC.
  - Pcode instructs the ring PLLs to start locking.
  - RESET_CPU_N signal is deasserted.
  - De-assertion of RESET_CPU_N signal will bring PCU out of reset and signifies the transition from the end of Phase 1c to the beginning of Phase 2.

- **Phase 2**: Uncore initialization and core bring up
  - The starting assumptions are:
    - All IVRs except core IVRs have ramped-up and are stable.
    - All PLLs except core PLLs have locked.
    - Phase 2 is entered as a result of de-assertion of external pin RESET_CPU_N.
    - Boot mode related straps have been sampled and are available.
    - Some IO link calibration have started and may or may not have completed by the start of this phase.
  - In this phase
    - PCU comes out of reset again and again determines the reset type.
    - Reset is deasserted to the ring units (HA, Cbo, IIO).
    - Reset is de-asserted to System Agents (IMC, IIO).
    - Pcode initializes the ring stops
    - Pcode performs boot mode processing based on straps. Set the advertised firmware, IO, and Intel TXT agent bits appropriately.
    - Pcode services DMI2 handshake protocol. If DMI2 links are used in DMI2 mode, pcode checks if the links have trained to L0. If it's the legacy socket, and if DMI2 links does not reach L0 within 3-4 ms, pcode executes error flow.
    - Pcode determines number of cores, slices and st/mt-threading for the core. In this step pcode also takes into account number of BIOS-disabled cores. Pcode determines whether BIST should be executed. BIST is executed if BIST Strap is set or requested.
    - Pcode programs the logical ids and switches from physical to logical mode.
    - LLC reset and configuration.
    - If it's not service processor boot mode, pcode waits for links to get to parameter exchange.
    - Pcode releases links to get to Normal operation (i.e. L0)
    - Pcode sets core Cstate to C1

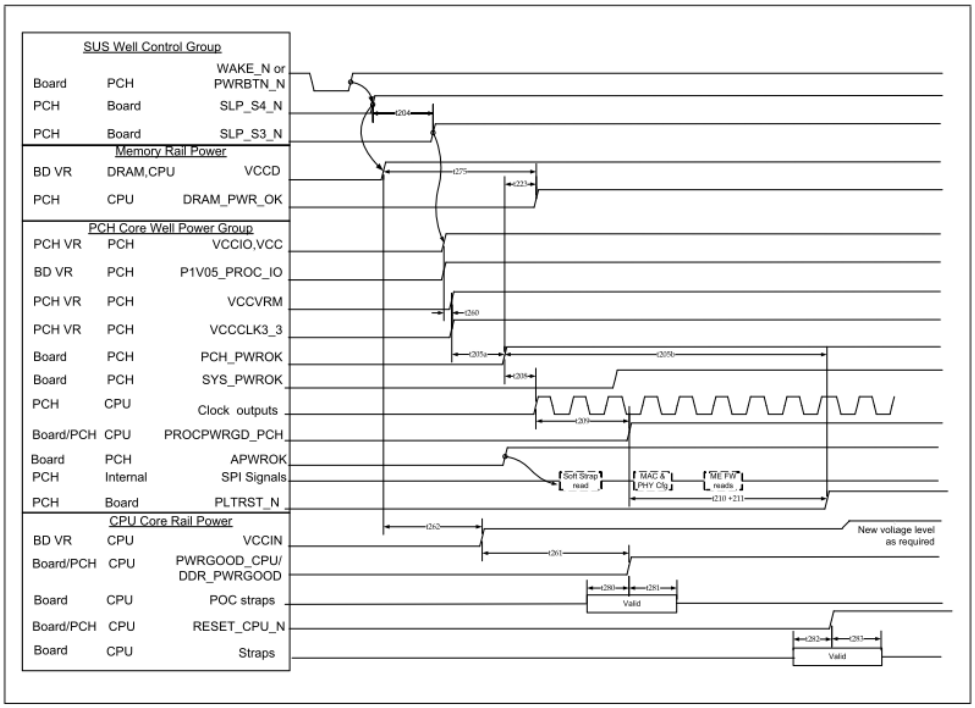
- **Phase 3**: Reset execution (from core reset to fetch boot vector)
  - The starting assumptions are:
    - Before this phase starts, following information is provided to the core: APIC-ID, whether it's the BSP, SMT enable/disable, reset type (cold, warm, C6 exit).
    - Uncore necessary to the get to the BIOS and Intel TXT Address space is fully initialized.
  - In this phase:
    - Initialize core's internal structures, arrays, microarchitectural and architectural state.

- Execute MLC BIST if BIST enabled.
- Initialize uncore.
- Read LLC BIST results from the uncore and report it in the EAX register.
- Report LLC and MLC BIST results.
- The core and thread selected as package BSP fetches BIOS or goes to “Wait-for-SIPI” state
- The end assumption is there is at least one thread that was designated as package BSP.

➢ **Phase 4**: BIOS execution



Power Sequencing Diagram G3 with RTC loss to S5



Power Sequencing Diagram S5 to S0

- BIOS has two flash memories (Flash 1/U1 and Flash 2/U31) to boot up from, the boot up sequence is same as phase 4.
- The relation of reset sequence and power on sequence:
  This relation can be described from different boot status.
  - Cold boot: When turning on the system after it has been powered off, the power on and reset sequence will be restarted.
  - Warm boot: When restarting the system without interrupting power, the power on sequence do not restart. Reset sequence differs from power on sequence.

1.1.2. PCH Strap pin definition

Strap pin	Description	Default Value/Setting
SATA1GP/ GPIO19	This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap. Bit11 Bit 10 Boot BIOS Destination 0 1 Reserved 1 0 Reserved 1 1 SPI (default) 0 0 LPC	1
GPIO51	This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.	1
SATA3GP /GPIO37	0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).	0
MFG_MODE_STRAP	0 = Enable security measures defined in the Flash Descriptor. 1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.	0
INTVRMEN	0 = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). It should not pull the strap low. 1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left as No Connect.	1
GPIO62 / SUSCLK	0 = Disable PLL On-Die voltage regulator. 1 = Enable PLL On-Die voltage regulator.	1

DSWODVREN	0 = Disable Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This mode is only supported for testing environments. 1 = Enable DSW 3.3 V-to-1.05 V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards.	1
SPKR	0 = Disable “No Reboot” mode. 1 = Enable “No Reboot” mode (integrated PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.	
SATA2GP/GPIO36	0 = SoC RX is terminated to VSS. Grangeville platform only supports SoC Rx terminated to VSS. 1 = SoC RX is terminated to VCC/2.	0
GPIO33	0 = SoC TX is terminated to VSS. Grangeville platform only supports SoC Tx terminated to VSS 1 = SoC TX is terminated to VCC/2.	0
GPIO53	0 = SoC is in AC-coupling mode. Grangeville platform only supports AC-coupling mode. 1 = SoC is in DC-coupling mode.	0
GPIO55	0 = Enable “Top Swap” mode. This inverts an address on access to SPI and firmware hub, so the processor believes its fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64 KB blocks in the FWH or the appropriate address lines (A16, A17, A18, A19, or A20) as selected in Top-Swap Block size soft strap (handled through FITc. 1 = Disable “Top Swap” mode.	1
GPIO8	This pin must not be driven low until after rising edge of RSMRST_N.	1
GPIO44	This pin must not be driven low until after rising edge of RSMRST_N.	1
GPIO46	This pin must not be driven low until after rising edge of RSMRST_N.	1
BIST_ENABLE	Build-in Self Test (BIST) enable strap: 0 = BIST Disable 1 = BIST Enable	0
BMCINIT	Integrated Service Processor Boot Mode Selection: 0 = Integrated Service Processor Boot Mode Disabled. 1 = Integrated Service Processor Boot Mode Enable	1
TXT_PLTEN	0 = The platform is not Intel TXT enabled.	0

	1 = Default. The platform is Intel TXT enabled.	
TXT_AGENT	0 = Default. The SoC is not the Intel TXT Agent. 1 = The SoC is the Intel TXT Agent.	0
SAFE_MODE_BOOT	0 = Safe Mode Boot Disabled 1 = Safe Mode Boot Enabled	1
DEBUG_EN_N	0 = Debug Mode 1 = Normal Mode	XDP_PRESENT_N
DDR3_4_STRAP	Select between DDR4 and DDR3 0 = DDR3, it requires <1K ohm pull down in order to out drive the internal pull up. 1= DDR4 (Default)	1
PECI0 ; PECI1 ; PECI2	In micro-server design space, there will be multiple sockets that share a PECI bus. However these sockets are effectively independent agents. The PECI IDs are used as straps to identify which socket is which in order for PECI bus to work.	000
LAN_MDIO_DIR_CTL_0; LAN_MDIO_DIR_CTL_1	00 = Both LAN ports are disabled. Note: In this mode manageability is not functional and must not be enabled in NVM control word 1. 01 = Port 1 is disabled. Port 0 is enabled. 10 = Reserved 11 = Both Port 0 and 1 are enabled. Recommend 5.1K ohm pull up to VCCIOIN or 5.1K ohm pull down to GND.	11
RSVD12_AJ67	This pin should have a 5.1K ohm pull down to GND.	0
RSVD11_AG67	This pin should have a 5.1K ohm pull down to GND.	0
RSVD10_AN78	This pin should have a 5.1K ohm pull down to GND.	0
RSVD09_AC64	This pin should have a 5.1K ohm pull down to GND.	0
SERIRQ_DIR	Recommend 5.1k ohm pull up to VCCIOIN.	1
UART_TXD[0]	Recommend 5.1k ohm pull down to GND.	0
UART_TXD[1]	Controls the security attributes on the NVM - for pre-production usage only. 0 = Disable NVM Security (Default) 1 = Security Enabled Recommend 5.1K ohm pull down to GND.	0
LAN_NCSI_RXD0	Recommend 5.1K ohm pull up to VCCIOIN.	1
LAN_NCSI_RXD1	Enable/Disable manageability traffic: 0 = LAN available in S5 for WoL (Default) 1 = LAN not available in S5. Manageability is	0

	disabled. Recommend 5.1K ohm pull down to GND.	
LAN_NCSI_ARB_OUT	Selects SVID VR Operating Mode 1 - VCCSCSUS, P1V05_PCH, VCCGBE, VCCIOIN are combined into one SVID controlled supply. 0 - Separate SVID controllers (default).	1
RSVD84	49.9Ω 1% to GND	0
RSVD93	1k - 5.1kΩ to GND	0
RSVD94	1k - 5.1kΩ to GND	0
RSVD00	1k - 5.1kΩ to VCC3_3	1
RSVD18	1k - 5.1kΩ to GND	0
RSVD16	1k - 5.1kΩ to GND	0
RSVD17	1k - 5.1kΩ to GND	0
RSVD21	1k - 5.1kΩ to GND	0
NCTF/TP	1k - 5.1kΩ to VCC3_3	1

Table 1 PCH Strap definitions

1.2. Memory Mapping

Broadwell-DE SoC contains registers that are located in the processor I/O space and memory space and sets of PCI configuration registers that are located in PCI configuration space. This chapter describes Broadwell-DE SoC I/O and memory maps at the register-set level. Register access is also described.

Bus:Device:Function	Function Description
Bus0:Device31:Function0	LPC controller
Bus0:Device31:Function2	SATA controller #1
Bus0:Device31:Function3	SMBus controller
Bus0:Device31:Function5	SATA controller#2
Bus0:Device31:Function6	Thermal subsystem
Bus0:Device29:Function0	USB EHCI controller#1
Bus0:Device28:Function0	PCI-e port1
Bus0:Device28:Function1	PCI-e port2
Bus0:Device28:Function2	PCI-e port3
Bus0:Device28:Function3	PCI-e port4
Bus0:Device28:Function4	PCI-e port5
Bus0:Device28:Function5	PCI-e port6
Bus0:Device28:Function6	PCI-e port7
Bus0:Device28:Function7	PCI-e port8
Bus0:Device25:Function0	Gigabit Ethernet controller
Bus0:Device22:Function0	Intel management engine interface#1
Bus0:Device22:Function1	Intel management engine interface#2
Bus0:Device22:Function2	IDE-R
Bus0:Device22:Function3	KT
Bus0:Device20:Function0	xHCI controller

Table 2 PCI devices and functions

I/O Address	Read Target	Write Target	Internal Unit
00h-08h	DMA controller	DMA controller	DMA
09h-0Eh	reserved	DMA controller	DMA
0Fh	DMA controller	DMA controller	DMA
10h-18h	DMA controller	DMA controller	DMA
19h-1Eh	reserved	DMA controller	DMA
1Fh	DMA controller	DMA controller	DMA
20h-21h	Interrupt controller	Interrupt controller	interrupt
24h-25h	Interrupt controller	Interrupt controller	interrupt
28h-29h	Interrupt controller	Interrupt controller	interrupt
2Ch-2Dh	Interrupt controller	Interrupt controller	interrupt
2Eh-2Fh	LPC SIO	LPC SIO	Forwarded to LPC
30h-31h	Interrupt controller	Interrupt controller	interrupt
34h-35h	Interrupt controller	Interrupt controller	interrupt
38h-39h	Interrupt controller	Interrupt controller	interrupt
3Ch-3Dh	Interrupt controller	Interrupt controller	interrupt
40h-42h	Timer/Counter	Timer/Counter	PIT
43h	reserved	Timer/Counter	PIT
4Eh-4Fh	LPC SIO	LPC SIO	Forwarded to LPC
50h-52h	Timer/Counter	Timer/Counter	PIT
53h	reserved	Timer/Counter	PIT
60h	microcontroller	microcontroller	Forwarded to LPC
61h	NMI controller	NMI controller	Processor I/F
62h	microcontroller	microcontroller	Forwarded to LPC
64h	microcontroller	microcontroller	Forwarded to LPC
66h	microcontroller	microcontroller	Forwarded to LPC
70h	reserved	NMI and RTC controller	RTC
71h	RTC controller	RTC controller	RTC
72h	RTC controller	NMI and RTC controller	RTC
73h	RTC controller	RTC controller	RTC
74h	RTC controller	NMI and RTC controller	RTC
75h	RTC controller	RTC controller	RTC
76h	RTC controller	NMI and RTC controller	RTC
77h	RTC controller	RTC controller	RTC
80h	DMA controller, LPC, PCI or PCIe	DMA controller, LPC, PCI or PCIe	DMA
81h-83h	DMA controller	DMA controller	DMA
84h-86h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
87h	DMA controller	DMA controller	DMA
88h	DMA controller	DMA controller, LPC, PCI or PCIe	DMA
89h-8Bh	DMA controller	DMA controller	DMA
8Ch-8Eh	DMA controller	DMA controller, LPC, PCI or PCIe	DMA

8Fh	DMA controller	DMA controller	DMA
90h-91h	DMA controller	DMA controller	DMA
92h	Reset generator	Reset generator	Processor I/F
93h-9Fh	DMA controller	DMA controller	DMA
A0h-A1h	Interrupt controller	Interrupt controller	interrupt
A4h-A5h	Interrupt controller	Interrupt controller	interrupt
A8h-A9h	Interrupt controller	Interrupt controller	interrupt
ACh-ADh	Interrupt controller	Interrupt controller	interrupt
B0h-B1h	Interrupt controller	Interrupt controller	interrupt
B2h-B3h	Power management	Power management	Power management
B4h-B5h	Interrupt controller	Interrupt controller	interrupt
B8h-B9h	Interrupt controller	Interrupt controller	interrupt
BCh-BDh	Interrupt controller	Interrupt controller	interrupt
C0h-D1h	DMA controller	DMA controller	DMA
D2h-DDh	reserved	DMA controller	DMA
DEh-DFh	DMA controller	DMA controller	DMA
F0h	Ferr#/interrupt controller	Ferr#/interrupt controller	Processor I/F
170h-177h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
1F0h-1F7h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
200h-207h	Gameport low	Gameport low	Forwarded to LPC
208h-20Fh	Gameport high	Gameport high	Forwarded to LPC
376h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
3F6h	SATA controller, PCI, or PCIe	SATA controller, PCI, or PCIe	SATA
4D0h-4D1h	Interrupt controller	Interrupt controller	interrupt
CF9h	Reset generator	Reset generator	Processor I/F

Fixed I/O ranges decoded by Broadwell-DE

Range name	Mappable	Size (bytes)	Target
ACPI	Anywhere in 64KB I/O space	64	Power management
IDE bus master	Anywhere in 64KB I/O space	1. 16 or 32 2. 16	1. SATA host controller #1, #2 2. IDE-R
Native IDE command	Anywhere in 64KB I/O space	8	1. SATA host controller #1, #2 2. IDE-R
Native IDE control	Anywhere in 64KB I/O space	4	1. SATA host controller #1, #2 2. IDE-R
SATA index/data pair	Anywhere in 64KB I/O space	16	1. SATA host controller #1, #2 2. IDE-R
SMBus	Anywhere in 64KB I/O space	32	SMB unit
TCO	96 bytes above ACPI base	32	TCO unit
GPIO	Anywhere in 64KB I/O space	128	GPIO unit
Parallel port	3 ranges in 64KB I/O space	8	LPC peripheral
Serial port 1	8 ranges in 64KB I/O space	8	LPC peripheral
Serial port 2	8 ranges in 64KB I/O space	8	LPC peripheral
Floppy disk controller	2 ranges in 64KB I/O space	8	LPC peripheral
LAN	Anywhere in 64KB I/O space	32	LAN unit
LPC generic 1	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 2	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 3	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
LPC generic 4	Anywhere in 64KB I/O space	4 to 256	LPC peripheral
I/O trapping ranges	Anywhere in 64KB I/O space	1 to 256	Trap on backbone
PCI bridge	Anywhere in 64KB I/O space	I/O base/limit	PCI bridge
PCI-E root ports	Anywhere in 64KB I/O space	I/O base/limit	PCI-E root ports 1-8
KT	Anywhere in 64KB I/O space	8	KT

Variable I/O decode ranges

Memory range	target	Dependency/comments
0000 0000h-000D FFFFh 0010 0000h-TOM	Main memory	TOM registers in host controller
000E 0000h-000E FFFFh	LPC or SPI	Bit 6 in BIOS decode enable register is set
000F 0000h-000F FFFFh	LPC or SPI	Bit 7 in BIOS decode enable register is set
FEC_ _000h-FEC_ _040h	IOx APCI inside broadwell-de SoC	_ _ is controlled using APIC range select (ASEL) field and APIC enable (AEN) bit.
FEC1 0000h-FEC1 7FFFh	PCI-E port 1	PCI-E root port 1 I/OxAPIC enable (PAE) set
FEC1 8000h-FEC1 FFFFh	PCI-E port 2	PCI-E root port 2 I/OxAPIC enable (PAE) set
FEC2 0000h-FEC2 7FFFh	PCI-E port 3	PCI-E root port 3 I/OxAPIC enable (PAE) set
FEC2 8000h-FEC2 FFFFh	PCI-E port 4	PCI-E root port 4 I/OxAPIC enable (PAE) set

FEC3 0000h-FEC3 7FFFh	PCI-E port 5	PCI-E root port 5 I/OxAPIC enable (PAE) set
FEC3 8000h-FEC3 FFFFh	PCI-E port 6	PCI-E root port 6 I/OxAPIC enable (PAE) set
FEC4 0000h-FEC4 7FFFh	PCI-E port 7	PCI-E root port 7 I/OxAPIC enable (PAE) set
FEC4 8000h-FEC4 FFFFh	PCI-E port 8	PCI-E root port 8 I/OxAPIC enable (PAE) set
FFC0 0000h-FFC7 FFFFh FF80 0000h- FF87 FFFFh	LPC or SPI (or PCI)	Bit 8 in BIOS decode enable register is set
FFC8 0000h-FFCF FFFFh FF88 0000h- FF8F FFFFh	LPC or SPI (or PCI)	Bit 9 in BIOS decode enable register is set
FFD0 0000h-FFD7 FFFFh FF90 0000h- FF97 FFFFh	LPC or SPI (or PCI)	Bit 10 in BIOS decode enable register is set
FFD8 0000h-FFDF FFFFh FF98 0000h- FF9F FFFFh	LPC or SPI (or PCI)	Bit 11 in BIOS decode enable register is set
FFE0 0000h-FFE7 FFFFh FFA0 0000h- FFA7 FFFFh	LPC or SPI (or PCI)	Bit 12 in BIOS decode enable register is set
FFE8 0000h-FFEF FFFFh FFA8 0000h- FFAF FFFFh	LPC or SPI (or PCI)	Bit 13 in BIOS decode enable register is set
FFF0 0000h-FFF7 FFFFh FFB0 0000h-FFB7 FFFFh	LPC or SPI (or PCI)	Bit 14 in BIOS decode enable register is set
FFF8 0000h–FFFF FFFFh FFB8 0000h–FFBF FFFFh	LPC or SPI (or PCI)	Always enabled. The top two 64KB blocks of this range can be swapped.
FF70 0000h–FF7F FFFFh FF30 0000h–FF3F FFFFh	LPC or SPI (or PCI)	Bit 3 in BIOS Decode Enable register is set
FF60 0000h–FF6F FFFFh FF20 0000h–FF2F FFFFh	LPC or SPI (or PCI)	Bit 2 in BIOS Decode Enable register is set
FF50 0000h–FF5F FFFFh FF10 0000h–FF1F FFFFh	LPC or SPI (or PCI)	Bit 1 in BIOS Decode Enable register is set
FF40 0000h–FF4F FFFFh FF00 0000h–FF0F FFFFh	LPC or SPI (or PCI)	Bit 0 in BIOS Decode Enable register is set
128 KB anywhere in 4 GB range	Integrated LAN Controller	Enable using BAR in D25:F0 (Integrated LAN Controller MBARA)
4 KB anywhere in 4 GB range	Integrated LAN Controller	Enable using BAR in D25:F0 (Integrated LAN Controller MBARB)
1 KB anywhere in 4 GB range	USB EHCI Controller #1	Enable using standard PCI mechanism (D29:F0)
64 KB anywhere in 4 GB range	USB xHCI Controller	Enable using standard PCI mechanism (D20:F0)
FED0 X000h–FED0 X3FFh	High Precision Event Timers	BIOS determines “fixed” location which is one of four, 1-KB ranges where X (in the first column) is 0h, 1h, 2h, or 3h.
FED4 0000h–FED4 FFFFh	TPM on LPC	None
Memory Base/Limit anywhere in 4 GB range	PCI Bridge	Enable using standard PCI mechanism (D30:F0)
Prefetchable Memory Base/Limit anywhere in 64-bit address range	PCI Bridge	Enable using standard PCI mechanism (D30:F0)
64 KB anywhere in 4 GB range	LPC	LPC Generic Memory Range.

		Enable using setting bit[0] of the LPC Generic Memory Range register (D31:F0:offset 98h).
32 Bytes anywhere in 64-bit address range	SMBus	Enable using standard PCI mechanism (D31:F3)
2 KB anywhere above 64 KB to 4 GB range	SATA Host Controller #1	AHCI memory-mapped registers. Enable using standard PCI mechanism (D31:F2)
Memory Base/Limit anywhere in 4 GB range	PCI Express* Root Ports 1-8	Enable using standard PCI mechanism (D28: F 0-7)
Prefetchable Memory Base/Limit anywhere in 64-bit address range	PCI Express Root Ports 1-8	Enable using standard PCI mechanism (D28:F 0-7)
4 KB anywhere in 64-bit address range	Thermal Reporting	Enable using standard PCI mechanism (D31:F6 TBAR/ TBARH)
4 KB anywhere in 64-bit address range	Thermal Reporting	Enable using standard PCI mechanism (D31:F6 TBARB/TBARBH)
16 Bytes anywhere in 64-bit address range	Intel® MEI #1, #2	Enable using standard PCI mechanism (D22:F 1:0)
4 KB anywhere in 4 GB range	KT	Enable using standard PCI mechanism (D22:F3)
16 KB anywhere in 4 GB range	Root Complex Register Block (RCRB)	Enable using setting bit[0] of the Root Complex Base Address register (D31:F0:offset F0h).

Memory decode ranges from processor perspective

1.3. RAM

The Intel Broadwell-DE CPU family can support memory DDR3 and DDR4 that need via strap pin DDR3_4_STRAP to configure which one be supported.

Currently the board supports two DDR4 SODIMM modules with ECC, so the DDR3_4_STRAP should be pull to high.

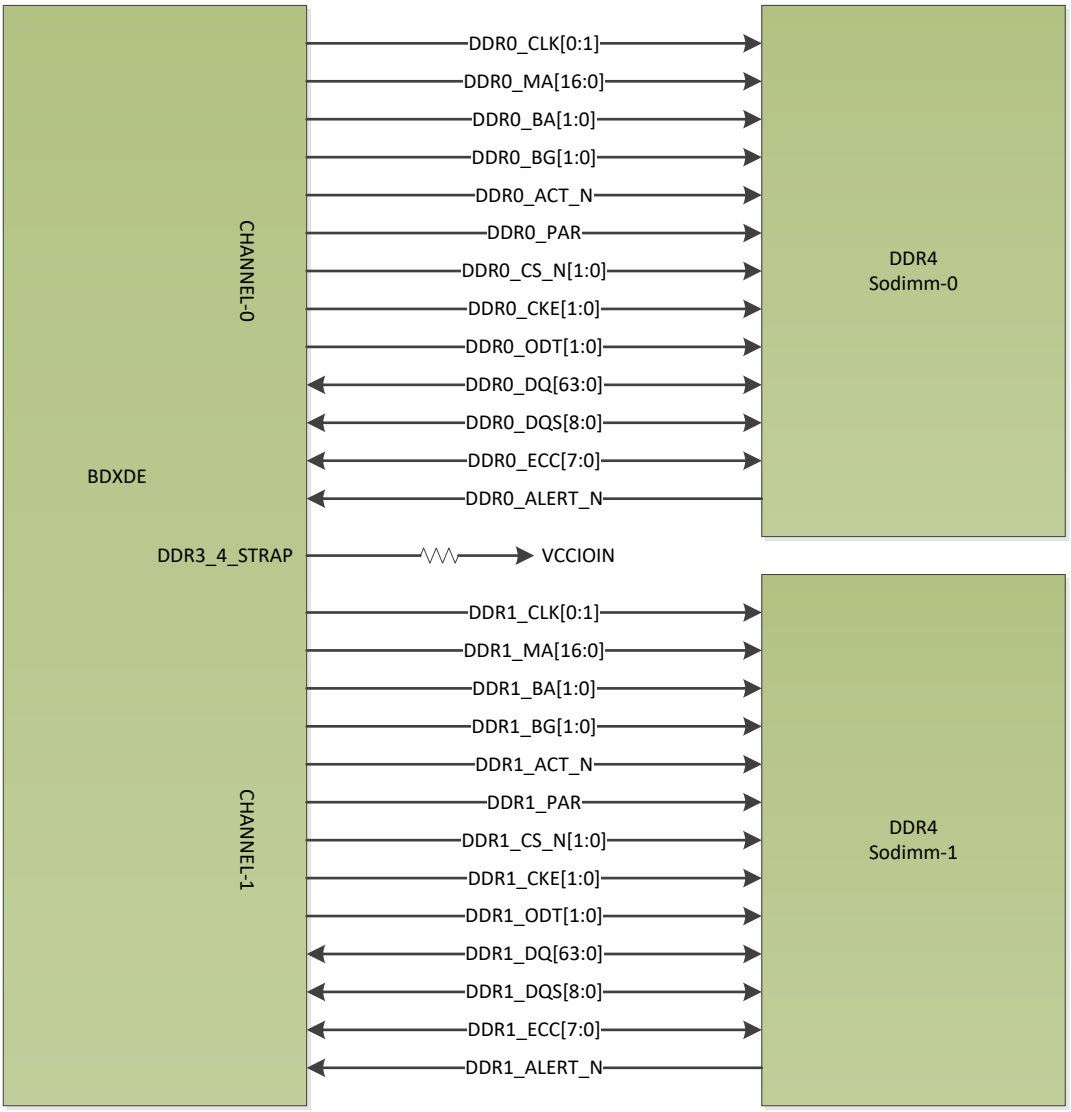


Figure 3 RAM Connection

1.4. PCIe

TBD

Figure 4 PCIe Topology TBD

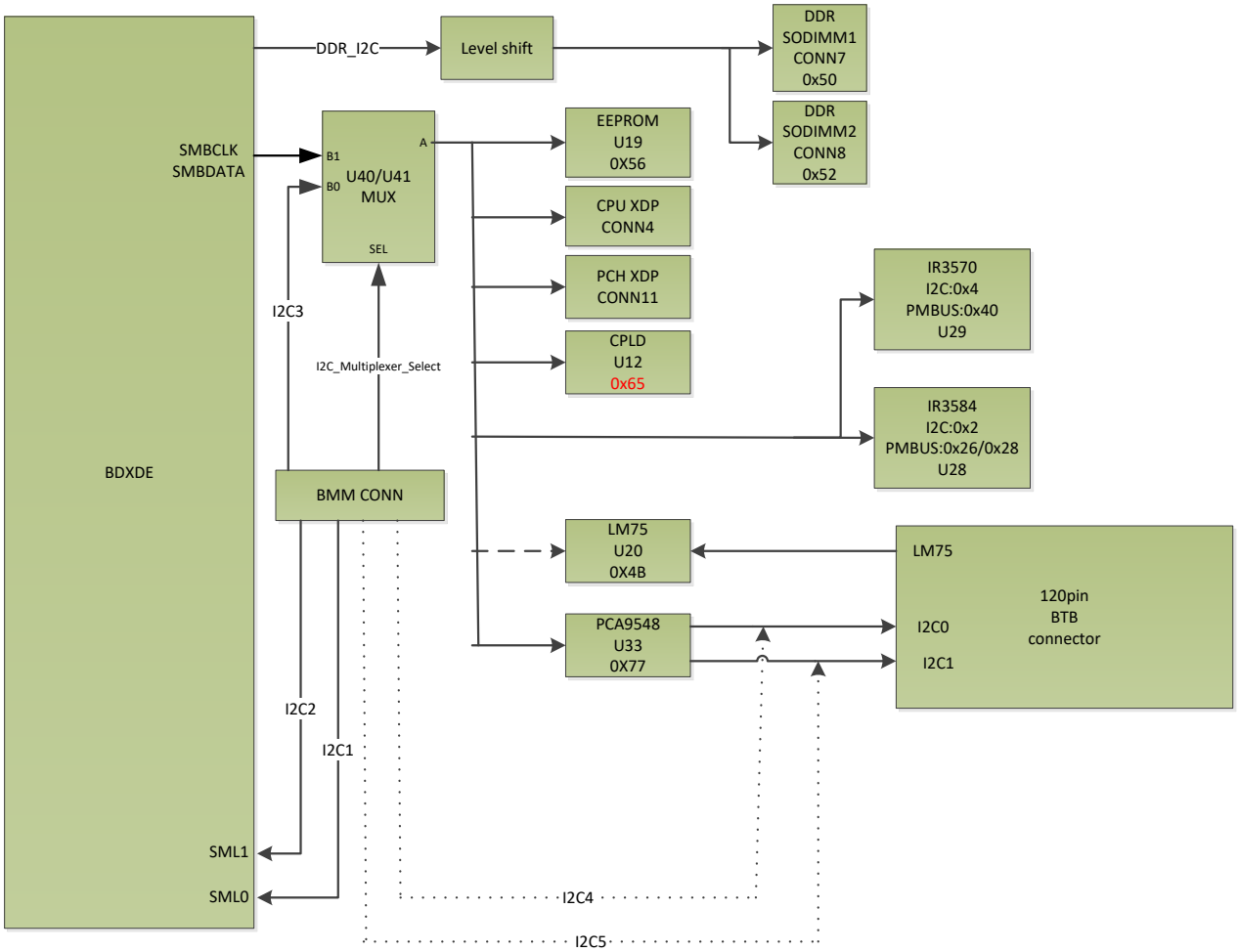
1.5. SMbus

The SMbus from Broadwell-DE can access the CPU board and main board device via SMBUS0.

The U40/U41 multiplexers are used to prevent multi-master issues on the SMBUS.

The BMC module could use the SMBUS when the I2C_multiplexer_select pin is driven from high to low.

In order to prevent the hang-up issue which occurred when the CPU is accessing the SMBUS and BMC module want to take the bus master (I2C_multiplexer_select would be driven low), if the BMC module is installed, BMC would be the master for all SMBUS, CPU would ask BMC for SMBUS information via LPC by IPMI.



Note: I2C[1:5] are from the BMM point of view, not related to the I2C[0:1] through the B2B CONN

SMBUS Connection

Device	I2C address	Note
DDR4 SODIMM 1	0x50	Need to be accessed by DDR_I2C interface
DDR4 SODIMM 2	0x52	Need to be accessed by DDR_I2C interface
LM75	0x4B	Need to be accessed by main board CPLD Not display at SMBus 0.
EEPROM	0x56,0x57	For R1 CPU board
IR3584 (I2C)	0x02	
IR3584 (PMBUS-Loop1)	0x26	
IR3584 (PMBus-Loop2)	0x28	

IR3570 (I2C)	0x4	
IR3570 (PMBus Loop1)	0x42	
PCA9548	0X77	

SMBus 0 Address Table

1.6. UART

There are two UART interfaces of Broadwell-DE CPU, UART0 and UART1.

UART0 is the main system console and connect to main board through 120pin connector and BMC via CPLD, the reason is to support the SOL function when BMC is present.

UART1 is the reserved UART interface and directly connect to BMC module.

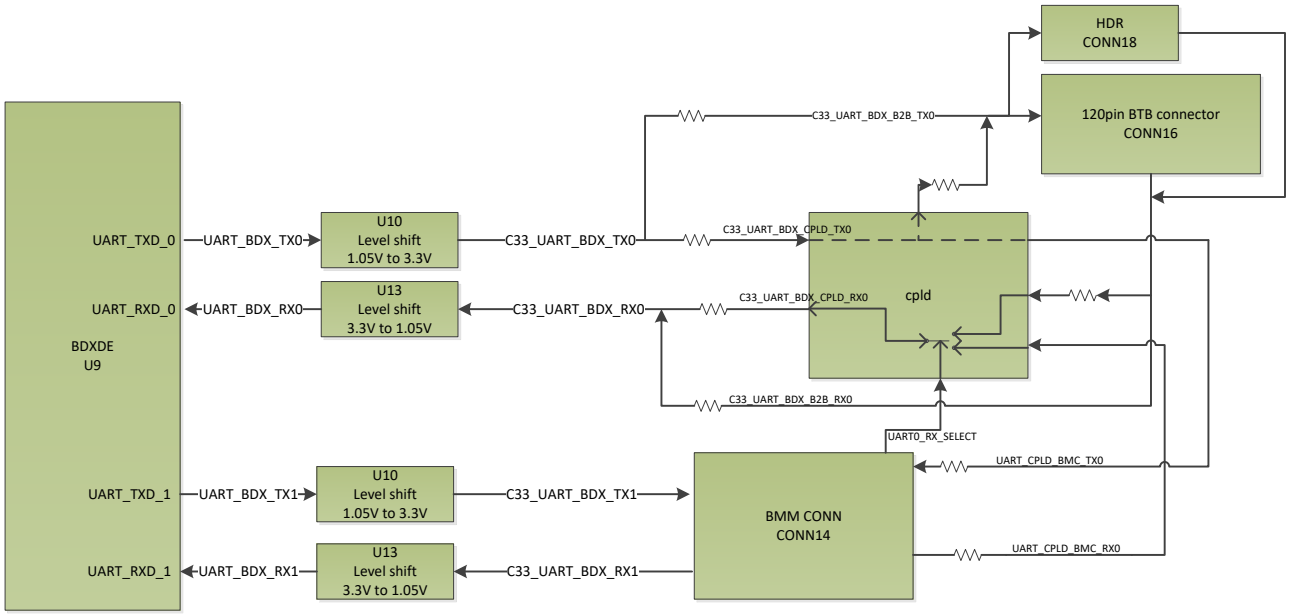


Figure 5 UART Connector

Pin Number	Description
1	VCC
2	TX
3	RX
4	GND

CONN18 PIN ASSIGNMENT

1.7. USB

There are three USB 2.0 interfaces in the project.

- The USB-0 via the 120pins BTB connector to switch board is for chassis USB connector.
- The USB-1 is for debug function.
- The USB-3 is connected to BMC module for vMEDIA function.

USB Connection

1.8. SATA

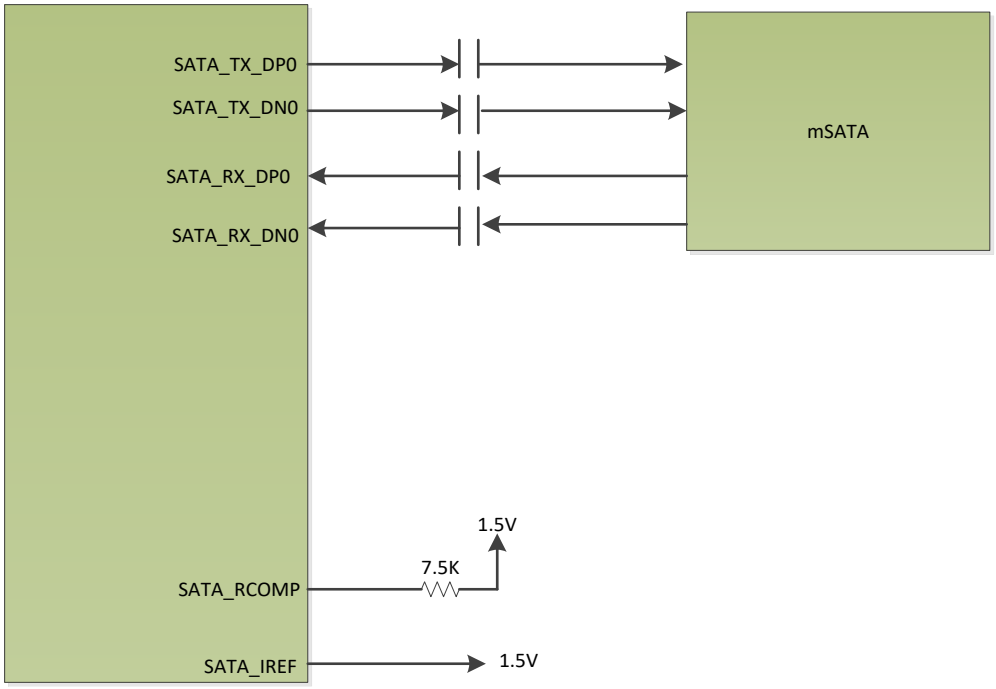
The CPU board supports 1 SATA SSD devices via SATA 3.0 interface.

- SATA 3.0 CH0 support mSATA SSD module.

The following table shows the mSATA dimension and size.

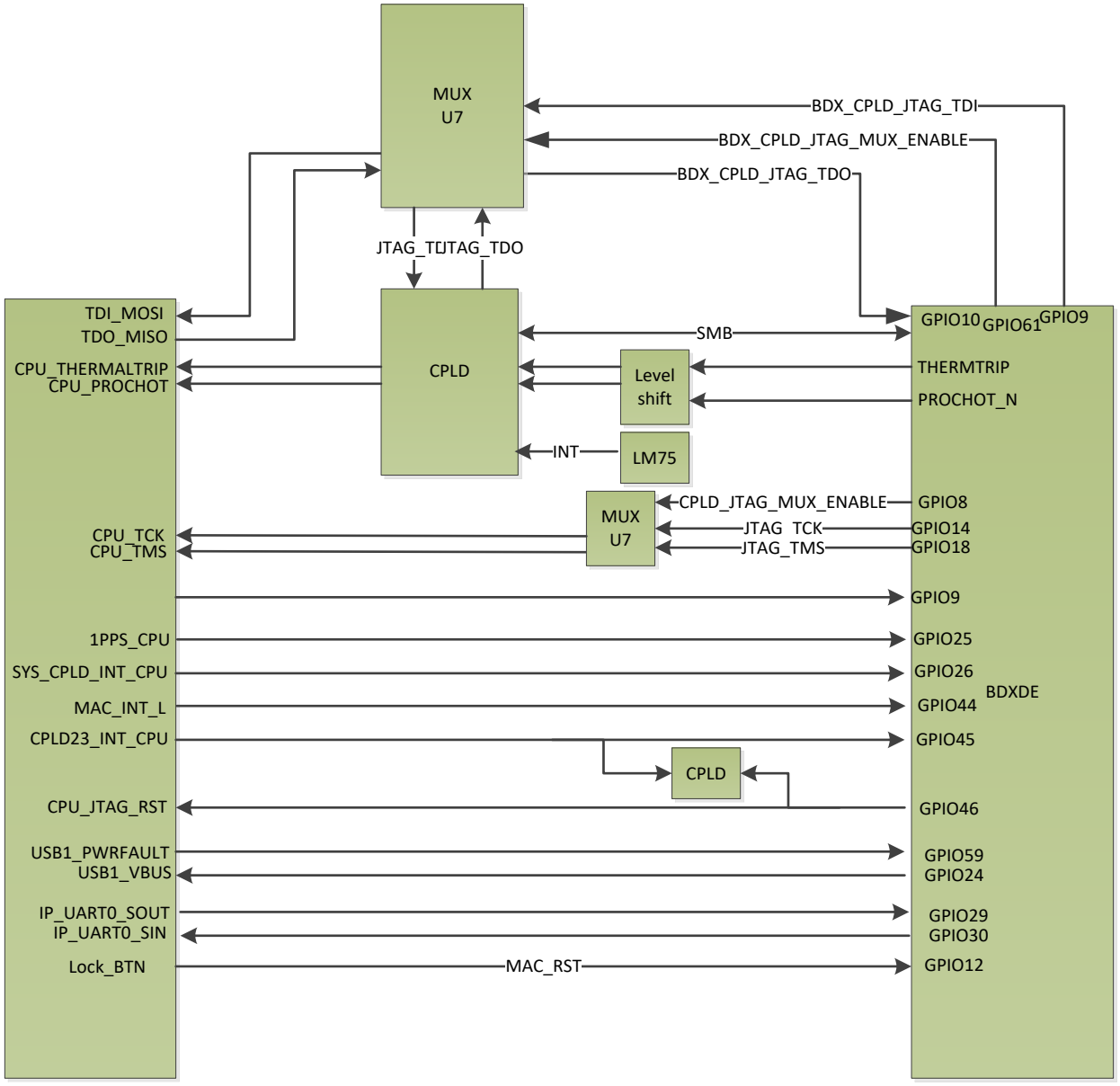
Type	Dimension	Capacity
mSATA SSD	50.8mm x 29.85mm x 4.0mm	16GB~512GB (default)

SATA SSD Module Table



SATA Connection

1.9. GPIO



GPIO Connection

The following table is the GPIO function description of BDXDE CPU.

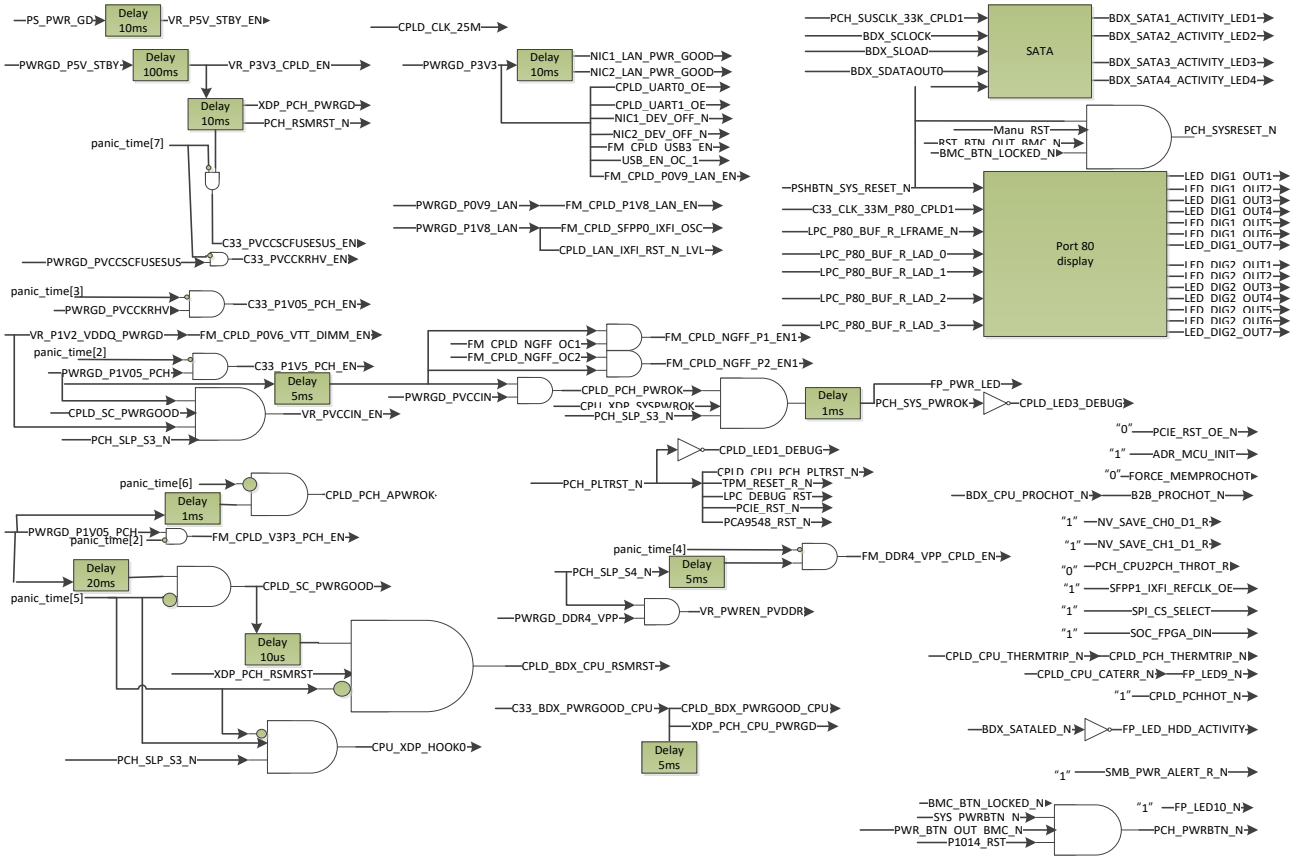
Pin name	GPIO_USE_SEL 1: GPIO 0: Native	GPIO_IO_SEL 1: input 0: output	Function
GPIO0	0	X	BMBUSY#
GPIO1	1	0	Watch dog event clear indicator
GPIO2	0	X	NC
GPIO3	0	X	NC
GPIO4	1	1	CPU to PCH Throttle event interrupt
GPIO5	0	X	NC
GPIO6	1	0	JTAG enable, enable JTAG multiplexer to update CPLD code from CPU. 1: enable the JTAG multiplexer 0: disable the JTAG multiplexer
GPIO7	0	X	NC
GPIO8	1	0	JTAG Multiplexer select, which select the JTAG signals from CPU would go to CPLD or main board 1: to CPLD (default) 0: to Main board
GPIO9	1	0	XDP_NOA5_PCH/ BDX_CPLD_JTAG_TDI When configure to be BDX_CPLD_JTAG_TDI, which is CPU JTAG output
GPIO10	1	1	XDP_NOA6_PCH/ BDX_CPLD_JTAG_TDO When this pin configure to BDX_CPLD_JTAG_TDO , which is CPU JTAG input
GPIO11	0	X	SMBALERT#
GPIO12	1	0	Reset MAC, to do the sleep function.
GPIO14	1	0	XDP_NOA7_PCH/ BDX_CPLD_JTAG_TCK

GPIO15	1	0	SOC_FPGA_CLK
GPIO16	1	0	FM_THROTTLE_PCH_N/ FM_THROTTLE_N
GPIO17	1	1	BMC present detect
GPIO18	1	0	XDP_NOA14_PCH/ BDX_CPLD_JTAG_TMS
GPIO19	1	BI-DIR	XDP_NOA9_PCH
GPIO20	1	0	FM_SMI_ACTIVE_PCH_N/ FM_SMI_ACTIVE_CPLD_N
GPIO21	1	BI-DIR	XDP_NOA8_PCH
GPIO22	1	0	SCLOCK
GPIO23	0	X	NC
GPIO24	0	0	NC
GPIO25	1	1	1PPS_CPU
GPIO26	1	1	SYS_CPLD_INT_CPU
GPIO27	1	1	SOC_FPGA_DIN
GPIO28	1	0	SOC_FPGA_DOUT
GPIO29	1	0	IP_UART0_SOUT
GPIO30	1	1	IP_UART0_SIN
GPIO31	1	1	SMB_PWR_ALERT
GPIO32	X	X	NC
GPIO33	X	X	NC
GPIO35	1	0	FM_NMI_EVENT_PCH_N/ FM_NMI_EVENT_CPLD_N
GPIO36	1	0	ADR_STATUS_RD
GPIO37	1	1	ADR_STATUS_CLR
GPIO38	0	0	SLOAD
GPIO39	0	0	SDATAOUT0
GPIO40	0	BI	XDP_NOA1_PCH
GPIO41	1	0	XDP_NOA2_PCH/ CPLD_CONFIG_CLK
GPIO42	1	BI	XDP_NOA3_PCH/

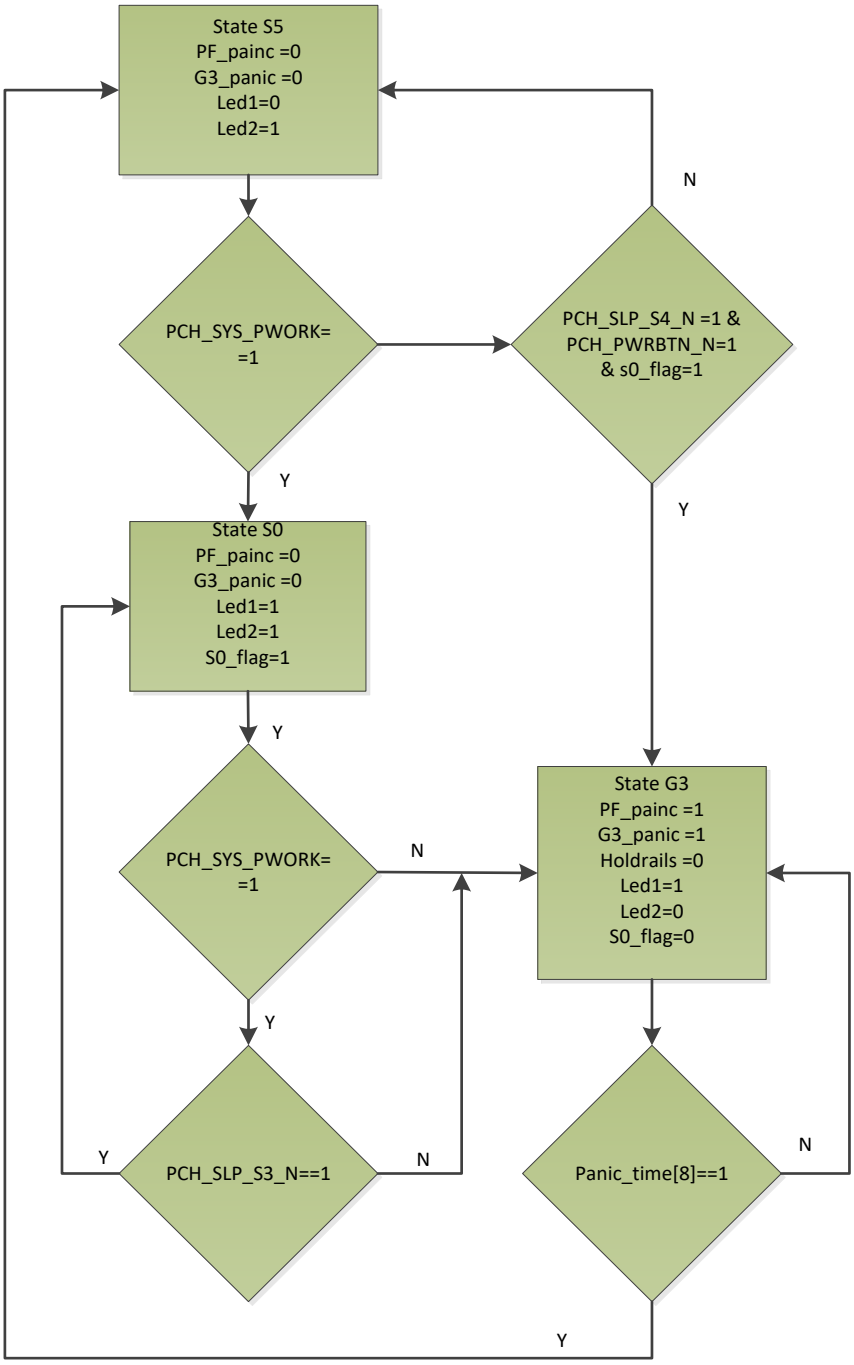
			CPLD_CONFIG_DATA
GPIO43	1	0	XDP_NOA4_PCH / ADR_MCU_INIT
GPIO44	0	1	NC
GPIO45	1	1	CPLD23_INT_CPU
GPIO46	1	0	CPU_JTAG_RST
GPIO48	1	0	SDATAOUT1
GPIO49	1	0	FM_CPU_PROCHOT_PCH_N/ FM_PROCHOT_N
GPIO50	X	X	NC
GPIO51	1	1	4.7k pull to 3.3V
GPIO52	1	1	CPU_SV
GPIO53	1	1	1k pull to gnd
GPIO54	X	X	NC
GPIO55	1	1	FM_BIOS_RCRV_BOOT_N
GPIO57	1	1	FM_ME_RCRV_N
GPIO58	0	X	SML1_CLK
GPIO59	1	BI	XDP_NOA0_PCH
GPIO60	0	X	SML0ALERT#
GPIO61	X	X	NC
GPIO62	0	X	SUSCLK_33K
GPIO65	0	X	NC
GPIO67	0	X	NC
GPIO68	1	1	CPLD interrupt
GPIO69	0	X	NC
GPIO70	0	X	NC
GPIO71	0	X	NC
GPIO72	1	1	1K pull to 3.3V
GPIO74	0	X	SML1ALERT#/TEMP_ALERT#.
GPIO75	0	X	SML1DATA

GPIO table

1.10. CPLD



CPLD Block Diagram



Power Sequence Flow Chat

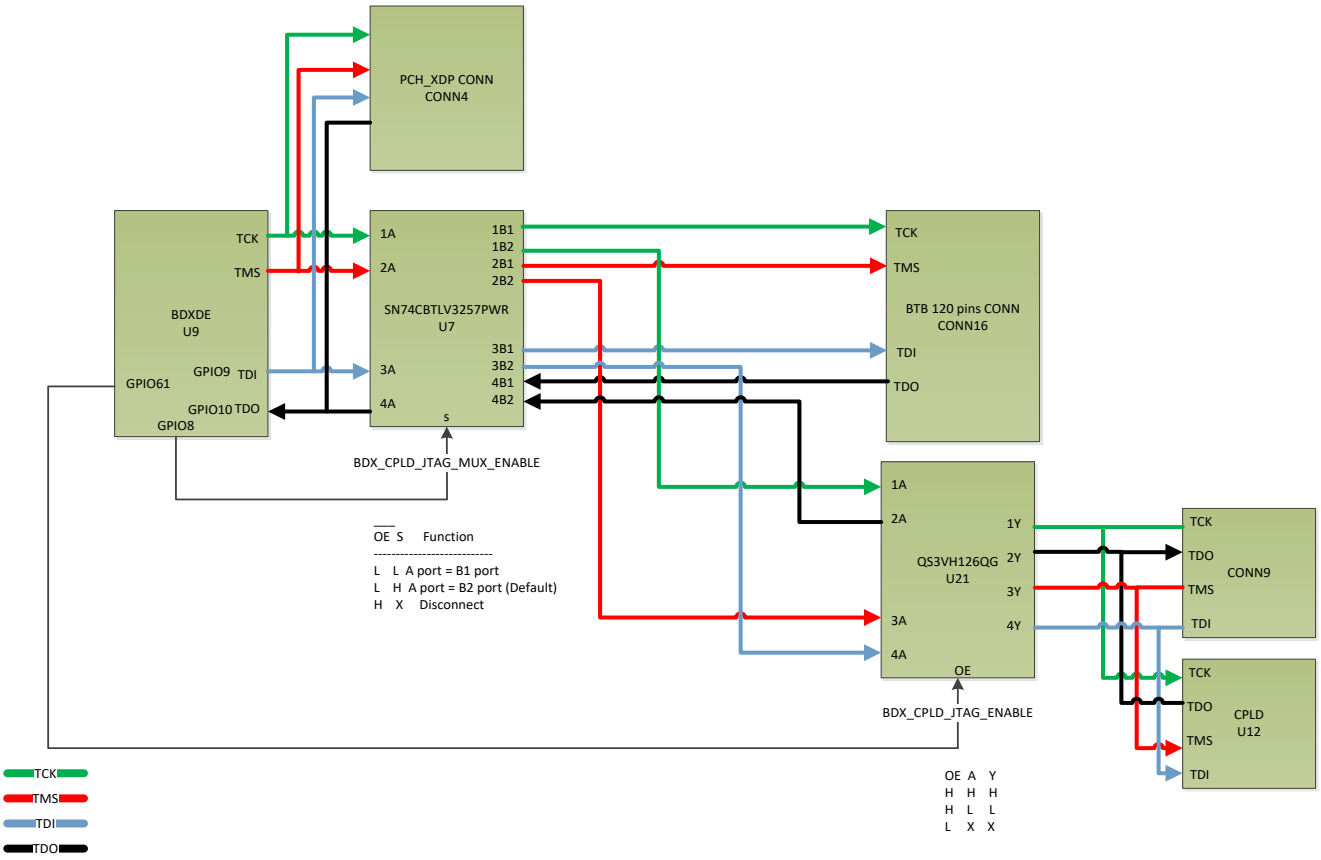
1.11.JTAG

The JTAG interface of the CPU board is used to upgrade the CPLD via CPU in the whole chassis, including U12 on the CPU board, other CPLDs are on the main board and FAN board.

When the CPLD on the CPU board needs to be upgraded, the GPIO8 of Broadwell-DE needs to select to “1”, and the GPIO61 needs to select to “1”.

When the CPLD devices on the main board or FAN board need to be upgrade, GPIO8 of

Broadwell-DE needs to select to “0”, and the GPIO61 needs to select to “0”.



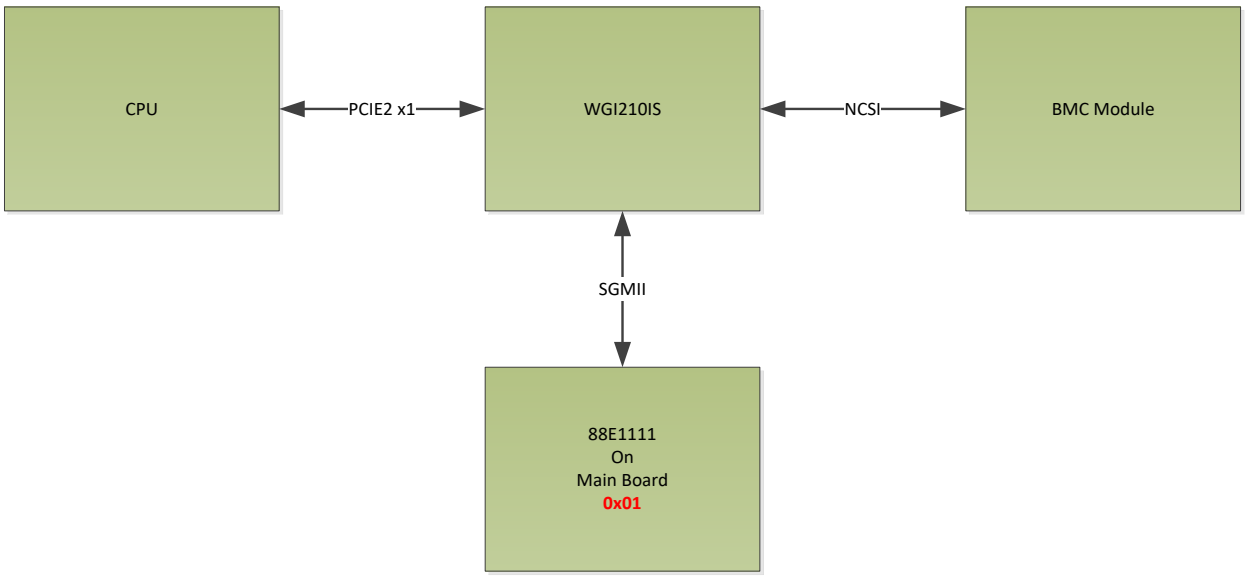
JTAG architecture

1.12.I210

The MAC sub-system is used for CPU to connect the management PHY (WGI210IS) on the main board, the Ethernet controller solution is Intel WGI210IS.

The I210 communicates CPU via PCIE GEN2 x1, and connect to the management port PHY MARVELL 88E1111 on the main board via SGMII interface.

The NCSI interface is used to connect the BMC module to support share NIC function.



I210IS connection illustration

1.12.1. Feature

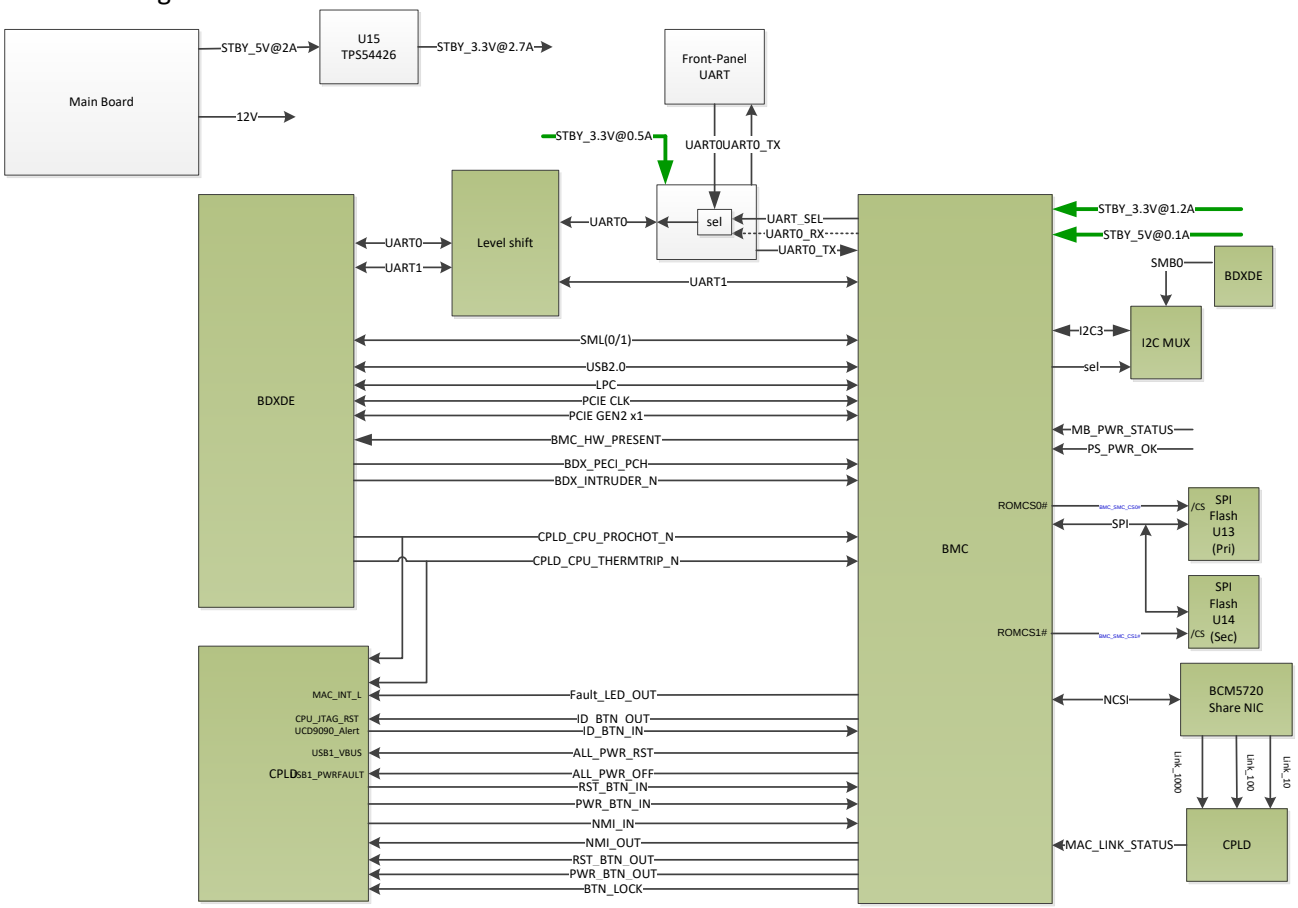
- Small package: 9 x 9 mm
- PCIe v2.1 (2.5 GT/s) x1, with Switching Voltage Regulator (iSVR)
- Integrated Non-Volatile Memory (iNVM)
- Platform Power Efficiency
  - IEEE 802.3az Energy Efficient Ethernet (EEE)
  - Proxy: ECMA-393 and Windows* logo for proxy offload
- Advanced Features:
  - 0 to 70 °C commercial temperature or -40 to 85 °C industrial temperature
  - Jumbo frames
  - Interrupt moderation, VLAN support, IP checksum offload
  - PCIe OBFF (Optimized Buffer Flush/Fill) for improved system power management
  - Four transmit and four receive queues
  - RSS and MSI-X to lower CPU utilization in multi-core systems
  - ECC – error correcting memory in packet buffers
  - Four Software Definable Pins (SDPs)
- Manageability:
  - NC-SI for greater bandwidth pass through
  - Flexible firmware architecture with secure Flash update
  - MCTP over PCIe
  - PXE and iSCSI boot

2. BMC Sub-system

The BMC is used for monitoring the system HW information including thermal, power, FAN and CPU status.

The BMC module would be installed in CONN14 on CPU board.

The following brief descriptions are for the interface between BMC module and CPU board in following sections.



BMCM connection

2.1. LPC

The LPC interface is the main communication channel for CPU to get the whole system information from BMC via IPMI protocol, like SMBUS.

BMC would also listen the information from CPU via LPC, such as port 80 status and serial messages for SOL function.

2.2. SMBUS

In order to prevent the multi master hang-up issue, if BMC module is installed, the SMBUS host would change to BMC, not CPU.

When BMC is installed, the “I2C_Multiplexer_select” would be driven to low to let BMC be the only host on SMBUS.

CPU would change to via LPC to get the SMBUS information from BMC.

2.3. UART

The UART interface is used to achieve SOL function.

CPU UART0 is connected to BMC uart1 block, and is used for SOL.

If BMC want to send UART message to CPU via UART0 of CPU, “BMC_UART0_DIR_SEL” would be driven to “0” from “1”.

2.3.1. Power-On Reset

The BCM88470 requires an explicit power ramp and reset sequence. 3.3V supply rails should come up first, then 1.8V and Core VDD come up later. SerDes rails should come up last while 1.25V SerDes rail should not ramp earlier than any other SerDes rails as shown in **Figure 6**. Since the device requires ROV, the core supply and the SerDes rails originate at different supply sources.

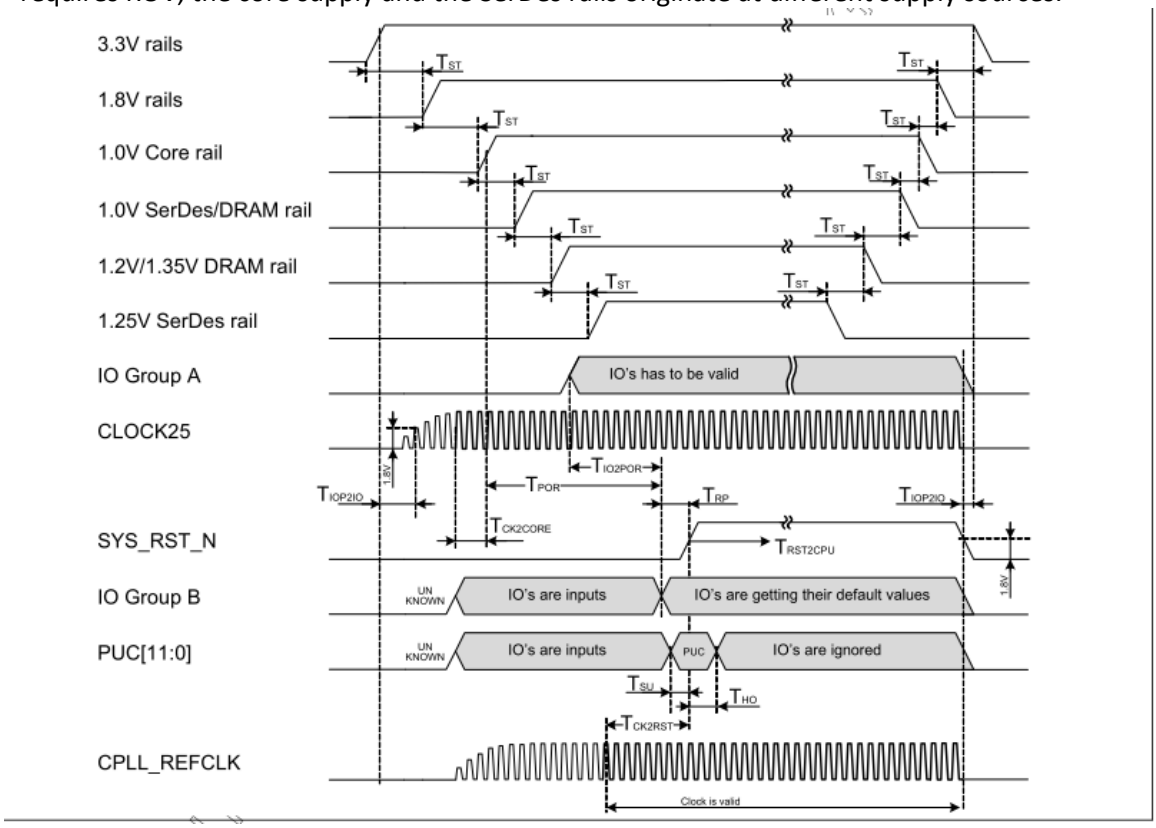
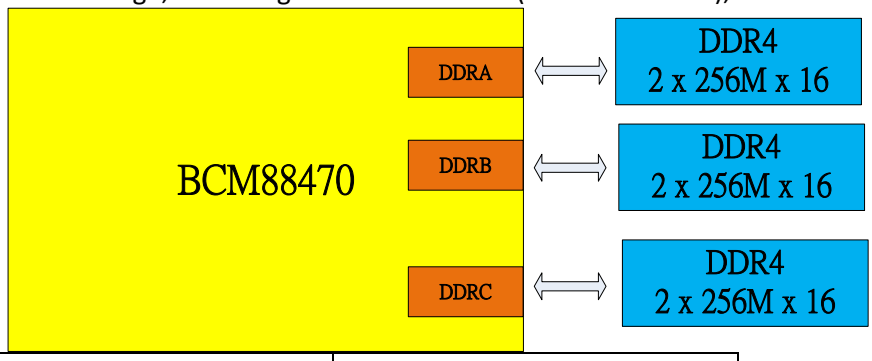


Figure 6 MAC Power Sequence

2.3.2. Deep buffering RAM

BCM88470 support three channels of DDR4/GDDR5(reference only) DRAM memory. Each channel can support up to two DDR4 devices that used separated CS signals. For DDR4 interface, 32b wide and storage capability up to 8Gb per channel. DRAM data rate of up to 3.2GB for DDR4.

In our design, we configuration Full DRAM (three interfaces), see below.



Vendor	Part Number
HYNIX	H5AN4G6NAFR-UHI

2.3.3. NIF/NIFE SerDes

The Ethernet protocol blocks are a pool of Ethernet Port Marcos (PM). There are three types of Ethernet Port Marco: 25G Ethernet protocol block (PM25), 10G Ethernet protocol block (PM10) and 10G Ethernet protocol with QSGMII (PM10Q).

BCM88470 includes four PM25, six PM10Q and two PM10.

BCM88470 network interface (NIF) is highly flexible and is composed of a pool of SerDes and a pool of protocol blocks that ae mapped via configuration to the SerDes. Table shows the NIF SerDes interface mapping.

Table 1: NIF SerDes Interface Mapping

PM	SRD Number	QSGMII (1G or 100M)	Single Lane Ports					Dual Lane Ports			Quad Lane Ports			ILKN	MESH
			100M over SGMII	1GbE or SGMII	2.5 GbE	10 GbE	25 GbE	RXAUI	XLAUI-2 (2x20.6G)	50 GbE	XAUI (10G)	XLAUI (40G)	100 GbE		
PM25-0	0-3			+		+	+		+	+	+	+	+	ILKN_A[a]	+
PM25-1	4-7			+		+	+		+	+	+	+	+	ILKN_A[a]	+
PM25-2	8-11			+		+	+		+	+	+	+	+	ILKN_A[a]	+
PM25-3	12-15			+		+	+		+	+	+	+	+	ILKN_A[a]	+
PM10Q-4	16-19	+	+	+	+	+		+			+	+		ILKN_B[b]	
PM10Q-5	20-23	+	+	+	+	+		+			+	+		ILKN_B[b]	
PM10Q-6	24-27	+	+	+	+	+		+			+	+		ILKN_B[b]	
PM10-7	28-31		+	+	+	+		+			+	+		ILKN_A[a]	
PM10Q-8	32-35	+	+	+	+	+		+			+	+		ILKN_B[b]	
PM10Q-9	36-39	+	+	+	+	+		+			+	+		ILKN_B[b]	
PM10Q-10	40-43	+	+	+	+	+		+			+	+		ILKN_B[b]	
PM10-11	44-47		+	+	+	+		+			+	+		ILKN_A[a]	

a. If a SerDes quad is configured to ILKN_A, each lane can be mapped either to ILKN#0, or ILKN#1.
b. If a SerDes quad is configured to ILKN_B, each lane can be mapped either to ILKN#2, or ILKN#3.

2.3.3.1. *Port mapping*

Below show BCM88470 Network Interface block diagram and NIF SerDes Interface mapping, PM25-2/3 runs at 100G per port and design for two of uplink port that connects to QSFP28 connector. The PM25-0/1 runs at 25G per port and connects to 2x4 SFP28 connector. Other NIFE SerDes configures as 10GbE that connects to SFP+ connector.

PM#	Interface	SFP+/SFP28/ QSFP28	Physical Port	Logical Port	MAC		
					Device	Lane	Interface
PM10-7	SerDes	SFP+	0	xe1	BCM88470	2	NIFE_TX[30]_P/N
							NIFE_RX[30]_P/N
	SerDes	SFP+	1	xe2	BCM88470	3	NIFE_TX[31]_P/N
							NIFE_RX[31]_P/N
	SerDes	SFP+	2	xe3	BCM88470	0	NIFE_TX[28]_P/N
							NIFE_RX[28]_P/N
	SerDes	SFP+	3	xe4	BCM88470	1	NIFE_TX[29]_P/N
							NIFE_RX[29]_P/N
PM10Q-6	SerDes	SFP+	4	xe5	BCM88470	1	NIFE_TX[25]_P/N
							NIFE_RX[25]_P/N
	SerDes	SFP+	5	xe6	BCM88470	0	NIFE_TX[24]_P/N
							NIFE_RX[24]_P/N
	SerDes	SFP+	6	xe7	BCM88470	3	NIFE_TX[27]_P/N
							NIFE_RX[27]_P/N

	SerDes	SFP+	7	xe8	BCM88470	2	NIFE_TX[26]_P/N
							NIFE_RX[26]_P/N
PM10Q-5	SerDes	SFP+	8	xe9	BCM88470	2	NIFE_TX[22]_P/N
							NIFE_RX[22]_P/N
	SerDes	SFP+	9	xe10	BCM88470	3	NIFE_TX[23]_P/N
							NIFE_RX[23]_P/N
	SerDes	SFP+	10	xe11	BCM88470	0	NIFE_TX[20]_P/N
							NIFE_RX[20]_P/N
	SerDes	SFP+	11	xe12	BCM88470	1	NIFE_TX[21]_P/N
							NIFE_RX[21]_P/N
PM10Q-4	SerDes	SFP+	12	xe13	BCM88470	2	NIFE_TX[18]_P/N
							NIFE_RX[18]_P/N
	SerDes	SFP+	13	xe14	BCM88470	3	NIFE_TX[19]_P/N
							NIFE_RX[19]_P/N
	SerDes	SFP+	14	xe15	BCM88470	0	NIFE_TX[16]_P/N
							NIFE_RX[16]_P/N
	SerDes	SFP+	15	xe16	BCM88470	1	NIFE_TX[17]_P/N
							NIFE_RX[17]_P/N
PM25-0	SerDes	SFP28	16	ce17	BCM88470	1	NIF_P/N_TX[01]
							NIF_P/N_RX[01]
	SerDes	SFP28	17	ce18	BCM88470	0	NIF_P/N_TX[00]
							NIF_P/N_RX[00]
	SerDes	SFP28	18	ce19	BCM88470	3	NIF_P/N_TX[03]
							NIF_P/N_RX[03]
	SerDes	SFP28	19	ce20	BCM88470	2	NIF_P/N_TX[02]
							NIF_P/N_RX[02]
PM25-1	SerDes	SFP28	20	ce21	BCM88470	1	NIF_P/N_TX[05]
							NIF_P/N_RX[05]
	SerDes	SFP28	21	ce22	BCM88470	0	NIF_P/N_TX[04]
							NIF_P/N_RX[04]
	SerDes	SFP28	22	ce23	BCM88470	3	NIF_P/N_TX[07]
							NIF_P/N_RX[07]
	SerDes	SFP28	23	ce24	BCM88470	2	NIF_P/N_TX[06]
							NIF_P/N_RX[06]
PM25-3	SerDes	QSFP28	0	ce25	BCM88470	3	NIF_TX[15]_P/N
							NIF_RX[15]_P/N

						2	NIF_TX[14]_P/N
							NIF_RX[14]_P/N
						1	NIF_TX[13]_P/N
							NIF_RX[13]_P/N
						0	NIF_TX[12]_P/N
							NIF_RX[12]_P/N
PM25-2	SerDes	QSFP28	1	ce26	BCM88470	3	NIF_TX[11]_P/N
							NIF_RX[11]_P/N
						2	NIF_TX[10]_P/N
							NIF_RX[10]_P/N
						1	NIF_TX[09]_P/N
							NIF_RX[09]_P/N
						0	NIF_TX[08]_P/N
							NIF_RX[08]_P/N

Table 3 NIF/NIFE mapping Table

2.3.4. CAUI-4 interface

The PM25-2 and PM25-3 run a 100GbE ports with CAUI-4 interface and directly connects to QSFP28 ports.

The PM25-0 and PM25-1 run a 25GbE ports with CAUI-4 interface and directly connects to SFP28 ports.

2.3.5. 10G KR interface

The PM10-11 runs at 10GbE ports with KR interface and directly connects to CPU for packet transmission between CPU and MAC.

2.3.6. LED stream

BCM88470 has two-wire (clock and data) LED interface is to control network port LEDs. Both signals are held low during periods of inactivity. A single LED refresh cycle consists of clocking out a programmable number of LED data bits. The LED data signal is pulsed high at the start of each LED refresh cycle, this selection define the Led stream by **Figure 7**.

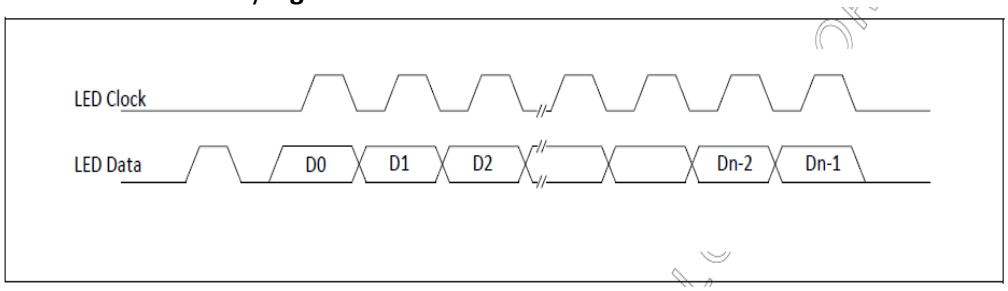


Figure 13: LED Refresh Timing

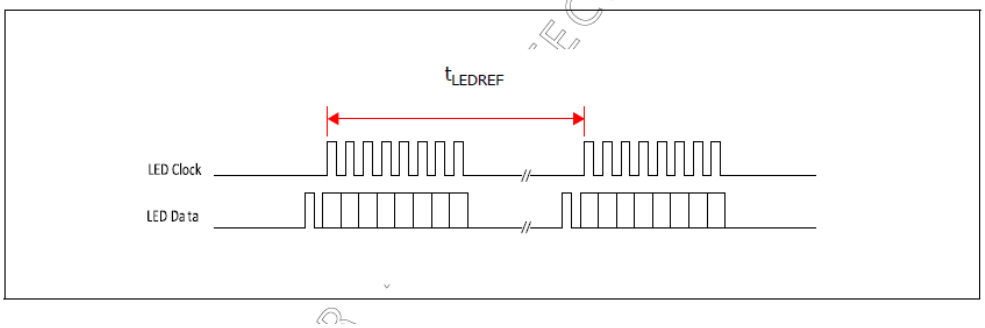


Figure 7 Led Refresh cycle

Table 33 shows LED stream from BCM88470 to CPLD then decode by CPLD.CPLD base on decode result to indicate each port LED status.

0	1	2	3	4	5	6	7	8	9	10	11	12	13
Port 25		Port 25 Lane 0			Port 25 Lane 1			Port 25 Lane 2			Port 25 Lane 3		
Lane[1:0]		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity
14	15	16	17	18	19	20	21	22	23	24	25	26	27
Port 26		Port 26 Lane 0			Port 26 Lane 1			Port 26 Lane 2			Port 26 Lane 3		
Lane[1:0]		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity
28	29	30	31	32	33	34	35	36	37	38	39	40	41
Lane[1:0]		Port 1			Port 2			Port 3			Port 4		
		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity
42	43	44	45	46	47	48	49	50	51	52	53	54	55
Lane[1:0]		Port 5			Port 6			Port 7			Port 8		
		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity
56	57	58	59	60	61	62	63	64	65	66	67	68	69
Lane[1:0]		Port 9			Port 10			Port 11			Port 12		
		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity
70	71	72	73	74	75	76	77	78	79	80	81	82	83
Lane[1:0]		Port 13			Port 14			Port 15			Port 16		
		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity
84	85	86	87	88	89	90	91	92	93	94	95	96	97
Lane[1:0]		Port 17			Port 18			Port 19			Port 20		
		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity
98	99	100	101	102	103	104	105	106	107	108	109	110	111
Lane[1:0]		Port 21			Port 22			Port 23			Port 24		
		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity

LED Stream bit define

Lane speed	Speed [1:0]	Lane Number	Lane [1:0]
1G	11	reserve	11
25G	10	4	10

20G	01	2	01
10G	00	1	00

Port configuration	Lane [1:0]	Speed [1:0]
100G	10	10
40G	10	00
10G	00	00
1G	00	11
4 x 25G	00	10
2 x 50G	01	10

Link-up/ Activity	LED
1	ON
0	OFF
Toggle	Activity

Below table shows default value of LED stream.

0	1	2	3	4	5	6	7	8	9	10	11	12	13
Port 25		Port 25 Lane 0			Port 25 Lane 1			Port 25 Lane 2			Port 25 Lane 3		
0 Lane[1:0] 1		0 Speed [1:0] 1		Link-up/ Activity 0	0 Speed [1:0] 1		Link-up/ Activity 0	0 Speed [1:0] 1		Link-up/ Activity 0	0 Speed [1:0] 1		Link-up/ Activity 0
14	15	16	17	18	19	20	21	22	23	24	25	26	27
Port 26		Port 26 Lane 0			Port 26 Lane 1			Port 26 Lane 2			Port 26 Lane 3		
0 Lane[1:0] 1		0 Speed [1:0] 1		Link-up/ Activity 0	0 Speed [1:0] 1		Link-up/ Activity 0	0 Speed [1:0] 1		Link-up/ Activity 0	0 Speed [1:0] 1		Link-up/ Activity 0
28	29	30	31	32	33	34	35	36	37	38	39	40	41
0 Lane[1:0] 0		Port 1			Port 2			Port 3			Port 4		
		0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0
42	43	44	45	46	47	48	49	50	51	52	53	54	55
0 Lane[1:0] 0		Port 5			Port 6			Port 7			Port 8		
		0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0
56	57	58	59	60	61	62	63	64	65	66	67	68	69
0 Lane[1:0] 0		Port 9			Port 10			Port 11			Port 12		
		0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0
70	71	72	73	74	75	76	77	78	79	80	81	82	83
0 Lane[1:0] 0		Port 13			Port 14			Port 15			Port 16		
		0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0
84	85	86	87	88	89	90	91	92	93	94	95	96	97
0 Lane[1:0] 0		Port 17			Port 18			Port 19			Port 20		
		0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0
98	99	100	101	102	103	104	105	106	107	108	109	110	111
0 Lane[1:0] 0		Port 21			Port 22			Port 23			Port 24		
		0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0	0 Speed [1:0] 0		Link-up/ Activity 0

2.4. CPLD and FPGA

~~A CPLD is used for Broadwell-DE as the glue logic for getting some Specific system-related information and doing some system controls.~~ This system totally has 3 x CPLDs and 1 x FPGA.

1. The CPLD on CPU board handles power sequence of Intel CPU.
2. The CPLD on main board shows network port LEDs and detects 10G SFP+ and 25G SFP28 transceiver status.
3. The CPLD on fan board handles fan speed adjustment and detects fan status.
4. The FPGA on main board do heater function control, detects 100G QSFP28 transceiver status, read thermal sensor temperature, power on/off each PSU, UART selection and interface translation.

~~(notes: missing CPLD and FPGA on switch sub-system)~~

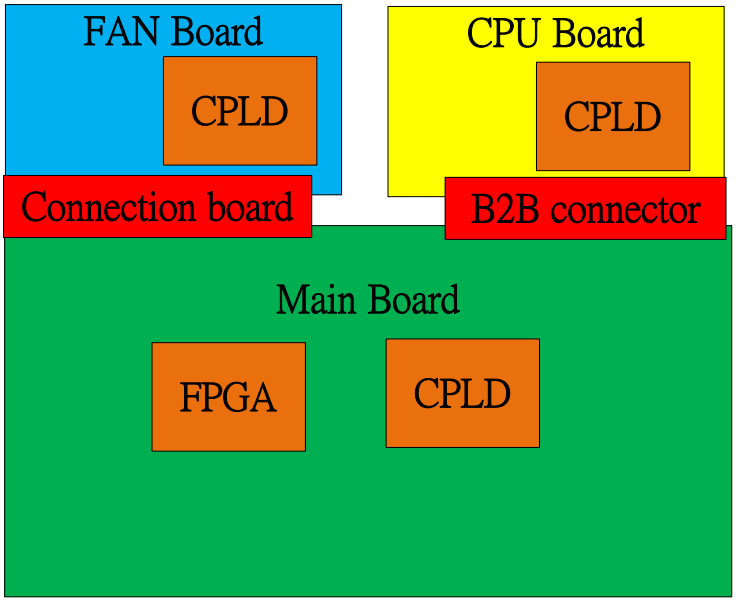


Figure 8 CPLD and FPGA

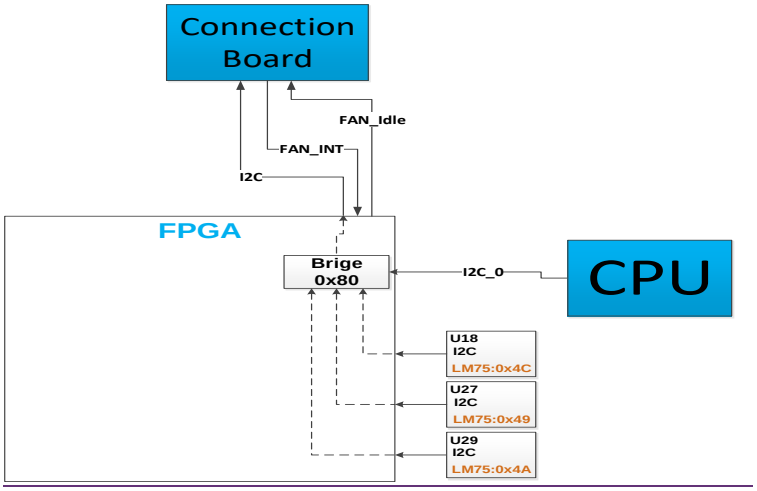
2.4.1. FPGA/CPLD Field upgrade information

The system support SW field upgraded function for main FPGA/CPLD and Fan CPLD

2.4.2. FPGA

FPGA locates on Main Board with connecting to CPU via I2C interface and I2C access address is 0x64. The following features are available with the FPGA:

- 40G/100G Optical transceiver status detect (Mode, Present, Reset…etc)
- Heater control
- FAN speed control by CPU via 0x80
- Thermal sensor read/write
- PSU Power On/Off control
- Reset and Interrupt
- Interface translation (I2C to SPI)
- UART selection



show block diagram for CPU FAN control via 0x80 to switch automatic or manual.

2.4.2.1. FPGA register

Address	Register	R/W	Default value
0x00	PCB Version	Read Only	0x02
0x01	FPGA version	Read Only	0x05
0x02	Power module status	Read Only	0x3C
0x03	Power Enable	Read&Write	0x01
0x16	UART Select	Read&Write	0x00
0x17	USB Present	Read&Write	0x04
0x18	QSFP28_Present_Port00 ~ 01	Read Only	0x03
0x19	QSFP28_ LPMODE _Port0 0 ~ 01	Read&Write	0x03
0x20	Interrup-1	Read Only	0xFF
0x21	Interrup-1 Mask	Read&Write	0x00
0x22	Interrup-2	Read Only	0xFF
0x23	Interrup-2 Mask	Read&Write	0x00
0x24	Interrup-3	Read Only	0xFF
0x25	Interrup-3 Mask	Read&Write	0x00
0x30	Reset-1	Read&Write	0xFF
0x31	Reset-2	Read&Write	0xFF
0x32	Reset-3	Read Only	0xFF
0x40	System LED-1	Read&Write	0xFF
0x41	System LED-2	Read&Write	0xFF
0x50	Heater state	Read&Write	0x0F

Address	Register	R/W	Default value
0x60	Misc. control and state signals	Read&Write	0x25
0x70	I2C WDPLL Mux Control	Read&Write	0x00
0x71	10M Hz Mux Control	Read&Write	TBD
0x72	4K Hz Mux Control	Read&Write	TBD
0x73	1PPS Mux Control	Read&Write	TBD
0x80	I2C LM75 CPLD Mux Control	Read&Write	0x10
0x81	LM75_1 Temp Stored	Read&Write	0x00
0x82	LM75_2 Temp Stored	Read&Write	0x00
0x83	LM75_3 Temp Stored	Read&Write	0x00
0x84	LM75_CPU Temp Stored	Read&Write	0x00
0x85	LM75_BMC Temp Stored	Read&Write	0x00

Table 4 FPGA I/O Register Table

2.4.2.2. Offset 0x00 PCB Version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:3	(Reserved)	R/W	0	
2:0	Main board PCB_version[1:0]	R	010	000: R0A 001: R0B 010: R0C 100: R01 Others: Reserved

2.4.2.3. Offset 0x01 FPGA version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	00000101	[7:0]: CPLD version

2.4.2.4. Offset 0x02 Power module status (Read&Write)

Bit	Name	R/W	Reset Value	Description
7	PS1_ON (PSU0)	R/W	0	0:PSU0 12V output 1: PSU0 12V no output
6	PS2_ON (PSU1)	R/W	0	0:PSU1 12V output 1: PSU1 12V no output

5	PS1_AC_ALERT (PSU0)	R	1	0: PSU0 POWER Fail 1: PSU0 POWER Good
4	PS2_AC_ALERT (PSU1)	R	1	0: PSU1 POWER Fail 1: PSU1 POWER Good
3	PS1_12V_PG (PSU0)	R	1	0: PSU0 12V Power Fail 1: PSU0 12V Power Good
2	PS2_12V_PG (PSU1)	R	1	0: PSU1 12V Power Fail 1: PSU1 12V Power Good
1	PS1_PRESENT (PSU0)	R	0	0: PSU0 Present 1: PSU0 not Present
0	PS2_PRESENT (PSU1)	R	0	0: PSU1 Present 1: PSU1 not Present

2.4.2.5. Offset 0x03 Power Enable (Read&Write)

Bit	Name	R/W	Reset Value	Description
7:1	(Reserved)	R/W	0	
0	USB_PWRON_N	R/W	1	0: USB HUB power converter disable 1: USB HUB power converter enable

2.4.2.6. Offset 0x16 UART select (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	GPS_RX or CPU_TX(FPGA1588_TOD_OUT_R) to FPGA1588_UART1_TOD_OUT	R/W	0	1: Switch FPGA1588_TOD_OUT_R to output. 0: Switch GPS_UART_RX_R to output.
5	FPGA_SN65C_2DE	R/W	00	[5:4] 11: Switch the ToD port as output. 00: Switch the ToD port as input.
4	FPGA_SN65C_1DE	R/W		
3:2	GPS_UART_RX_R (ToD_GPS) GPS_UART_RJ_RX (ToD_RJ45)	R/W	00	[3:2] 00: select GPS as UART input to the CPU. 01: select ToD_RJ45 as UART input to the CPU.
1:0	CPLD_RJ_UART_RX_R (RJ45) CPLD_USB_UART_RX_R (USB)	R/W	01	[1:0] 00: select RJ45 as UART input to the CPU. 01: select USB as UART input to the CPU.

2.4.2.7. Offset 0x17 USB_Present (Read & Write)

Bit	Name	R/W	Reset Value	Description

7:3	(Reserved)	R/W	0	
2	USB_Enable	R/W	1	1: USB ENABLED and USB cable is installed, USB Rx connects to CPU, If the USB cable is NOT installed, the RJ Rx signal connects to the CPU. 0: USB DISABLED, the RJ Console port will become the primary Rx.
1	USB_SUSP_L	R	0	1: indicates that the host USB port and USB console port is active. 0: indicates that the host USB port is in sleep mode or the USB cable is not connected.
0	USB_VBUS_DET	R	0	1: indicates that the Micro USB console is inserted. 0: No USB cable module be installed

2.4.2.8. Offset 0x18 QSFP28_Present_Port00 ~ 01 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:2	(Reserved)~~(Reserved)~~	R/W	00~~0~~	
1	QSFP_PRSNT_P02 (Port 01)	R	1	0: Show QSFP28 module has been installed 1: No QSFP28 module be installed
0	QSFP_PRSNT_P01 (Port 01)	R	1	0: Show QSFP28 module has been installed 1: No QSFP28 module be installed

2.4.2.9. Offset 0x19 QSFP28_LPMODE_Port00~01 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:2	(Reserved)~~(Reserved)~~	R/W	00~~0~~	
1	QSFP_MODE_P02 (Port 01)	R/W	1	0: Module work in High Power. 1: Module work in Lowe Power.
0	QSFP_MODE_P01 (Port 00)	R/W	1	0: Module work in High Power. 1: Module work in Lowe Power.
Note1: Depend on transceiver supplier support this function or not.				
Note2: Need to consider "Power_over-ride" and "Power_set" software control bits.				

2.4.2.10. Offset 0x20 Interrup-1 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	CPLD2_INT	R	1	0: Interrupt assert 1: Interrupt dessert

6	CPU_THERMALTRIP	R	1	0: Interrupt assert 1: Interrupt dessert
5	CPU_PROCHOT	R	1	0: Interrupt assert 1: Interrupt dessert
4	LM75BD3_INT	R	1	0: Interrupt assert 1: Interrupt dessert
3	LM75BD2_INT	R	1	0: Interrupt assert 1: Interrupt dessert
2	LM75BD1_INT	R	1	0: Interrupt assert 1: Interrupt dessert
1	LM75BD_HEATER_INT_1	R	1	0: Interrupt assert 1: Interrupt dessert
0	LM75BD_HEATER_INT_0	R	1	0: Interrupt assert 1: Interrupt dessert

2.4.2.11. Offset 0x21 Interrup-1 Mask (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	CPLD2_INT_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
6	CPU_THERMALTRIP_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
5	CPU_PROCHOT_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
4	LM75BD3_INT_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
3	LM75BD2_INT_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
2	LM75BD1_INT_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
1	LM75BD_HEATER_INT_1_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
0	LM75BD_HEATER_INT_0_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable

2.4.2.12. Offset 0x22 Interrup-2 (Read Only)

Bit	Name	R/W	Reset Value	Description
7	UCD90160_INT	R	1	0: Interrupt assert

				1: Interrupt dessert
6	INT_MGMT_PHY_N	R	1	0: Interrupt assert 1: Interrupt dessert
5	MAC_CPLD_INT_L	R	1	0: Interrupt assert 1: Interrupt dessert
4	THERMAL_INT_L	R	1	0: Interrupt assert 1: Interrupt dessert
3	USB_PWRFLT_N	R	1	0: Interrupt assert 1: Interrupt dessert
2	82P33931_INT_REQ	R	1	0: Interrupt assert 1: Interrupt dessert
1	QSFP_INT_P02 (Port 01)	R	1	0: Interrupt assert 1: Interrupt dessert
0	QSFP_INT_P01 (Port 00)	R	1	0: Interrupt assert 1: Interrupt dessert

2.4.2.13. Offset 0x23 Interrup-2 Mask (Read & Write)

Bit	Name	R/W	Reset Value	Description
7	UCD90160_INT_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
6	INT_MGMT_PHY_N_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
5	MAC_CPLD_INT_L_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
4	THERMAL_INT_L_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
3	USB_PWRFLT_N_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
2	82P33731_INT_REQ_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
1	QSFP_INT_P02_Mask (Port 01)	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
0	QSFP_INT_P01_Mask (Port 00)	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable

2.4.2.14. Offset 0x24 Interrup-3 (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:6	(Reserved)	R	1	0: Interrupt assert

				1: Interrupt dessert
5	FAN_INT_L	R	1	0: Interrupt assert 1: Interrupt dessert
4	INT_DS26503_L	R	1	0: Interrupt assert 1: Interrupt dessert
3	CPLD23_INT_CPU	R/W	1	0: Interrupt assert 1: Interrupt dessert
2	MAC_INT_L	R/W	1	0: Interrupt assert 1: Interrupt dessert
1	USB1_PWRFAULT	R/W	1	0: Interrupt assert 1: Interrupt dessert
0	SYS_CPLD_INT_CPU	R/W	1	0: Interrupt assert 1: Interrupt dessert

2.4.2.15. Offset 0x25 Interrup-3 Mask (Read & Write)

Bit	Name	R/W	Reset Value	Description
7:6	(Reserved)	R	0	
5	FAN_INT_L_Mask	R/W	1	1: System Interrupt function enable 0: System Interrupt function disable
4	INT_DS26503_L_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
3	CPLD23_INT_CPU_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
2	MAC_INT_L_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
1	USB1_PWRFAULT_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
0	SYS_CPLD_INT_CPU_Mask	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable

2.4.2.16. Offset 0x30 Reset-1 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	I2C_CPU1_RESET_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
6	I2C_CPU0_RESET_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
5	QSP01_P02_RESET_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state

4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SP17_P24_RESET_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
1	SP09_P16_RESET_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
0	SP01_P08_RESET_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state

2.4.2.17. Offset 0x31 Reset-2 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	BITS_REST	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
6	CPLD_RST	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
5	QSFP_RST_P02_N (Port 01)	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
4	QSFP_RST_P01_N (Port 00)	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
3	MAC_RESET_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
2	PHY_RST_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
1	82P33931_RST	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state
0	USB_RESET_N	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state

2.4.2.18. Offset 0x32 Reset-3 (Read Only)

Bit	Name	R/W	Reset Value	Description
7:5	(Reserved)	R	0	
4	Reset_button_RST	R	1	0: Button reset to CPLD. Indicates Reset Button had pushed.
3	CPU_JTAG_RST_R	R	1	TBD

2	SYS_SW_RST_N	R	1	0:Indicate FPGA reset the system all of device ,system is in a reset state
1	UCD90160_RST_L	R	1	TBD
0	POWER_RST	R	1	TBD

2.4.2.19. Offset 0x40 System LED-1 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	LOC_A	R/W	1	0: Flashing by remote management command. Assists the technician in finding the right device for service in the rack. (show **Amber** blink) 1: Not a particular switch that technician need to find. (LED off)
5 4	FAN_G FAN_A	R/W	11 Now no function Control by fan int and LM75B temp	00: indicator light is off. 10: System FAN operating normally. 01: System FAN tray present but is fault. 11:Green blinking->System FAN tray is power on but not running due to low temperature (which means FAN is function OK)
3	PSU2_G (PSU1)	R/W	0	0: indicator light is on when power good enable. 1: indicator light is off.
2	PSU2_A (PSU1)	R/W	1	0: indicator light is on when power good disable. 1: indicator light is off.
1	PSU1_G (PSU0)	R/W	0	0: indicator light is on when power good enable. 1: indicator light is off.
0	PSU1_A (PSU0)	R/W	1	0: indicator light is on when power good disable. 1: indicator light is off.

2.4.2.20. Offset 0x41 System LED-2 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	(Reserved)	R/W	0	

5:4	DIAG_G DIAG_A	R/W	11	[5:4] 00: System self-diagnostic test is in progress.(show **Green Blink**) 01: System self-diagnostic test successfully completed. (show **Green**) 10: System self-diagnostic test has detected a fault. (show **Amber**) 11: Diagnostic doesn't active.(LEDs are all off)
3	ToD_G	R/W	1	0: indicator light is on.(when ToD port enable) 1: indicator light is off.
2	(Reserved)	R/W	0	
1	BITS_G	R/W	1	0: indicator light is on.(when LLP enable) 1: indicator light is off.
0	(Reserved)	R/W	0	

2.4.2.21. Offset 0x42 BITS LLP (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:1	(Reserved)~~(Reserved)~~	R/W	0	
0	RLOS_FPGA (This function still confirm)	R	1	0: indicates that the LLP cable is inserted.

~~2.4.2.2.~~2.4.2.22. Offset 0x50 Heater state (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	I2C_CTRL_HEATER/ PWR _EN	R/W	0	1: HEATER/ PWR _EN Control by i2c 0: HEATER/ PWR _EN Control by fpga
5	(Reserved)	R/W	0	
4	MB1_PWR_EN	R/W	1	1: Turn on DC12V switch 0: Turn off DC12V switch
3	Fan_idle	R	1	1:Fan normal operating 0:Fan stop operating
2	HEATER_ENABLE_3	R/W	1	1: Heater disable. 0: Heater enable.

1:0	(Reserved)	R/W	0	

2.4.2.23. Offset 0x60 Misc. control and state signals (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	RESET_MAC88470	R	0	1: The Device is in normal operating state 0: The Device is in reset state
6	SW1_Select	R/W	0	0:CPU JTAG signals pass through to FPGA 1. CPU JTAG signals pass through to FAN_CPLD
5	SYS_PWR_READY_R	R	1	1: Power sequence is ready. 0: Power sequence is not ready.
4	1588_EEPROM_SEL	R/W	1	0:The WAN-PLL's EEPROM control signal comes from CPU 1: The WAN-PLL's EEPROM control signal comes from WAN-PLL
3	ID_Button	R/W	0	TBD
2	EE_WP	R/W	1	0:EEPROM write protect disable 1:EEPROM write protect enable
1	(Reserved)	R/W	0	
0	UCD9090_ALERT_L	R/W	1	TBD

2.4.2.24. Offset 0x70 I2C Mux Control

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
2	I2C_MUX2_EN	R/W	0	0: internal max10 i2c master to WAN_PLL_33931_SCL/SDA_FP 1: enable I2C1: WAN_PLL_82P33931_SCL/SDA to WAN_PLL that CPU can access WDPLL.
1:0	(Reserved)	R/W	0	

2.4.2.25. Offset 0x71 10MHz Mux Control

Bit	Name	R/W	Reset Value	Description
7:1	(Reserved)	R/W	0	
0	10M_SYNCE_FPGA_R (default) 10MHZ_WDPLL_1588_OUT_R_FPGA	R/W	1	0: Select sync-E as input to the SMB Conn out and MAC. 1: Select 1588 as input to the SMB Conn out and MAC.

2.4.2.26. Offset 0x72 4K Hz Mux Control

Bit	Name	R/W	Reset Value	Description
7:1	(Reserved)	R/W	0	
0	4K_SYNCE_FPGA_R(default) 4K_1588_FPGA_R	R/W	0	0: Select sync-E as input to MAC. 1: Select 1588 as input to MAC.

2.4.2.27. Offset 0x73 1pps Mux Control

Bit	Name	R/W	Reset Value	Description
7:4	(Reserved)	R/W	0	
3:2	FAP_NSE_SYNC_IN1(default) MAC_1PPS_IN_2 MAC_1PPS_IN_1	R/W	00	00: Select MAC_NSE_SYNCE_IN1 as input to WDPLL and 1PPS_MAC_OUT_MUX 01: Select MAC_NSE_SYNCE_OUT as input to WDPLL and 1PPS_MAC_OUT_MUX 10: Select MAC_GPIO1 as input to WDPLL and 1PPS_MAC_OUT_MUX
1:0	1PPS_SYNCE_1588_OUT_R_FPGA(default) 1PPS_WDPLL_1588_OUT_R_FPGA 1PPS_MAC_OUT_MUX	R/W	00	00: Select sync-E as input to SMB CONN and MAC and ToD port. 01: Select 1588 as input to SMB CONN and MAC and ToD port. 10: Select MAC as input to SMB CONN and MAC and ToD port.

2.4.2.28. Offset 0x80 I2C LM75 CPLD Mux Control

Bit	Name	R/W	Reset Value	Description
7:5	I2C_Channel_Sel	R/W	3'b000	110: LM75B1_HEATER BMC 101: LM75B0_HEATER CPU 100: LM75BD3_SCLK U18 011: LM75BD2_SCLK U29 010: LM75BD1_SCLK U27 001: FAN_SCL_FPGA_R FAN_CPLD 0x66 000: I2C not selected **Notice: When bit4 =1 recommend set bit7:5 to 3'b000**
4	wI2cMasterEn	R/W	1'b1	LM75B / FPGA to CPLD I2C Master / I2C_MUX2 Enable Control 1'b1 : Enable FPGA to CPLD I2C Master & LM75B Temp IC I2C Master Disable I2C_MUX2 1'b0 : Disable FPGA to CPLD I2C Master & LM75B Temp IC I2C Master Enable I2C_MUX2 **Notice: When bit4 =1 CPU can't access LM75B & FAN_CPLD**
3:0	(Reserved)	R/W	0	

2.4.2.29. Offset 0x81 LM75_1 Temp Stored

Bit	Name	R/W	Reset Value	Description
7:0	2's complement of Temp data	R	8'h00	7.4.3 Temperature register The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in 2's complement format with the resolution of 0.125 °C. Table 8 shows the bit arrangement of the Temp data in the data bytes. Table 8. Temp register MSByte: 7 6 5 4 3 2 1 0 — LSByte: 7 6 5 4 3 2 1 0 D10 D9 D8 D7 D6 D5 D4 D3 — D2 D1 D0 X X X X X Notice: Only store Temp Reg MSByte **address:0x4C**

2.4.2.30. Offset 0x82 LM75_2 Temp Stored

Bit	Name	R/W	Reset Value	Description

7:0	2’s complement of Temp data	R	8’h00	7.4.3 Temperature register The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in 2’s complement format with the resolution of 0.125 °C. Table 8 shows the bit arrangement of the Temp data in the data bytes. Table 8. Temp register MSByte: 7 6 5 4 3 2 1 0 — LSByte: 7 6 5 4 3 2 1 0 D10 D9 D8 D7 D6 D5 D4 D3 — D2 D1 D0 X X X X X Notice: Only store Temp Reg MSByte **address:0x49**

2.4.2.31. Offset 0x83 LM75_3 Temp Stored

Bit	Name	R/W	Reset Value	Description
7:0	2’s complement of Temp data	R	8’h00	7.4.3 Temperature register The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in 2’s complement format with the resolution of 0.125 °C. Table 8 shows the bit arrangement of the Temp data in the data bytes. Table 8. Temp register MSByte: 7 6 5 4 3 2 1 0 — LSByte: 7 6 5 4 3 2 1 0 D10 D9 D8 D7 D6 D5 D4 D3 — D2 D1 D0 X X X X X Notice: Only store Temp Reg MSByte **address:0x4A**

2.4.2.32. Offset 0x84 LM75_CPU Temp Stored

Bit	Name	R/W	Reset Value	Description
7:0	2’s complement of Temp data	R	8’h00	7.4.3 Temperature register The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in 2’s complement format with the resolution of 0.125 °C. Table 8 shows the bit arrangement of the Temp data in the data bytes. Table 8. Temp register MSByte: 7 6 5 4 3 2 1 0 — LSByte: 7 6 5 4 3 2 1 0 D10 D9 D8 D7 D6 D5 D4 D3 — D2 D1 D0 X X X X X Notice: Only store Temp Reg MSByte **address:0x4E**

2.4.2.33. Offset 0x85 LM75_BMC Temp Stored

Bit	Name	R/W	Reset Value	Description
7:0	2’s complement of Temp data	R	8’h00	7.4.3 Temperature register The Temperature register (Temp) holds the digital result of temperature measurement or monitor at the end of each analog-to-digital conversion. This register is read-only and contains two 8-bit data bytes consisting of one Most Significant Byte (MSByte) and one Least Significant Byte (LSByte). However, only 11 bits of those two bytes are used to store the Temp data in 2’s complement format with the resolution of 0.125 °C. Table 8 shows the bit arrangement of the Temp data in the data bytes. Table 8. Temp register MSByte: 7 6 5 4 3 2 1 0 — LSByte: 7 6 5 4 3 2 1 0 D10 D9 D8 D7 D6 D5 D4 D3 — D2 D1 D0 X X X X X Notice: Only store Temp Reg MSByte **address:0x4F**

~~*2.4.2.3.*~~*2.4.2.34. Offset 0x86 Max 10 FPGA I2C to UART & SPI Ctrl*

Bit	Name	R/W	Reset Value	Description
7:4	(Reserved)	R/W	0	
3	ToD_RX (GPS_UART_RJ_RX) Control	R/W	0	0: FIFO not save ToD_RX in
2	GPS_RX (GPS_UART_RX_R) Control	R/W	0	0: FIFO not save GPS_RX in
1 2	I2C_to_UART Controller Module Reset control	R/W	1	0: Reset I2C_to_UART Controller module
0 0	I2C_to_SPI Module Reset control I2C_to_UART Module Reset control	R/W	1	0: Reset iic_to_spi & iic_to_uart module

Max 10 FPGA I2C to UART & SPI Address mapping

I2C Address: 0x62 (7 bit) Offset address mode: 1 byte
SPI_BITS: SCLK: 1250000, CPOL=1, CPHA=1
UART_GPS : Core Speed: 38400 hz / Data Bit: 8bit / Parity: None / Stop Bit: 1bit /Not include CTS/RTS
UART_ToD : Core Speed: 38400 hz / Data Bit: 8bit / Parity: None / Stop Bit: 1bit /Not include CTS/RTS
FIFO_GPS: Depth:256
FIFO_ToD: Depth:256

Table 1.1. System Address mapping control by I2C slave to Avalon Master

	i2cslave_to_avlmm_bridge_0.avalon_master
mm_bridge_0.s0	
spi_0.spi_control_port	0x0000_0000 - 0x0000_001f
uart_gps.s1	0x0000_0020 - 0x0000_003f
uart_gps_read_fifo.in	0x0000_00a0 - 0x0000_00a3
uart_gps_read_fifo.out	0x0000_00a4 - 0x0000_00a7
uart_gps_read_fifo.in_csr	0x0000_0060 - 0x0000_007f
uart_tod.s1	0x0000_0040 - 0x0000_005f
uart_tod_read_fifo.in	0x0000_00b0 - 0x0000_00b3
uart_tod_read_fifo.out	0x0000_00b4 - 0x0000_00b7
uart_tod_read_fifo.in_csr	0x0000_0080 - 0x0000_009f

Table 1.2. SPI Master Core Address mapping control by I2C slave to Avalon Master

Internal Address	Register Name	Type [R/W]	32-11	10	9	8	7	6	5	4	3	2-0
0	rxdata (8)	R	RXDATA (n-1..0)									
1	txdata (8)	W	TXDATA (n-1..0)									
2	status (6)	R/W			EOP	E	RRDY	TRDY	TMT	TOE	ROE	
3	control	R/W		SSO (7)	IEOP	IE	IRRDY	ITRDY		ITOE	IROE	
4	Reserved	—										
5	slaveselect (7)	R/W	Slave Select Mask									
6	eop_value(8)	R/W	End of Packet Value (n-1..0)									

Table 1.3 Uart Master Core Address mapping control by I2C slave to Avalon Master

Offset	Register Name	R/W	Description/Register Bits													
			15:13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	rxdata	RO	Reserved					(2)	(2)	Receive Data						
1	txdata	WO	Reserved					(2)	(2)	Transmit Data						
2	status (1)	RW	Reserved	eop	cts	dcts		e	rrdy	trdy	tmt	toe	roe	brk	fe	pe
3	control	RW	Reserved	ieop	rts	idcts	trbk	ie	irrdy	itrdy	itmt	itoe	iroe	ibrk	ife	ipe
4	divisor (3)	RW	Baud Rate Divisor													
5	endof-packet (3)	RW	Reserved					(2)	(2)	End-of-Packet Value						

Table 1.4 FIFO CSR register Address mapping control by I2C slave to Avalon Master

offset	31 … 24	23 … 16	15 … 8	7	6	5	4	3	2	1	0
base	fill_level										
base + 1											i_status
base + 2											event
base + 3											interrupt enable
base + 4	almostfull										
base + 5	almostempty										

I2C to Uart Command Example

1. I2C write data to UART GPS TX flow
   i2c read addr:0x62 offset :0x28(status) (Check offset 0x28 bit 5(TOE) , 6(ROE) is equal to 1 or not
   i2c write addr:0x62 offset :0x24(txdata) Data:0xFF (UART TX Send 0xFF to GPS RX
2. i2c read data from UART GPS RX flow
   i2c read addr:0x62 offset :0x64(status) bit 1 (Check offset 0x64 bit0 is equal to 1 or not
   i2c read addr:0x62 offset :0xA4(fifo.out) ➔ Read data from fifo output data is gps tx data\
3. i2c read data from UART ToD RX flow
   i2c read addr:0x62 offset :0x84(status) bit 1 ➔Check offset 0x84 bit0 is equal to 1 or not
   i2c read addr:0x62 offset :0xB4(fifo.out) ➔ Read data from fifo output data is ToD tx data

2.4.3. CPLD

CPLD locates on Main Board with connecting to CPU via I2C interface and I2C access address is 0x63. The following features are available with the CPLD:

- SFP+ Port LED Link/Act indicates for Port 00 to Port 15
- SFP28 Port LED Link/Act indicates for Port 16 to Port 23
- QSFP28 Port LED Link/Act indicates for Port 00 to Port 01
- Uplink Port rate LED indicates. (40G/100G)
- Interrupt

- I2C
- Reset

2.4.3.1. CPLD register

Address	Register	R/W	Default value
0x01	CPLD version	Read Only	0x02
0x10	SFP+_ PRESENT _Port00 ~07	Read Only	0xFF
0x11	SFP+_ TX_Fault _Port00 ~07	Read Only	0x00
0x12	SFP+_ TX_Disable _Port00 ~07	Read&Write	0x00
0x13	SFP+_ RX_LOSS _Port00 ~07	Read Only	0x00
0x14	SFP+_ PRESENT _Port08 ~16	Read Only	0xFF
0x15	SFP+_ TX_Fault _Port08 ~16	Read Only	0x00
0x16	SFP+_ TX_Disable _Port08 ~16	Read&Write	0x00
0x17	SFP+_ RX_LOSS _Port08 ~16	Read Only	0x00
0x18	SFP+_ PRESENT _Port17 ~23	Read Only	0xFF
0x19	SFP+_ TX_Fault _Port17 ~23	Read Only	0x00
0x1A	SFP+_ TX_Disable _Port17 ~23	Read&Write	0x00
0x1B	SFP+_ RX_LOSS _Port17 ~23	Read Only	0x00
0x1C	QSFP28_P00_Speed Configuration	Read Only	0x55
0x1D	QSFP28_P01_Speed Configuration	Read Only	0x55
0x20	QSFP28_Port00 Configuration	Read&Write	0x0B
0x21	QSFP28_Port00_ Lane0-1 LED	Read&Write	0xFF
0x22	QSFP28_Port00_ Lane2-3 LED	Read&Write	0xFF
0X23	QSFP28_Port01 Configuration	Read&Write	0x0B
0x24	QSFP28_Port01_ Lane0-1 LED	Read&Write	0xFF
0x25	QSFP28_Port01_ Lane2-3 LED	Read&Write	0xFF
0x26	SFP+_Port00 LED	Read&Write	0x03
0x27	SFP+_Port01 LED	Read&Write	0x03
0x28	SFP+_Port02 LED	Read&Write	0x03
0x29	SFP+_Port03 LED	Read&Write	0x03
0x2A	SFP+_Port04 LED	Read&Write	0x03
0x2B	SFP+_Port05 LED	Read&Write	0x03
0x2C	SFP+_Port06 LED	Read&Write	0x03
0x2D	SFP+_Port07 LED	Read&Write	0x03
0x2E	SFP+_Port08 LED	Read&Write	0x03
0x2F	SFP+_Port09 LED	Read&Write	0x03
0x30	SFP+_Port10 LED	Read&Write	0x03

Address	Register	R/W	Default value
0x31	SFP+_Port11 LED	Read&Write	0x03
0x32	SFP+_Port12 LED	Read&Write	0x03
0x33	SFP+_Port13 LED	Read&Write	0x03
0x34	SFP+_Port14 LED	Read&Write	0x03
0x35	SFP+_Port15 LED	Read&Write	0x03
0x36	SFP28_Port16 LED	Read&Write	0x03
0x37	SFP28_Port17 LED	Read&Write	0x03
0x38	SFP28_Port18 LED	Read&Write	0x03
0x39	SFP28_Port19 LED	Read&Write	0x03
0x3A	SFP28_Port20 LED	Read&Write	0x03
0x3B	SFP28_Port21 LED	Read&Write	0x03
0x3C	SFP28_Port22 LED	Read&Write	0x03
0x3D	SFP28_Port23 LED	Read&Write	0x03
0x50	Reset	Read Only	0x01

Table 5 CPLD I/O Register Table

2.4.3.2. Offset 0x01 CPLD version (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	010	[7:3]: Reserved

				[2:0]: CPLD version

~~2.4.3.2.~~2.4.3.3. Offset 0x10 SFP+ PRESENT Port00 ~07 (Read only)

Bit	Name	R/W	Reset Value	Description
7	MOD_ABS_08 (Port 07)	R	1	0: indicates which SFP+ has been installed. 1: No SFP+ install
6	MOD_ABS_07 (Port 06)	R	1	0: indicates which SFP+ has been installed. 1: No SFP+ install
5	MOD_ABS_06 (Port 05)	R	1	0: indicates which SFP+ has been installed. 1: No SFP+ install
4	MOD_ABS_05 (Port 04)	R	1	0: indicates which SFP+ has been installed. 1: No SFP+ install
3	MOD_ABS_04 (Port 03)	R	1	0: indicates which SFP+ has been installed. 1: No SFP+ install
2	MOD_ABS_03 (Port 02)	R	1	0: indicates which SFP+ has been installed. 1: No SFP+ install
1	MOD_ABS_02 (Port 01)	R	1	0: indicates which SFP+ has been installed. 1: No SFP+ install
0	MOD_ABS_01 (Port 00)	R	1	0: indicates which SFP+ has been installed. 1: No SFP+ install

2.4.3.4. Offset 0x11 TX_Fault Port 00 ~07 (Read only)

Bit	Name	R/W	Reset Value	Description
7	TXFLT_08 (Port 07)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
6	TXFLT_07 (Port 06)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
5	TXFLT_06 (Port 05)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
4	TXFLT_05 (Port 04)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
3	TXFLT_04 (Port 03)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
2	TXFLT_03 (Port 02)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
1	TXFLT_02 (Port 01)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
0	TXFLT_01 (Port 00)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault

2.4.3.5. Offset 0x12 TX_Disable Port 00 ~07 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	TXDIS_08 (Port 07)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.

6	TXDIS_07 (Port 06)	R/W	0	When a value of "1" is written, will turn off the laser's power for each SFP module.
5	TXDIS_06 (Port 05)	R/W	0	When a value of "1" is written, will turn off the laser's power for each SFP module.
4	TXDIS_05 (Port 04)	R/W	0	When a value of "1" is written, will turn off the laser's power for each SFP module.
3	TXDIS_04 (Port 03)	R/W	0	When a value of "1" is written, will turn off the laser's power for each SFP module.
2	TXDIS_03 (Port 02)	R/W	0	When a value of "1" is written, will turn off the laser's power for each SFP module.
1	TXDIS_02 (Port 01)	R/W	0	When a value of "1" is written, will turn off the laser's power for each SFP module.
0	TXDIS_01 (Port 00)	R/W	0	When a value of "1" is written, will turn off the laser's power for each SFP module.

2.4.3.6. Offset 0x13 RX_LOSS_Port00 ~07 (Read only)

Bit	Name	R/W	Reset Value	Description
7	RXLOS_08 (Port 07)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.
6	RXLOS_07 (Port 06)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.
5	RXLOS_06 (Port 05)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.
4	RXLOS_05 (Port 04)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.
3	RXLOS_04 (Port 03)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.
2	RXLOS_03 (Port 02)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.
1	RXLOS_02 (Port 01)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.
0	RXLOS_01 (Port 00)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.

2.4.3.7. Offset 0x14 SFP+_PRESENT_Port08 ~15 (Read only)

Bit	Name	R/W	Reset Value	Description
7	MOD_ABS_16 (Port 15)	R	1	0: indicates which SFP has been installed. 1: No SFP install
6	MOD_ABS_15 (Port 14)	R	1	0: indicates which SFP has been installed. 1: No SFP install
5	MOD_ABS_14 (Port 13)	R	1	0: indicates which SFP has been installed. 1: No SFP install
4	MOD_ABS_13 (Port 12)	R	1	0: indicates which SFP has been installed.

				1: No SFP install
3	MOD_ABS_12 (Port 11)	R	1	0: indicates which SFP has been installed. 1: No SFP install
2	MOD_ABS_11 (Port 10)	R	1	0: indicates which SFP has been installed. 1: No SFP install
1	MOD_ABS_10 (Port 09)	R	1	0: indicates which SFP has been installed. 1: No SFP install
0	MOD_ABS_09 (Port 08)	R	1	0: indicates which SFP has been installed. 1: No SFP install

2.4.3.8. Offset 0x15 TX_Fault_Port08 ~15 (Read only)

Bit	Name	R/W	Reset Value	Description
7	TXFLT_16 (Port 15)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
6	TXFLT_15 (Port 14)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
5	TXFLT_14 (Port 13)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
4	TXFLT_13 (Port 12)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
3	TXFLT_12 (Port 11)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
2	TXFLT_11 (Port 10)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
1	TXFLT_10 (Port 09)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault
0	TXFLT_09 (Port 08)	R	0	0: SFP+ Transmitter is working well 1: SFP+ Transmit Fault

2.4.3.9. Offset 0x16 TX_Disable_Port 08 ~15 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	TXDIS_16 (Port 15)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
6	TXDIS_15 (Port 14)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
5	TXDIS_14 (Port 13)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
4	TXDIS_13 (Port 12)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
3	TXDIS_12 (Port 11)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
2	TXDIS_11 (Port 10)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.

1	TXDIS_10 (Port 09)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.
0	TXDIS_09 (Port 08)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP module.

2.4.3.10. Offset 0x17 RX_LOSS_Port 08 ~15 (Read only)

Bit	Name	R/W	Reset Value	Description
7	RXLOS_16 (Port 15)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.
6	RXLOS_15 (Port 14)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.
5	RXLOS_14 (Port 13)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.
4	RXLOS_13 (Port 12)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.
3	RXLOS_12 (Port 11)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.
2	RXLOS_11 (Port 10)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.
1	RXLOS_10 (Port 09)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.
0	RXLOS_09 (Port 08)	R	0	0: SFP+ optical level meet the standard. 1: SFP+ optical level lower than the standard.

2.4.3.11. Offset 0x18 SFP28_PRESENT_Port16 ~23 (Read only)

Bit	Name	R/W	Reset Value	Description
7	MOD_ABS_24 (Port 23)	R	1	0: indicates which SFP28 has been installed. 1: No SFP28 install
6	MOD_ABS_23 (Port 22)	R	1	0: indicates which SFP28 has been installed. 1: No SFP28 install
5	MOD_ABS_22 (Port 21)	R	1	0: indicates which SFP28 has been installed. 1: No SFP28 install
4	MOD_ABS_21 (Port 20)	R	1	0: indicates which SFP28 has been installed. 1: No SFP28 install
3	MOD_ABS_20 (Port 19)	R	1	0: indicates which SFP28 has been installed. 1: No SFP28 install
2	MOD_ABS_19 (Port 18)	R	1	0: indicates which SFP28 has been installed. 1: No SFP28 install
1	MOD_ABS_18 (Port 17)	R	1	0: indicates which SFP28 has been installed. 1: No SFP28 install
0	MOD_ABS_17	R	1	0: indicates which SFP28 has been installed.

	(Port 16)			1: No SFP28 install

2.4.3.12. Offset 0x19 SFP28 TX_Fault_Port 16 ~23 (Read only)

Bit	Name	R/W	Reset Value	Description
7	TXFLT_24 (Port 23)	R	0	0: SFP28 Transmitter is working well 1: SFP28 Transmit Fault
6	TXFLT_23 (Port 22)	R	0	0: SFP28 Transmitter is working well 1: SFP28 Transmit Fault
5	TXFLT_22 (Port 21)	R	0	0: SFP28 Transmitter is working well 1: SFP28 Transmit Fault
4	TXFLT_21 (Port 20)	R	0	0: SFP28 Transmitter is working well 1: SFP28 Transmit Fault
3	TXFLT_20 (Port 19)	R	0	0: SFP28 Transmitter is working well 1: SFP28 Transmit Fault
2	TXFLT_19 (Port 18)	R	0	0: SFP28 Transmitter is working well 1: SFP28 Transmit Fault
1	TXFLT_18 (Port 17)	R	0	0: SFP28 Transmitter is working well 1: SFP28 Transmit Fault
0	TXFLT_17 (Port 16)	R	0	0: SFP28 Transmitter is working well 1: SFP28 Transmit Fault

2.4.3.13. Offset 0x1A SFP28 TX_Disable_Port 16 ~23 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	TXDIS_24 (Port 23)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP28 module.
6	TXDIS_23 (Port 22)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP28 module.
5	TXDIS_22 (Port 21)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP28 module.
4	TXDIS_21 (Port 20)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP28 module.
3	TXDIS_20 (Port 19)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP28 module.
2	TXDIS_19 (Port 18)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP28 module.
1	TXDIS_18 (Port 17)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP28 module.
0	TXDIS_17 (Port 16)	R/W	0	When a value of “1” is written, will turn off the laser’s power for each SFP28 module.

2.4.3.14. Offset 0x1B SFP28 RX_LOSS_Port 16 ~23 (Read only)

Bit	Name	R/W	Reset Value	Description
7	RXLOS_24 (Port 23)	R	0	0: SFP28 optical level meet the standard. 1: SFP28 optical level lower than the standard.
6	RXLOS_23	R	0	0: SFP28 optical level meet the standard.

	(Port 22)			1: SFP28 optical level lower than the standard.
5	RXLOS_22 (Port 21)	R	0	0: SFP28 optical level meet the standard. 1: SFP28 optical level lower than the standard.
4	RXLOS_21 (Port 20)	R	0	0: SFP28 optical level meet the standard. 1: SFP28 optical level lower than the standard.
3	RXLOS_20 (Port 19)	R	0	0: SFP28 optical level meet the standard. 1: SFP28 optical level lower than the standard.
2	RXLOS_19 (Port 18)	R	0	0: SFP28 optical level meet the standard. 1: SFP28 optical level lower than the standard.
1	RXLOS_18 (Port 17)	R	0	0: SFP28 optical level meet the standard. 1: SFP28 optical level lower than the standard.
0	RXLOS_17 (Port 16)	R	0	0: SFP28 optical level meet the standard. 1: SFP28 optical level lower than the standard.

2.4.3.15. Offset 0x1C QSFP28_Port 00_Speed Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7	QSFP28_P01_lane3_Speed1 (LSB)(Port 00)	R	0	00: 10G 01: 20G 10: 25G 11: 1G
6	QSFP28_P01_lane3_Speed0 (MSB)(Port 00)	R	1	
5	QSFP28_P01_lane2_Speed1 (LSB)(Port 00)	R	0	00: 10G 01: 20G 10: 25G 11: 1G
4	QSFP28_P01_lane2_Speed0 (MSB)(Port 00)	R	1	
3	QSFP28_P01_lane1_Speed1 (LSB)(Port 00)	R	0	00: 10G 01: 20G 10: 25G 11: 1G
2	QSFP28_P01_lane1_Speed0 (MSB)(Port 00)	R	1	
1	QSFP28_P01_lane0_Speed1 (LSB)(Port 00)	R	0	00: 10G 01: 20G 10: 25G 11: 1G
0	QSFP28_P01_lane0_Speed0 (MSB)(Port 00)	R	1	

2.4.3.16. Offset 0x1D QSFP28_Port 01_Speed Configuration (Read Only)

Bit	Name	R/W	Reset Value	Description
7	QSFP28_P02_lane3_Speed1 (LSB)(Port 01)	R	0	00: 10G 01: 20G 10: 25G 11: 1G
6	QSFP28_P02_lane3_Speed0 (MSB)(Port 01)	R	1	

5	QSFP28_P02_lane2_Speed1 (LSB)(Port 01)	R	0	00: 10G 01: 20G 10: 25G 11: 1G
4	QSFP28_P02_lane2_Speed0 (MSB)(Port 01)	R	1	
3	QSFP28_P02_lane1_Speed1 (LSB)(Port 01)	R	0	00: 10G 01: 20G 10: 25G 11: 1G
2	QSFP28_P02_lane1_Speed0 (MSB)(Port 01)	R	1	
1	QSFP28_P02_lane0_Speed1 (LSB)(Port 01)	R	0	00: 10G 01: 20G 10: 25G 11: 1G
0	QSFP28_P02_lane0_Speed0 (MSB)(Port 01)	R	1	

2.4.3.17. Offset 0x20 QSFP28 Port 01 Configuration (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	QSFP28_P01_lane3_ Link-up/Activity (Port 00)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
6	QSFP28_P01_lane2_ Link-up/Activity (Port 00)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
5	QSFP28_P01_lane1_ Link-up/Activity (Port 00)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
4	QSFP28_P01_Lane_number_1 (LSB)(Port 00)	R	0	00: 1 lane 01: 2 lane 10: 4 lane 11: reserve
3	QSFP28_P01_Lane_number_0 (MSB)(Port 00)	R	1	
2	QSFP28_P01_lane0_ Link-up/Activity(Port 00)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P01_100G_LED_G (Port 00)	R/W	1	11: There is no link on the port. 10: QSFP28 port has a valid link at 40G. 01: QSFP28 port has a valid link at 100G.
0	P01_40G_LED_B (Port 00)	R/W	1	

Bit0, 1 refer to below table (14 bits).
When

10 101 101 101 101
Green LED is on. (bit1=0)
When
10 001 001 001 001
Blue LED is on. (bit0=0)

0	1	2	3	4	5	6	7	8	9	10	11	12	13
Port 00		Port 00 Lane 0			Port 00 Lane 1			Port 00 Lane 2			Port 00 Lane 3		
Lane[1:0]		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity

2.4.3.18. Offset 0x21 QSFP28_Port 00_Lane0-1 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	(reserved)	R	0	
5	P01_LANE1_LED_R (Port 00)	R/W	1	111: There is no link on the port. 001: QSFP28 port has a valid link at 25G. 010: QSFP28 port has a valid link at 10G. Flashing indicates activity.
4	P01_LANE1_LED_G (Port 00)	R/W	1	
3	P01_LANE1_LED_B (Port 00)	R/W	1	
2	P01_LANE0_LED_R (Port 00)	R/W	1	111: There is no link on the port. 001: QSFP28 port has a valid link at 25G. 010: QSFP28 port has a valid link at 10G. Flashing indicates activity.
1	P01_LANE0_LED_G (Port 00)	R/W	1	
0	P01_LANE0_LED_B (Port 00)	R/W	1	

2.4.3.19. Offset 0x22 QSFP28_Port 00_Lane2-3 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	(reserved)	R	0	
5	P01_LANE3_LED_R (Port 00)	R/W	1	111: There is no link on the port. 001: QSFP28 port has a valid link at 25G. 010: QSFP28 port has a valid link at 10G. Flashing indicates activity.
4	P01_LANE3_LED_G (Port 00)	R/W	1	

3	P01_LANE3_LED_B (Port 00)	R/W	1	
2	P01_LANE2_LED_R (Port 00)	R/W	1	111: There is no link on the port. 001: QSFP28 port has a valid link at 25G. 010: QSFP28 port has a valid link at 10G. Flashing indicates activity.
1	P01_LANE2_LED_G (Port 00)	R/W	1	
0	P01_LANE2_LED_B (Port 00)	R/W	1	

2.4.3.20. Offset 0x23 QSFP28_Port 01 configuration (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	QSFP28_P02_lane3_ Link-up/Activity (Port 01)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
6	QSFP28_P02_lane2_ Link-up/Activity (Port 01)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
5	QSFP28_P02_lane1_ Link-up/Activity (Port 01)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
4	QSFP28_P02_Lane_number_1 (LSB)(Port 01)	R	0	00: 1 lane 01: 2 lane 10: 4 lane 11: reserve
3	QSFP28_P02_Lane_number_0 (MSB)(Port 01)	R	1	
2	QSFP28_P02_lane0_ Link-up/Activity (Port 01)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P02_100G_LED_G (Port 01)	R/W	1	11: There is no link on the port. 10: QSFP28 port has a valid link at 40G. 01: QSFP28 port has a valid link at 100G.
0	P02_40G_LED_B (Port 01)	R/W	1	

Bit0, 1 refer to below table (14 bits).
When
10 101 101 101 101
Green LED is on. (bit1=0)
When
10 001 001 001 001

Blue LED is on. (bit0=0)

0	1	2	3	4	5	6	7	8	9	10	11	12	13
Port 01		Port 01 Lane 0			Port 01 Lane 1			Port 01 Lane 2			Port 01 Lane 3		
Lane[1:0]		Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity	Speed [1:0]		Link-up/ Activity

2.4.3.21. Offset 0x24 QSFP28_Port 01_Lane0-1 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	(reserved)	R	0	
5	P02_LANE1_LED_R (Port 01)	R/W	1	111: There is no link on the port. 001: QSFP28 port has a valid link at 25G. 010: QSFP28 port has a valid link at 10G. Flashing indicates activity.
4	P02_LANE1_LED_G (Port 01)	R/W	1	
3	P02_LANE1_LED_B (Port 01)	R/W	1	
2	P02_LANE0_LED_R (Port 01)	R/W	1	111: There is no link on the port. 001: QSFP28 port has a valid link at 25G. 010: QSFP28 port has a valid link at 10G. Flashing indicates activity.
1	P02_LANE0_LED_G (Port 01)	R/W	1	
0	P02_LANE0_LED_B (Port 01)	R/W	1	

2.4.3.22. Offset 0x25 QSFP28_Port 01_Lane2-3 (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:6	(reserved)	R	0	
5	P02_LANE3_LED_R (Port 01)	R/W	1	111: There is no link on the port. 001: QSFP28 port has a valid link at 25G. 010: QSFP28 port has a valid link at 10G. Flashing indicates activity.
4	P02_LANE3_LED_G (Port 01)	R/W	1	
3	P02_LANE3_LED_B (Port 01)	R/W	1	
2	P02_LANE2_LED_R (Port 01)	R/W	1	111: There is no link on the port. 001: QSFP28 port has a valid link at 25G. 010: QSFP28 port has a valid link at 10G. Flashing indicates activity.
1	P02_LANE2_LED_G (Port 01)	R/W	1	

0	P02_LANE2_LED_B (Port 01)	R/W	1	

2.4.3.23. Offset 0x26 SFP+ Port 00 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P1_Speed1(Port 00)	R	0	00: 10G 11: 1G
5	SFP+_P1_Speed0(Port 00)	R	0	
4	SFP+_P1-4_Lane_number_1 (Port 00-03)	R	0	00: 1 lane
3	SFP+_P1-4_Lane_number_0 (Port 00-03)	R	0	
2	SFP+_P1_ Link-up/Activity (Port 00-03)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P1_LED_SFP+_A (Port 00)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P1_LED_SFP+_G (Port 00)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.24. Offset 0x27 SFP+ Port 01 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P2_Speed1(Port 01)	R	0	00: 10G 11: 1G
5	SFP+_P2_Speed0(Port 01)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P2_ Link-up/Activity (Port 01)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P2_LED_SFP+_A (Port 01)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P2_LED_SFP+_G (Port 01)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.25. Offset 0x28 SFP+ Port 02 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description

7	(Reserved)	R/W	0	
6	SFP+_P3_Speed1(Port 02)	R	0	00: 10G 11: 1G
5	SFP+_P3_Speed0(Port 02)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P3_ Link-up/Activity (Port 02)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P3_LED_SFP+_A (Port 02)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P3_LED_SFP+_G (Port 02)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.26. Offset 0x29 SFP+_Port4 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P4_Speed1(Port 03)	R	0	00: 10G 11: 1G
5	SFP+_P4_Speed0(Port 03)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P4_ Link-up/Activity (Port 03)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P4_LED_SFP+_A (Port 03)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P4_LED_SFP+_G (Port 03)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.27. Offset 0x2A SFP+_Port 04 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P5_Speed1(Port 04)	R	0	00: 10G 11: 1G
5	SFP+_P5_Speed0(Port 04)	R	0	
4	SFP+_P5-8_Lane_number_1 (Port 04-07)	R	0	00: 1 lane
3	SFP+_P5-8_Lane_number_0 (Port 04-07)	R	0	

2	SFP+_P5_ Link-up/Activity (Port 04)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P5_LED_SFP+_A (Port 04)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P5_LED_SFP+_G (Port 04)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.28. Offset 0x2B SFP+ Port 05 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P6_Speed1(Port 05)	R	0	00: 10G 11: 1G
5	SFP+_P6_Speed0(Port 05)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P6_ Link-up/Activity (Port 05)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P6_LED_SFP+_A (Port 05)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P6_LED_SFP+_G (Port 05)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.29. Offset 0x2C SFP+ Port 06 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P7_Speed1(Port 06)	R	0	00: 10G 11: 1G
5	SFP+_P7_Speed0(Port 06)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P7_ Link-up/Activity (Port 06)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P7_LED_SFP+_A (Port 06)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P7_LED_SFP+_G (Port 06)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G.

				Flashing indicates activity.

2.4.3.30. Offset 0x2D SFP+_Port 07 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P8_Speed1(Port 07)	R	0	00: 10G 11: 1G
5	SFP+_P8_Speed0(Port 07)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P8_ Link-up/Activity (Port 07)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P8_LED_SFP+_A (Port 07)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P8_LED_SFP+_G (Port 07)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.31. Offset 0x2E SFP+_Port 08 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P9_Speed1(Port 08)	R	0	00: 10G 11: 1G
5	SFP+_P9_Speed0(Port 08)	R	0	
4	SFP+_P9_Lane_number_1 (Port 08)	R	0	00: 1 lane
3	SFP+_P9_Lane_number_0 (Port 08)	R	0	
2	SFP+_P9_ Link-up/Activity (Port 08)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P9_LED_SFP+_A (Port 08)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P9_LED_SFP+_G (Port 08)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.32. Offset 0x2F SFP+_Port 09 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description

7	(Reserved)	R/W	0	
6	SFP+_P10_Speed1(Port 09)	R	0	00: 10G 11: 1G
5	SFP+_P10_Speed0(Port 09)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P10_ Link-up/Activity (Port 09)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P10_LED_SFP+_A (Port 09)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P10_LED_SFP+_G (Port 09)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.33. Offset 0x30 SFP+ Port 10 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P11_Speed1(Port 10)	R	0	00: 10G 11: 1G
5	SFP+_P11_Speed0(Port 10)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P11_ Link-up/Activity (Port 10)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P11_LED_SFP+_A (Port 10)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P11_LED_SFP+_G (Port 10)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.34. Offset 0x31 SFP+ Port 11 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P12_Speed1(Port 11)	R	0	00: 10G 11: 1G
5	SFP+_P12_Speed0(Port 11)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P12_ Link-up/Activity (Port 11)	R	0	0: The Led light is off. 1: The Led light is on.

				Toggle: Activity
1	P12_LED_SFP+_A (Port 11)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P12_LED_SFP+_G (Port 11)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.35. Offset 0x32 SFP+ Port 12 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P13_Speed1(Port 12)	R	0	00: 10G 11: 1G
5	SFP+_P13_Speed0(Port 12)	R	0	
4	SFP+_P13_Lane_number_1 (Port 12)	R	0	00: 1 lane
3	SFP+_P13_Lane_number_0 (Port 12)	R	0	
2	SFP+_P13_ Link-up/Activity (Port 12)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P13_LED_SFP+_A (Port 12)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P13_LED_SFP+_G (Port 12)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.36. Offset 0x33 SFP+ Port 13 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P14_Speed1(Port 13)	R	0	00: 10G 11: 1G
5	SFP+_P14_Speed0(Port 13)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P14_ Link-up/Activity (Port 13)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P14_LED_SFP+_A (Port 13)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P14_LED_SFP+_G (Port 13)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.37. Offset 0x34 SFP+ Port 15 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P15_Speed1(Port 14)	R	0	00: 10G 11: 1G
5	SFP+_P15_Speed0(Port 14)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P15_ Link-up/Activity (Port 14)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P15_LED_SFP+_A (Port 14)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P15_LED_SFP+_G (Port 14)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.38. Offset 0x35 SFP+ Port16 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P16_Speed1(Port 15)	R	0	00: 10G 11: 1G
5	SFP+_P16_Speed0(Port 15)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P16_ Link-up/Activity (Port 15)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P16_LED_SFP+_A (Port 15)	R/W	1	1: There is no link on the port. 0: **Amber** SFP+ port has a valid link at 1G. Flashing indicates activity.
0	P16_LED_SFP+_G (Port 15)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.39. Offset 0x36 SFP28_Port 16 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P17_Speed1 (SFP28_Port 16)	R	0	00: 10G 10: 25G
5	SFP+_P17_Speed0 (SFP28_Port 16)	R	0	

4	SFP+_P17_Lane_number_1 (SFP28_Port 16)	R	0	00: 1 lane
3	SFP+_P17_Lane_number_0 (SFP28_Port 16)	R	0	
2	SFP+_P17_ Link-up/Activity (SFP28_Port 16)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P17_LED_SFP+_A (SFP28_Port 16)	R/W	1	1: There is no link on the port. 0: **Blue** SFP+ port has a valid link at 25G. Flashing indicates activity.
0	P17_LED_SFP+_G (SFP28_Port 16)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.40. Offset 0x37 SFP28_Port 17 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P18_Speed1 (SFP28_Port 17)	R	0	00: 10G 10: 25G
5	SFP+_P18_Speed0 (SFP28_Port 17)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P18_ Link-up/Activity (SFP28_Port 17)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P18_LED_SFP+_A (SFP28_Port 17)	R/W	1	1: There is no link on the port. 0: **Blue** SFP+ port has a valid link at 25G. Flashing indicates activity.
0	P18_LED_SFP+_G (SFP28_Port 17)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.41. Offset 0x38 SFP28_Port 18 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P19_Speed1 (SFP28_Port 18)	R	0	00: 10G 10: 25G
5	SFP+_P19_Speed0 (SFP28_Port 18)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P19_ Link-up/Activity (SFP28_Port 18)	R	0	0: The Led light is off. 1: The Led light is on.

				Toggle: Activity
1	P19_LED_SFP+_A (SFP28_Port 18)	R/W	1	1: There is no link on the port. 0: **Blue** SFP+ port has a valid link at 25G. Flashing indicates activity.
0	P19_LED_SFP+_G (SFP28_Port 18)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.42. Offset 0x39 SFP28_Port 19 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P20_Speed1 (SFP28_Port 19)	R	0	00: 10G 10: 25G
5	SFP+_P20_Speed0 (SFP28_Port 19)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P20_ Link-up/Activity (SFP28_Port 19)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P20_LED_SFP+_A (SFP28_Port 19)	R/W	1	1: There is no link on the port. 0: **Blue** SFP+ port has a valid link at 25G. Flashing indicates activity.
0	P20_LED_SFP+_G (SFP28_Port 19)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.43. Offset 0x3A SFP28_Port 20 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P21_Speed1 (SFP28_Port 20)	R	0	00: 10G 10: 25G
5	SFP+_P21_Speed0 (SFP28_Port 20)	R	0	
4	SFP+_P21_Lane_number_1 (SFP28_Port 20)	R	0	
3	SFP+_P21_Lane_number_0 (SFP28_Port 20)	R	0	
2	SFP+_P21_ Link-up/Activity (SFP28_Port 20)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P21_LED_SFP+_A (SFP28_Port 20)	R/W	1	1: There is no link on the port. 0: **Blue** SFP+ port has a valid link at 25G. Flashing indicates activity.

0	P21_LED_SFP+_G (SFP28_Port 20)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.44. Offset 0x3B SFP28_Port 21 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P22_Speed1 (SFP28_Port 21)	R	0	00: 10G 10: 25G
5	SFP+_P22_Speed0 (SFP28_Port 21)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P22_ Link-up/Activity (SFP28_Port 21)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P22_LED_SFP+_A (SFP28_Port 21)	R/W	1	1: There is no link on the port. 0: **Blue** SFP+ port has a valid link at 25G. Flashing indicates activity.
0	P22_LED_SFP+_G (SFP28_Port 21)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.45. Offset 0x3C SFP28_Port 22 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P23_Speed1 (SFP28_Port 22)	R	0	00: 10G 10: 25G
5	SFP+_P23_Speed0 (SFP28_Port 22)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P23_ Link-up/Activity (SFP28_Port 22)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P23_LED_SFP+_A (SFP28_Port 22)	R/W	1	1: There is no link on the port. 0: **Blue** SFP+ port has a valid link at 25G. Flashing indicates activity.
0	P23_LED_SFP+_G (SFP28_Port 22)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.46. Offset 0x3D SFP28_Port 23 LED (Read& Write)

Bit	Name	R/W	Reset Value	Description
7	(Reserved)	R/W	0	
6	SFP+_P24_Speed1 (SFP28_Port 23)	R	0	00: 10G 10: 25G
5	SFP+_P24_Speed0 (SFP28_Port 23)	R	0	
4	(Reserved)	R/W	0	
3	(Reserved)	R/W	0	
2	SFP+_P24_ Link-up/Activity (SFP28_Port 23)	R	0	0: The Led light is off. 1: The Led light is on. Toggle: Activity
1	P24_LED_SFP+_A (SFP28_Port 23)	R/W	1	1: There is no link on the port. 0: **Blue** SFP+ port has a valid link at 25G. Flashing indicates activity.
0	P24_LED_SFP+_G (SFP28_Port 23)	R/W	1	1: There is no link on the port. 0: **Green** SFP+ port has a valid link at 10G. Flashing indicates activity.

2.4.3.47. Offset 0x50 Reset(Read& Write)

Bit	Name	R/W	Reset Value	Description
7:1	(Reserved)	R/W	0	
0	CPLD_RST	R/W	1	1: The Device is in normal operating state 0: The Device is in reset state

2.4.4. Fan Board CPLD

The following features are available with the CPLD:

- FAN speed adjustment
- Fan detection
- Reset
- JTAG
- Interrupt

2.4.4.1. CPLD register

Address	Register	R/W	Default value
0x01	CPLD version	Read Only	0x01
0x04	Fan	Read&	0x80

	CPLD Reset	Write	
0x05	Interrupt Status	Read& Write	0xE0
0x06	Interrupt Mask	Read& Write	0x00
0x0F	Fan Module Present	Read Only	0xFF
0x12	Front Fan4 Module Speed	Read Only	0x00
0x13	Front Fan3 Module Speed	Read Only	0x00
0x14	Front Fan2 Module Speed	Read Only	0x00
0x15	Front Fan1 Module Speed	Read Only	0x00
0x16	Front Fan0 Module Speed	Read Only	0x00
0x41	Fan4 Module PWM	Read& Write	0x09
0x42	Fan3 Module PWM	Read& Write	0x09
0x43	Fan2 Module PWM	Read& Write	0x09
0x44	Fan1 Module PWM	Read& Write	0x09
0x45	Fan0 Module PWM	Read& Write	0x09

Table 6 Fan CPLD I/O Register Table

2.4.4.2. Offset 0x01 CPLD version (ReadOnly)

Bit	Name	R/W	Reset Value	Description
7:0	CPLD_ver[7:0]	R	001	[7:3]: Reserved [2:0]: CPLD version

2.4.4.3. Offset 0x04 Fan CPLD Reset (Read & Write)

Bit	Name	R/W	Reset	Description

			Value	
7	Reset_CPLD	R/W	1	1: CPLD is placed in normal operation state. 0: CPLD is placed in reset state.
6:0	(Reserved)	R/W	0	

2.4.4.4. Offset 0x05 Interrupt Status (Read Only)

Bit	Name	R/W	Reset Value	Description
7	FAN_INT	R/W	1	1: No interrupt 0: There is INTR to CPU
6	FAN_idle	R/W	1	1: Fan module normal operating 0: Fan module stop operating
5	FAN_PW_EN	R/W	1	1: Fan power enable 0: Fan power disable
4:0	(Reserved)	R/W	0	

2.4.4.5. Offset 0x06 Interrupt Mask (Read Only)

Bit	Name	R/W	Reset Value	Description
7	FAN_INT_MASK	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
6	FAN_idle_MASK	R/W	0	1: System Interrupt function enable 0: System Interrupt function disable
5:0	(Reserved)	R/W	0	

2.4.4.6. Offset 0x0F Fan Module Present (Read Only)

Bit	Name	R/W	Reset Value	Description
7:5	(Reserved)	R/W	0	
4	FAN5_PRES (FAN4)	R	1	1: Fan5 isn't inserted

				0: Fan5 is inserted
3	FAN4_PRES (FAN3)	R	1	1: Fan4 isn't inserted 0: Fan4 is inserted
2	FAN3_PRES (FAN2)	R	1	1: Fan3 isn't inserted 0: Fan3 is inserted
1	FAN2_PRES (FAN1)	R	1	1: Fan2 isn't inserted 0: Fan2 is inserted
0	FAN1_PRES (FAN0)	R	1	1: Fan1 isn't inserted 0: Fan1 is inserted

2.4.4.7. Offset 0x10 Fan Module Direction (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	(Reserved)	R/W	0	

2.4.4.8. Offset 0x12 Front Fan4 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN1_SENSOR (FAN4)	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

2.4.4.9. Offset 0x13 Front Fan3 Module Speed(Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN2_SENSOR (FAN3)	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

2.4.4.10. Offset 0x14 Front Fan2 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN3_SENSOR (FAN2)	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

2.4.4.11. Offset 0x15 Front Fan1 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN4_SENSOR (FAN1)	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms Fan speed (RPM) = Reg_value * 100 EX: register value : 80

				The RPM value is 80*100 = 8000

2.4.4.12. Offset 0x16 Front Fan0 Module Speed (Read Only)

Bit	Name	R/W	Reset Value	Description
7:0	FAN5_SENSOR (FAN0)	R	0	0: Fan failed 1 ~ 255: the number of fan rotations in 600ms Fan speed (RPM) = Reg_value * 100 EX: register value : 80 The RPM value is 80*100 = 8000

2.4.4.13. Offset 0x41 Fan4 Module PWM (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	(Reserved)	R/W	0	
3:0	FAN_PWM_1 (FAN4)	R/W	1001	0100 : 5 x 6.25% = 31.5% duty cycle 0101 : 6 x 6.25% = 37.5% duty cycle 0110: 7 x 6.25% = 43.75% duty cycle …… 1110: 15 x 6.25% = 93.75% duty cycle 1111: 16 x 6.25% = 100% duty cycle

2.4.4.14. Offset 0x42 Fan3 Module PWM (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	(Reserved)	R/W	0	
3:0	FAN_PWM_2 (FAN3)	R/W	1001	0100 : 5 x 6.25% = 31.5% duty cycle 0101 : 6 x 6.25% = 37.5% duty cycle 0110: 7 x 6.25% = 43.75% duty cycle …… 1110: 15 x 6.25% = 93.75% duty cycle 1111: 16 x 6.25% = 100% duty cycle

2.4.4.15. Offset 0x43 Fan2 Module PWM (Read& Write)

Bit	Name	R/W	Reset	Description

			Value	
7:4	(Reserved)	R/W	0	
3:0	FAN_PWM_3 (FAN2)	R/W	1001	0100 : 5 x 6.25% = 31.5% duty cycle 0101 : 6 x 6.25% = 37.5% duty cycle 0110: 7 x 6.25% = 43.75% duty cycle …… 1110: 15 x 6.25% = 93.75% duty cycle 1111: 16 x 6.25% = 100% duty cycle

2.4.4.16. Offset 0x44 Fan1 Module PWM (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	(Reserved)	R/W	0	
3:0	FAN_PWM_4 (FAN1)	R/W	1001	0100 : 5 x 6.25% = 31.5% duty cycle 0101 : 6 x 6.25% = 37.5% duty cycle 0110: 7 x 6.25% = 43.75% duty cycle …… 1110: 15 x 6.25% = 93.75% duty cycle 1111: 16 x 6.25% = 100% duty cycle

2.4.4.17. Offset 0x45 Fan0 Module PWM (Read& Write)

Bit	Name	R/W	Reset Value	Description
7:4	(Reserved)	R/W	0	
3:0	FAN_PWM_5 (FAN0)	R/W	1001	0100 : 5 x 6.25% = 31.5% duty cycle 0101 : 6 x 6.25% = 37.5% duty cycle 0110: 7 x 6.25% = 43.75% duty cycle …… 1110: 15 x 6.25% = 93.75% duty cycle 1111: 16 x 6.25% = 100% duty cycle