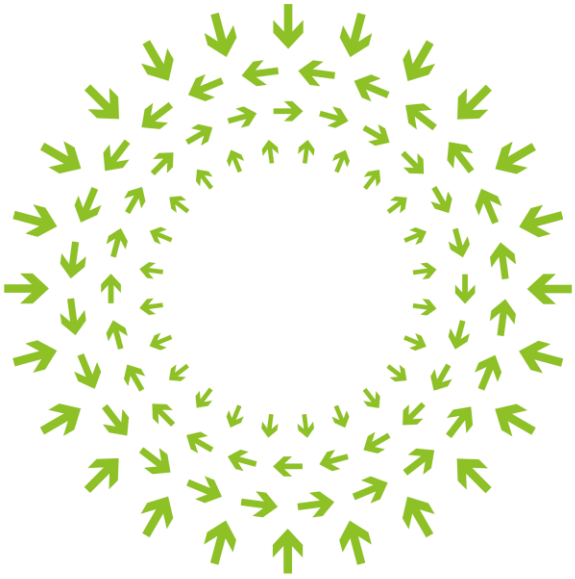


OPEN

Compute Project

MSX1400-OCP

Author: Shy Zimmerman

1 Scope

This document defines the technical specifications for the MSX1400-OCP switch used in Open Compute Project

2 Contents

3 Overview

The MSX1400-OCP switch is a top of rack switch with 48 ports of 10GbE and 12 uplink ports of 40GbE for non-blocking throughput between rack and aggregation layer. Based on advanced hardware design, this switch packs 48 SFP+ and 12 QSFP interfaces in an ultra-dense 1U form factor. The MSX1400-OCP features latency of 250ns and power efficiency, while providing optimal performance for open rack based enterprise data centers, financial services, Web 2.0, high performance computing and cloud computing applications.

4 License

5 Mechanical

5.1 Mechanical System Overview

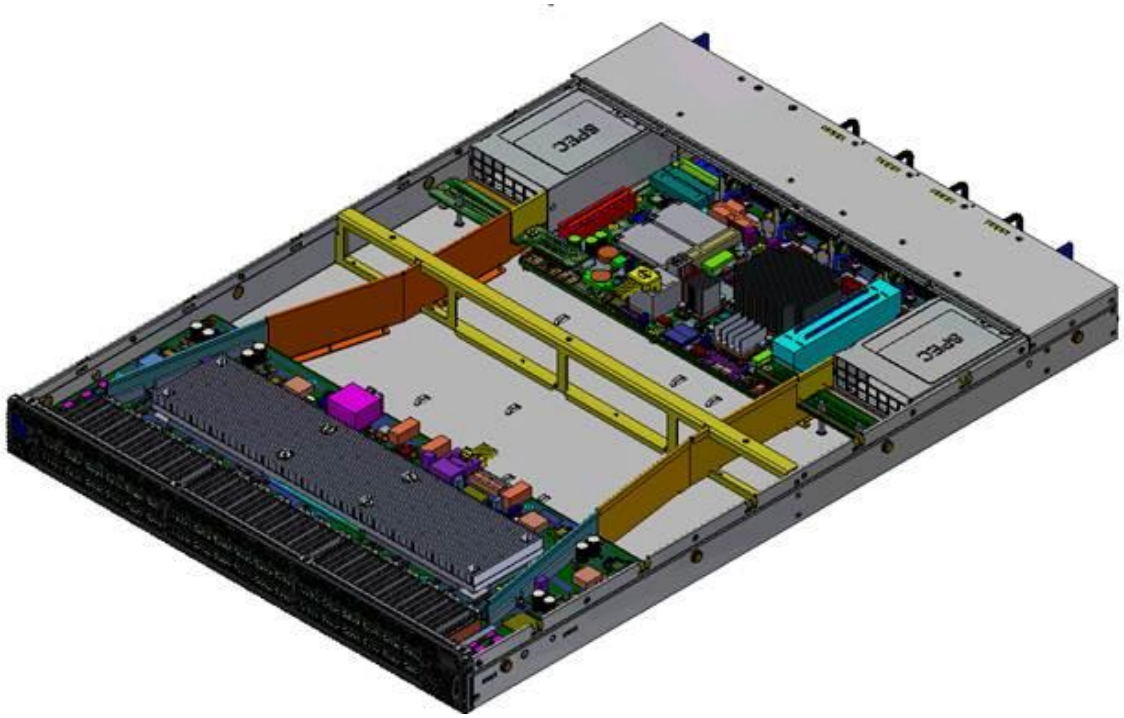


Figure 1 - Mechanical System Overview

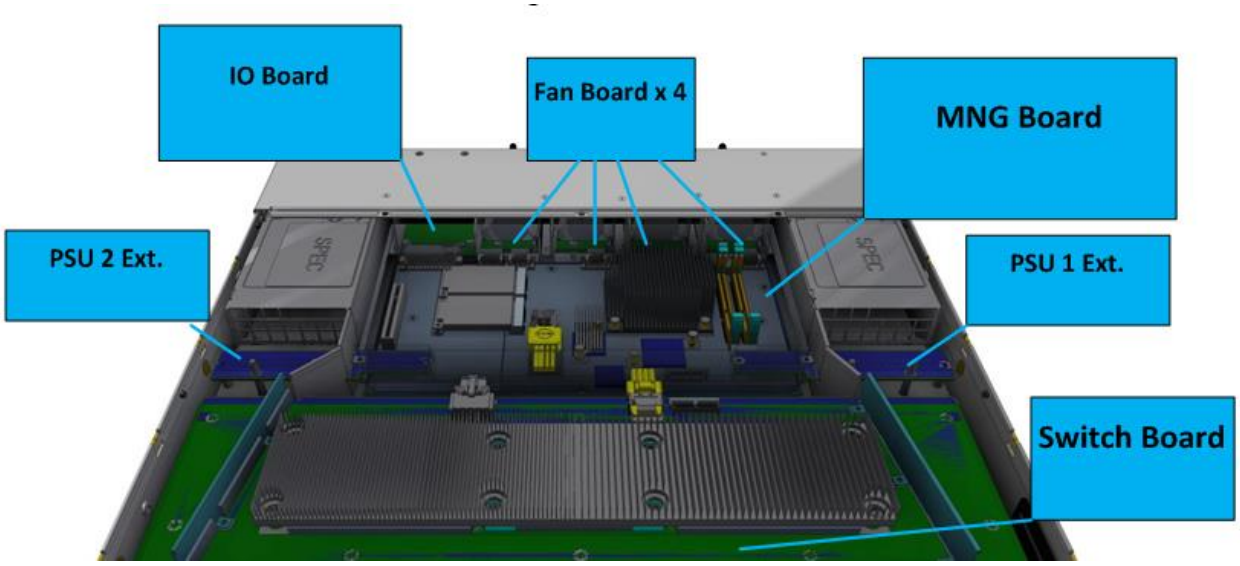


Figure 2 - Main Components

5.2 Switch Dimensions (in mm)

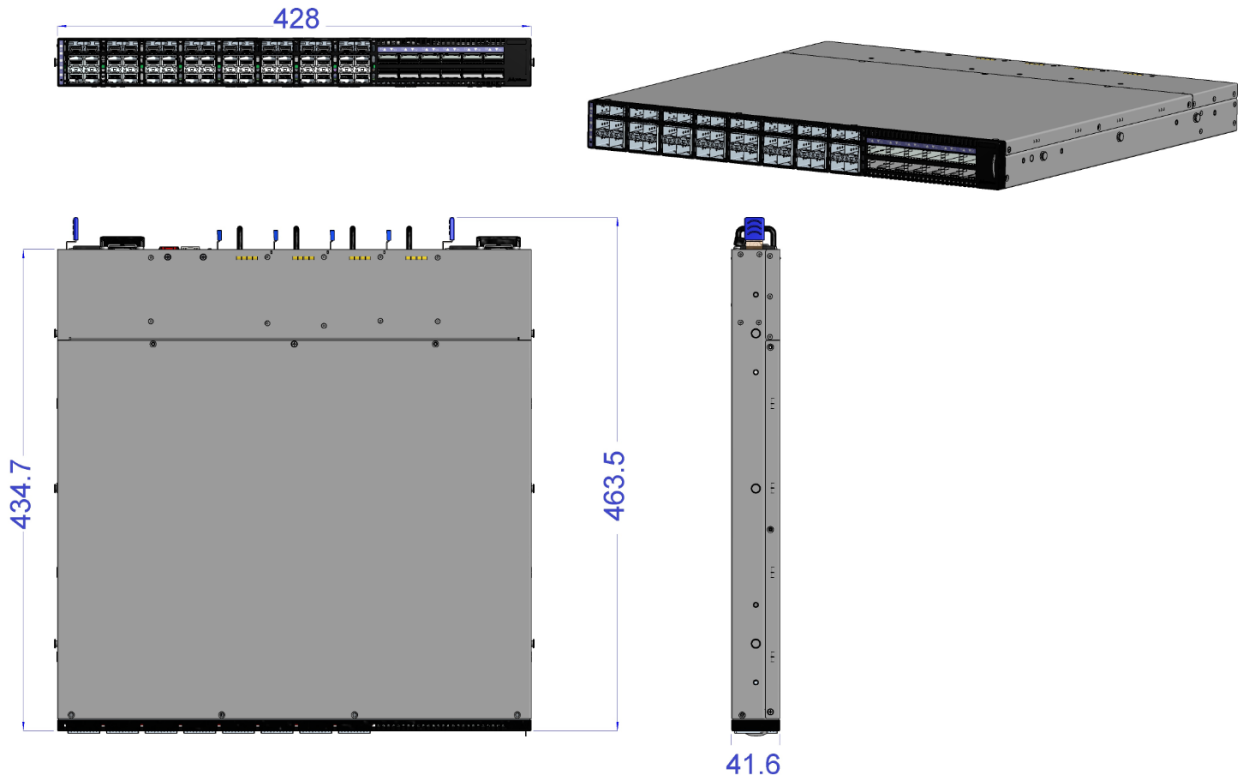


Figure 3: Switch Dimensions

5.3 Fan Unit Dimension (in mm)

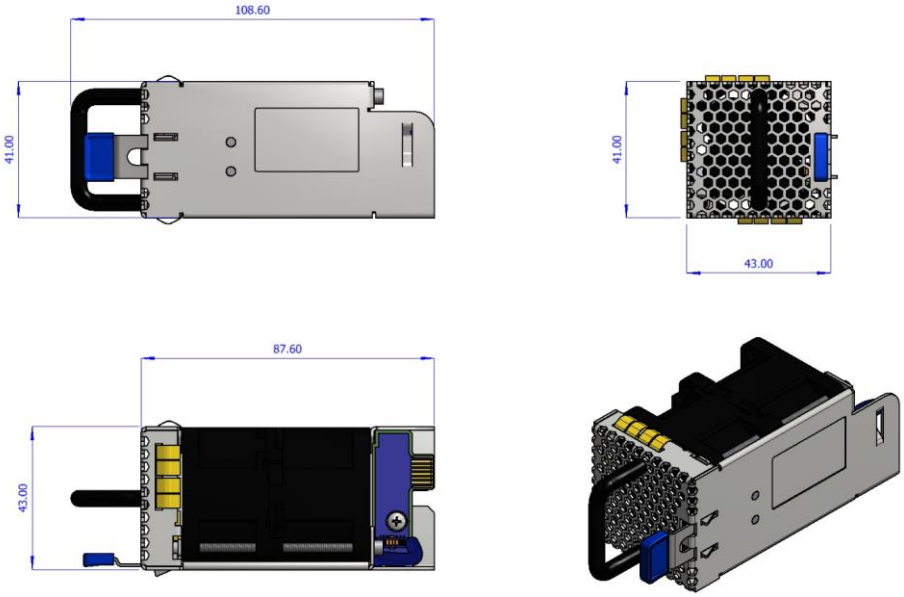


Figure 4: Fan Unit Dimensions

5.4 Power Supply Dimensions (in mm)

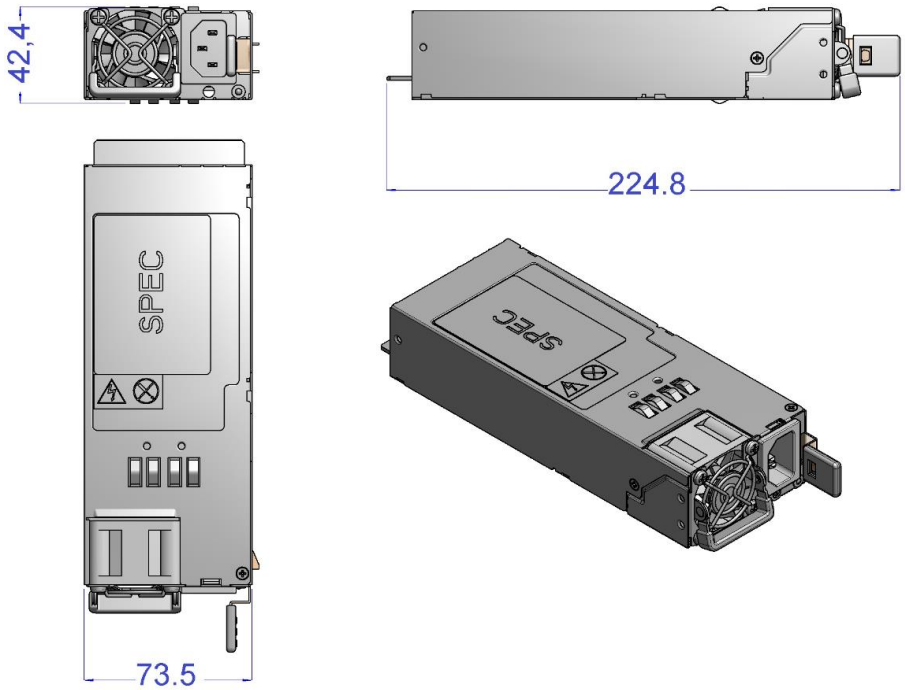


Figure 5: Power Supply Dimensions

5.5 SFP+ Port Assembly

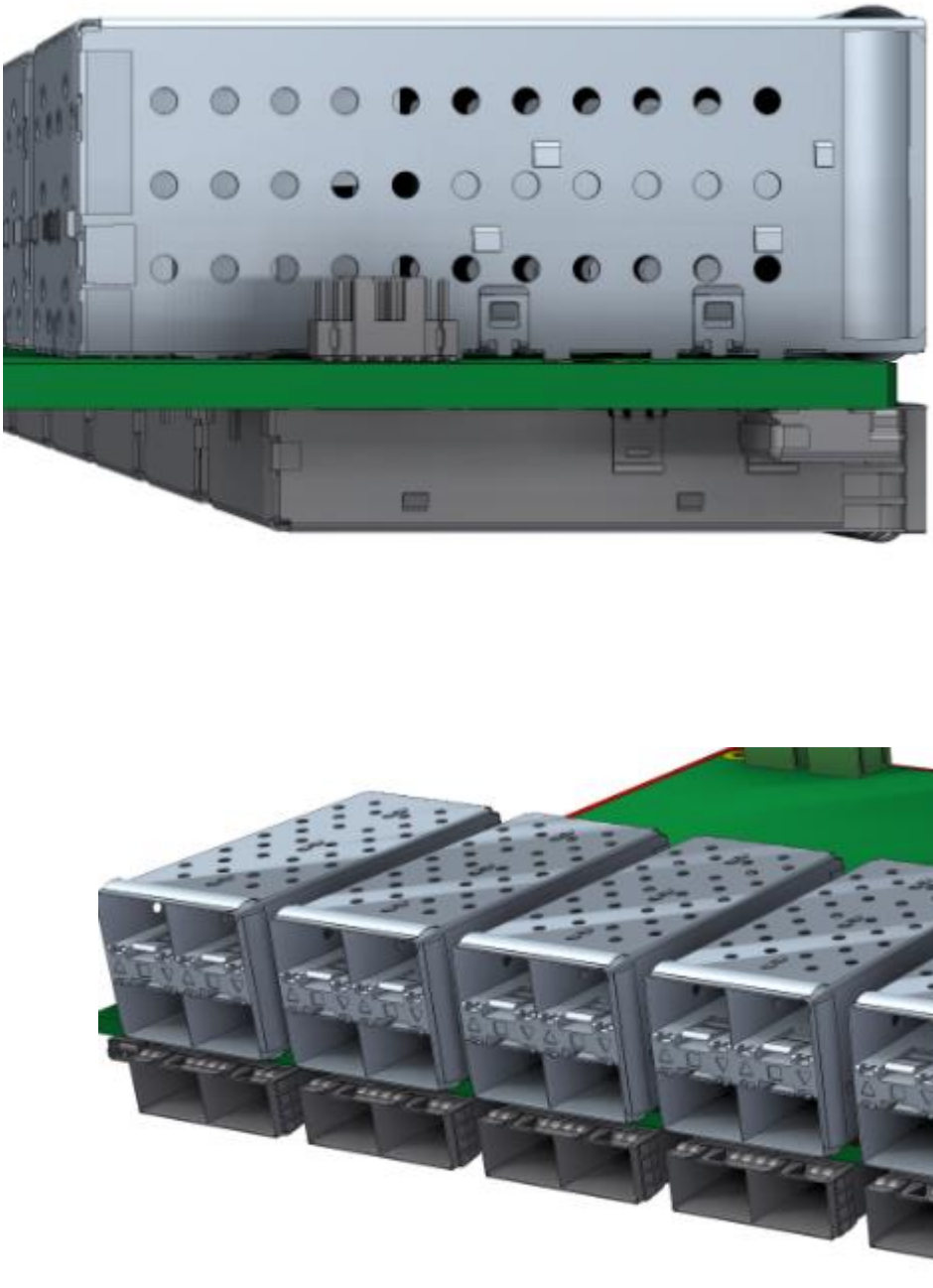


Figure 6: SFP+ Assembly on MSX1400-OCP

6 MSX1400-OCP Features

6.1 Electrical Features

6.1.1 Port Configurations – Based on SwitchX-2™

With each new generation of technology, server sizes shrink. Whereas in the past all servers occupied the entire rack width (19”), it is quite common today to find different racking solutions that allow fitting two servers on the same rack shelf, yielding a total of 56, 60 or more servers in the same rack.

Since most commercially available ToR switches have 48 10GbE ports, connecting more than 48 servers in this rack would require two ToR switches. These two switches increase the rack cost, latency and energy consumption, and occupy space that could have been allocated for servers.

This problem is solved by the port flexibility of the MSX1400-OCP switch. By simple configuration, its 40GbE ports can be configured to 10GbE and support more servers. For example, the MSX1400-OCP can be configured with 60 ports of 10GbE and 4 ports of 40GbE. This configuration connects 60 servers with an uplink of 160Gb/s, or oversubscription of 3.75:1. If configuring the four uplink ports to operate at 56GbE, the oversubscription ratio improves to 2.68:1. Alternatively, the MSX1400-OCP can be configured with 56 ports of 10GbE and 8 ports of 40GbE. This configuration connects 56 servers with an uplink of 320Gb/s, or oversubscription of 1.75:1.

A listing of all possible port configurations can be found in ***Table 1***.

40GbE/56GbE ports	12	10	8	6	4	2	0
10GbE ports	48	52	56	58	60	62	64

Table 1: MSX1400-OCP Ports Configuration

Figure 7: MSX1400-OCP Ports Panel

6.1.1.1 Cable Support

- SR
- SR4
- LR
- LR4
- DAC

6.1.2 Management I/O Interfaces

- 2x 10/100/1000BASE-T RJ-45 Ethernet port
- 1x RS232/I2C RJ-45 Console connector
- 1x USB connector

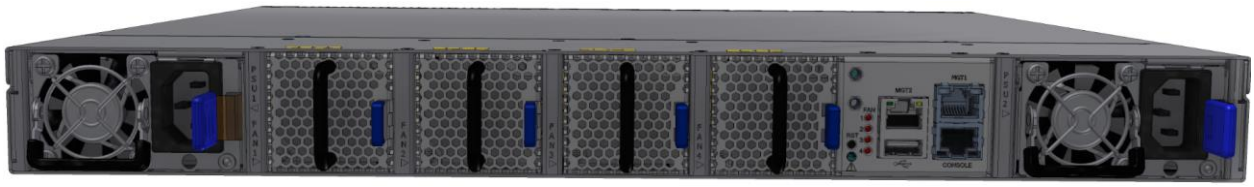


Figure 8: Management I/O interfaces

6.1.3 Field Replaceable Units - FRU

- 3+1 redundant fan field replaceable modules. Can support a dual fan pack in each module
- 1+1 redundant field replaceable power supplies. Two optional power supplies:
    - AC/DC 90-240Vac inlet - 460W
    - DC/DC 48vdc inlet - 800W

6.1.4 Management

- CPU: Intel Ivy Bridge
    - Supports all flavors:
        - Celeron
        - i3
        - i5
        - i7
- Chipset: Intel QM77 (Panther Point)
- Up to two 1600MTs, 8GB (Each), DDR3, ECC SO-DIMM modules
- Supports up to two SATA-slim 4/8/16/64GB SLC or MLC SSD modules
- BIOS Field upgrade with fail safe
- Real time clock 24H-SuperCap (optional battery)
- 4x CPLDs with field upgrade and fails safe capabilities

7 MSX1400-OCP Blocks

7.1 Main Block Diagram

The following block diagram specifies the main blocks in the MSX1400-OCP switch:

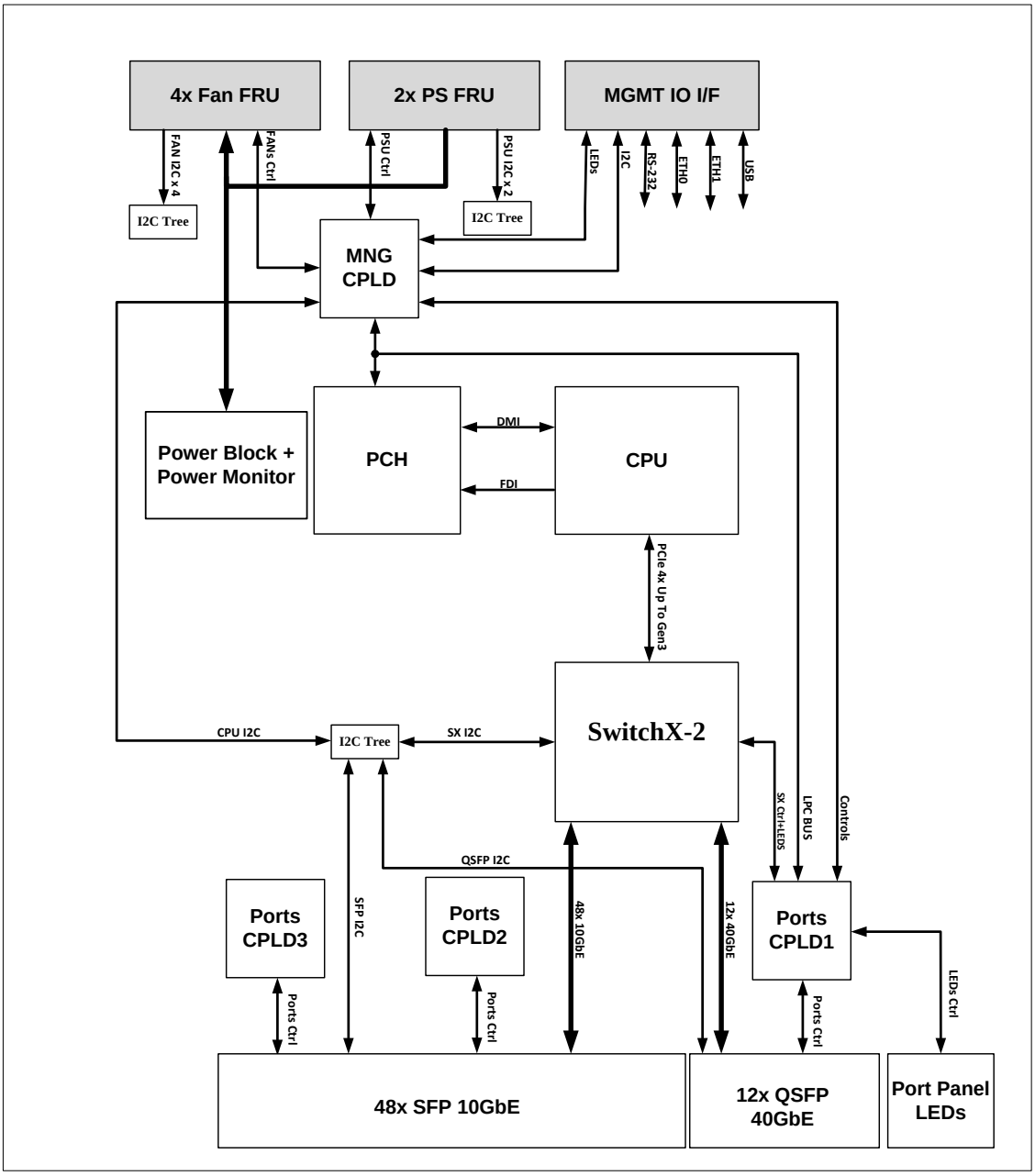
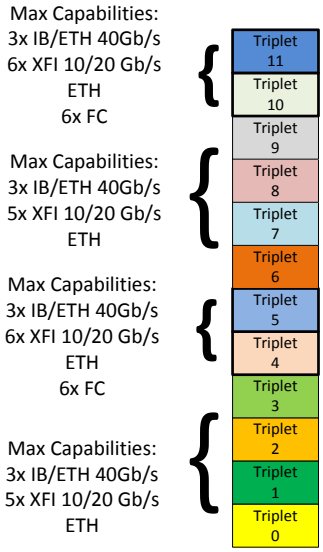


Figure 9: MSX1400-OCP Main Block Diagram

7.2 SwitchX-2™ Block

There are 12x40GbE QSFP ports and 48x10GbE SFP+ ports towards the panel from the SwitchX-2. The following diagrams show SwitchX-2 breakout capabilities and the general fan-out of ETH signals on the MSX1400-OCP accordingly:



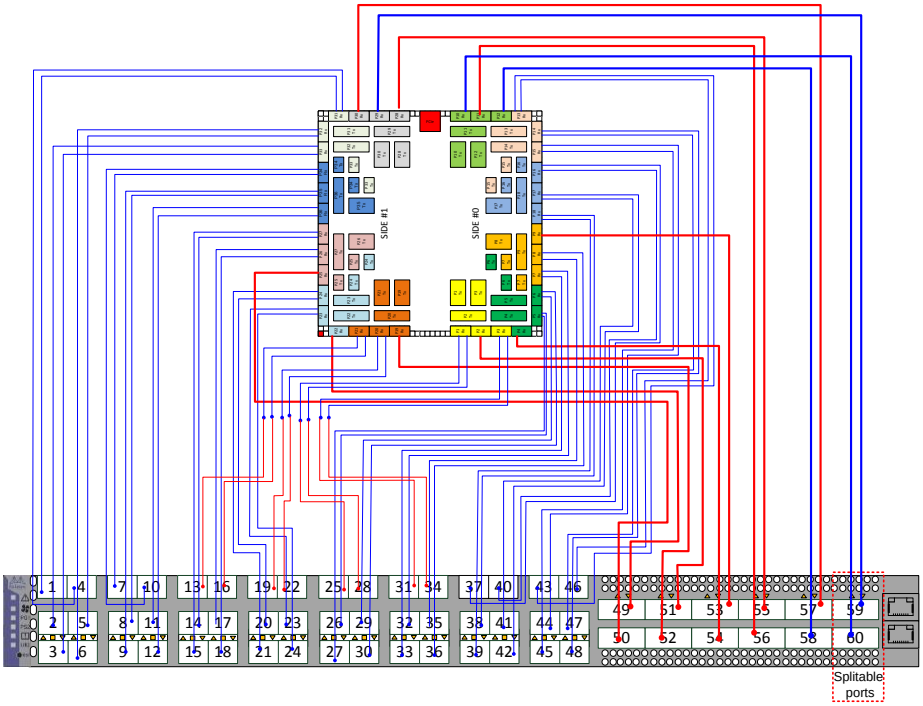


Figure 10: SwitchX-2™ Breakout Capabilities and Layout

Table 2 specifies the x1/x4 ports mapping in the MSX1400-OCP:

Panel Port	HW Port	RX SerDes	TX SerDes
1	31	B	B
2	33	B	C
3	33	D	D
4	31	D	A
5	32	C	C
6	32	A	D
7	34	C	C
8	35	D	C
9	35	B	D
10	34	A	D
11	36	A	D
12	36	C	C
13	21	B	B
14	27	D	C
15	27	B	D
16	21	D	A
17	26	A	D
18	26	C	C
19	20	C	C
20	24	A	C
21	24	C	D
22	20	A	D
23	23	D	C
24	23	B	D
25	1	C	A
26	5	B	B
27	5	D	A
28	1	A	B
29	6	C	D
30	6	A	C

Panel Port	HW Port	RX SerDes	TX SerDes
31	3	A	A
32	7	B	D
33	7	D	C
34	3	C	B
35	8	C	D
36	8	A	C
37	16	B	D
38	18	D	D
39	18	B	C
40	16	D	C
41	17	A	A
42	17	C	B
43	13	D	C
44	15	A	C
45	15	C	D
46	13	B	D
47	14	D	B
48	14	B	C
49	22		
50	25		
51	2		
52	19		
53	9		
54	4		
55	11		
56	28		
57	30		
58	12		
59	29		
60	10		

Table 2 : MSX1400-OCP Port Mapping

7.2.1 SFP+ Interface

48 ports of the MSX1400-OCP have SFP+ connectors.
Each SFP+ connector supports the following:

Signal Name	Description	Type
TD+/TD-	High Speed Transmission pair	CML from SX to connector
RD+/RD-	High Speed Receive pair	CML from connector to SX
SCL/SDA	I2C slave interface address 0x50 or 0x51	Open Drain from SX to connector
TX Fault	Module transmitter fault	LVTTL from connector to CPLD
TX Disable	Turn off transmitter output (optical)	LVTTL from CPLD to connector
Mod ABS	Module absent (logic high)	Short to GND in module
RS0/RS1	RS0 – Receiver rate select RS1 – Transmitter rate select	LVTTL from CPLD to connector (short together)
RX LOS	Receiver loss of signal indication	LVTTL from connector to CPLD

Table 3 : SFP+ Interface

A single SFP+ interface on the MSX1400-OCP switch is illustrated in ***Figure 11***.

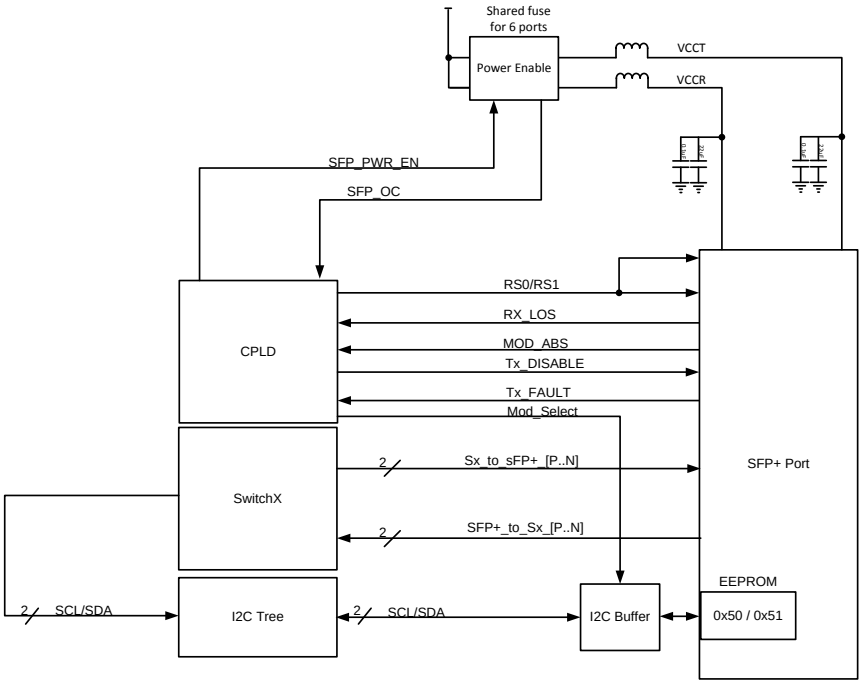


Figure 11 : SFP+ Interface

7.2.2 QSFP Interface

12 ports of the MSX1400-OCP are QSFP connectors.

Each QSFP connector supports the following:

Signal Name	Description	Type
TD+/TD-	High Speed Transmission pairs (x4)	CML from SX to connector
RD+/RD-	High Speed Receive pairs (x4)	CML from connector to SX
SCL/SDA	I2C slave interface address 0x50 or 0x51	Open Drain from SX to connector
ModSel	Module select for I2C communication to prevent bus conflicts	LVTTL from CPLD to connector
ResetL	Module reset use to reset all user module settings to their default state	LVTTL from CPLD to connector
IntL	Use to indicate the host for a fault or status critical.	OC from Connector to CPLD
ModPrsL	Module present	Short to GND in module
LPMod	When the module is in a low power mode it has a maximum power consumption of 1.5W	LVTTL from CPLD to connector

Table 4 : QSFP Interface

A single QSFP interface in the MSX1400-OCP board is presented in ***Figure 12***.

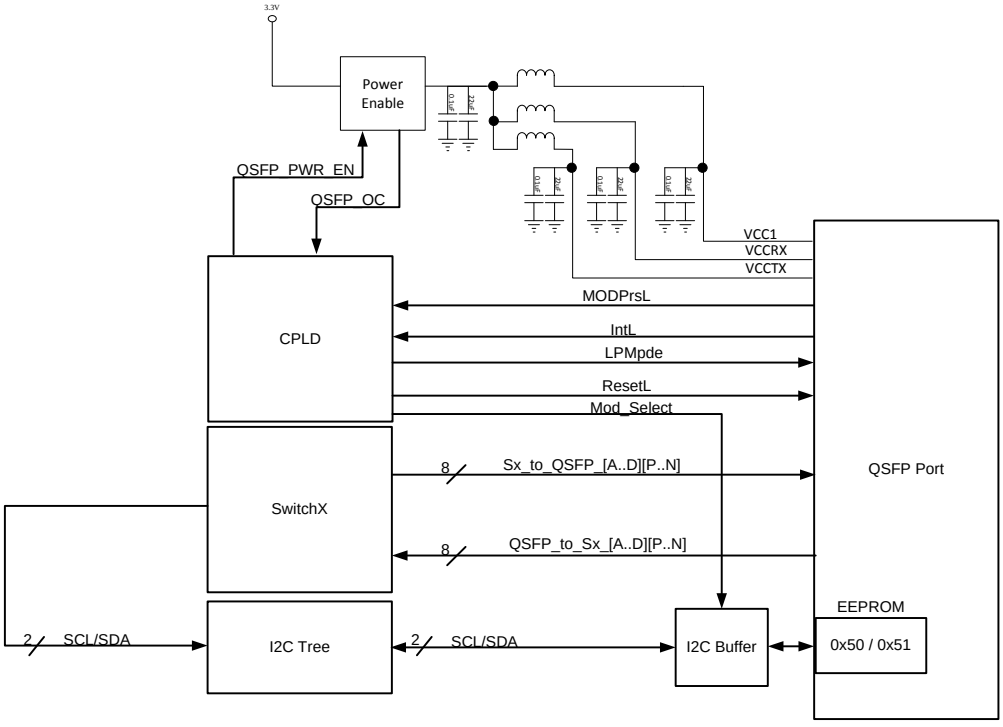


Figure 12 : QSFP Interface

7.2.3 Port over Current Protection

The power for every 4 QSFP/ 6 SFP modules is controlled by a current limited power distribution switch. All of these power limiting switches are controlled by QSFP_PWR_EN signals (default enabled), originated from the CPLD. When the output load exceeds the current limit threshold, the power switch limits the current to a safe level. In addition, the SFP/QSFP_OC signals are asserted low and create an interrupt event towards the CPU from the CPLD.

7.2.4 Port I2C Interface

CPLD controls the I2C switch and connected to SwitchX-2 secondary I2C bus. 60 different I2C buses are connected from I2C switch to the 60 MSX1400-OCP ports. MOD_SEL register selects which I2C bus will be open– each time only one bus can be open.

The main reason for using this CPLD buffering method is that all the QSFP modules have the same address (0x50). By separating the buses in the CPLD, Switch-X2 can select a specific module to communicate with. Another reason for selecting a different bus for each port is to isolate problematic modules from the others. This way, if a specific port is corrupted, it does not affect the other ports.

7.3 I2C

- MSX1400-OCP I2C tree has 4 optional masters:
    1. SW (LPC to I2C module)
    2. FW (SwitchX2)
    3. External connector
    4. BIOS (SMbus)
- The PCH does not support I2C, therefore, LPC to I2C module was implemented inside the MGMT CPLD.
- I2C switching is done by external switch devices. These devices are controlled by an I2C machine inside the CPLD. I2C channel access is controlled via relevant CPLD registers.
- The CPU and the I2C external connector are sharing the same switches.
- The I2C external connector is not connected directly to the head of the CPU I2C tree. Access to CPU I2C is granted by request to CPLD 0x80.
- When connection between the I2C external connector and the head of the tree is enabled, the CPU I2C connection to the head of the tree is disabled.
- In case of collision between masters, the following hierarchy will be implemented (decreasing order):
    1. Connector
    2. SW I2C register
    3. SW LPC register
    4. FW
- The I2C and the RS232 are sharing a single RJ45 connector.

The following diagram illustrates an I2C tree on MSX1400-OCP:

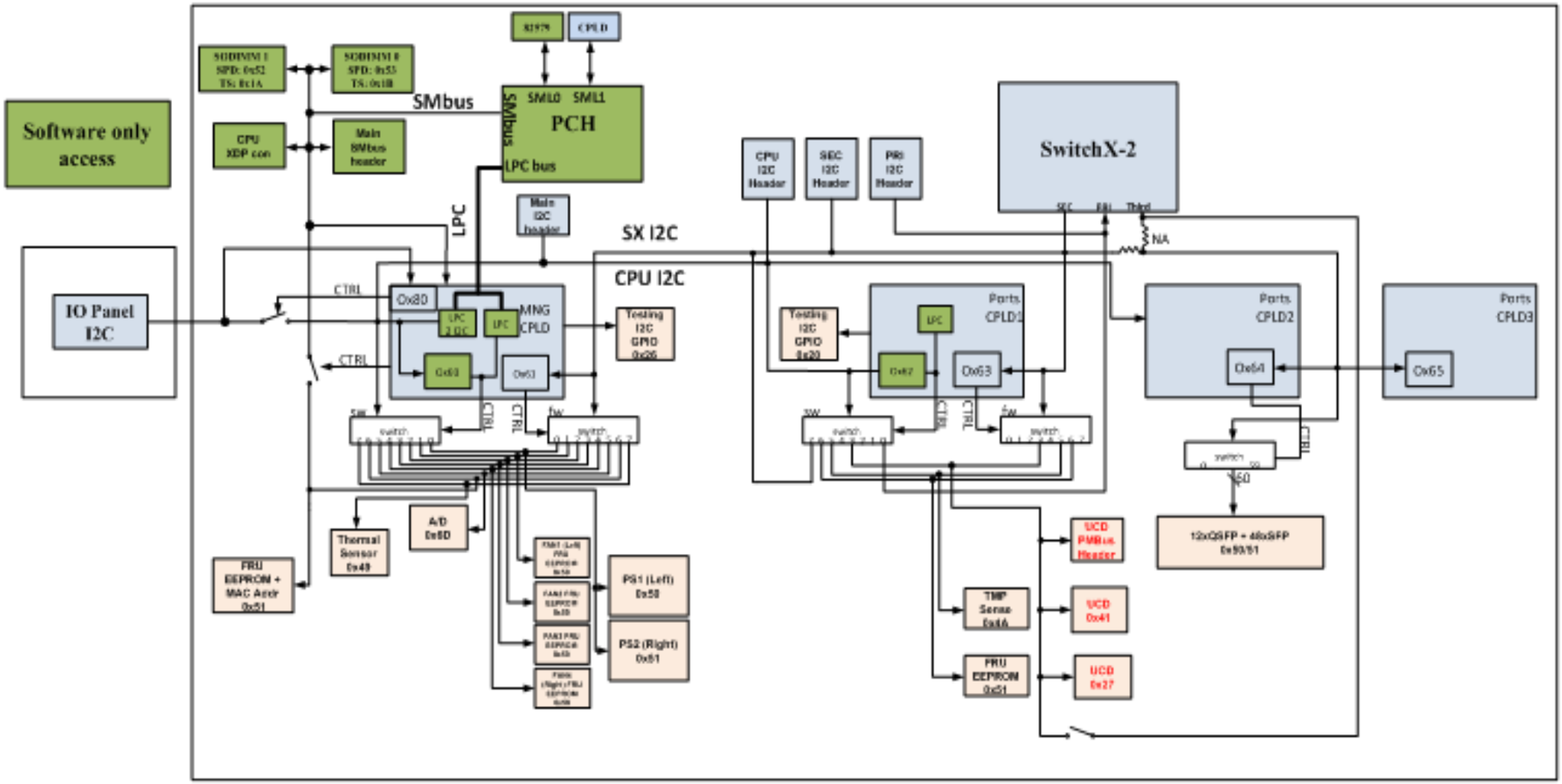


Figure 13: I2C Tree

7.4 CPLD

Four CPLD devices on the MSX1400-OCP provide monitoring and controlling capabilities:

1. MGMT CPLD: located on the MGMT board. Controls fans, PS, power sequence, software register map, software interrupt controller, firmware interrupt controller, reset controller, I2C switching, LEDs, CPU power and safe BIOS.
2. Ports CPLDs (1-3): controls LEDs, SwitchX-2 reset logic, power monitor, SwitchX-2 power sequence, I2C switching and ports control and monitor signals.

All CPLDs are powered from the auxiliary power; therefore, they are still functioning during main 12V rail shutdown.

7.4.1 CPLD Features

- Lattice XO2 CABGA332 device
- 4320 Logic elements
- 271 I/Os in four banks
- 96K bit UFM User flash memory
- 332-Pin FineLine BGA
- Fail-safe mechanism using SPI flash memory

7.4.2 CPLD Field Upgrade

All four CPLD devices can be field upgraded via SwitchX-2 JTAG emulation. Fail safe feature is supported in case of field upgrade failure for all CPLDs.

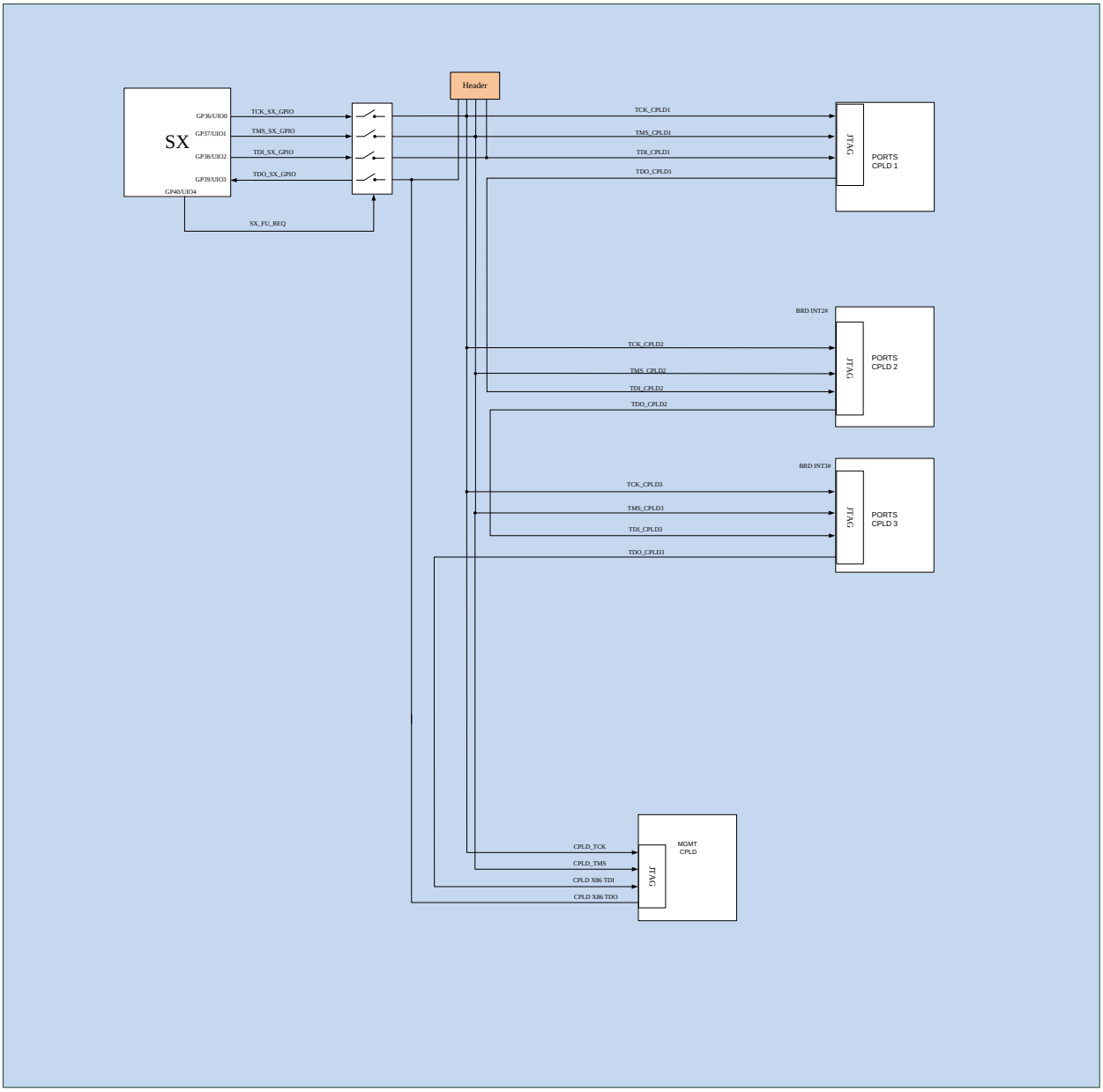


Figure 14: CPLD Field Upgrade

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7.5 SPI and Safe BIOS Mechanism

The Serial Peripheral Interface on the chipset supports two 64MB (each) flash devices, storing a Unified BIOS Code.

The MGMT board has two pairs of SPI flash devices: one serves as the default pair and the other serves as the safe BIOS pair.

The BIOS SPI interface is described in ***Figure 15***.

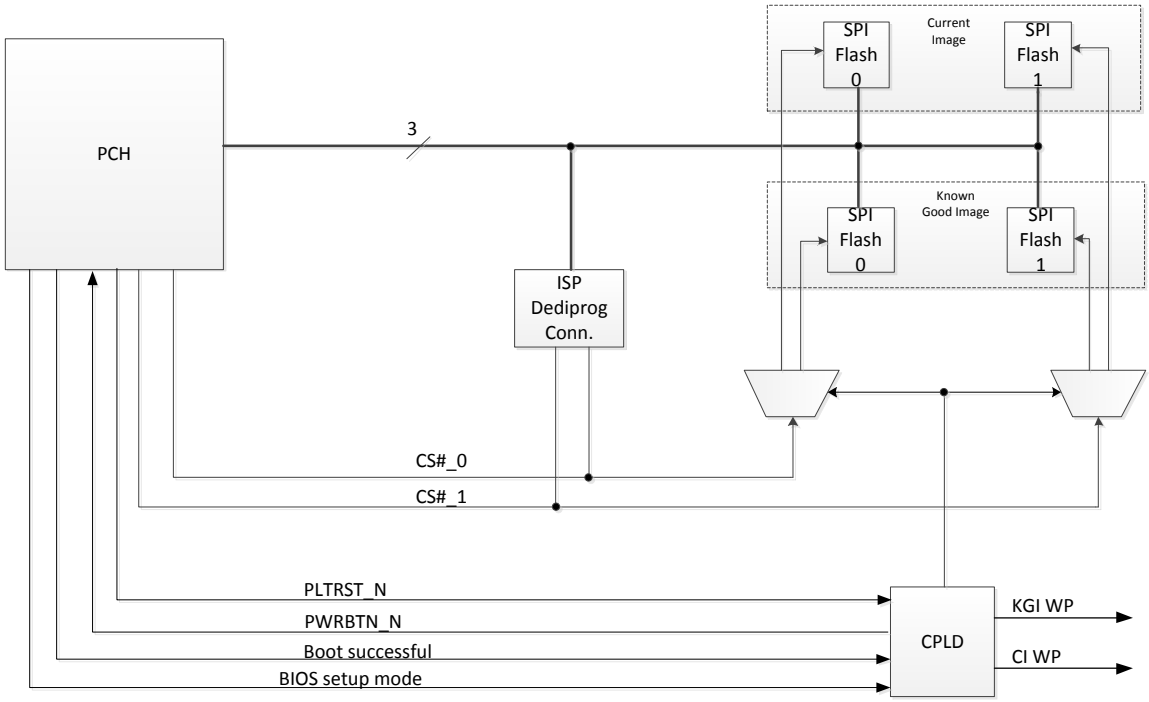

Figure 15: Safe BIOS Mechanism

The system has two SPI Flash pairs:

- Known Good Image (KGI) pair
- Current Image (CI) pair

Both of these pairs are loaded with identical images at the factory. The factory programmed images are the KGI images. The KGI image is never intended for update. The KGI provides an image to always recover the system.

The system always chooses the CI as the default boot device after power up. This selection is made by the CPLD.

Safe BIOS Events flow:

1. Initial boot: the default is CI.
2. When PLTRST_N is asserted (logic low) and then de-asserted, a timer starts inside the CPLD (this timer value can be a variable, based upon boot time of the system).
3. The CPLD then waits for “Boot Successful” bit driven by the BIOS.
4. If Boot Successful is high before the timer has been expired, then this is a normal boot.
5. If not, the mechanism starts working.
6. CPLD selects the KGI pair.
7. Then PWRBTN_N is asserted for 6 seconds, de-asserted for 5 seconds, asserted for 1 second and then released. This will power cycle the platform (PCH and CPU).
8. The system then boots from KGI.
9. After a successful boot, the CPLD selects the CI again.
10. At this stage, it is possible to recover the CI using BIOS FU mechanism.

In addition to the BOOT_SUCCESS signals, two other signals are connecting the PCH to the CPLD:

i. BIOS_SETUP_MODE - Asserted high by the PCH in case the user entered the setup menu. As long as this signal is high, the CPLD counter for boot success is paused.

ii. BIOS_STARTED - Asserted high by the PCH once BIOS load was started.

BOOT_SUCCESS and BIOS_STARTED are used for status LED control.

7.6 Ethernet

The MSX1400-OCP provides two Ethernet MDI 10/100/1000MB/s ports. One port is connected through internal PCH MAC and Intel 82579 PHY (port 1). The other port is connected through Intel 82583 MAC/PHY (port 2).

These two MDI ports are routed to two RJ45 ports on the FRU panel.

The Ethernet interface is displayed in ***Figure 16***.

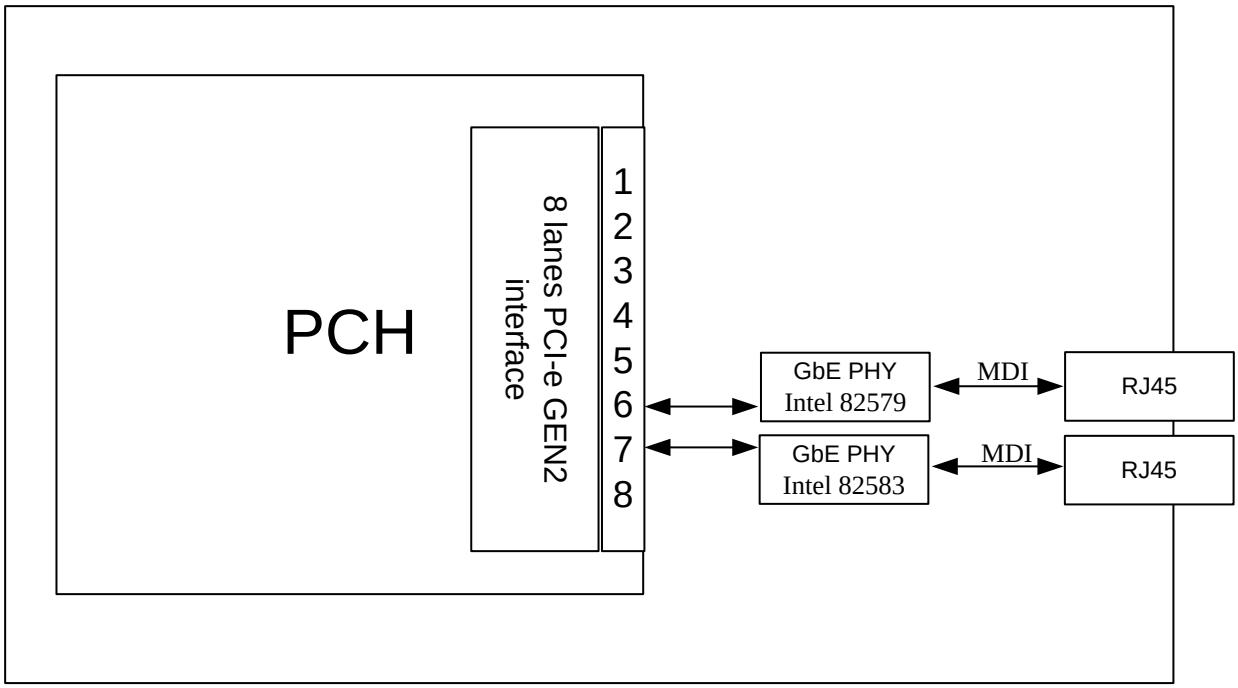

Figure 16: Ethernet Interface

7.7 RS232 Interface

The 8-pin RJ-45 connector provides CLI connectivity (RS-232) to the CPU. The I2C and the RS232 are sharing the same RJ45 connector. The RS-232 interface is shown in ***Figure 17***.

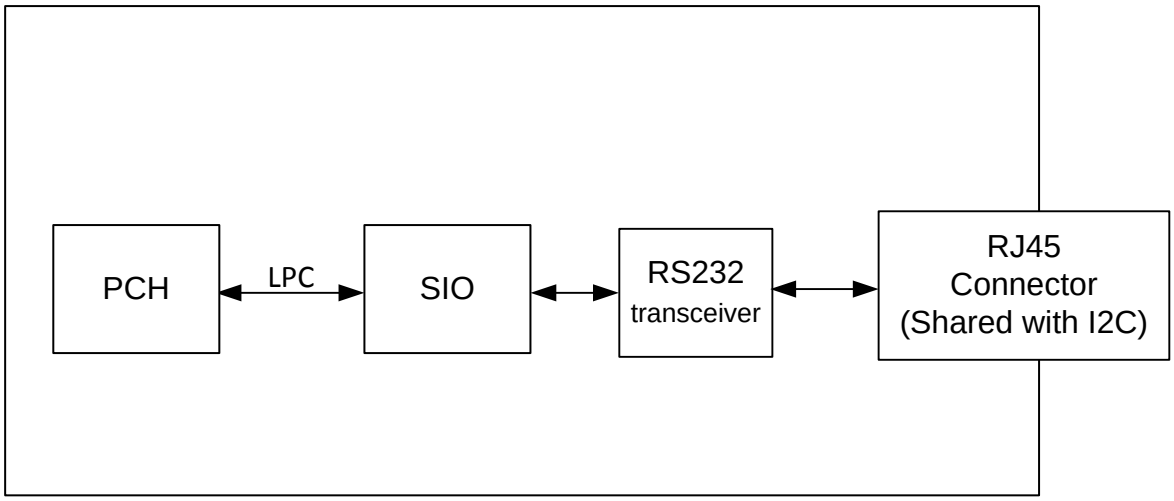

Figure 17: RS-232 Interface

7.8 USB

The system has one external USB 2.0 host interface for general use. The USB port can supply 500mA @ 5V and has internal current limiter with fault signal. ***Figure 18*** describes the USB interface.

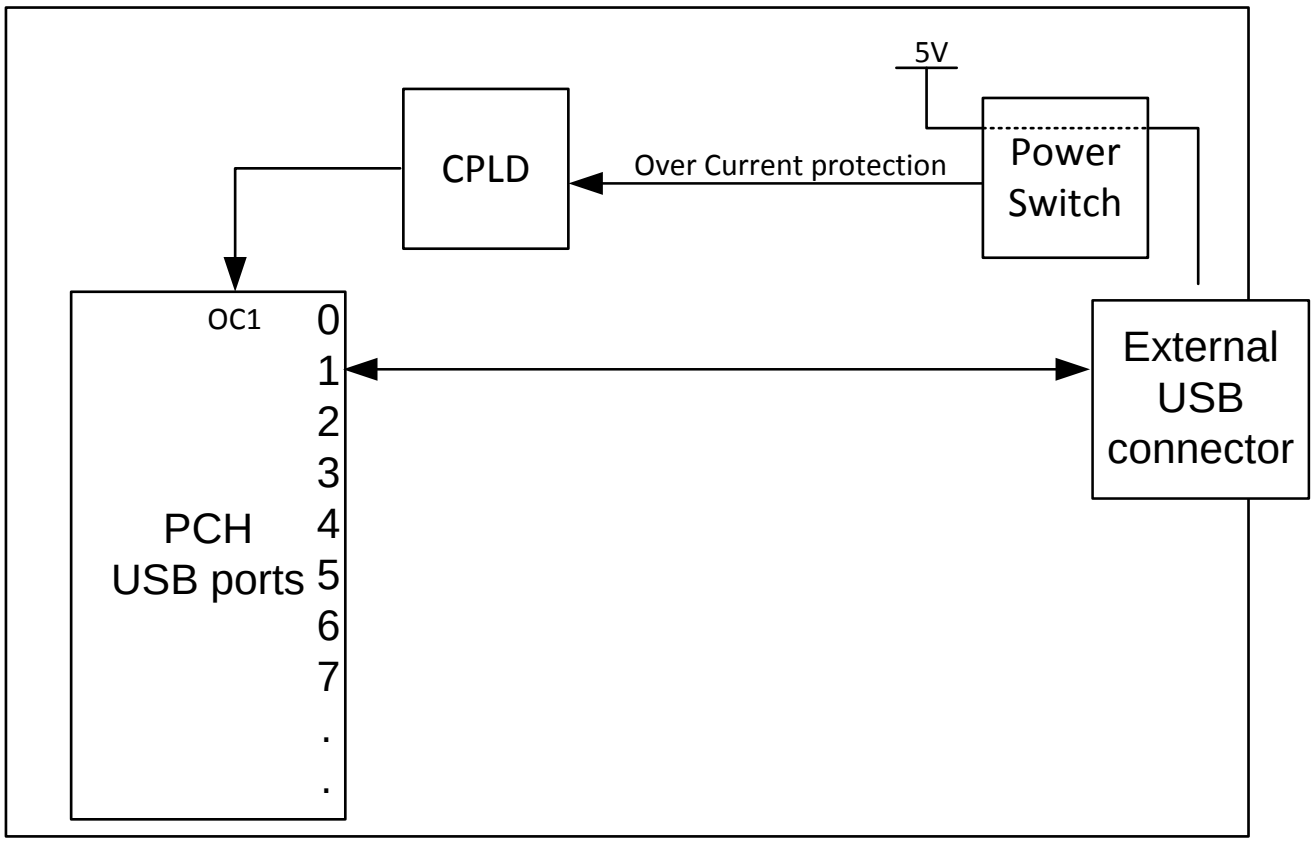

Figure 18: USB Interface

7.9 LPC

The PCH implements an LPC interface, as described in the Low Pin Count Interface Specification, Revision 1.1. The LPC interface from the PCH is shown in ***Figure 19***.

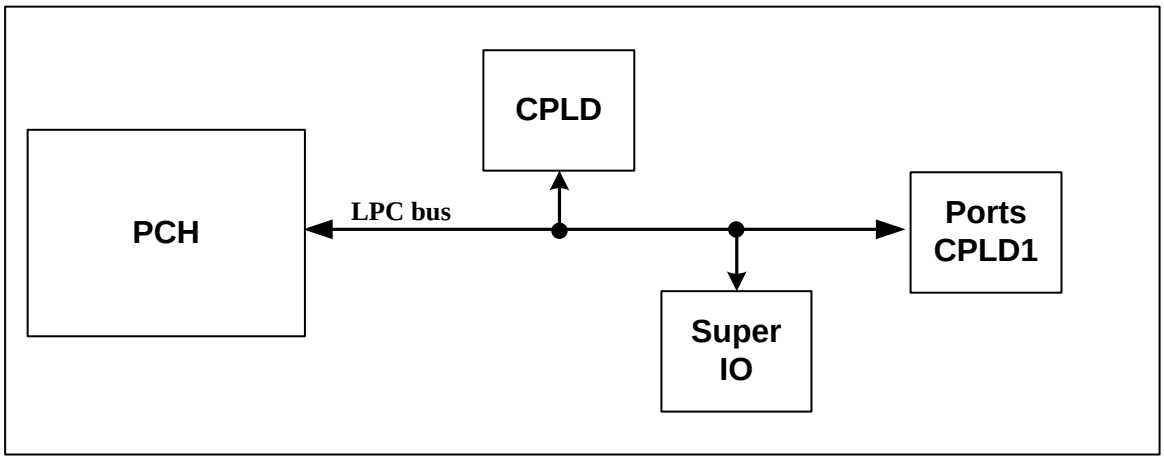

Figure 19: LPC Interface

7.10 SATA

Up to two mSATA SSD (Solid State Drive) modules are supported in the system. Each SSD supports 4-64GB SLC or MLC.

On power down sequence, both of the SSD modules are powered from Super capacitor, in order to perform a graceful shutdown. The super capacitors provide power to the SSD modules while the rest of the system is in shutdown mode.

The SATA interface is described in ***Figure 20***.

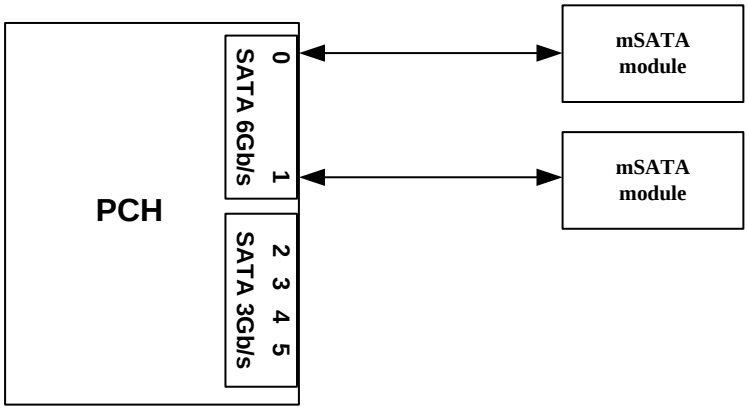

Figure 20: SATA Interface

7.11 PCIe

MSX1400-OCP implements 4 PCIe interfaces:

1. 1X from PCH to 82579
2. 1X from PCH to 82583
3. 8X (gen 2 for Celeron/i3, Gen3 for i5/i7) from CPU to 8X slot
4. 4X gen 2 connection between CPU and SwitchX -2.

The PCIe interface is shown in ***Figure 21***.

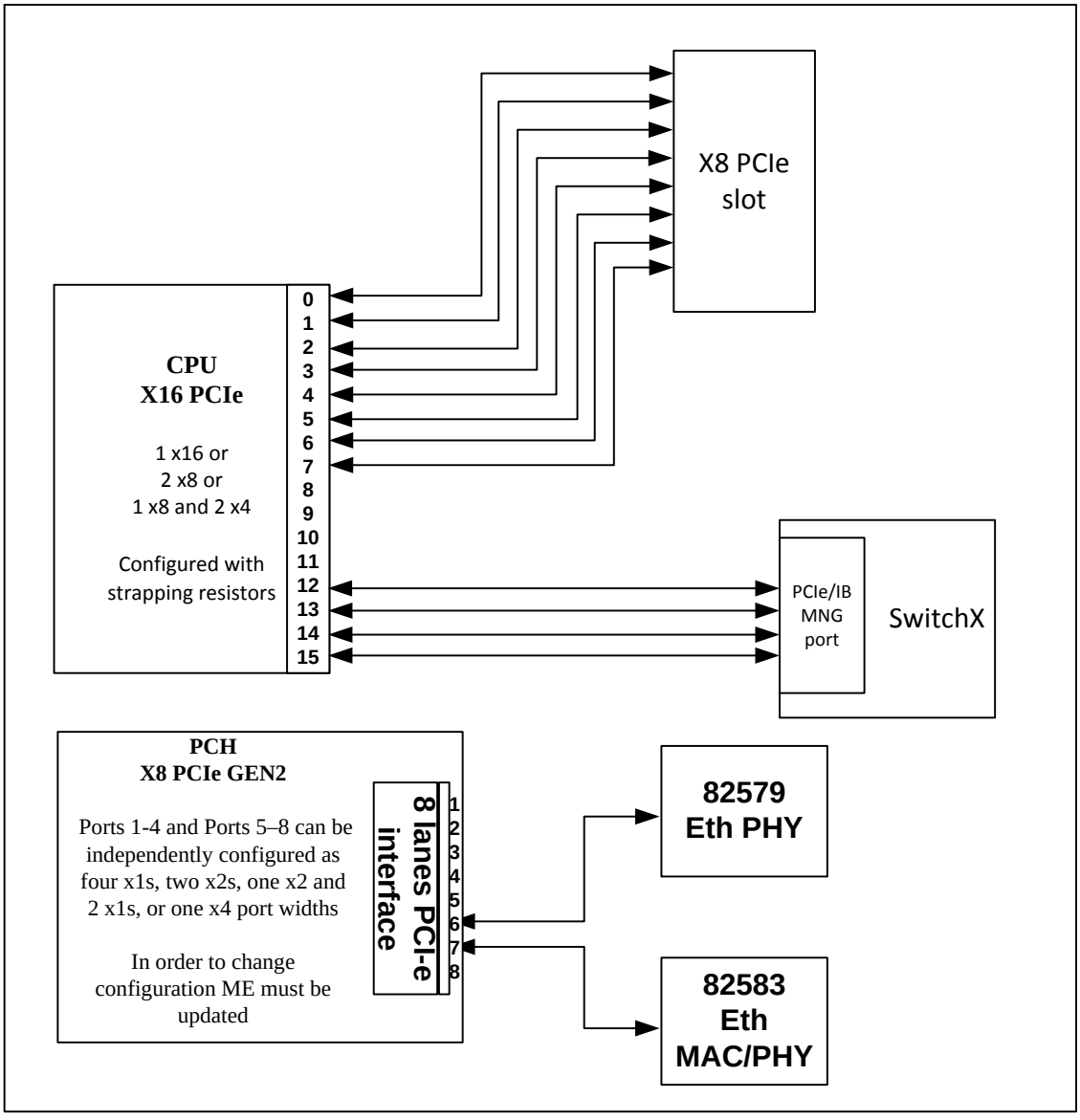

Figure 21: PCIe Interface

7.12 FRU Control

7.12.1 Fan Control

The MGMT CPLD includes a fan controller which is controlled by the SwitchX-2 FW. The fans speed is controlled by 8 PWM signals from the MGMT CPLD to the fans and they are monitored by 8 Tacho signals from the fans towards the CPLD.

PWM:

- A single PWM output signal from SwitchX-2 is connected to the MGMT CPLD. This signal is reflected to all 8 fans as default.
- 8 PWM registers (register per fan) are available via the FW I2C (part of the FW register map). Writing into one of these registers will override the PWM signal into the specific mated fan

Tacho:

- 8 Tacho RO registers will be available via the FW I2C (part of the FW register map).
- FW will be interrupted in case PWM ≠ Tacho.

Fan present signal can be monitored by SW and FW via the CPLD.

Inside the FRU, I2C is connected only to one EEPROM. FW and SW can accesses the fans I2C buses.

7.12.2 Power Supply Control

The PS is controlled via PMbus and a few signals. SW and FW can access the PMbus.

PS fans can be controlled via the PMbus. By default, PS fans are controlled automatically by the PS. PS fans speed can only be increased through FW/SW, but can never be decreased.

All other PS control signals can be controlled (for PS inputs) and monitored (for PS outputs) via FW and SW registers maps.

The MSX1400-OCP FRU control is illustrated in ***Figure 22***.

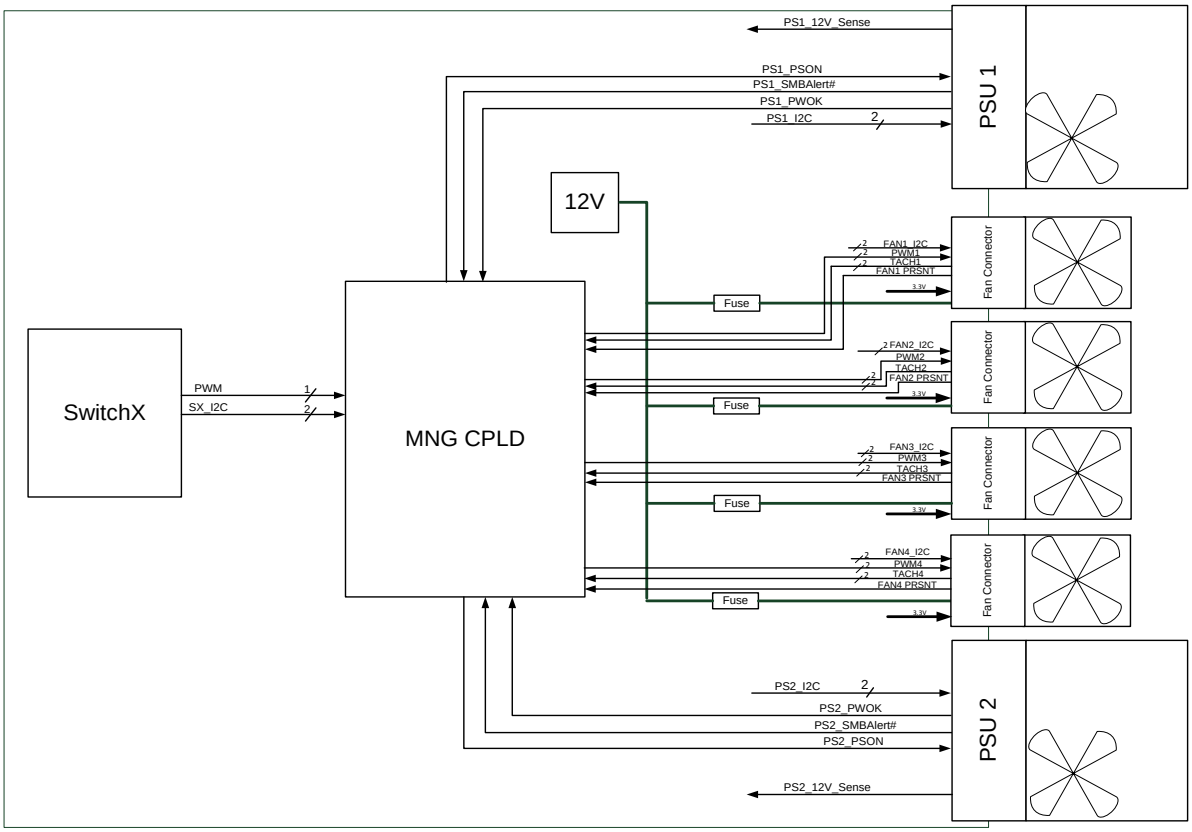

Figure 22: MSX1400-OCP FRU Control

7.13 Reset

Table 5 specifies the reset scenarios and power monitoring in the system:

	Cause	Source	Target	Description
1.	Power monitor circuit indication	CPLD	Entire system	The power monitor circuit verifies that the local voltages are in the range of ±10% of the nominal value.
2.	External push button Short assertion	Push Button	Entire system	User reset from panel. Assertion of more than ½ sec and less than 12sec.
3.	External push button Long assertion	Push Button	Entire system	User reset from panel. Restores CPU factory defaults. Assertion of more than 12sec.
4.	SW RST	SW	Entire system SW has the ability to reset specific components via CPLD	SW request RST.
4.	FW RST	FW	Entire system SW has the ability to reset specific components CPLD	FW request RST
5.	WD expired	CPLD	Entire system WD is disabled as default.	WD mechanism is implemented in the CPLD device. The CPU periodically writes counter value via LPC to 4 WD registers in the SW board 0xXX CPLD – if the CPLD does not recognize a counter value change, board reset is initiated.
6.	I2C Reset request	CPU\SX	I2C tree	CPU\SX requests the CPLD to reset the internal I2C Switches.

Table 5: MSX1400-OCP Reset Matrix

The MSX1400-OCP reset mechanism is displayed in ***Figure 17.***

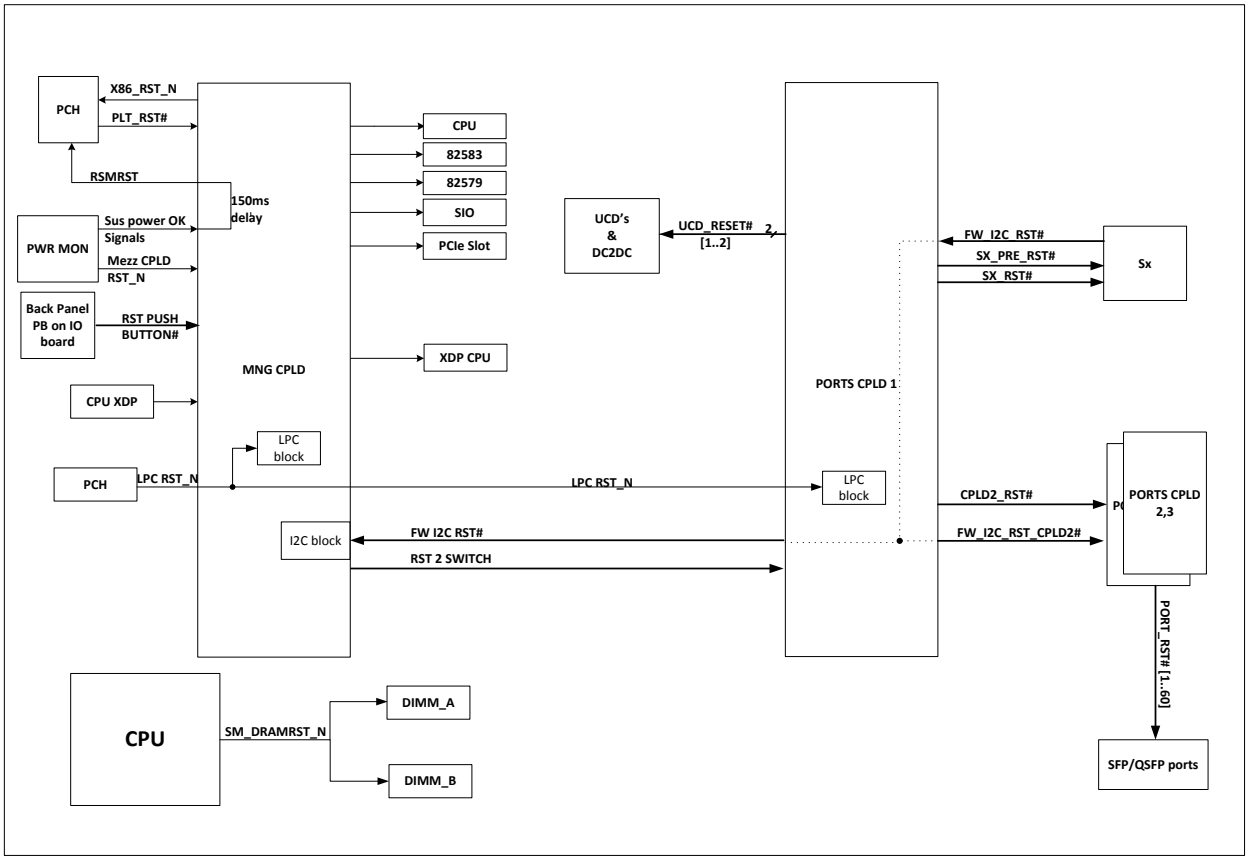

Figure 23: MSX1400-OCP Reset Tree

7.14 Temperature Monitor

The following temperature sensors can be read by SW, FW or both:

- Two external sensors provide temperature sensing:
  - In front of fan FRUs: sense the ambient temperature when fans are pushing air into the system (Air in system)
  - In front of the ports panel: sense the ambient temperature when fans are sucking air from the system (Air out system)
- The Switch-X2 has an internal temperature sensing diode. The temperature sensed by the diode is processed and according to it, two signals may be asserted: Over Thermal Warning and Over Thermal Shutdown. The temperature above / below which these signals are activated /deactivated is controlled by firmware via the INI file, and it must be within the operational temperature range of the device.
- The CPU has an internal sensor that can be monitored only by SW. The CPU can reduce its power (the performance might be reduced as well) in order to prevent from reaching its maximum value.
- The PCH has an internal sensor that can be monitored only by SW.
- Each SODIMM has one module thermal sensor that can be monitored only by SW.

7.15 Clock Distribution

7.15.1 Switch Clock Distribution

Figure 24 specifies the clock distribution in the switch board.

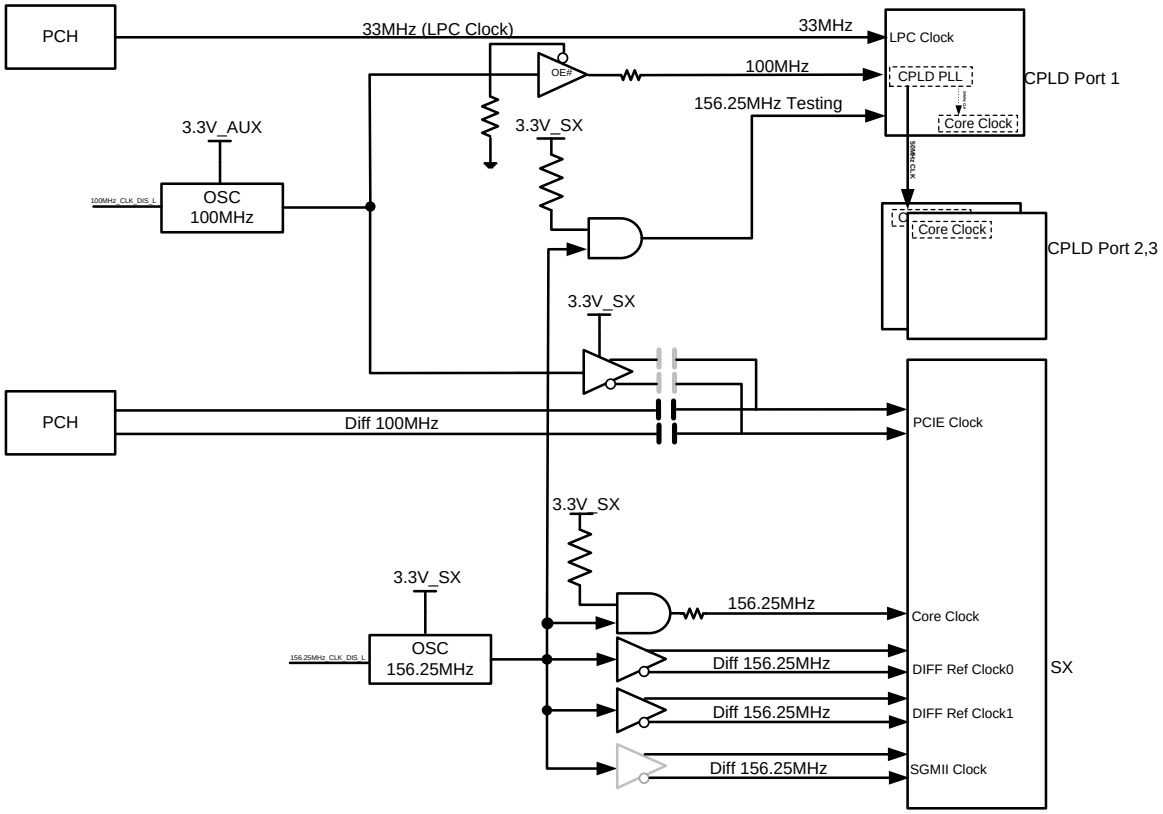

Figure 24: Switch Clock Distribution

7.15.2 MGMT Clocks

Most of the MGMT clocks are generated from two crystals and distributed by the PCH. In addition, one 25MHz oscillator is buffered and distributed to the ETH PHYs and to the CPLD.

The ConnectX3 and the PCIe slot are connected to GEN3 supported clocks (PCIe clocks, A and B) the rest of the PCIe components are connected to GEN2 clocks. In case a GEN 3 connection with the switch board is required, a GEN 3 clock source on the switch board will be needed. ***Figure 25*** describes the clock distribution for the MGMT.

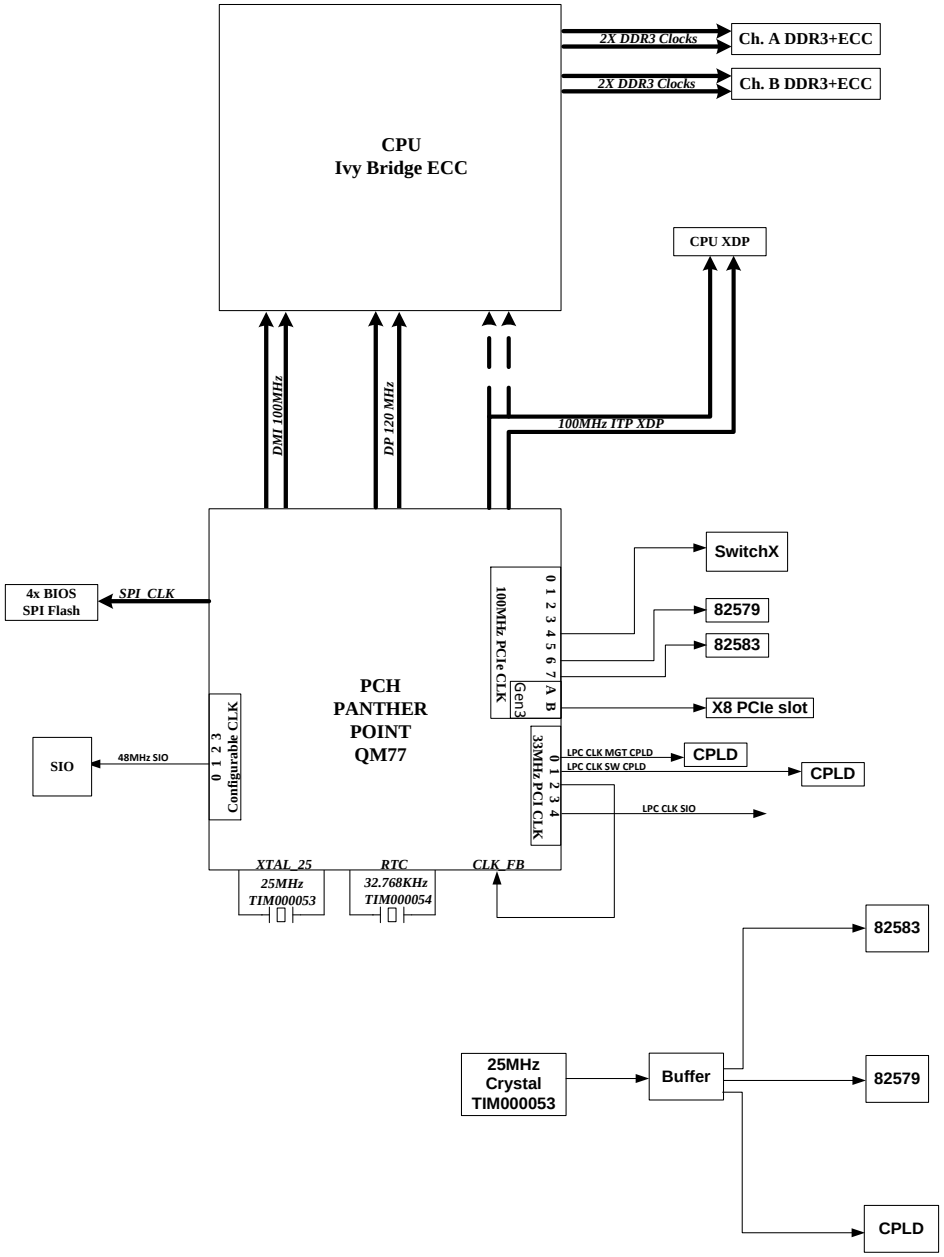

Figure 25: MGMT Clock Distribution

7.16 LEDs

Table 6 describes the indication LEDs on the MSX1400-OCP.

LED	Qty.	Color	Description		Originator	Location
QSFP LEDs	12	Green/ Orange	Ethernet: Off – Link down Solid Green – Link up ,no traffic Blinking Green – Traffic (Received packet) Blinking Orange – Physical errors		Switch-X2	Above QSFP Ports
SFP	12	Green/ Orange	Ethernet: Off – Link down Solid Green – Link up ,no traffic Blinking Green – Traffic (Received packet) Blinking Orange – Physical errors		Switch-X2	Above SFP Ports
Status LED	1	Red/ Green	Off – No power Solid Red – Fault Solid Green – Normal operation Blinking Green – Boot		CPU	On Ports Side and on FRU side
General Fans LED	1	Red/ Green	Off – No power Green – All fans are operating Red – Fan failure		CPLD	On Ports Side
Fans 1-4 LEDs	4	Red/ Green	Off – No power Green – Fan# is operating Red – Fan failure		CPLD	FRU side
UID LED	1	Blue	Static – The operator has activated this LED to identify this module. Blinking – The Operator is instructing to replace this module		SwitchX-2	Ports Side
Bad Port indication	1	Green / Yellow	Blinking yellow – Bad port indication		Switch-X2	Ports Side
PSU LED	1	Green/ Red	Green – Both PSU OK Red –PSU is Faulty		CPLD	Ports Side
PSU	1 per	Green /	Output ON and OK	GREEN	PS	PS FRU

LED	Qty.	Color	Description		Originator	Location
LED	PS FRU	Amber	No AC power to all power supplies	OFF		
			AC present / Only 12VSB on (PS off) or PS in Smart on state	1Hz Blink GREEN		
			AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	AMBER		
			Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Amber		
			Power supply critical event causing a shutdown; failure, OCP, OVP, Fan Fail	AMBER		
			Power Supply FW updating	2Hz Blink GRENN		

Table 6: MSX1400-OCP LEDs

7.17 Power

7.17.1 Power Consumption

7.17.1.1 Celeron Based CPU, 48xDAC+12xSR4

	Voltage	Current	Power
Fans (normal speed)	12V	3.2	38.4
CPU + periphery	12V	4.3	51.7
Switch + periphery	12V	6.4	76.6
SFP – DAC	12V	0	0
QSFP – SR4	12V	2.2	26.6
Total 12V power	12V	16.1	193.3
Auxilary power	12VSB	1.3	15.6

Table 7: Celeron, 48xDAC, 12xSR4

7.17.1.2 Celeron based CPU, 48xSR+12xLR4

	Voltage	Current	Power
Fans (high speed)	12V	4.8	57.6
CPU + periphery	12V	4.3	51.7
Switch + periphery	12V	6.4	76.6
SFP – SR	12V	4.4	53.3
QSFP – LR4	12V	3.9	46.6
Total 12V power	12V	22.2	285.8
Auxilary power	12VSB	1.3	15.6

Table 8: Celeron,48xSR, 12xLR4

7.17.2 Power Distribution – Switch

The power rails of SwitchX-2 and its periphery are driven from TI UCD9224 with UCD74120 power stages.

Figure 26 specifies the power distribution of the Switch power:

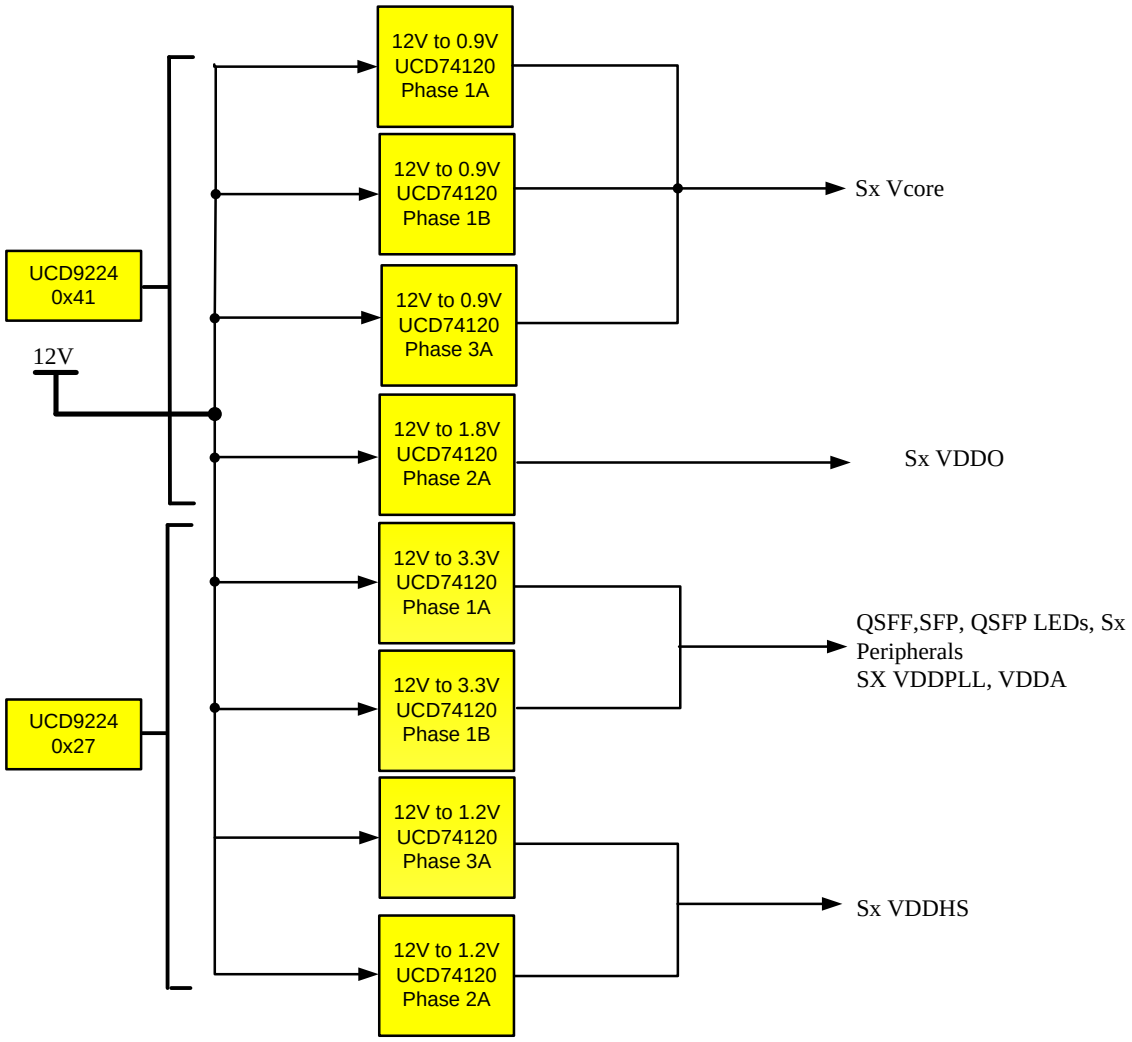

Figure 26: Power Distribution - Switch

7.17.3 Power Monitoring – Switch

Power monitoring on SwitchX-2 power rails is done in Port CPLD 1.

Figure 27 specifies Switch power monitoring.

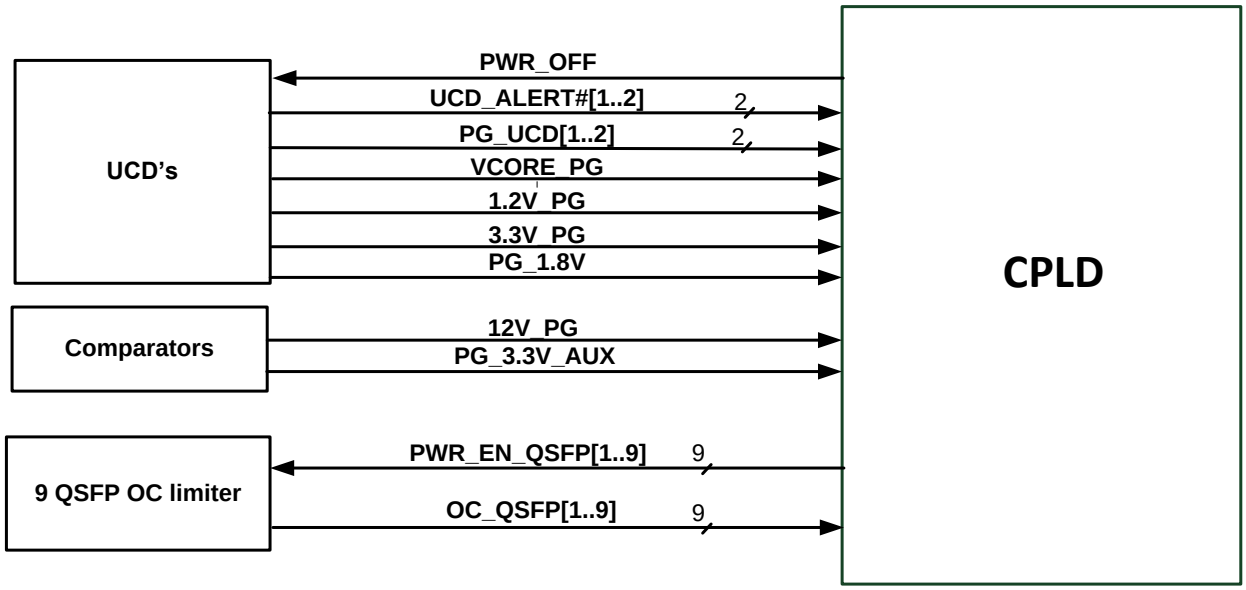

Figure 27: Power Monitoring - Switch

7.17.4 Power Distribution and Monitoring – Management

Figure 28 specifies power distribution on CPU, chipset, and fans.

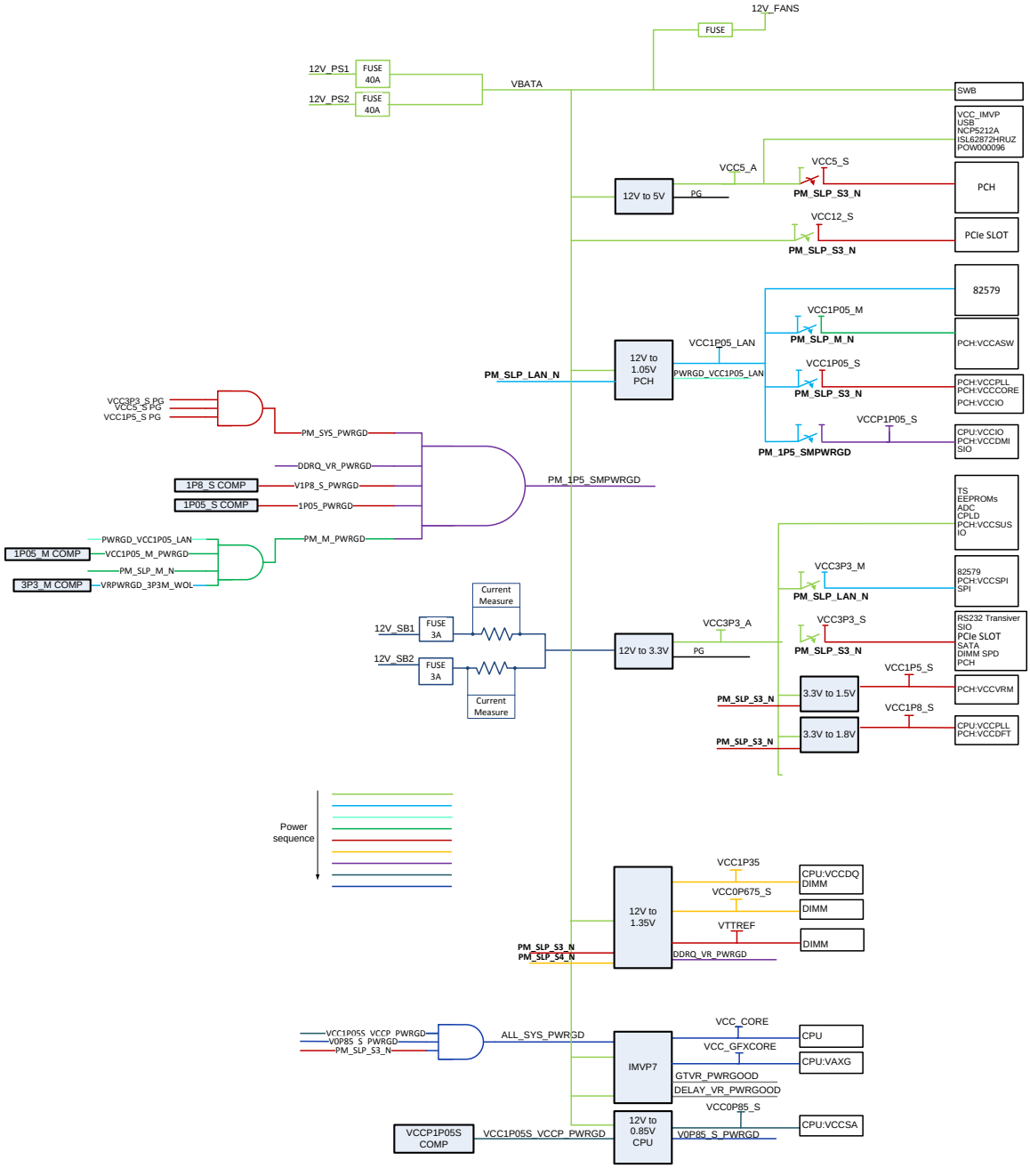

Figure 28: Management Power Distribution and Monitoring

7.17.5 System Voltages and Currents Sensing

System voltages and currents are accessible by SW/FW via an 8 channel I2C analog to digital converter. Voltage/current inputs to the A2D channels 2-7 are MUXed by 1:2 MUX. Therefore, two values can be read per channel. The MUX select signal is derived by the CPLD and can be controlled by SW and FW. The main 12V voltages and currents can be read directly from the AC/DC PS.

Table 9 describes the voltage rail at each channel and the expected reading.

Acceptable range for each rail is +-10% from nominal value.

A/D Channel	MUX Select Signal	Monitored Voltage/Current		"B" Parameter
0	NA	DDR3 VTT 0.675V (VCC0P675_S)		0.008
1	NA VCC0P85_S (See Note 1)	***Rail level***	***[VID0,VID1]***	0.008
		0.675	[1,1]	
		0.725	[1,0]	
		0.8	[0,1]	
		0.9	[0,0]	
2	0	12V_AUX1 (12VSB1 current)		0.0586
	1	12V_AUX2 (12VSB2 current)		0.0586
3	0	3.3V (VCC3P3_A)		0.016
	1	5V (VCC5_A)		0.024
4	0	CPU 1.8V (VCC1P8_S)		0.008
	1			0.008
5	0	CPU/PCH 1.05V (VCC1P05_LAN)		0.008
	1	CPU 1.5V (VCC1P5_S)		0.008
6	0	CPU 1.05V (VCCP1P05_S)		0.008
				0.008
7	0	DDR3 1.35V (VCC1P35)		0.008
				0.008

Table 9: A/D Channels

Notes:

Parameter B is used to calculate the real voltage/current from I2C reading, using the following formula: V=B*R, where V is the real voltage and R is the I2C reading. This voltage is divided by voltage divider before it is sampled; therefore, its parameter B contains the divider.

8 Compliancy

- Shock & Vibration: ETSI EN 300 019-2-2: 1999-09
- Humidity operating: 5% - 95% non-condensing
- Safety:

    - US/Canada: cTUVus
    - EU: IEC60950
    - International: CB
- EMC (Emissions):
    - USA: FCC, Class A
    - Canada: ICES, Class A
    - EU: EN55022, Class A
    - EU: EN55024, Class A
    - EU: EN61000-3-2, Class A
    - EU: EN61000-3-3, Class A
    - Japan: VCCI, Class A
- Environmental
    - EU: IEC 60068-2-64: Random Vibration
    - EU: IEC 60068-2-29: Shocks Type I /II
    - EU: IEC 60068-2-32: Fall Test
- Acoustics:
    - ISO 7779
    - ETS 300 753