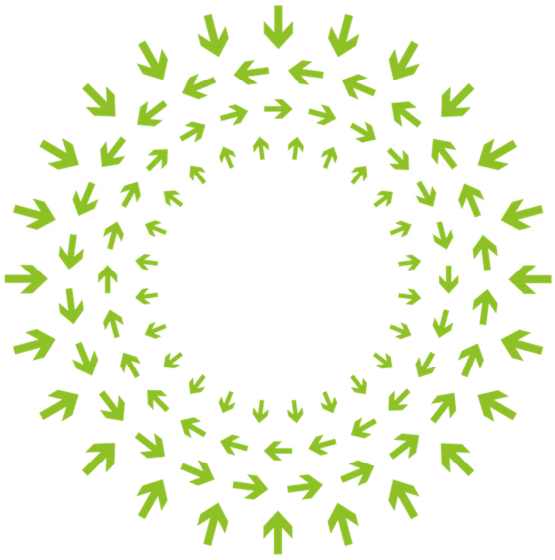

OPEN
Compute Project

Alpha Networks Inc

SNX-60x0-486F

48-port 10G SFP+ & 6-port 40G QSFP Switch
(ToR/Aggregation Switch)

Author: Damon Lee, Chloe Lin

Revision History

Version	Revised Date	Author	Content Revised
0.4	20/09/14	Damon Lee	
0.5	24/09/14	Chloe Lin	Add Fan module connector part number
0.6	09/10/14	Damon Lee	Add PSU and CPU module connectors part number and pin-out

Scope

This documents defines the technical specification for SNX-60x0-486F used in the Open Compute Project as 10G Top of the Rack (ToR) or as an aggregation switch

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Overview

The SNX-60x0-486F Series Data Center, Top-of-Rack (ToR)/aggregation switches, with a total combined bandwidth of 720 Gbps, feature 48 ports of 10 Gbps and 6 ports of 40 Gbps Ethernet wire-speeds. The Layer 3 capable, bare metal system also provides an RJ-45 console port and an Out-Of-Band (OOB) management port. It also provides a micro USB interface in the front panel for the administrators to upgrade code by using an extended cable. The SNX-60x0-486F switch is a PHY-less design with SFP+ and QSFP+ connections directly attached to the SERDES interface of Broadcom BCM56854.

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Manufacturer	Description
Broadcom	BCM56854
Intel	x86 CPU C2538-2.4GHz
Freescale	P2020NSN2MHC
Marvell	88E1112
Transcend	SODIMM TS512MSK72V3N
Transcend	SD Card TS8GUSDC10M
Macronix	Flash MX29LV640EBTI-70G
Renesas	EEPROM R1EX24002ASAS0I
Atmel	AT24C128C-SSHM-T
Lattice	LCMXO256C-3TN100C

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1 Feature Highlights

The SNX-60x0-486F Series Data Center, Top-of-Rack (ToR)/aggregation switches, with a total combined bandwidth of 720 Gbps, feature 48 ports of 10 Gbps and 6 ports of 40 Gbps Ethernet wire-speeds. The Layer 3 capable, bare metal system also provides an RJ-45 console port and an Out-Of-Band (OOB) management port. Administrators can selectively access the Command Line Interface (CLI) through the RJ-45 console port. It also provides a micro USB interface in the front panel for the administrators to upgrade code by using an extended cable.

- Modular CPU board with large flash and memory
- Temperature warning
- Software-readable thermal monitor
- Real time clock (RTC) support
- Two Hot-swappable redundant power supply
- Four redundant (3+1) fan modules
- One 10/100/1000 Mbps management port
- One RJ45 type console port in the front panel
- One Micro USB port in the front panel for hosting an external USB flash via micro USB to USB cable
- One Reset button in the front panel

2 Physical Overview

2.1 Mechanical Dimension

Dimension	
Height x Width x Depth	44mm(H)440mm(W) x 487.4 mm(D)

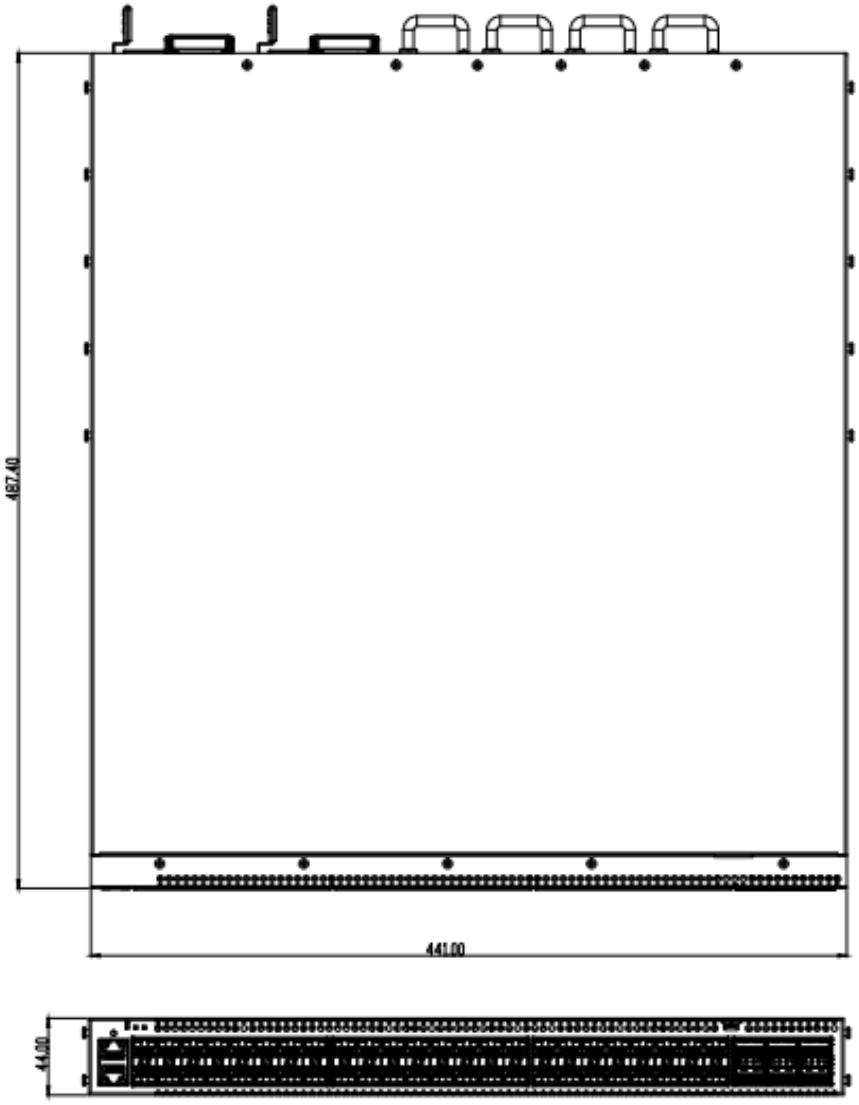
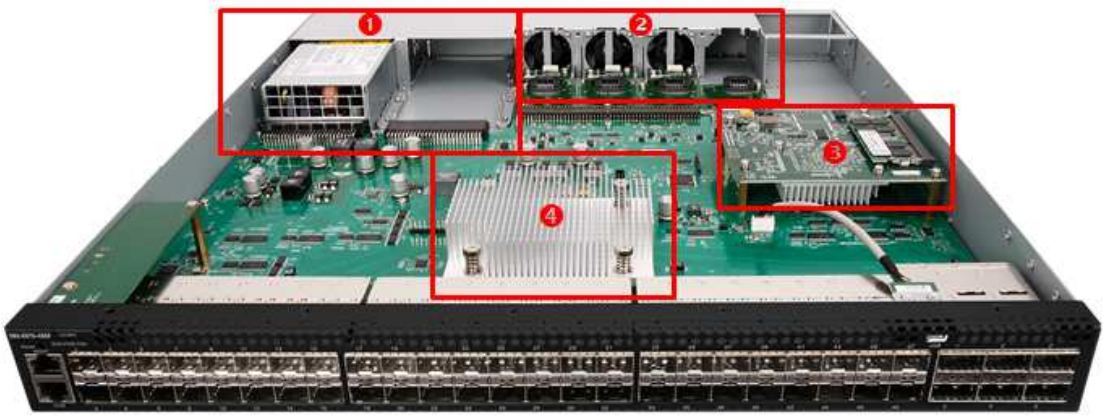


Figure 1: SNX-60x0-486F Chassis dimension

2.2 Top View



❶: Hot swappable power supply
❷: Hot swappable fan modules
❸: CPU module
❹: Switch MAC – Trident 2

Figure 2: SNX-60x0-486F top view

2.3 Front View

❶: Out of band management port
❷: Console Port
❸: 48* 10G SFP+ ports
❹: Mini USB port for storage
❺: 6* 40G QSFP ports

Figure 3: SNX-60x0-486F front view

2.4 Rear View

Figure 4: SNX-60x0-486F rear view

3 LED Definition

The following table defines the per device LEDs' behaviors:

Items	LED Indication	Color	Behavior	Description
1	Locator	Blue	Blinking	Locator function is enable
			Light off	Locator function is disable
	STAT	Green	Solid Light	POST Passed, normal operation
			Blinking	POST in progress
			Light off	Power off
		Amber	Blinking	POST failed or overheat or power supply failed or Fan module fail or over temperature
	PWR	Green	Solid Light	Power On
			Light off	Power Off and no power attached
		Amber	Blinking	Power supply failures, over voltage, over current, over temperature

	FAN	Green	Solid Light	The fan modules are operating normally
		Amber	Blinking	There is any fan module failed
2	MGMT	Green(R)	Solid Light	Connection is active
			Blinking	Packet transmitting or receiving
			Light off	No connection detected. Port is disabled
3	CON	Green(R)	Solid Light	Console is on
			Light off	No link up or port disable

Table 1: LED behavior for system

The following defines the 10G SFP+ Ethernet port LEDs' behaviors:

Location	LED Indication	Color	Behavior	Description
LED Port 1~48 (10G bps)	Link/Act/Speed	Green	Solid Light	A transceiver module or cable has been correctly installed. The port has a link and is operating at 10Gbps
			Blinking	The port is sending or receiving data at 10Gbps
		Off	Light off	Link down or no link

Table 2: LED behavior for Port 1~48 10G Ethernet Port

The following table defines the 40G QSFP+ Ethernet port LEDs' behaviors:

Location	LED Indication	Color	Behavior	Description
LED Port 1~6 (40Gbps)	Link/Act/Speed	Green	Solid	A transceiver module or cable has been correctly installed. The port has a link and is operating at 40Gbps
			Blinking	The port is sending or receiving data at 40Gbps
		Amber	Solid	A transceiver module or cable has been correctly installed. The port has a link and is operating at 10Gbps

			Blinking	Packet is transmitting or receiving at 10Gbps
		Off	Light off	Link down or no link

Table 3: LED behavior for Port 49~54 40G Ethernet Port

Each power supply module has a bi-color LED, which behavior is descript in the following:

LED Color	Behavior	Description
Green	Solid Light	Output ON and OK
	Blinking	AC present / AC Line 12VSB Holdup
	Light off	No AC power to all power supplies
Amber	Solid Light	Power supply critical event causing a shutdown; failure, Fan Fail
	Blinking	Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.

Table 4: Power supply LED definition

4 Field Replaceable Components

4.1 Power Supply Modules

Then SNX-60x0-486F supports two hot swappable power supplies plugged in at the same time for redundancy. The details of the power supplies are as following:

Power Supply	
Number of power supply	2
Power supply types	AC version (forward and reversed airflow) ● DPS-460KB C ● DPS-460KB B DC version (forward and reversed airflow) ● DPS-800KB C ● DPS-800KB B
AC PSUs ● **Input voltage** ● **Frequency** ● **Efficiency**	 ● 100 to 240 VAC ● 50 to 60 Hz ● 89 to 91% at 220V

DC PSUs • **Input voltage range** • **Efficiency**	• 40.5V/23.8A 48V/19.0A -60V/15.6 • 85 to 88%

Table 5: Power supplies details

Power Supply connector: FCI 10035388-102LF

Pin #	Descriptin	Pin #	Descriptin3
A1~9	GND	**B1~9**	GND
A10~18	+12V	**B10~18**	+12V
A19	PMBus SDA	**B19**	A0 (SMBus Address)
A20	PMBus SCL	**B20**	N/A
A21	PSON	**B21**	12VSB
A22	SMBAlert#	**B22**	Smart_on
A23	Return Sense	**B23**	12VLS
A24	+12V Remote Sense	**B24**	No Connect
A25	PWOK	**B25**	N/A

Table 6: Power supply connector pin out

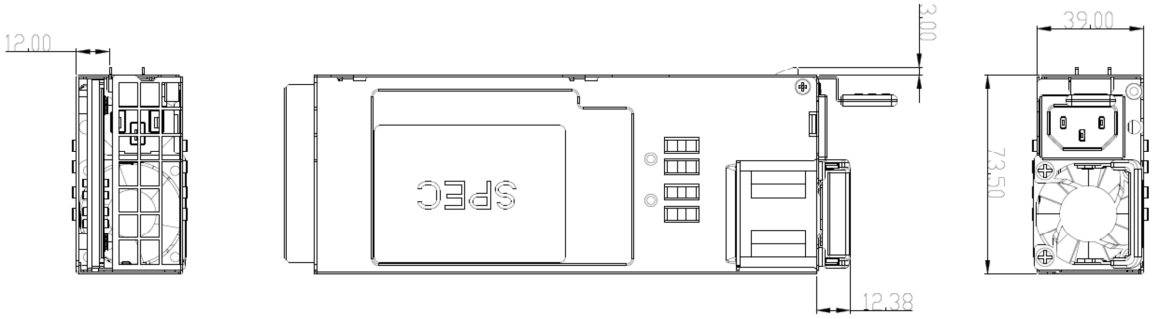


Figure 5: Power Supply Mechanical specification

LED definition on power supply

Power Supply Condition	LED Status
Output on and OK	Green
No AC power to all power supplies	Off
AC present/ Only 12VSB on (PS off) or PS in Smart on state	1Hz on Blink Green
AC power cord unplugged or AC power lost; with a second power supply in parallel still with AC power input	Amber
Power supply warning events where the power supply continue to operate at high temperature, high current, high	1Hz on Blink Amber

power or slow fan	
Power supply critical event causing shutdown, OVP, OCP, fan fail	Amber
Power supply FW updating	2Hz on Blink Green

Table 7: LED definition on power supply

FRU

FRU data format compliant with IPMI ver 1.0 (per rev 1.1 from Sept. 25, 1999) specification. The FRU device will implement the same protocols as the commonly used AT24C02 device, including the Byte Read, Sequential Read, Byte Write and Page Read protocols.

The EEPROM content is as following

Area Type	Description
Common Header	As defined by the FRU document
Internal Use Area	Not required, do not reserve
Chassis Info Area	Not applicable, do not reserve
Board Info Area	Not applicable, do not reserve
Product Info Area	As defined by the IPMI FRU document. Product information is defined as following
Field name	Field Description
Manufacturer Name	{Formal name of manufacturer}
Product Name	{Manufacturer's model number}
Product part/model number	Customer part number
Product Version	Customer current revision
Product Serial Number	{Defined at time of manufacture}
Asset Tag	{Not used, code is zero length byte}
FRU File ID	{Not required}
PAD Bytes	{Added as necessary to allow for 8-bype offset to next area}
Mulit-Record Area	As defined by the IPMI FRU documentation. The following information shall be used by this power supply: Power Supply Information (Record type 0x00) DC Output (Record Type 0x01) No other record types are required for power supply Multi-Record information shall be defined as following

Field Name (PS Info)	Field Information Definition
Overall Capacity (watts)	460
Peak VA	1070
Inrush current (A)	55
Inrush interval (msec)	5
Low end input voltage range 1	90
High end input voltage range 1	140
Low end input voltage range 2	180
High end input voltage range 2	264
A/C dropout total (msec)	20
Binary flags	Set for: Hot Swap support, Auto switch and PFC
Peak Wattage	Set for 575 Watts
Combined wattage	None
Predictive fail tach support	Supported
Field Name (Output)	Field Description : Two output are to be defined from #1 to #2, as follows: +12V and +12VSB
Output Information	Set for: Standby on +12VSB, no 12VSB on all others
All other output fields	Format per IPMI specification , using parameters in this specification

Table 8: Power Supply EEPROM FRU data format

4.2 Fan Modules

The SNX-60x0-486F supports up to 5 fan modules. For front to rear and rear to front air flow, different types of fan modules are required.

Air Flow Direction	Part Number
Front to Rear	AVC DFTA0456B2UP057
Rear to Front	AVC DFTA0456B2UP058

Table 9: Fan Modules part number

Fan module connector: LCU SM401V-20P

#	NAME	Description	#	NAME	Description
1	FAN_CON_TACH_0	FAN tachometer 0	**11**	FAN_DIR	FAN Direction
2	GND	GND	**12**	GND	GND
3	FAN_12VIN	12V	**13**	FAN_12VIN	12V
4	FAN_CON_PWM_0	PWM control for FAN0	**14**	EE_GND	EEPROM GND
5			**15**	EE_SDA	EEPROM SDA
6	EE_SCL	EEPROM SCL	**16**	EE_VDD	EEPROM VDD
7	EE_A0	EEPROM ADDR_0	**17**	FAN_CON_PWM_1	PWM control for FAN1
8	FAN_12VIN	12V	**18**	FAN_12VIN	12V
9	GND	GND	**19**	GND	GND
10	FAN_PRESENT#	Exist FAN module	**20**	FAN_CON_TACH_1	FAN tachometer 0

Table 10: Fan Modules connector pin out

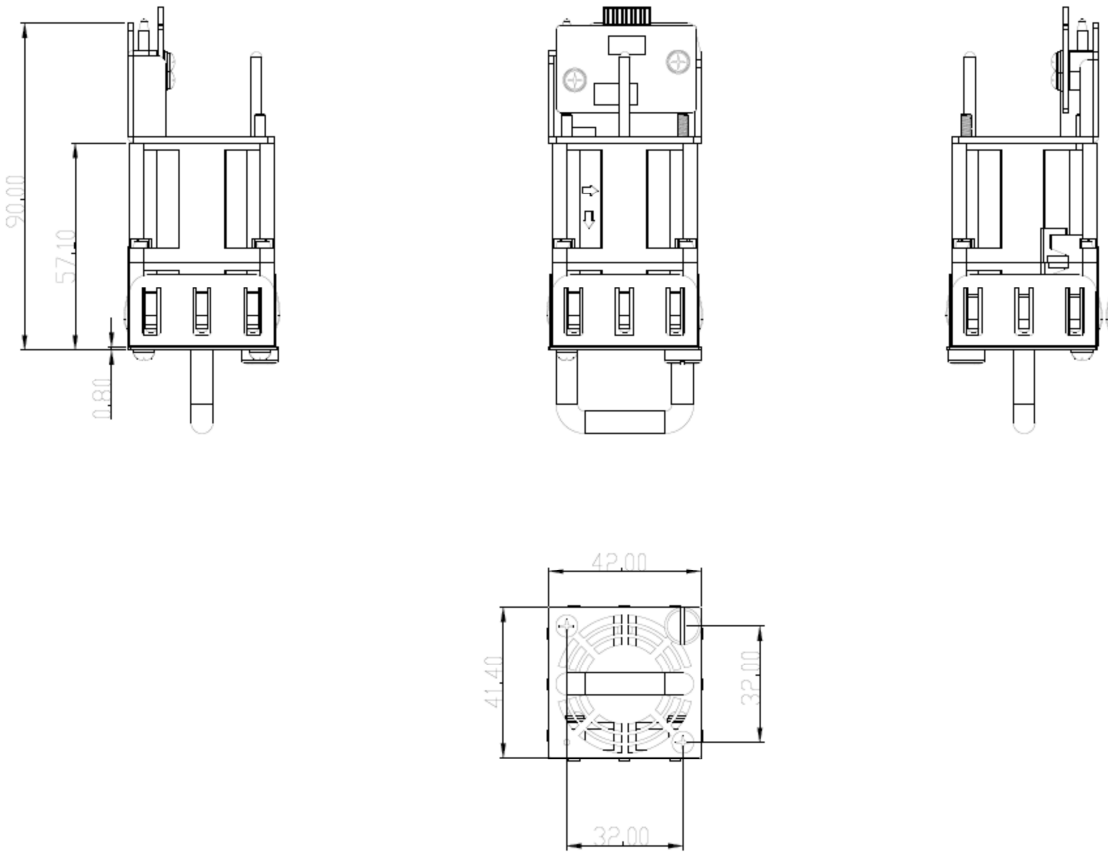


Figure 6: Fan module mechanical specification

5 System Overview

The SNX-60x0-486F comprised of the following PCB

PCB Function	PCB Layer	Dimension (mmxmm)
Main board	12	431*315.5
FAN module	2	38.5*29
FAN Adapter	4	185*60.4
LED board	2	35*121.1
USB board	2	20*37
Freescale CPU board	6	120*109*1.6
Intel CPU board	12	255*165.1

Table 11: PCBs for SNX-60x0-486F

5.1 Main PCB

The main PCB is a 12 layer PCB where the switch MAC resides. It also supports the following functions:

- Networking I/O ports
- Management ports
- LED
- Connectivity to power supply and fan
- Power conversion circuit
- Etcs

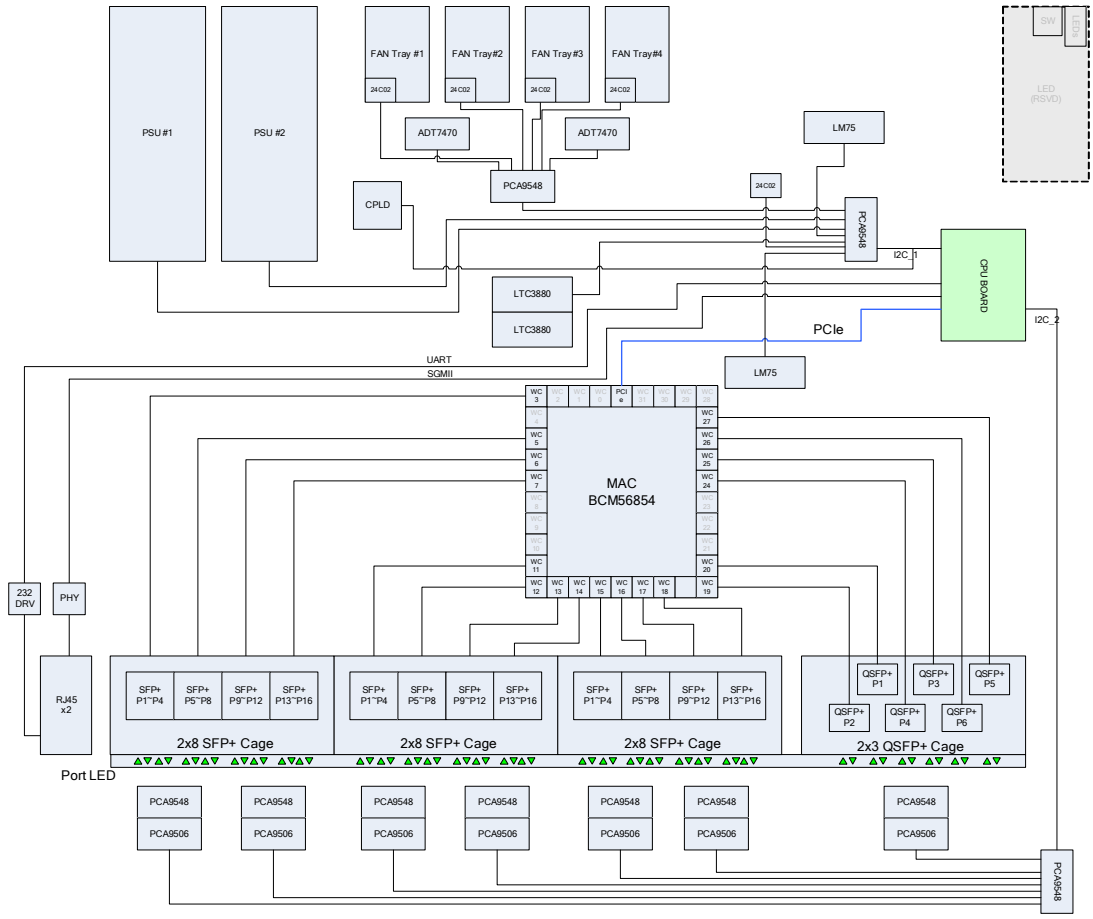


Figure 7: Main board block diagram

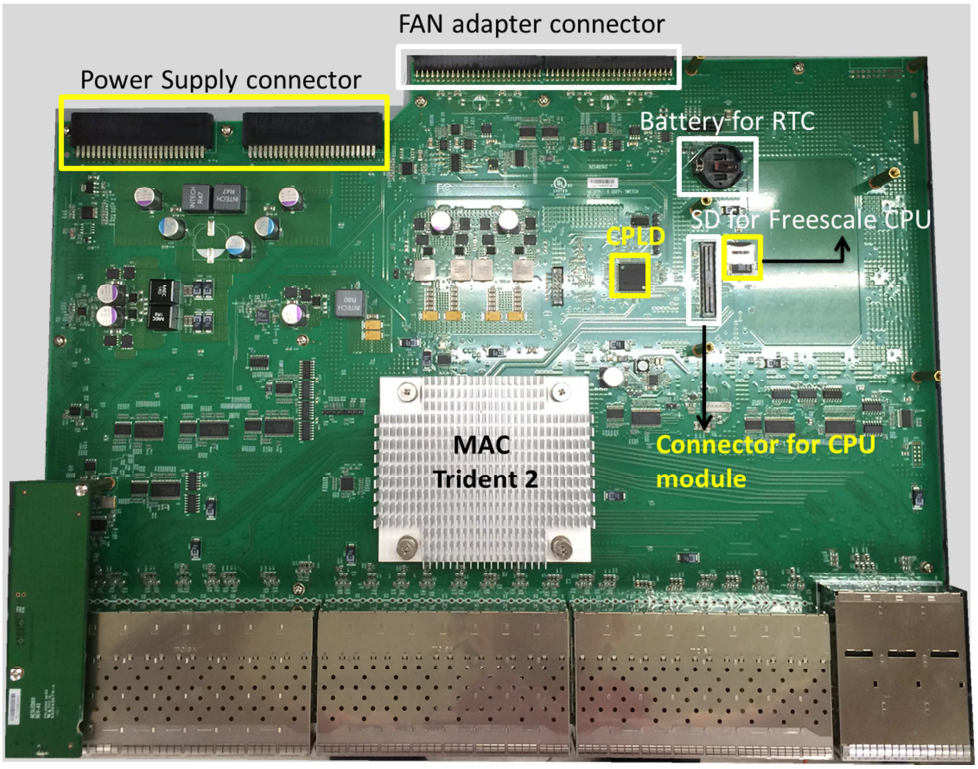


Figure 8: Main PCB top view

5.1 CPU Subsystem

The SNX-60x0-486F offers CPU in modular form to allows the flexibility for different CPU preference. Currently two types of CPU modules are supported, and the detail is provided in the following table and sections.

Items		Detailed Description
Freescale		
Modular CPU board (Option 1)	CPU	Freescale P2020,1.2GHz with PCIe connector to main board
	RAM	DDR3 4GB for Freescale CPU
	Flash	Micro-SD Card 8GB for Freescale CPU
	Boot Flash	8MB for Freescale CPU
Intel		
Modular CPU board (Option 2)	CPU	Intel Rangeley C2558 4 Cores/2.4G
	RAM	DDR3 4GB for Intel Rangeley CPU
	Flash	SSD 8GB for Intel Rangeley CPU
	Boot Flash	8MB for Intel Rangeley CPU

Table 12: CPU subsystem key Components

5.1.1 Freescale CPU (P2020)

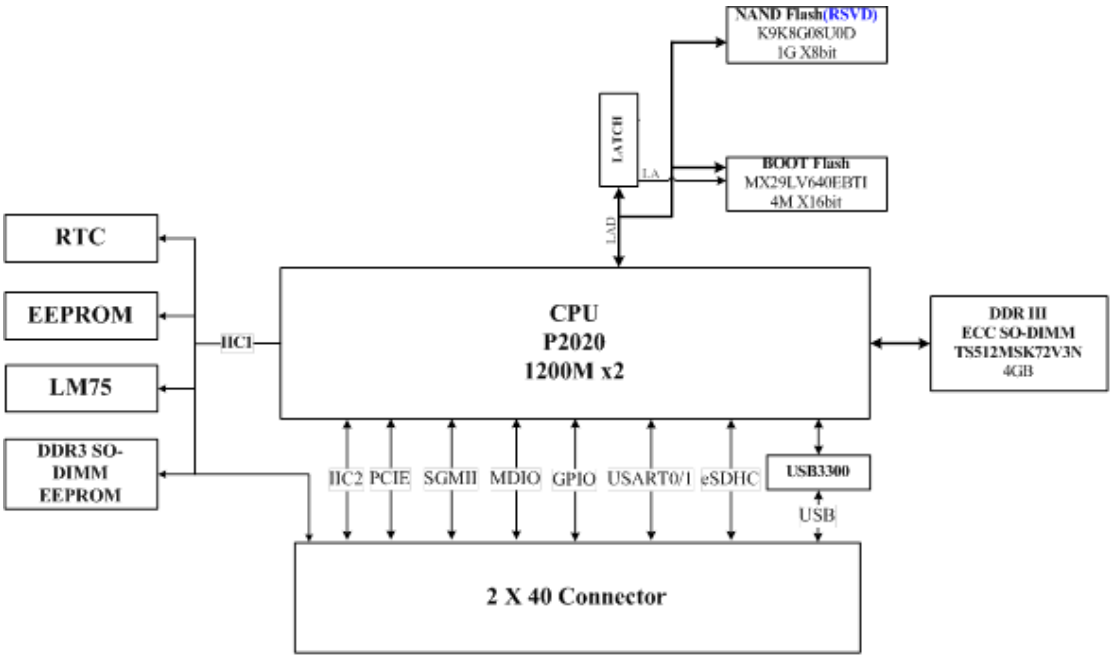


Figure 9: Freescale CPU board block diagram

Freescale CPU module connector: SAMTEC BSE-040-01-F-D-A-TR

For 80 PIN connector					
#		Description	#		**Description**
1	3.3V	3.3V	**2**	3.3V	3.3V
3	SGMII_TXDP	SGMII transmit serial data. Differential interface positive leg.	**4**	GND	GND
5	SGMII_TXDN	SGMII transmit serial data. Differential interface negative leg.	**6**	GND	GND
7	GND	GND	**8**	PCIE0_TXP	PCI Express transmit serial data. Differential interface positive leg of lane 0
9	GND	GND	**10**	PCIE0_TXN	PCI Express transmit serial data. Differential interface negative leg of lane 0
11	SGMII_RXDP	SGMII receive serial data. Differential interface positive leg.	**12**	GND	GND
13	SGMII_RXDN	SGMII receive serial data. Differential interface negative leg.	**14**	GND	GND
15	GND	GND	**16**	PCIE0_RXP	PCI Express receive serial data. Differential interface positive leg of lane 0
17	GND	GND	**18**	PCIE0_RXN	PCI Express receive serial data. Differential interface negative leg of lane 0

19	USB_DP	USB_DP	**20**	GND	GND
21	USB_DN	USB_DN	**22**	GND	GND
23	GND	GND	**24**	PCIe1_REFCLKp	Differential interface positive Reference Clock of PCIe 1
25	GND	GND	**26**	PCIe1_REFCLKn	Differential interface negative Reference Clock of PCIe 1
27	PCIE1_TXP	PCI Express transmit serial data. Differential interface positive leg of lane 1	**28**	GND	GND
29	PCIE1_TXN	PCI Express transmit serial data. Differential interface negative leg of lane 1	**30**	GND	GND
31	GND	GND	**32**	PCIe0_REFCLKp	Differential interface positive Reference Clock of PCIe 0
33	GND	GND	**34**	PCIe0_REFCLKn	Differential interface negative Reference Clock of PCIe 0
35	PCIE1_RXP	PCI Express receive serial data. Differential interface positive leg of lane 1	**36**	GND	GND
37	PCIE1_RXN	PCI Express receive serial data. Differential interface negative leg of lane 1	**38**	GND	GND
39	GND	GND	**40**	RESET for CPLD	RESET for CPLD
41	3.3V	3.3V	**42**	SD_CMD	Command for micro SD Card
43	SD_CLK	micro SD Card Clock	**44**	SD_WP	Write Protect for micro SD Card
45	3.3V	3.3V	**46**	RESET_ALL#	Globe reset from CPU board
47	CPLD_INT#	Interrupt for CPLD	**48**	RPS_INT#	Interrupt for RPS

49	TS_INT#	Thermal Sensor IRQ mask	**50**	NC	NC
51	MGMT_INT#	Interrupt for management PHY	**52**	QSFP_INT#	Reset all I2C device on I2C Bus 2
53	3.3V	3.3V	**54**	3.3V	3.3V
55	SCL1	Serial clock line of I2C-bus 1	**56**	SDA1	Serial data line of I2C-bus 1
57	GND	GND	**58**	GND	GND
59	SCL2	Serial clock line of I2C-bus 2	**60**	SDA2	Serial data line of I2C-bus 2
61	3.3V	3.3V	**62**	3.3V	3.3V
63	UART0_TX	UART0_TX	**64**	UART0_RX	UART0_RX
65	GND	GND	**66**	GND	GND
67	SD_DATA0	Data Line [Bit0] of micro SD Card	**68**	SD_DATA2	Data Line [Bit2] of micro SD Card
69	SD_DATA1	Data Line [Bit1] of micro SD Card	**70**	SD_DATA3	Data Line [Bit3] of micro SD Card
71	3.3V	3.3V	**72**	3.3V	3.3V
73	GND	GND	**74**	GND	GND
75	MDC	Management data clock	**76**	MDIO	Management data
77	Fan_SPD_CTRL	Control Fan Speed	**78**	NC	NC
79	NC	NC	**80**	SDHC_CD_B	Card Detect of micro SD Card

Table 13: Freescale CPU module connector pin out

5.1.1.1 DDR3 SDRAM

The Freescale DDR SDRAM controller supports most JEDEC standard ×8, ×16, ×32, or ×64 DDR2 and DDR3 memories available. Built-in error checking and correction (ECC) ensures very low bit-error rates for reliable high-frequency operation. Dynamic power management and auto-precharge modes simplify memory system design. The DDR memory controller includes these distinctive features:

- Support for DDR2 and DDR3 SDRAM
- 64-/72-bit SDRAM data bus, 32-/40-bit SDRAM for DDR2 and DDR3
- Support for up to 32Gbits of memory

5.1.1.2 PCIe Interface

The P2020 supports three PCI Express interfaces that are compliant with the PCI Express Base Specification Revision 1.0a. The physical layer of the PCI Express

interface operates at a transmission rate of 2.5 Gbaud (data rate of 2.0 Gbps) per lane. The theoretical unidirectional peak bandwidth is 2 Gbps per lane. Receive and transmit ports operate independently, resulting in an aggregate theoretical bandwidth of 4 Gbps per lane.

5.1.2 Intel CPU (C2558)

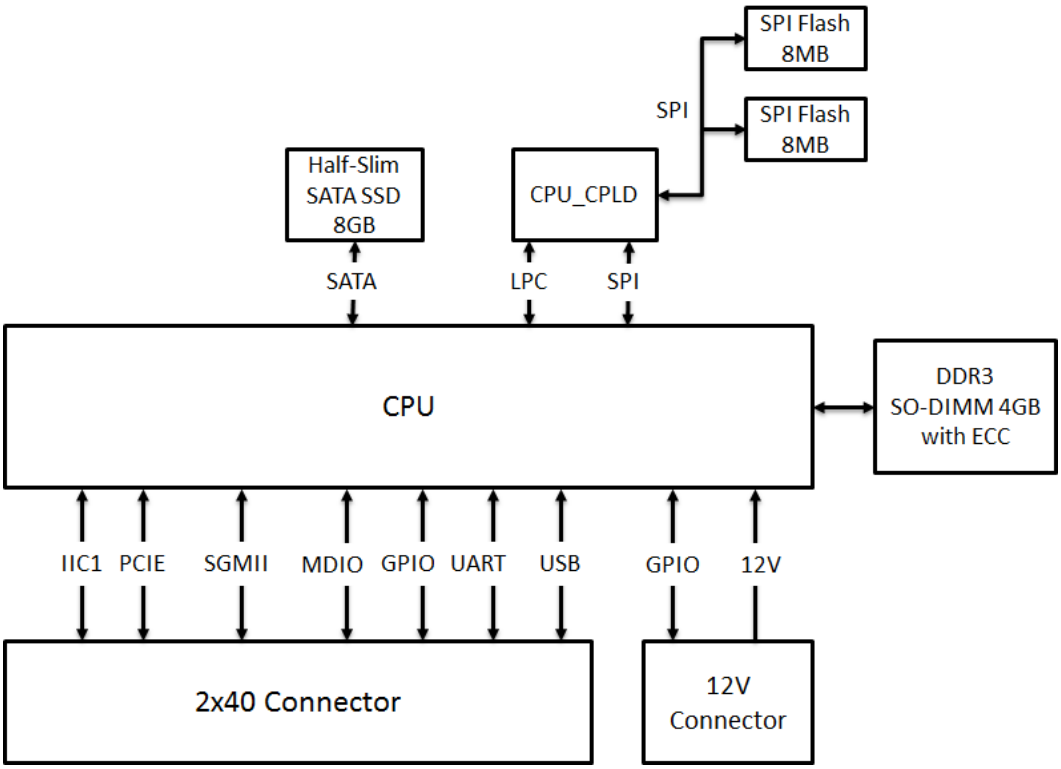


Figure 10: Intel CPU board block diagram

Intel CPU module connector: SAMTEC BSE-040-01-F-D-A-TR

For 80 PIN connector					
#		Description	#		**Description**
1	3.3V	3.3V	**2**	3.3V	3.3V
3	SGMII_TXDP	SGMII transmit serial data. Differential interface positive leg.	**4**	GND	GND
5	SGMII_TXDN	SGMII transmit serial data. Differential interface negative leg.	**6**	GND	GND
7	GND	GND	**8**	PCIE0_TXP	PCI Express

					transmit serial data. Differential interface positive leg of lane 0
9	GND	GND	**10**	PCIE0_TXN	PCI Express transmit serial data. Differential interface negative leg of lane 0
11	SGMII_RXDP	SGMII receive serial data. Differential interface positive leg.	**12**	GND	GND
13	SGMII_RXDN	SGMII receive serial data. Differential interface negative leg.	**14**	GND	GND
15	GND	GND	**16**	PCIE0_RXP	PCI Express receive serial data. Differential interface positive leg of lane 0
17	GND	GND	**18**	PCIE0_RXN	PCI Express receive serial data. Differential interface negative leg of lane 0
19	USB_DP	USB_DP	**20**	GND	GND
21	USB_DN	USB_DN	**22**	GND	GND
23	GND	GND	**24**	PCIe1_REFCLKp	Differential interface positive Reference Clock of PCIe 1
25	GND	GND	**26**	PCIe1_REFCLKn	Differential interface negative Reference Clock of PCIe 1
27	PCIE1_TXP	PCI Express transmit serial data. Differential interface positive leg of lane 1	**28**	GND	GND
29	PCIE1_TXN	PCI Express transmit serial data. Differential	**30**	GND	GND

		interface negative leg of lane 1			
31	GND	GND	**32**	PCIe0_REFCLKp	Differential interface positive Reference Clock of PCIe 0
33	GND	GND	**34**	PCIe0_REFCLKn	Differential interface negative Reference Clock of PCIe 0
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37	PCIE1_RXN	PCI Express receive serial data. Differential interface negative leg of lane 1	**38**	GND	GND
39	GND	GND	**40**	RESET for CPLD	RESET for CPLD
41	3.3V	3.3V	**42**	SD_CMD	Command for micro SD Card
43	SD_CLK	micro SD Card Clock	**44**	SD_WP	Write Protect for micro SD Card
45	3.3V	3.3V	**46**	RESET_ALL#	Globe reset from CPU board
47	CPLD_INT#	Interrupt for CPLD	**48**	RPS_INT#	Interrupt for RPS
49	TS_INT#	Thermal Sensor IRQ mask	**50**	NC	NC
51	MGMT_INT#	Interrupt for management PHY	**52**	QSFP_INT#	Reset all I2C device on I2C Bus 2
53	3.3V	3.3V	**54**	3.3V	3.3V
55	SCL1	Serial clock line of I2C-bus 1	**56**	SDA1	Serial data line of I2C-bus 1
57	GND	GND	**58**	GND	GND
59	SCL2	Serial clock line of I2C-bus 2	**60**	SDA2	Serial data line of I2C-bus 2
61	3.3V	3.3V	**62**	3.3V	3.3V
63	UART0_TX	UART0_TX	**64**	UART0_RX	UART0_RX
65	GND	GND	**66**	GND	GND
67	SD_DATA0	Data Line [Bit0] of micro SD Card	**68**	SD_DATA2	Data Line [Bit2] of micro SD Card
69	SD_DATA1	Data Line [Bit1] of micro SD Card	**70**	SD_DATA3	Data Line [Bit3] of micro SD Card

71	3.3V	3.3V	**72**	3.3V	3.3V
73	GND	GND	**74**	GND	GND
75	MDC	Management data clock	**76**	MDIO	Management data
77	Fan_SPD_CTRL	Control Fan Speed	**78**	NC	NC
79	NC	NC	**80**	SDHC_CD_B	Card Detect of micro SD Card

Table 14: Intel CPU module connector pin out

Intel Rangeley module power connector: LCU MM2554G-2*8-G1

#	NAME	Description	#	NAME	Description
1	12V	12V	**16**	12V	12V
2	12V	12V	**15**	12V	12V
3	GND	GND	**14**	GND	GND
4	GND	GND	**13**	GND	GND
5	CPU_PROCHOT_3P3	Signal of Processor Hot from Intel CPU Board	**12**	PM_V3P3_PWRGD	3.3V power good from MB
6	FP_PWR_BTN_N	interrupt Signal from MB	**11**	CPU_THERMTRIP_3P3	Signal of Thermal trip from Intel CPU Board
7	RTC_3V3	3.3V for RTC	**10**	PM_V3P3_V1P9_EN	3.3V Enable from Intel CPU Board
8	GND	GND	**9**	GND	GND

Table 15: Intel CPU module power connector pin out

5.1.2.1 DDR3 SDRAM

The Rangeley Memory Controller supports up to 64 GB. The memory controller supports a 64-bit data bus with 8-bit ECC. When only one of the two memory channels is used in a platform board design, Channel 0 must be used. In all designs, Channel 0 must be populated by DRAM devices. Within each memory channel DIMMs are populated in slot order; slot 0 is populated first and slot 1 last. If a DIMM has two ranks, the ranks must be symmetrical (same chip width, same chip density, and same total memory size per rank). If both memory channels of the memory controller are used, then both channels must be populated identically. The CPU board is used a DDR3-1333 4GB SO-DIMM.

5.1.2.2 PCIe Interface

The Rangeley has up to 16 PCIe ports. Each port consists of a Transmitter differential pair and a Receiver differential pair which are in the 1.0-Volt Core power well of the

SoC. The Rangeley supports devices with 5.0 GT/s and 2.5 GT/s capabilities.

6 IO and Connectors

6.1 RS232 Interface

- Baud Rate: s/w define
- Data bits: 8
- Stop Bit: 1
- Parity: None
- Flow control: None

6.2 Management Ethernet Interfaces

There are one single PHY on front panel PCBA, use SGMII interface from CPU module convert to 10/100/1000 RJ-45 GbE Management port. The PHY used is Marvell 88E1112.

6.3 USB Interface

The CPU contains one Enhanced Host Controller Interface (EHCI) and complies to the EHCI 1.0 Specification. The EHCI supports up to four USB 2.0 root ports. USB 2.0 allows data transfers up to 480 Mbps. The controller integrates a Rate-Matching Hub (RMH) to support USB 1.1 devices. The USB Port 1 interface is configured by the debug software to be a debug port.

7 Power/Environmental/Agency Certifications

Power	
Number of power supply	2 (default in Power 2 only)
Max. Operating power	Max. 360 (W)
Maximum power	456 watts (W) (from Power supply)
Maximum heat dissipation	Max. 1228 BTU/hr
Environment	
Dimensions (height x width x depth)	44mm(H)440mm(W) x 487.4 mm(D)
Weight	Around 9.07kg, include 2 PSU and 4 FANs
Operating temperature	0~40°C
Storage temperature	-40~70°C

Operating relative humidity	0%-95% RH
Storage relative humidity	0%~95% RH
Altitude	3,000 meters (9,850 feet)
Acoustic Noise Test Result	All FB fan modules are running at high speed: around 75.5dB All FB fan modules are running at low speed: around 59.3dB

Table 16: Power consumption and environment table

Regulatory Standards Compliance	
Regulatory compliance	Comply with CE markings per directives 2004/108/EC and 2006/95/EC FCC/IC Report Class A BSMI UL/cUL Listed Mark CCC CB
Safety	IEC60950-1 FCC/IC Report Class A EN 60950-1 FCC/IC Report Class A UL/CSA 60950-1 CNS 14336-1 GB4943.1
EMC	EN 55022/EN 55024, Class A FCC CFR47, Part 15B, Class A ICES-003, Class A CNS 13438, Class A GB9254 YDT993

RoHS Requirement		
#	**Description**	**Limitation/ ppm**
1	Cadmium/ Cadmium Compounds	80
2	Hexavalent Chromium/ Hexavalent Chromium Compounds	800
3	Lead/ Lead Compounds	800
4	Mercury/ Mercury Compounds	800
5	Polybrominated Biphenyls (PBBs)	800
6	Polybrominated Diphenylethers (PBDEs)	800

Table 17: Regulatory Standards Compliance table