Open. Together.
Fronthaul Gateway (FHG) and Converged Access Switch (CAS)

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Fronthaul Gateway Introduction

**Objective:** Consolidate multi-protocols into a common transport solution

- **Interoperable without vendor lock-in**
  - Standards based open interfaces
- **Agility via modular, µs-latency, flexible architectures**
  - Ethernet based aggregation
  - Converged protocols
- **Customized model and policy driven automation**
  - SDN controlled
- **White Box Solution**
  - Open Compute Project (OCP) design
Ethernet Solution for Fronthaul switchable/routeable

- Semi Dynamic TRP to BBU connection for CPRI links
  - Semi-Dynamic Switchable CPRI
- Dynamic TRP to BBU connection for eCPRI links
  - eCPRI switching
  - Dynamic load balancing
- Load balancing & BBU resource sharing
- Less exotic optics
- Fewer Fiber connections

Fronthaul Gateway (FHG)
- Low PHY, RoE, TSN...
- RAN specific functions
- 800 Gbps

Converged Access Switch (CAS)
- Large switch capacity 4.x Tb with TSN
- Aggregation of multiple sites
- Converged White Box
- Switching and routing functions
FHG / CAS Transport Architecture

Architecture
1. Point to Point Dark Fiber from Macro to CAS
2. eCPRI traffic switched to vDU
3. RoE traffic
4. PICO site transport CPRI over dark fiber to Hub
RoE vs Low PHY

RoE
- CPRI over ethernet using 1914.3 standard
  - Tunneling Mode
  - Line Code Aware
  - Structure Aware

Low PHY
- Convert CPIR to eCPRI
- Target Architecture
- Functional 7.2x split from ORAN Standard
Deployment Scenarios

**Target architecture**

- CAS routing capability for efficient DU pooling, load balancing
- Multiple sites connected to CAS
- Dual CASs for resiliency
- L-PHY at hub (or site) to enable LTE pooling with NR

**Combability to early step deployment**

- Direct fiber to FHG to achieve routeability to BBUs
- Rack mount at site with RoE enables co-existence of LTE and NR
# Fronthaul Gateway (FHG) & Converged Access Switch (CAS)

<table>
<thead>
<tr>
<th>Form Factor</th>
<th>Deployment Environment</th>
<th>Port Capacity</th>
<th>Switching Bandwidth</th>
<th>Power</th>
<th>Cooling</th>
<th>Environmental</th>
<th>Size</th>
<th>LPHY</th>
<th>RoE</th>
<th>Synch</th>
<th>Preferred Silicon Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>FHG-Pico</td>
<td>Pole Mount Strand Mount</td>
<td>(6) X 10/25G CPRI/ROE/ECPRI</td>
<td>200Gbps</td>
<td>AC (100 to 240 VAC)</td>
<td>Passive</td>
<td>Outdoor Enclosure NEBS 3 OSP Class 4</td>
<td>10&quot;x8&quot;x4&quot; &lt; 35lbs</td>
<td>Optional (Desired)</td>
<td>Required</td>
<td>Boundary Clock</td>
<td>1) Monterey 2) Xilinx FPGA</td>
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<tr>
<td></td>
<td></td>
<td>(2) X 25G eCPRI (1) X 100G</td>
<td>DC (-57 to -40VDC)</td>
<td></td>
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<tr>
<td>FHG</td>
<td>Tower-Cabinet Hub Site MTSo/CO</td>
<td>(18) X 10/25G CPRI/ROE/ECPRI (6) X 25G eCPRI (4) X 100G</td>
<td>800Gbps</td>
<td>AC (100 to 240 VAC)</td>
<td>Redundant Fans Front to back</td>
<td>Rack Mount: 19” NEBS 3 OSP Class 2 -40C to + 65C Ambient IP54 Front access</td>
<td>1-2 RU 19” Rack 11.8” Deep</td>
<td>Required</td>
<td>Required</td>
<td>Boundary Clock</td>
<td>1) Monterey 2) ASIC + FPGA Qumran MX Marvell Xilinx 3) FPGA</td>
</tr>
<tr>
<td></td>
<td>Hub Site MTSo/CO</td>
<td>(40) X 100G</td>
<td>4.8Tbps</td>
<td>AC (100 to 240 VAC)</td>
<td>Redundant Fans Front to back</td>
<td>Rack Mount: 19” NEBS 3 OSP Class 2 -40C to + 65C Ambient IP54 Front access</td>
<td>2 RU 19” Rack</td>
<td>No</td>
<td>No</td>
<td>Edge Grand Master (S-Plane config 3)</td>
<td>1) Jericho 2C</td>
</tr>
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<td>Hub Site MTSo/CO</td>
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## Required Standards Compliance

<table>
<thead>
<tr>
<th>Standards Specification</th>
<th>FHG</th>
<th>CAS</th>
</tr>
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<tbody>
<tr>
<td>IEEE STD 802.1CM-2018 Time Sensitive Networking for Fronthaul, Profile A (support strict priority queuing) for Class 1 &amp; 2 (CPRI and eCPRI) traffic</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>IEEE STD 802.1CM-2018 Time Sensitive Networking for Fronthaul – Profile B (support IEEE 802.1Qbu frame preemption and IEEE 802.3br Interspersed Express Traffic) on ports used as an NNI port whose date rate is not higher than 25Gbps.</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>O-RAN WG4, Control, User and Synchronization Plane Specification, for Low PHY functionality and interfaces</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>CPRI Specification v7.0 Common Public Radio Interface</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>eCPRI specification v1.2, Common Public Radio Interface: eCPRI Interface Specification</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>IEEE 1914.1 NGFI node processing time (latency) class A (&lt; 2us for 25-100GbE).</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>IEEE 1914.3-2018 Radio over Ethernet Encapsulations and Mappings</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>ITU-T G.8262.1 – Timing characteristics of enhanced synchronous Ethernet equipment slave clock</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>ITU-T G.8273.2 Telecom Boundary Clock Class C</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>ITU-T G.8273.4 – Timing characteristics of partial timing support telecom boundary clocks and telecom time slave clocks</td>
<td>Yes</td>
<td>No</td>
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<tr>
<td>ITU-T G.8275.1 – Precision time protocol telecom profile for phase/time synchronization with full timing support from the network</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>ITU-T G.8275.2 – Precision time protocol telecom profile for time/phase synchronization with partial timing support from the network</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>Ethernet Service OAM (IEEE 802.1Q/ag, ITU-T Y.1731, MEF17/30.1/35.1)</td>
<td>Yes</td>
<td>Yes</td>
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FHG: RoE ASIC + Low PHY FPGA (Optional)

RoE Configuration
- Monterey (BCM5667x) for ROE
- FPGA not required

Low PHY Configuration
- Monterey handling L2/L3 Functions
- Xilinx FPGA (KU15) supporting Low PHY
FHG: L2/L3 ASIC + FPGA

L2 / L3 ASIC
- Monterey (BCM5667x), Qumran MX, Marvell
- Handling L2/L3 Switching and Routing

FPGA
- Xilinx FPGA (KU15) supporting Low PHY
- Could be programmed to support:
  - RoE (IEEE 1914.3)
  - Low PHY

**Diagram**

- CPU: 4-core, 16G DRAM, 128G SSD
- Xilinx FPGA (KU15) supporting Low PHY
- Could be programmed to support:
  - RoE (IEEE 1914.3)
  - Low PHY

**Interfaces**
- Management interfaces
- CPRI/eCPRI
- Synchronization interfaces
- ETH, SFP28, 10G
- RJ45
- Micro USB
- 8x OTC Input/output
- 1PPS output
- IEEE-1588 Sync-E, GPS, 1PPS Timing Block
- Transport and Service OAM

**Other Components**
- PSUs (2)
- BMC
- IEEE-1588 Sync-E, GPS, 1PPS Timing Block
- Transport and Service OAM

**Airflow Diagram**
- Front view
- Back view

**Removable FAN**
FHG: FPGA

- Xilinx FPGA (KU15) supporting Low PHY
- Could be programmed to support:
  - RoE (IEEE 1914.3)
  - Low PHY
- L2/L3 Switching
  - Could be accommodated by the CAS

FPGA

- FPGA
- CPU 4Core, 16G DRAM, 128G SSD
- IEEE-1588 Sync-E, GPS, 1PPS Timing Block
- Transport and Service OAM
- 24x SFP28
  - TOD+1PPS, Input/output
- ≥4x QSFP28
- 10 MHz Input
- 1PPS Output
- 8x OTU Input/output
- PSU (2)
- BMC
- Removable FAN

Management interfaces
- ETH Mgmt RJ45
- Craft RJ45
- Micro USB
- ≥1x QSFP28

CPRI/eCPRI
- TCD+IPPS Input/output
- 10 MHz Input
- 1PPS Output
- 8x OTU Input/output

Synchronization interfaces
CAS: Jericho 2C ASIC

Fronthaul Aggregation + Timing

- Jericho 2C (BCM88800)
- IEEE STD 802.1CM-2018 Time Sensitive Networking for Fronthaul, Profile A (support strict priority queuing) for Class 1 & 2 (CPRI and eCPRI) traffic
- ITU-T G.8273.2 Telecom Boundary Clock Class C
- ITU-T G.8262.1 – Timing characteristics of enhanced synchronous ethernet equipment slave clock