ENG. WORKSHOP:
Networking
SAI Behavioral Model
Implementation in P4

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**Motivation:** HW agnostic protocol stack

**Current state:** First integrated silicon ‘contaminates’ the protocol stack with vendor specific pipeline logic

**Solution:** Reference pipeline

SAI Behavioral Model is accepted by all SAI members

[github.com/opencomputeproject/SAI/tree/master/doc/behavioral%20model](github.com/opencomputeproject/SAI/tree/master/doc/behavioral%20model)
Current Visio doc supports the following flows:
- vBridge, .1Q UC, .1Q MC MAC based, .1Q MC IP based, .1Q&UC router, .1D rifs (subport) router, IPMC, .1Q+IPMC, VxLAN decap, VxLAN encap

Pipeline blocks example:
iPort->ACL->Bridge (vlan, stp, fdb)->eACL->ePort
Visio drawings are good means for human discussions, BUT they don’t forward packets...

Nope, you are not supposed to be able to read this 😊
P4 implementation of SAI pipeline

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https://github.com/Mellanox/SAI-P4-BM
Status: Port + Bridge is implemented, Host Interface is next
SAI behavioral model (P4)

SAI to P4 API wrappers (C++)

PTF

User (Direct Include of sai.h)

Thrift (RPC-handler) Includes sai.h

SAI lib (C)

SAI C++ layer

C++ Thrift client

BM Thrift server

“Soft Switch” compiled P4 model

Linux veth interfaces
Milestones

Port, Bridge, Host Interface, Router, Buffers, QoS, ACL, Tunnels,

Certification program?
P4 1.1.0 challenges:
Legacy pipelines may be hard to implement:
- Soft switch/ Behavioral model compiler doesn’t accept same table twice, Mandates a ‘crunched’ implementation
- SAI behavioral model is built in discrete ingress/ egress model
Seems like P4.16 addresses some of these issues
What’s the end in mind?

Protocol development process:

1. Add the support to my stack
2. SAI API exist? If not, contribute a proposal to SAI community
3. P4 BM exist? If not, contribute a patch to the BM and SAI host adapter
4. Run the relevant SAI test suit on top of the SW switch
5. Port on top of the desired switch ASICs
Help!

We are looking for contributors...