A Novel, Scalable, Energy Proportional Architecture for 48V to PoL Direct Conversion

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Data Center Power Challenges

• **Data Center Energy Consumption** *(US Department of Energy Study)*
  - US data centers consumed about 70 billion kilowatt-hours of electricity in 2014
  - Total US data center energy consumption to grow by 4 percent between now and 2020
  - Efficiency improvements played an enormous role in taming the growth rate of the data center industry’s energy consumption.
  - If stayed at efficiency levels of 2010, data centers would have consumed close to 40 billion kWh more than they did in 2014

• **Higher Power Needed by Silicon Key Components**
  - CPU power demand going above 240W
  - GPU and Networking ASICs power demand above 350W
  - DDR power increase due to faster memory and higher number of DIMMs

• **More Efficient Data Center and Power Architectures are Needed**
Power Distribution Overview

12V IBA from AC Line

12V IBA from 48V Line

48V Direct Conversion Advantages

- 48V distribution current is $\frac{1}{4}$th compared to 12V with distribution losses reduced to $\frac{1}{16}$th.
- Better conversion efficiency (downstream and upstream).
- High Power Boost converter not required.
- Simpler distributed BBS maximizing server density.
- Leverage of existing Telecom infrastructure.
Direct Conversion Challenges Addressed

- 15+ Years Multiphase DCDC
- CPU VR Digital Core
- Scalability IPs
- PMBus AVS1.3
- HV Digital Direct Conversion
- High Efficiency DC/DC
- BCD Technology

New Product Ideas

New Product Concept

New IPs Development

Direct Conversion
From 54V to CPU/DDR/ASIC

Intel VR13 Fully Compliant (No Waiver)

Fully Isolated Architecture

Scalable Architecture

High and Flat Efficiency Curve

Phase Shedding and Pulse Skipping

400V Input Ready

New Architecture
New Architecture: Resonant Current Doubler

**STRG06** Multiphase Resonant Constant On Time Digital Controller 6 interleaved Cells (automatically turned on/off by load request) with PMBUS

**STRG04** 100V Full Bridge Driver with programmable predictive control for zero voltage operations in constant phase shift control

**STRG02** Single wire controlled Synchronous Rectifier able to zero voltage and zero current operations
Architecture Scalability

More Power → More Cells

- Design Only One Cell to Design a Flexible System
- Support up to 6 Cells
- Automatic Interleaving Among Cells
- Automatic Cell Turn on/off Management
- Active Current Balancing Among Cells
- Pulse Skipping Mode When in Single Cell

Digital Commands and Current Sensing

Cell #1 → Cell #2 → Cell #3 → Cell #4 → Cell #5 → Cell #6

Load

Power Level

STRG06

100W

600W

One Cell

Multiple Cell
Architecture Key Advantages

- Fully Isolated, Resonant or Non-Resonant Direct Conversion
  - 54V $\rightarrow V_{CORE}(1.xV)$, $V_{DDR}(1.2V)$, $V_{SOC}(0.8V)$, $V_{IBC}(12V, 5V, 3.3V)$

- Maximum Efficiency Across Full Load Range
  - ZVS and ZCS under any working conditions
  - Energy Proportional Management $\rightarrow$ Dynamic Cell Management, Pulse Skipping
  - No Heat Sink Required
  - OpEx savings enhances system and datacenter performance/watt

- Scalable and Flexible
  - Converter Cells are paralleled and interleaved
  - System scalability according to the load power demand
  - Variable Frequency in CCM and DCM
  - Instantaneous turn-on of resonant converters when load increases
  - Resonant or Non-Resonant Mode of Operations

- Any Digital Load (CPU, GPU, DDR, ASICs)
  - High Bandwidth to sustain CPUs’ load transient
  - Easy to design and to compensate like a Buck converter
  - Up and down reference transitions $\rightarrow$ Sink mode operations
  - Minimized noise content for closer proximity to Digital Loads

- High Power Density and Telemetry (PMBus™, AVS1.3)
Fully Isolated Option

• This Architecture Natively Supports Full Isolation
  • Controller at secondary side for direct interaction with SVI/PMBus signals from Load
  • Controller directly manages remote sense functions
  • Primary side is driven through digital isolator (when isolation is needed)

• Electrical Isolation provided by the transformer
  • No direct connection of the 48V, or -48V, input line to the load

• Safety Isolation
  • Required above 60VDC
  • 400V Input ready topology

• Optional Feature
  • If Isolation is not Required Digital Isolator can be Removed
eColumbus Design Tool

The specifications view

A fully annotated and interactive schematic

The actual view

A fully interactive BOM

A full set of analysis diagrams

A full set of commands
A complete set of software tools, HW programmers and Technical Collaterals are available to support custom application designs.

- **POWER MASTER Tool (1st)**
  - Device & Application Configuration definition
    - Security: different rights for different operators
    - NVM file (Non Volatile Memory) generation

- **NVM Flasher Tool (2nd)**
  - Allows Programming STRG06 on board in a few simple steps
  - Totally safe process since it is impossible altering the parameters by this tool

- **Technical documentation available (3rd)**
  - Detailed command sequence to support writing the NVM file by PMBUS on board in production line
## Reference Designs

<table>
<thead>
<tr>
<th>Conversion Type</th>
<th>Application</th>
<th>Output Current and Power</th>
<th>Number of Cells</th>
</tr>
</thead>
<tbody>
<tr>
<td>54V (\rightarrow) 1.8V</td>
<td>Intel VR13 CPU</td>
<td>165W TDC 360W Peak</td>
<td>4</td>
</tr>
<tr>
<td>54V (\rightarrow) 1.2V</td>
<td>VDDQ DDR3/4</td>
<td>120A - 150W</td>
<td>2</td>
</tr>
<tr>
<td>54V (\rightarrow) 0.9V</td>
<td>ASIC Core</td>
<td>300A - 270W</td>
<td>6</td>
</tr>
<tr>
<td>54V (\rightarrow) 12V</td>
<td>Point of Load</td>
<td>42A - 500W</td>
<td>1</td>
</tr>
<tr>
<td>54V (\rightarrow) 1V</td>
<td>Point of Load</td>
<td>80A - 80W</td>
<td>1</td>
</tr>
<tr>
<td>54V (\rightarrow) 3.3V</td>
<td>Point of Load</td>
<td>46A - 150W</td>
<td>1</td>
</tr>
</tbody>
</table>

Same Scalable Topology for Different Point of Load
Ideal for Power Modules Applications
Innovative Resonant Current Doubler Architecture for 48V to PoL Direct Conversion Addressing Data Center Power Needs

Fully Isolated, Scalable, Maximized Flat Efficiency (ZVS, ZCS), Energy Proportional Able to Support Any Load (DDR, GPU, ASIC)

Fully Compliant to Intel and Other Brand CPUs

Flexible Architecture Extendable to Direct Conversion from 400V Bus

Available in Mass Production Since 2016
48V direct conversion to CPU, memory or ASIC

High efficiency (ZVS, ZCS). Fully isolated, scalable and energy proportional